

HIGHLY ACCELERATED LIFE TESTING (ALT) - WEBINAR

Finding the VITAL FEW weak points faster than you imagined ...



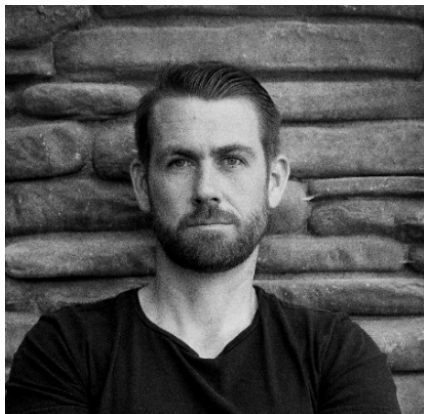
Workbook

Presented by

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Still learning

Reliability engineering is all about preventing failures occurring – like the one below ...



Depending on what phase of production we are involved in, reliability engineering might be focusing more or less on improving versus understanding the ways our product or system can **fail**.

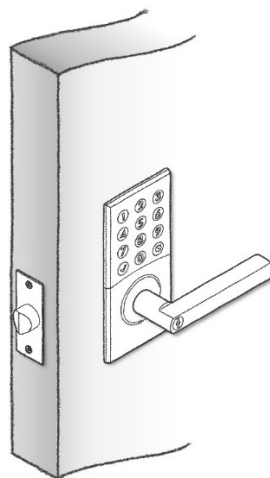
... measuring ^{or analyzing} reliability CAN be important ...

... but not nearly as important as **DESIGNING IN RELIABILITY** ...

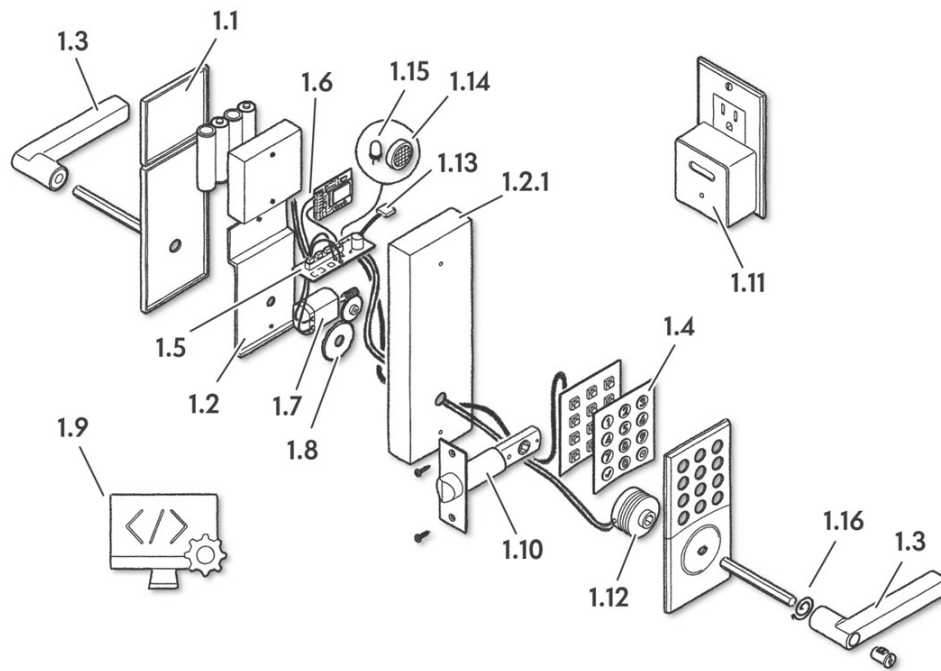
Reliability engineering happens when we incorporate simple and effective design characteristics from the very start. Every problem (no matter how technologically complex your 'thing' is) has a range of solutions. The cheapest and easiest are ALWAYS those that can only be solved using a design characteristic **BUILT INTO YOUR FIRST DESIGN**.

It is only when you are forced to redesign something without 'affecting' other components that fixes become complex and expensive.

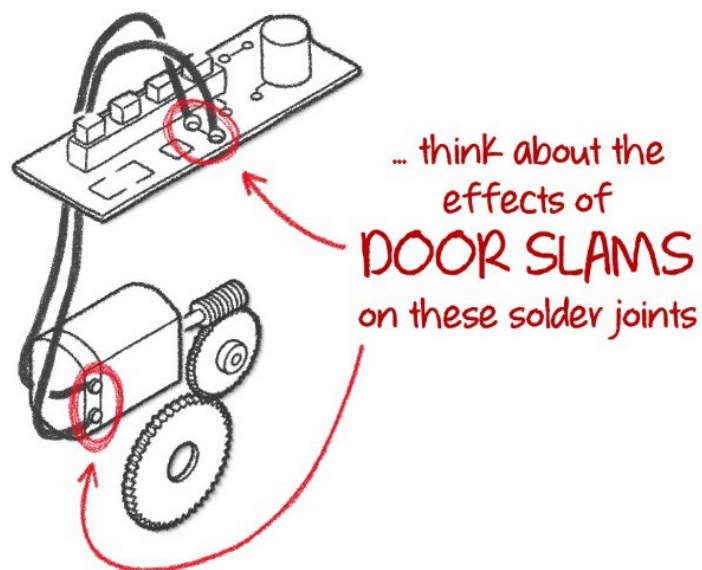
Think about a smart lock, which combines traditional 'mechanical' lock technology with contemporary 'smart' technology.



At the heart of the system is an electric motor controlled by electronic circuitry to transition the lock to or from a locked or unlocked state. Electric motor failure is 'critically bad.'



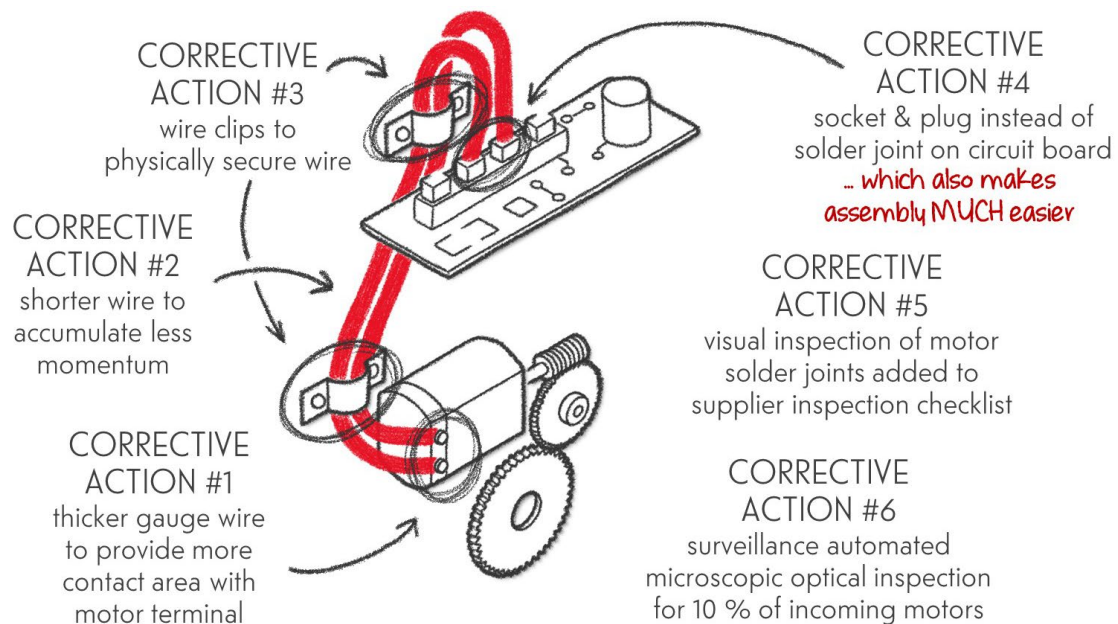
When we design something that is 'novel' or 'cool' we can often overlook the simplest of things. Like electric cables that connect the electric motor to the Printable Circuit Board (PCB). A **BUILD-TEST-FIX** approach means building a prototype that uses soldered cable that is not resilient to shock loads that are generated when a user or customer slams the door shut.



Perhaps qualification testing will uncover this critical design flaw ... as our lock needs to be able to withstand multiple shock forces when the door it is installed on is slammed (which a significant number of our future customers will no doubt do.) Unsecured cables in our smart lock that are only physically restrained with solder is a recipe for failure.

But instead of doing that, the smart lock's design team did 'smart' reliability engineering and perhaps conducted either a **FMEA** or a **FMECA**. The key outputs are a set of **corrective actions**

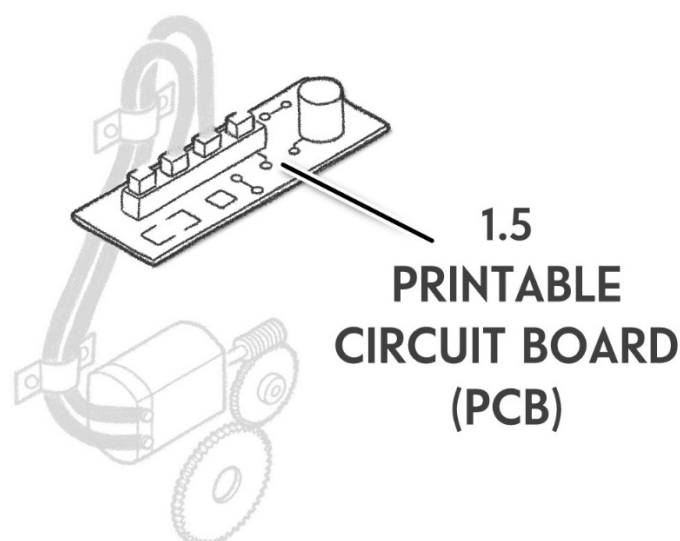
that address the design, manufacture, maintenance or anything else that can improve reliability. And look how simple and inexpensive they are.



None of these design changes are complex or expensive as long as they were thought of at the start. Which is something that a **BUILD-TEST-FIX** approach can't do. **This is how we make reliability happen.**

... but we can't PREDICT EVERYTHING

Let's say that during our initial reflection on our design, we are concerned with the robustness of the Printable Circuit Board (PCB). We don't know exactly what might break. But we also don't know what needs to happen to keep it robust and reliable.

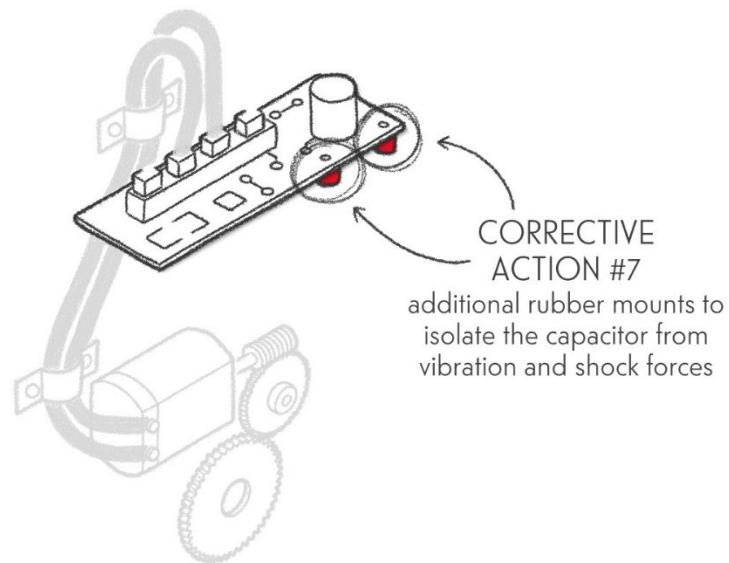


So what can we do?

We can use this activity called Highly Accelerated Life Testing (HALT). HALT is a wonderful activity that pushes components and prototypes not only to their limits, but beyond them. This forces our components and prototypes to 'break.' And when they do, we work out the VITAL FEW weak points that need to be addressed to make reliability happen.

When we conducted HALT on the PCB, several things broke (failed). One of them was the capacitor to the rear (the large, cylindrical component). The capacitor broke free from vibration that the HALT procedure was exposing to the product. And that means we have a problem.

Fortunately, there are lots of potential solutions to this problem.



And our smart lock is now even more robust and reliable.

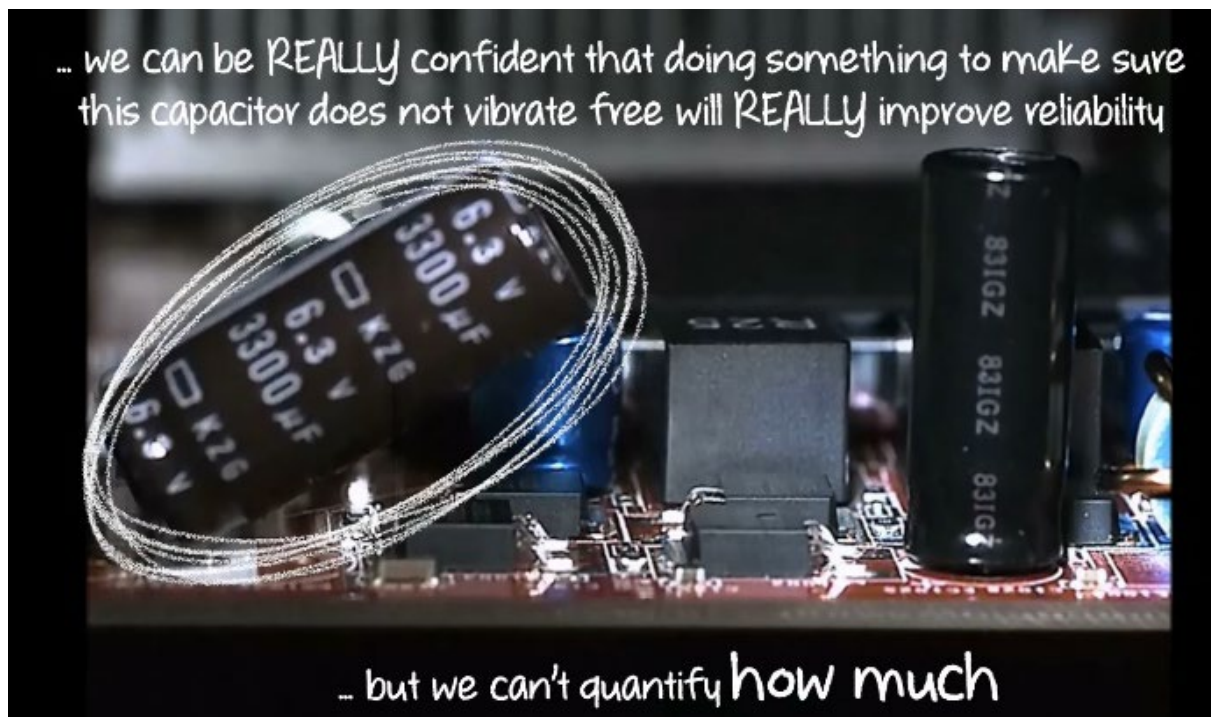
so what is HIGHLY ACCELERATED LIFE TESTING (HALT)?

A well-known example of test that are focused on improving reliability is **Highly Accelerated Life Testing (HALT)**. A Qualmark Typhoon 4.0 HALT chamber is illustrated below.



The chamber contains a table upon which systems and components can be secured and then subjected to random vibrations (with six degrees of freedom) up to 75 g RMS. It can also rapidly cycle temperature between 200°C to -100°C. The temperature cycling simulates cycling stresses as adjacent components have different coefficients of thermal expansion.

A circuit board that is being subject to **HALT** is illustrated on the right. A capacitor has just dislodged. The idea is that vibration and thermal stresses are increased systematically until the first failure is observed.

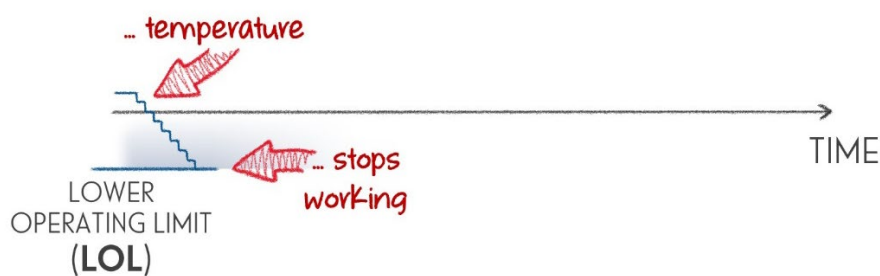


The system is then repaired, and testing continues until a prioritized list of likely failure mechanisms emerges. Or ... the **VITAL FEW. HALT** involves increasing well known stresses in a controlled, but not scientific way. We keep increasing the stress to identify **WHAT** will break. This can help us then understand **HOW** our product will fail. **HALT** can't measure, it can only point us in the right direction.

what is a HALT PROFILE?

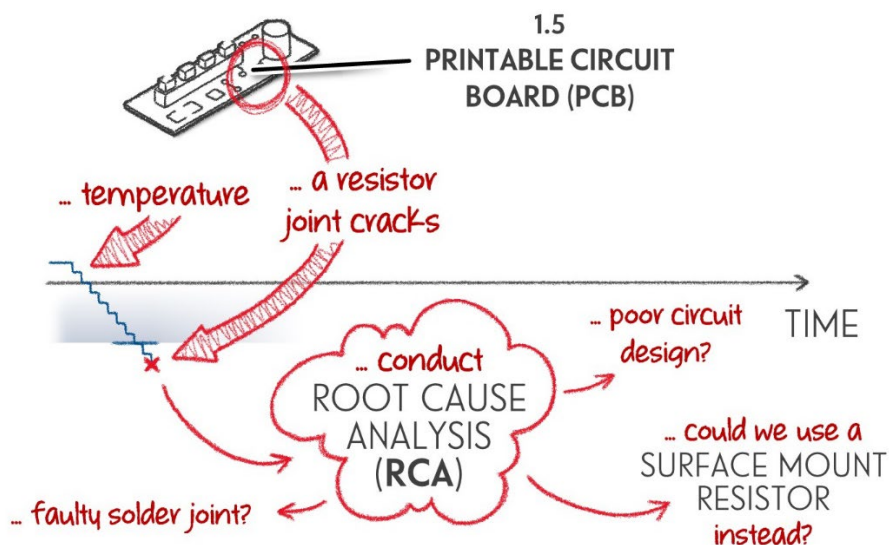
Let's also say that we have decided to subject a prototype PCB to HALT. We can't just 'put it in the chamber' and turn it on. We need to come up with a plan. And this plan is often represented with a thing we call a 'profile.'

The profile maps out how we intend to apply stresses to something being tested. For example, we might start with mapping out a 'cold thermal step stress test' where we subject our product or component to increasingly cold temperatures. Eventually, our PCB might stop working. We call this the Lower Operating Limit (LOL). The amount that the temperature drops for each step is usually around 10 ° C.



The LOL refers to the cold temperature where if our PCB is allowed to warm up again, it will work. During testing, we can have the PCB wired up or connected to another device to work out if it still works. This 'test bed' might be designed specifically for the PCB, or it can be a more generic device that tests for certain levels of functionality (like conductivity, resistance, capacitance and so on). Once we have identified the LOL, we then keep testing to see how much it can endure before something breaks.

When it breaks, we stop the test, do a basic Root Cause Analysis (RCA) that will either immediately come up with Corrective Actions (CAs), or can provide advice for other people to come up with CAs.



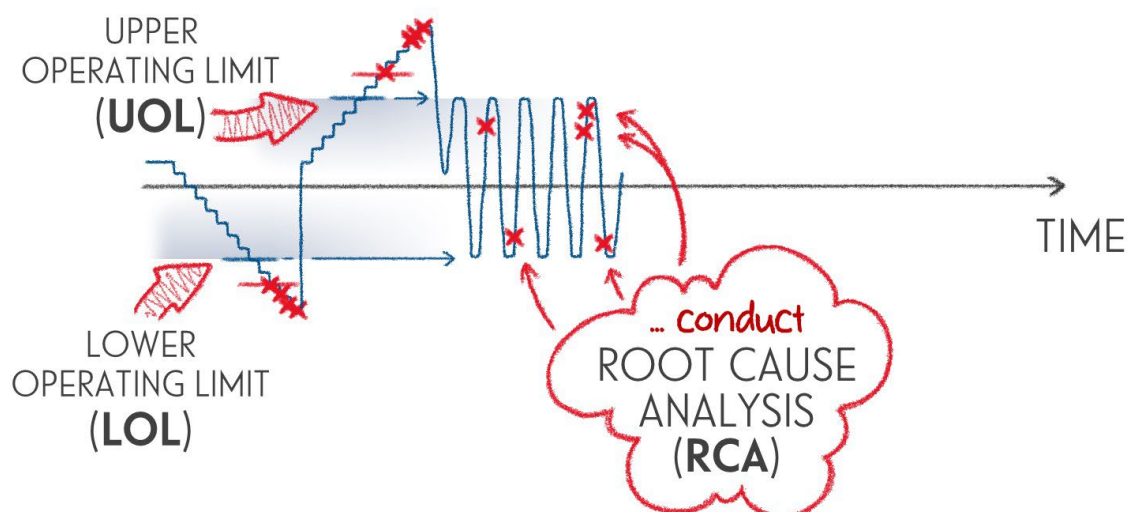
We can then 'patch up' the PCB and keep testing. The cold temperature at which we experience that first failure is the Lower Destruct Limit (LDL).



We would obviously see several more failures before we decide to stop that part of the test. The next part of the test is the 'hot thermal stress step test' where we essentially repeat the first part of the test, but with increasing temperature.

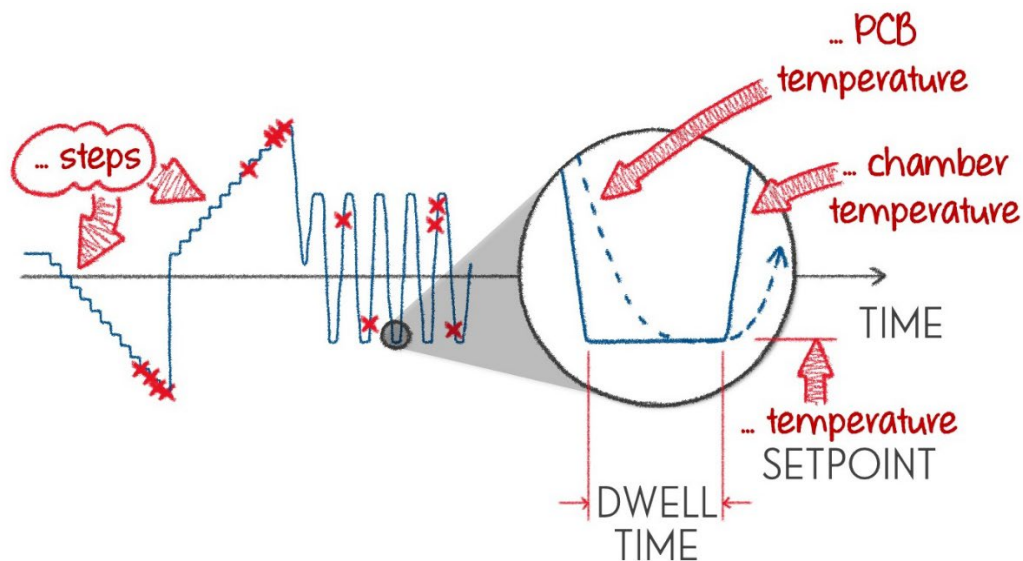


We then get two more higher temperatures that define the Upper Operating Limit (UOL) and the Upper Destruct Limit (UDL). But now we need to do something different. Instead of pushing temperature too far in either direction, we now oscillate temperatures between the UOL and LOL. This will typically induce failures that we then subject to more RCA to come up with more CAs.

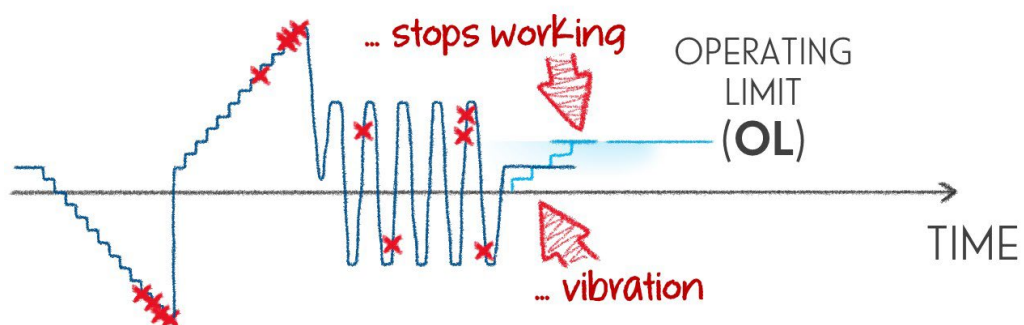


The reason we want to do this rapid cycling of temperatures is that it will force the PCB and its components to grow and shrink based on their coefficients of thermal expansion. Different component will expand and shrink at different rates. This introduces stresses and strains that mimic many of the fatigue and shock stresses the PCB will experience during its normal life. And this is how HALT will induce failure.

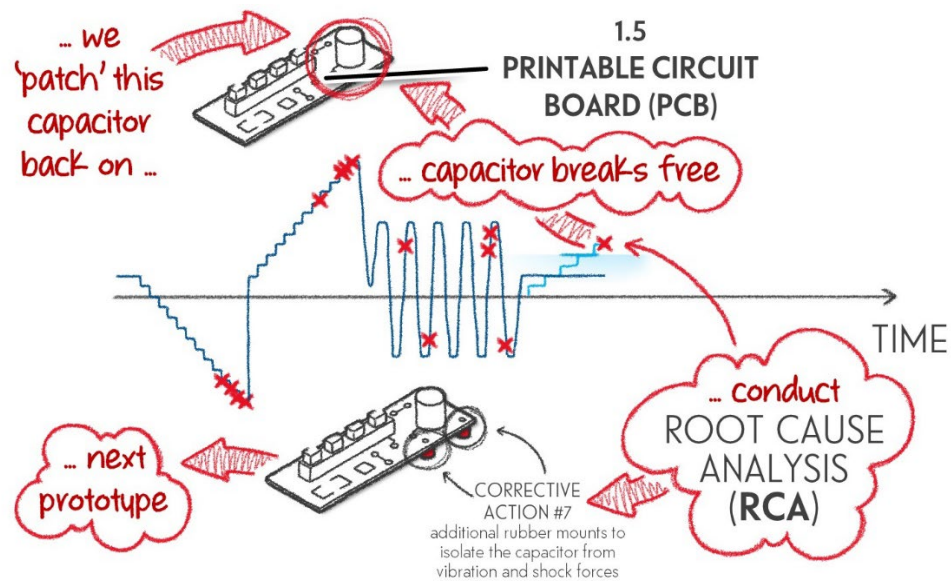
You might have noticed that in the profiles above, the temperatures 'dwell' for period of time before they change. This is called the 'dwell time.' The dwell time can last a couple of minutes to ensure that the entire PCB will reach a certain temperature.



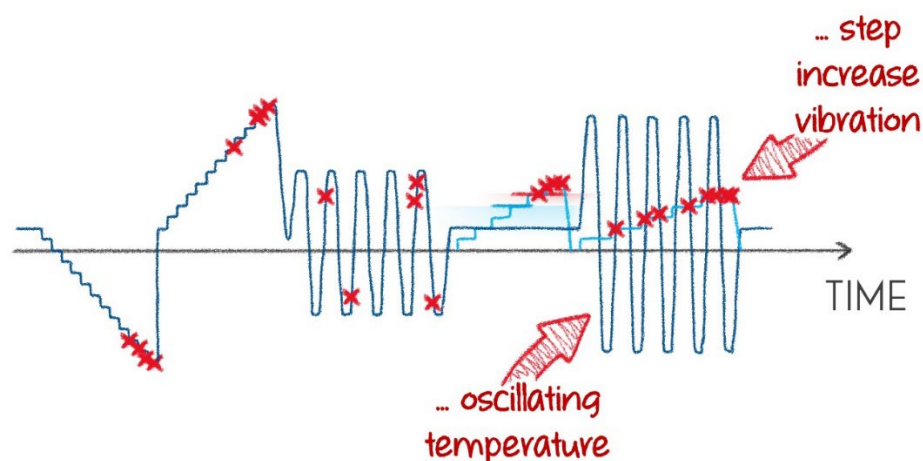
The next step of most HALT profiles stops dealing with temperature and starts dealing with vibration. So we start a 'vibration step stress test' where we increase vibration levels in steps of around 5 gRMS. The acronym 'gRMS' stands for '(earth's) gravity, root mean square.' It is a way of characterizing the amount of vibration in relation to the earth's gravitational force. We then get the Operating Limit (OL) where the PCB stops working. In this case, there is no 'upper' or 'lower' operating limit as vibration can only ever increase.



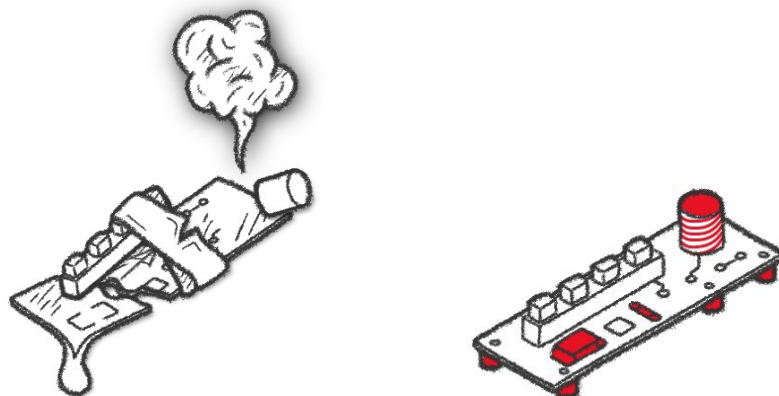
We keep increasing the vibration until the capacitor breaks free. This is the Destruct Limit (DL) for vibration.



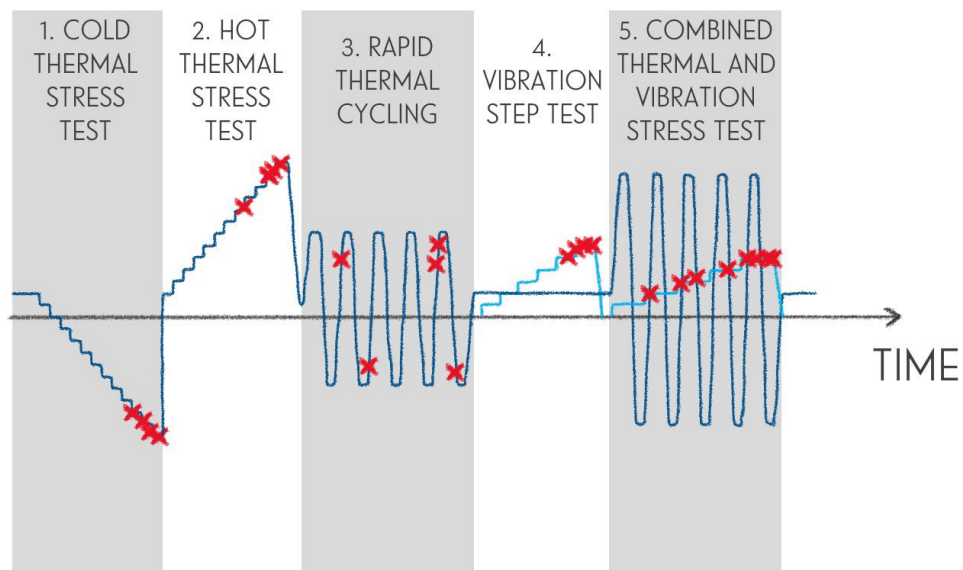
The last part of the test is to combine both temperature and vibration stresses.



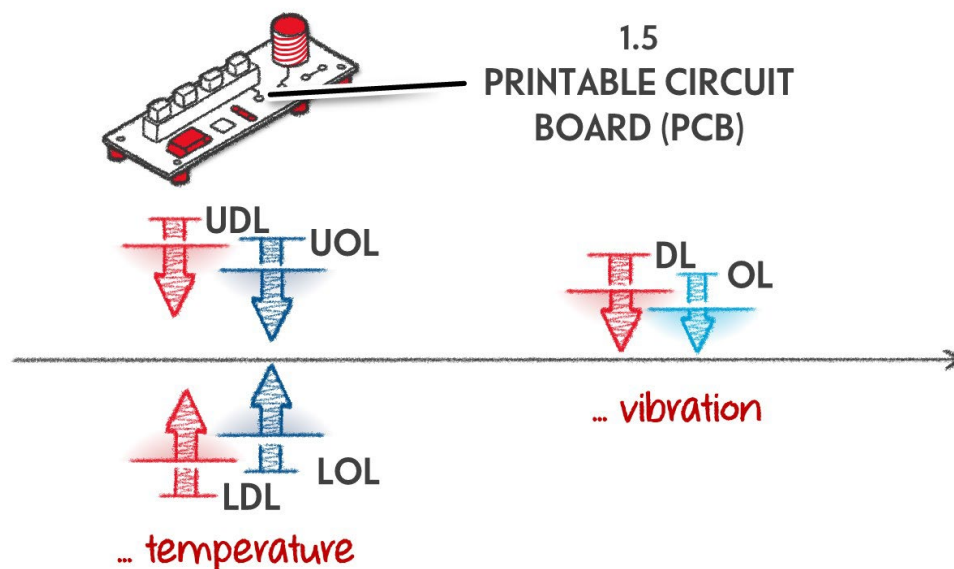
By the end of HALT, we have a PCB that is very, very broken (below left). But we now have information to create a wonderfully more reliable and robust PCB (below right).



This leaves a 'typical' HALT profile that many components and prototypes are subjected to.

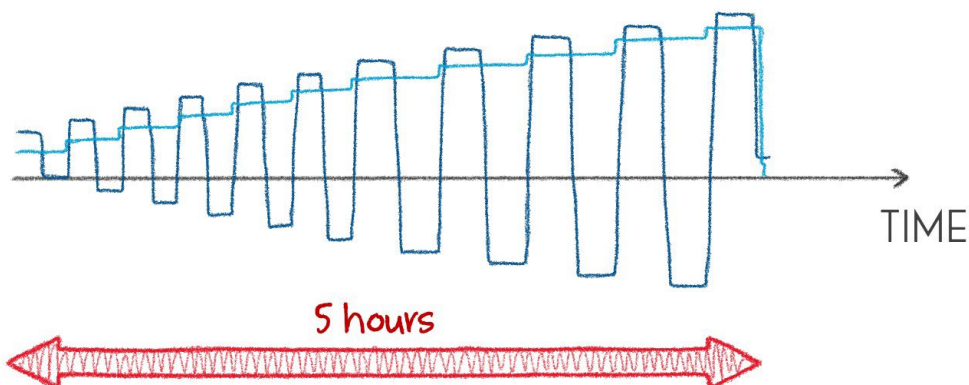


This profile has been shown through decades of industry experience. It is a very good way of identifying the VITAL FEW weak points of components like PCBs. This also means that subsequent versions and models have operating and damage limits that extend further away from use conditions. This is what more reliable and robust prototypes look like.



... HALT PROFILES are whatever you need them to be

There are lots of different approaches to HALT, notwithstanding the generic steps discussed above. For example, below is what is called a 'rapid HALT profile.' It quickly combines both thermal and vibration stresses. But because they are being combined, we don't ever identify damage and operating limits.



But these profiles are very tailored to components and prototypes that often involve electronic componentry. When dealing with other types of components and prototypes, you need to come up with different stresses and different profiles based on your understanding of likely failures. Perhaps voltage needs to be a stress. Perhaps chemical agents need to accelerate aging/life. You must always make sure the stresses (even if they are from a 'standard') align with the technology involved in your component or prototype under test.

HIGHLY ACCELERATED LIFE TESTING (HALT) is not ACCELERATED LIFE TESTING (ALT)

Accelerated Life Testing (ALT) is all about increasing a stress to decrease the **Time to Failure (TTF)** in a reliability test to understand what the **TTF** would be in 'operational conditions.' This has to be done in a 'scientific' way. We need to know what effect increasing stress has on **TTF**.

***ALT** is a term that is often used in a very generic (or 'throwaway') context.*

*Don't have time? ... we can simply do **Accelerated Life Testing (ALT)**!*

However, there are a couple of pre-requisites for any successful ALT program.

- 1. You must **KNOW HOW** your product fails. Or ... you must understand the **VITAL FEW** weak points of your system*
- 2. You must be able to **MODEL HOW** your product fails*
- 3. You must **UNDERSTAND THE CONDITIONS** in which your product will normally be used*

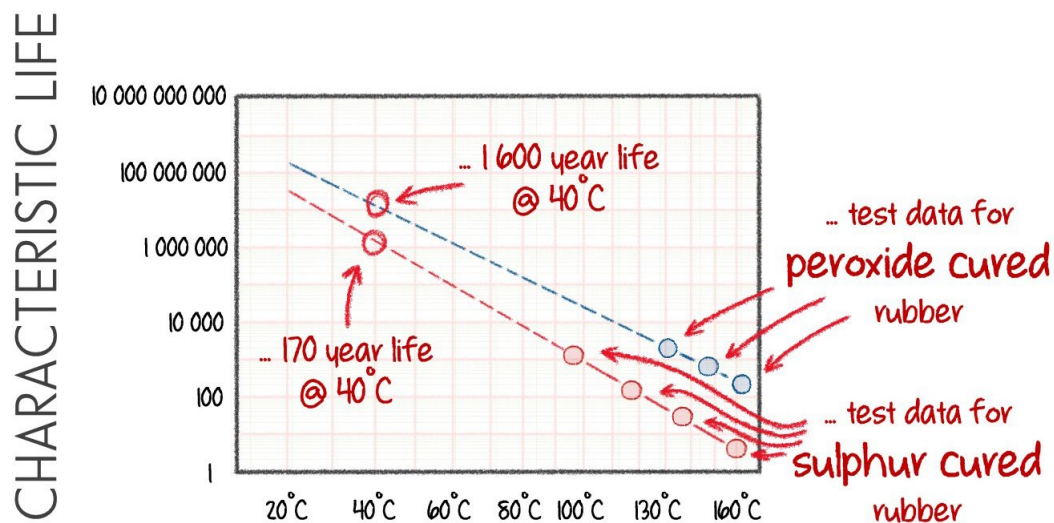
4. You must not change the **CONFIGURATION** or **STATE** of your product by increasing the stress.

The last one is very important. There is not point in increasing temperature until your product melts. This changes the state of your product. A molten product is (usually) not possible during normal operating conditions. So a test where you force your product to melt is not useful.

HALT can be very helpful in finding these failure mechanisms to be accelerated. For example, if we know that one failure mechanism is based on a chemical reaction, there are things we can do to 'measure' how long it will take before that reaction causes failure.

So to speed up the reaction, we need to give more and more energy to the **reactant**. And one way of doing this is to increase the temperature of the **reactants** which makes the molecules travel faster. Which means they have more energy.

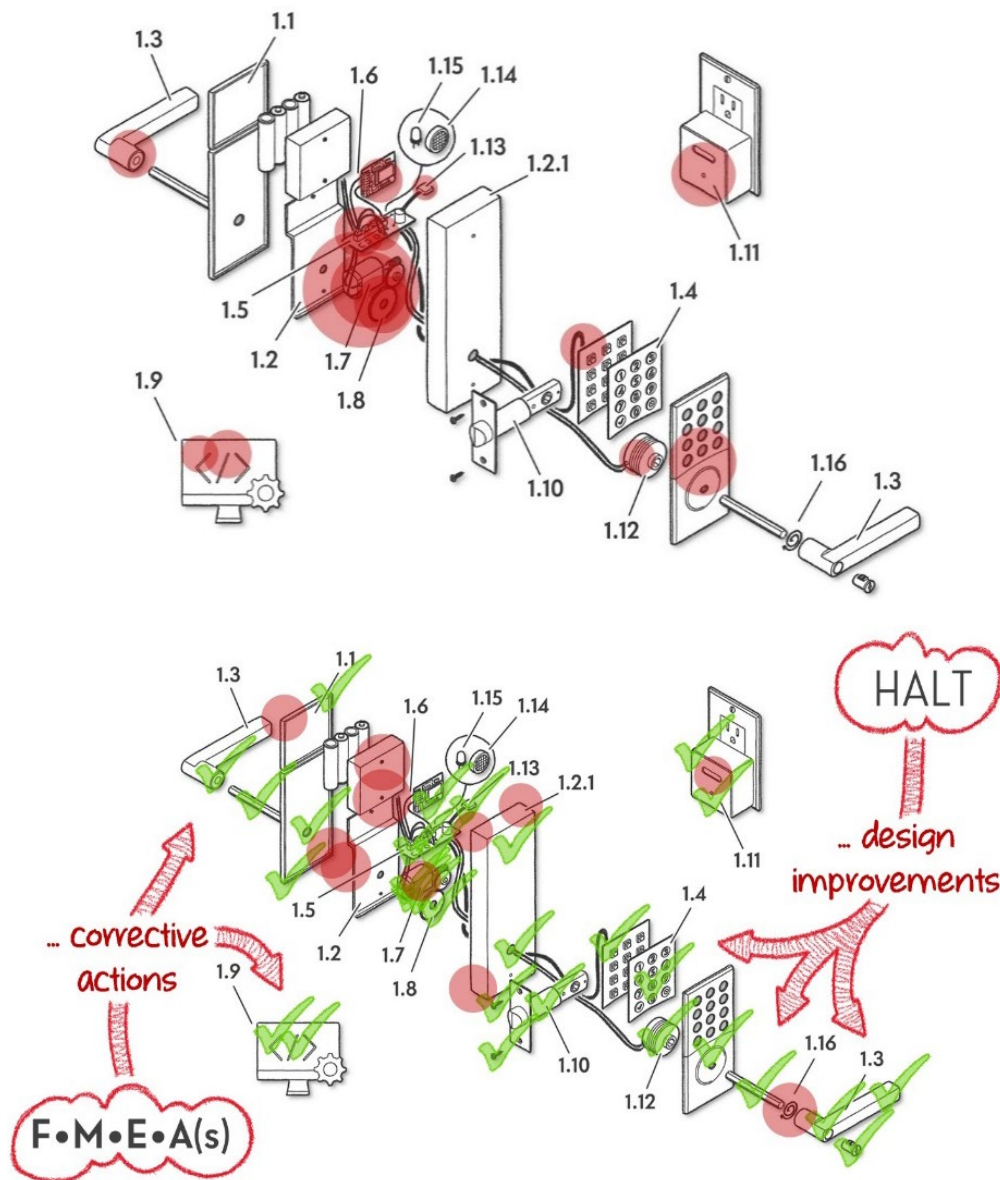
For chemical reactions, there is a well-known accelerated life chart that allows us to increase temperatures in order to project back to operational use conditions (illustrated below). The vertical (characteristic life) axis is scaled logarithmically, and the horizontal (stress or temperature) axis is scaled using a negative inverse. This allows us to compare different rubbers to help us select the one that is the most robust for our smart lock.



ALT will typically take longer than HALT. HALT can be completed in hours. ALT can sometimes take weeks. Both test regimes are very short compared to the overall production process, but clearly involve different resource costs. HALT will give you a list of the VITAL FEW weak points. ALT focuses on a very scientific analysis of one of these VITAL FEW. So even though they sound the same, they have very different roles and outputs.

IMPROVING reliability

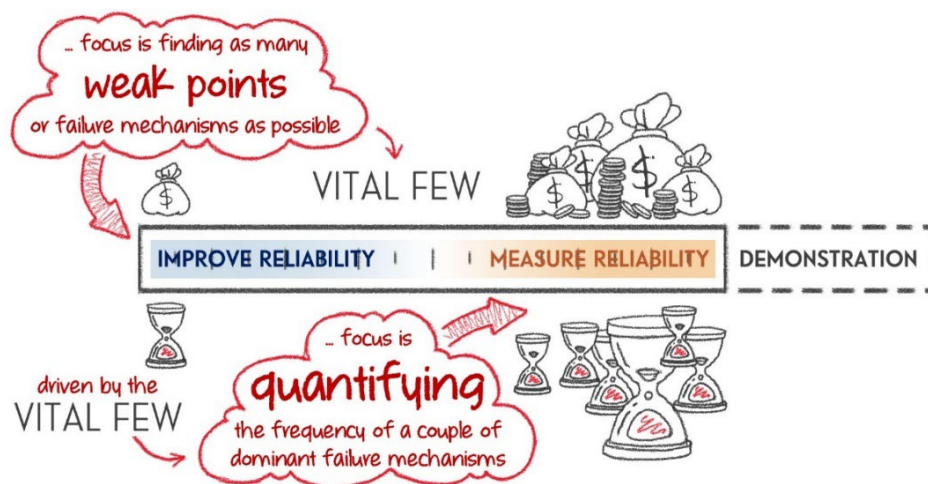
Let's also say that we have conducted a **system FMEA**, and several **design FMEAs**, to identify a prioritized list of **failure modes** and **mechanisms**. Or ... the **VITAL FEW**. They are represented with red circles in the illustration on the right. There are of course hundreds of ways our smart lock can fail, so these represent the failures that matter the most.



The first iterations of the **reliability design cycle** involve implementing **FMEA corrective actions** and design improvements based on **HALT** (and other **exploratory tests**) to efficiently improve reliability. These improvements and **corrective actions** are represented with green ticks in the illustration on the left.

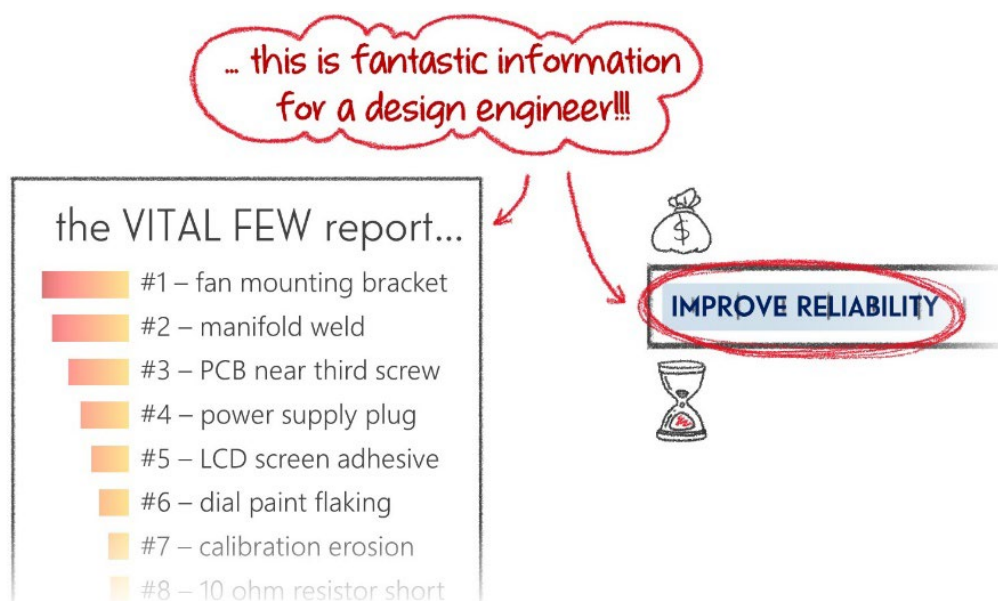
start by UNDERSTANDING your DECISION

Reliability testing typically falls on a continuum that starts at **improving reliability** and finishes at **measuring reliability**. Plenty of tests are a combination of both. One key difference is that **measuring reliability** can be longer and more expensive as it typically requires lots of (potentially difficult to gather) data.

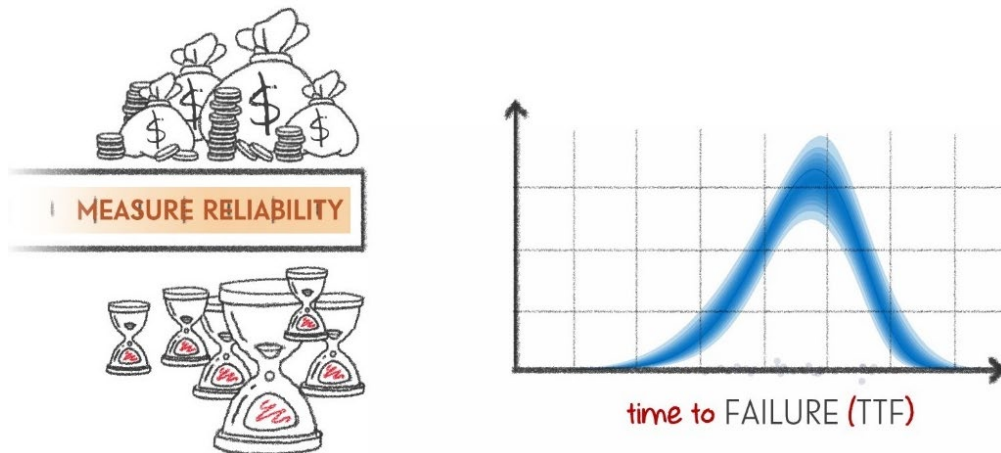


At the extreme of measuring is **demonstration**. This is categorized on its own, as **demonstration** testing typically means you test your product or system as a whole in 'use' conditions with no scope to accelerate testing. This means that any information you learned during design and other tests needs to be 'ignored.'

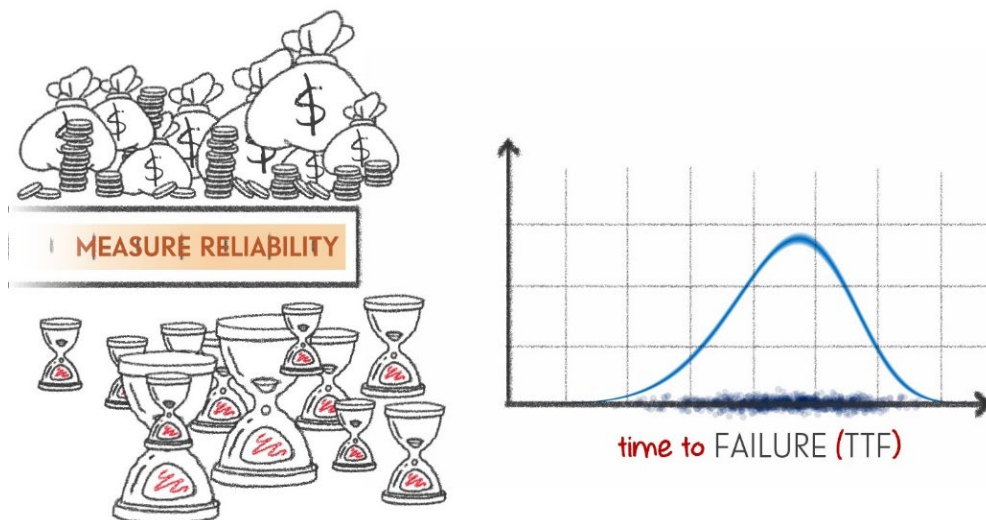
Tests (like **HALT**) that focus on **improving reliability** are all about finding the **VITAL FEW** ways your product or system will fail. This includes design weak points. This sort of testing includes **discovery** or **exploration testing** that pushes our products or systems to failure to find these **VITAL FEW**.



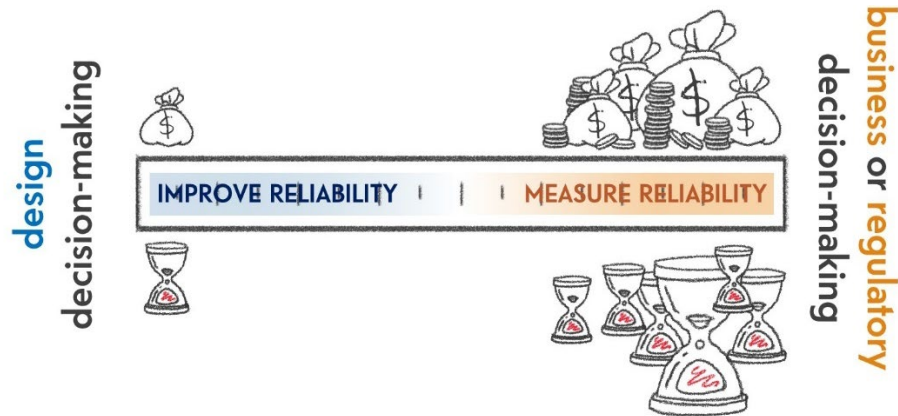
Tests (like **ALT**) that focus on **measuring reliability** where we try and understand how long it will take for the **VITAL FEW** weak points to cause your product or system will fail. These tests often involve gathering failure data. And because failure is a random process, we need to subject that data to statistical (or data) analysis.



So this means that we need to include confidence or uncertainty in the outputs of statistical (or data) analysis. If that confidence is too low, or uncertainty is too high, we need more data to give us more information. This also means we need more time and money to get that data.



So the type of test comes back to the **decision** you are trying to inform.



Many reliability engineering endeavors have been ruined before they started because people failed to understand the decision they are trying to inform. Improving reliability is very different to (and more important than) measuring reliability. If you simply measure reliability without ever trying to improve it, all you do is admire a problem. HALT is a wonderful tool for finding as many of the VITAL FEW weak points as possible that allow fast, simple and free corrective actions to 'make them go away' ... especially if these weak points are found early.

