

CHIPS

CENTER FOR HETEROGENEOUS INTEGRATION
AND PERFORMANCE SCALING

Designing Systems in CHIPS Interconnect Fabric

Puneet Gupta (puneet@ee.ucla.edu)

Sudhakar Pamarti

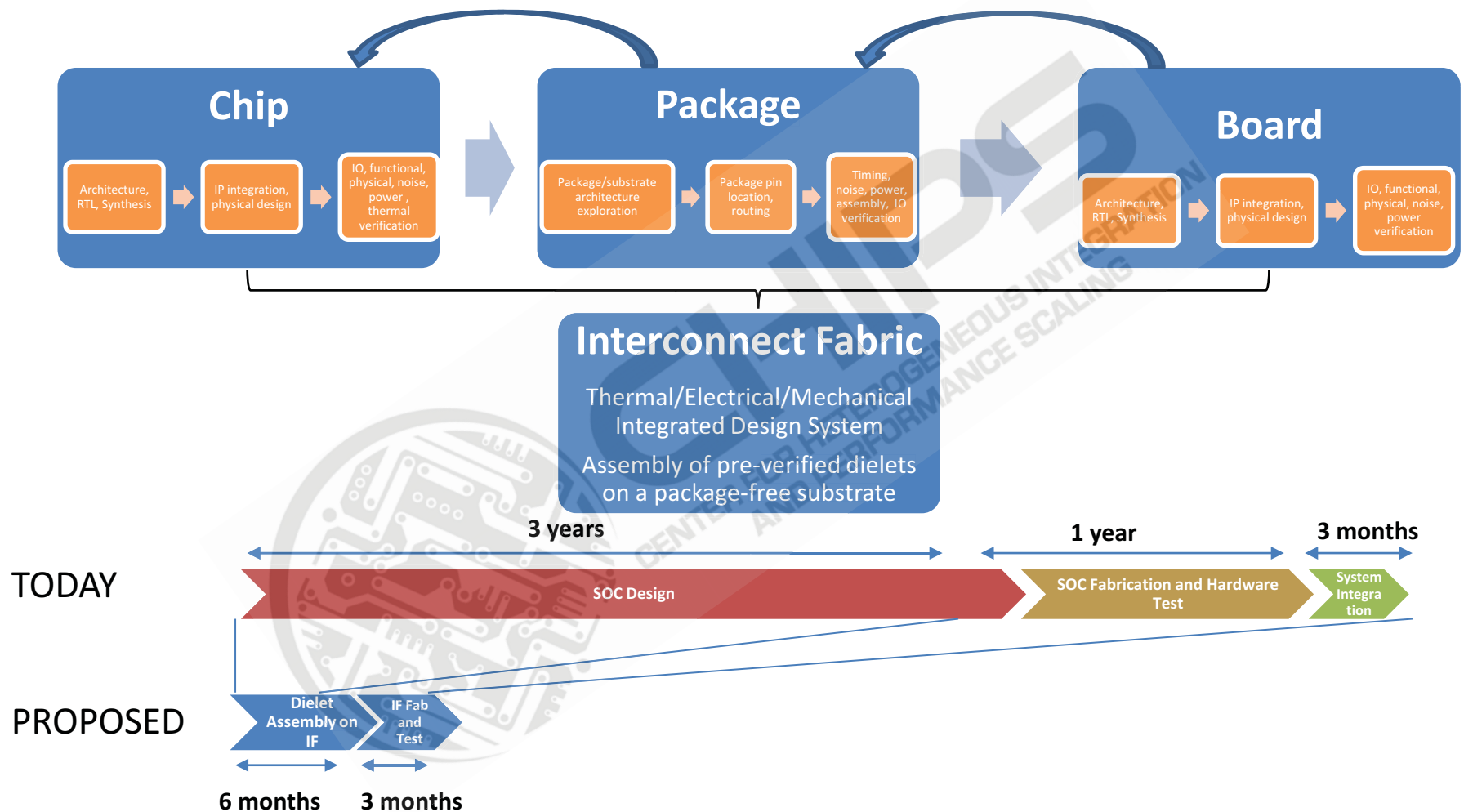
Ankur Mehta



CHIPS

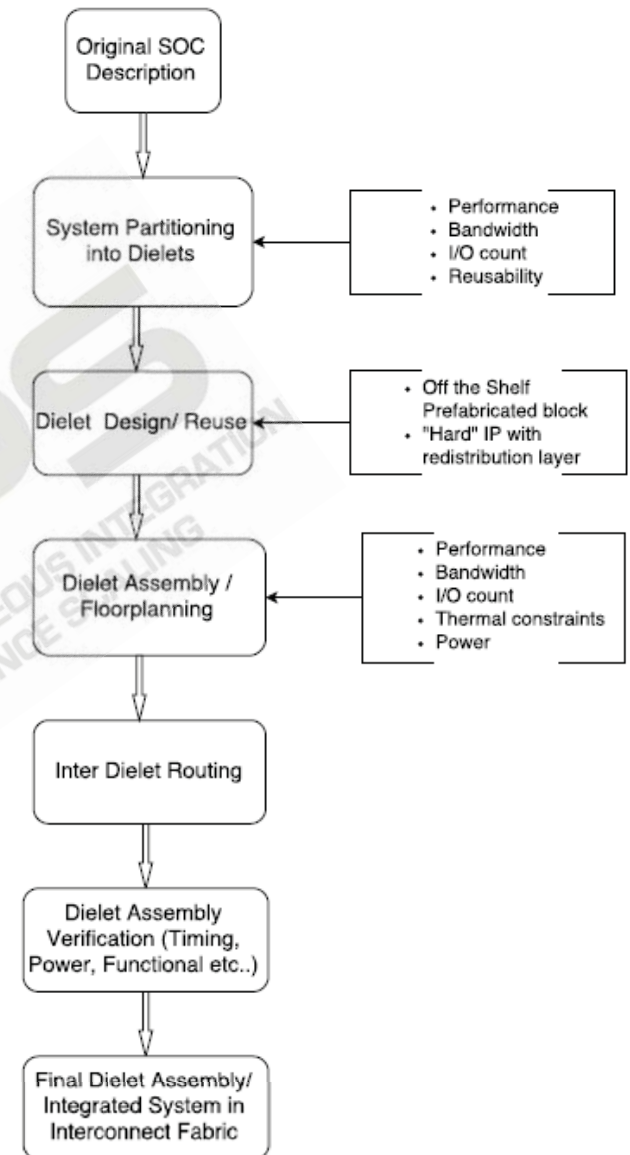
CENTER FOR HETEROGENEOUS INTEGRATION
AND PERFORMANCE SCALING

CHIPS Design System Vision



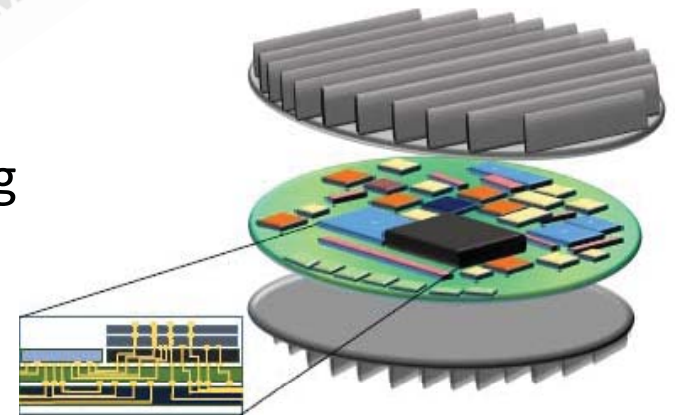
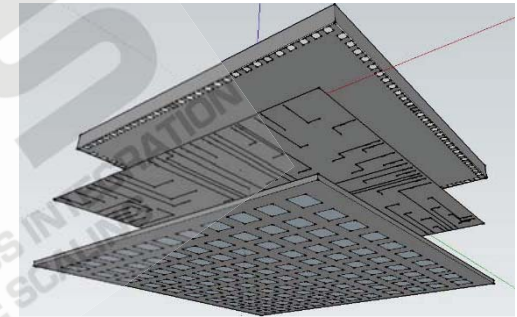
Overall SIF Design Flow

- Key elements
 - System-level thermal modeling and thermally-aware dielet floorplanning
 - Dielet assembly timing/noise/power analyses to integrate multiple PDKs (from heterogeneous dielets)
 - Resistive rather than transmission line behavior of interconnect
 - Simplified *parallel* I/Os for dielets and appropriate I/O selection
- Build upon existing SoC design infrastructure



SIF Design Components

- Dielets
 - Pre-fabricated bare die
 - Hard IP with perimeter IO
 - automated redistribution layer design
 - Discrete components
- Interconnect substrate
 - Fine pitch on rigid substrate
 - Need tolerance to unreliable bonding
 - Flexible substrate
 - Need to model flex stresses and failures



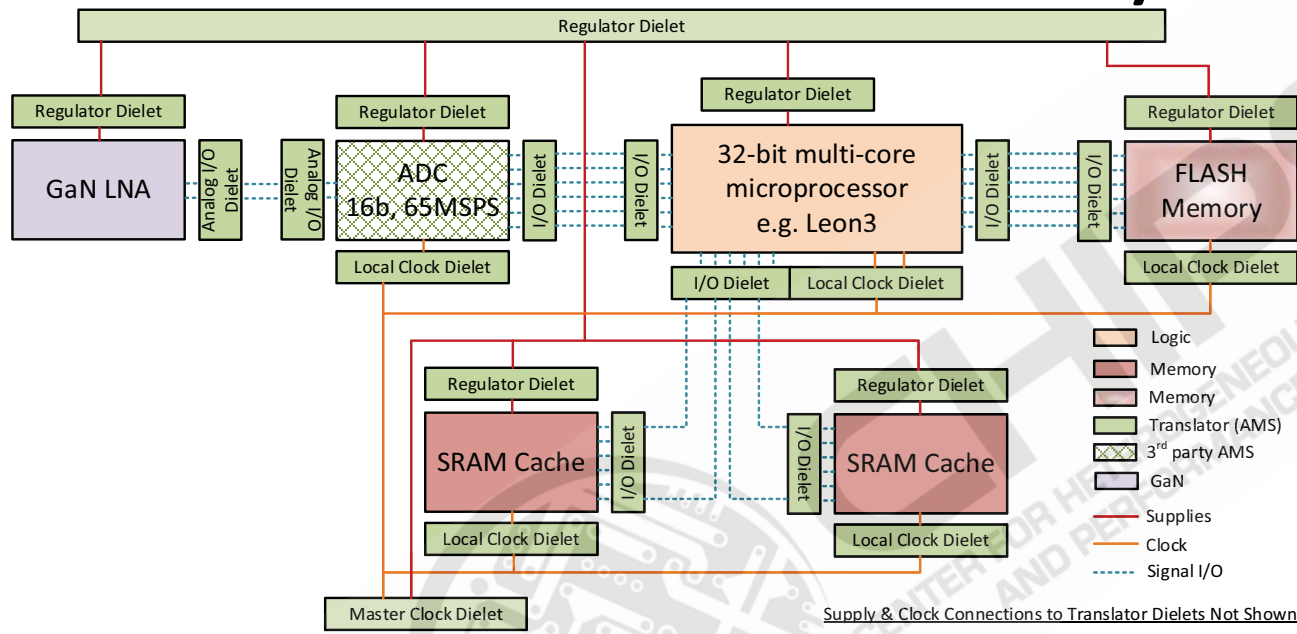
Electrical Environment in SIF

- Numerous I/Os
 - Potentially complex electromagnetic crosstalk
- Numerous supply domains to power the various dielets
 - Significant isolation/coupling concerns
- Several clock domains
 - Different frequencies and performance
 - Clock domain crossing and synchronization concerns
- Elaborate “dielet management” tasks
 - Selective sleep/wakeup of individual or groups of dielets
- Individual dielet failure – self-test, self-healing, and redundancy requirements
- Interconnect variability and resilience

Standardized Interfaces: Enabler for Fast IF-based System Design

- Physical standardization
 - pad/bump sizes, wire pitches
- Electrical standardization
 - voltage/current levels, resistive/capacitive load
- Functional standardization
 - Communication interfaces e.g., multi-Gb/s digital I/O, Z-controlled analog I/O, etc.
 - Dielet health monitor interfaces
 - Temperature, state info, error/mismatch info etc.
 - Facilitate system tuning, self-healing, self-testing
 - Control interfaces
 - Dielet configuration, etc
- Test standardization
 - Continuity tests, JTAG-like infrastructure for BIST

Active IF: Getting to Plug-n-Play Dielet Assembly



All green blocks are interface dielets
 → active interconnect fabric

Other blocks are application specific dielets (ASDs)

- Active Interconnect Fabric
 - Library of dielets to handle necessary interface tasks
 - Regulator dielets, I/O dielets, clock dielets, test dielets ...
 - Library cells available as hard IP

Eventual Push-Button SIF Design

- Secure dielet repository
 - Inventory
 - Design description (behavioral, timing views, etc)
 - Models (thermal, PDK, etc)
- A visual hardware description system
 - Easy to use, cloud hosted to proliferate use in educational and Maker communities
 - Automated dielet selection from repository
 - Automated dielet assembly and verification
- “SIF in a day” with limited hardware design background

Next Frontier: Cyberphysical Systems on IF

- Cyber-physical dielet capabilities
 - RF
 - Optics
 - MEMS
- Additional design constraints
 - Structural (SIF weight)
 - Geometric (SIF shape)
- Interdisciplinary design automation
 - Electrical + mechanical + software subsystems
- “*Robot in a day*” with limited hardware design background

