



Electromigration Studies on 6 μm Solid Cu TSV (Via last) in 32 nm SOI Technology

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Outline

1 Background – Via Last TSV Integration

2 Problem Statement (*What, Why and How?*)

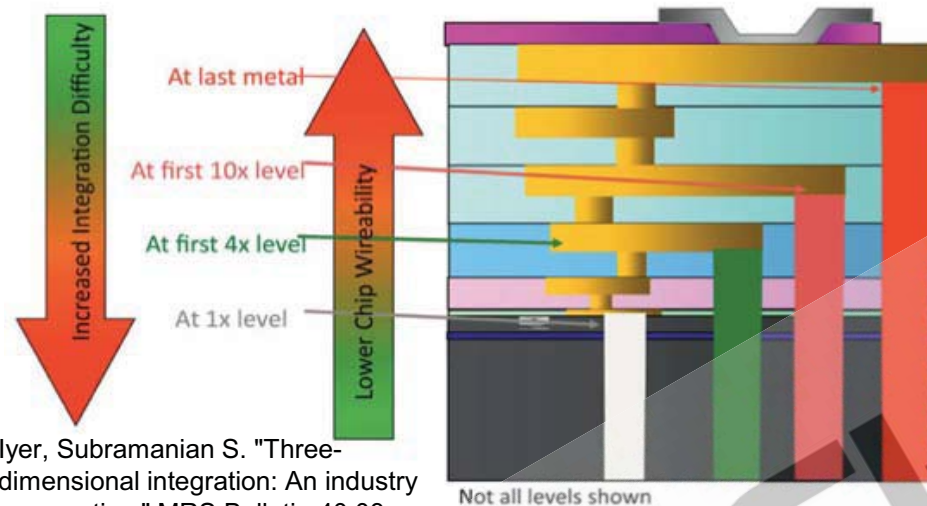
3 Experimental Details

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5 Concluding Remarks

Background: via-last TSV Integration

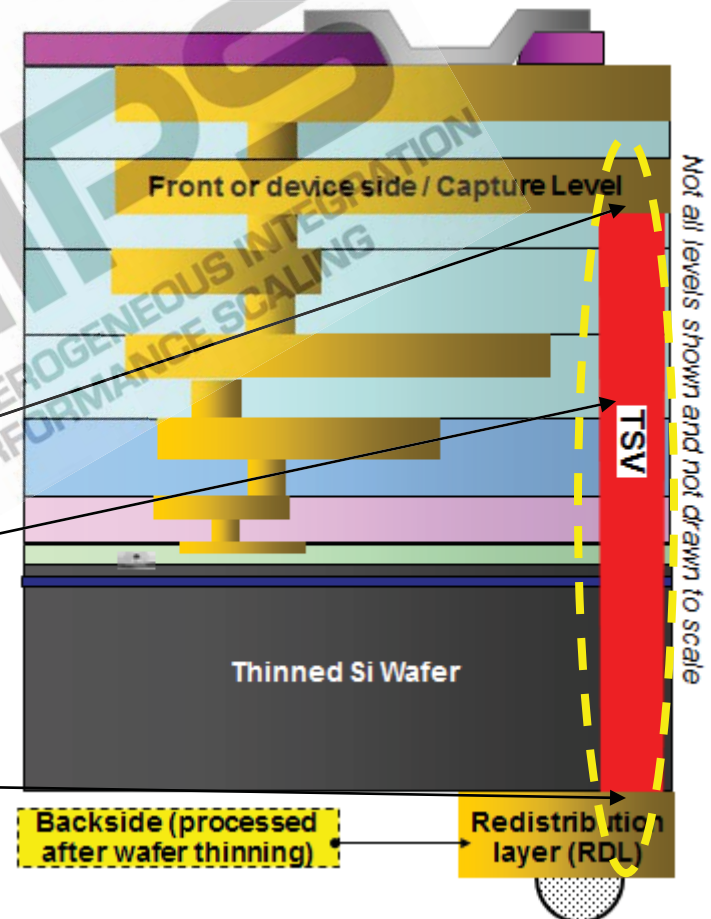
Need for via-last TSV integration



Iyer, Subramanian S. "Three-dimensional integration: An industry perspective." MRS Bulletin 40.03 (2015): 225-232

This study

6 μm solid Cu via-last TSV



Elements/links of interest in this study

- ☐ TSV/Capture Level
- ☐ TSV itself
- ☐ TSV/Redistribution layer (RDL)

What is the electromigration limited min/max. current for each of these links?

Problem Statement

What?

- ❑ *What* is the electromigration limited min/max. current for the links comprising of TSV, TSV/Capture Level and TSV/Grindside RDL?

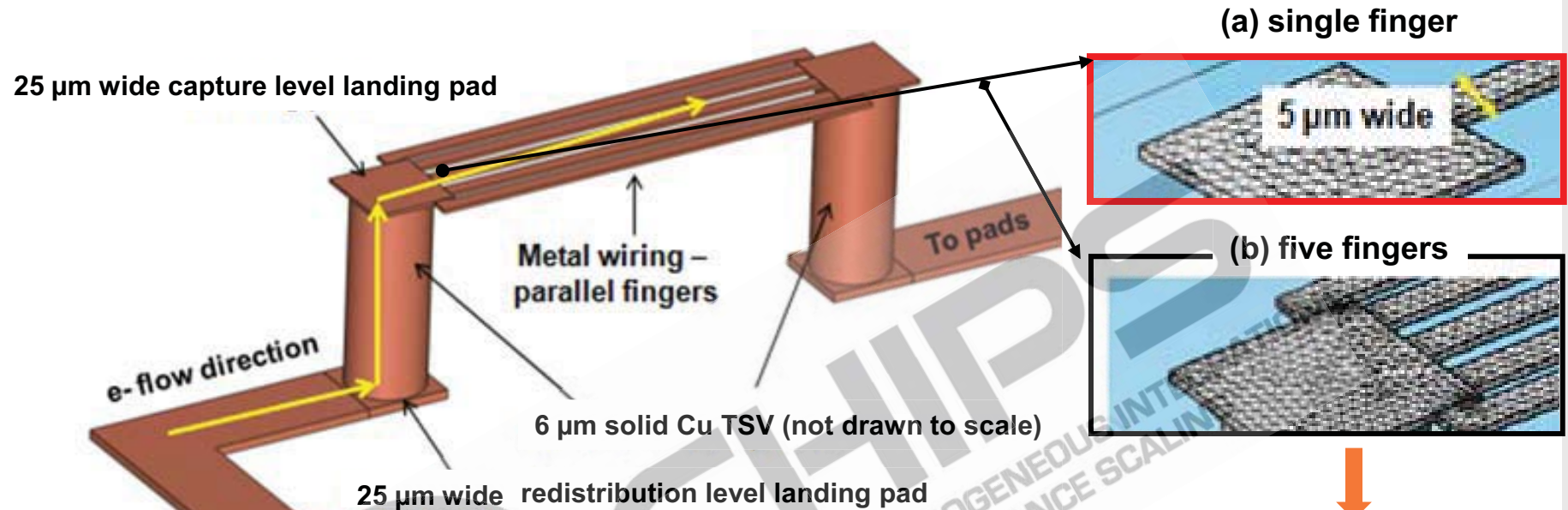
Why?

- ❑ Maximize the current loading (within the existing design) per TSV and thereby reduce the number of TSVs per chip if possible
- ❑ Aid designers and package engineers with electromigration related guidelines

How?

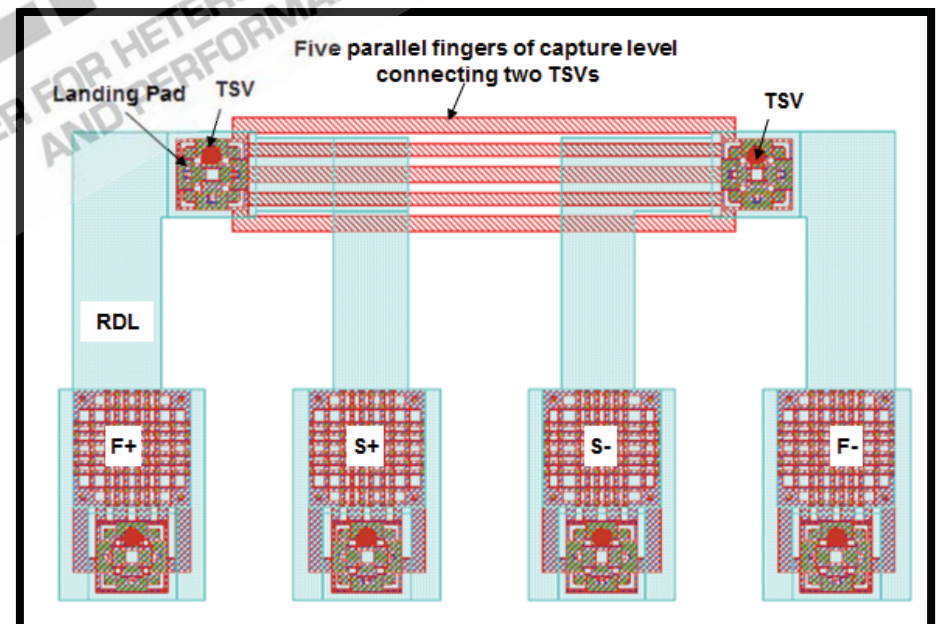
- ❑ By making each of the elements (TSV, Capture Level, Grindside RDL) in the link as the weakest in properly designed electromigration test structure to gain failure distribution

Experimental Details – Test Structures (TSV/Capture Level)

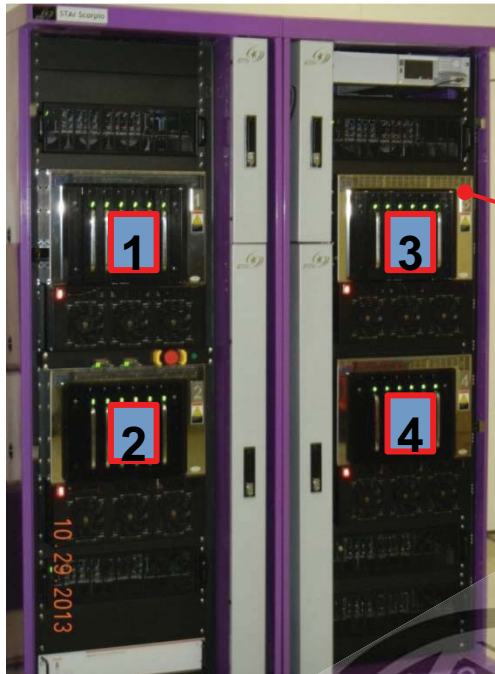


Link of interest: TSV/Capture level.
All other links are design robust

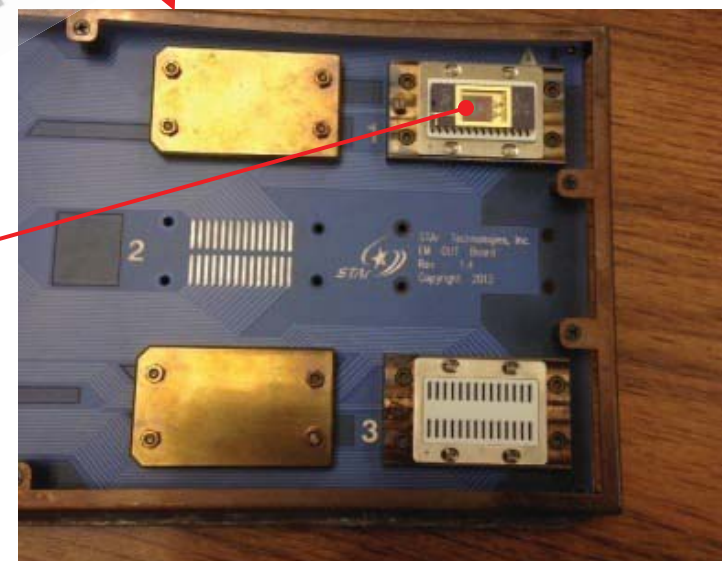
Two variations: (a) Single capture level finger vs (b) Five fingers



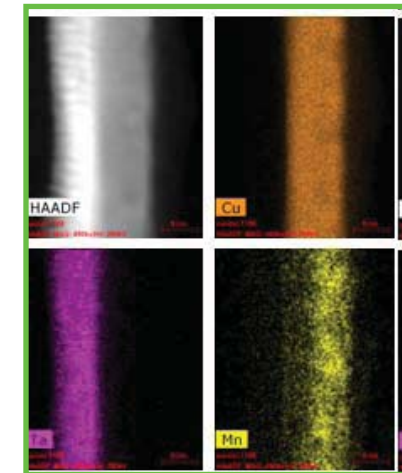
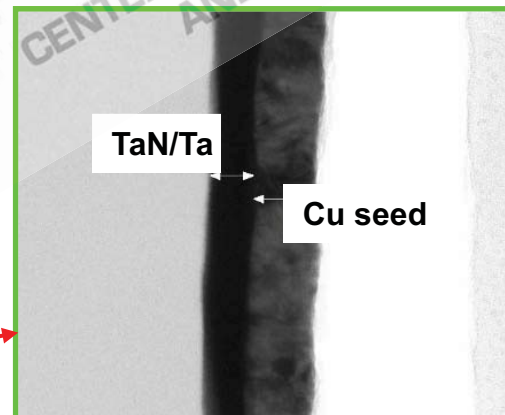
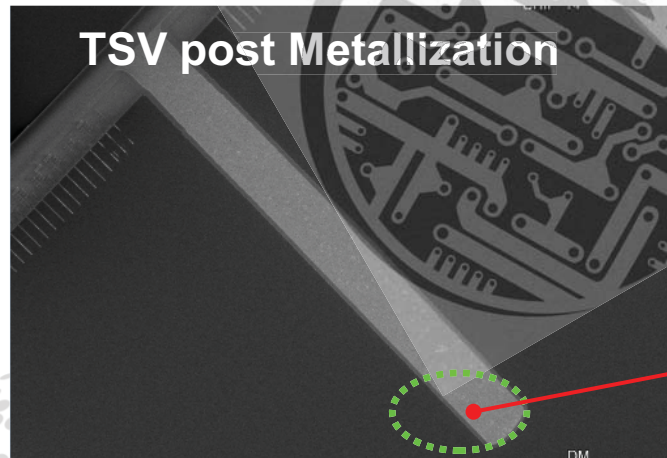
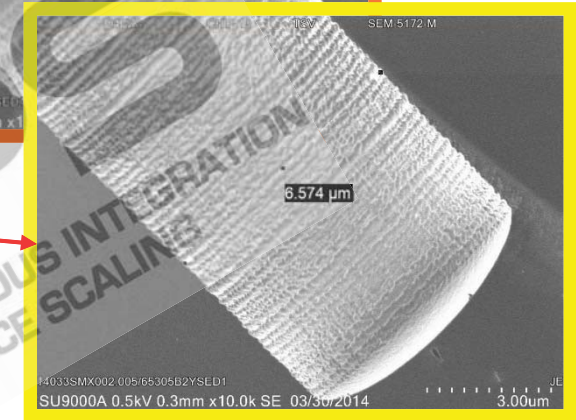
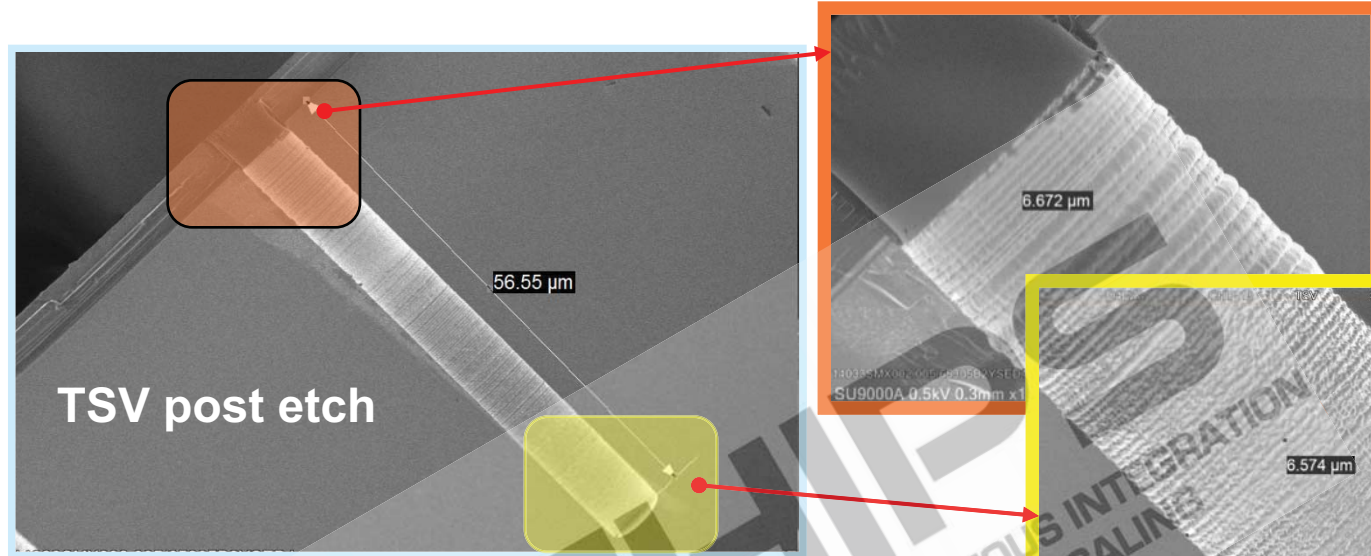
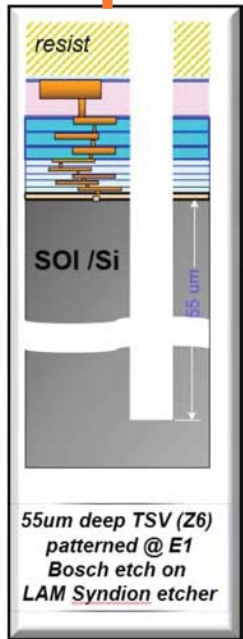
Experimental Details – High Current Electromigration Oven



Current range: $\pm 2 \mu\text{A}$ to 4 A
Temperature: 60°C to 400°C

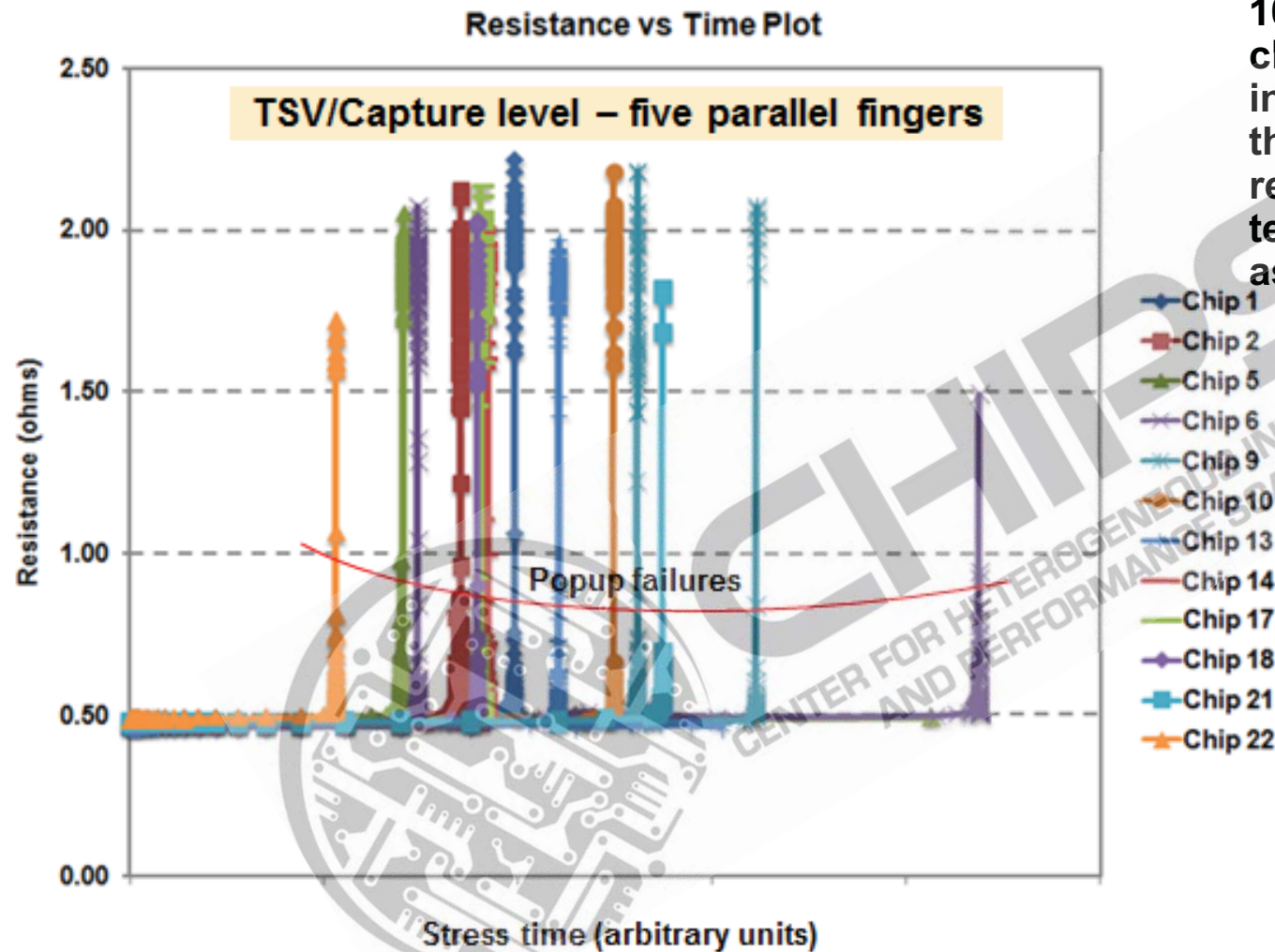


Experimental Details – TSV RIE and Fill Process



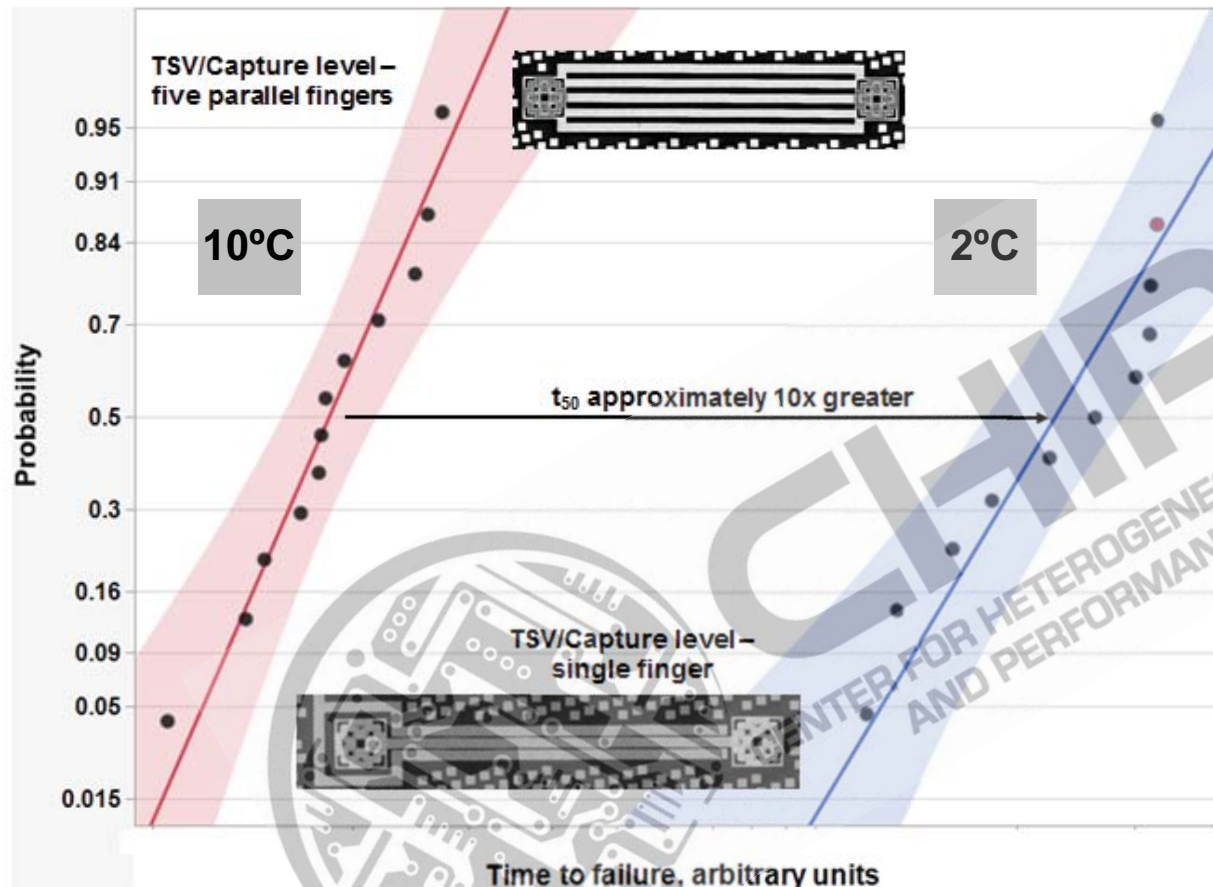
Results & Discussions – TSV/Capture Level

10% failure criteria -> chip that exhibits 10% increase in resistance than the baseline resistance at stress temperature is classified as failed chip.



Popup failures (rapid rise in resistance) → five parallel capture level fingers connecting two TSVs

Results & Discussions – Electromigration Performance (TSV/Capture Level)

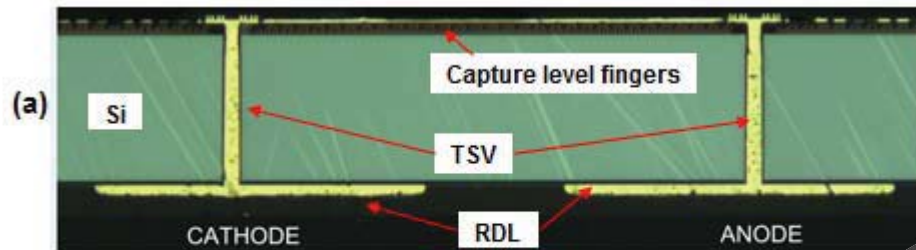


Joule heating extracted by TCR (temperature coefficient of resistance) measurements

Stress current is 2.4x times higher for five fingers (300 vs 125 mA)

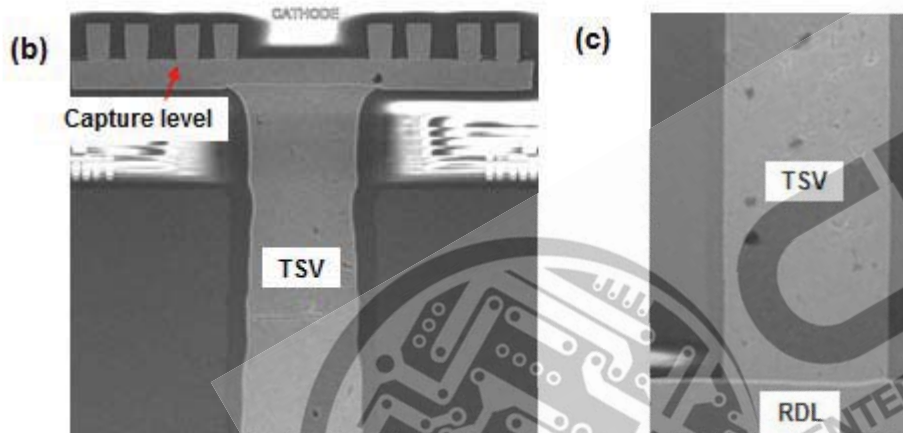
- Single finger exhibits 10x times better EM performance than five fingers capture level
- Higher joule heating in five finger indicates a design influenced current crowding (intrinsic integrity of the link is robust)
- At lower stress current as that of single finger, five finger lasted with no fail till 2700 hrs

Results & Discussions – Cross sectional Image (Single finger versus Five fingers)



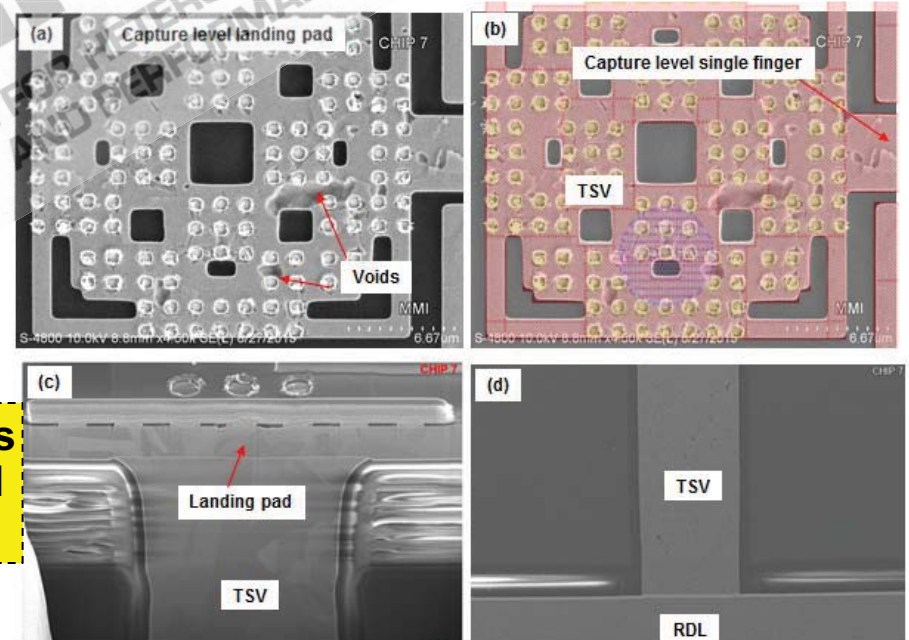
Five Fingers

No significant degradation. Few voids at capture pad and TSV

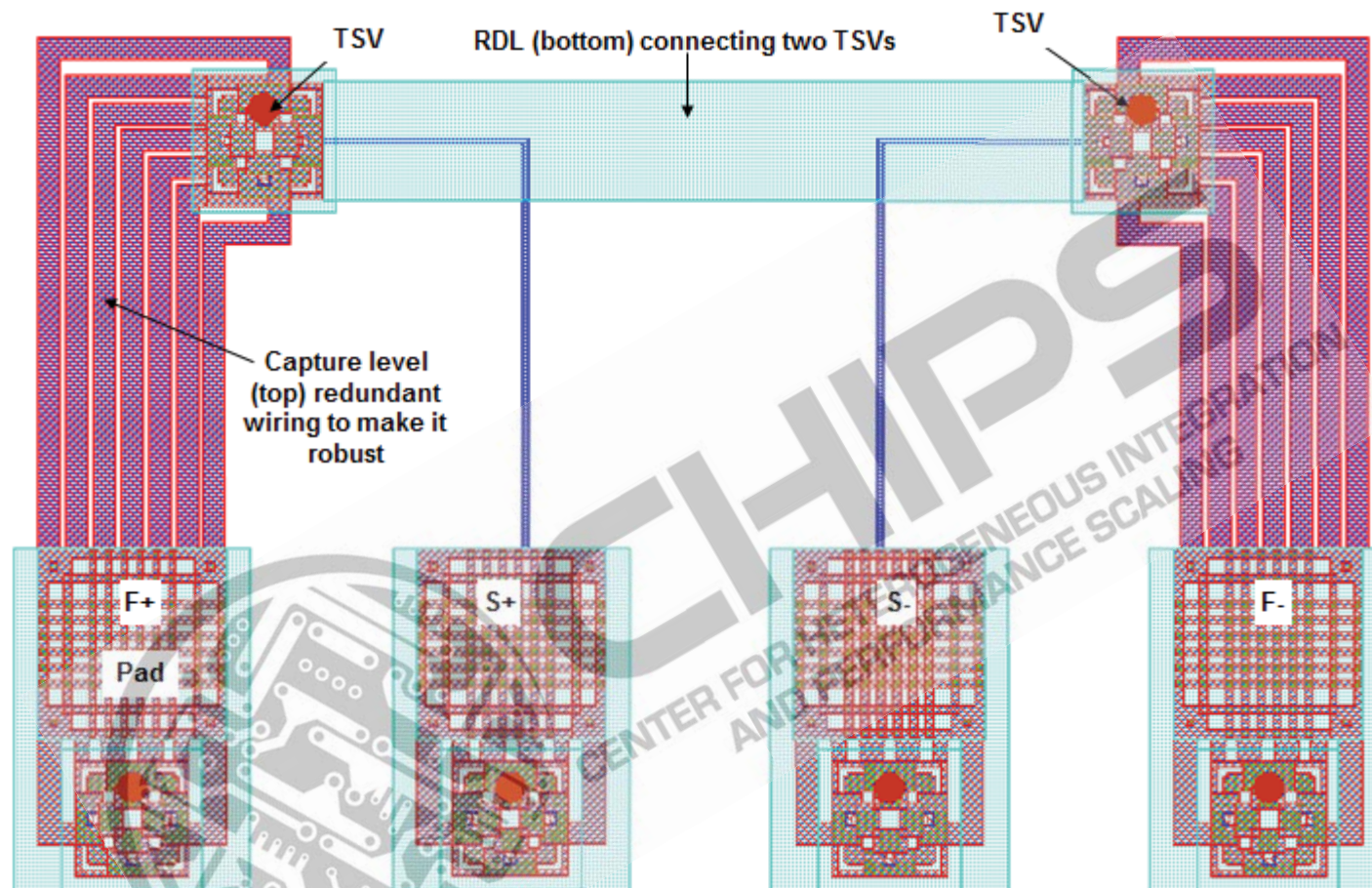


Single Finger

No significant degradation. Voids at capture pad and capture level single finger

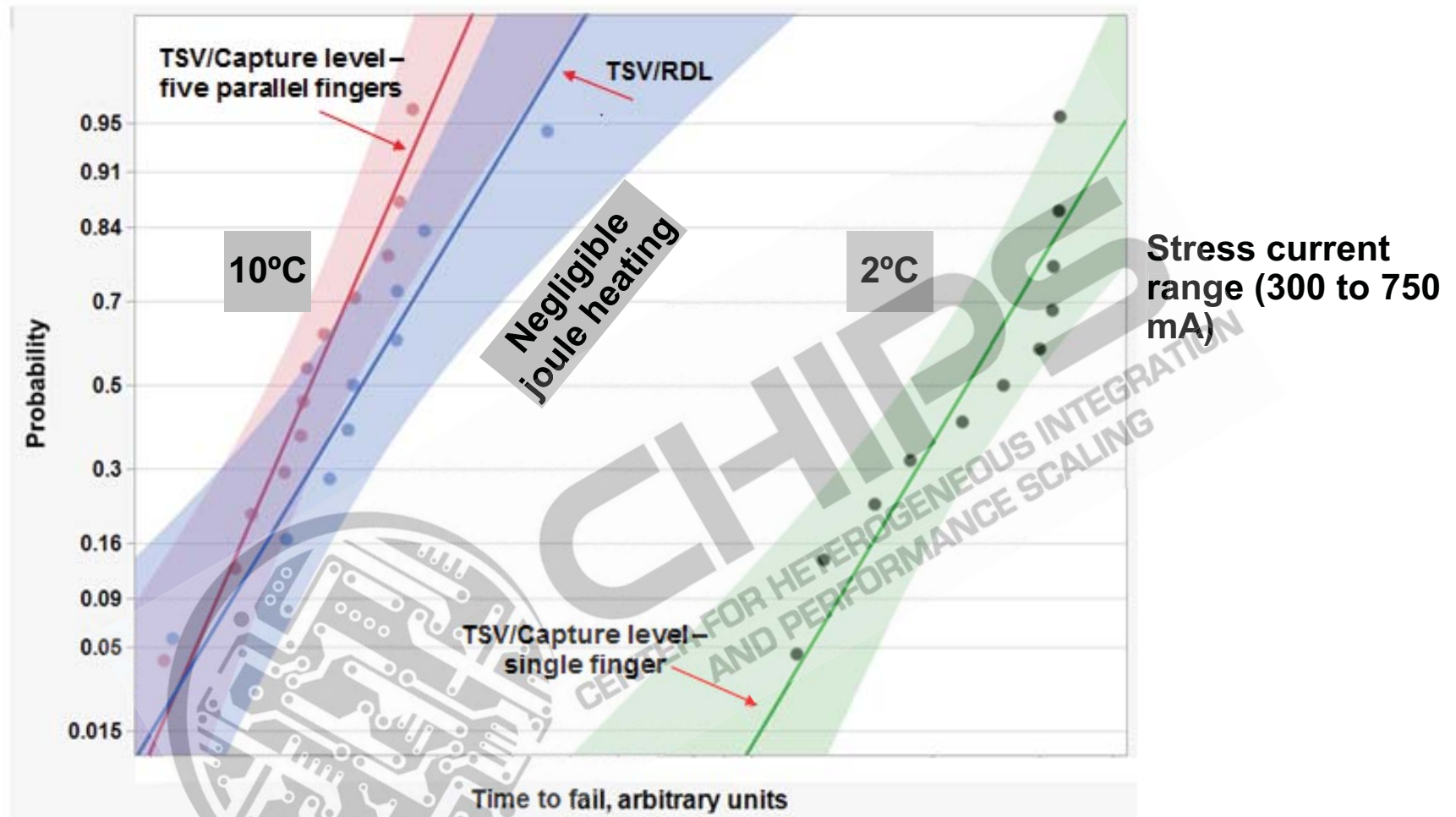


Experimental Details – Test Structures (TSV/RDL)



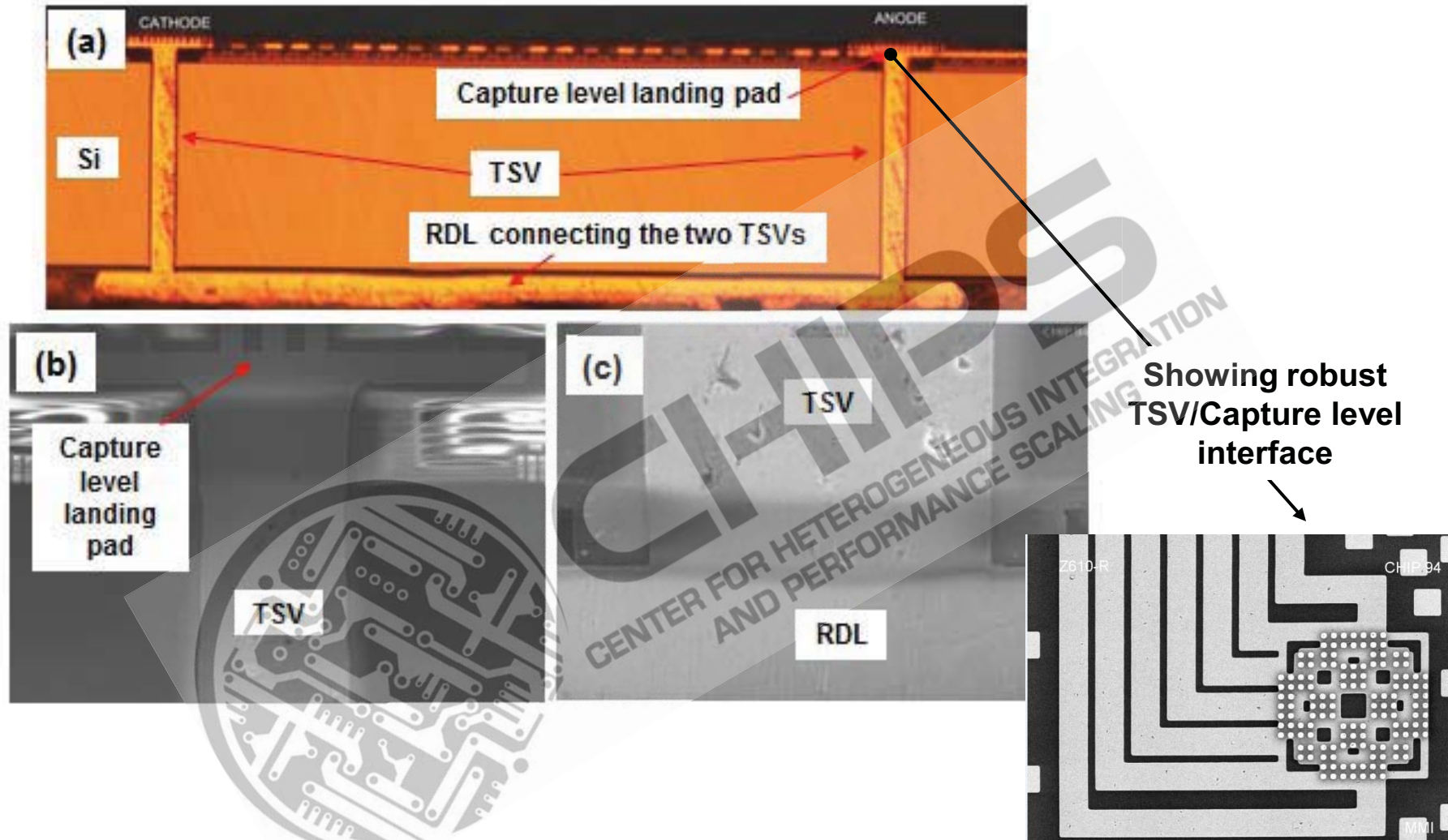
Link of interest: TSV/RDL. All other links are design robust

Results & Discussion– Electromigration Performance (TSV/RDL)



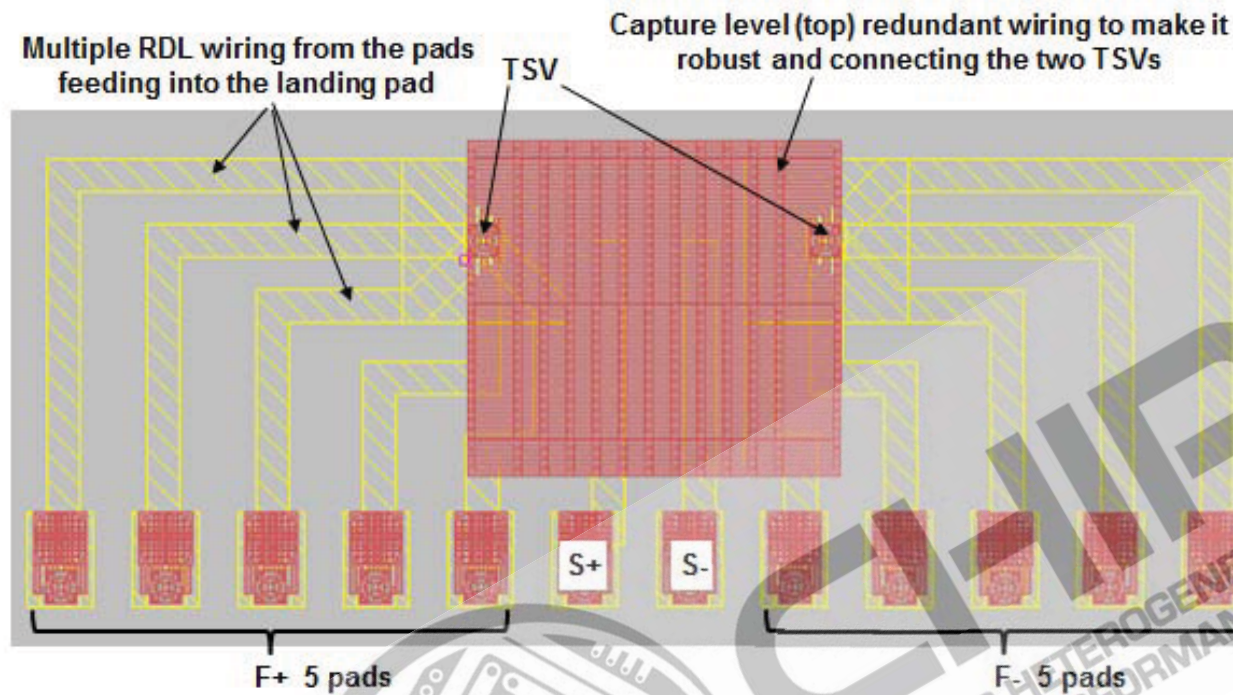
- TSV/RDL structure EM performance equivalent to TSV/five finger capture level
- The failure criteria is aggressive and it only takes 0.05 ohms resistance increase to classify as a failure for this huge structure. The structure didn't result in hard open
- Test done at lower current didn't tail till 2700 hrs of stress

Results & Discussion– Cross-sectional Images (TSV/RDL)

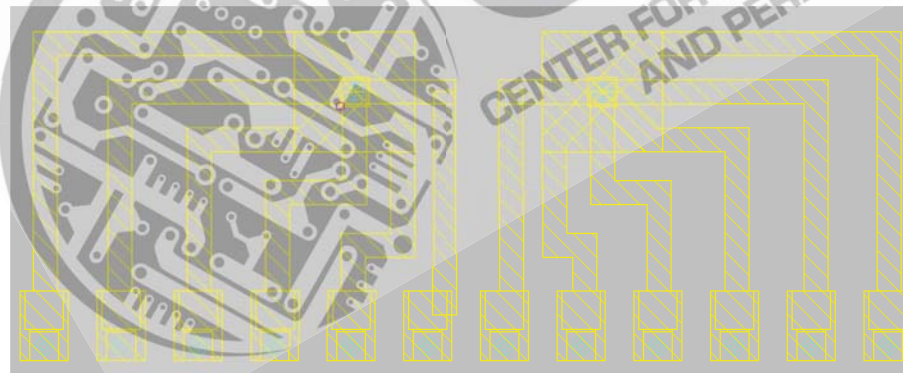


TSV/RDL structure post EM performance is still intact. No significant degradation was observed

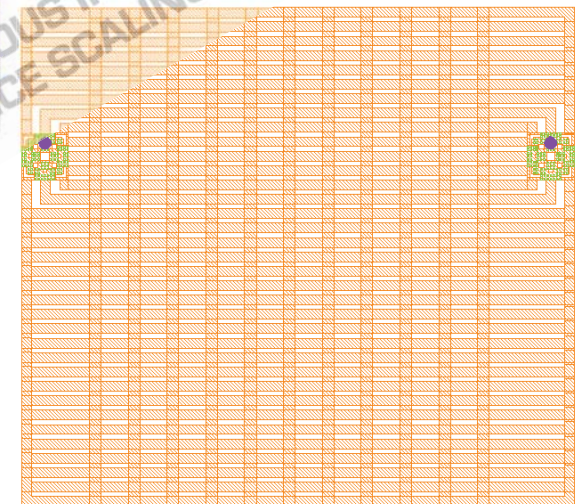
Experimental Details – Test Structures (TSV itself)



RDL
only

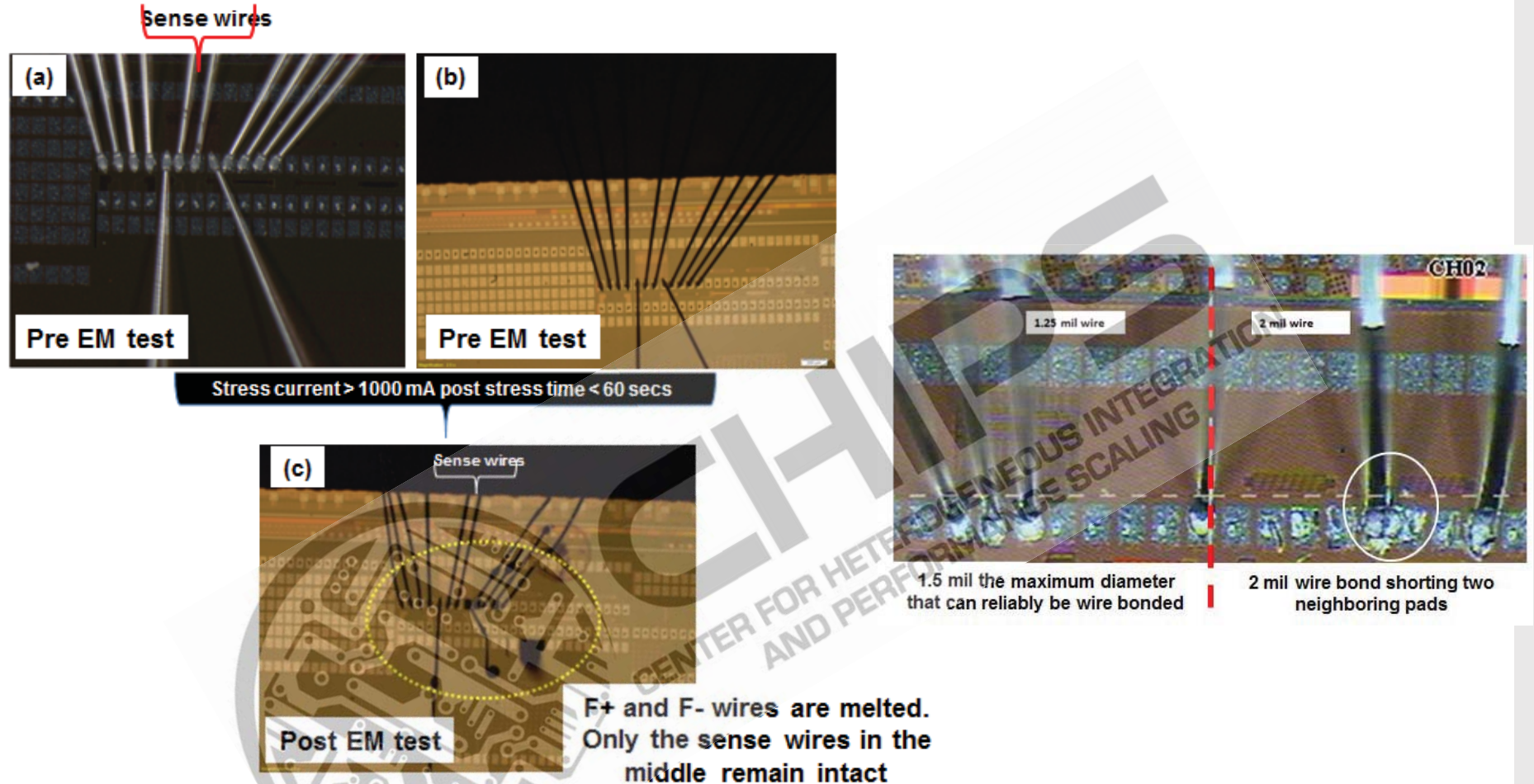


Capture level only



Link of interest: TSV. All other links are design robust

Experimental Details – Test Structures (TSV itself)



(a) Wirebonds are not robust enough to test the TSV itself structure

(b) 1.5 mil diameter wirebonds fuse beyond 1 A for 5 parallel wires (250 mA/wire)

Good candidate to test in package form with C4s. Need a robust design to maintain TSV as the weakest link and uniform current distribution

Take Away Message/Concluding Remarks

| Link of Interest | Experimental Condition | | | | Current Loading Capability* |
|-----------------------------------|------------------------|-------------------------|--------------------|---|-----------------------------|
| | Stress Current (mA) | Stress Temperature (°C) | Joule Heating (°C) | Electrical C/S Area (μm^2) | |
| TSV/Capture Level (Single Finger) | 125 | 300 | 2 | ~5 | 1A |
| TSV/Capture Level (Five Fingers) | 300 | 300 | 10 | ~12 | >1A |
| TSV/Grindside RDL | 300 | 300 | Negligible | ~20 | >1A |
| TSV element by itself | 540-1000 | 300 | Negligible | ~20 | >>1A |

* By passing electromigration targets comfortably. Parameters used in this calculation: 10KPOH, Activation Energy: 0.9 eV, Current Exponent=1.1, Operation condition = 100°C, 1A, Lifetime=11.4 years

What is the electromigration limited min/max. current for the links comprising of TSV, Capture Level and Grindside RDL?

Integration Scheme is robust enough to handle 1A* and above

Concluding Remarks

- ❑ In the 6 μm solid Cu via-last integration scheme, current loading as high as 1 A is demonstrated successfully
- ❑ Results indicate strong interaction of current crowding. EM intelligent design to route the TSVs in the device side and grind side RDL will result in current loading higher than 1A comfortably

Optimized Power Delivery for 3D IC Technology Using Grind Side Redistribution Layers

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Friday, June 3, 2016. Session 41: Student Interactive Presentations
8:30 AM - 10:30 AM

- ❑ Improved structures and testing methodology needs to be derived to test the limitation of the TSV element itself by making other elements/links robust enough. >1 A stress current to 5 parallel wire bond wires had fused

Acknowledgements

- ❑ One of the authors (Prakash P) sincerely thank Tim Sullivan (IBM, Retired) for his mentorship and structure concepts used in this study
- ❑ Authors also thank Carole Grass, Dinesh Badami, Henry Nye and Gary St Onge for their managerial support during this work
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Thank You