



FlexTrate™: High Interconnect Density Fan-Out Wafer Level Processing for Flexible Bio-compatible Electronics

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Outline

1. UCLA CHIPS – A Brief Introduction
2. New Flexible Device Integration Technology
 - 2-1. Introduction of “FlexTrate®” based on FOWLP
 - 2-2. Fine-Pitch Interconnect Formation
 - 2-3. Process Optimization and Evaluation
3. Summary
4. Acknowledgement

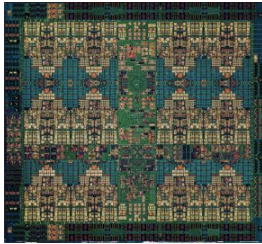
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SoCs have been driven by Silicon Scaling



1964 - Transistor
SLT module
6 transistors, 4 resistors

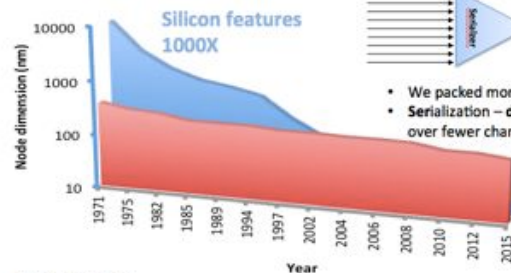


2016-7 – IBM POWER 9 Processor
fabbed @ Global Foundries
14nm SOI eDRAM technology,
650mm²

24 cores and 120MB of on-chip eDRAM memory

8 billion transistors, 17 wiring levels !!

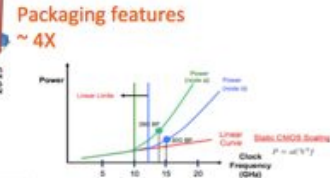
Courtesy IBM



- Boards are large
- "Serdes" area (>25%) and power (>25%) getting out of hand



- We packed more function on die – SoC era
- Serialization – deserialization techniques allowed high data rates over fewer channels



Packaging has scaled modestly

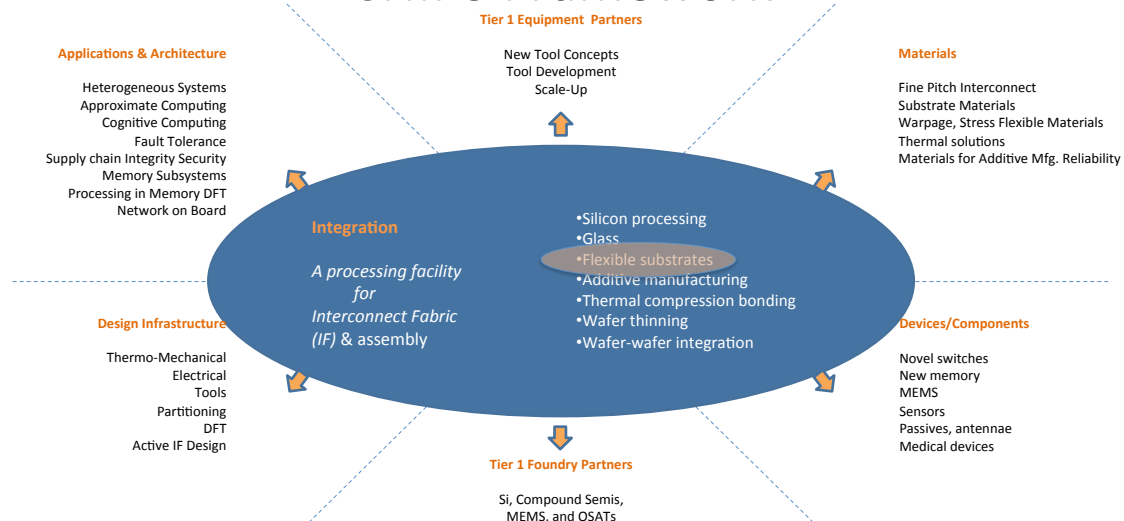
Interconnect density & transistor performance are both important

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CHIPS Framework



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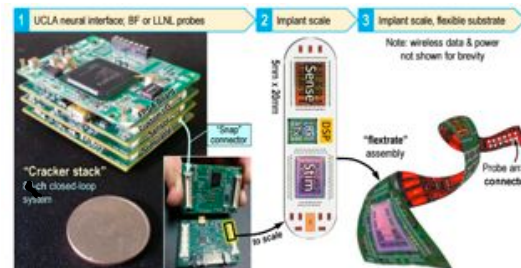
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High Performance Flexible systems will require high performance heterogeneous Chips and high interconnect density



Self contained implantable and autonomous electronics has widespread applications

- Depression
- Parkinson's
- Epilepsy
- And many more

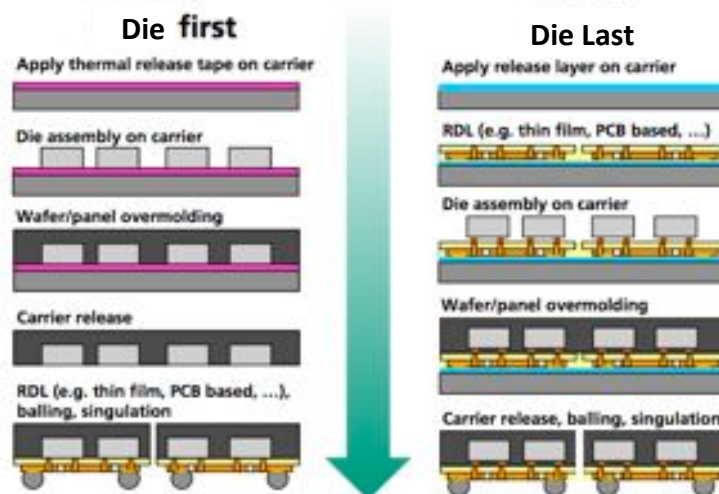


Markovich et al

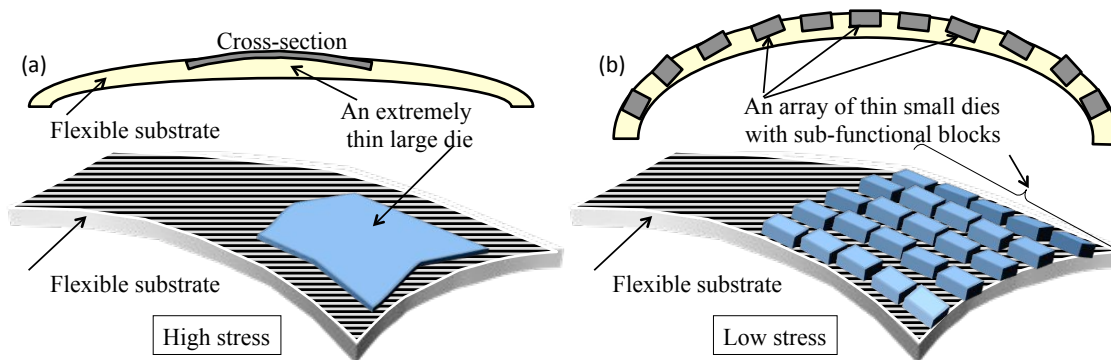
But they do need Hi performance processors, heterogeneous components and innovative power delivery and communication and Fine pitch interconnects on flexible substrates to conform and insert

Fan-out Wafer Level Packaging (FOWLP) – a Quick Tutorial

- Developed by Infineon (now Nanium)
- Practiced by n some form or the other by
 - TSMC
 - Amkor
 - ASE
 - ...



Concept of New Flexible Device Integration “FlexTrate®” : Configuration of Single Crystalline Dies Embedded in Flexible Substrate



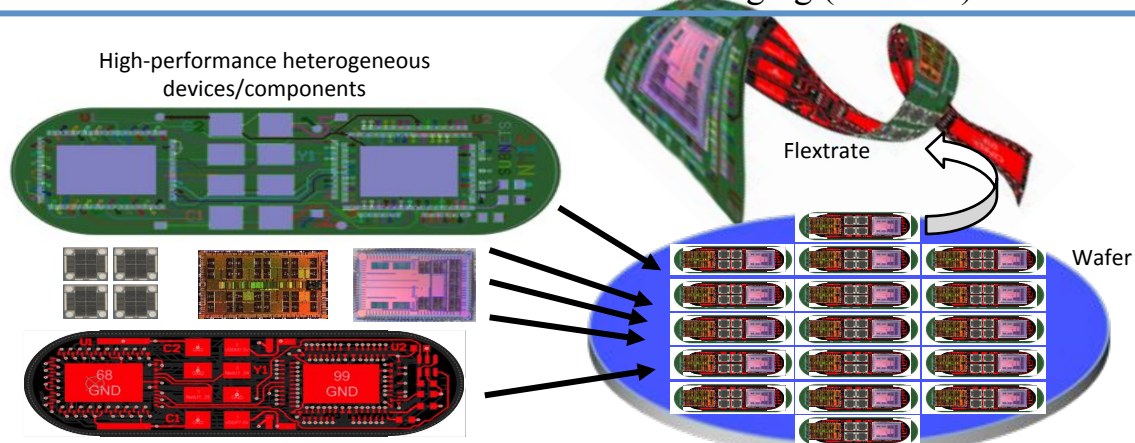
Small dielets embedded in a polymeric film enable bendable and stretchable structure. Thin Si is also flexible, but bending would give serious reliability issues with high stress.

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Methodology of FlexTrate® Based on Fan-Out Wafer-Level Packaging (FOWLP)



FlexTrate® allows for hetero integration with high-performance inorganic single crystal semiconductor devices (Si & GaAs etc.) and much tighter interconnects compared to printed flexible electronics with organic semiconductors in roll-to-roll processing.

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A Fabrication Flow of FlexTrate[®] using Flexible FOWLP Process with a Biocompatible PDMS

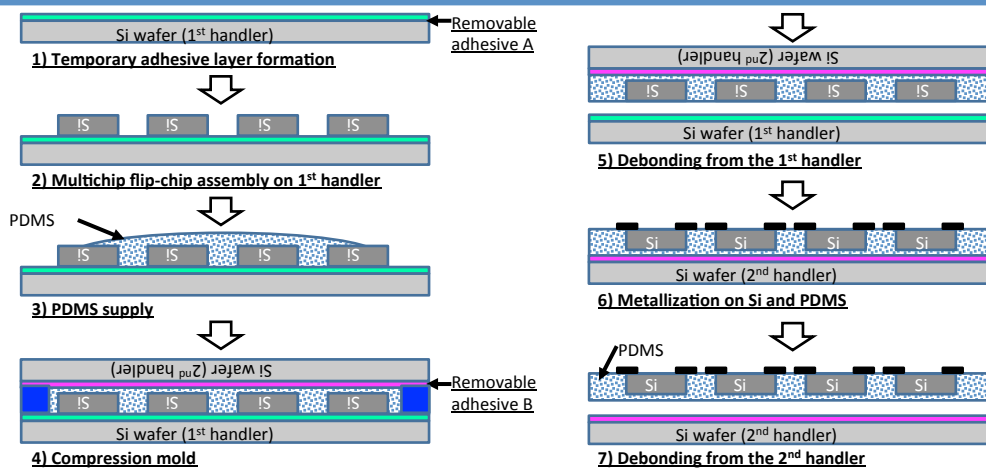


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A Fabrication Flow of FlexTrate[™] using Flexible FOWLP Process with a Biocompatible PDMS



Double Flip Transfer process allows wafer-level processing based on fan-out wafer-level packaging to make fine-pitch interconnects and flexible Si & III-V devices.

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Properties of a Biocompatible PDMS (SILASTIC® MDX4-4210 / Dow)

Properties	Biocompatible PDMS
Hardness	30 (Shore A)
Tensile strength	5 (MPa)
Elongation at break	~500%
Dielectric constant @ 100kHz	3.0 (3.01@100Hz)
Dissipation factor @ 100KHz	0.001 (0.0009@100Hz)
Volume resistivity	$2 \times 10^{15} (\Omega \cdot \text{cm})$
CTE	~300 (ppm/K)
Young modulus	0.5 (MPa)
Tg	-120 (°C)
Thermal decomposition temp.	200 (°C) or more
Screening test	Applicable for implantation in the human body for up to 29 days without encapsulation

Comparison of Multi-Die Placement: K&S CtW Flip-Chip Bonder and Capillary Self-Assembly with Liquid Droplets

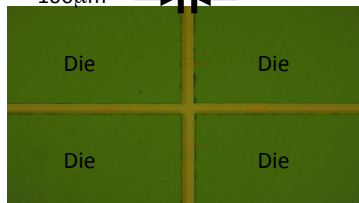
(a) Pick-and-Place



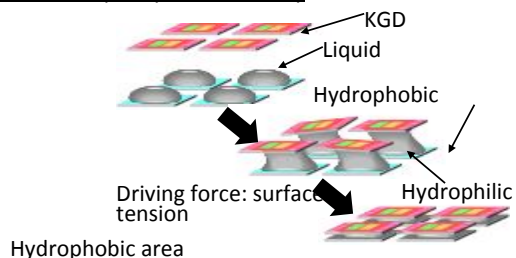
K&S alpha bonder

100μm → || ← 5mm

Advantage:
Tight Die-Die
placement with
~1 μm overlay
tolerance



(b) Tohoku Capillary Self-Assembly

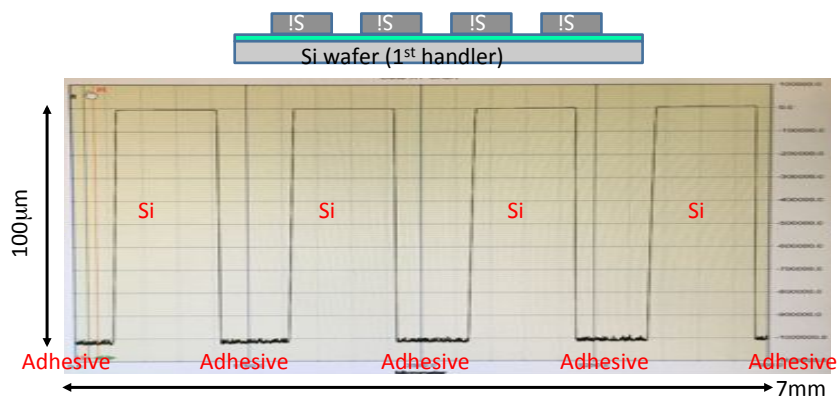


Hydrophobic area



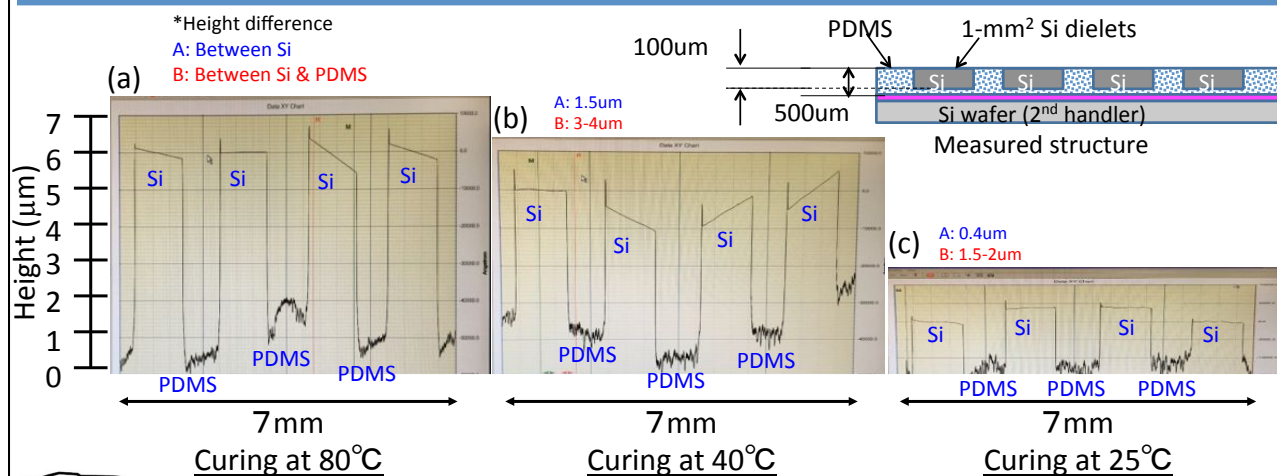
Advantage:
High thru'put Batch
assembly
is possible with 1-2
μm alignment
accuracy

A Surface Profile of Multi-Dies Placed on the 1st Temporary Adhesive on the 1st Si Handler



There is very small die tilt. The maximum height difference among the Si dies is approximately 1.5 µm, similar to the dielet TTV values.

Curing Temperature impact on Final Topography



The height gap is gradually reduced with the decrease in curing temperature.

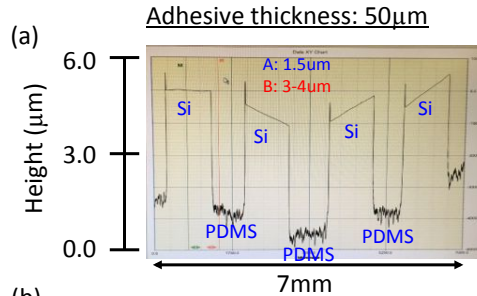
Reducing First Adhesive Thickness and PDMS curing temperature

*Height difference

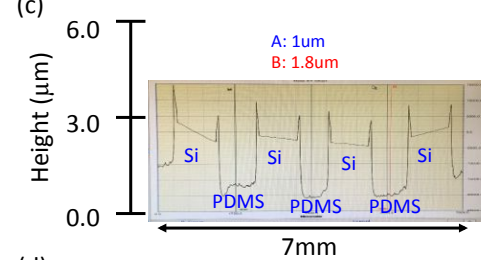
A: Between Si

B: Between Si & PDMS

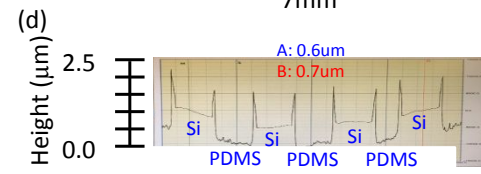
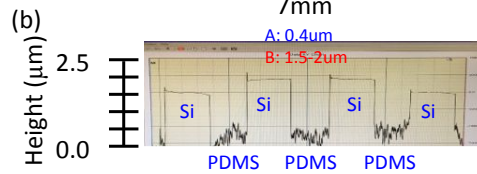
Curing at
40°C



Adhesive thickness: 10μm



Curing at
25°C



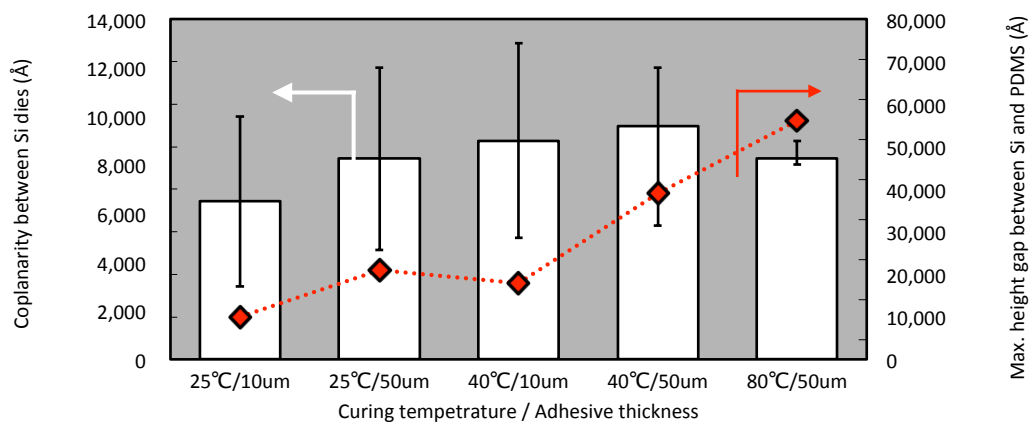
Thinner adhesive layer (10μm) can further reduce the height gap down to 1μm

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Summary of final dielet co-planarity studies



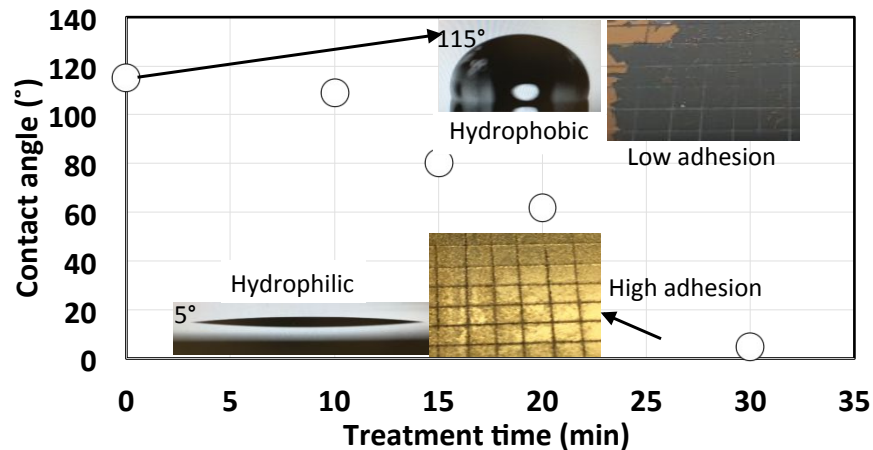
- The height gap is gradually reduced with the decrease in curing temperature
- Thinner adhesive layer (10μm) can further reduce the height gap down to <1μm

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Water Contact Angle Shift as a Function of Surface Modification Time with UV/O₃, and their Adhesion Properties



By using UV/O₃ treatment, the water contact angle is dramatically decreased, and consequently, the surface is rendered highly hydrophilic.

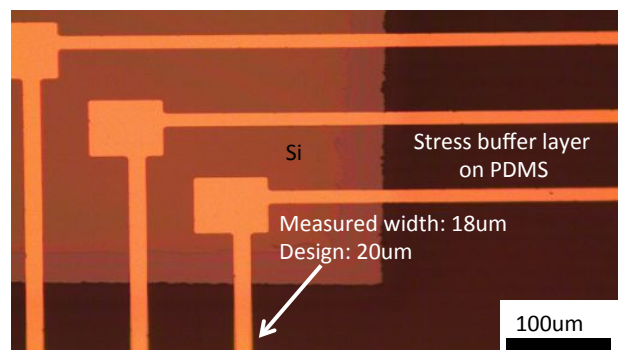
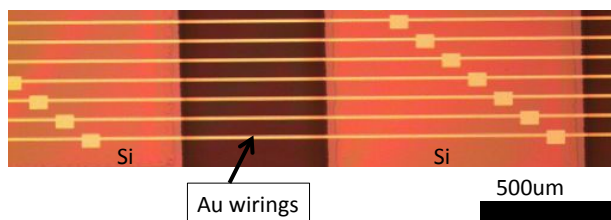
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Fine wiring formation on Si dielets & PDMS: Line Width Meas.



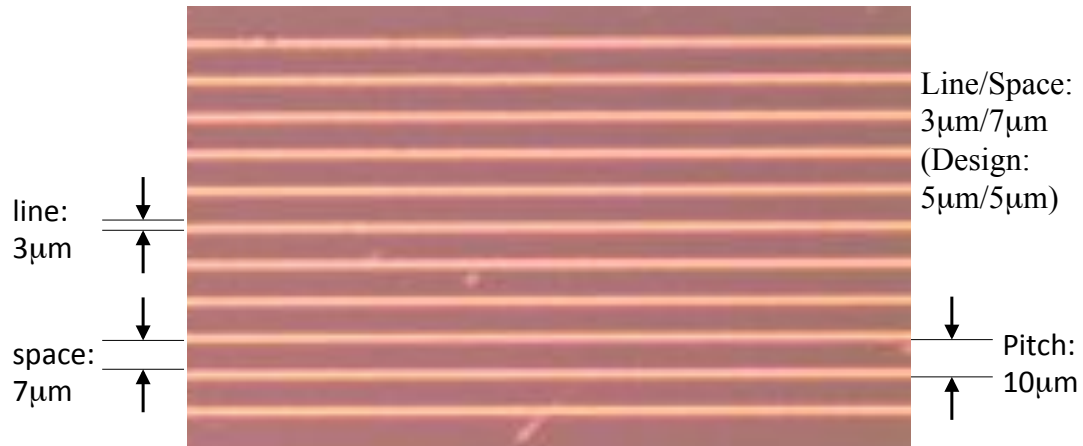
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An Optical Images of 10- μm -pitch Ti/Au Wirings Formed on Si/PDMS at the Wafer-Level



Fine-pitch (pitch: $10\mu\text{m}$) wirings are successfully formed on PDMS.

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An Optical Images of 8- μm -pitch Ti/Au Wirings Formed on Si/PDMS at the Wafer-Level



Fine-pitch (pitch: $8\mu\text{m}$) wirings are successfully formed on PDMS.

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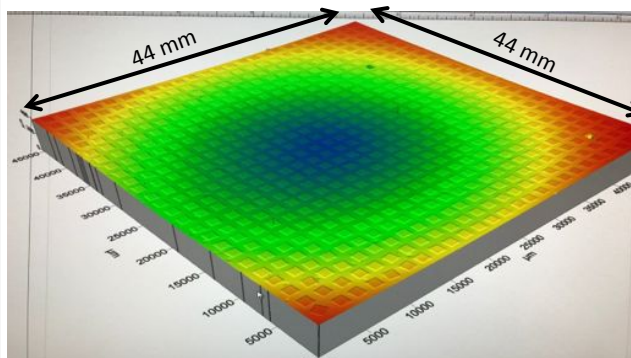


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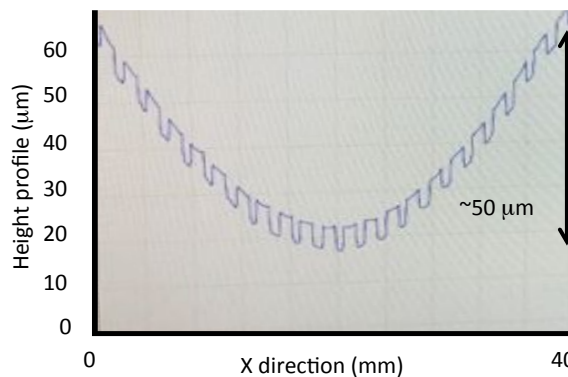
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Wafer Warpage

625 (25 by 25) Si dielets embedded in PDMS



Wafer bow



Typical FOWLP shows serious wafer bow beyond 1mm. This flexible FOWLP technology with PDMS can significantly reduce the thermomechanical stress due to the low glass transition temperature T_g of the PDMS.

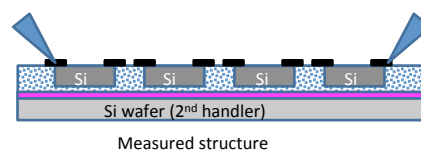
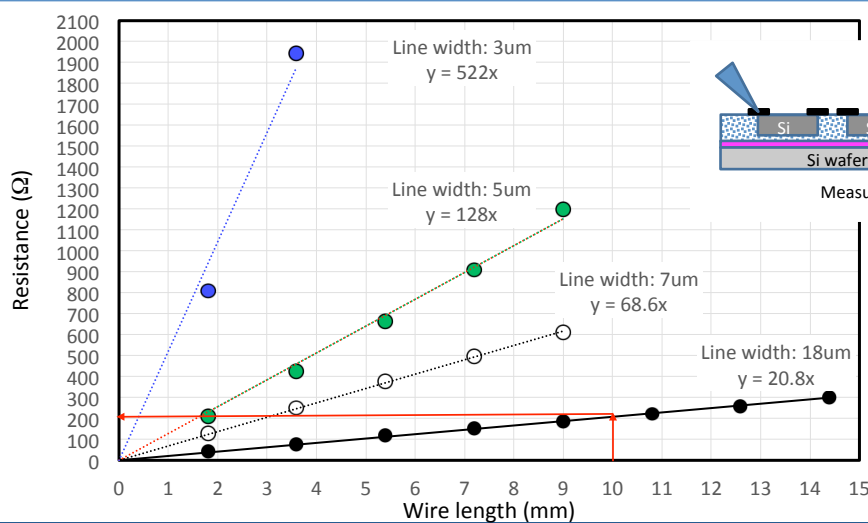
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Electrical Property of Fine Wirings on FlexTrate[®]



Theoretical resistance:
122 Ω
@18μm(w),
10mm(l),
100nm(t)
(Au: $2.21 \times 10^{-8} \Omega \cdot m$)

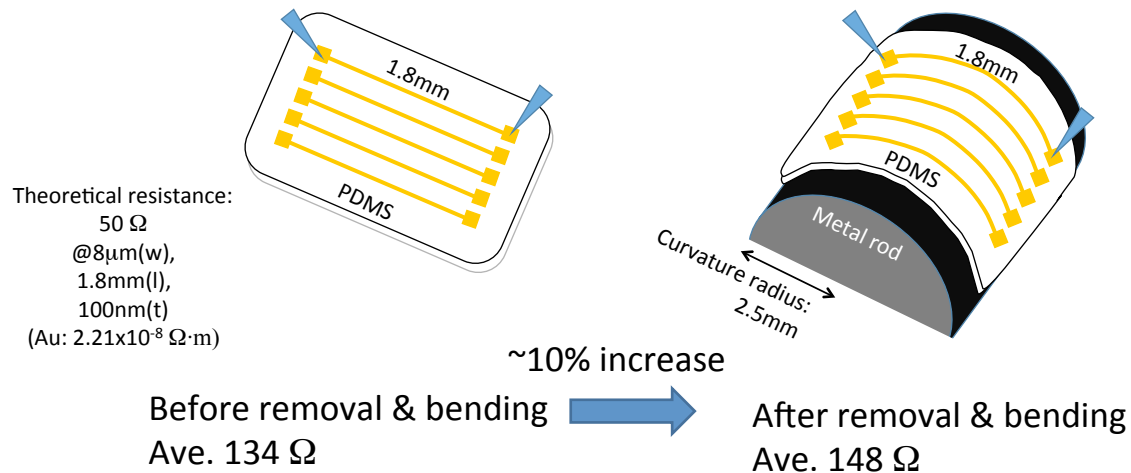
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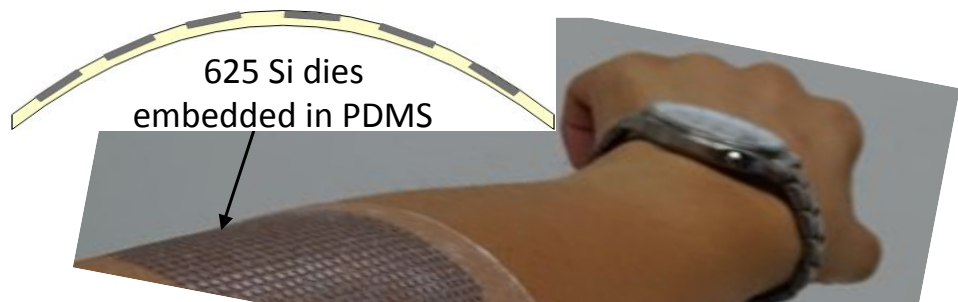
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Electrical Property before/after Removal & Bending



Pictures of a wearable demonstrator of FlexTrate[®]



The flexible substrate FlexTrate[®] embedding large numbers of small Si dies in the biocompatible PDMS is bendable, wearable and implantable, and can be attached on the curved surfaces such as the human arm or even inserted into the cranium.

Summary

- FlexTrate™ is introduced as a hi-performance wafer-level fan-out process on flexible moulded substrates
 - Biocompatible if needed
 - Heterogeneous integration of high performance dielets including MEMS and sensors, passives, coils, antennae, batteries, supercaps.....
 - High density Interconnects
 - Embedded Fluidic interconnects
- Tight lithographic alignment of dies and wiring
- Mechanical /electrical testing in progress

Acknowledgements

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