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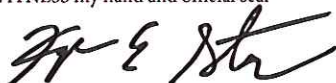
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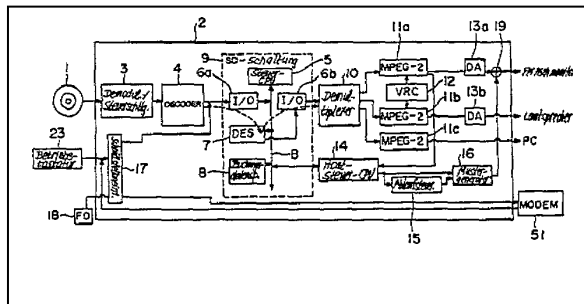
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54 Device for managing software amounts

57 The user is to be informed when a defined amount of software has been exceeded. Video data frames, encoded and compressed according to MPEG standards are decoded and extended successively in an expansion circuit (11a). After each expansion of a single frame, the circuit delivers a signal to a host control CPU (14), which counts the signals received and decrements the content of a bookkeeping data store (8). When the content falls to zero the CPU delivers symbol pattern image data which are superimposed on the video signal by an adding circuit (19).

Software with limitation with respect to the usage amount



The following information is taken from the documents provided by the applicant

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Description

1 The present invention generally relates to a device for managing and maintaining a software usage amount, such as a computer program, and an image, particularly digitized software. The present invention particularly relates to a device for managing a software usage amount, the device being able to cause a software user, to recognize this when a software usage amount of a usable quantity on the basis of a user authorized by the software to a software entitlement exceeds a paid amount of money.

2 With the progressive development of storage mediums with large storage volumes such as a CD-ROMs, etc., and a fast communication technology with high capacity, such as B-ISDN, etc., not only computer programs, but also image data and audio data in the form of distributed digital information is distributed over such a medium. This means that, CD-ROMs are sold on which work is stored as an image which previously had been provided in the form of a game program or video tape. Furthermore, there is also currently a sale or sales system, in which an image is supplied via a communication line to a user.

3 However, it is quite easy to copy these types of digital information to other media, with a loss of quality as is the case with analog information that cannot be seen. Accordingly, absolutely the same information can be copied and there is a significant possibility that these measures violate the profit of the author. Thus, a third party, with little computer knowledge can copy the contents of the CD-ROM, if he just has a writable disk device and a high-capacity magnetic disk device. As described above, in the majority of cases a lease of this type of digital information carrier due to an inability to carry out a comprehensive security vetting by the author is prohibited. Thus, an end user is not allowed to use the software if the end user does not buy the software. However, this type of software is currently expensive. Therefore, the end user has no alternative but to refrain from purchasing the software until he confirms that the software is identical to that which he or she wishes to receive or actually even that it is usable by its own hardware. Accordingly, the profit-making revenue from this type of software has made little progress.

4 In order to eliminate this situation, the implementation of a new software distribution system has started in which a CD-ROM on which a plurality of software sets are stored but with limited function, and available at a low price and the end-user is informed of a code to eliminate the functional limitation after he has paid a license fee for a lawful use of a set of desired (software). However, the granting of rights to use includes a difficulty in terms of creating a useful life of limitations and the number of uses. There is therefore no alternative

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but to fix or issue such a license for permanent use. Accordingly, the license fee is inevitably high as in the case of conventional distributors of the software.

5 In this regard, in JP-A 6-19707, there is provided a system for registration of a previous amount of money corresponding to a software usage amount specified on an IC card. In this system, a user inserts this IC card into an information device in which this software is used (executable and reproducible), when the software requires a cash payment, and the software is made available or otherwise according to a balance of the registered amount of money available. According to this system, the information device allows the use of the software by canceling the functional restriction on the condition that the registered amount of money is equal to or greater than the required minimum for the use of the software. Further the information device subtracts the balance of the registered amount of money when the software has been used once. If this system of registered amount of money resulting from the subtraction is reduced on the IC card to the minimum amount of money that is required for the use of the software, then the software will again thereby rendered non-usable, then the lifting of functional restrictions of the software is stopped. In this case, all the video, audio and computer program output signals are interrupted by this information device.

6 If all output signals are interrupted, however, the software user is unable to recognize whether the interruption of consumption is due to an error in the information apparatus or on the basis of the running out of, or the end of the registered amount of money.

7 A main object of the present invention is to provide a device for managing a software usage amount, said device should be capable of preventing the use of software, while a software user is informed of the fact that a software usage amount has reached a defined amount in which usable data is output in an incomplete form, if the software is used in excess of this usable amount.

8 According to one aspect of the present invention, an apparatus for managing a software usage amount is provided in a system for providing a signal to the outside by use of the software that manages a set of software. The device for managing a software usage amount includes a software usage amount detection means for determining the useful amount of the software and a determination unit for determining that the determined usage quantity has been achieved. The same device further possesses an output prevention unit for preventing the normal output of the signal to the outside when the determining unit has determined that the software usage amount has reached certain amount of use.

9 The software in the present invention comprises, in addition to a computer software program, audio and/or video information, such as image data, as represented by film data, etc., music and voice data, etc.

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10 The software can be been encrypted or compressed. If the software is previously compressed, an expansion mechanism may be used for expansion of the compressed software and for recovery. If the software has been previously encrypted, a decoding mechanism can be provided for decoding the encoded software. Further, the data, such as the software, may be in analog or digital form. It should be noted that it is desirable that the software that is

applicable to this invention, is a program that enables the user to perceive an image or language, by which this or these are output when the program or the image itself or the language itself is used.

1 The facility or arrangement for delivering the signal to the outside can be a computer or information device other than the computer. Accordingly, the installation can be a video deck or a viewing device that is capable of outputting a digital image and digital language.

2 A method, according to which the software usage amount detecting unit acquires the software usage amount under whatever conditions, may be any method. Further, a format for recording the determined usage amount may also be any desired format and an arrangement may be used for the subtraction of a count value in accordance with the software usage amount. For example, an arrangement for counting the number of operations or the stretching operations of an image data frame that is compressed based on MPEG standards, may be provided, and can output a count value in accordance with the number of operation can be subtracted. Also, a means for counting the number of operations of the decoding of encrypted data and for subtracting a count value in accordance with a number of operation and operation capacity can be provided. An arrangement for measuring a software usage time and subtracting a count in accordance with this time by reference to the time can also be assumed. In addition, an arrangement may be adopted, that performs a subtraction with respect to each of a usable limit when the total software is used once. However, the use of the software includes some output indicators as a result thereof, and the delivery of these displays is associated with the operation by the user. It is therefore desirable to count the release of the software to include the image formed, or the transmission number of a processing result of the software to a personal computer, etc., or to count the number of pieces of music in the case where the software is music or similar.

3 The determination unit defines whether the software usage volume achieves the determined user quantity or not. The defined quantity can be determined beforehand by a person entitled to do this for a defined amount of money to be paid. Furthermore, the use of certain quantity may be determined according to exclusive money-condition. Thus, the software may be defined, for example in the form of a sample distribution as usable only once without fee. The definition of the determination unit software usage amount may be in the form of software usage time or usage rate if

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the software consists of a plurality of minute modules (or frames) in the case that the software consists of a number of minute modules (or frame), and defined as a number of usages of the entire software.

4 The display and output-prevention unit is able to obstruct a normal outside display in that an incomplete display to the outside is undertaken. If, in this case, the display to the outside is a video signal, then the output or discharge prevention, the dispensing unit to the outside can interfere in that a further signal is superimposed on the output signal of the video signal. In this case, the output signal superimposed on the other signal may be a data mark field, which indicates to the software user that the limit of usable amount is reached or that the limited usable set is terminated. If the display to the outside is the display of a video signal, then the display of the output signal of the device may be further impeded in that the polarity of the video signal is inverted. If blind data or dummy data of the software have been previously overlaid, also the display prevention unit can be constructed such that the dummy data is eliminated from the software only if the determination unit has defined that the software usage amount has not been reached. If the output signals to the outside, however, are a plurality of output signals, which are located with each other on the delivery in synchronization, then the output-disabled can transport unit the output to the outside can be prevented in that be that some of the output signals from the plurality of output signals are prevented. In this case, the plurality of types of output signals can comprise the output signals of the video signal and the audio signal. The display prevention unit may then, in the case that the loading determination unit detects or determines that the software utilization rate reaches certain usage amount, like the audio signal to the outside and block the release of the video signal to the outside. Alternatively, the same unit can output the video signal to the outside and lock the display of the audio signal to the outside. Furthermore, the video signal only can be output, as well as also the audio signal, indicating that the use of certain quantity is reached and that a further use is not allowed without approval.

5 The invention will be explained in more detail by means of drawing examples. In the drawing:

Fig. 1 shows a block diagram of a structure common to the respective embodiments,

Fig. 2 is a block diagram showing a configuration of a software-reproducing device according to a first embodiment of the present invention,

Fig. 3 is a block diagram showing the internal functions of a DES device shown in **Fig. 2**,

Fig. 4 is a block diagram showing functions of control central units or CPU units according to **Fig. 2**,

Fig. 5 is a flowchart showing the processing performed by a control CPU processing according to **Fig. 2**,

Fig. 6 is a flowchart showing the processing performed by a different control CPU processing according to **Fig. 2**,

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Fig. 7 is a timing diagram showing signal conditions of the corresponding units according to **Fig. 2**,

Fig. 8 is a block diagram showing a configuration of a software-reproducing device according to a second embodiment of the present invention,

Fig. 9 is a timing chart showing signal conditions in the corresponding units of **Fig. 8**,

Fig. 10 is a block diagram showing a configuration of a software-reproducing device according to a third embodiment of the present invention,

Fig. 11 is a block diagram of a speech-prevention circuit shown in **Fig. 10**,
Fig. 12 is a block diagram showing a configuration of a software-reproducing device according to a fourth embodiment of the present invention,
Fig. 13 is a timing diagram showing signal conditions in the units corresponding to units of **Fig. 12**,
Fig. 14 is a block diagram showing a configuration of a software-reproducing device according to a fifth embodiment of the present invention,
Fig. 15 is a timing diagram showing signal conditions in accordance with the units according to **Fig. 14**,
Fig. 16 is a block diagram showing a configuration of a software-reproducing device according to a sixth embodiment of the present invention,
Fig. 17 is a block diagram of a device that causes a CD-ROM to store data that is used in the sixth embodiment of the present the invention,
Fig. 18 is a block diagram showing a configuration of a processing unit according to **Fig. 16**, and,
Fig. 19 is a timing diagram in which signal conditions referring to units according to **Fig. 16** are shown.

In the following, the preferred embodiments will be described. For this purpose, reference is made to the drawings.

Fig. 1 illustrates a structure which is common to the following embodiments. A software reproduction device **100** includes a software usage amount detection unit **101**, a determination unit **102** and a display or output-prevention unit **103**. When the software is entered into the software's reproduction device **100** and when a software user uses this software, then the software usage amounts detection unit **101** determines a usage amount of this software. The determination unit **102** compares the software usage amount by means of the detection unit or detector unit **101** software usage amount with a defined amount of available usage. The output prevention unit **103** prevents display to the outside when the determination unit **101** determines that the software usage amount reaches certain amount of use.

The structure of the first embodiment will now be explained with reference to **FIG. 2**, in which a block diagram showing the software structure of a reproduction device is illustrated as used in the first embodiment according to the present invention.

According to **Fig. 2** a software reproduction device **2** is an information device that is able to use a plurality of software which are offered via data carriers such as a CD-ROM **1** and is offered by communication via a telephone line. The plurality of software includes forms of digital data such as audio data, image data, character data, and a computer programs, etc. The contents

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of the software diversity can be offered by a computer program and data for the program that has been previously provided on a floppy disk, can be provided by a television program which has been previously sent from an analog television system, by a film program that has so far been offered on video tape, and can be provided by a video disk containing music data, which was previously offered through broadcasting, as well as a compact disk and also still pictures, etc.

The following explains the format of the stored plurality of software stored in CD-ROM **1**. With respect to the video and audio data, this means that frames are sequentially formed, thus forming a set of software. Then the video and audio data frames are subjected to an analog-digital conversion before being stored in the CD-ROM **1**. Subsequently, the analog-to-digital converted data frames are compressed in accordance with the standards of MPEG-2. Herein, MPEG-2 is understood to be those recommended by the video compression standards developed by MPEG (Motion Picture Image Coding Experts Group), which includes the primary video format, CCIR601 standards (4: 2: 2 format) and HDVT (up to 1920 × 1080 lines / picture). The compressed data frames are encoded using a given encryption key. In contrast, the data are directly encoded, without being subjected to the compression processing on the basis of MPEG-2 as the MPEG standards are related to video and speech signals with respect to the computer program. The data encrypted (and compressed) by such a process is written to the CD-ROM.

The thus processed data is stored in or on the CD-ROM **1** and is read by a control unit, not shown. The data frames read through this control unit, not shown, are fed through a demodulation/control circuit **3** of the software reproduction line **2** on the input side.

The demodulation/control circuit **3** includes a function for demodulating the data frame supplied to the input side, and transmits these items of data to a decoder **4**.

The decoder **4** performs an error correction and a bit reallocation and transmits the data frame to a SD circuit **9** at a maximum speed of 2 megabytes / sec (mean 1 megabyte / sec). For transferring the data frames, the decoder **4** is connected to a system bus B within the SD circuit **9** via an input/output (I / O) unit **6a**.

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An interface unit **17** is also connected via the I/O unit **6a** to the B system within the SD circuit device **9**. This interface unit **17** performs a input/output process between the SD device **9** and an operating keyboard **23** on the outside of this software reproduction unit, a floppy disk drive unit **18** and a modem unit **51**. Then, the software data that has been transferred via a communication network from a software vendor is input through this modem unit **51** and the interface unit **17** in the SD circuit **9**. The software delivered over the connection has the same format as the software that was supplied on the CD-ROM **1**; it is first encrypted (and compressed).

Now, an explanation of the SD (super distribution) circuit **9** that is connected with the decoder **4** and the interface

17. The plurality of software passed to the software reproduction device 2 is distributed via a readily available medium such as the above-mentioned CD-ROM 1 and communication channels, which is why the problem exists of how an accounting and billing system is to be configured to take into account a user permission in the accounting. The SD circuit 9 is used for this purpose. This means that the plurality of software that can be used by the software reproduction device 2 is distributed in an encrypted state. The plurality of encrypted software is sequentially decrypted by the CD-circuit 9. Furthermore, the SD circuit 9 subtracts an accounting counter value X in synchronization with the use of the software. This accounting value X is defined as a point that is written into the SD-9 circuit in conjunction with an amount of money, which has previously been paid by the user entitled to a software (copyright authorized use). The SD circuit 9 possesses a safety of the software that stops the decoding process when the count value X accounting becomes zero.

1 It should be noted that the SD circuit 9 is updated in the form of an IC card, which is removably inserted into a card slot (a card slot corresponding PCMCII for example) in the software reproduction device 2. As the IC card shape is selected, the SD-9 circuit can be easily transported. Accordingly, the user takes it to a software store sale (Software seller) or the like, and the accounting counter value X can be added to it in exchange for payment of a fee.

2 The SD circuit 9 consists of a control CPU 5, a DES (Data Encryption Standard) device 7, an accounting memory 8, and input / output units 6a, 6b, which are connected with the bus or the bus line B .

3 The control CPU or central processing unit 5 divides its work with a host control CPU 14 in the software reproduction device 2 with regards to transmission and reception of data between the decoder 4, a demultiplexer 10 and the DES device 7

4 Further, the control CPU 5 includes a function for controlling the DES device 7 and the calculation or accounting data memory 8.

5 The invoice or accounting data memory 8 is a memory that stores the abovementioned accounting counter value X. It should be noted that the accounting counter value X is encoded in the accounting memory 8.

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6 This makes it impossible for anyone other than the authorized software person to define the accounting count value X, to write or to re-write it in that this accounting data memory 8 is analyzed.

7 The DES unit 7 has a function for decrypting the received video and audio data obtained by the decoder 4, and a function for encrypting user data (a period of use and the frequency of use of software), which are generated by operation of the software. It should be noted that the software vendor is informed via the communication network by the modem 51 of the user data or that users was or is data written to the floppy disk 7 and are then collected by the software vendor, when the user pays the costs the next time. Fig. 3 schematically illustrates a configuration or a structure of the DES device 7. The DES unit 7 comprises, as illustrated in Fig. 3, a DES execution unit 20 in which a function for decoding the input data (IN) on the basis of key data 21 and the delivery of said decoded results in the form of output data (OUT) is included. According to this embodiment, the DES execution unit 20, possesses a mode identifying unit 22. This mode identification unit 22 has a function for selecting an optimum mode of operation based on a data format, etc. of a plurality of DES modes and informs the DES execution unit 20 with respect to the selected optimal mode of operation. The key data 21 are key evaluation keys in which the software vendor is informed via the communication link when the software vendor has confirmed the receipt of the cost to use the software from the software users. It should be noted that the use of the DES unit 7 may include an IC chip (with the designation 46, DATA ENCRYPTION STANDARD NIST) as manufactured by Phillips Publication Corporation.

8 Returning to Fig. 2, it should be noted that the data frames decrypted by the DES unit 7 (video data and audio data, etc.) is transmitted to the demultiplexer 10 outside of the SD circuit 9 via the I/O unit 6b. The demultiplexer 10 demultiplexes the audio frame data, the of video data frames and the computer program as well as the data for the program. Then, the video data frame is passed to a MPEG expansion circuit (MPEG-2) 11a, while the audio data frame is passed to a MPEG expansion circuit (MPEG-2) 11b. Then, the computer program and the data for the program are passed to a MPEG expansion circuit (MPEG-2) 11c.

9 The MPEG-expansion circuits (MPEG-2) 11a, 11b are circuits for expanding the video or audio frames of data that are transmitted in the compressed state, on the basis of the MPEG standard in order to recreate the signal of the picture or speech. When the data frames have been expanded by these MPEG expansion circuits (MPEG-2) 11a, 11b have been expanded, a VRC circuit 12 undertakes a synchronization of the output signals of the circuits 11a, 11b. This means that the MPEG expansion circuits (MPEG-2) 11a, 11b, output the expanded data frames in synchronization with synchronizing signals which are output from the VRC-circuit 12.

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It should be noted that the MPEG-expansion circuits 11 can include using an IC chip (ISO / IEC CD 13188'1-3).

10 The output signal from the expansion circuit MPEG (MPEG-2) 11 for a video data is converted in a converter 13a to an analog signal by means of a digital-analog (D/A) converter . This analog signal is output to a TV monitor unit, not shown, which is connected via an adding circuit 19 on the software reproduction device 2. Further, the output signal of the MPEG expansion processing circuit (MPEG-2) is converted to 11b by means of a digital audio data

analog (D/A) converter **13b** into an analog signal. This analog signal is delivered directly to the software associated with a software reproduction device **2** to a speaker (not shown). In contrast, the computer-based program and the data for the program are passed directly from the expansion circuit MPEG (MPEG-2) **11c** to a personal computer (not shown) and are connected to a software reproduction device **2**.

1 The expansion circuit MPEG (MPEG-2) **11a** for video data always outputs a frame expansion completeness signal when an elongation of the individual compressed data frame process is completed. This framework completeness or ending signal is received by the host control CPU **14** of the software reproduction device **2** and then used to control the accounting or accounts position. This means that the host control CPU **14**, in the case that it receives this frame expansion complete signal, works in conjunction with a control CPU **5** that is provided in the SD circuit and that is connected with the CPU **14** and the counter value X of the subtracting accounting via the bus line as is shown in the accounting memory **8**. The host control CPU **14** controls a display prevention, if the accounting count value X is zero. It should be noted that the host control CPU **14** is a processor for controlling the software reproduction device **2** as a whole and of the accounting.

2 The following is a detailed explanation of the special contents of the accounting process, which is performed the host control CPU **14** and the control CPU **5** within the SD circuit **9**, with reference to **Figs. 4** and **5**.

3 **Fig. 4** illustrates a diagram showing functional blocks of the two control CPUs **14** and **5**. According to **Fig. 4**, the host control CPU **14** comprises a frame-counter block **29** for displaying the transmitted frame completeness strain signal of the MPEG expansion circuit **11a** and a mode selection block **24** for receiving an input signal (via the interface **17**, the input / output unit **6a** and the bus line B) of an operating keyboard **33** that is provided on the outside of the software reproduction device **2**. The host control CPU **14** is also made up of a jump-operation control block **27** for receiving a signal from said mode selection block **24** of a jumping mode control block **27**, for accepting a signal from this mode selection block **24**, a normal reproduction mode control block **26** for the reception of signals from the mode selection block **24** and the jumping operation control block **27** and a condition transport operation control block **25** for receiving a signal from the mode selection block **24**. The host control CPU further comprises a converter block **28** for the reception of signals from the control block **26**

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with reference to the usual reproduction operation, the condition transport operational control block **25** and the frame-counter block **29** as well as a display prevention signal display block **30** for receiving a signal from CPU **5** of the control of the SD circuit **9**. In contrast, the control CPU **5** of the SD circuit **9** comprises an image extraction block **33** for receiving a signal from the decoder **4**, a DES encryption block **34** for receiving a signal from the image extraction block **33** and a frame selection block **35** for the reception of signals from the condition transport operation control block **25** as well as from the DES decryption block **34**, and outputs these signals to the MPEG-expansion circuit **11a**. The control CPU **5** also comprises a subtraction block **31** for receiving a signal from the converter block **28**, and an accounting counter register block **32** for receiving a signal from the subtractor **31**, and outputs the signals to the display prevention signal display block **30** and the subtractor **31**. The above functional blocks are described below.

4 The mode selection block **24** determines that a key from a row of buttons, including a "Key renewal", a "Condition-transport-key" and a "Spring transportation" key are pressed, and comprise the operation buttons **23**. The mode selection block **24** then decreases according to the actuated or depressed key and activates a block of the jumping operation control block **27**, the normal playback mode control block **26** and the transport operation control as block **25**. It should be noted that the respective control blocks **25**, **26** and **27** are stopped on the actuation or pressing a "Stop" key that is part of the operating keys **23**. The normal reproduction mode control block **26** guides the control of the display of the SD circuit **9** of the transmitted frame in a defined sequential interval. When the normal reproducing operation of control block **26** is put into operation, then a start-up display signal is sent to the block converter **28** on the input side for the duration of the actuation of the control block **26**. The jump operation control block **27** carries out the control of an intermittent operation of the normal reproduction operation control block **26**. The condition transport operation control block **25** causes the control to select and display the output of the frame sent to the SD circuit **9**, in accordance with a certain algorithm. With condition transport operation, the video data are displayed as a time-lapse image of the supplied pictures. If the condition transport operation control block **25** is activated, then an activation display signal is transmitted to the block converter **28** and the image or the frame selection block **35** is transmitted for the duration of the operation of the control unit **25**.

5 In contrast, when the normal reproduction mode control block **26** or the condition transport operation control block **25** are activated or triggered, then a not-shown CD-ROM drive, a demodulation/control circuit **3** and the decoder **4** are put into operation (alternatively, the data frame is downloaded via a modem **51**), whereby the frame is transmitted to the image data extraction block **33**. The image extraction block **33** extracts only the video data frame of the transmitted data frame, and transmits the extracted data frame to the DES decryption block **34**.

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6 This DES decryption block **34** operates the DES device **7** and decrypts the transmitted video frame. The corresponding video data frame decrypted by the DES decryption block **34**, is fed to the input side of the frame selection block **35**.

1 For the duration of reception, the frame selection block **35** selects the operation display signal from the condition transport operation control block **25** of some of the received frames of video data and video images in accordance with the specific algorithm and outputs it to the MPEG-expansion circuit **11a**. As algorithm for this video frame, for example, there are selectively used algorithms for selecting only one of the frames or images in which a specific indicator or flag is set; for selecting an image frame or picture at an interval, a specified number of frames or images, and for selecting a frame or image in a particular time interval. It should be noted that the frame or image selection block **35** displays all received video data frames or images of the MPEG expansion circuit **11a** during which it receives no activating signal from the condition transport operation control block **25**.

2 The MPEG expansion circuit **11a** for video data, which receives the video data frame, causes a sequential expansion process on the received video data frames. Whenever the MPEG-expansion circuit **11a** completes the expansion process of the individual frame, the circuit **11a** sends the video signal to the D/A converter **13a**, and transfers the frame end-expansion signal, to the frame counter block **29**.

3 The frame counter block **29** is a counter for incrementing a count value n by 1 when the block **29**, receives the frame completeness expansion signal. The frame counter **29** indicates this count value n to the converter in block **28** at all times. Further, if a deletion signal is received from the converter block **28**, the frame counter block **29** deletes the count value n , thus, making it zero.

4 The converter unit block **28** compares the count value n information that it has received from the frame counter block **29**, with a predetermined reference value for the duration of reception of the operation display signal from the normal reproduction mode control block **26** or the condition transport operation control block **25**. This predetermined reference value is set to R (for example, is $R = 100\,000\,000$) when the operation indication signal is obtained from the normal reproducing operation, control block **26**, whereas it is set to $2R$, when the operation display signal is received from the condition transport operation control block **25**. Then, in the case that the counter value n has reached a defined reference value, the block **28** issues an accounting subtraction command to the subtraction block **35**. The converter unit block **28** especially issues a subtraction value "1" to the subtraction block **31**. It should be noted that the converter unit block **28** is stopped in the event that the actuation is stopped or in case that the accounting block has received a subtraction command and issues the deletion signal to write to the frame counter block **29**. A software usage amount device is made up of the MPEG expansion circuit for the video signal **11a**, the frame counter block **29** and the converter unit block composed **28**.

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5 The accounting counter register block **32** reads the count value X from the accounting memory **8** and shows this value of the subtraction block **31**. At the same time, the accounting counter register block **32** updates the accounting count X of the accounting memory **8**.

6 In the event that the accounting monitoring subtraction block is present from the unit converter block **28**, the subtractor **31** makes a reduction of the accounting counter value X by 1 which is displayed by the accounting counter register block **32**. Then the subtraction block **31** indicates this new reduced accounting counter value X ($X = X - 1$) to the accounting counter register block **32**. The accounting counter register block **32** registration overwrites the new accounting count value X ($X = X - 1$) which the subtraction block **31** has transmitted in the accounting data memory **8**.

7 The accounting counter registration block **32** determines whether the accounting count value X , which is described in the accounting memory **8** is not 0 (no usable value) or not. In the case that the accounting counter value X is 0, the accounting counter register block **32** indicates this effect to the accounting counter register block **30**. It should be noted that the accounting counter register block **32**, in the case that the accounting counter value X is written into the accounting data memory **8** again by the software vendor from "0" to "1" or a higher value, the display prevention signal output block **30** indicates this effect. The subtraction block **31** and the accounting counter register block **32** are combined to form a determination device.

8 In the case that a display is taken up that the accounting count value $X = 0$, the display prevention signal output block **30** issues a video prevention signal from the accounting counter register block **32**.

9 In addition, in the case that a display is taken up that the accounting count value X is greater than 0, the display prevention signal output block **30** issues a reset signal from the accounting counter register block **32**.

10 With reference to the flow charts shown in **Figs. 5** and **6**, a working sequence based on the above-described control CPUs **5**, **14** will be described.

11 **Fig. 5** illustrates in a flow chart of the course of the accounting process as carried out by the host CPU **14** of the software reproduction device **2**. This process begins when it is determined that one of the operation buttons **23** buttons representing, namely the "Play button", the "Condition transport button" and the "Jump transport button" has been pressed. At initial step S101, the host control CPU **14** determines that an image display operation is to be performed or is performed, and on the basis of the type of the pressed button. This means that when the "Play button" or the "Jump transport button", is pressed, the host control CPU **14** determines this as a "Normal play mode". In contrast, the host control CPU **14** then determines if the "Condition transport key" is pressed, this as a "Condition transport operation". The subsequent processes are dependent on the particular playback modes.

12 In the case of "Condition transport mode", the

frame expansion completeness signal is detected by the MPEG expansion circuit **11a** at a step S102. When the relevant frame completion signal is determined, the processing proceeds to step S103 in which the count value *n* of the frame counter unit **120** is incremented by 1.

1 In the subsequent step S104, the CPU **14** determines whether the count value *n* has reached a reference value *n* **2R** (for example, $2R = 200\,000\,000$) or not. If the count value *n* does not reach the reference value **2R**, then, in step S105, the CPU **14** will determine whether the accounting process is completed or not. This determination is performed on the basis of whether the operation display signal has been received from the condition transport operation control block **25** or not. This means that, in the case where the operation display signal has not been received, the processing proceeds to step S116, in that it is determined that the accounting process is to be terminated. On the other hand, if the operation display signal has been received, the processing returns to step S101, by determining that the accounting process is to continue.

2 In contrast, when it is determined that the count *n* reaches the reference value **2R** in step S104, then the processing proceeds to step S106. At step S106, the accounting subtraction command is issued to the CPU **5** of the SD circuit **9**.

3 In the subsequent step S107, the count *n* of the frame counter block **29** is cleared to 0.

4 In the subsequent step S108, the CPU **14** determines in the same manner as in step S105 whether the accounting control process is completed or not. If it is determined that the accounting control process continues, then the processing returns to step S102. In contrast, the processing proceeds to step S116 if it is determined that the accounting control process is to end.

5 In contrast, in the case of "Normal play mode", the frame expansion completeness signal is determined by the MPEG expansion the circuit **11a** at a step 109. When the frame expansion completeness signal is determined, the processing proceeds to block S110, the count value *n* of the frame of the counter block **29** is incremented by 1. Subsequently, the CPU **14** determines in step S111 whether the count value *n* of a reference value *R* (for example $R = 100\,000\,000$) has been reached or not. If the count value *n* has not yet reached the reference value *R*, then the CPU **14** determines in step S112 whether the accounting process is completed or not. This determination is made on the basis of whether the operation display signal is obtained from the normal reproduction mode control block **26** or not. This means that in the case that the actuating display signal has not been received, the processing proceeds to step S116, by determining that the accounting process is terminated. If, on the other hand the operation display signal has been received, then the processing returns to step S109, by determining that the accounting process is to continue.

6 In contrast, if it is determined that the count *n* has reached the reference value *R* in step S111, the processing proceeds to step S113. At step S113, the accounting block subtraction command is issued to the control CPU **5** of the SD circuit **9**.

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7 In the following step S114 the count value *n* of the frame or frame counter block **29** is cleared to "0".

8 In the subsequent step S115, the CPU **14** determines, in the same manner as in step S112, whether the accounting control process is terminated or not. If it is determined that the accounting control process is continued, then the processing returns to step S109. If it is determined, in contrast to that of accounting control process is to be terminated, then the processing proceeds to step S116.

9 In each case, the count value *n* of the frame counter block **29** is deleted and set to "0" at step S116.

10 Subsequently, the CPU **14** waits for the display prevention command, which is issued by the control CPU **5** of the SD circuit **9** in step S117. If the display prevention command is issued by the respective device, then the video prevention signal is issued in step S118. After the above procedure, this accounting process is terminated.

11 **Fig. 6** illustrates a flow chart showing a flow of an accounting process, as carried out by the control of the CPU **5** SD circuit **9**.

12 This process begins when the IC card enclosing CD circuit **9** is inserted or plugged into the software reproduction device **2**. Then, at the starting step S201 the control CPU **5** will perform the authorization. . This authorization implies the checking of the control CPU **14, 5** when the SD circuit **9** is set.

13 Subsequently, the control CPU **5** checks whether the accounting block-subtraction command has been received from the host controller or CPU **14** in step S202. If no accounting block subtraction command has been received, then the check is repeated at step S202.

14 In contrast, if the accounting subtraction unit has been received, then, at step S203, the accounting count value *X* is read from the accounting data memory **8**. Then, a "1" of this accounting value is subtracted from *X*, and the read subtracted value (*X*-1) is defined as a new accounting count value *X*.

15 In the subsequent step S204, the CPU **5** determines whether the new accounting count value *X* is at 0 or below. If the new accounting count *X* is greater than 0, then the processing proceeds to step S206. In step S206, the new accounting count value *X* is written into the accounting data memory **8**. Then, the processing returns to step S202. If, on the other hand, the accounting counter value *X* is 0 or less, then in step S205 the display prevention command is delivered to the host control CPU **14**. Thereafter, this processing is terminated.

16 It should be noted that repeated execution of the process shown in **Fig. 6** has such an operating effect that the SD circuit **9** is briefly removed from the software's reproduction device **2**, that the software vendor introduces the

accounting count in accounting data memory **8** in exchange for a payment of the fee to use the software and that the **SD-9** circuit must again be installed in the software reproduction device **2**.

1 Returning to **Fig. 2**, there is explained a configuration of the display prevention device for carrying out

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an uncompleted display or output by overlaying image patterns over the video signal that is displayed on the television monitor, in accordance with the display prevention signal that is output from the host control CPU **14**.

2 A pattern generator **16** and a sequence control device **15** are added to the input side of the display prevention signal from the host control CPU. The sequence control device **15** outputs a signal which is received in a defined time sequence with the video prevention signal and is switched on/off. This means that the sequence control device **15** as shown in **Fig. 7(c)**, switches off the output signal before the receipt of the video prevention signal in that, after receipt of the affected video prevention signal, the output signal is switched on/off several times. Then the sequence control device **15** continues the display of the switched-on output signal. The output signal of the sequence control device **15** is supplied to the pattern generator **16** on the inlet side.

3 In the case that it receives the display prevention signal, the pattern generator **16** generates picture patterns for displaying the character data in order to attract attention of the software user to point out, for example, that the "accounting count = 0". The pattern generator **16** outputs the pattern image data generated only when the output signal of the sequence control device **15** is switched on. The picture patterns generated by this pattern generator **16** are fed to the input side of the adding circuit **19**.

4 The adding circuit **19** superimposes the picture pattern received from the pattern generator **16** on to an analog video signal output by the digital/analog converter **13** for the video signal and outputs the superimposed signals to the TV monitor unit. When the picture pattern signal, transferred or displayed by the pattern generator **16** is switched off, then the output of the digital/analog converter **13a** is delivered as it is. In contrast, when the image signal pattern is switched on, then a corresponding video signal is displayed in which the image pattern is superimposed on the analog video signal which is output from the digital/analog converter **13a**. It should be noted that this adding circuit **19** is provided only on the output side of the video-oriented digital/analog converter **13**. Accordingly, even in the case that the host control CPU **14** outputs the display prevention signal, the analog audio signal, the computer program and the data for the program (hereinafter referred to as "PC-signal") are displayed normally as previously.

5 It should be noted that the sequence control device **15** and the pattern generator **16** shut down the display signal when a reset signal is received from the host control CPU **14**.

6 In the following the method of operation of the embodiment will be explained.

7 Assume now that a part of the operation buttons **23**, the "Play button" is pressed. Then, the audio and video data frames are so related to each other that these frames are provided in synchronization to the SD circuit **9** by the CD-ROM **1**. These frame audio and video frames are

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decrypted by the DES device or circuit **7**.

8 The SD circuit **9** displays all decoded audio and video data frames in succession to the input side of the demultiplexer **10**. The video data frame, subjected by the demultiplexer **10** to a demultiplexing operation, is fed to the input side of the MPEG expansion circuit **11a** for video data while the audio data is fed to the input side of the MPEG expansion circuit **11b** for video data. Each of the MPEG expansion circuits **11a**, **11b** expands the received frames in a sequential order, and outputs the expanded frames to the digital-converter **13a**, **13b**.

9 Each time that the MPEG-expansion circuit **11a** for video data has fully extended the individual video data frame, the frame expansion completeness signal is sent to the input side of the host control CPU **14**. This host control CPUs **14** counts the number of frame expansion completeness signals and causes the CPU **5** in the SD circuit **9** to reduce the accounting counter value X in the accounting data memory **8**, if this count n reaches the defined reference value R.

10 Thus, in accordance with this embodiment, a load is imposed, which corresponds to the number of displayed frames, even in the event that the user is viewing any area of a film frame, or in the case that the user repeatedly views the same portion of a film image (for example, a film). If the image is stopped, then no new frame is displayed and thus a load is not imposed. Thus, a nonsensical situation is not called forth as occurs in conventional accounting procedures, but rather a suitable loading is imposed. Consequently, there is no need to add an uncollectible load for the use of load for usage, whereby the usage load can be reduced to a comparatively relatively small amount of money.

11 It should be noted that in the case that a part of the operation buttons **23** representing "Condition transport key" is pressed, the SD circuit **9**, outputs to the demultiplexer **10** only the video data frames that are selected in a jump-type manner on the basis of the specific algorithm, and its corresponding audio data frame.

12 The video data frames subjected by the demultiplexer **10** to a demultiplexing function, are fed to the input side of the MPEG expansion circuit **11a** for video data while the audio data are fed to the input side of the MPEG expansion circuit **11b** for audio data. When the MPEG-expansion circuit **11a** for a video data completes the expansion process with respect to the individual video data frame, then an expansion completion signal is output to the host CPU control **14**. In this case, the host control CPU **14** does not cause the CPU **5** in the SD circuit **9**, to decrement the accounting count value X in the accounting data storage unit until the count value n of the number of images of the frame

expansion close signals reaches a value which is twice the reference value R. This means that the accounting counter value X is decremented each time the count value n reaches the value of 2R.

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1 Even if the same number of frames are displayed within the same time period, the load imposed by the step load is generally half of the load imposed in the normal reproducing mode. Thus, generally a part that is based of normal reproduction is switched off or prevented and, on the other hand, a load for the display of data can also be imposed. Accordingly a fair profit balance can be achieved between the software authorization and the user .

2 As a result of decrementing the accounting count value X in this way, the accounting count X is 0. In this case, the signal state of each unit runs in the way as is illustrated in Fig. 7. Fig. 7(g) shows that the accounting count value X at time point "A" is 0.

3 Once the DES device, even in the case of decrypting, the data that the accounting counter value X has become 0, the analog/digital A / D converter 13a for video data, continues the display of the normal analog video signal for the time "A" (see Fig. 7(a)).

4 Then, in the case that the accounting counter value X at time "A" is 0, the host control CPU 14 issues the pulse-like output prevention signal (see Fig. 7 (b)).

5 In response, the sequence control device 15 issues the signal which is alternately switched ON/OFF at a fixed time interval that the output disabled signal is received. After expiry of this period, a continuous output signal display is kept in an ON state (see Fig. 7 (c)).

6 On the input side, the pattern generator 16 receives the display prevention signal (b) and the output signal of the sequence control device 15, and then outputs the character pattern data (a video signal for displaying a character "accounting count value = 0"), only at a time at which the output of the sequence control device 15 is switched on. The time sequence in which the pattern generator 16 outputs the character pattern data is illustrated in Fig. 7(c).

7 The adding circuit 19 for superimposing the video signal (a) and the character pattern data (c) are output from the normal video signal (a) as long as an accounting count X (g) is greater than 0. During a fixed time period from the time "A" from, in the case that the accounting counter value X (g) becomes 0, the output signal of the superimposition of the character pattern on the image and the normal image output signal is alternately repeated (see Fig. 7(d)).

8 It should be noted that an audio signal (e) and a PC-signal (f) are normally to be continually displayed before and after the time point "A".

9 Accordingly, after the time "A" in the case that the accounting counter value is 0, there is generated an output or display prevention signal, such that the character pattern is only superimposed with respect to the image signal of the three output signals (image signal, voice signal and PC signal). Therefore, the software user, who is viewing the TV monitor (not shown) does not misunderstand that this is not the occurrence of a failure of error but is in a position to recognize that the accounting count has been reduced to 0. At this point, the audio signal and the PC signal are normally

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forwarded as they are . If the software is mainly based on the image (e.g., a film, animation, etc.), however, the profit and benefit of the software entitlement is not injured. Much rather, as will be appreciated, an effect is called up such that the desire for continued use by the user of the software is increased. As a result the software user will be ready to pay the fee for the use to the software vendor as compensation for adding to the accounting count X or for removing the SD circuit 9 of the software reproduction device 2.

10 Hereinafter, the structure of the second embodiment is explained.

11 Fig. 8 illustrates in a block diagram, the software construction of the reproduction device used in the second embodiment of the present invention.

12 This embodiment, in the same manner as the first embodiment, possesses a structure in which the number of operations of the expansion of the compressed video data frames is counted on the basis of the MPEG standards and that the accounting counter value X is reduced in accordance with the number of these operations. Further, in the case that the accounting counter value X is 0, the output prevention signal prevents the use of such a structure, that the image signal and the PC signal is stopped completely while the output of the normal audio signal is continued.

13 The format of the software released to the reproducing apparatus 2 in this embodiment, is absolutely the same as that in the first embodiment. Further, the same components of the software are used for the reproducing device 2 in this embodiment as those in the first embodiment with the same reference numerals as provided there. A description of these common elements is omitted, while only the configuration of a device for preventing the display in accordance with the output or output prevention signal, which is emitted or transmitted from the host control CPU 14 is explained.

14 The output prevention signal from the host control CPU 14 here is fed to the input side of a register 40. The register 40 issues a logical value L in an initial state and, upon detection of an increase output prevention signal on the input side, thereafter it continues to output a logic value H.

15 An output signal of the register 40 is inverted by an inverter 41. Thus, the inverter 41 issues the logic value H in the initial state, except that after the output of the initial prevention signal, it continues to output the logic value L.

1 An output signal of the inverter **41** is provided to an input terminal of an AND circuit **42** for video data. The other input terminal of this AND circuit **42** for video data is connected to an output terminal of the MPEG expansion circuit **11a** for video data (MPEG-2). Accordingly, this AND circuit **42** for video data acts as a gateway or key switch for the video signal in order to feed this to the input side of the digital/ analog converter **13a** for a video from the MPEG expansion circuit **11a** for video data. For this reason, a transmission of the video signal is only allowed when the output

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signal of Inverter **41** accepts the linkage value H, whereby the analog video signal is output from the digital/ analog converter **13a** for video data to a not shown TV monitor. When the output of inverter **41** accepts the linkage value L, the transfer of the video signal is prevented or locked and thus no analog video signal is output from the digital/analog converter **13a** for video data.

2 The output of inverter **41** is also supplied to an input terminal of an AND circuit **43** for a PC signal. The other input terminal of the AND circuit **43** of the PC signal is connected to an output terminal of the MPEG expansion circuit **11c** for the PC signal (MPEG-2). Accordingly this AND circuit **43** for the PC signal serves as a gate or key circuit for the PC signal in that it only permits forwarding this PC signal when the output signal of the inverter **41** accepts the logic or linkage value H, but locks the forwarding of the PC signal in the case that the output signal of the inverter **41** is the linkage value L.

3 It should be noted that the AND circuit serving as a gate or key circuit is not provided at the output terminal of the MPEG expansion circuit **11b** for audio data. Thus, even in the case that the output prevention signal has been issued by the host control CPU **14**, the analog audio signal from the digital analog converter **13b** for audio data is displayed normally as before .

4 Incidentally, the register **40** issues the logic value L when the reset signal is output or transmitted from the host control CPU **14**.

5 The operation of the embodiment under consideration is explained in implementation form.

6 The software reproducing device **2** of this embodiment operates in the same manner as the first embodiment until the host CPU **14** outputs the output prevention. Therefore, only the operation after the issue of the output prevention signal by the host control CPU **14** will be explained.

7 If the data in the accounting memory **8** accounting count value X is reduced to 0 as a result of the decrement, the signal status in each unit such is as illustrated in Fig. 9. Fig. 9 shows that the accounting X count at a time point "B" is reduced to 0 (see Fig. 9(b)).

8 The DES device **7** decrypts the data even after the accounting count X has become 0, which is the reason why the video signal continues to be displayed by the MPEG expansion circuit **11a** for video signals after the time "B" (see Fig. 9(a)).

9 When the accounting counter value X at time "B" is 0, then the host control CPU **14** issues the pulse-like output prevention signal (see Fig. 9(b)).

10 The register **40**, which issues the logic value L before time "B", issues the linkage value H after the time period B causing a synchronization with an increase of the received output prevention signal.

11 Accordingly, the inverter **41**, which receives the output signal of the register **40**, issues the linkage value H before the time point "B", but the linkage value L after the time point "B" (see Fig. 9 (c)).

12 The AND circuit **42** for video data which permits or inhibits

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the transmission of the image signal in accordance with the output signal of the inverter **41**, issues a normal video signal "A" before such a time point "B" when an accounting count value X(g) is greater than 0. The AND circuit **42** then prevents the output of the video signal after the time "B" if the accounting count value X (g) is 0 (see Fig. 9 (d)).

13 Similarly, the AND circuit **43** for the PC signal that locks or permits forwarding of the PC signal in agreement with the output signal, of the inverter **41**, issues the PC signal to the outside of the software reproduction device **2** prior to the time "B" when the accounting counter value X(g) is greater than 0, whereas it locks the issue of the PC signal to the outside of the software reproduction device **2** after the time "B", when the accounting counter value X(g) is 0 (see Fig. 9 (f)).

14 It should be noted that the audio signal continues to be issued before and after the normal time "B" (see Fig. 9(e)).

15 Accordingly, in the event that the accounting count becomes 0 after the time of "B", such a display prevention causes the issue to the outside of the software reproduction device **2** to be prevented based solely on the image signal and the PC signal among the three output signals (image signal and voice signal PC signal). At this point, however, the audio signal remains for normal forwarding. Therefore, the software user is able to recognize that the accounting count X has become 0, without assuming that there is a malfunction in the software reproduction device **2**.

16 As described above in connection with this embodiment, the PC signal is prevented from being forwarded to the outside of the software reproduction device **2**, and it is therefore possible to prevent illegal use of computer sub-program. It should be noted that the audio signal is also delivered normally, but that profit, or profit for the software-authorized person, is not violated if the software on the image (such as a film, environmental or ambient video, etc.) is not violated. As can be seen this effect rather increases such the desire for continued use by the user of software. As a

result, the software user is willing to pay the fee for the use of the software as compensation for the removal of the SD circuit 9 from the software reproduction device 2.

1 The structure of the third embodiment is described in the following.

2 **Fig. 10** illustrates a block diagram showing the software reproduction structure of the third embodiment of the present invention.

3 There is a difference Between this embodiment and the second embodiment only in that an audio signal prevention circuit 50, which inputs the signal from the register 40, is connected between the MPEG expansion circuit 11b for audio data and the digital/ analog converter 13b for audio data. Accordingly only additional configurations will be explained in comparison with the second embodiment, while the other explanations are omitted.

4 **Fig. 11** illustrates a detailed structure of the audio signal prevention circuit 50. As is clear from **Fig. 11**, the output of the MPEG expansion circuit 11b for audio data is fed

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to an input terminal "b" on the input side of a multiplexer 501. An output signal of a mute signal generator circuit 500 is fed to an input terminal "a" of this multiplexer 501 on the input side. In contrast, an output signal of the register 40 as a counter-start signal is sent to the input side of a first counter 502 and as a reset signal to the input side of a second counter 506, and also to a first control terminal of the multiplexer 501 via an AND member 509. A counter value of the first counter 502 is sent to the input side memory access circuit 503. Furthermore, a pulse output signal of the first counter 502 is fed to the input side of a timing control member 507 and the second counter 506. An output signal of the memory access circuit 503, is fed to the input side of a code memory 504. An output signal of this code memory 504 is fed to the input side of a speech signal generation circuit 505. An output signal of this speech signal generating circuit 505 is fed to an input terminal "c" of the multiplexer 501. An output of timing control member 507 is inverted by an inverter 508 and fed to the other input terminal of the AND member 509. An output signal of the second counter 506 is fed to the input side of a second control terminal of the multiplexer 501.

5 The first counter 502 begins at the start of the recording signal with the counting within a fixed period of time and feeds the count to the memory access circuit 503. This memory access circuit 503 is used to access the code memory 504 in accordance with the counter value of the first counter 502. Thus, the first counter 502 acts as address counter of the code memory 504. Then, when its count value reaches the maximum value, the first counter 502 outputs a single pulse to the timing control member 507 and the second counter 506 and stops the count. The first counter 502 increases the count again, when the count value, on a delete signal from the timing control member 507, is reset back to a minimum value.

6 The code memory 504 stores language codes corresponding to individual languages (vowels, consonants, etc.), that form a speech sentence such as an alarm when the software usage amount exceeds a limit of use in a reproduction or reproduction sequence. Accordingly, each time that the first counter 502 counts up, access is made to the code memory 504 via the memory access circuit 503 and the alarm-language sentence of the corresponding language codes are output in succession. The content of the speech sentences, for example, "The used quantity has reached the limit. Please follow the procedures again and use the system. The Image is not displayed." This means that the corresponding language codes are sequentially disposed corresponding to successive addresses in the code memory 504 to compose the sentences or phrases. A memory 504 from the code string output voice code is supplied to the voice signal generation circuit 505.

7 The voice signal generating circuit 505 is a commercially available essential speech IC chip; it outputs a language code string passed into the corresponding digital voice signal. This gives the voice signal production circuit device 505, in the event that a corresponding alarm speech sentence is fed to it,

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a digital reproduction of the speaking language code string to the input terminal "c" of the multiplexer 501.

8 The timing control member 507 feeds a signal with the L linkage value to the inverter 508 during a normal state. On the pulse of the first counter 502, the timing control part 507 outputs the linkage value H during a fixed period of passed, for example, from about 10 to 20 sec. At the end of this fixed time period. The linkage value fed to the inverter 508 is set to L, and the delete signal is supplied to the first counter 502. The first counter 502 again counts to feed the alarm voice sentence of the voice signal generating circuit 505 of this delete signal.

9 The inverter 508 inverts the linkage value output from the timing control member 507 and feeds the inverted linkage value to the input terminal of the AND gate 509. Accordingly, the inverter 508, causes the AND gate 509, to feed the output of the register 40 directly to multiplexer 501 only when the output signal of the timing element 507 accepts the linkage value L, while the link value L is fed to the multiplexer 501 independently of the starting condition of the register 40 when the output signal of the timing control member 507 accepts the linkage value H from the timing control member.

10 The second counter 506 always feeds the link value L to the multiplexer 501 when the output signal of the register 40 accepts the linkage value L. This second counter 506 is reset when the output register 40 accepts the linkage value

H, reset and able to count. When the second counter **506** is able to count, it counts every impulse it receives from the first counter **502**. When this count reaches "5", the second counter **506** feeds the logic value H to the multiplexer **501**.

1 The mute signal generating circuit **500** is a circuit that outputs a fixed voltage.

2 The multiplexer **501** outputs a signal received from the input connections "a" to "c" to the digital/ analog converter **13b** for audio data, wherein the signal received from the AND member **509** and the signal received from the second counter **506** are used as control signals. This means that the multiplexer **501** outputs the audio signal of the MPEG expansion circuit **11b** for audio data outputs, which are received through the input terminal "b" when the output signal of the AND member **509** accepts L level and the output signal of the second counter **506** shows or accepts the L level. The multiplexer **501** outputs the digital output speech signal of the speech signal generating circuit **505**, which has been received through the input terminal "c", when the output signal of the AND member **509** accepts the H-level and the output signal of the second counter **506** indicates the L level. The multiplexer **501** outputs the fixed voltage of the mute signal generating circuit **500** that has been received through the input terminal "a", when the output signal of the second counter **506** indicates the high level.

3 In the following, the operation of the embodiment under consideration is explained in operational form.

4 The software reproduction device **2** in this embodiment form works form in the same manner as in the

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first embodiment, until the host control CPU **14** outputs the output prevention signal. Furthermore, the software reproduction device **2** works in the same manner as in the second embodiment with respect to the image signal and the PC signal, after the host control CPU **14** has output the output prevention signal. Accordingly, only the method of operation relating to the audio signal will be described.

5 As explained above, the register **40** continues the output signal with the linkage value L before accepting the output prevention signal from the host control CPU **14**. This link value L is fed to the input side of the first counter **502**, the AND member **509** and the second counter **506**. Accordingly, the first counter **502** does not start counting up, and therefore the timing pulse is not supplied to the input side of the timing control member **507**. For this reason, the AND member **509** is brought into an open state, whereby the linkage value L output by the register is fed to the first control terminal on the input side of the multiplexer **501**. The second counter **506** continues to output the value of the linkage value L to the second control terminal of the multiplexer **501**. Accordingly, the multiplexer **501** outputs the audio signal to the MPEG expansion circuit **11b** for audio data, which are fed to the input terminal "b" of the digital/ analog converter **13b** for audio data. As a result the software reproduces the corresponding information and tones from the speaker.

6 On receipt of the prevention signals from the host control CPU **14**, the register **40** continues with the output of the linkage value H. This linkage value H is fed to the input side of the first counter **502**, the AND member **509** and the second counter **506**. The first counter **502** begins to increment within the fixed time and to feed the count value sequentially to the memory access circuit **503**. The memory access circuit **503** undertakes an access to the code memory **504** in accordance with this count and reads out the appropriate language code from the alarm speech sentence string. The speech signal generating circuit **505** is fed on the input side with the code string of the speech and produces the digital speech signal and outputs this signal to the input terminal "b" of the multiplexer. The first counter **502** does not output pulses to the timing member **507** and the second counter **506** before the count of the first counter **502** has reached the maximum value. Thus, the AND member remains open before the count value of the first counter **502** reaches the maximum value. Accordingly, the linkage value H output from the register **40** is fed to the input side of the first control terminal of the multiplexer **501**. It should be noted that the reset signal shows the linkage value H that the second counter **506** is thus reset and thus brought into the countable state. However, at this time, the count value less than "5", and thus the linkage connection from the second counter **506** to the multiplexer **501** remains at L. Thus, the multiplexer **501** outputs the digital voice signal to the voice signal generation circuit **505** from which it is fed via the input terminal "c" of the digital/analog converter **13b** for audio data. As a result, the speaker alarm message is output by the, not shown, loudspeaker.

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7 The alarm prompts are triggered during the counts by the first counter **502**. When the count of the first counter **502** reaches the maximum value, the first Counters **502** issues the pulse to the timing member **507** and the second counter **506**. The timing control member **507** which receives the pulse, issues the logic value H to the inverter **508** for only from 10 to 20 sec. Therefore, the AND member **509** closes only for 10-20 sec, and outputs the logic value L to the first control terminal on the input side of the multiplexer **501**. It should be noted that the second counter **506** increments by 1 on receiving the pulse. However, the counter value is less than "5" at this time, which is the reason that the linkage value issued by the second counter **506** to the second terminal of the multiplexer **501** remains at L. Consequently, the multiplexer **501** issues to the D/A converter **13b** for audio data the audio signal of the MPEG expansion circuit **11b** for the audio signal which is supplied through the input terminal "b", for only 10-20. As a result, the software-based information or announcements and tones from the speaker (not shown) occur only for 10-20 sec.

- 1 After 20 seconds from the time of the input pulse, the timing control member **507** issues the delete signal to the first counter **502** and the linkage value L to the inverter **508** to open the AND member **509**. Thus, the first counter **502** performs the increment count again from the minimum value and the speech signal generating circuit **505** repeats the digital alarm voice signal to the input terminal "c" of the multiplexer **501**. Further, the AND member **509** issues the linkage value H to the first control terminal of the Multiplexers **501**. Therefore, the multiplexer **501** again issues the digital speech signal of the speech signal generating circuit **505**, which has been supplied via the input terminal "c", to the digital/analog converter **13b** for the audio signal. As a result, the alarm announcements are made by the speaker (not shown).
- 2 In the method described above, the software-generated alarm tones and announcements and speeches are issued alternately. If the alarm announcements or comments have been repeated five times, then the count value of the second counter **506** reaches "5", and linkage value issued by the second counter **506** to the second control terminal of the multiplexer **501** indicates the H level. Thus, the multiplexer **501** always issues low voltage to the mute signal generating circuit **500** which is supplied to the input terminal "a" to the voice-oriented digital/analog converter **13b** regardless of the linkage value which is fed to the input side of the first control terminal of the AND member **501**. The linkage value fed from the input side of the second control terminal of the second counter **506** remains at the H level, if the output signal from the register does not assume the L-level. Consequently, the announcements or statements and notes are no longer output by the speaker (not shown).
- 3 It should be noted that the output signal of the mute signal generating circuit **500** can be a signal of a fixed audible frequency, for example a tone signal of 1000 Hz.
- 4 As described above in connection with this embodiment, the picture signal

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and the PC signal, the output of the audio signal are completely stopped after the alarm signals for a fixed period of time. However, it can be considered that the request of the software user for continued use is encouraged by the speech, which is intermittently provided during the alarm signal intervals. As a result, the software user is ready, to pay the fee for using the software as compensation for the addition of the accounting counter value X by removing the SD circuit **9** of the software reproduction device **2**.

- 5 Hereinafter, the structure of the fourth embodiment is explained.
- 6 **Fig. 12** illustrates a block diagram showing the software structure of the reproducing apparatus used in a fourth embodiment of the present invention.
- 7 In the same manner as the first embodiment, this embodiment possesses a structure in which the number of operations of the expansion of the video data frame is counted, which is compressed according to the MPEG standards, and in that the accounting counter value X is subtracted corresponding to the number of the transactions. This embodiment further includes a structure such that, as a display prevention, the audio signal and the PC signal are completely stopped whereas the normal image signal is output when the accounting count value X becomes 0.
- 8 According to this embodiment, the format of the software released to the reproduction apparatus **2** is absolutely the same as in the first embodiment. Further, the same components of the software reproduction device **2** in this embodiment have the same reference numbers as those described in the first embodiment. Hereinafter, the explanation of the common elements will be omitted, while only a configuration of a device for preventing the display will be explained in accordance with the output-disabled signal, which is output from the host control CPU **14**.
- 9 The output signal or display prevention signal-issued by the host control of the CPU **14** is fed to the input side of register **40**. this register **40** outputs the logical value L in the initial state, but continues with the issue of the linkage value H if an increase of the input prevention signal is determined.
- 10 An output signal of the register **40** is inverted by an inverter **41**. Thus, in the initial state, the inverter **41** issues the linkage value from H, but continues to output the value of the linkage value L after issue of display prevention signal.
- 11 An output signal of the inverter **41** is supplied to the input terminal of an AND circuit **44** for audio data. The other input terminal of this AND circuit **44** for audio data is connected to an output terminal of the MPEG expansion detection circuit **11b** for audio data (MPEG-2). Accordingly, the AND circuit **44** for audio data serves as a gate or key switch for the speech signal that is fed to the D/A converter **13b** for audio data from expansion circuit **11b** for audio data on the input side. For this reason, transmission of the speech signal is only possible when the output signal of the inverter **41** has the linkage value H, and thus the analog signal output from the D/A converter **13b** for audio data

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is output to the speaker (not shown). When the output signal of the inverter **41** has the linkage value L, then the transfer of the speech signal is prevented, and thus no analog speech signal from the D/A converter **13b** for audio data is output.

- 12 The output of the inverter **41** is also fed to an input terminal of the AND circuit **43** of the PC signal. The other input terminal of the AND circuit **43** for the PC signal is connected to the output terminal of the MPEG expansion circuit **11c** for the PC signal (MPEG-2). Accordingly, it permits this AND circuit **43** for the PC signal, which serves as a gateway or key circuit to the PC signal, to forward the PC signal only when the output of the inverter **41** has the

linkage value H, while the forwarding of the affected PC signal is prevented or inhibited in the case that the output of the inverter 41 has the linkage value L.

It should be noted that an AND circuit serving as a gateway or key circuit, for video data is not provided at the output terminal of the MPEG expansion circuit 11a for video data. Thus, even in the case that the delivery or output prevention signal is output from the host control CPU 14, the analog video signal from D/A converter 13 for video data is issued as normal.

Incidentally, the register 40 issues the linkage value L from when the reset signal is transmitted from the host control CPU 14.

In the following the operation of the embodiment will be explained.

The software reproduction device 2 according to this embodiment is in the same manner as that in the first embodiment, until the host CPU 14 outputs the output prevention signal. Accordingly, the operation will be explained here merely from where the host control CPU 14 has submitted the display prevention signal.

If the value stored in the accounting data memory 8 accounting count value X is 0 as a result of the decrement, then the signal state as shown in Fig. 13 extends in each unit. Fig. 13 shows that the accounting X count becomes 0 at a time point "C" (see Fig. 13(g)).

The DES device 7 decrypts the data even after the accounting count X has become 0, which is the reason that the normal audio signal is continued by the MPEG expansion circuit 11b for audio data after the time "C" (see Fig. 13(a)).

Then, the host control CPU 14 outputs the pulse-type output-prevention signal, if the accounting counter value X at time "C" becomes 0 (see Fig. 13(b)).

The register 40, which outputs the linkage value L before the time "C", issues the linkage value H after time "C", which is synchronized with the increase of the received display prevention signal.

Accordingly, the inverter 41, which receives the output of the register 40 before the time "C" outputs the linkage value H and the linkage value L after the time "C" (see Fig. 13(c)).

The AND circuit 44 for audio data, which permits or prevents the transmission of the speech signal in accordance with the output signal of the inverter 41, outputs a normal audio signal prior to the time "C"

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when the accounting counter value is X(g) is greater than 0. The AND circuit 44, however, prevents the release of the audio signal after time "C" if the accounting count X(g) is 0 (see Fig. 13(e)).

Similarly, the AND circuit 43 for the PC signal, which allows or locks the forwarding of the PC signal in accordance with the output signal of the inverter 41, issues the PC output signal to the outside of the device 2 before the time "C" when the accounting count X(g) is greater than 0, while the output of the PC output signal to the outside of the device 2 after time "C" is locked or prevented when the accounting count X(g) becomes 0 (see Fig. 13(f)).

It should be noted that the normal picture signal is also delivered before and after the time "C" (see FIG 13(d)).

Accordingly, after the time of "C", in the event that the accounting counter value is 0, such a display prevention is called up, that the discharge to the outside of the software prevention device 2 is prevented or locked only with respect to the audio signal and computer signal among the three output signals (image signal, speech signal and PC signal). At this time, however, the normal output of the image signal is maintained. Therefore, the knowledgeable user of software is able to recognize that the accounting count value X is 0 without a misinterpretation of an error in the device 2.

As described above and in accordance with this embodiment, the forwarding of the PC signal is locked to the outside of the software reproducing device 2, and therefore it is possible to prevent illegal use of the computer program. It should be noted that the normal output of image signal is continued, however, the profit of the software authorized person is not violated if the software is based on language or sound (e.g., a video of a classical music concert, a karaoke video, a language study video, etc.). Much rather, as will be appreciated, an effect is called up such that the desire for continued use by the user of the software is increased. As a result the software user will be ready to pay the fee for the use to the software vendor as compensation for adding to the accounting count X or for removing the SD circuit 9 of the software reproduction device 2.

Hereinafter, the structure of the fifth embodiment will be explained.

Fig. 14 illustrates in a block diagram the structure of the fifth embodiment of the present invention of software reproduction device.

This embodiment has the same implementation as the first embodiment that the number sequences of expansion of the video data frame count compressed based according to MPEG standards and the accounting counter value is subtracted in accordance with the number of the operations concerned. This embodiment further includes a form structure such that a brightness and darkness of the image signal during the normal display of the audio signal and the PC output signal is inverted as a display prevention when the accounting counter value becomes 0.

According to this embodiment, the format of the software

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released to the software reproduction device 2 is now absolutely the same as in the first embodiment. Further, the same components of the software reproduction device 2 in this embodiment are referred to with identical reference

numerals as those of components in the first embodiment. Hereinafter, an explanation of the common elements will be omitted, whereas only a configuration of a device for preventing the delivery in accordance with the output prevention signals which are transmitted from the host CPU **14** will be explained.

1 In this embodiment, the adding circuit **19** of the first embodiment is not prepared. Therefore, the output signal of the A/D converter **13a** for video data is output directly to the outside of the software reproduction device **2**. According to this embodiment, an exclusive OR circuit **45** is inserted between the (MPEG-2) expansion circuit **11a** for video data and the A/D converter **13a** for video data. Described in further detail, this means that an outlet line from the MPEG expansion circuit **11a** for video (MPEG-2) consists of an output line for a blue color video signal, an output line for a green-color video signal and an output line for a red-color video signal. The output line for each color video signal then consists of an output line for a signal indicating the intensity, and an output line for a signal for indicating a polarity. The above exclusive-OR circuit **45** is provided in the output line, indicative of the polarity in the respective color. This means that this polarity signal is fed to one input terminal of the exclusive OR circuit **45**. Further, an output signal of the registers **40** is fed to the other input terminal of the exclusive-OR circuit **45**. The register **40** receives the display prevention signal of the host CPU **14**. Then, the register **40** outputs the linkage value L in the initial state, but continues to output the linkage value H when an increase in the input side prevention signal is detected. The exclusive OR circuit **45**, in the case that the output signal of the register **40** has the linkage value L, enables a forwarding of the polarity signal of the MPEG expansion circuit **11a** for video data, while inverting the polarity signal of the MPEG expansion circuit **11a** for video data when the output signal of the register **40** assumes the linkage value H, and then enables further transmission of this inverted signal. As the result, the analog signal forwarded by the D/A converter **13a** for video data in the case that the output signal of register **40** has the linkage value of L, shows a normal picture on the TV monitor (not shown), whereas in the case that the output signal of the register **40** has the linkage value H, it shows a picture of inverted brightness on the TV monitor (not shown).

2 It should be noted that the above-mentioned linkage circuit is not connected with the output terminal of the MPEG expansion circuits **11b** and **11c** for the audio signal and the PC signal. Thus, even in the case that the display-prevention signal is output from the host control CPU **14**, the audio signal and the PC signal are displayed as normal.

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3 It should be noted that the register **40** outputs the linkage value L, when the reset signal is transmitted from the host CPU control **14**.

4 The operation of the embodiment will be explained.

5 According to this embodiment, the software reproduction device **2** operates in the same manner as in the first embodiment up to the host CPU **14** and outputs the prevention signal. Accordingly, only the operation will be explained after the host control CPU **14** has issued the display prevention signal.

6 If the value stored in the accounting data memory **8** accounting count value X as a result of the decrement is 0, then the signal condition in each unit is as shown in Fig. 15. Fig. 15. shows that the accounting counter value X at a time "D" becomes 0 (see Fig. 15(g)).

7 The DES device or circuit **7** decrypts the data even after the accounting count value X is 0, and thus the output of the normal analog video signal from the MPEG expansion circuit **11a** for video data continues after the time "D" (see Fig. 15(a)).

8 When the value of the accounting counter X at time "D" is 0, then the host control CPU **14** outputs the pulsed-type display prevention signal (see Fig. 15(b)).

9 The register **40**, which outputs the linkage value L before the time "D", outputs the linkage value H, after time "D", whereby a synchronization with an increase of the accepted display prevention signal is present.

10 The exclusive-OR circuit **45**, which accepts the output signal of the register **40** via its own input terminal, directly outputs the polarity video signal accepted by the other input terminal before time "D". Accordingly, the normal analog video signal is released from the video DAC **13a** for video data. In contrast to this, the exclusive-OR circuit **45** after the time "D" inverts the video polarity signal received from the above-named other input terminal and issues this inverted signal. Thus, the inverted brightness in the analog video signal is output from the D/A converter **13a** for video data (see Fig. 15(d)).

11 It should be noted that the displays of the audio signal and the PC output signal are normally continued (see Fig. 15(e) and 15(f)).

12 Accordingly, after time "D", when the accounting count becomes 0, such a display prevention is called up, that the brightness of the picture, with reference only to the picture signal of the three output signals (picture signal, audio signal, PC Signal) is inverted. At this time, however, the voice signal and the PC signal are further output normally. Therefore, the viewer of the television monitor device (not shown) is able to identify that the accounting counter value X is 0 without having the impression that there is a malfunction in the device **2**.

13 At this moment, the audio signal and the PC signal will continue to be forwarded normally. If the software is based mainly on the image (e.g., a film, animation, etc.), a profit to the person authorized to use software is not injured.

1 Much rather, as will be appreciated, an effect is called up such that the desire for continued use by the user of the software is increased. As a result the software user will be ready to pay the fee for the use to the software vendor as compensation for adding to the accounting count X or for removing the SD circuit 9 of the software reproduction device 2.

2 Hereinafter, the structure of the sixth embodiment is explained.

3 **Fig. 16** illustrates in a block diagram the structure of the sixth embodiment of the present invention using software rendering means and the software reproduction device.

4 This embodiment, in the same manner as the first embodiment, possesses a structure in which the number of expansions of the video data frame is counted and which are being compressed on the basis of the MPEG standards, and that the accounting counter value X is set and decremented in accordance with the number of operations concerned. Moreover, this embodiment has such a structure in that, as output prevention in the event that the accounting counter value X is 0, the output of the image signal is superimposed by a dummy or blind signal, while the output of the normal audio signal and the PC signal are continued.

5 According to this embodiment, the format of the plurality of software stored in the CD-ROM 1 is explained. **Fig. 17** illustrates in a block diagram, a configuration of a circuit, which is used when the CD-ROM 1 stores this video data. According to **Fig. 17**, F1, F2, . . . denote analog picture frames. Furthermore, the symbol D denotes dummy or blind data. These blind data fields include the use of the image data for the display of patterns, for example, based on random numbers. These frames D, F1, F2, . . . are fed successively to an A/D converter 51. The A/D converter 51 converts the frame D, F1, F2, . . . into digital data. An output of the A/D converter 51 is fed to a blind data recovery circuit 52 and an adding circuit 53. This blind data recovery circuit 52 extracts only the blind data D from the data parts fed to the input side. In the adding circuit 53, the blind data D, extracted by this extraction circuit 52, are superimposed on the frames F1, F2, . . . , which are supplied directly to the adding circuit 53 from the A/D converter 51. Thus, the adding circuit inputs D, D + F1, F2 + D. The output signals D, D + F1, F2 + D of the adding circuit 53 are then fed to a MPEG-2 encoder 54, and then compressed in accordance with the MPEG-2 standards. The frames D, D + F1, F2 + D, . . . compressed by this MPEG-2 encoder 54, are described below with D', F'(F1 + D), F'(F2 + D), The output signals D', F'(F1 + D), F'(F2 + D), . . . of the MPEG-2 encoder 54 are subsequently fed to an input side of an encryption circuit 55. This encryption circuit 55 creates the encryption by use of a specific encryption key. The frames D', F'(F1 + D), F'(F2 + D), . . . , encrypted by this encryption circuit 55 are then written to the CD-ROM 1. In fact, these frames are briefly written on an original plate and then the resulting bit patterns are printed on commercially available CD-ROM 1.

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6 It should be noted that the blind data D cannot be placed at the start or head of the speech signal, which is why the blind data D is not added by the adding circuit 53, but is fed directly to the MPEG-2 encoder 54. Further, the blind data D are not used in view of the computer program, and are therefore fed directly to the input side of the MPEG-2 encoder 54. The computer program, is not compressed according to the MPEG-2 standard, but only encrypted by the encryption circuit 55.

7 The CD-ROM 1 stores the data subjected to analog/digital processing, encryption processing, and compression processed data. The data format of the software with the same compression device 2 are input via the connection from the software vendor and demodulated by a modem 51.

8 The majority of components of the software reproduction device 2 according to this embodiment are the same as those in the software reproduction device 2 according to the first embodiment form. Accordingly, as with the first embodiment they have the same reference numerals as in the first embodiment for the same components of the software. In the following, the explanation of these common elements is omitted, while only the construction of a device for prevention of the delivery in accordance with the output prevention signal by the host control CPU 14 is explained.

9 According to this embodiment, the adding circuit 19 used in the first embodiment from is not used. Therefore, the output of the A/D converter 13a for a video input device is fed directly to the outside of the software reproduction device 2. According to this embodiment, a processing unit as shown in **Fig. 18**, is provided between the MPEG expansion circuit 11a for video data (MPEG-2) and the A/D converter 13a for a video data.

10 The MPEG-expansion circuit 11a for video data outputs the signal to this processing unit 46, expands the data frames D', F'(F1 + D), F'(F2 + D), . . . decoded by the DES unit 7. The recovered data frames D, D + F1, F2 + D, . . . are fed to the input side of the processing unit 46.

11 In contrast, the display prevention signal from the host CPU control 14 is fed to the input side of the register 40. This register 40 outputs the linkage value from L in initial state but continues with the output of the linkage value H if the increase of the fed-in display prevention signals is detected.

12 The output signal of the register 40 is inverted by the inverter 41. Thus, the inverter 41 outputs the linkage value H at the initial state, but continues to output the linkage value L link after output of the display prevention signal.

13 The output signal of inverter 41 is fed to an input terminal of the AND circuit 43 for a PC signal. The other input terminal of this AND circuit 43 for a PC signal is connected to an outer side of the MPEG-expansion circuit 11c for video data (MPEG-2). Accordingly, this AND circuit 43 for a PC signal serves as a gate or key

circuit for the PC signal. Therefore, a forwarding of this PC signal is only possible when the output signal of the inverter **41** has the linkage value **H**, while it is locked in the case that the output of the inverter **41** has the linkage value **L**.

The output signal of inverter **41** is also fed to the input side of the processing unit **46**. With regards to **Fig. 18**, a specific configuration of the processing unit **46** will be described. According to **Fig. 18** an output line of the MPEG expansion circuit **11a** for video (MPEG-2) is connected with the blind data extraction circuit **47** and a subtraction circuit **49**. An output line of the blind data extraction circuit **47** is connected to the Subtraction circuit **49** through a switch circuit **48**. The blind data extraction circuit **47** extracts only the blind data frame from the data frames $D, D + F1, F2 + D, \dots$, that are issued by the MPEG expansion circuit **11a** for video data (MPEG-2) and continues with the display of his blind data frame **D**. The switching circuit **48** undertakes a standard link-opening and closing of a signal line between the blind data extraction circuit **47** and the subtracting circuit **49** in accordance with the output signal of the inverter **41**. When the output signal of inverter **41** accepts the linkage value **H**, then especially this signal line for displaying the blind data frame **D** to the subtractor **49** is closed. In contrast, when the output of the inverter **41** has the linkage value **L**, the switch circuit **48** opens this signal line in order to lock the display of the blind frame **D** to the subtracting circuit **49**. The subtraction circuit **49** undertakes a link-standard subtraction of the blank data accepted by the circuit **47** of the $D + D$ data frames $F1, F2 + D, \dots$, which have been received from the MPEG expansion circuit **11a** (MPEG-2). This occurred after carrying out the subtraction of the input data frame from the subtracting circuit **9** with $D, F1, F2, \dots$. Implementing the other subtractions of the other is limited to a single case in which the switch circuit **48** closes a signal line to receive the output signal with the linkage value **H** by the inverter **41**.

In contrast, the switching circuit **48** opens when the inverter **41** outputs the linkage value **L**, and the blind data **D** of the subtractor **41** is therefore not fed to the input side. Accordingly, the data $F1 + D, D + F2, \dots$, which were accepted by the MPEG-expansion circuit **11a** for video data (MPEG-2) are not subtracted. thus, the subtraction unit **49** forwards the received data frame $D, D + F1, F2 + D, \dots$ directly to the digital/ analog converter **13a** for video data.

It should be noted that the above-mentioned processing unit **46** is not connected to the of the MPEG expansion circuit **11b** for video data and the MPEG- circuit **11c** for the PC signal. Therefore, even in the case that the display prevention signal is output from the host control CPU **14**, the analog audio signal and the PC signal are output as normal.

It should be noted that the register **40** stops the output of the linkage value **L** when the reset signal is transmitted from the host CPU control **14**.

The operation of the embodiment will be explained in the following.

According to this embodiment, the software reproduction device **2** operates in the same manner as in the first embodiment until the host control CPU **14** outputs the display prevention signal. Accordingly, only the operation after the host control CPU **14** has submitted the display prevention signal is described.

If the value stored in the accounting data memory **8** accounting count value **X** is a result of incrementing **0**, then the signal state takes place in each unit illustrated in **Fig. 19**. **Fig. 19** shows that the accounting counter value **X** at a time "E" becomes 0 (see **Fig. 19(g)**).

The DES device **7** decrypts the data even after the accounting count, **X** reaches 0, which is why the same video signal is added to the blind which are displayed like the previous one, at the time the "E" see **Fig. 19(a)**). In the case that the accounting counter value **X** at time "E" is 0, the host control CPU **14** issues the pulse-like display prevention signal (see **Fig. 19(b)**).

The register **40**, which had issued the linkage value **L** before the time the "E", delivers the linkage value **H** after the time "E", which is synchronized with the increase of the display prevention signal. Accordingly, the output of the register **40** of the linkage value **H** is received by the inverter **41** before time "E", but the linkage value **L** after the time the "E" (see **Fig. 19(c)**).

The AND circuit **43** for the PC signal, which permits or locks the forwarding of the PC signal in accordance with the output signal output of the signal inverter **41**, issues the PC signal before a time "E" when the accounting count value $X(g)$ is greater than 0, whereas it blocks the discharge of the PC signal to the outside of the device **2** after the time "E" when the accounting counter value $X(g)$ is 0 (see **Fig. 19(f)**).

The circuit **48** enables or locks the transmission of blind data **D** extracted by the extraction circuit **47** in accordance with the output signal of the inverter **41**. As a result, the subtraction circuit **47**, that is, the processing unit **46** issues the data frames $D, F1, F2, \dots$ to the D/A converter **13a** for video data prior to the time "E" when the accounting counter value is $X(g)$ is greater than 0. For this reason, the D/A converter **13a** for a video data is capable of delivering the analog video signal for displaying a normal image on the television monitor unit (not shown). The initial blind data frame **D** is not displayed. Furthermore, the subtraction circuit **47**, namely, the processing unit **46**, issues the data frames $D, D + F1, F2 + D, \dots$, which remain with the added blind data **D** to the D/A converter **13a** for video before the date "E" when the accounting count $X(g)$ becomes 0. It therefore follows that the D/A converter **13a** for video data issues the video signal (which are to be added to the blind data) for the display of a non-recognizable image to the television monitor unit(not shown).

1 It should be noted that the audio signal is normally continually output before and after the time "E" (see **Fig. 19(e)**).

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2 Accordingly, after time "E", in the event that the accounting counter value is 0, a display prevention is caused such that the blind data D for the display of the unrecognized picture are not eliminated as regards the picture signal and further a display prevention is output that the display to the outside of the software reproduction device **2** with respect to the PC signal among the three output signals (image signal, audio signal and PC signal) is locked. At this time, however, the normal display of a speech signal C is maintained. Therefore, the user of the television monitor unit (not shown) is able to recognize that the accounting count value X is 0 without evaluating it as an incorrect loading caused by a malfunction in the device **2**. If the software is based mainly on the image (e.g., a film, animation, etc.) then a profit by the person authorized to use the software, by the way, is not violated even when the audio signal is displayed as normal. Much rather, as will be appreciated, an effect is called up such that the desire for continued use by the user of the software is increased. As a result the software user will be ready to pay the fee for the use to the software vendor as compensation for adding to the accounting count X or for removing the SD circuit **9** of the software reproduction device **2**.

3 Modified examples are explained further in the following.

4 In each of the above embodiments, the prevention processing is undertaken such that the image or tones or announcements in respect of the image signal and the audio signal are processed. However the following exclusionary device is acceptable for a personal computer-based signal delivery, meaning the PC signal illustrated for each of the figures relating to the relevant embodiment.

5 Such a restriction device is explained, for example, with reference to **Fig. 2**.

6 To the operating program of the host control CPU **14** there is added a working operating program for the display of a reproduction image signal via the input/output I/O unit **6b** before the DES device **7** decrypts the accounting target software when the accounting count value X in the accounting data memory **8** is 0.

7 In this case it is necessary that the host control CPU **14** is provided with a memory for storing the image signal prevention program. At the same time, it is necessary that a circuit for separating or as an interface at a read output of the memory or with respect to the PC signal be connected. A prevention picture program is generated on the basis of a program system affiliated with the present device **2** of the present personal computer. The prevention picture program is structured so that it is to start immediately after the personal computer has installed a program from the CD-ROM **1**. The disability-image program is made up of prevention image data and a command to read this item of the prevention image data from an address location in which the data are stored, and output the data to a display device such as a cathode ray tube, etc. of the personal computer. The prevention image data are used, for example, to display a message "The desired program is not usable because of the accounting limit."

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Please bring the SD card to your nearby sales shop".

8 In the following, the operations of the host controller-CPU **14** will be explained.

9 The control CPU **5** immediately shows the relevant effects on the host CPU **14** when a content of the data memory **8** accounting present, meaning that it has the effect that the accounting counter value X is 0. The host control CPU **14** stores this effect in a register area of memory and starts the operation program for reading the prevention image signal program. The operating program works in such a way that the image prevention output program is read from program memory (not shown) byte by byte. Then the image prevention output program is fed to the demultiplexer **10** via the I/O unit **6b**. Then, this image prevention output program is subjected in form of the PC signal to a demultiplexing effect and then forwarded via the MPEG expansion circuit **11c** for video data to the personal computer (not shown). The output signal for this, not shown, personal computer is effected in a serial or byte-serial manner. When the reading and display of image prevention output program are completed, then the host control CPU **14** ends the operation, but is placed in a waiting or standby state for the next process. In contrast, the personal computer connected with this software reproduction device **2**, in the event that the output image prevention output program is fully installed, starts this prevention output program as an initialization program. In this start-up, the image prevention output program is assigned to a particular address region of the main memory of the personal computer. Then the prevention image data are developed in an image memory, etc. The developed image is displayed on a monitor display unit of the personal computer by means of an output. The display prevention can thus be carried out for the PC-based software application that is read from the CD-ROM **1**. The software user is then able to recognize the need to pay the fee for use from the displayed image prevention.

10 As explained above in detail, the preventions are mechanisms for the corresponding displays in the depicted embodiments that are taken into account independently of each other. The embodiments in the above-mentioned prevention mechanisms shown may be combined in a variety of ways within the present invention. Thus, for example, the embodiment in **Fig. 2** of the structure of the superimposition and display of the prevention display patterns on the

decoded image signals. However, such a structure can be undertaken such that the audio signal passes through device **50**, by means of a voice signal prevention switch, as is illustrated in **Figs. 10 and 11**. Further, with respect to the PC signal, the switch construction, on the basis of a further modified embodiment described above, may be included in the control CPU **14**. Moreover, in the sixth embodiment shown in **Fig. 16**, a structure is shown, in accordance with which the digital/analog conversion is undertaken, wherein the blind data is added to the decoded image signal.

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However, such a structure may be undertaken that the audio signal passes through the audio signal prevention circuit **50**, as is illustrated in **Figs. 10 and 11**. Also with regard to the PC signal of the further embodiment mentioned above may be incorporated in the control CPU **14**.

1 According to the present invention, in the case of the use of the software beyond the defined amount, the use of the software can be prevented while the software user is made aware of the fact that the software usage amount has reached the specified usable amount in that data is displayed in incomplete form.

Claims

- 1 An apparatus for managing a software usage amount in a device for providing a signal to the outside through the use of software, **characterized in that** a detecting means (**101**) is provided for detecting the amount of use of the software, that determination means (**102**) is provided which determines that the detecting means (**101**) identified software usage amount reaches a certain amount of use, and that a signal display prevention device (**103**) is provided, which hinders a normal display of the signal to the outside when the determination means (**102**) determines that the software usage amount reaches a defined amount of use.
- 2 Apparatus according to claim 1, **characterized in that** the signal display prevention device (**103**) is caused to deliver the signal to the outside in an incomplete form in the case that the determination means (**102**) determines that the software usage amount has reached the defined amount of use.
- 3 Apparatus according to claim 2, **characterized in that** the signal output to the outside is a video signal.
- 4 Apparatus according to claim 3, **characterized in that** the discharge prevention means superimposes any signal to the video signal and the superimposed signal is output in the case that the determination means (**102**) determines that the software usage amount reaches the defined amount of use.
- 5 Apparatus according to claim 4, **characterized in that** said signal is a character data signal for displaying a character.
- 6 Apparatus according to claim 3, **characterized in that** the prevention signal display prevention device (**103**) inverts a polarity of the video signal and that such a signal with polarity inverted is output to the outside in the case that the determination means (**102**) determines that the software usage volume has reached the defined amount of use.
- 7 Apparatus according to claim 2, **characterized in that** blind data of the software are previously superimposed and that the display prevention device only removes the blind data from the software in the case that the determination means (**102**) determines that the software usage amount lies within the amount of use.

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- 8 Apparatus according to claim 2, **characterized in that** the signals output to the outside are such a plurality of interrelated signals that they are to be displayed in synchronization with each other, and that the display prevention means locks some types of signals among the plurality of types as regards display to the outside in the case that the determination means (**102**) determines that the use of software usage has reached the defined amount of use.
- 9 Apparatus according to claim 8, **characterized in that** the plurality of types of signals including a video signal and an audio signal, and that the display determination means prevents or blocks the delivery of the audio signal to the outside, while the output of the video signal is to the outside, when the determination means (**102**) determines that the use of software usage has reached the defined amount of use.
- 10 Apparatus according to claim 8, **characterized in that** the plurality of types of signals includes a video signal and an audio signal, and that the display prevention means prevents or blocks the delivery of the video signal to the outside, while the output of the audio signal is to the outside, if said determining means (**102**) has determined that the use of software quantity has reached the defined amount of use.

- 11 Apparatus according to claim 2, **characterized in that** the display to the outside comprises an audio signal and that the display prevention means stops the output of the audio signal to the outside, however it causes the delivery of an alarm tone signal to the outside in the case that the determining means (102) determines that the software usage amount has reached the defined amount of use.
- 12 Apparatus according to claim 11, **characterized in that** the display prevention means includes a timing member by means of which a period of time is controlled during which the alarm tone signal is alternately repeated between the audio signal and the alarm tone signal to the outside in accordance with the output signals of the timing control member.
- 13 Apparatus according to claim 12, **characterized in that** the display prevention means further comprises a counter in which the number of times the alarm tone signal has been output is counted and blocks the output of the audio signal and the alarm signal to the outside in the case that a counting value of the respective counter has reached a defined value.
- 14 Apparatus according to claim 2, **characterized in that** the output signals to the outside form a computer program, and that the display prevention means program is an image signal, which operates at startup of a computer, for display of an alarm record to the computer, that is linked to the means of managing the software usage amount and in which the computer program is installed when the affected prevention means (102) determines that the software usage amount has reached a defined amount of use.

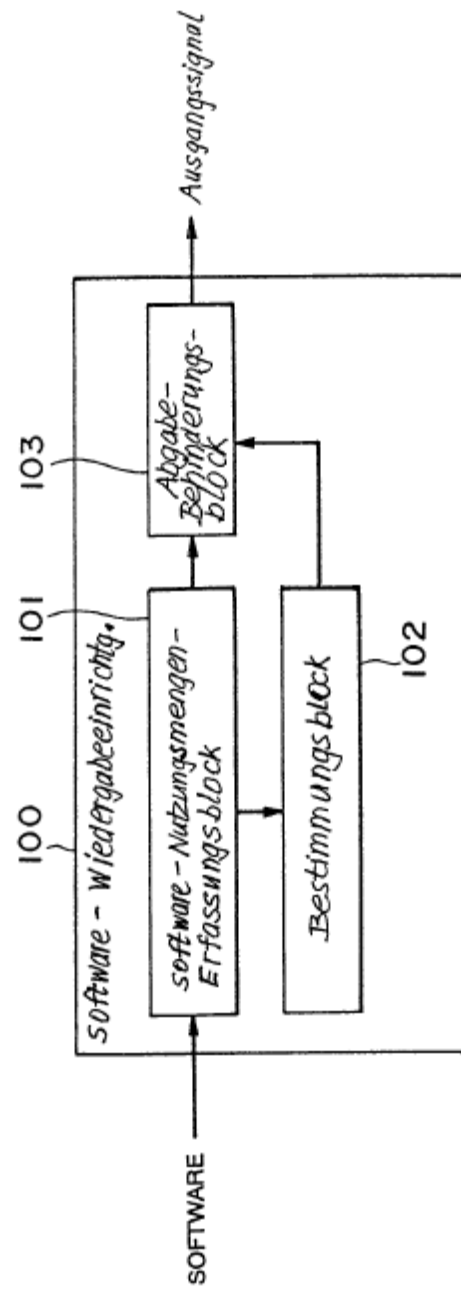
38

- 15 Apparatus for managing a software usage amount in an installation for displaying a signal to the outside by use of software, **characterized in that** a detecting means (101) is provided, which determines the amount of use of the software, that determination means (102) is provided that determines that the detecting means (101) identifies when a defined software usage amount reaches a defined amount of use, and in that a disposal device (103) is provided that removes the blind data, which has previously been superimposed on the software, only in the case that the determination means (102) determines that the software usage amount is within the defined usage amount.
- 16 Apparatus for managing a software usage amount in an installation for displaying a signal to the outside by use of software, **characterized in that** a detecting means (101) is provided, which determines the amount of use of the software, that a determination means (102) is provided that determines that the software usage amount determined by the detecting means (101) reaches a predetermined used amount, and in that a display means is provided, which displays an image signal of the program that runs in start-up of a computer, for displaying an alarm record to the computer, which is connected to the device for managing the software usage amount and in which the computer program is installed when said determination means (102) determines that the software usage amount has reached a certain amount of use.
- 17 Apparatus according to claim 11, **characterized in that** a time control device is provided for restricting the time during which it can stop the alarm tone signal that is output, wherein after the period in question no sound and audio signal is output.

19 Pages of drawings

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FIG. 1

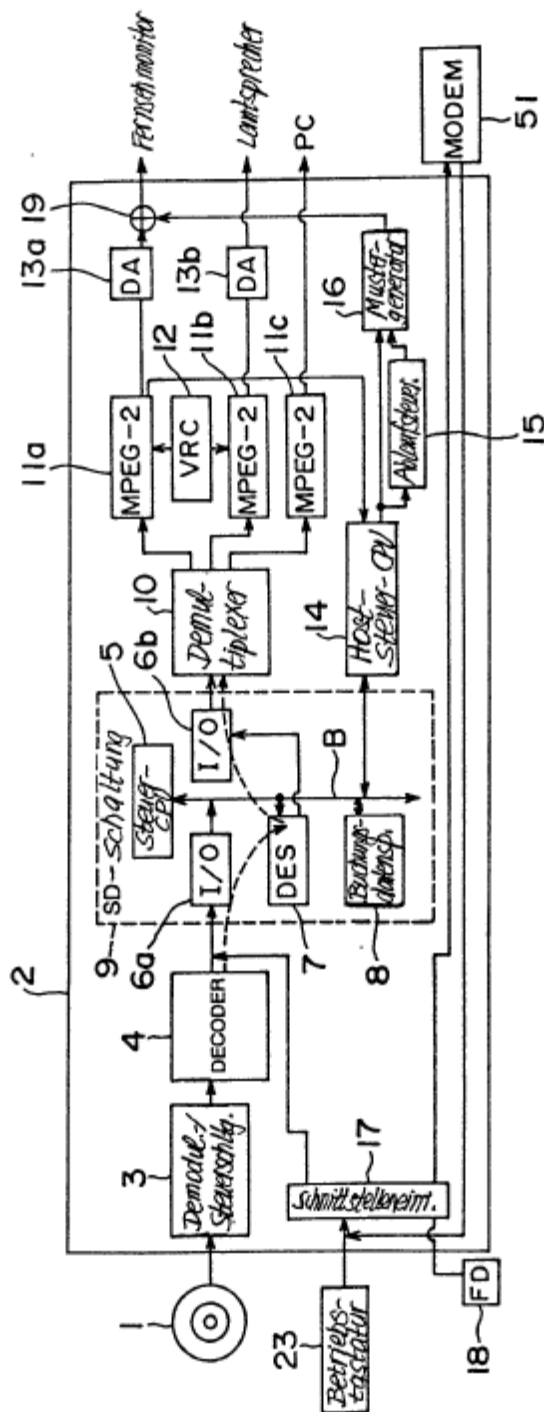


Output signal

- 100** Software reproduction device
- 101** Usage amount detection unit
- 102** Determination unit
- 103** Output-prevention unit

Software

FIG. 2



- TV monitor
- Loudspeaker
- PC
- 51 MODEM
- 3 Demodulation/control circuit
- 4 Decoder
- 5 Control CPU
- 8 Accounting memory
- 9 SD circuit
- 10 Demultiplexer
- 14 Host control CPU
- 15 Sequence control device
- 16 Pattern generator
- 17 Interface unit
- 23 Operating keyboard

FIG. 3

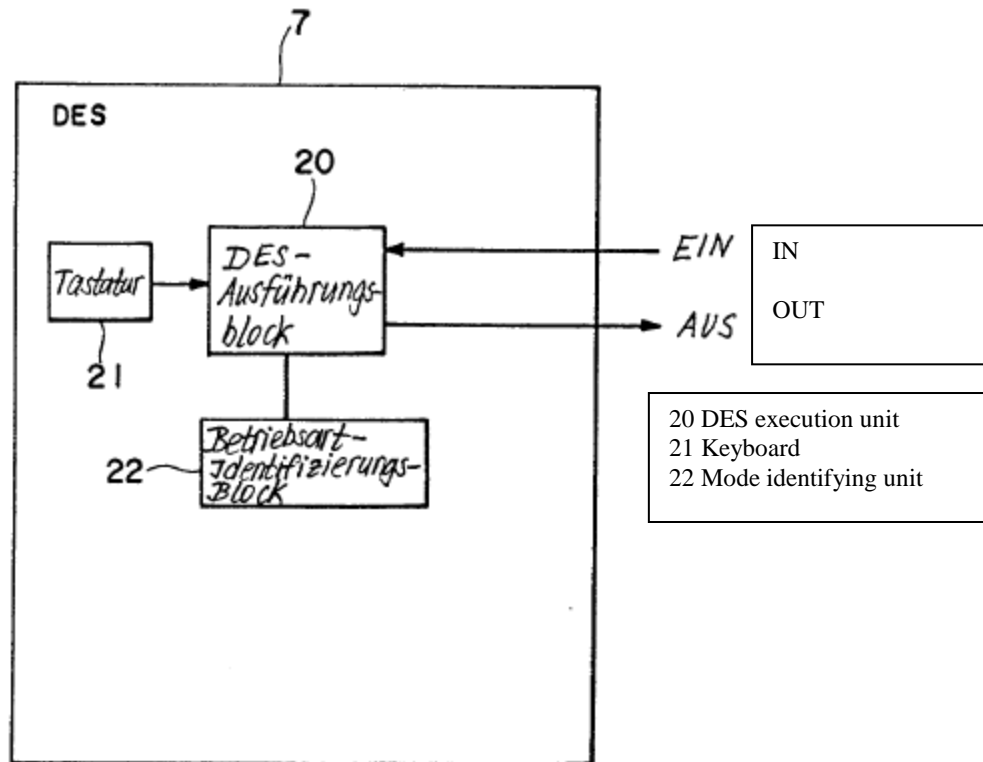
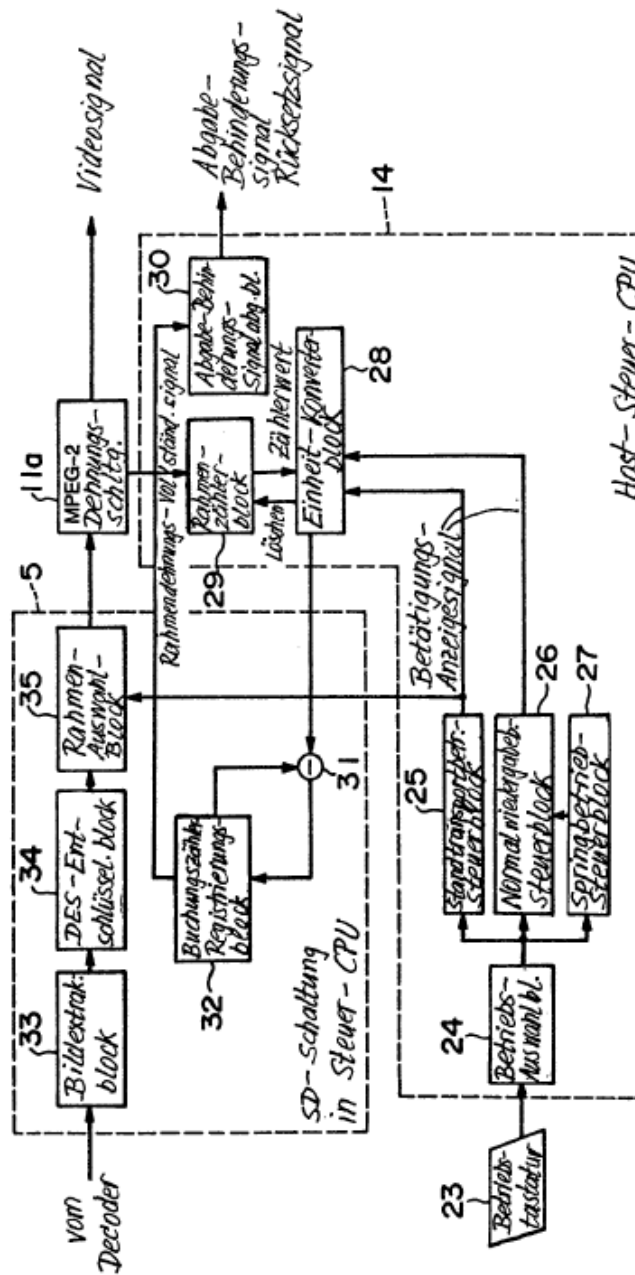


FIG. 4



Video Signal
Display prevention signal
Reset signal

- 11a Expansion circuit (MPEG-2)
- 14 Host control CPU
- 23 Operating keyboard
- 24 Mode selection block
- 25 Condition transport operation control block
- 26 Normal reproduction mode control block
- 27 Jump-operation control block
- 28 Converter block
- 29 Frame-counter block
- 30 Display prevention signal output block
- 32 Counting counter register block
- 33 Image extraction block
- 34 DES encryption block **34**
- 35 frame selection block

SD Circuit in control CPU

From decoder

FIG. 5

Ja = Yes
Nein = No

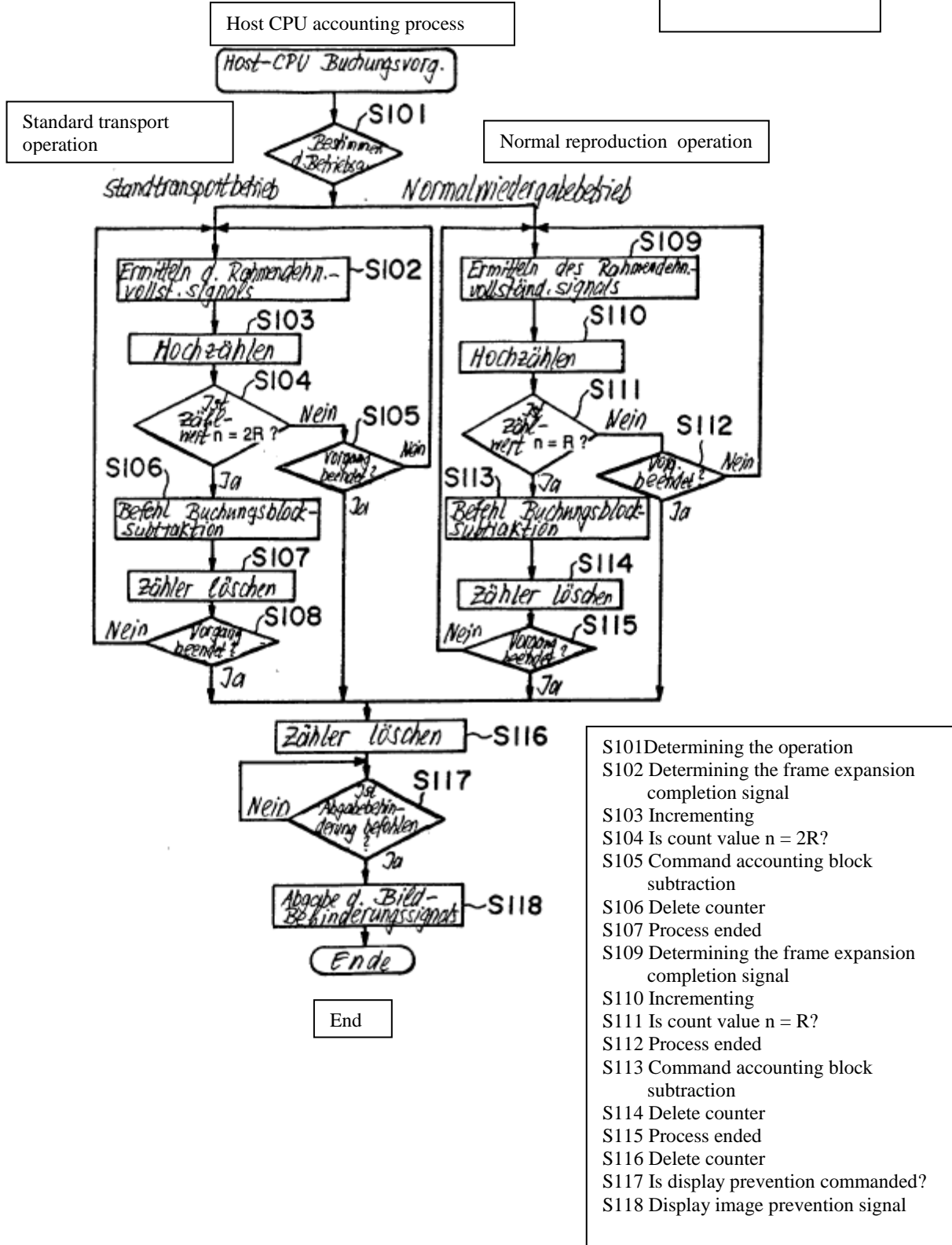


FIG. 6

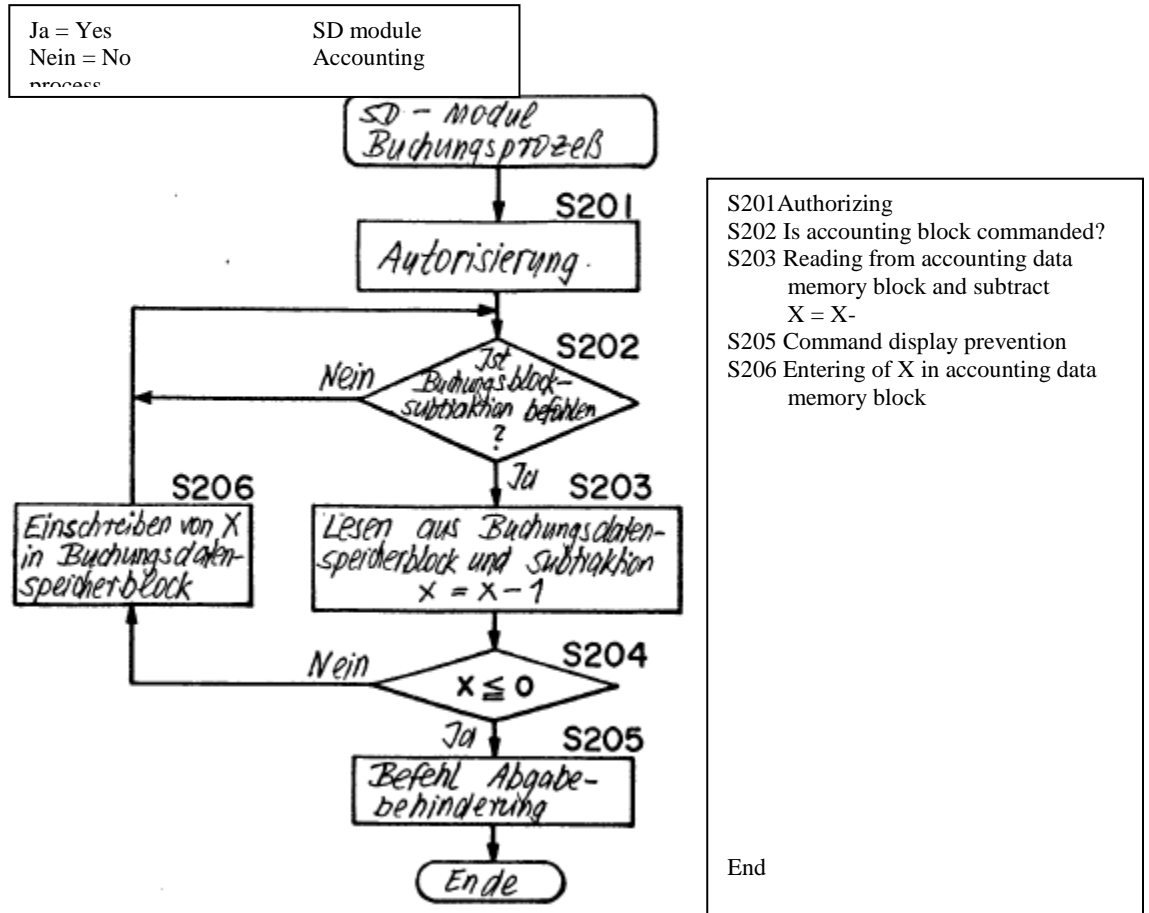


FIG. 7

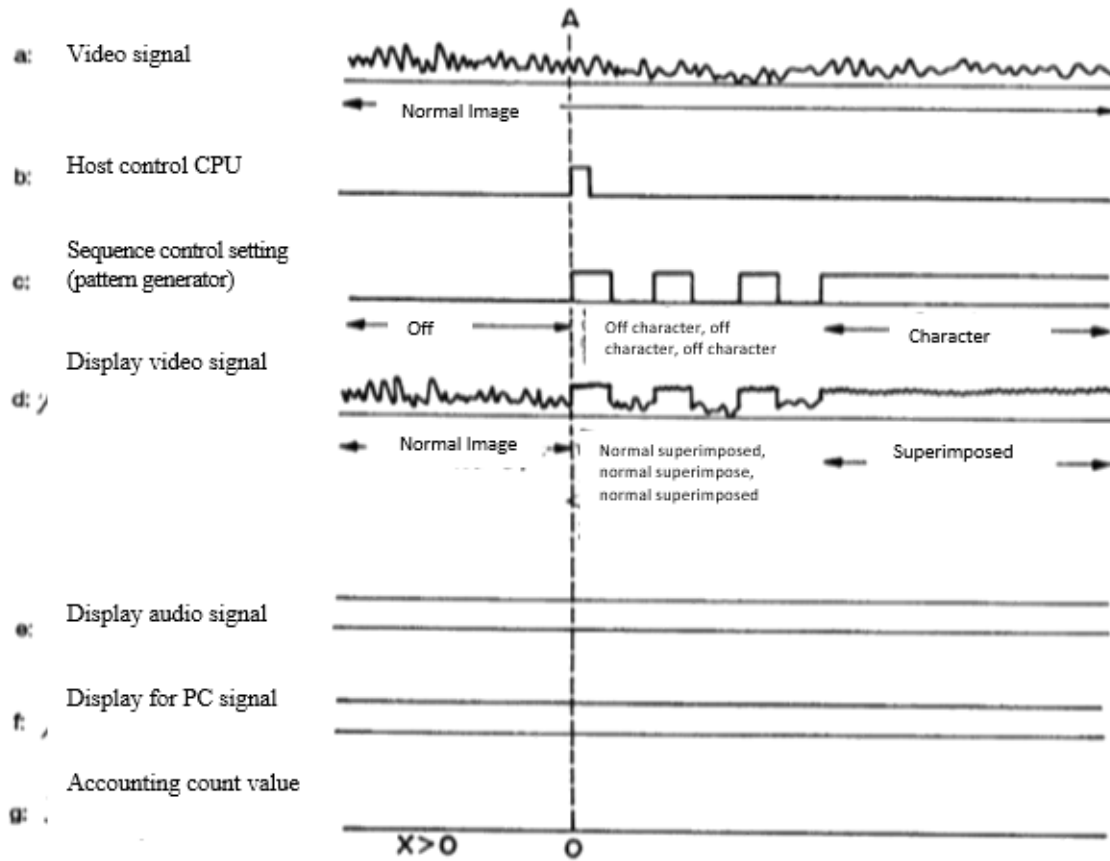
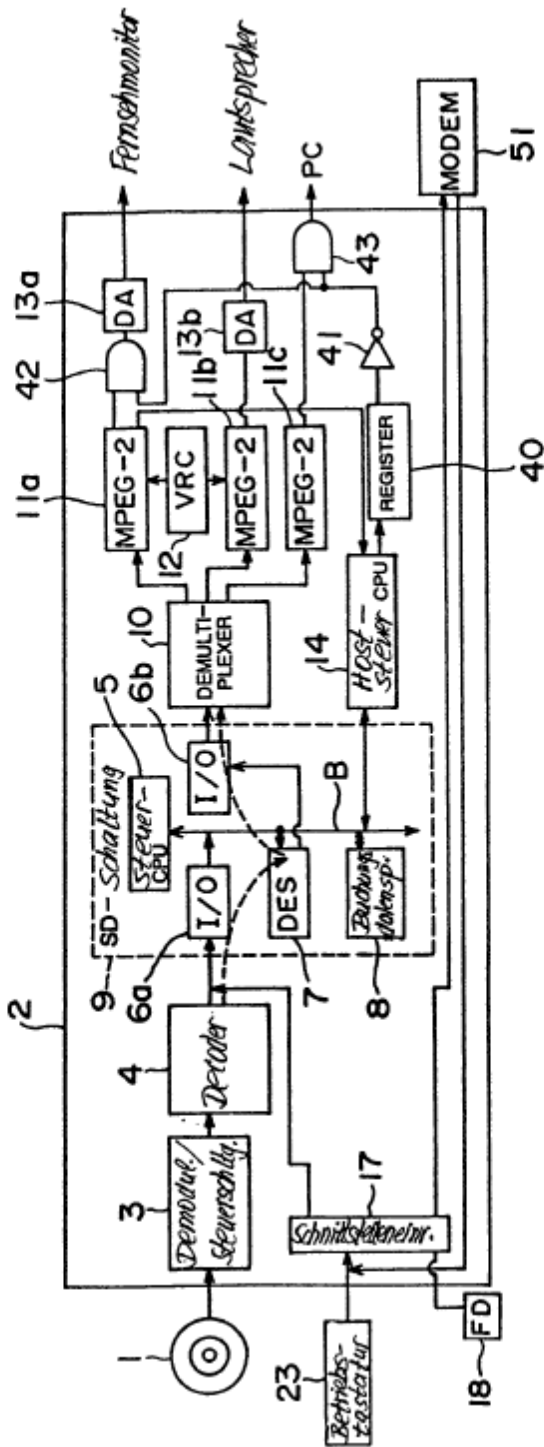


Fig. 8



TV monitor
Loudspeaker
PC

51 MODEM

3 Demodulation/control circuit

4 Decoder

5 Control CPU

8 Accounting memory

9 SD circuit

10 Demultiplexer

14 Host control CPU

17 Interface unit

23 Operating keyboard

40 Register

FIG. 9

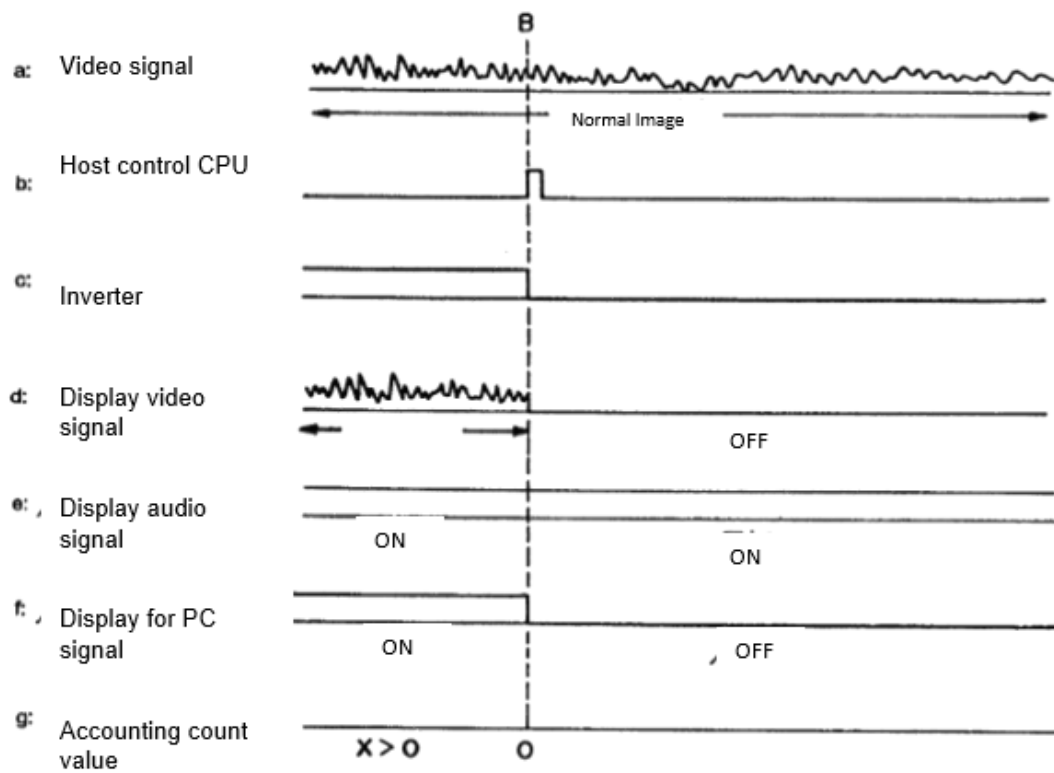
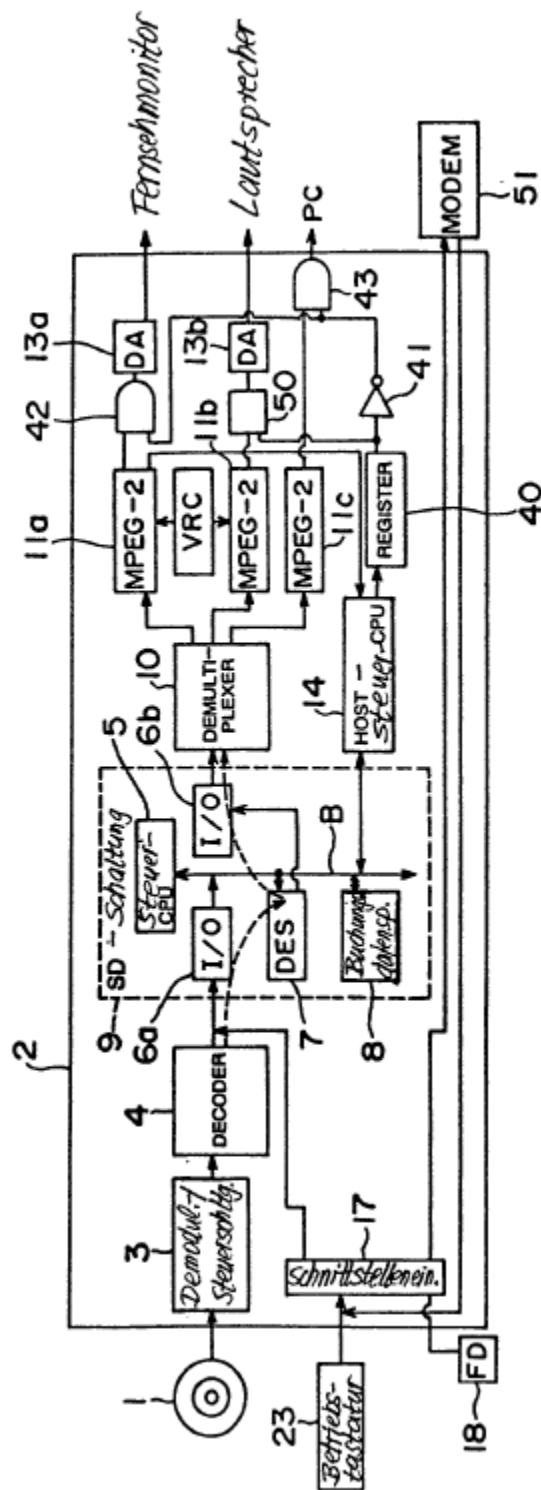


FIG. 10



TV monitor
Loudspeaker
PC

51 MODEM

3 Demodulation/control
circuit

4 Decoder

5 Control CPU

8 Accounting memory

9 SD circuit

10 Demultiplexer

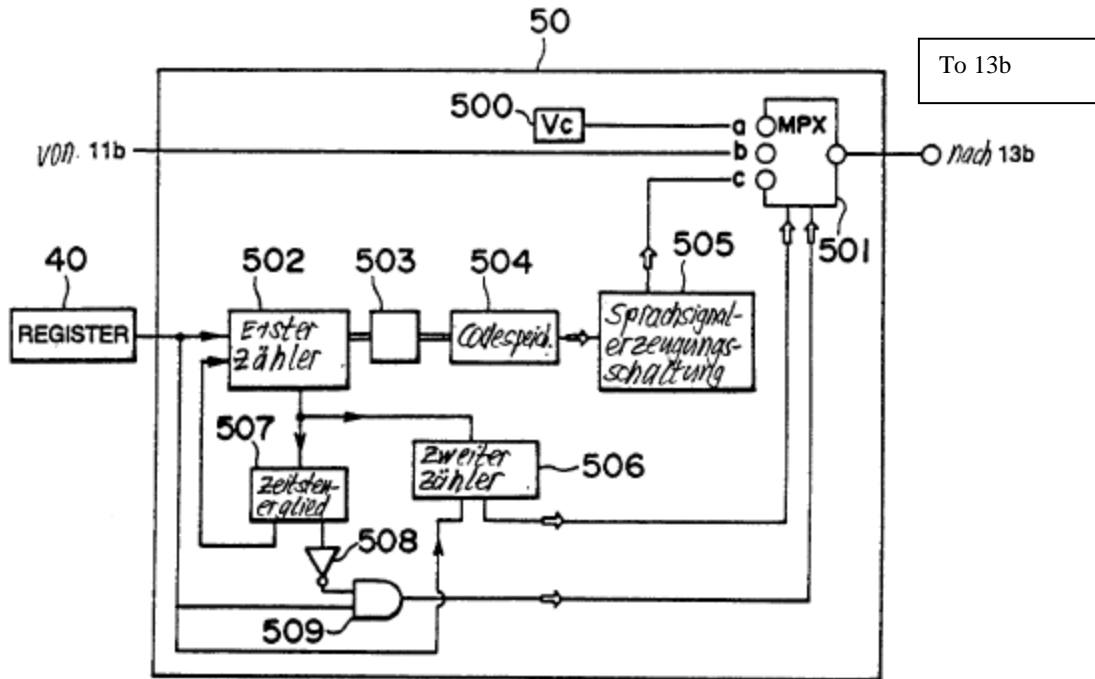
14 Host control CPU

17 Interface unit

23 Operating keyboard

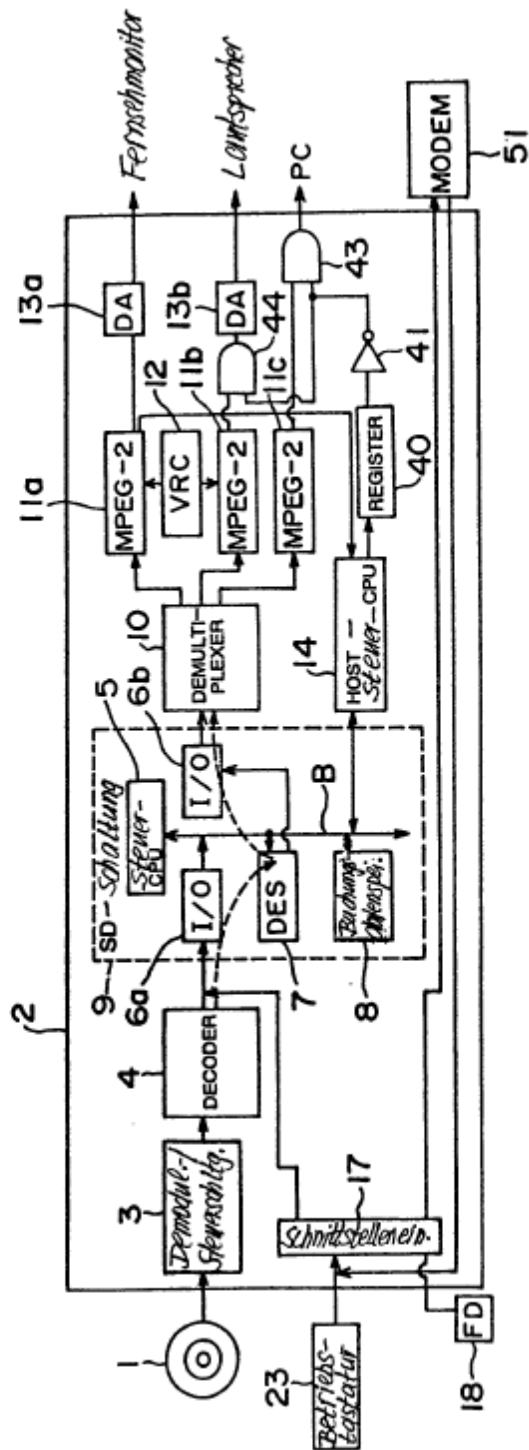
40 Register

FIG. 11



- 40 Register
- 502 First counter
- 504 Code memory
- 505 Speech signal generation circuit
- 506 second counter

FIG. 12



TV monitor
Loudspeaker
PC

51 MODEM

3 Demodulation/control circuit

5 Control CPU

8 Accounting memory

9 SD Circuit

10 Demultiplexer

14 Host control CPU

17 Interface unit

23 Operating keyboard

40 Register

FIG. 13

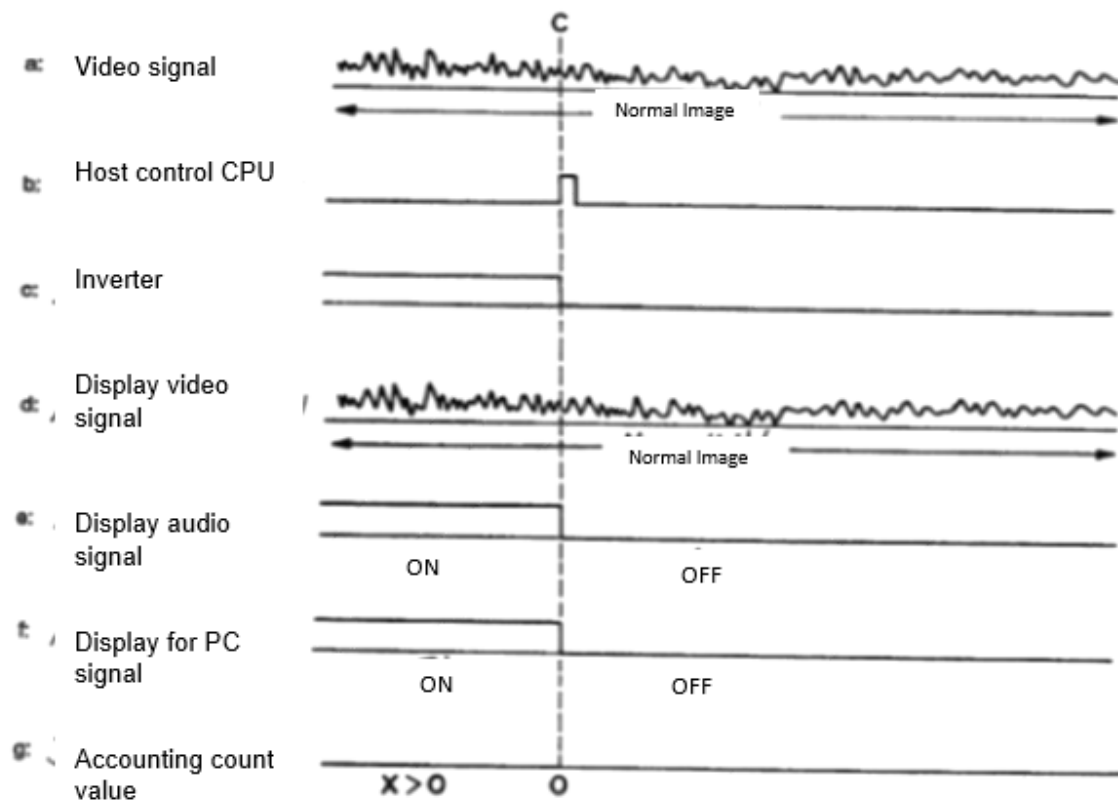
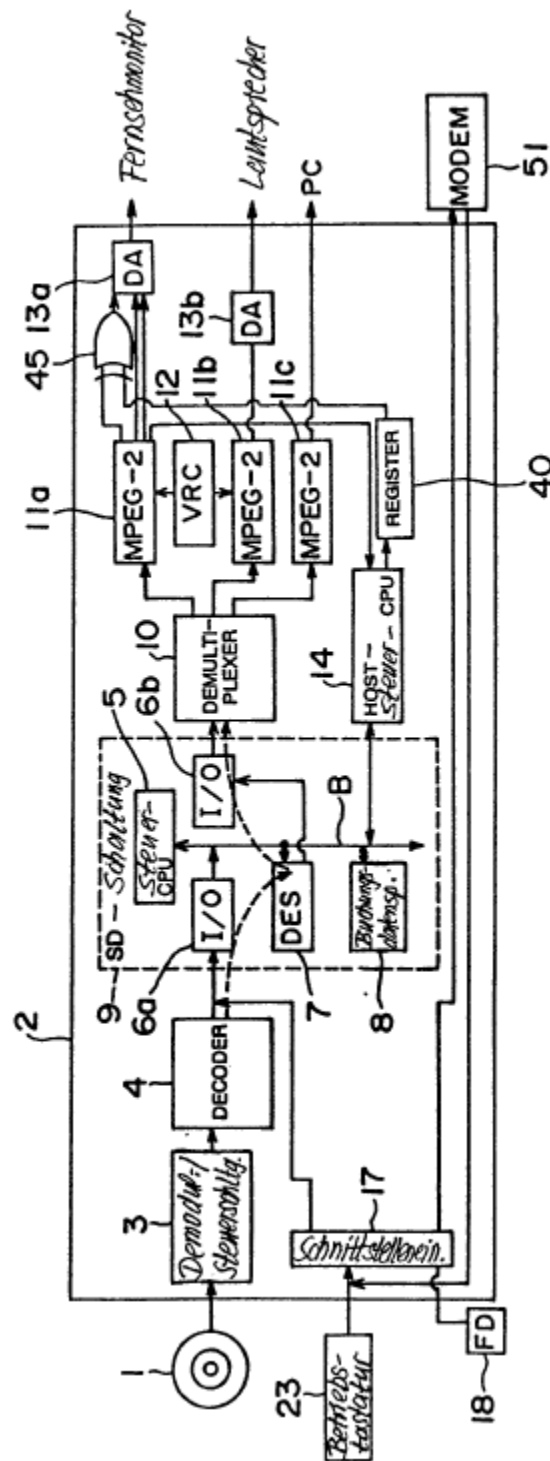


FIG. 14



TV monitor
Loudspeaker
PC

51 MODEM

3 Demodulation/control circuit
4 Decoder
5 Control CPU
8 Accounting memory
9 SD circuit
10 Demultiplexer
14 Host control CPU
17 Interface unit
23 Operating keyboard
40 Register

FIG. 15

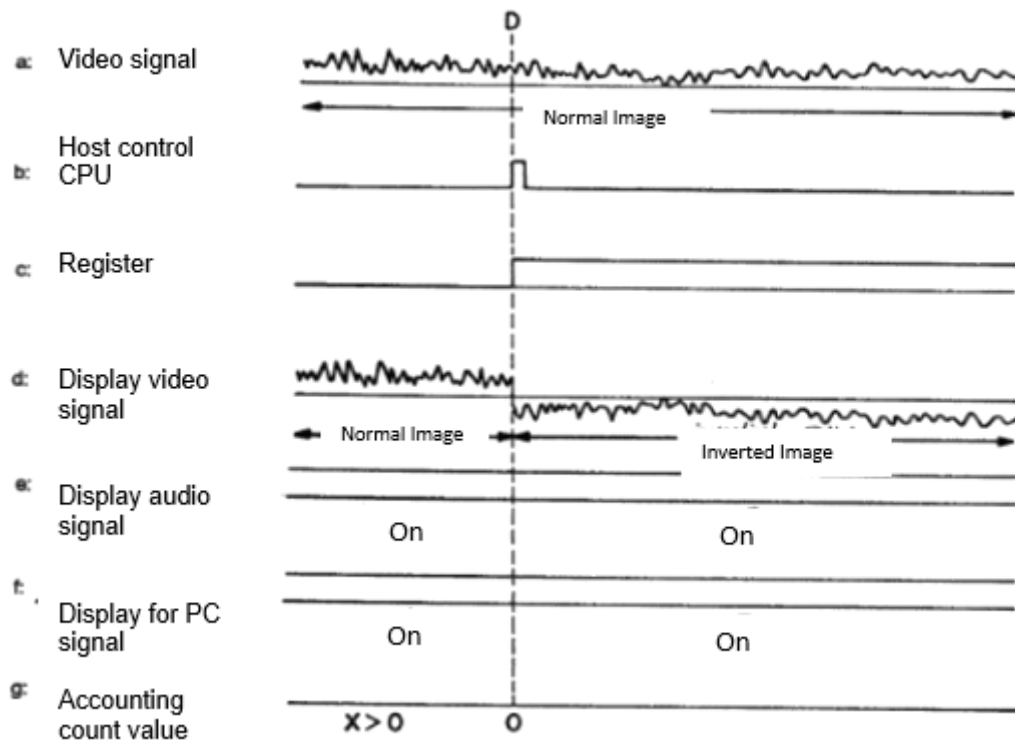
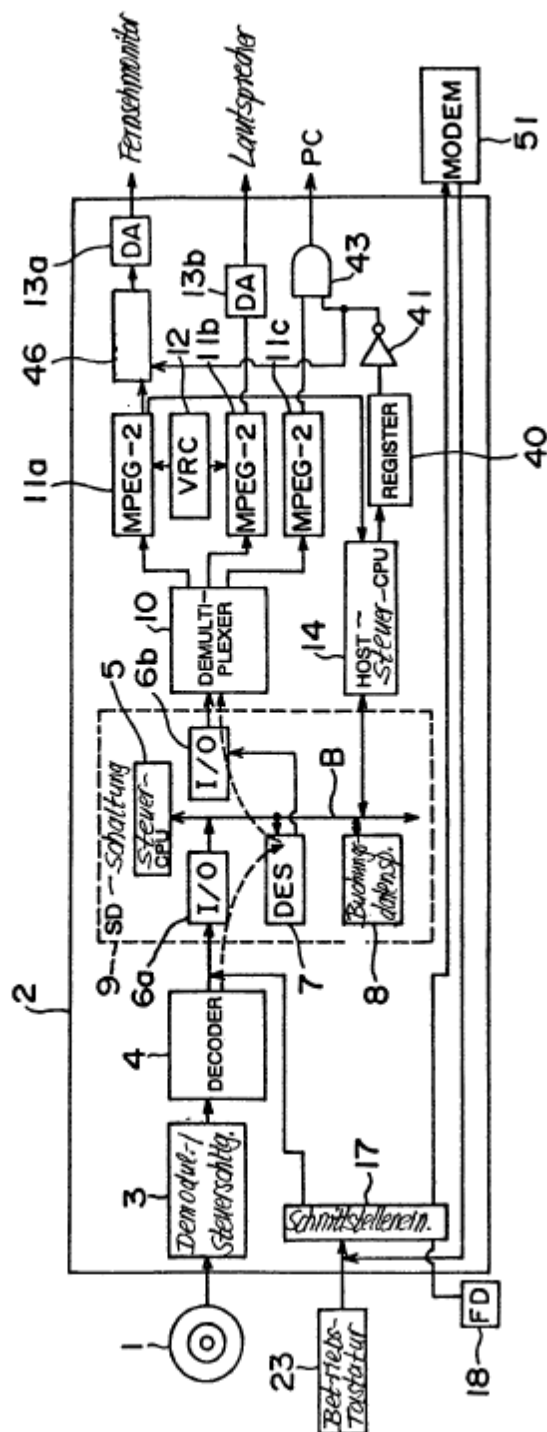
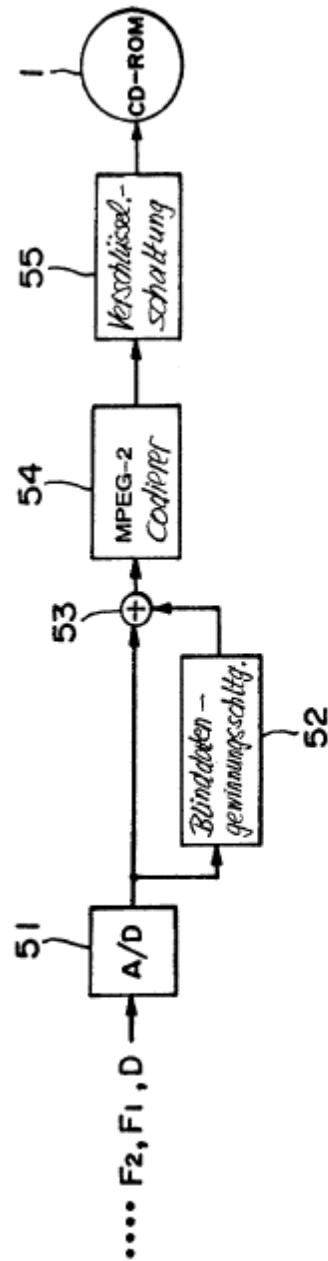


FIG. 16



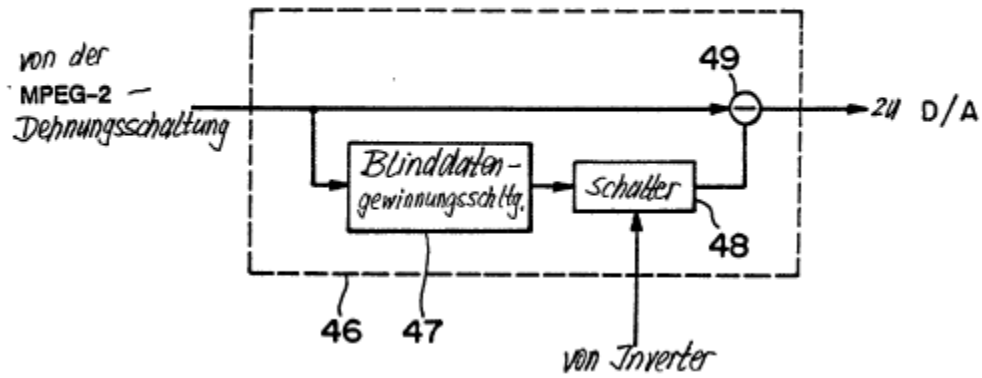
- TV monitor
- Loudspeaker
- PC
- 51 MODEM
- 3 Demodulation/control circuit
- 4 Decoder
- 5 Control CPU
- 8 Accounting memory
- 9 SD circuit
- 10 Demultiplexer
- 14 Host control CPU
- 17 Interface unit
- 23 Operating keyboard
- 40 Register

FIG. 17



- 1 CD Rom
- 52 Blind data recovery circuit
- 54 MPEG-2 encoder
- 55 Encryption circuit

FIG. 18



From the MPEG 2 expansion circuit
 47 Blind data extraction circuit
 48 Switch
 From inverter
 To D/A

FIG. 19

