



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/188,396	09/19/2017	9768339	111848-0002-101	1083

1473 7590 08/30/2017  
Haley Guiliano LLP  
75 Broad Street  
Suite 1000  
NEW YORK, NY 10004

## ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

### **Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)** (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

IQE, plc, St. Mellons, UNITED KINGDOM;  
Robert Yanka, Kernersville, NC;  
Seokjae Chung, Oak Ridge, NC;  
Kalyan Nunna, High Point, NC;  
Rodney Pelzel, Emmaus, PA;  
Howard Williams, St. Mellons, UNITED KINGDOM;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit [SelectUSA.gov](http://SelectUSA.gov).

IR103 (Rev. 10/09)

Solar Junction 1004  
Solar Junction v. IQE, plc  
DER2018-00019



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Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/188,396	06/21/2016	Robert Yanka	111848-0002-101

**CONFIRMATION NO. 1083**

**POWER OF ATTORNEY NOTICE**



OC000000093627652\*

28120  
ROPES & GRAY LLP  
IPRM Docketing - Floor 43  
PRUDENTIAL TOWER  
800 BOYLSTON STREET  
BOSTON, MA 02199-3600

Date Mailed: 08/25/2017

**NOTICE REGARDING CHANGE OF POWER OF ATTORNEY**

This is in response to the Power of Attorney filed 08/21/2017.

- The Power of Attorney to you in this application has been revoked by the applicant. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/sleutchit/



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/188,396	06/21/2016	Robert Yanka	111848-0002-101

**CONFIRMATION NO. 1083**

**POA ACCEPTANCE LETTER**



OC000000093627761\*

1473  
Haley Guiliano LLP  
75 Broad Street  
Suite 1000  
NEW YORK, NY 10004

Date Mailed: 08/25/2017

**NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY**

This is in response to the Power of Attorney filed 08/21/2017.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/sleutchit/

# PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**  
**Commissioner for Patents**  
**P.O. Box 1450**  
**Alexandria, Virginia 22313-1450**  
**or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

28120 7590 05/22/2017  
**ROPES & GRAY LLP**  
**IPRM Docketing - Floor 43**  
**PRUDENTIAL TOWER**  
**800 BOYLSTON STREET**  
**BOSTON, MA 02199-3600**

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

## Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/188,396	06/21/2016	Robert Yanka	111848-0002-101	1083

TITLE OF INVENTION: OPTOELECTRONIC DETECTORS HAVING A DILUTE NITRIDE LAYER ON A SUBSTRATE WITH A LATTICE PARAMETER NEARLY MATCHING GAAS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	08/22/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS
YUSHIN, NIKOLAY K	2893	257-186000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Haley Guiliano LLP

2 \_\_\_\_\_

3 \_\_\_\_\_

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

IQE, plc

St. Mellons, Cardiff, United Kingdom

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies \_\_\_\_\_

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 06-1075 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Jiaping Liu, Reg. 71506/

Date August 21, 2017

Typed or printed name Jiaping (Charlene) Liu

Registration No. 71,506

Electronic Patent Application Fee Transmittal				
<b>Application Number:</b>		15188396		
<b>Filing Date:</b>		21-Jun-2016		
<b>Title of Invention:</b>		OPTOELECTRONIC DETECTORS HAVING A DILUTE NITRIDE LAYER ON A SUBSTRATE WITH A LATTICE PARAMETER NEARLY MATCHING GAAS		
<b>First Named Inventor/Applicant Name:</b>		Robert Yanka		
<b>Filer:</b>		Jiaping Liu/Pamela Harrison		
<b>Attorney Docket Number:</b>		111848-0002-101		
Filed as Large Entity				
<b>Filing Fees for Utility under 35 USC 111(a)</b>				
<b>Description</b>	<b>Fee Code</b>	<b>Quantity</b>	<b>Amount</b>	<b>Sub-Total in USD(\$)</b>
<b>Basic Filing:</b>				
<b>Pages:</b>				
<b>Claims:</b>				
<b>Miscellaneous-Filing:</b>				
<b>Petition:</b>				
<b>Patent-Appeals-and-Interference:</b>				
<b>Post-Allowance-and-Post-Issuance:</b>				
UTILITY APPL ISSUE FEE	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				960

## Electronic Acknowledgement Receipt

<b>EFS ID:</b>	30137277
<b>Application Number:</b>	15188396
<b>International Application Number:</b>	
<b>Confirmation Number:</b>	1083
<b>Title of Invention:</b>	OPTOELECTRONIC DETECTORS HAVING A DILUTE NITRIDE LAYER ON A SUBSTRATE WITH A LATTICE PARAMETER NEARLY MATCHING GAAS
<b>First Named Inventor/Applicant Name:</b>	Robert Yanka
<b>Customer Number:</b>	28120
<b>Filer:</b>	Jiaping Liu/Pamela Harrison
<b>Filer Authorized By:</b>	Jiaping Liu
<b>Attorney Docket Number:</b>	111848-0002-101
<b>Receipt Date:</b>	21-AUG-2017
<b>Filing Date:</b>	21-JUN-2016
<b>Time Stamp:</b>	17:43:16
<b>Application Type:</b>	Utility under 35 USC 111(a)

### Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$960
RAM confirmation Number	082217INTEFSW00004616061075
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Post Allowance Communication - Incoming	111848-0002-101_Comments.pdf	64871	no	2
			05ead8e662a7e4ed009d10702c08c5aea01b60b8		
Warnings:					
Information:					
2	Power of Attorney	111848-0002-101_POA.pdf	203940	no	2
			3d9d76d2e39c6d1521ff1f73f094ad90476eeefb		
Warnings:					
Information:					
3	Issue Fee Payment (PTO-85B)	111848-0002-101_Issue_Fee_Payment.pdf	245621	no	1
			598e8e717c685b1a71aff2d0a80b282dea736041		
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	30967	no	2
			0bf460de6a1b998ba96c5a8f0b8103149fb837a6		
Warnings:					
Information:					
Total Files Size (in bytes):			545399		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

**New Applications Under 35 U.S.C. 111**

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

**National Stage of an International Application under 35 U.S.C. 371**

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Docket No.: 111848-0002-101  
(PATENT)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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In re Patent Application of:  
Yanka et al.

Application No.: 15/188,396

Confirmation No.: 1083

Filed: June 21, 2016

Art Unit: 2893

For: OPTOELECTRONIC DETECTORS HAVING A  
DILUTE NITRIDE LAYER ON A SUBSTRATE  
WITH A LATTICE PARAMETER NEARLY  
MATCHING GAAS

---

Examiner: Nikolay K. Yushin

**COMMENTS ON STATEMENT OF REASONS  
FOR ALLOWANCE UNDER 37 C.F.R. § 1.104(e)**

MS Issue Fee  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

This application was allowed on May 22, 2017. The Notice of Allowability included a Statement of Reasons for Allowance.

While applicant appreciates the allowance of this application, applicant notes that in the Statement of Reasons for Allowance, the Examiner paraphrases certain limitations of each of applicant's independent claims as the reasons for allowance of that claim and all of its dependent claims. Applicant states for the record that:

First, to the extent that the Examiner's reasons for allowance refer to certain claim limitations, applicant does not necessarily agree that the paraphrased or referenced claim limitations are the only reasons that the allowed claims are patentable; and

Second, to the extent, if any, that the actual limitations of any of applicant's claims differ from the claims as paraphrased by the Examiner, each claim is limited only by its actual language (including the language of any claim from which it depends), and limitations are not to be read into any claim.

Dated: August 21, 2017

Respectfully submitted,

/Jiaping Liu, Reg. 71506/  
Jiaping (Charlene) Liu  
Reg. No. 71,506  
HALEY GUILIANO LLP  
75 Broad Street  
Suite 1000  
New York, New York 10004  
(646) 973-2500  
Attorney for Applicant

Doc Code: PA..  
Document Description: Power of Attorney

PTO/AIA/82B (07-13)  
Approved for use through 11/30/2014. OMB 0651-0051  
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

## TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA/82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	15/188,396		
Filing Date	June 21, 2016		
First Named Inventor	Robert Yanka		
Title	OPTOELECTRONIC DETECTORS HAVING A DILUTE NITRIDE LAYER ON A SUBSTRATE WITH A LATTICE PARAMETER NEARLY MATCHING GAAS		
Art Unit	2893		
Examiner Name	Nikolay K. Yushin		
Attorney Docket Number	111848-0002-101		
<b>SIGNATURE of Applicant or Patent Practitioner</b>			
	/Jiaping Liu, Reg. 71506/	Date (Optional)	August 21, 2017
Name	Jiaping (Charlene) Liu	Registration Number	71,506
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			
<b>NOTE:</b> This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.			
<input checked="" type="checkbox"/>	*Total of <u>1</u> forms are submitted.		

**POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO**

I hereby revoke all previous powers of attorney given in the above-identified patent application.

☒ I hereby appoint Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s) and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent):

01473

OR

☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent):

Name Registration	Number	Name Registration	Number

Please recognize or change the correspondence address for the above-identified patent to:

☒ The address associated with the above-mentioned Customer Number:

OR

☐ The address associated with Customer Number:

OR

☐ Firm or  
Individual Name

Address

City

State

Zip

Country

Telephone

Email

**SIGNATURE of Applicant for Patent**

Signature



Date

20 AUGUST 2017

Name

Rodney Pelzel

Telephone

+1-610-972-1477

Title and Company

Vice President, Group Technology, IQE, plc

NOTE: This form must be signed by the applicant or applicant's representative in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below\*.

☒\*Total of 1 forms are submitted.

1 0



# UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

## NOTICE OF ALLOWANCE AND FEE(S) DUE

28120 7590 05/22/2017  
ROPES & GRAY LLP  
IPRM Docketing - Floor 43  
PRUDENTIAL TOWER  
800 BOYLSTON STREET  
BOSTON, MA 02199-3600

EXAMINER

YUSHIN, NIKOLAY K

ART UNIT

PAPER NUMBER

2893

DATE MAILED: 05/22/2017

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/188,396	06/21/2016	Robert Yanka	111848-0002-101	1083

TITLE OF INVENTION: OPTOELECTRONIC DETECTORS HAVING A DILUTE NITRIDE LAYER ON A SUBSTRATE WITH A LATTICE  
PARAMETER NEARLY MATCHING GAAS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	08/22/2017

**THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.**

**THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.**

### HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

**IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.**

## PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
or Fax (571)-273-2885**

**INSTRUCTIONS:** This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

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Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/188,396	06/21/2016	Robert Yanka	111848-0002-101	1083

TITLE OF INVENTION: OPTOELECTRONIC DETECTORS HAVING A DILUTE NITRIDE LAYER ON A SUBSTRATE WITH A LATTICE PARAMETER NEARLY MATCHING GAAS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	08/22/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS
YUSHIN, NIKOLAY K	2893	257-186000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 \_\_\_\_\_
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 \_\_\_\_\_
- 3 \_\_\_\_\_

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies \_\_\_\_\_

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number \_\_\_\_\_ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

**NOTE:** Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

**NOTE:** If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

**NOTE:** Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

**NOTE:** This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature \_\_\_\_\_

Date \_\_\_\_\_

Typed or printed name \_\_\_\_\_

Registration No. \_\_\_\_\_



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/188,396	06/21/2016	Robert Yanka	111848-0002-101	1083

28120 7590 05/22/2017  
ROPES & GRAY LLP  
IPRM Docketing - Floor 43  
PRUDENTIAL TOWER  
800 BOYLSTON STREET  
BOSTON, MA 02199-3600

EXAMINER
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YUSHIN, NIKOLAY K

ART UNIT	PAPER NUMBER
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2893

DATE MAILED: 05/22/2017

## Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

## OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

### Privacy Act Statement

**The Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

<b>Notice of Allowability</b>	<b>Application No.</b> 15/188,396	<b>Applicant(s)</b> YANKA ET AL.	
	<b>Examiner</b> NIKOLAY YUSHIN	<b>Art Unit</b> 2893	<b>AIA (First Inventor to File) Status</b> Yes

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--**

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to Amendments filed on 03/02/2017.  
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on \_\_\_\_\_.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on \_\_\_\_\_; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 1,4-16 and 19-32. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see [http://www.uspto.gov/patents/init\\_events/pph/index.jsp](http://www.uspto.gov/patents/init_events/pph/index.jsp) or send an inquiry to [PPHfeedback@uspto.gov](mailto:PPHfeedback@uspto.gov).
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

**Certified copies:**

- a) ☐ All    b) ☐ Some    \*c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.  
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.  
**Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

- |  |  |
|--|--|
| 1. <input type="checkbox"/> Notice of References Cited (PTO-892)   | 5. <input type="checkbox"/> Examiner's Amendment/Comment                             |
| 2. <input checked="" type="checkbox"/> Information Disclosure Statements (PTO/SB/08),<br>Paper No./Mail Date <u>04/12/2017</u> | 6. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance |
| 3. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit<br>of Biological Material                     | 7. <input type="checkbox"/> Other _____.   |
| 4. <input type="checkbox"/> Interview Summary (PTO-413),<br>Paper No./Mail Date _____.   |  |

/NIKOLAY YUSHIN/  
Primary Examiner, Art Unit 2893

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

## **DETAILED ACTION**

### **Status of Claims**

Applicant's cancellation of claims 1, 3, 17, and 18 in the reply filed on 03/20/2017 is acknowledged.

Applicant's amendment of claims 1, 4, 16, and 19 in the reply filed on 03/20/2017 is acknowledged.

Applicant's addition of new claims 31 and 32 in the reply filed on 03/20/2017 is acknowledged.

Claims 1, 4-16, and 19-32 are under consideration in this Office Action.

### ***Allowable Subject Matter***

Claims 1, 4-16, and 19-32 are allowed.

The following is an examiner's statement of reasons for allowance:

In re Claim 1, Sakai et al., US 4,682,196 discloses all limitations of claim 1 except for that "a dilute nitride comprising  $\text{In}_x\text{Ga}_{1-x}\text{N}_y\text{As}_{1-y-z}\text{Sb}_z$ , ( $0 < x < 1$ ;  $0 < y < 0.1$ ;  $0 < z \leq 0.1667$ ), an In/Sb ratio of at least approximately 6." Therefore, the claimed device differs from prior art devices on this point and there is no evidence it would have been obvious to make this change.

In re Claim 16, Sakai discloses all limitations of claim 16 except for that "a dilute nitride comprising  $\text{In}_x\text{Ga}_{1-x}\text{N}_y\text{As}_{1-y-z}\text{Sb}_z$ , ( $0 < x < 1$ ;  $0 < y < 0.1$ ;  $0 < z \leq 0.1667$ ), an In/Sb ratio of at least approximately 6." Therefore, the claimed method differs from prior art methods on this point and there is no evidence it would have been obvious to make this change.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NIKOLAY YUSHIN whose telephone number is (571)270-7885. The examiner can normally be reached on 8 AM - 5 PM PST.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would


Application/Control Number: 15/188,396

Page 4

Art Unit: 2893

like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/NIKOLAY YUSHIN/  
Primary Examiner, Art Unit 2893

<b>Search Notes</b>  	<b>Application/Control No.</b>  15188396	<b>Applicant(s)/Patent Under Reexamination</b>  YANKA ET AL.
	<b>Examiner</b>  NIKOLAY YUSHIN	<b>Art Unit</b>  2893

CPC- SEARCHED		
Symbol	Date	Examiner
H01L31/1075; H01L31/03046; H01L31/03044	11/29/2016	NY
Y02E10/544	05/04/2017	NY


CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
Keyword, inventor names, assignee searching - see search history	11/29/2016	NY
Updated keyword searching - see search history	05/04/2017	NY

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
Y02E10	544	05/04/2017	NY
H01L31	1075; 03046; 03044	05/04/2017	NY

	/NIKOLAY YUSHIN/ Primary Examiner.Art Unit 2893
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<b>Issue Classification</b> 	<b>Application/Control No.</b> 15188396	<b>Applicant(s)/Patent Under Reexamination</b> YANKA ET AL.	
	<b>Examiner</b> NIKOLAY YUSHIN	<b>Art Unit</b> 2893	

CPC						
Symbol					Type	Version
H01L		31	/	1075	F	2013-01-01
H01L		31	/	03044	I	2013-01-01
H01L		31	/	03046	I	2013-01-01
H01L		31	/	03048	I	2013-01-01
H01L		31	/	105	I	2013-01-01
H01L		31	/	1848	I	2013-01-01
H01L		31	/	1852	I	2013-01-01
Y02E		10	/	544	A	2013-01-01
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CPC Combination Sets				
Symbol	Type	Set	Ranking	Version

NONE  (Assistant Examiner) _____ (Date)		<b>Total Claims Allowed:</b> 28	
/NIKOLAY YUSHIN/ Primary Examiner.Art Unit 2893  (Primary Examiner) _____ (Date)		05/04/2017 (Date)	O.G. Print Claim(s) 1
			O.G. Print Figure 4



<b>Issue Classification</b> 	<b>Application/Control No.</b> 15188396	<b>Applicant(s)/Patent Under Reexamination</b> YANKA ET AL.
	<b>Examiner</b> NIKOLAY YUSHIN	<b>Art Unit</b> 2893

<input type="checkbox"/> <b>Claims renumbered in the same order as presented by applicant</b> <input type="checkbox"/> <b>CPA</b> <input type="checkbox"/> <b>T.D.</b> <input type="checkbox"/> <b>R.1.47</b>															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1		17												
	2		18												
	3	16	19												
2	4	17	20												
3	5	18	21												
4	6	19	22												
5	7	20	23												
6	8	21	24												
7	9	22	25												
8	10	26	26												
12	11	27	27												
13	12	28	28												
14	13	23	29												
9	14	24	30												
10	15	11	31												
15	16	25	32												

NONE  (Assistant Examiner) _____ (Date) _____		<b>Total Claims Allowed:</b> 28	
/NIKOLAY YUSHIN/ Primary Examiner.Art Unit 2893  (Primary Examiner) _____ (Date) _____		O.G. Print Claim(s) 1	O.G. Print Figure 4



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## BIB DATA SHEET

CONFIRMATION NO. 1083

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
15/188,396	06/21/2016	257	2893	111848-0002-101

**APPLICANTS**  
 IQE, plc, St. Mellons, UNITED KINGDOM;

**INVENTORS**  
 Robert Yanka, Kernersville, NC;  
 Seokjae Chung, Oak Ridge, NC;  
 Kalyan Nunna, High Point, NC;  
 Rodney Pelzel, Emmaus, PA;  
 Howard Williams, St. Mellons, UNITED KINGDOM;

**\*\* CONTINUING DATA \*\*\*\*\***  
 This appln claims benefit of 62/183,060 06/22/2015

**\*\* FOREIGN APPLICATIONS \*\*\*\*\***

**\*\* IF REQUIRED, FOREIGN FILING LICENSE GRANTED \*\***  
 06/30/2016

Foreign Priority claimed 35 USC 119(a-d) conditions met Verified and Acknowledged	<input type="checkbox"/> Yes <input checked="" type="checkbox"/> No <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No /NIKOLAY K YUSHIN/ Examiner's Signature	<input type="checkbox"/> Met after Allowance Initials	STATE OR COUNTRY NC	SHEETS DRAWINGS 9	TOTAL CLAIMS 30	INDEPENDENT CLAIMS 2
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**ADDRESS**  
 ROPES & GRAY LLP  
 IPRM Docketing - Floor 43  
 PRUDENTIAL TOWER  
 800 BOYLSTON STREET  
 BOSTON, MA 02199-3600  
 UNITED STATES

**TITLE**  
 OPTOELECTRONIC DETECTORS HAVING A DILUTE NITRIDE LAYER ON A SUBSTRATE WITH A LATTICE PARAMETER NEARLY MATCHING GAAS

FILING FEE RECEIVED 2540	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	<input type="checkbox"/> All Fees
		<input type="checkbox"/> 1.16 Fees (Filing)
		<input type="checkbox"/> 1.17 Fees (Processing Ext. of time)
		<input type="checkbox"/> 1.18 Fees (Issue)
		<input type="checkbox"/> Other _____
		<input type="checkbox"/> Credit

PTO/SB/08a (07-09)

Approved for use through 07/31/2016. OMB 0651-0031

U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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Substitute for form 1449/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  <i>(Use as many sheets as necessary)</i>				<b>Complete if Known</b>	
				Application Number	15/188,396
				Filing Date	June 21, 2016
				First Named Inventor	Robert Yanka
				Art Unit	2893
				Examiner Name	Nikolay K. Yushin
				Attorney Docket Number	111848-0002-101
Sheet	1	of	2		

[illegible][illegible]

Examiner Signature	/NIKOLAY K YUSHIN/	Date Considered	05/04/2017
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\*EXAMINER. Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. <sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> See Kinds Codes of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04. <sup>3</sup> Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>5</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. <sup>6</sup> Applicant is to place a check mark here if English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.K.Y/

PTO/SB/08b (07-09)

Approved for use through 07/31/2016. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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Substitute for form 1449/PTO				<b>Complete if Known</b>	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (Use as many sheets as necessary)				Application Number	15/188,396
				Filing Date	June 21, 2016
				First Named Inventor	Robert Yanka
				Art Unit	2893
				Examiner Name	Nikolay K. Yushin
Sheet	2	of	2	Attorney Docket Number	111848-0002-101

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		Bank et al., "Low-Threshold Continuous-Wave 1.5-μm GaInNAsSb Lasers Grown on GaAs," <i>IEEE Journal of Quantum Electronics</i> , Vol. 40 No. 6 (2004) 9 pages.	
		Jackrel, "InGaAs and GaInNAs(Sb) 1064 NM Photodetectors and Solar Cells on GaAs Substrates," (2005) 264 pages.	
		Jackrel et al., "Dilute nitride GaInNAs and GaInNAsSb solar cells by molecular beam epitaxy," <i>Journal of Applied Physics</i> 101, 114916 (2007) 9 pages.	
		Kim et al., "Characteristics of bulk InGaAsN and InGaAsSbN materials grown by metal organic vapor phase epitaxy (MOVPE) for solar cell application," <i>Proc. of SPIE</i> , Vol. 8256, (2012) 8 pages.	
		Ng et al., "Molecular beam epitaxy growth of bulk GaNAsSb on Ge/graded-SiGe/Si substrate," <i>Journal of Crystal Growth</i> 311, pages 1754-1757 (2009).	
		Sin et al., "Carrier Dynamics in MOVPE-Grown Bulk Dilute Nitride Materials for Multi-Junction Solar Cells," <i>Proc. of SPIE</i> , Vol. 7933, (2011) 11 pages.	
		Tan et al., "Molecular beam epitaxy grown GaNAsSb 1 eV photovoltaic cell," <i>Journal of Crystal Growth</i> 335 (2011) pages 66-69.	
		Yuen, "Growth and Characterization of Dilute Nitride Antimonides for Long-Wavelength Optoelectronics," a Dissertation submitted to the department of materials science and engineering and the committee on graduate studies of Stanford University in partial fulfillment of the requirements for the degree of doctor of philosophy, March 2006, 203 pages.	

Examiner Signature	/NIKOLAY K YUSHIN/	Date Considered	05/17/2017
-----------------------	--------------------	--------------------	------------

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.K.Y/

## EAST Search History

## EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L12	81	((In\$6Ga\$6N\$6As\$6Sb\$6))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2017/05/04 10:31
L13	21	L12 AND (Y02E10/544).CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2017/05/04 10:31
S1	4	((Robert) near2 (Yanka)).INV.	US-PGPUB; USPAT	AND	ON	2016/11/28 11:50
S2	0	((Seokjae) near2 (Chung)).INV.	US-PGPUB; USPAT	AND	ON	2016/11/28 11:51
S3	0	((Kalyan) near2 (Nunna)).INV.	US-PGPUB; USPAT	AND	ON	2016/11/28 11:51
S4	0	((Rodney) near2 (Pelzel)).INV.	US-PGPUB; USPAT	AND	ON	2016/11/28 11:51
S5	941	((Howard) near2 (Williams)).INV.	US-PGPUB; USPAT	AND	ON	2016/11/28 11:51
S6	4	((Robert) near2 (Yanka)).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/11/28 11:52
S7	0	((Seokjae) near2 (Chung)).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/11/28 11:52
S8	0	((Kalyan) near2 (Nunna)).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/11/28 11:52
S9	0	((Rodney) near2 (Pelzel)).INV.	US-PGPUB; USPAT; USOCR; FPRS;	AND	ON	2016/11/28 11:52

			EPO; JPO; DERWENT; IBM_TDB			
S10	3991	((Howard) near2 (Williams)).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/11/28 11:53
S11	4	(S5 OR S6 OR S7 OR S8 OR S9 Or S10) AND (IQE).AS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/11/28 11:54
S12	44	(IQE).AS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/11/28 11:54
S13	30	("III-V" In\$Ga\$N\$As\$Sb)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/11/28 12:56
S14	1	(13/197588).APP.	USPAT; USOCR	AND	ON	2016/11/28 13:05
S15	0	(14/599290).APP.	USPAT; USOCR	AND	ON	2016/11/28 13:09
S16	54	("GaAs" In\$Ga\$N\$As\$Sb)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/11/28 13:16
S17	4471	("GaAs" substrate bandgap carrier doped absorb\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/11/28 13:19
S18	19	("GaAs" substrate bandgap carrier doped absorb\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/28 13:20
S19	2	("GaAs" substrate bandgap carrier concentration doped absorb\$4)	US-PGPUB; USPAT; USOCR; FPRS;	SAME	ON	2016/11/28 13:24

			EPO; JPO; DERWENT; IBM_TDB			
S20	6	("GaAs" AND (substrate bandgap carrier concentration doped absorb\$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/28 13:25
S21	1	(13/727845).APP.	USPAT; USOCR	AND	ON	2016/11/28 13:32
S22	28	(( "GaAs" substrate) AND (bandgap (carrier ADJ concentration) absorb\$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/28 13:34
S23	46	(( "GaAs" substrate) AND (band\$1gap (carrier ADJ concentration) absorb\$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/28 13:34
S24	46	(( "GaAs" substrate) AND ((bandgap OR band\$1gap) (carrier ADJ concentration) absorb\$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/28 13:34
S25	32	("3353114"   "3514715"   "3604987"   "3659159"   "3852591"   "4015280"   "4017332").PN. OR ("4127862").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2016/11/28 14:57
S26	22	("GaAs" In\$6Ga\$6N\$6As\$6Sb)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/28 15:37
S27	5	(absorb\$6 In\$6Ga\$6N\$6As\$6Sb)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/28 15:39
S28	35	("20020195677"   "20040061056"   "20040108461"   "20040108564"   "20060118722"   "20060162768"   "20060164633"   "20070075224"   "20080111152"   "20090121307"   "4679063"   "4847489"   "5093580"   "5113076"   "5216244"   "5229611"   "5453727"   "5457331"   "5581084"   "5729018"   "5731621"   "5977557"   "6043550"   "6049116"   "6157020"   "6455908"   "6504222"   "6803557"	US-PGPUB; USPAT; USOCR	AND	ON	2016/11/28 15:41

		"7067856"   "7671341").PN. OR ("8093559").URPN.				
S29	1	(absorb\$6 "InGaNaSb")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/28 15:47
S30	50	(In\$6Ga\$6N\$6As\$6Sb layer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/28 15:48
S31	52	(In\$6Ga\$6N\$6As\$6Sb\$4 layer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/29 05:26
S32	76	(In\$6Ga\$6N\$6As\$6Sb\$6)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/29 05:26
S33	76	(In\$6Ga\$6N\$6As\$6Sb\$6 OR "InGaNaSb")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/29 05:27
S34	6	( "InGaNaSb")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/29 05:27
S35	18	S32 AND (H01L31/1075; H01L31/03046; H01L31/03044).CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/29 05:28
S36	0	(In\$6Ga\$6N\$6As\$6Sb\$6 AND multiplication)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/29 05:31
S37	0	(S33 AND multiplication)	US-PGPUB; USPAT; USOCR;	SAME	ON	2016/11/29 05:31

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S38	328570	( multiplication)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/29 05:31
S39	1	("7045833").PN.	US-PGPUB; USPAT	OR	OFF	2016/11/29 05:47
S40	1	(09/969133).APP.	US-PGPUB; USOCR	AND	ON	2016/11/29 05:47
S41	1	(( "8957376" ) or ( "201009665" ) ).PN.	US-PGPUB; USPAT	OR	OFF	2016/11/29 11:28
S42	1	(( "8957376" ) or ( "201009665" ) ).PN.	US-PGPUB; USPAT	OR	OFF	2016/11/29 11:28
S43	0	("201009665").PN.	US-PGPUB; USPAT	OR	OFF	2016/11/29 11:28
S44	1	("8957376").PN.	US-PGPUB; USPAT	AND	ON	2016/11/29 11:30
S45	0	("(MacDougal).INV.").PN.	US-PGPUB; USPAT	OR	OFF	2016/11/29 11:32
S46	0	("(MacDougal).IN.").PN.	US-PGPUB; USPAT	OR	OFF	2016/11/29 11:32
S47	0	("(MacDougal).IN.").PN.	US-PGPUB; USPAT	OR	OFF	2016/11/29 11:33
S48	1	("2010009665").PN.	US-PGPUB; USPAT	OR	OFF	2016/11/29 11:33
S49	1	(12/254634).APP.	USPAT; USOCR	AND	ON	2016/11/29 11:38
S50	1	("4032951").PN. OR ("7915639").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2016/11/29 11:52
S51	1	(15/188396).APP.	US-PGPUB; USPAT	OR	OFF	2017/02/05 17:37
S52	953	((Howard) near2 (Williams)).INV.	US-PGPUB; USPAT	AND	ON	2017/05/04 08:55
S53	6	((Robert) near2 (Yanka)).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/04 08:55
S54	2	((Seokjae) near2 (Chung)).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/04 08:55
S55	2	((Kalyan) near2 (Nunna)).INV.	US-PGPUB; USPAT; USOCR;	AND	ON	2017/05/04 08:55

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S56	2	((Rodney) near2 (Pelzel)).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/04 08:55
S57	4029	((Howard) near2 (Williams)).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/04 08:55
S58	4	(S52 OR S53 OR S54 OR S55 OR S56 Or S57) AND (IQE).AS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/04 08:55
S59	1	(15/188396).APP.	US-PGPUB; USPAT	OR	OFF	2017/05/04 08:56
S60	81	(In\$6Ga\$6N\$6As\$6Sb\$6)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2017/05/04 08:56
S61	22	S60 AND (H01L31/1075; H01L31/03046; H01L31/03044).CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2017/05/04 08:56

## EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	(semiconductor substrate lattice GaAs doped "III-V" absor\$4 layer dilute nitride "In/Sb" ratio bandgap carrier concentration).CLM.	US-PGPUB; USPAT	AND	ON	2017/05/04 10:01
L2	1	(semiconductor substrate lattice GaAs doped "III-V" absor\$4 layer dilute nitride "In/Sb" ratio bandgap carrier concentration)	US-PGPUB; USPAT	AND	ON	2017/05/04 10:01
L3	1	( substrate lattice GaAs doped "III-V" absor\$4 layer nitride "In/Sb" ratio bandgap carrier concentration)	US-PGPUB; USPAT	AND	ON	2017/05/04 10:01
L4	1	( substrate GaAs doped "III-V" absor\$4 layer nitride "In/Sb" ratio bandgap carrier concentration)	US-PGPUB; USPAT	AND	ON	2017/05/04 10:01
L5	1	( substrate "GaAs" doped "III-V" absor\$4 layer nitride "In/Sb" ratio bandgap concentration)	US-PGPUB;	AND	ON	2017/05/04 10:02

			USPAT			
L6	1	( substrate "GaAs" doped "III-V" absor\$4 nitride "In/Sb" ratio bandgap concentration)	US-PGPUB; USPAT	AND	ON	2017/05/04 10:02
L7	918	( substrate "GaAs" doped "III-V" absor\$4 nitride ratio bandgap concentration)	US-PGPUB; USPAT	AND	ON	2017/05/04 10:02
L8	0	( substrate "GaAs" doped "III-V" absor\$4 nitride ratio bandgap concentration)	US-PGPUB; USPAT	SAME	ON	2017/05/04 10:02
L9	0	( substrate "GaAs" doped "III-V" (absor\$4 SAME nitride) ratio bandgap concentration)	US-PGPUB; USPAT	SAME	ON	2017/05/04 10:03
L10	130	( substrate "GaAs" doped "III-V" (absor\$4 SAME nitride) ratio bandgap concentration)	US-PGPUB; USPAT	AND	ON	2017/05/04 10:03
L11	11	L10 AND (H01L31/1075; H01L31/03046; H01L31/03044).CPC.	US-PGPUB; USPAT	AND	ON	2017/05/04 10:03
L14	21	L10 AND (Y02E10/544).CPC.	US-PGPUB; USPAT	AND	ON	2017/05/04 10:32

5/ 4/ 2017 10:37:06 AM

C:\Users\nyushin\Documents\EAST\Workspaces\15188396.wsp

Substitute for form 1449/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  <i>(Use as many sheets as necessary)</i>				<b>Complete if Known</b>	
				Application Number	15/188,396
				Filing Date	June 21, 2016
				First Named Inventor	Robert Yanka
				Art Unit	2893
				Examiner Name	Nikolay K. Yushin
				Attorney Docket Number	111848-0002-101
Sheet	1	of	2		

[illegible][illegible]

Examiner Signature		Date Considered	
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. <sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> See Kinds Codes of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04. <sup>3</sup> Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>5</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. <sup>6</sup> Applicant is to place a check mark here if English language Translation is attached.

Substitute for form 1449/PTO				<b>Complete if Known</b>	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  <i>(Use as many sheets as necessary)</i>				Application Number	15/188,396
				Filing Date	June 21, 2016
				First Named Inventor	Robert Yanka
				Art Unit	2893
				Examiner Name	Nikolay K. Yushin
Sheet	2	of	2	Attorney Docket Number	111848-0002-101

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		Bank et al., "Low-Threshold Continuous-Wave 1.5-μm GaInNAsSb Lasers Grown on GaAs," <i>IEEE Journal of Quantum Electronics</i> , Vol. 40 No. 6 (2004) 9 pages.	
		Jackrel, "InGaAs and GaInNAs(Sb) 1064 NM Photodetectors and Solar Cells on GaAs Substrates," (2005) 264 pages.	
		Jackrel et al., "Dilute nitride GaInNAs and GaInNAsSb solar cells by molecular beam epitaxy," <i>Journal of Applied Physics</i> 101, 114916 (2007) 9 pages.	
		Kim et al., "Characteristics of bulk InGaAsN and InGaAsSbN materials grown by metal organic vapor phase epitaxy (MOVPE) for solar cell application," <i>Proc. of SPIE</i> , Vol. 8256, (2012) 8 pages.	
		Ng et al., "Molecular beam epitaxy growth of bulk GaNAsSb on Ge/graded-SiGe/Si substrate," <i>Journal of Crystal Growth</i> 311, pages 1754-1757 (2009).	
		Sin et al., "Carrier Dynamics in MOVPE-Grown Bulk Dilute Nitride Materials for Multi-Junction Solar Cells," <i>Proc. of SPIE</i> , Vol. 7933, (2011) 11 pages.	
		Tan et al., "Molecular beam epitaxy grown GaNAsSb 1 eV photovoltaic cell," <i>Journal of Crystal Growth</i> 335 (2011) pages 66-69.	
		Yuen, "Growth and Characterization of Dilute Nitride Antimonides for Long-Wavelength Optoelectronics," a Dissertation submitted to the department of materials science and engineering and the committee on graduate studies of Stanford University in partial fulfillment of the requirements for the degree of doctor of philosophy, March 2006, 203 pages.	

Examiner Signature		Date Considered	
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached.

Electronic Patent Application Fee Transmittal				
<b>Application Number:</b>		15188396		
<b>Filing Date:</b>		21-Jun-2016		
<b>Title of Invention:</b>		OPTOELECTRONIC DETECTORS HAVING A DILUTE NITRIDE LAYER ON A SUBSTRATE WITH A LATTICE PARAMETER NEARLY MATCHING GAAS		
<b>First Named Inventor/Applicant Name:</b>		Robert Yanka		
<b>Filer:</b>		James Francis Mack/Pamela Harrison		
<b>Attorney Docket Number:</b>		111848-0002-101		
Filed as Large Entity				
<b>Filing Fees for Utility under 35 USC 111(a)</b>				
<b>Description</b>	<b>Fee Code</b>	<b>Quantity</b>	<b>Amount</b>	<b>Sub-Total in USD(\$)</b>
<b>Basic Filing:</b>				
<b>Pages:</b>				
<b>Claims:</b>				
<b>Miscellaneous-Filing:</b>				
<b>Petition:</b>				
<b>Patent-Appeals-and-Interference:</b>				
<b>Post-Allowance-and-Post-Issuance:</b>				
<b>Extension-of-Time:</b>				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
<b>Miscellaneous:</b>				
Submission- Information Disclosure Stmt	1806	1	180	180
<b>Total in USD (\$)</b>				<b>180</b>

Electronic Acknowledgement Receipt	
<b>EFS ID:</b>	28888591
<b>Application Number:</b>	15188396
<b>International Application Number:</b>	
<b>Confirmation Number:</b>	1083
<b>Title of Invention:</b>	OPTOELECTRONIC DETECTORS HAVING A DILUTE NITRIDE LAYER ON A SUBSTRATE WITH A LATTICE PARAMETER NEARLY MATCHING GAAS
<b>First Named Inventor/Applicant Name:</b>	Robert Yanka
<b>Customer Number:</b>	28120
<b>Filer:</b>	James Francis Mack/Pamela Harrison
<b>Filer Authorized By:</b>	James Francis Mack
<b>Attorney Docket Number:</b>	111848-0002-101
<b>Receipt Date:</b>	12-APR-2017
<b>Filing Date:</b>	21-JUN-2016
<b>Time Stamp:</b>	15:20:17
<b>Application Type:</b>	Utility under 35 USC 111(a)

### Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$180
RAM confirmation Number	041317INTEFSW00001742181945
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1	Non Patent Literature	Bank_Low-Threshold.pdf	557481	no	9
			3257d8a0e330962130839bd71010ff59da0ae21d		
Warnings:					
Information:					
2	Non Patent Literature	Jackrel_A_Dissertation.pdf	8505075	no	264
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Information:					
3	Non Patent Literature	Jackrel_Dilute.pdf	2743515	no	9
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5	Non Patent Literature	Ng_Molecular.pdf	712267	no	4
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6	Non Patent Literature	Sin_Carrier.pdf	368268	no	11
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7	Non Patent Literature	Tan_Molecular.pdf	144858	no	4
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Information:					
8	Transmittal Letter	111848-0002-101_Supp_IDS.pdf	83670	no	2
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Warnings:					
Information:					
9	Information Disclosure Statement (IDS) Form (SB08)	111848-0002-101_SB-08.pdf	124968	no	2
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Information:					
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Information:					
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Information:					
Total Files Size (in bytes):			21551117		

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**New Applications Under 35 U.S.C. 111**

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

**National Stage of an International Application under 35 U.S.C. 371**

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Docket No.: 111848-0002-101  
(PATENT)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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In re Patent Application of:  
Yanka et al.

Application No.: 15/188,396

Confirmation No.: 1083

Filed: June 21, 2016

Art Unit: 2893

For: OPTOELECTRONIC DETECTORS HAVING A  
DILUTE NITRIDE LAYER ON A SUBSTRATE  
WITH A LATTICE PARAMETER NEARLY  
MATCHING GAAS

---

Examiner: Nikolay K. Yushin

**AMENDMENT IN RESPONSE TO NON-FINAL OFFICE ACTION**  
**UNDER 37 C.F.R. § 1.111**

Mail Stop AMENDMENT  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

In response to the Office Action dated December 2, 2016, please amend the above-identified U.S. patent application as follows:

**Amendments to the Claims** are reflected in the listing of claims which begins on page 2 of this paper.

**Remarks/Arguments** begin on page 6 of this paper.

## **REMARKS**

### **Summary of Examiner Interview**

Applicant thanks Examiner Yushin for the courtesies extended during a telephonic interview on February 6, 2017. During the interview, Examiner Yushin and the undersigned discussed claims 1, 2, and 3, proposed amendments, and the Sakai and Tan references. Examiner Yushin agreed that amendments substantially the same as those contained herein would overcome the references of record. Applicant thanks the Examiner for his time and has prepared this Reply to be responsive to the discussion during the interview.

### **Summary of Applicants' Reply**

Claims 1, 4, 16, and 19 are amended herein. Claims 31 and 32 are added. Claims 2-3 and 17-18 are canceled. No new matter is added by the amendments, which are supported by the originally-filed specification at least at paragraph 6, 28, 38, 57 and Figure 8. Applicant respectfully traverses the rejections and requests the withdrawal of the objections.

### **Response to Prior Art Rejections**

Without conceding the patentability of the claims, but solely to advance prosecution, Applicant has amended independent claim 1 based on the discussion with the Examiner during the Examiner interview dated February 6, 2017. Amended claim 1 recites “a dilute nitride comprising  $\text{In}_x\text{Ga}_{1-x}\text{N}_y\text{As}_{1-y-z}\text{Sb}_z$  ( $0 \leq x \leq 1$ ;  $0 < y \leq 0.1$ ;  $0 < z \leq 0.1667$ )” and “an In/Sb ratio of at least approximately 6.” The cited references, alone or in combination, fail to describe at least these features.

Sakai relates to a semiconductor device with an i-layer between n- and p-doped layers. Sakai at 3:54-4:63. While Sakai describes an i-layer of  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ , Sakai at 3:68-4:2, Sakai does not show or suggest a dilute nitride containing N and Sb, let alone one with an In/Sb ratio of at least approximately 6. Thus, Sakai does not show or suggest “a dilute nitride comprising  $\text{In}_x\text{Ga}_{1-x}\text{N}_y\text{As}_{1-y-z}\text{Sb}_z$  ( $0 \leq x \leq 1$ ;  $0 < y \leq 0.1$ ;  $0 < z \leq 0.1667$ )” and “an In/Sb ratio of at least approximately 6,” as required by independent claim 1.

Tan fails to remedy the deficiencies of Sakai. Tan relates to GaInNAsSb p-i-n photodetectors on GaAs substrates. Tan at Abstract. However, Tan describes that mass spectrometry analysis of the GaInNAsSb layers shows mole fractions of 10% In and 4.4% Sb in one device (A) and mole fractions of ~9.5% In and 4.89 % Sb in another device (B). This results in In/Sb ratios of 2.27 for Tan's device A and ~1.94 for Tan's device B. Accordingly, Tan, alone or in combination with Sakai, does not show or suggest "a dilute nitride comprising  $\text{In}_x\text{Ga}_{1-x}\text{N}_y\text{As}_{1-y-z}\text{Sb}_z$  ( $0 \leq x \leq 1$ ;  $0 < y \leq 0.1$ ;  $0 < z \leq 0.1667$ )" and "an In/Sb ratio of at least approximately 6," as required by independent claim 1.

Campbell, Baribeau, and Dargis fail to remedy the deficiencies of Sakai and Tan. Campbell, Baribeau, and Dargis are alleged to relate to other dependent claims and are not relevant to amended claim 1. Accordingly, Campbell, Baribeau, and Dargis, alone or in combination with Sakai and Tan, do not show or suggest "a dilute nitride comprising  $\text{In}_x\text{Ga}_{1-x}\text{N}_y\text{As}_{1-y-z}\text{Sb}_z$  ( $0 \leq x \leq 1$ ;  $0 < y \leq 0.1$ ;  $0 < z \leq 0.1667$ )" and "an In/Sb ratio of at least approximately 6," as required by independent claim 1.

Accordingly, amended claim 1 is patentable over the cited references. Amended claim 16 recites similar features as amended claim 1 and is patentable over the cited references for at least the same reasons. Claims 4-15 and 19-32 depend, directly or indirectly, from claims 1 or 16 and are allowable for at least the same reasons. Applicants therefore request that the rejections of the pending claims be withdrawn.

Conclusion

In view of the above amendment, applicant believes the pending application is in condition for allowance. The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 18-1945, from which the undersigned is authorized to draw.

Dated: March 2, 2017

Respectfully submitted,

By /James F. Mack/

James F. Mack

Registration No.: 74,196

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Agent For Applicant

### **AMENDMENTS TO THE CLAIMS**

The following listing of claims, if entered, will replace all prior versions, and listings, of claims in the application.

#### **Listing of Claims:**

1. (Currently Amended) A semiconductor, comprising:
  - a substrate with a lattice parameter matching or nearly matching GaAs;
  - a first doped III-V layer over the substrate;
  - an absorber layer over the first doped III-V layer, the absorber layer having:
    - a dilute nitride comprising  $\text{In}_x\text{Ga}_{1-x}\text{N}_y\text{As}_{1-y-z}\text{Sb}_z$  ( $0 \leq x \leq 1$ ;  $0 < y \leq 0.1$ ;  $0 < z \leq 0.1667$ ),
    - an In/Sb ratio of at least approximately 6,
    - a bandgap between approximately 0.7 eV and 0.95 eV, and
    - a carrier concentration less than approximately  $1 \times 10^{16} \text{ cm}^{-3}$  at room temperature;
  - and
  - a second doped III-V layer over the absorber layer.
- 2-3. (Canceled)
4. (Currently Amended) The semiconductor of claim [[2]] 1, wherein the dilute nitride comprises  $\text{In}_x\text{Ga}_{1-x}\text{N}_y\text{As}_{1-y-z}\text{Sb}_z$  ( $0 \leq x \leq 0.55$ ;  $[[0 \leq y \leq 0.1]]$   $0 < y \leq 0.1$ ;  $[[0 < z \leq 0.1]]$   $0 < z \leq 0.1$ ).
5. (Original) The semiconductor of claim 1, wherein the carrier concentration of the absorber layer is less than approximately  $5 \times 10^{15} \text{ cm}^{-3}$ .
6. (Original) The semiconductor of claim 1, wherein the carrier concentration of the absorber layer is less than approximately  $1 \times 10^{15} \text{ cm}^{-3}$ .

7. (Original) The semiconductor of claim 1, wherein a thickness of the absorber layer is between approximately 2 micrometers and approximately 10 micrometers.
8. (Original) The semiconductor of claim 1, wherein a thickness of the absorber layer is between approximately 3 micrometers and approximately 5 micrometers.
9. (Original) The semiconductor of claim 1, further comprising a multiplication layer between the absorber layer and one of the first and second doped III-V layers.
10. (Original) The semiconductor of claim 1, wherein the substrate comprises GaAs.
11. (Original) The semiconductor of claim 1, wherein the substrate comprises:
  - a silicon substrate; and
  - a lattice engineered layer over the silicon substrate, the surface of the lattice engineered layer opposite the silicon substrate having a lattice parameter that is matched or nearly matched to GaAs.
12. (Original) The semiconductor of claim 11, wherein the lattice engineered layer comprises a  $\text{Si}_x\text{Ge}_{1-x}$  layer, with  $x$  graded from 1 at a surface of the  $\text{Si}_x\text{Ge}_{1-x}$  layer nearest the silicon substrate to 0 at a surface of the  $\text{Si}_x\text{Ge}_{1-x}$  layer opposite the silicon substrate.
13. (Original) The semiconductor of claim 11, wherein the lattice engineered layer comprises a rare earth containing layer, the rare earth containing layer comprising one or more of Sc, Y, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, and/or Lu.
14. (Original) The semiconductor of claim 1, wherein the first doped III-V layer is n-type and the second doped III-V layer is p-type.
15. (Original) The semiconductor of claim 1, wherein the first doped III-V layer is p-type and the second doped III-V layer is n-type.

16. (Currently Amended) A method of forming a semiconductor, comprising:
- forming a first doped III-V layer over a substrate with a lattice parameter matching or nearly matching GaAs;
  - forming an absorber layer over the first doped III-V layer, the absorber layer having:
    - a dilute nitride comprising  $\text{In}_x\text{Ga}_{1-x}\text{N}_y\text{As}_{1-y-z}\text{Sb}_z$  ( $0 \leq x \leq 1$ ;  $0 < y \leq 0.1$ ;  $0 < z \leq 0.1667$ ),
    - an In/Sb ratio of at least approximately 6,
    - a bandgap between approximately 0.7 eV and 0.95 eV, and
    - a carrier concentration less than approximately  $1 \times 10^{16} \text{ cm}^{-3}$  at room temperature;
  - and
  - forming a second doped III-V layer over the absorber layer.

17-18. (Canceled)

19. (Currently Amended) The method of claim [[17]] 16, wherein the dilute nitride comprises  $\text{In}_x\text{Ga}_{1-x}\text{N}_y\text{As}_{1-y-z}\text{Sb}_z$  ( $0 \leq x \leq 0.55$ ;  $[[0 \leq y \leq 0.1]]$   $0 < y \leq 0.1$ ;  $[[0 < z \leq 0.1]]$   $0 < z \leq 0.1$ ).

20. (Original) The method of claim 16, wherein the carrier concentration of the absorber layer is less than approximately  $5 \times 10^{15} \text{ cm}^{-3}$ .

21. (Original) The method of claim 16, wherein the carrier concentration of the absorber layer is less than approximately  $1 \times 10^{15} \text{ cm}^{-3}$ .

22. (Original) The method of claim 16, wherein a thickness of the absorber layer is between approximately 2 micrometers and approximately 10 micrometers.

23. (Original) The method of claim 16, wherein a thickness of the absorber layer is between approximately 3 micrometers and approximately 5 micrometers.

24. (Original) The method of claim 16, further comprising forming a multiplication layer between the absorber layer and one of the first and second doped III-V layers.

25. (Original) The method of claim 16, wherein the substrate comprises GaAs.

26. (Original) The method of claim 16, wherein the substrate comprises:

a silicon substrate; and

a lattice engineered layer over the silicon substrate, the surface of the lattice engineered layer opposite the silicon substrate having a lattice parameter that is matched or nearly matched to GaAs.

27. (Original) The method of claim 26, wherein the lattice engineered layer comprises a  $\text{Si}_x\text{Ge}_{1-x}$  layer, with  $x$  graded from 1 at a surface of the  $\text{Si}_x\text{Ge}_{1-x}$  layer nearest the silicon substrate to 0 at a surface of the  $\text{Si}_x\text{Ge}_{1-x}$  layer opposite the silicon substrate.

28. (Original) The method of claim 26, wherein the lattice engineered layer comprises a rare earth containing layer, the rare earth containing layer comprising one or more of Sc, Y, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, and/or Lu.

29. (Original) The method of claim 16, wherein the first doped III-V layer is n-type and the second doped III-V layer is p-type.

30. (Original) The method of claim 16, wherein the first doped III-V layer is p-type and the second doped III-V layer is n-type.

31. (New) The semiconductor of claim 1, wherein the absorber layer is p-type.

32. (New) The method of claim 16, wherein the absorber layer is p-type.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/188,396	06/21/2016	Robert Yanka	111848-0002-101	1083
28120	7590	02/10/2017		
ROPE & GRAY LLP IPRM Docketing - Floor 43 PRUDENTIAL TOWER 800 BOYLSTON STREET BOSTON, MA 02199-3600			EXAMINER YUSHIN, NIKOLAY K	
			ART UNIT	PAPER NUMBER
			2893	
			NOTIFICATION DATE	DELIVERY MODE
			02/10/2017	ELECTRONIC

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USPatentMail@ropesgray.com  
USPatentMail2@ropesgray.com  
pair\_rg@firsttofile.com



## Summary of Record of Interview Requirements

### Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record

A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

### Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews

#### Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

#### 37 CFR §1.2 Business to be transacted in writing.

All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:

- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:

- 1) A brief description of the nature of any exhibit shown or any demonstration conducted,
- 2) an identification of the claims discussed,
- 3) an identification of the specific prior art discussed,
- 4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
- 5) a brief identification of the general thrust of the principal arguments presented to the examiner,  
(The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
- 6) a general indication of any other pertinent matters discussed, and
- 7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

### Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

Continuation of Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments:

Draft claim amendments have been discussed.

In re the amended claim 1, Examiner indicates that

1) According to Specification ([0028]) "The dilute nitride is a III-V material that includes low concentrations of nitrogen, concentrations that are LOW alloy-level concentrations and are higher than doping-level concentrations." Therefore, the limits for x, y, and z should be corrected.

2) As far as the thickness limitation is concerned, experimental evidences in the Specification as filed or an Affidavit signed by the inventors should be presented.

3) If the new claim 31 "The semiconductor of claim 1, wherein the absorber layer has an In/Sb ratio of at least approximately 6" would be incorporated in to claim 1, no evidence needed because Fig. 8 of the Specification demonstrates this limitation.

It seems that proposed amendments overcome the prior-art of record but a full search should perform..



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/188,396	06/21/2016	Robert Yanka	111848-0002-101

**CONFIRMATION NO. 1083**

## PUBLICATION NOTICE



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28120  
ROPES & GRAY LLP  
IPRM Docketing - Floor 43  
PRUDENTIAL TOWER  
800 BOYLSTON STREET  
BOSTON, MA 02199-3600

**Title:**OPTOELECTRONIC DETECTORS HAVING A DILUTE NITRIDE LAYER ON A SUBSTRATE WITH A LATTICE PARAMETER NEARLY MATCHING GAAS

**Publication No.**US-2016-0372624-A1

**Publication Date:**12/22/2016

## NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at [www.uspto.gov](http://www.uspto.gov). The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at [www.uspto.gov](http://www.uspto.gov) using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



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ROPE & GRAY LLP IPRM Docketing - Floor 43 PRUDENTIAL TOWER 800 BOYLSTON STREET BOSTON, MA 02199-3600			EXAMINER YUSHIN, NIKOLAY K	
			ART UNIT 2893	PAPER NUMBER
			NOTIFICATION DATE 12/02/2016	DELIVERY MODE ELECTRONIC

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<b>Office Action Summary</b>	<b>Application No.</b> 15/188,396	<b>Applicant(s)</b> YANKA ET AL.	
	<b>Examiner</b> NIKOLAY YUSHIN	<b>Art Unit</b> 2893	<b>AIA (First Inventor to File) Status</b> Yes

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 06/21/2016.  
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on \_\_\_\_; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims\***

- 5) ☒ Claim(s) 1-30 is/are pending in the application.  
5a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 6) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 7) ☒ Claim(s) 1-30 is/are rejected.
- 8) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 9) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

\* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see [http://www.uspto.gov/patents/init\\_events/pph/index.jsp](http://www.uspto.gov/patents/init_events/pph/index.jsp) or send an inquiry to [PPHfeedback@uspto.gov](mailto:PPHfeedback@uspto.gov).

**Application Papers**

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

**Certified copies:**

- a) ☐ All    b) ☐ Some\*\*    c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\*\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)  
Paper No(s)/Mail Date 06/21/2016; 10/07/2016.
- 3) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 4) ☐ Other: \_\_\_\_.

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 103***

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103 are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 1, 5-8, 10, 14-16, 20-23, 25, 29, and 30 are rejected under 35 U.S.C. 103 as being unpatentable over Sakai et al., US 4,682,196.

In re Claim 1, Sakai discloses a semiconductor, comprising: a substrate 10 (Fig. 4); a first doped III-V layer (11,12) over the substrate 10; an absorber layer 13 over the first doped III-V layer (11, 12), the absorber layer 13 (being  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  (column 3, line 68 –column 4, line 1))) having: inherently a bandgap of 0.75 eV, that is within the claimed range of between approximately 0.7 eV and 0.95 eV, therefore anticipates the range (MPEP2131.03.I), and a carrier concentration of  $10^{15} \text{ cm}^{-3}$  (column 4, line 1) that is within the claimed range of less than approximately  $1 \times 10^{16} \text{ cm}^{-3}$  at room temperature, therefore anticipates the range (MPEP2131.03.I); and a second doped III-V layer (14, 15) over the absorber layer 13 (Figs. 2 and 4; column 3, line 28 –column 4, line 64). It is inherent because according to Takeda et al., “Electron mobility and energy gap of  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  on InP substrate”, 1976, Journal of Applied Physics, Vol. 47, No 12, p.5405, Abstract , published Dec. 1976. Let’s note that Takeda’s reference is presented here only as an evidence of inherency (MPEP2131.01.I).

In an embodiment related to Fig. 4, Takeda does not disclose that a substrate 10 (Fig. 4) is with a lattice parameter matching or nearly matching GaAs. However, in an embodiment related to Fig. 4, Takeda teaches a substrate 1 (made of GaAs (column 3, lines 27 -51)) with a lattice parameter matching or nearly matching GaAs.

Due to high level of knowledge and skills of person capable to operate very sophisticated and expensive equipment in semiconductor technology, it would have been an obvious matter of design choice of one of ordinary skill in the semiconductor art to substitute the substrate 10 of Fig. 4 made of InP with substrate 1 of Fig. 2 made of GaAs, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its

suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416 (See MPEP2144.07).

In re Claim 5, Sakai discloses the semiconductor of claim 1, wherein the carrier concentration of the absorber layer 13 is  $10^{15} \text{ cm}^{-3}$  (column 4, line 1) that is within the claimed range of less than approximately  $5 \times 10^{15} \text{ cm}^{-3}$ , therefore anticipates the range (MPEP2131.03.I).

In re Claim 6, Sakai discloses the semiconductor of claim 1, wherein the carrier concentration of the absorber layer 13 is  $\approx 10^{15} \text{ cm}^{-3}$  (column 4, line 1) that is touching the claimed range of less than approximately  $1 \times 10^{15} \text{ cm}^{-3}$  (MPEP2131.03.II).

In re Claim 7, Sakai discloses all limitations of claim 7 except for that a thickness of the absorber layer 13 is between approximately 2 micrometers and approximately 10 micrometers. It is known in the art that the thickness is a result effective variable – because a mass depends on it. Due to high level of knowledge and skills of personal capable to operate very sophisticated and expensive equipment in semiconductor technology, it would have been an obvious matter of design choice of one of ordinary skill in the semiconductor art to use the specified thickness, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (MPEP2144.05.I).

In re Claim 8, Sakai discloses all limitations of claim 8 except for that a thickness of the absorber layer is between approximately 3 micrometers and approximately 5 micrometers. It is known in the art that the thickness is a result effective variable – because a mass depends on it. Due to high level of knowledge and skills of personal capable to operate very sophisticated and expensive equipment in semiconductor technology, it would have been an obvious matter of

design choice of one of ordinary skill in the semiconductor art to use the specified thickness, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (MPEP2144.05.I).

In re Claim 10, Sakai discloses the semiconductor of claim 1, wherein the substrate 10 (Fig. 4) being substitute with the substrate 1 of Fig. 2 comprises GaAs (column 3, lines 27 -51).

In re Claim 14, Sakai discloses the semiconductor of claim 1, wherein the first doped III-V layer (11, 12) is n-type and the second doped III-V layer (14, 15) is p-type (Fig. 4, column 3, line 28 –column 4, line 64).

In re Claim 15, Sakai discloses all limitations of claim 15 except for that the first doped III-V layer is p-type and the second doped III-V layer is n-type. Due to high level of knowledge and skills of personal capable to operate very sophisticated and expensive equipment in semiconductor technology, it would have been an obvious matter of design choice of one of ordinary skill in the semiconductor art to use a reverse order of doped layers, since it has been held that a mere reversal of the essential working parts of a device involves only routine skill in the art. *In re Gazda*, 219 F.2d 449, 104 USPQ 400 (CCPA 1955) (MPEP2144.04.VI.A).

In re Claim 16, Sakai discloses a method of forming a semiconductor, comprising: forming a first doped III-V layer (11, 12) over a substrate 10 (Fig. 4); forming an absorber layer 13 over the first doped III-V layer (11, 12), the absorber layer 13 (being  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  (column 3, line 68 –column 4, line 1))) having: inherently a bandgap of 0.75 eV, that is within the claimed range of between approximately 0.7 eV and 0.95 eV, therefore anticipates the range

(MPEP2131.03.I), and a carrier concentration of  $10^{15} \text{ cm}^{-3}$  (column 4, line 1) that is within the claimed range of less than approximately  $1 \times 10^{16} \text{ cm}^{-3}$  at room temperature, therefore anticipates the range (MPEP2131.03.I); and a second doped III-V layer (14, 15) over the absorber layer 13 (Figs. 2 and 4; column 3, line 28 –column 4, line 64). It is inherent because according to Takeda et al., “Electron mobility and energy gap of  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  on InP substrate”, 1976, Journal of Applied Physics, Vol. 47, No 12, p.5405, Abstract, published Dec. 1976. Let’s note that Takeda’s reference is presented here only as an evidence of inherency (MPEP2131.01.I).

In an embodiment related to Fig. 4, Takeda does not disclose that a substrate 10 (Fig. 4) is with a lattice parameter matching or nearly matching GaAs. However, in an embodiment related to Fig. 4, Takeda teaches a substrate 1 (made of GaAs (column 3, lines 27 -51)) with a lattice parameter matching or nearly matching GaAs.

Due to high level of knowledge and skills of person capable to operate very sophisticated and expensive equipment in semiconductor technology, it would have been an obvious matter of design choice of one of ordinary skill in the semiconductor art to substitute the substrate 10 of Fig. 4 made of InP with substrate 1 of Fig. 2 made of GaAs, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416 (See MPEP2144.07).

In re Claim 20, Sakai discloses the method of claim 16, wherein the carrier concentration of the absorber layer 13 is  $10^{15} \text{ cm}^{-3}$  (column 4, line 1) that is within the claimed range of less than approximately  $5 \times 10^{15} \text{ cm}^{-3}$ , therefore anticipates the range (MPEP2131.03.I).

In re Claim 21, Sakai discloses the method of claim 16, wherein the carrier concentration of the absorber layer 13 is  $\approx 10^{15} \text{ cm}^{-3}$  (column 4, line 1) that is touching the claimed range of less than approximately  $1 \times 10^{15} \text{ cm}^{-3}$  (MPEP2131.03.II).

In re Claim 22, Sakai discloses all limitations of claim 22 except for that a thickness of the absorber layer 13 is between approximately 2 micrometers and approximately 10 micrometers. It is known in the art that the thickness is a result effective variable – because a mass depends on it. Due to high level of knowledge and skills of personal capable to operate very sophisticated and expensive equipment in semiconductor technology, it would have been an obvious matter of design choice of one of ordinary skill in the semiconductor art to use the specified thickness, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233 (MPEP2144.05.I).

In re Claim 23, Sakai discloses all limitations of claim 23 except for that a thickness of the absorber layer is between approximately 3 micrometers and approximately 5 micrometers. It is known in the art that the thickness is a result effective variable – because a mass depends on it. Due to high level of knowledge and skills of personal capable to operate very sophisticated and expensive equipment in semiconductor technology, it would have been an obvious matter of design choice of one of ordinary skill in the semiconductor art to use the specified thickness, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233 (MPEP2144.05.I).

In re Claim 25, Sakai discloses the method of claim 16, wherein the substrate 10 (Fig. 4) being substitute with the substrate 1 of Fig. 2 comprises GaAs (column 3, lines 27 -51).

In re Claim 29, Sakai discloses the method of claim 16, wherein the first doped III-V layer (11, 12) is n-type and the second doped III-V layer (14, 15) is p-type (Fig. 4, column 3, line 28 –column 4, line 64).

In re Claim 30, Sakai discloses all limitations of claim 30 except for that the first doped III-V layer is p-type and the second doped III-V layer is n-type. Due to high level of knowledge and skills of personal capable to operate very sophisticated and expensive equipment in semiconductor technology, it would have been an obvious matter of design choice of one of ordinary skill in the semiconductor art to use a reverse order of doped layers, since it has been held that a mere reversal of the essential working parts of a device involves only routine skill in the art. *In re Gazda*, 219 F.2d 449, 104 USPQ 400 (CCPA 1955) (MPEP2144.04.VI.A).

Claims 2-4 and 17-19 are rejected under 35 U.S.C. 103 as being unpatentable over Sakai as applied to claim 1 and 16, respectively, above, and further in view of Tan et al., “GaInNAsSb/GaAs Photodiodes for Long-Wavelength Application”, IEEE Electron Devices Letters, Vol. 32, No. 7, pp 919-92, 1 July 2011 (listed in IDS filed on 06/21/2016).

In re Claim 2, Sakai discloses all limitations of claim 2 except for that the absorber layer 13 comprises a dilute nitride. Tan teaches a semiconductor wherein absorber layer 13 comprises a dilute nitride (page 919, left column).

It would have been obvious to one of ordinary skill in the art at the time of the invention to substitute Sakai’s absorber layer with Tan’s absorber layer made of dilute nitride, for long-

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wavelength detection in high-speed low-noise GaAs-based APDs as taught by Tan (page 921, right column).

In re Claim 3, Sakai taken with Tan discloses the semiconductor of claim 2, wherein the dilute nitride comprises  $\text{Ga}_{0.88}\text{In}_{0.12}\text{N}_{0.037}\text{As}_{0.962}$  (page 920) corresponding to  $\text{In}_x\text{Ga}_{1-x}\text{N}_y\text{As}_{1-y-z}\text{Sb}_z$  with  $x=0.12$ ;  $y=0.037$ ;  $z=0$  that are within the claimed range of  $(0 \leq x \leq 1; 0 \leq y \leq 1; 0 \leq z \leq 1)$  therefore anticipates the range (MPEP2131.03.I).

In re Claim 4, Sakai taken with Tan discloses the semiconductor of claim 2, wherein the dilute nitride comprises  $\text{Ga}_{0.88}\text{In}_{0.12}\text{N}_{0.037}\text{As}_{0.962}$  (page 920) corresponding to  $\text{In}_x\text{Ga}_{1-x}\text{N}_y\text{As}_{1-y-z}\text{Sb}_z$  with  $x=0.12$ ;  $y=0.037$ ;  $z=0$  that is within the claimed range of  $(0 \leq x \leq 0.55; 0 \leq y \leq 0.1; 0 \leq z \leq 0.1)$  therefore anticipates the range (MPEP2131.03.I).

In re Claim 17, Sakai discloses all limitations of claim 17 except for that for that the absorber layer 13 comprises a dilute nitride. Tan teaches a semiconductor wherein absorber layer 13 comprises a dilute nitride (page 919, left column).

It would have been obvious to one of ordinary skill in the art at the time of the invention to substitute Sakai's absorber layer with Tan's absorber layer made of dilute nitride, for long-wavelength detection in high-speed low-noise GaAs-based APDs as taught by Tan (page 921, right column).

In re Claim 18, Sakai taken with Tan discloses the method of claim 17, wherein the dilute nitride comprises  $\text{Ga}_{0.88}\text{In}_{0.12}\text{N}_{0.037}\text{As}_{0.962}$  (page 920) corresponding to  $\text{In}_x\text{Ga}_{1-x}\text{N}_y\text{As}_{1-y-z}\text{Sb}_z$  with  $x=0.12$ ;  $y=0.037$ ;  $z=0$  that are within the claimed range of  $(0 \leq x \leq 1; 0 \leq y \leq 1; 0 \leq z \leq 1)$  therefore anticipates the range (MPEP2131.03.I).

In re Claim 19, Sakai taken with Tan discloses the method of claim 17, wherein the dilute nitride comprises  $\text{Ga}_{0.88}\text{In}_{0.12}\text{N}_{0.037}\text{As}_{0.962}$  (page 920) corresponding to  $\text{In}_x\text{Ga}_{1-x}\text{N}_y\text{As}_{1-y-z}\text{Sb}_z$  with  $x=0.12$ ;  $y=0.037$ ;  $z=0$  that is within the claimed range of ( $0 \leq x \leq 0.55$ ;  $0 \leq y \leq 0.1$ ;  $0 \leq z \leq 0.1$ ) therefore anticipates the range (MPEP2131.03.I).

Claims 9 and 24 are rejected under 35 U.S.C. 103 as being unpatentable over Sakai as applied to claim 1 and 16, respectively, above, and further in view of Campbell et al., US 2003/0047752 (corresponding to US7,045,833).

In re Claim 9, Sakai discloses all limitations of claim 9 except for that semiconductor, further comprising a multiplication layer between the absorber layer and one of the first and second doped III-V layers.

Campbell teaches a semiconductor comprising a multiplication layer 142c between the absorber layer 142b and one of the first and second doped III-V layers 142d (Fig. 73; [0383-0385]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine teachings of Sakai and Campbell, and to use the specified multiplication layer for low excess noise as taught by Campbell ([00384]).

In re Claim 24, Sakai discloses all limitations of claim 24 except for forming a multiplication layer between the absorber layer and one of the first and second doped III-V layers.

Campbell teaches a method comprising forming a multiplication layer 142c between the absorber layer 142b and one of the first and second doped III-V layers 142d (Fig. 73; [0383-0385]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine teachings of Sakai and Campbell, and to form the specified multiplication layer for low excess noise as taught by Campbell ([00384]).

Claims 11, 12, and 26, 27 are rejected under 35 U.S.C. 103 as being unpatentable over Sakai as applied to claim 1 and 16, respectively, above, and further in view of Baribeau et al., "Heteroepitaxy of Ge on (100) Si substrates," Journal of Vacuum Science & Technology, A 5 (4), pp. 1898-1902; Jul/Aug 1987 (listed in IDS filed on 10/07/2016).

In re Claim 11, Sakai discloses all limitations of claim 11 except for that the substrate comprises: a silicon substrate; and a lattice engineered layer over the silicon substrate, the surface of the lattice engineered layer opposite the silicon substrate having a lattice parameter that is matched or nearly matched to GaAs.

Baribeau teaches a semiconductor wherein the substrate (Fig. 1) comprises: a silicon substrate Si; and a lattice engineered layer over the silicon substrate Si, the surface of the lattice engineered layer opposite the silicon substrate having a lattice parameter that is matched or nearly matched to GaAs (Fig. 1a; pages 1898-1899).

It would have been obvious to one of ordinary skill in the art at the time of the invention to substitute Sakai's substrate with Baribeau's substrate, and to use the specified for growing high-quality semiconducting layers as taught by Baribeau (page 1898, left column).

In re Claim 12, Sakai taken with Baribeau discloses the semiconductor of claim 11, wherein the lattice engineered layer comprises a  $\text{Si}_x\text{Ge}_{1-x}$  layer, with x graded from 1 at a surface of the  $\text{Si}_x\text{Ge}_{1-x}$  layer nearest the silicon substrate to 0 (i.e. Ge) at a surface of the  $\text{Si}_x\text{Ge}_{1-x}$  layer opposite the silicon substrate (Baribeau: Fig. 1a).

In re Claim 26, Sakai discloses all limitations of claim 26 except for that the substrate comprises: a silicon substrate; and a lattice engineered layer over the silicon substrate, the surface of the lattice engineered layer opposite the silicon substrate having a lattice parameter that is matched or nearly matched to GaAs.

Baribeau teaches a method wherein the substrate (Fig. 1) comprises: a silicon substrate Si; and a lattice engineered layer over the silicon substrate Si, the surface of the lattice engineered layer opposite the silicon substrate having a lattice parameter that is matched or nearly matched to GaAs (Fig. 1a; pages 1898-1899).

It would have been obvious to one of ordinary skill in the art at the time of the invention to substitute Sakai's substrate with Baribeau's substrate, and to use the specified for growing high-quality semiconducting layers as taught by Baribeau (page 1898, left column).

In re Claim 27, Sakai taken with Baribeau discloses the method of claim 26, wherein the lattice engineered layer comprises a  $\text{Si}_x\text{Ge}_{1-x}$  layer, with x graded from 1 at a surface of the  $\text{Si}_x\text{Ge}_{1-x}$  layer nearest the silicon substrate to 0 (i.e. Ge) at a surface of the  $\text{Si}_x\text{Ge}_{1-x}$  layer opposite the silicon substrate (Baribeau: Fig. 1a).

Claims 13 and 28 are rejected under 35 U.S.C. 103 as being unpatentable over Sakai and Baribeau as applied to claim 11 and 26, respectively, above, and further in view Dargis et al.,

"Growth and application of epitaxial heterostructures with polymorphous rare-earth oxides,  
Journal of Crystal Growth, 378 (2013) 177-179 (listed in IDS filed on 10/07/2016).

In re Claim 13, Sakai taken with Baribeau discloses all limitations of claim 13 except for that the lattice engineered layer comprises a rare earth containing layer, the rare earth containing layer comprising one or more of Sc, Y, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, and/or Lu.

Dargis teaches a semiconductor wherein the lattice engineered layer comprises a rare earth containing layer, the rare earth containing layer comprising one or more of Sc, Y, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, and/or Lu (Fig. 1; pages 178-179).

It would have been obvious to one of ordinary skill in the art at the time of the invention to substitute Sakai-Baribeau's lattice engineered layer with Dargis' layer comprising a rare earth containing layer, for close matching of lattice constants as taught by Dargis (Abstract).

In re Claim 28, Sakai taken with Baribeau discloses all limitations of claim 28 except for that the lattice engineered layer comprises a rare earth containing layer, the rare earth containing layer comprising one or more of Sc, Y, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, and/or Lu.

Dargis teaches a method wherein the lattice engineered layer comprises a rare earth containing layer, the rare earth containing layer comprising one or more of Sc, Y, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, and/or Lu (Fig. 1; pages 178-179).

It would have been obvious to one of ordinary skill in the art at the time of the invention to substitute Sakai-Baribeau's lattice engineered layer with Dargis' layer comprising a rare earth containing layer, for close matching of lattice constants as taught by Dargis (Abstract).

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. Ilegems et al., US 4,127,862;
2. Iguchi et al., US 2010/0072457;
3. Rajavel., US 8093559.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NIKOLAY YUSHIN whose telephone number is (571)270-7885. The examiner can normally be reached on 8 AM - 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/NIKOLAY YUSHIN/  
Primary Examiner, Art Unit 2893

<b>Notice of References Cited</b>	Application/Control No. 15/188,396	Applicant(s)/Patent Under Reexamination YANKA ET AL.	
	Examiner NIKOLAY YUSHIN	Art Unit 2893	Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-4,127,862 A	11-1978	Ilegems; Marc	G02B6/4202	136/249
*	B	US-4,682,196 A	07-1987	Sakai; Kazuo	H01L31/035281	257/458
*	C	US-2003/0047752 A1	03-2003	Campbell, Joe C.	H01L31/107	257/186
*	D	US-7,045,833 B2	05-2006	Campbell; Joe C.	H01L31/107	257/185
*	E	US-2010/0072457 A1	03-2010	Iguchi; Yasuhiro	B82Y20/00	257/21
*	F	US-8,093,559 B1	01-2012	Rajavel; Rajesh D.	H01L31/03046	250/330
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Takeda et al., "Electron mobility and energy gap of In <sub>0.53</sub> Ga <sub>0.47</sub> As on InP substrate", 1976, Journal of Applied Physics, Vol. 47, No 12, p.5405-5408, published Dec. 1976
	V	
	W	
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

## EAST Search History

## EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	4	((Robert) near2 (Yanka)).INV.	US-PGPUB; USPAT	AND	ON	2016/11/28 14:50
S2	0	((Seokjae) near2 (Chung)).INV.	US-PGPUB; USPAT	AND	ON	2016/11/28 14:51
S3	0	((Kalyan) near2 (Nunna)).INV.	US-PGPUB; USPAT	AND	ON	2016/11/28 14:51
S4	0	((Rodney) near2 (Pelzel)).INV.	US-PGPUB; USPAT	AND	ON	2016/11/28 14:51
S5	941	((Howard) near2 (Williams)).INV.	US-PGPUB; USPAT	AND	ON	2016/11/28 14:51
S6	4	((Robert) near2 (Yanka)).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM TDB	AND	ON	2016/11/28 14:52
S7	0	((Seokjae) near2 (Chung)).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM TDB	AND	ON	2016/11/28 14:52
S8	0	((Kalyan) near2 (Nunna)).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM TDB	AND	ON	2016/11/28 14:52
S9	0	((Rodney) near2 (Pelzel)).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM TDB	AND	ON	2016/11/28 14:52
S10	3991	((Howard) near2 (Williams)).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM TDB	AND	ON	2016/11/28 14:53
S11	4	(S5 OR S6 OR S7 OR S8 OR S9 Or S10) AND (IQE).AS.	US-PGPUB; USPAT; USOCR; FPRS;	AND	ON	2016/11/28 14:54

			EPO; JPO; DERWENT; IBM_TDB			
S12	44	(IQE).AS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/11/28 14:54
S13	30	("III-V" In\$6Ga\$6N\$6As\$6Sb)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/11/28 15:56
S14	1	(13/197588).APP.	USPAT; USOCR	AND	ON	2016/11/28 16:05
S15	0	(14/599290).APP.	USPAT; USOCR	AND	ON	2016/11/28 16:09
S16	54	("GaAs" In\$6Ga\$6N\$6As\$6Sb)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/11/28 16:16
S17	4471	("GaAs" substrate bandgap carrier doped absorb\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/11/28 16:19
S18	19	("GaAs" substrate bandgap carrier doped absorb\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/28 16:20
S19	2	("GaAs" substrate bandgap carrier concentration doped absorb\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/28 16:24
S20	6	("GaAs" AND (substrate bandgap carrier concentration doped absorb\$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/28 16:25
S21	1	(13/727845).APP.	USPAT; USOCR	AND	ON	2016/11/28 16:32
S22	28	((("GaAs" substrate) AND (bandgap carrier ADJ concentration) absorb\$4))	US-PGPUB; USPAT;	SAME	ON	2016/11/28 16:34

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S23	46	(( "GaAs" substrate) AND (band\$1gap (carrier ADJ concentration) absorb\$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/28 16:34
S24	46	(( "GaAs" substrate) AND ((bandgap OR band\$1gap) (carrier ADJ concentration) absorb\$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/28 16:34
S25	32	("3353114"   "3514715"   "3604987"   "3659159"   "3852591"   "4015280"   "4017332").PN. OR ("4127862").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2016/11/28 17:57
S26	22	("GaAs" In\$6Ga\$6N\$6As\$6Sb)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/28 18:37
S27	5	(absorb\$6 In\$6Ga\$6N\$6As\$6Sb)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/28 18:39
S28	35	("20020195677"   "20040061056"   "20040108461"   "20040108564"   "20060118722"   "20060162768"   "20060164633"   "20070075224"   "20080111152"   "20090121307"   "4679063"   "4847489"   "5093580"   "5113076"   "5216244"   "5229611"   "5453727"   "5457331"   "5581084"   "5729018"   "5731621"   "5977557"   "6043550"   "6049116"   "6157020"   "6455908"   "6504222"   "6803557"   "7067856"   "7671341").PN. OR ("8093559").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2016/11/28 18:41
S29	1	(absorb\$6 "InGaNaSb")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/28 18:47
S30	50	(In\$6Ga\$6N\$6As\$6Sb layer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	SAME	ON	2016/11/28 18:48

			DERWENT; IBM_TDB			
S31	52	(In\$6Ga\$6N\$6As\$6Sb\$4 layer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/29 08:26
S32	76	(In\$6Ga\$6N\$6As\$6Sb\$6)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/29 08:26
S33	76	(In\$6Ga\$6N\$6As\$6Sb\$6 OR "InGaNaSb")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/29 08:27
S34	6	( "InGaNaSb")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/29 08:27
S35	18	S32 AND (H01L31/1075; H01L31/03046; H01L31/03044).CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/29 08:28
S36	0	(In\$6Ga\$6N\$6As\$6Sb\$6 AND multiplication)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/29 08:31
S37	0	(S33 AND multiplication)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/29 08:31
S38	328570	( multiplication)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/29 08:31
S39	1	("7045833").PN.	US-PGPUB; USPAT	OR	OFF	2016/11/29 08:47

## EAST Search History

S40	1	(09/969133).APP.	US-PGPUB; USOCR	AND	ON	2016/11/29 08:47
S41	1	((("8957376") or ("2010096665")).PN.	US-PGPUB; USPAT	OR	OFF	2016/11/29 14:28
S42	1	((("8957376") or ("2010096665")).PN.	US-PGPUB; USPAT	OR	OFF	2016/11/29 14:28
S43	0	("2010096665").PN.	US-PGPUB; USPAT	OR	OFF	2016/11/29 14:28
S44	1	("8957376").PN.	US-PGPUB; USPAT	AND	ON	2016/11/29 14:30
S45	0	("(MacDougal).INV.").PN.	US-PGPUB; USPAT	OR	OFF	2016/11/29 14:32
S46	0	("(MacDougal).IN.").PN.	US-PGPUB; USPAT	OR	OFF	2016/11/29 14:32
S47	0	("(MacDougal).IN.").PN.	US-PGPUB; USPAT	OR	OFF	2016/11/29 14:33
S48	1	("20100096665").PN.	US-PGPUB; USPAT	OR	OFF	2016/11/29 14:33
S49	1	(12/254634).APP.	USPAT; USOCR	AND	ON	2016/11/29 14:38
S50	1	("4032951").PN. OR ("7915639").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2016/11/29 14:52

11/ 29/ 2016 6:05:43 PM

C:\Users\nyushin\Documents\EAST\Workspaces\15188396.wsp

15188396 - GAU: 2893

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<p>Substitute for form 1449/PTO</p> <p><b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b></p> <p><i>(Use as many sheets as necessary)</i></p>				<b>Complete if Known</b>	
				Application Number	Not Yet Assigned
				Filing Date	Concurrently Herewith
				First Named Inventor	Robert Yanka
				Art Unit	N/A
				Examiner Name	Not Yet Assigned
				Attorney Docket Number	111848-0002-101
Sheet	1	of	3		

[illegible][illegible]

Examiner Signature	/Nikolay Yushin/	Date Considered	11/29/2016
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. <sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> See Kinds Codes of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04. <sup>3</sup> Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>5</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. <sup>6</sup> Applicant is to place a check mark here if English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.Y./

Substitute for form 1449/PTO				<b>Complete if Known</b>	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  <i>(Use as many sheets as necessary)</i>				Application Number	Not Yet Assigned
				Filing Date	Concurrently Herewith
				First Named Inventor	Robert Yanka
				Art Unit	N/A
				Examiner Name	Not Yet Assigned
Sheet	2	of	3	Attorney Docket Number	111848-0002-101

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		Cheah et al., "GaAs-Based Heterojunction p-i-n Photodetectors Using Pentanary InGaAsNSb as the Intrinsic Layer," <i>IEEE Photonics Technology Letters</i> , Vol. 17, No. 9, September 2005, 3 pages.	
		Chen, et al., "GaAsSbN/GaAs long wavelength PIN detectors," <i>Indium Phosphide and Related Materials</i> , 2008. IPRM 2008. 20th International Conference on, Versailles, 2008, 4 pages.	
		Ferguson et al., "Optical Gain in GaInNAs and GaInNAsSb Quantum Wells," <i>IEEE Journal of Quantum Electronics</i> , Vol. 47, No. 6, June 2011, 8 pages.	
		Gobet et al., "GaInNAsSb/GaAs vertical cavity surface-emitting lasers (VCSELs): Current challenges and techniques to realize multiple-wavelength laser arrays at 1.55 $\mu\text{m}$ ," <i>Proc. of SPIE</i> , Vol. 6908, February 2008, 13 pages.	
		Harris et al., Development of GaInNAsSb alloys: Growth, band structure, optical properties and applications," <i>Phys. Stat. Sol. (b)</i> 244, No. 8, 2707-2729 (2007), 23 pages.	
		Harris, J. S. Jr., "The opportunities, successes and challenges for GaInNAsSb," <i>Journal of Crystal Growth</i> 278 (2005) 2 March 2005, 15 pages.	
		Jackrel et al., "Thick lattice-matched GaInNAs films in photodetector applications," <i>Proc. of SPIE</i> , Vol. 5726, (2005), 8 pages.	
		Khalil et al., "Photoconductivity and photoluminescence under bias in GaInNAs/GaAs MQW p-i-n structures," <i>Nanoscale Research Letter</i> , 7:539 (2012), 4 pages.	
		Ng et al., "Long wavelength bulk GaInNAs p-i-n photodiodes lattice matched to GaAs," <i>Journal of Applied Physics</i> 101, (2007), 6 pages.	
		Niu et al., "GaAs-based room-temperature continuous-wave 1.59 $\mu\text{m}$ GaInNAsSb single-quantum-well laser diode grown by molecular-beam epitaxy," <i>Applied Physics Letters</i> , 5 December 2005, Vol. 87 No. 23, 4 pages.	

Examiner Signature	/Nikolay Yushin/	Date Considered	11/29/2016
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.Y./

Substitute for form 1449/PTO				<b>Complete if Known</b>	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  <i>(Use as many sheets as necessary)</i>				Application Number	Not Yet Assigned
				Filing Date	Concurrently Herewith
				First Named Inventor	Robert Yanka
				Art Unit	N/A
				Examiner Name	Not Yet Assigned
Sheet	3	of	3	Attorney Docket Number	111848-0002-101

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		Ohnaka et al., "A Low Dark Current InGaAs/InP p-i-n Photodiode with Covered Mesa Structure," <i>IEEE Transactions on Electron Devices</i> , Vol. Ed-34, No. 2, February 1987, 6 pages.	
		Ptak et al., "Effects of temperature, nitrogen ions, and antimony on wide depletion width GaInNAs," <i>Journal of Vacuum Science &amp; Technology B</i> , Second Series, Vol. 25, No. 3, May/June 2007, 6 pages.	
		Tan et al., "Dilute nitride GaInNAs and GaInNAsSb for solar cell applications," <i>Proc. of SPIE</i> , Vol. 8256 (2012), 10 pages.	
		Tan et al., "GaInNAsSb/GaAs Photodiodes for Long-Wavelength Applications," <i>IEEE Electron Device Letters</i> Vol. 32 No. 7, July 2011, 3 pages.	
		Tan et al., "Reduction of dark current and unintentional background doping in InGaAsN photodetectors by ex situ annealing," <i>Proc. of SPIE</i> , Vol. 7726, (2010), 8 pages.	
		Wistey et al., "Monolithic, GaInNAsSb VCSELs at 1.46 $\mu$ m on GaAs by MBE," <i>Electronics Letters</i> , 11 December 2003, Vol. 39, No. 25, 2 pages.	
		Yuen et al., "The role of antimony on properties of widely varying GaInNAsSb compositions," <i>Journal of Applied Physics</i> 99, (2006), 8 pages.	

Examiner Signature	/Nikolay Yushin/	Date Considered	11/29/2016
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Receipt date: 10/07/2016

PTO/SB/08b (07-09)

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Substitute for form 1449/PTO				<b>Complete if Known</b>	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  <i>(Use as many sheets as necessary)</i>				Application Number	15/188,396
				Filing Date	June 21, 2016
				First Named Inventor	Robert Yanka
				Art Unit	2811
				Examiner Name	Lynne Ann Gurley
Sheet	2	of	2	Attorney Docket Number	111848-0002-101


NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		Baribeau et al., "Heteroepitaxy of Ge on (100) Si substrates," <i>Journal of Vacuum Science &amp; Technology</i> , A 5 (4), Jul/Aug 1987 (6 Pages).	
		Dargis et al., "Growth and application of epitaxial heterostructures with polymorphous rare-earth oxides," <i>Journal of Crystal Growth</i> , 378 (2013) 177-179.	
		International Search Report and Written Opinion dated October 4, 2016 in PCT/US2016/038567, filed June 21, 2016 (15 pages).	

Examiner Signature	/Nikolay Yushin/	Date Considered	11/28/2016
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<sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached.

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<b>Search Notes</b>  	<b>Application/Control No.</b>  15188396	<b>Applicant(s)/Patent Under Reexamination</b>  YANKA ET AL.
	<b>Examiner</b>  NIKOLAY YUSHIN	<b>Art Unit</b>  2893

CPC- SEARCHED		
Symbol	Date	Examiner
H01L31/1075; H01L31/03046; H01L31/03044	11/29/2016	NY

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
Keyword, inventor names, assignee searching - see search history	11/29/2016	NY

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

	/NIKOLAY YUSHIN/ Primary Examiner.Art Unit 2893
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<p align="center"><b><i>Index of Claims</i></b></p> 	<b>Application/Control No.</b> 15188396	<b>Applicant(s)/Patent Under Reexamination</b> YANKA ET AL.
	<b>Examiner</b> NIKOLAY YUSHIN	<b>Art Unit</b> 2893

✓	<b>Rejected</b>	-	<b>Cancelled</b>	N	<b>Non-Elected</b>	A	<b>Appeal</b>
=	<b>Allowed</b>	÷	<b>Restricted</b>	I	<b>Interference</b>	O	<b>Objected</b>

<input type="checkbox"/> Claims renumbered in the same order as presented by applicant											<input type="checkbox"/> CPA											<input type="checkbox"/> T.D.											<input type="checkbox"/> R.1.47										
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## BIB DATA SHEET

CONFIRMATION NO. 1083

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
15/188,396	06/21/2016	257	2893	111848-0002-101

**APPLICANTS**  
 IQE, plc, St. Mellons, UNITED KINGDOM;

**INVENTORS**  
 Robert Yanka, Kernersville, NC;  
 Seokjae Chung, Oak Ridge, NC;  
 Kalyan Nunna, High Point, NC;  
 Rodney Pelzel, Emmaus, PA;  
 Howard Williams, St. Mellons, UNITED KINGDOM;

**\*\* CONTINUING DATA \*\*\*\*\***  
 This appln claims benefit of 62/183,060 06/22/2015

**\*\* FOREIGN APPLICATIONS \*\*\*\*\***

**\*\* IF REQUIRED, FOREIGN FILING LICENSE GRANTED \*\***  
 06/30/2016

Foreign Priority claimed 35 USC 119(a-d) conditions met Verified and Acknowledged	<input type="checkbox"/> Yes <input checked="" type="checkbox"/> No <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No /NIKOLAY K YUSHIN/ Examiner's Signature	<input type="checkbox"/> Met after Allowance Initials	STATE OR COUNTRY NC	SHEETS DRAWINGS 9	TOTAL CLAIMS 30	INDEPENDENT CLAIMS 2
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**ADDRESS**  
 ROPES & GRAY LLP  
 IPRM Docketing - Floor 43  
 PRUDENTIAL TOWER  
 800 BOYLSTON STREET  
 BOSTON, MA 02199-3600  
 UNITED STATES

**TITLE**  
 OPTOELECTRONIC DETECTORS HAVING A DILUTE NITRIDE LAYER ON A SUBSTRATE WITH A  
 LATTICE PARAMETER NEARLY MATCHING GAAS

<b>FILING FEE RECEIVED</b> 2540	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	<input type="checkbox"/> All Fees
		<input type="checkbox"/> 1.16 Fees (Filing)
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Substitute for form 1449/PTO				<b>Complete if Known</b>	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  <i>(Use as many sheets as necessary)</i>				Application Number	15/188,396
				Filing Date	June 21, 2016
				First Named Inventor	Robert Yanka
				Art Unit	2811
				Examiner Name	Lynne Ann Gurley
Sheet	2	of	2	Attorney Docket Number	111848-0002-101

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		Baribeau et al., "Heteroepitaxy of Ge on (100) Si substrates," <i>Journal of Vacuum Science &amp; Technology, A</i> 5 (4), Jul/Aug 1987 (6 Pages).	
		Dargis et al., "Growth and application of epitaxial heterostructures with polymorphous rare-earth oxides," <i>Journal of Crystal Growth</i> , 378 (2013) 177-179.	
		International Search Report and Written Opinion dated October 4, 2016 in PCT/US2016/038567, filed June 21, 2016 (15 pages).	

Examiner Signature		Date Considered	
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<sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached.

Docket No.: 111848-0002-101  
(PATENT)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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In re Patent Application of:  
Yanka et al.

Application No.: 15/188,396

Confirmation No.: 1083

Filed: June 21, 2016

Art Unit: 2811

For: OPTOELECTRONIC DETECTORS HAVING A  
DILUTE NITRIDE LAYER ON A SUBSTRATE  
WITH A LATTICE PARAMETER NEARLY  
MATCHING GAAS

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Examiner: Lynne Ann Gurley

**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT (SIDS)**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to 37 C.F.R. § 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Supplemental Information Disclosure Statement is filed before the mailing date of a first Office Action on the merits as far as is known to the undersigned (37 C.F.R. § 1.97(b)(3)).

In accordance with 37 C.F.R. § 1.98(a)(2)(ii), Applicant has not submitted a copy of the U.S. patent publication. Applicant submits herewith copies of non-patent literature in accordance with 37 C.F.R. § 1.98(a)(2).

In accordance with 37 C.F.R. § 1.97(g), the filing of this Supplemental Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 C.F.R. § 1.56(a) exists. In accordance with 37 C.F.R. § 1.97(h), the filing of this Supplemental Information Disclosure Statement shall not be construed to be an admission that any patent, publication or other information referred to therein is “prior art” for this invention unless specifically designated as such.

It is submitted that the Supplemental Information Disclosure Statement is in compliance with 37 C.F.R. § 1.98 and the Examiner is respectfully requested to consider the listed references.

The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 18-1945.

Dated: October 7, 2016

Respectfully submitted,

By /James F. Mack/

James F. Mack

Registration No.: 74,196

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/188,396	06/21/2016	Robert Yanka	111848-0002-101

**CONFIRMATION NO. 1083**

**POA ACCEPTANCE LETTER**



OC000000084370624

28120  
ROPES & GRAY LLP  
IPRM Docketing - Floor 43  
PRUDENTIAL TOWER  
800 BOYLSTON STREET  
BOSTON, MA 02199-3600

Date Mailed: 07/15/2016

**NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY**

This is in response to the Power of Attorney filed 07/01/2016.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/zmoguss/

<b>PATENT APPLICATION FEE DETERMINATION RECORD</b> Substitute for Form PTO-875						Application or Docket Number 15/188,396	
<b>APPLICATION AS FILED - PART I</b>							
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	30	minus 20 = *	10			x 80 =	800
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2	minus 3 = *				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL		TOTAL	2400
<b>APPLICATION AS AMENDED - PART II</b>							
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =	x =	=
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =	x =	=
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
				TOTAL ADD'L FEE		TOTAL ADD'L FEE	
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =	x =	=
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =	x =	=
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
				TOTAL ADD'L FEE		TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.							



# UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY DOCKET NO	TOT CLAIMS	IND CLAIMS
15/188,396	06/21/2016	2811	2540	111848-0002-101	30	2

CONFIRMATION NO. 1083

## FILING RECEIPT



28120  
ROPES & GRAY LLP  
IPRM Docketing - Floor 43  
PRUDENTIAL TOWER  
800 BOYLSTON STREET  
BOSTON, MA 02199-3600

Date Mailed: 07/05/2016

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

### Inventor(s)

Robert Yanka, Kernersville, NC;  
Seokjae Chung, Oak Ridge, NC;  
Kalyan Nunna, High Point, NC;  
Rodney Pelzel, Emmaus, PA;  
Howard Williams, St. Mellons, UNITED KINGDOM;

### Applicant(s)

IQE, plc, St. Mellons, UNITED KINGDOM;

Power of Attorney: None

### Domestic Priority data as claimed by applicant

This appln claims benefit of 62/183,060 06/22/2015

**Foreign Applications** for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

*Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.*

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

**If Required, Foreign Filing License Granted:** 06/30/2016

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/188,396**

**Projected Publication Date:** 12/22/2016

**Non-Publication Request:** No

**Early Publication Request:** No  
**Title**

OPTOELECTRONIC DETECTORS HAVING A DILUTE NITRIDE LAYER ON A SUBSTRATE WITH  
A LATTICE PARAMETER NEARLY MATCHING GAAS

**Preliminary Class**

257

**Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications:** No

## **PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES**

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

**LICENSE FOR FOREIGN FILING UNDER**  
**Title 35, United States Code, Section 184**  
**Title 37, Code of Federal Regulations, 5.11 & 5.15**

**GRANTED**

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

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The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

**NOT GRANTED**

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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Doc Code: PA..  
Document Description: Power of Attorney

PTO/AIA/82B (07-13)  
Approved for use through 11/30/2014. OMB 0651-0051  
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## TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA/82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	15/188,396		
Filing Date	June 21, 2016		
First Named Inventor	Robert Yanka		
Title	OPTOELECTRONIC DETECTORS HAVING A DILUTE NITRIDE LAYER ON A SUBSTRATE WITH A LATTICE PARAMETER NEARLY MATCHING GAAS		
Art Unit	2811		
Examiner Name	Not Yet Assigned		
Attorney Docket Number	111848-0002-101		
<b>SIGNATURE of Applicant or Patent Practitioner</b>			
Signature	/James F. Mack/	Date (Optional)	July 1, 2016
Name	James F. Mack	Registration Number	74,196
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			
<b>NOTE:</b> This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.			
<input checked="" type="checkbox"/> *Total of <u>1</u> forms are submitted.			

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

## POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☒ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above:

28120

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☒ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

Firm or Individual Name			
Address			
City	State	Zip	
Country			
Telephone	Email		


I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

IQE, plc

- ☐ Inventor or Joint Inventor (title not required below)
- ☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)
- ☒ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)
- ☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

### SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature		Date (Optional)	15 JUNE 2016
Name	Rodney Pelzel, Ph.D.		
Title	Vice President, Group Technology for IQE, plc.		

**NOTE:** Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☒ Total of 1 forms are submitted.

**STATEMENT UNDER 37 CFR 3.73(c)**

Applicant/Patent Owner: IQE, plc

Application No./Patent No.: 15/188,396 Filed/Issue Date: June 21, 2016

Titled: OPTOELECTRONIC DETECTORS HAVING A DILUTE NITRIDE LAYER ON A SUBSTRATE WITH A LATTICE PARAMETER MATCHING GAAS

IQE, plc, a Corporation  
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is \_\_\_\_\_ %. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

- A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 039046, Frame 0343, or for which a copy thereof is attached.
- B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:
1. From: \_\_\_\_\_ To: \_\_\_\_\_  
The document was recorded in the United States Patent and Trademark Office at Reel \_\_\_\_\_, Frame \_\_\_\_\_, or for which a copy thereof is attached.
2. From: \_\_\_\_\_ To: \_\_\_\_\_  
The document was recorded in the United States Patent and Trademark Office at Reel \_\_\_\_\_, Frame \_\_\_\_\_, or for which a copy thereof is attached.

**STATEMENT UNDER 37 CFR 3.73(c)**

3. From: \_\_\_\_\_ To: \_\_\_\_\_

The document was recorded in the United States Patent and Trademark Office at  
Reel \_\_\_\_\_, Frame \_\_\_\_\_, or for which a copy thereof is attached.

4. From: \_\_\_\_\_ To: \_\_\_\_\_

The document was recorded in the United States Patent and Trademark Office at  
Reel \_\_\_\_\_, Frame \_\_\_\_\_, or for which a copy thereof is attached.

5. From: \_\_\_\_\_ To: \_\_\_\_\_

The document was recorded in the United States Patent and Trademark Office at  
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6. From: \_\_\_\_\_ To: \_\_\_\_\_

The document was recorded in the United States Patent and Trademark Office at  
Reel \_\_\_\_\_, Frame \_\_\_\_\_, or for which a copy thereof is attached.☐ Additional documents in the chain of title are listed on a supplemental sheet(s).☒ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

\_\_\_\_\_  
Signature /James F. Mack/\_\_\_\_\_  
Date July 1, 2016\_\_\_\_\_  
Printed or Typed Name James F. Mack\_\_\_\_\_  
Title or Registration Number 74,196

## Electronic Acknowledgement Receipt

<b>EFS ID:</b>	26246110
<b>Application Number:</b>	15188396
<b>International Application Number:</b>	
<b>Confirmation Number:</b>	1083
<b>Title of Invention:</b>	OPTOELECTRONIC DETECTORS HAVING A DILUTE NITRIDE LAYER ON A SUBSTRATE WITH A LATTICE PARAMETER NEARLY MATCHING GAAS
<b>First Named Inventor/Applicant Name:</b>	Robert Yanka
<b>Customer Number:</b>	28120
<b>Filer:</b>	James Francis Mack/Pamela Harrison
<b>Filer Authorized By:</b>	James Francis Mack
<b>Attorney Docket Number:</b>	111848-0002-101
<b>Receipt Date:</b>	01-JUL-2016
<b>Filing Date:</b>	21-JUN-2016
<b>Time Stamp:</b>	19:37:07
<b>Application Type:</b>	Utility under 35 USC 111(a)

### Payment information:

Submitted with Payment	no
------------------------	----

### File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	111848-0002-101_POA.pdf	126345	no	2
			68238e8c60f8a8094d216ddad0f1cb68bac6bf2b		

### Warnings:

<b>Information:</b>					
2	Assignee showing of ownership per 37 CFR 3.73	111848-0002-101_Assignee_Statement.pdf	71105	no	2
			1b09b5c0886da3d7ce35ff871d8beef1241c6927		
<b>Warnings:</b>					
<b>Information:</b>					
<b>Total Files Size (in bytes):</b>			197450		
<p><b>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</b></p> <p><b><u>New Applications Under 35 U.S.C. 111</u></b>  If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><b><u>National Stage of an International Application under 35 U.S.C. 371</u></b>  If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><b><u>New International Application Filed with the USPTO as a Receiving Office</u></b>  If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN  
APPLICATION DATA SHEET (37 CFR 1.76)**

**Title of  
Invention**

**OPTOELECTRONIC DETECTORS HAVING A DILUTE NITRIDE LAYER ON A SUBSTRATE WITH A  
LATTICE PARAMETER NEARLY MATCHING GAAS**

As the below named inventor, I hereby declare that:

This declaration ☐ The attached application, or  
is directed to:

☒ United States application or PCT international application number 15/188,396  
filed on June 21, 2016

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001  
by fine or imprisonment of not more than five (5) years, or both.

**WARNING:**

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

**LEGAL NAME OF INVENTOR**

Inventor: Robert Yanka Date (Optional) : \_\_\_\_\_

Signature: 

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN  
APPLICATION DATA SHEET (37 CFR 1.76)**

**Title of  
Invention**

**OPTOELECTRONIC DETECTORS HAVING A DILUTE NITRIDE LAYER ON A SUBSTRATE WITH A  
LATTICE PARAMETER NEARLY MATCHING GAAS**

As the below named inventor, I hereby declare that:

This declaration ☒ The attached application, or  
is directed to:

☐ United States application or PCT international application number \_\_\_\_\_  
filed on \_\_\_\_\_.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

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**WARNING:**

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**LEGAL NAME OF INVENTOR**

Inventor: Seokjae Chung

Date (Optional): 6/21/2016

Signature: \_\_\_\_\_



Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN  
APPLICATION DATA SHEET (37 CFR 1.76)**

**Title of  
Invention**

**OPTOELECTRONIC DETECTORS HAVING A DILUTE NITRIDE LAYER ON A SUBSTRATE WITH A  
LATTICE PARAMETER NEARLY MATCHING GAAS**

As the below named inventor, I hereby declare that:

This declaration ☒ The attached application, or  
is directed to:

☐ United States application or PCT international application number \_\_\_\_\_  
filed on \_\_\_\_\_

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

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by fine or imprisonment of not more than five (5) years, or both.

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**LEGAL NAME OF INVENTOR**

Inventor: Kalyan Nunna

Date (Optional): 06/21/2016

Signature: 

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN  
APPLICATION DATA SHEET (37 CFR 1.76)**

<b>Title of Invention</b>	OPTOELECTRONIC DETECTORS HAVING A DILUTE NITRIDE LAYER ON A SUBSTRATE WITH A LATTICE PARAMETER NEARLY MATCHING GAAS
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As the below named inventor, I hereby declare that:

This declaration ☒ The attached application, or  
is directed to: ☐ United States application or PCT international application number \_\_\_\_\_  
filed on \_\_\_\_\_.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001  
by fine or imprisonment of not more than five (5) years, or both.

**WARNING:**

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

**LEGAL NAME OF INVENTOR**

Inventor: Rodney Peizel Date (Optional): 21 June 2016

Signature: 

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN  
APPLICATION DATA SHEET (37 CFR 1.76)**

**Title of  
Invention**

OPTOELECTRONIC DETECTORS HAVING A DILUTE NITRIDE LAYER ON A SUBSTRATE WITH A  
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As the below named inventor, I hereby declare that:

This declaration ☒ The attached application, or  
is directed to:

☐ United States application or PCT international application number \_\_\_\_\_  
filed on \_\_\_\_\_

The above-identified application was made or authorized to be made by me.

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**LEGAL NAME OF INVENTOR**

Inventor: Howard Williams

Date (Optional): 06/21/16

Signature: 

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

## Electronic Acknowledgement Receipt

<b>EFS ID:</b>	26215457
<b>Application Number:</b>	15188396
<b>International Application Number:</b>	
<b>Confirmation Number:</b>	1083
<b>Title of Invention:</b>	OPTOELECTRONIC DETECTORS HAVING A DILUTE NITRIDE LAYER ON A SUBSTRATE WITH A LATTICE PARAMETER NEARLY MATCHING GAAS
<b>First Named Inventor/Applicant Name:</b>	Robert Yanka
<b>Customer Number:</b>	28120
<b>Filer:</b>	James Francis Mack/Pamela Harrison
<b>Filer Authorized By:</b>	James Francis Mack
<b>Attorney Docket Number:</b>	111848-0002-101
<b>Receipt Date:</b>	29-JUN-2016
<b>Filing Date:</b>	
<b>Time Stamp:</b>	18:14:42
<b>Application Type:</b>	Utility under 35 USC 111(a)

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### File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Oath or Declaration filed	111848-0002-101_Declaration.pdf	1221590  1c4f7280c5c8831bf05f8f1d2609b47b09b6a672	no	5

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<b>UTILITY PATENT APPLICATION TRANSMITTAL</b>		<b>Attorney Docket No.</b> 111848-0002-101	
		<b>First Named Inventor</b> Robert Yanka	
		<b>Title</b> OPTOELECTRONIC DETECTORS HAVING A DILUTE NITRIDE LAYER ON A SUBSTRATE WITH A LATTICE PARAMETER NEARLY MATCHING GAAS	
<i>(Only for new nonprovisional applications under 37 CFR 1.53(b))</i>		<b>Express Mail Label No.</b>	

<b>APPLICATION ELEMENTS</b> <i>See MPEP chapter 600 concerning utility patent application contents.</i>	<b>ADDRESS TO:</b> Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450
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<ol style="list-style-type: none"> <li>1. <input type="checkbox"/> <b>Fee Transmittal Form</b>            (PTO/SB/17 or equivalent)</li> <li>2. <input type="checkbox"/> <b>Applicant asserts small entity status.</b>            See 37 CFR 1.27</li> <li>3. <input type="checkbox"/> <b>Applicant certifies micro entity status.</b> See 37 CFR 1.29.            Applicant must attach form PTO/SB/15A or B or equivalent.</li> <li>4. <input checked="" type="checkbox"/> <b>Specification</b> [Total Pages <u>24</u>]            Both the claims and abstract must start on a new page.            (See MPEP § 608.01(a) for information on the preferred arrangement)</li> <li>5. <input checked="" type="checkbox"/> <b>Drawing(s)</b> (35 U.S.C. 113) [Total Sheets <u>9</u>]</li> <li>6. <input type="checkbox"/> <b>Inventor's Oath or Declaration</b> [Total Pages _____]            (including substitute statements under 37 CFR 1.64 and assignments            serving as an oath or declaration under 37 CFR 1.63(e))           <ol style="list-style-type: none"> <li>a. <input type="checkbox"/> Newly executed (original or copy)</li> <li>b. <input type="checkbox"/> A copy from a prior application (37 CFR 1.63(d))</li> </ol> </li> <li>7. <input checked="" type="checkbox"/> <b>Application Data Sheet</b> * See note below.            See 37 CFR 1.76 (PTO/AIA/14 or equivalent)</li> <li>8. <input type="checkbox"/> <b>CD-ROM or CD-R</b>            in duplicate, large table, or Computer Program (Appendix)  <input type="checkbox"/> Landscape Table on CD</li> <li>9. <b>Nucleotide and/or Amino Acid Sequence Submission</b>            (if applicable, items a. – c. are required)           <ol style="list-style-type: none"> <li>a. <input type="checkbox"/> Computer Readable Form (CRF)</li> <li>b. <input type="checkbox"/> Specification Sequence Listing on:               <ol style="list-style-type: none"> <li>i. <input type="checkbox"/> CD-ROM or CD-R (2 copies); or</li> <li>ii. <input type="checkbox"/> Paper</li> </ol> </li> <li>c. <input type="checkbox"/> Statements verifying identity of above copies</li> </ol> </li> </ol>	<b>ACCOMPANYING APPLICATION PAPERS</b> <ol style="list-style-type: none"> <li>10. <input type="checkbox"/> <b>Assignment Papers</b>            (cover sheet &amp; document(s))             Name of Assignee  <div style="border: 1px solid black; height: 20px; width: 100%;"></div> </li> <li>11. <input type="checkbox"/> <b>37 CFR 3.73(c) Statement</b> <input type="checkbox"/> <b>Power of Attorney</b>            (when there is an assignee)</li> <li>12. <input type="checkbox"/> <b>English Translation Document</b> (if applicable)</li> <li>13. <input checked="" type="checkbox"/> <b>Information Disclosure Statement</b>            (PTO/SB/08 or PTO-1449)  <input checked="" type="checkbox"/> Copies of citations attached</li> <li>14. <input type="checkbox"/> <b>Preliminary Amendment</b></li> <li>15. <input type="checkbox"/> <b>Return Receipt Postcard</b>            (MPEP § 503) (Should be specifically itemized)</li> <li>16. <input type="checkbox"/> <b>Certified Copy of Priority Document(s)</b>            (if foreign priority is claimed)</li> <li>17. <input type="checkbox"/> <b>Nonpublication Request</b>            Under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35            or equivalent.</li> <li>18. <input type="checkbox"/> <b>Other:</b> <div style="border: 1px solid black; height: 40px; width: 100%;"></div></li> </ol>
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**\*Note:** (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 **must** be included in an Application Data Sheet (ADS).  
 (2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).

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Optoelectronic Detectors Having a Dilute Nitride Layer on a Substrate With a Lattice Parameter  
Nearly Matching GaAs

Inventors

Robert Yanka, Seokjae Chung, Kalyan Nunna, Rodney Pelzel, Howard Williams

Cross Reference to Related Applications

**[0001]** This application claims priority to U.S. Provisional Application Serial No. 62/183,060, filed June 22, 2015, the entire contents of which are hereby incorporated by reference.

Background

**[0002]** III-V materials are the materials of choice for fabricating optoelectronic emitters and detectors for a variety of applications. One reason for this is that the bandgap of the III-V material can be chosen for the specific wavelength of interest. Fiber optic systems typically use the 1.33  $\mu\text{m}$  (micrometer) and 1.50  $\mu\text{m}$  wavelengths because of their transmission characteristics.

**[0003]** Historically, the vast majority of 1.33  $\mu\text{m}$  and 1.50  $\mu\text{m}$  emitters and detectors employ indium gallium arsenide (InGaAs) alloys as the emitting and detecting medium. To generate high quality InGaAs needed for an emitter or detector, it is preferred that the material be as free as possible of crystalline defects. The alloy composition and thickness of the InGaAs layers needed for functional devices necessitates growth on an indium phosphide (InP) substrate since InP has the same in-plane lattice parameter as  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  ( $E_g = 0.75$  eV at 300 K which corresponds to a wavelength of 1.65  $\mu\text{m}$ ).

**[0004]** From a cost perspective, it would be preferable to grow optoelectronic detectors and emitters on a less expensive substrate than InP, such as gallium arsenide (GaAs), germanium (Ge), or silicon (Si). However, the lattice mismatch between less expensive substrates and InGaAs alloys of desired composition results in highly defective material when grown sufficiently thick to fabricate a viable detector or emitter. Substrate cost is a significant portion of overall manufacturing cost, and therefore, finding a route to grow a material of sufficient bandgap on a less expensive substrate is of significant technical and practical interest.

## Summary

**[0005]** Optoelectronic detectors having one or more dilute nitride layers on substrates with lattice parameters matching or nearly matching GaAs are described herein. A semiconductor can include a substrate with a lattice parameter matching or nearly matching GaAs and a first doped III-V layer over the substrate. The semiconductor can also include an absorber layer over the first doped III-V layer, the absorber layer having a bandgap between approximately 0.7 eV and 0.95 eV and a carrier concentration less than approximately  $1 \times 10^{16} \text{ cm}^{-3}$  at room temperature. The semiconductor can also include a second doped III-V layer over the absorber layer.

**[0006]** The absorber layer can include a dilute nitride. The dilute nitride can include  $\text{In}_x\text{Ga}_{1-x}\text{N}_y\text{As}_{1-y-z}\text{Sb}_z$ , with x, y, and z falling within the following respective ranges: ( $0 \leq x \leq 1$ ;  $0 \leq y \leq 1$ ;  $0 \leq z \leq 1$ ). In some examples, x, y, and z can fall within the following respective ranges: ( $0 \leq x \leq 0.55$ ;  $0 \leq y \leq 0.1$ ;  $0 \leq z \leq 0.1$ ).

**[0007]** The carrier concentration of the absorber layer can be less than approximately  $5 \times 10^{15} \text{ cm}^{-3}$ , or it can be less than approximately  $1 \times 10^{15} \text{ cm}^{-3}$ . The thickness of the absorber layer can be between approximately 2 micrometers and approximately 10 micrometers, or it can be between approximately 3 micrometers and approximately 5 micrometers.

**[0008]** The semiconductor can further include a multiplication layer between the absorber layer and one of the first and second doped III-V layers.

**[0009]** One or more implementations can result in a substrate with a lattice parameter matching or nearly matching GaAs. The substrate can include GaAs. The substrate can include a silicon substrate and a lattice engineered layer over the silicon substrate, with the surface of the lattice engineered layer opposite the silicon substrate having a lattice parameter that is matched or nearly matched to GaAs. The lattice engineered layer can include a  $\text{Si}_x\text{Ge}_{1-x}$  layer, with x graded from 1 at a surface of the  $\text{Si}_x\text{Ge}_{1-x}$  layer nearest the silicon substrate to 0 at a surface of the  $\text{Si}_x\text{Ge}_{1-x}$  layer opposite the silicon substrate. The lattice engineered layer can include a rare earth containing layer, with the rare earth containing layer including one or more of Sc, Y, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, and/or Lu.

**[0010]** The first doped III-V layer can be n-type and the second doped III-V layer can be p-type. The first doped III-V layer can be p-type and the second doped III-V layer can be n-type.

### Brief Description of the Drawings

**[0011]** The above and other features of the present disclosure, including its nature and its various advantages, will be more apparent upon consideration of the following detailed description, taken in conjunction with the accompanying drawings in which:

**[0012]** FIG. 1 depicts a semiconductor comprising a p-i-n diode, according to an illustrative implementation;

**[0013]** FIG. 2 depicts a semiconductor with a p-i-n diode and a multiplication layer, according to an illustrative implementation;

**[0014]** FIG. 3 depicts a semiconductor with a GaAs-based p-i-n diode, according to an illustrative implementation;

**[0015]** FIG. 4 depicts a semiconductor with a GaAs-based p-i-n diode and a multiplication layer, according to an illustrative implementation;

**[0016]** FIG. 5 depicts a graph that shows the characterization of the semiconductor shown in FIG. 3 by x-ray diffraction (XRD), according to an illustrative implementation;

**[0017]** FIG. 6 depicts a graph that shows XRD scans of intrinsic InGaNaSb layers of different thicknesses epitaxially formed on GaAs, according to an illustrative implementation;

**[0018]** FIG. 7 depicts a graph that shows XRD scans of InGaNaSb layers grown on p-type and semi-insulating GaAs substrates, according to an illustrative implementation;

**[0019]** FIG. 8 depicts a graph showing the effect of the In/Sb ratio on carrier properties of InGaNaSb, as measured by the Hall effect, according to an illustrative implementation;

**[0020]** FIG. 9 depicts a graph showing the effect of the In/Sb ratio on optical properties of InGaNaSb, as measured by photoluminescence (PL), according to an illustrative implementation;

**[0021]** FIG. 10 depicts a graph that shows the effect of growth temperature and As flux on the carrier concentration of InGaNaSb, as measured by the Hall effect, according to an illustrative implementation;

**[0022]** FIG. 11 depicts a graph that shows the effect of growth temperature and arsenic flux on the bandgap of InGaNaSb, as measured by photoluminescence, according to an illustrative implementation;

**[0023]** FIG. 12 depicts a graph showing the effect of rapid thermal annealing (RTA) on the carrier concentration of InGaNaSb, as measured by the Hall effect, according to an illustrative implementation;

**[0024]** FIG. 13 includes a graph showing the effect of RTA on the bandgap of InGaNaSb as measured by photoluminescence, according to an illustrative implementation;

**[0025]** FIG. 14 depicts a graph that shows a photoluminescence spectrum of a 0.5  $\mu\text{m}$  layer of InGaNaSb grown on a GaAs substrate, according to an illustrative implementation;

**[0026]** FIG. 15 includes a colormap that shows cross-wafer variation in bandgap of a 0.5  $\mu\text{m}$  layer of InGaNaSb grown on a 150 mm GaAs substrate, according to an illustrative implementation; and

**[0027]** FIG. 16 illustrates several examples of p-i-n diodes formed over substrates with lattice parameters matching or nearly matching GaAs, according to an illustrative implementation.

#### Detailed Description

**[0028]** Systems and methods described herein include processes for the growth of high quality optoelectronic detectors on a substrate with a lattice parameter matching or nearly matching GaAs. Detectors described herein use a dilute nitride layer, typically an  $\text{In}_x\text{Ga}_{1-x}\text{N}_y\text{As}_{1-y-z}\text{Sb}_z$  layer as the absorbing medium, where  $x$  ranges from 0 to 0.55,  $y$  ranges from 0 to 0.1, and  $z$  ranges from 0 to 0.1, herein referred to as the InGaNaSb layer. The dilute nitride is a III-V material that includes low concentrations of nitrogen, concentrations that are low alloy-level concentrations and are higher than doping-level concentrations. The dilute nitride layer may have trace amounts of dopants or contamination, but in amounts that do not prevent the layer from functioning in a detector. In some examples the optoelectronic detectors use a p-i-n structure. In a typical p-i-n, the absorption medium is an intrinsic semiconductor (i) is sandwiched between an n-type semiconductor and a p-type semiconductor. The n-type region has electrons as the majority carrier, usually due to doping by donor dopants. The p-type region has holes as the majority carrier, usually due to doping by acceptor dopants. In operation, the diode is reverse biased which serves to “sweep” out carriers generated by photons of sufficient energy.

**[0029]** The substrate with a lattice parameter matching or nearly matching GaAs may comprise a GaAs substrate, a Ge substrate, or a lattice engineered substrate. Examples of lattice

engineered substrates include a substrate comprising a graded SiGe layer on a Si handle wafer and a substrate comprising a rare-earth containing layer on a Si handle wafer. The lattice parameter is a dimension of a unit cell in a crystal lattice. The substrate with a lattice parameter matching or nearly matching GaAs may have a lattice parameter that is the same as or slightly different than the lattice parameter of GaAs (5.65 Å), but is similar enough that high-quality GaAs can be epitaxially grown on the substrate surface. High quality GaAs can include a defect level that is comparable to or lower than a defect level of an  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  layer grown on an InP substrate. This can mean the substrate has a lattice parameter different than that of GaAs by less than or equal to 3%, less than 1%, or less than 0.5%.

**[0030]** An InGaNaSb absorber layer of high quality enables low cost, high performance detectors. One reason for this is that the absorber layer can be grown coherently (*i.e.*, crystalline, non-relaxed and with minimal defectivity) on a substrate with a lattice parameter matching or nearly matching GaAs. The composition of the InGaNaSb layer can be tuned so that a layer of desired bandgap and thickness can be coherently grown on a substrate with a lattice parameter matching or nearly matching GaAs with minimal defects. The bandgap is the energy difference between conduction and valence bands of a material, and can be direct (where electronic transitions between the bands can occur with only emission or absorption of a photon) or indirect (where electronic transitions between the bands require emission or absorption of a phonon in addition to emission or absorption of a photon). III-V materials generally have direct bandgaps, but the layers described herein can have direct or indirect bandgaps.

**[0031]** FIG. 1 depicts a semiconductor 100 comprising a p-i-n diode. The semiconductor 100 includes a substrate 114, an  $n^+$  III-V layer 112 epitaxially formed over the substrate 114, an intrinsic dilute nitride layer 106 epitaxially formed over the  $n^+$  III-V layer 112, and a  $p^+$  III-V layer 102 epitaxially formed over the dilute nitride layer 106.

**[0032]** The III-V layers 102 and 112 can include any III-V material, such as GaAs, InGaAs, AlGaAs, InGaP, InGaAsP, InGaAsN, InGaNaSb, or another III-V material. The substrate 114 can be a semiconducting, conducting, or an insulating substrate. The upper surface of the substrate 114 has a lattice parameter that matches or nearly matches GaAs. Examples of the substrate 114 are described below with reference to FIG. 16. The dilute nitride layer 106 is an intrinsic layer in the p-i-n diode and serves as an absorption medium. The terms absorber layer and absorption medium can be used to describe any layer that absorbs photons.

**[0033]** The dilute nitride layer 106 has a lattice parameter that is compatible with the III-V layers 102 and 112. The dilute nitride layer 106 can be lattice-matched to the III-V layers 102 and 112, or it may have a lattice parameter that is relatively close (nearly matched) to the III-V layers 102 and 112. Thus, the dilute nitride layer 106 has a sufficiently low defect level such that it has good optical performance. Such a sufficiently low defect level can include a comparable or lower defect level than would occur in an  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  layer grown on an InP substrate. Each of the layers 102, 106, and 112 and the substrate 114 can include one or more layers that improve lattice-matching, interface quality, electron transport, hole transport and/or other optoelectronic properties.

**[0034]** FIG. 2 depicts a semiconductor 200 with a p-i-n diode and a multiplication layer. The semiconductor 200 is similar to the semiconductor 100, but also includes a multiplication layer to amplify the photocurrent generated by the intrinsic layer of the p-i-n diode. The structure of the semiconductor 200 can be described as an avalanche photodiode (APD) structure. In an APD, the addition of the multiplication layer results in an additional p-i-n or p-n junction. This allows a higher reverse bias to be applied, resulting in carrier multiplication via the avalanche process. As a result the gain (number of electrons per photon) of the device (as compared to a standard p-i-n) is increased. This results in a higher sensitivity device. The semiconductor 200 includes a substrate 214, an  $n^+$  III-V layer 212 epitaxially formed over the substrate 214, a p-type multiplication layer 208 formed over the  $n^+$  III-V layer 212, an intrinsic dilute nitride layer 206 epitaxially formed over the p-type multiplication layer 208, and a  $p^+$  III-V layer 202 epitaxially formed over the dilute nitride layer 206.

**[0035]** The III-V layers 202 and 212 can include any III-V material, such as GaAs, InGaAs, AlGaAs, InGaP, InGaAsP, InGaAsN, InGaNaSb, or another III-V material. The substrate 214 can be a semiconducting, conducting, or an insulating substrate. The upper surface of the substrate 214 has a lattice parameter that matches or nearly matches GaAs. Examples of the substrate 214 are described below with reference to FIG. 16. The dilute nitride layer 206 is an intrinsic layer in the p-i-n diode and serves as an optical absorber layer.

**[0036]** The dilute nitride layer 206 has a lattice parameter that is compatible with the III-V layers 202 and 212. The dilute nitride layer 206 can be lattice-matched to the III-V layers 202 and 212, or it may have a lattice parameter that is relatively close (nearly matched) to the III-V layers 202 and 212. Thus, the dilute nitride layer 206 has a sufficiently low defect level such that

it has good optical performance. Such a sufficiently low defect level can include a comparable or lower defect level than would occur in an  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  layer grown on an InP substrate. Each of the layers 202, 206, and 212 and the substrate 214 can include one or more layers that improve lattice-matching, interface quality, electron transport, hole transport and/or other optoelectronic properties.

**[0037]** The multiplication layer 208 can be a p-type III-V layer that amplifies the current generated by the dilute nitride layer 206 through avalanche multiplication. Thus, for each free carrier (electron or hole) generated by the dilute nitride layer 206, the multiplication layer 208 generates one or more carriers via the avalanche effect. Thus, the multiplication layer 208 increases the total current generated by the semiconductor 200.

**[0038]** FIG. 3 depicts a semiconductor 300 with a GaAs-based p-i-n diode. The semiconductor 300 includes a substrate 314 with a top surface having a lattice parameter matching or nearly matching that of GaAs. The substrate 300 includes an n-type GaAs layer 312 epitaxially formed over the substrate 314, and an n-type GaAs layer 310 epitaxially formed over the GaAs layer 312. The GaAs layer 312 can be more heavily doped than the GaAs layer 310. The semiconductor 300 also includes an intrinsic InGaNaSb layer 306 epitaxially formed over the GaAs layer 310, a p-type InGaNaSb layer 304 epitaxially formed over the intrinsic InGaNaSb layer 306, and a p-type GaAs layer 302 epitaxially formed over the p-type InGaNaSb layer 304. The p-type GaAs layer 302 can be more heavily doped than the p-type InGaNaSb layer 304. The InGaNaSb layer 304 and the InGaNaSb layer 306 can each have the composition  $\text{In}_x\text{Ga}_{1-x}\text{N}_y\text{As}_{1-y-z}\text{Sb}_z$  ( $0 \leq x \leq 1$ ;  $0 \leq y \leq 1$ ;  $0 \leq z \leq 1$ ). The mole fractions x, y, and z can have different values in the different layers 302 and 304. In some examples, x ranges from 0 to 0.55, y ranges from 0 to 0.1, and z ranges from 0 to 0.1.

**[0039]** In some examples, the p-type GaAs layer 302 can have a thickness of approximately  $0.2 \mu\text{m}$  and can be doped with Be or C to result in a free hole concentration of approximately  $1.5 \times 10^{19} \text{ cm}^{-3}$ . The p-type InGaNaSb layer 304 can have a thickness of approximately  $0.25 \mu\text{m}$  and can be doped with Be or C to result in a free hole concentration of approximately  $7 \times 10^{18} \text{ cm}^{-3}$ . The composition of the InGaNaSb layer 304 can be selected to result in a bandgap of approximately 0.8 eV. The InGaNaSb layer 306 can have a thickness of approximately  $3 \mu\text{m}$  and can be unintentionally doped (UID) with a free carrier concentration of approximately  $6 \times 10^{14} \text{ cm}^{-3}$ . The carrier concentration of a material is the number density of

charge carriers such as electrons or holes in the material. The carrier concentration of a material is sometimes expressed in units of electrons- $\text{cm}^{-3}$ , holes- $\text{cm}^{-3}$ , or atoms- $\text{cm}^{-3}$  (referring to the atomic dopant density), but more often, the name of the particle is omitted while referencing the same quantity and the carrier concentration is simply expressed in units of  $\text{cm}^{-3}$ . UID semiconductors do not have dopants that were intentionally added, but can include a nonzero concentration of impurities that act as dopants. The InGaNaSb layer 306 can act as an absorber layer to absorb incident photons. The InGaNaSb layer 306 can have primarily holes as the free carriers, making the layer 306 p-type. The composition of the InGaNaSb layer 306 can also be selected to result in a bandgap of approximately 0.8 eV. The InGaNaSb layer 306 can have a bandgap between approximately 0.8 eV and approximately 0.95 eV, corresponding to wavelengths between 1.3  $\mu\text{m}$  and 1.55  $\mu\text{m}$ .

**[0040]** With the appropriate concentration of In, InGaAs alloys can have bandgaps within the wavelength range 1.3 – 1.55  $\mu\text{m}$ . However, the lattice parameters of such InGaAs alloys are similar to that of InP, but not that of GaAs or Si. Thus, InGaAs absorbers are not readily compatible with epitaxial growth on GaAs or silicon substrates. However, the addition of N to InGaAs can reduce the bandgap while resulting in a lattice parameter that matches or nearly matches GaAs. Addition of Sb to InGaNaSb results in improved crystallinity and lower background carrier concentration for a given bandgap. Sb can mitigate some defect types or can act as a surfactant to enhance device performance. Sb can improve the incorporation of N, allowing a lower N flux or flow to be used to grow a material of a given N concentration and correspondingly bandgap, thus reducing the background carrier concentration. Accordingly, the bandgap of InGaNaSb can be tailored to the appropriate range while maintaining good crystallinity and lattice matching to GaAs.

**[0041]** The GaAs layer 310 can have a thickness of approximately 0.5  $\mu\text{m}$  and can be doped with silicon to result in an n-type material with a free carrier concentration of approximately  $2 \times 10^{15} \text{ cm}^{-3}$ . The GaAs layer 312 can have a thickness of approximately 2.5  $\mu\text{m}$  and can be doped with silicon to result in an n-type material with a free carrier concentration of approximately  $5 \times 10^{18} \text{ cm}^{-3}$ . The substrate 314 can include one or more layers, and the top surface of the substrate can have a lattice parameter matching or nearly matching GaAs. This results in a high quality interface between the GaAs layer 312 and the substrate 314, and reduces defect levels in the semiconductor 300. Some examples of the substrate 314 are described below

with reference to FIG. 16. Accordingly, the semiconductor 300 includes a GaAs-based p-i-n diode that is optically active in the 1.3 – 1.55  $\mu\text{m}$  range and is formed on the top surface of a substrate with a lattice parameter matching or nearly matching that of GaAs.

**[0042]** FIG. 4 depicts a semiconductor 400 with a GaAs-based p-i-n diode and a multiplication layer. The semiconductor 400 is similar to the semiconductor 300, but also includes an avalanche multiplication layer to amplify the photocurrent generated by the intrinsic layer of the p-i-n diode. The semiconductor 400 includes a substrate 414 with a top surface having a lattice parameter matching or nearly matching that of GaAs. The substrate 400 includes an n-type GaAs layer 412 epitaxially formed over the substrate 414, and an n-type GaAs layer 410 epitaxially formed over the n-type GaAs layer 412. The GaAs layer 412 can be more heavily doped than the GaAs layer 410. The semiconductor 400 also includes a multiplication layer 408 epitaxially formed over the GaAs layer 410, an intrinsic InGaNaSb layer 406 epitaxially formed over the multiplication layer 408, a p-type InGaNaSb layer 404 epitaxially formed over the intrinsic InGaNaSb layer 406, and a p-type GaAs layer 402 epitaxially formed over the p-type InGaNaSb layer 404. The p-type GaAs layer 402 can be more heavily doped than the p-type InGaNaSb layer 404. The InGaNaSb layer 404 and the InGaNaSb layer 406 can each have the composition  $\text{In}_x\text{Ga}_{1-x}\text{N}_y\text{As}_{1-y-z}\text{Sb}_z$  ( $0 \leq x \leq 1$ ;  $0 \leq y \leq 1$ ;  $0 \leq z \leq 1$ ). The mole fractions  $x$ ,  $y$ , and  $z$  can have different values in the different layers 402 and 404. In some examples,  $x$  ranges approximately from 0 to 0.55, inclusive,  $y$  ranges approximately from 0 to 0.1, inclusive, and  $z$  ranges approximately from 0 to 0.1, inclusive.

**[0043]** In some examples, the p-type GaAs layer 402 can have a thickness of approximately 0.2  $\mu\text{m}$  and can be doped with Be or C to result in a free hole concentration of approximately  $1.5 \times 10^{19} \text{ cm}^{-3}$ . The p-type InGaNaSb layer 404 can have a thickness of approximately 0.25  $\mu\text{m}$  and can be doped with Be or C to result in a free hole concentration of approximately  $7 \times 10^{18} \text{ cm}^{-3}$ . The composition of the InGaNaSb layer 404 can be selected to result in a bandgap of approximately 0.8 eV. The InGaNaSb layer 406 can have a thickness of approximately 3  $\mu\text{m}$  and can be unintentionally doped (UID) with a free carrier concentration of approximately  $6 \times 10^{14} \text{ cm}^{-3}$ . The InGaNaSb layer 406 can act as an absorber layer to absorb incident photons. The InGaNaSb layer 406 can have primarily holes as the free carriers, making the layer 406 p-type. The composition of the InGaNaSb layer 406 can also be selected to result in a bandgap of approximately 0.8 eV. The InGaNaSb layer 406 can have a bandgap

between approximately 0.8 eV and approximately 0.95 eV, corresponding to wavelengths between 1.3  $\mu\text{m}$  and 1.55  $\mu\text{m}$ .

**[0044]** With the appropriate concentration of In, InGaAs alloys can have bandgaps within the wavelength range 1.3 – 1.55  $\mu\text{m}$ . However, the lattice parameters of such InGaAs alloys are similar to that of InP, but not that of GaAs or Si. Thus, InGaAs absorbers are not readily compatible with epitaxial growth on GaAs or silicon substrates. However, the addition of N to InGaAs can reduce the bandgap while resulting in a lattice parameter that matches or nearly matches GaAs. Addition of Sb to InGaAs results in improved crystallinity and lower background carrier concentration for a given bandgap. Sb can mitigate some defect types or can act as a surfactant to enhance device performance. Sb can improve the incorporation of N, allowing a lower N flux or flow to be used to grow a material of a given N concentration and correspondingly bandgap, thus reducing the background carrier concentration. Accordingly, the bandgap of InGaAsSb can be tailored to the appropriate range while maintaining good crystallinity and lattice matching to GaAs.

**[0045]** The GaAs layer 410 can have a thickness of approximately 0.5  $\mu\text{m}$  and can be doped with silicon to result in an n-type material with a free carrier concentration of approximately  $2 \times 10^{15} \text{ cm}^{-3}$ . The GaAs layer 412 can have a thickness of approximately 2.5  $\mu\text{m}$  and can be doped with silicon to result in an n-type material with a free carrier concentration of approximately  $5 \times 10^{18} \text{ cm}^{-3}$ . The substrate 414 can include one or more layers, and the top surface of the substrate can have a lattice parameter matching or nearly matching GaAs. This results in a high quality interface between the GaAs layer 412 and the substrate 414, and reduces defect levels in the semiconductor 400. Some examples of the substrate 414 are described below with reference to FIG. 16. Accordingly, the semiconductor 400 includes a GaAs-based p-i-n diode that is optically active in the 1.3 – 1.55  $\mu\text{m}$  range and is formed on the top surface of a substrate with a lattice parameter matching or nearly matching that of GaAs.

**[0046]** The multiplication layer 408 can be a p-type III-V layer that amplifies the current generated by the dilute nitride layer 406 through avalanche multiplication. One example of a p-type III-V layer is a p-type GaAs layer. For each free carrier (electron or hole) generated by the dilute nitride layer 406, the multiplication layer 408 generates one or more carriers via the avalanche effect. Thus, the multiplication layer 408 increases the total current generated by the semiconductor 400.

**[0047]** In some examples, the bandgap of one or more of the layers 106, 206, 304, 306, 404, and 406 is between 0.7 eV and 0.95 eV. In some examples, the bandgap of one or more of the layers 106, 206, 304, 306, 404, and 406 is 0.7 eV, 0.75 eV, 0.80 eV, 0.85 eV, 0.90 eV, or 0.95 eV. In some examples, one or more of the layers 106, 206, 304, 306, 404, and 406 is up to 10  $\mu\text{m}$  thick. In some examples, one or more of the layers 106, 206, 304, 306, 404, and 406 is 0.001-1, 0.05-5, 0.5-5, 0.1-1, 1-10, 0.001-0.005, 0.005-0.01, 0.01-0.05, 0.05-0.1, 0.1-0.5, 0.5-1, 1-2, 2-3, 3-4, 4-5, 5-6, 6-7, 7-8, 8-9, 9-10, 2-10, 3-10, or 3-5  $\mu\text{m}$  (micrometers) thick. The layers 106, 206, 306, and 406 have a free carrier concentration caused by unintentional dopants. The carrier concentration at room temperature of one or more of the layers 106, 206, 306, and 406 can be below approximately  $1 \times 10^{16} \text{ cm}^{-3}$ , can be below approximately  $5 \times 10^{15} \text{ cm}^{-3}$ , can be below approximately  $1 \times 10^{15} \text{ cm}^{-3}$ , and can be between approximately  $1 \times 10^{13} \text{ cm}^{-3}$  and  $5 \times 10^{15} \text{ cm}^{-3}$ . Room temperature can include a range of temperatures that the layers 106, 206, 306, and 406 will experience during normal operation, such as approximately 20 °C, between 15 °C and 25 °C, between 0 °C and 30 °C, and between -20 °C and 50 °C. Because the layers 106, 206, 306, and 406 are unintentionally doped, carrier freeze-out will occur at higher temperatures than for semiconductors with higher doping levels. Because of this freeze-out effect, a sample measured at a reduced or cryogenic temperature will exhibit a lower carrier concentration than the same sample measured at room temperature. Thus, measuring carrier concentrations at room temperature provides an accurate indication of carrier concentrations to be expected during device operation, as opposed to measuring carrier concentrations at reduced or cryogenic temperatures.

**[0048]** One or more of the layers 106, 206, 304, 306, 404, and 406 can have In molar concentrations between approximately 10% and approximately 20%, N molar concentrations between approximately 3% and approximately 7%, and Sb molar concentrations between approximately 0.5% and approximately 5%.

**[0049]** FIG. 5 depicts a graph 500 that shows the characterization of the semiconductor 300 by x-ray diffraction (XRD). The graph 500 includes a scan 502 which has peaks 504, 506, 508, and 510. Each peak corresponds to a material of distinct lattice parameter. The peak 504 corresponds to the intrinsic InGaAsSb layer 306, and peak 506 corresponds to the p-type InGaAsSb layer 304. The p-type dopant adds tensile strain to the layer 304 and thus shifts the peak 506 away from the peak 504 by approximately 26 arc-seconds. Peak 508 may correspond

to GaAsSb forming at the interface between the p-type GaAs layer 302 and the p-type InGaNaSb layer 304. The peak 510 corresponds to the substrate 314. The narrowness of the peaks 504, 506, 508, and 510 indicates that the epitaxial layers 302, 304, 306, 310, and 312 have high crystallinity and low defect levels.

**[0050]** FIG. 6 depicts a graph 600 that shows XRD scans of intrinsic InGaNaSb layers of different thicknesses epitaxially formed on GaAs. The layers were grown using molecular beam epitaxy (MBE) at a growth temperature of 440 °C and a Group V element to Group III element ratio (V/III) of 42:1. These layers are coherently strained (non-relaxed) with a bandgap as low as 0.78 eV. The graph 600 includes a scan 602 of a 4 μm layer of InGaNaSb and a scan 604 of a 0.5 μm layer of InGaNaSb. The scan 602 has two peaks, 606 and 608, indicating the presence of two different lattice parameters. The peak 608 corresponds to the GaAs substrate, and the peak 606 corresponds to the 4 μm layer of InGaNaSb. The peak 606 is shifted by -114 arcsec from the peak 608, indicating that the 4 μm layer of InGaNaSb layer is slightly compressive as compared to GaAs. In contrast, the scan 604 only has one peak 610, indicating the presence of only one lattice parameter. The XRD peaks from the 0.5 μm layer of InGaNaSb and the GaAs substrate overlap, indicating that the InGaNaSb layer and the GaAs substrate are lattice matched or nearly matched. Furthermore, the narrowness of the peaks 606, 608, and 610 indicates that the InGaNaSb layers have high crystallinity and low defect levels.

**[0051]** FIG. 7 depicts a graph 700 that shows XRD scans of InGaNaSb layers grown on p-type and semi-insulating GaAs substrates. The graph 700 includes a scan 702 of a 0.5 μm layer of InGaNaSb grown by MBE on a p-type GaAs substrate and a scan 704 of a 0.5 μm layer of InGaNaSb grown by MBE on a semi-insulating GaAs substrate.

**[0052]** Effective substrate temperature control can improve the quality of low-bandgap materials such as InGaNaSb when grown on semi-insulating substrates. As the temperature of a semiconducting substrate is increased, free carriers are thermally generated and its absorption edge shifts to a lower energy. This shift can be measured and used to calculate substrate temperature.

**[0053]** Epitaxial growth systems are often heated using radiant heaters that rely on substrate radiant absorption to raise the temperature of the substrate. Absorption is a function of both doping and bandgap; more absorption occurs as bandgap decreases and/or as doping increases. Layer absorption also scales with layer thickness. As such, growth of a sufficiently thick low-

bandgap material such as InGaNaSb on a semi-insulating higher-bandgap material such as a GaAs substrate can result in a situation in which the low-bandgap material dominates radiant absorption. Changes in thickness of this low-bandgap material can thereby significantly affect the substrate temperature.

**[0054]** If a constant heater power which would result in a constant equilibrium temperature for a semi-insulating substrate is maintained while growing a sufficiently thick low-bandgap material, the increase in substrate absorptivity increases the amount of heat absorbed at the constant heater power, resulting in an increase in substrate temperature. Thus, both open-loop temperature control and closed-loop temperature control that is based on indirect measurements of the substrate temperature can be inaccurate when growing sufficiently thick low-bandgap materials on semi-insulating substrates. These effects are not as pronounced when growing low-bandgap materials on more conductive substrates, because doped substrate absorptivities are higher than those for semi-insulating substrates and tend to dominate radiant absorption.

**[0055]** The layer grown on a p-type substrate (scan 702) was grown with closed-loop temperature control that simply regulated the temperature of the substrate holder using a thermocouple positioned to be sensitive to the temperature of the substrate backside (opposite the epitaxial layer growth surface). However, the layer grown on a semi-insulating substrate (scan 704) was grown with modified closed-loop control. A feedback loop regulated the temperature of the substrate holder using the thermocouple and a first closed-loop control algorithm, but the temperature setpoint of the first closed-loop control algorithm was adjusted by a second closed-loop control algorithm. The second closed-loop control algorithm measured the substrate temperature using the temperature dependence of the substrate's optical absorption edge, and then adjusted the temperature setpoint of the first closed-loop control algorithm to maintain a constant substrate temperature. In this way, the modified closed-loop control algorithm maintained a constant substrate temperature despite changes in the absorptivity of the substrate.

**[0056]** The scan 702 includes a peak 710, and the scan 704 includes peaks 706 and 708. The peaks 706 and 710 are aligned, indicating that temperature was held constant with effective closed-loop control during the growth of the low-bandgap InGaNaSb material. The peak 708 is a secondary peak on the scan 704, and is due to changes in composition resulting from temperature variations during initial growth of the InGaNaSb layer. However, the scans 702

and 704 are well-matched, indicating that with effective temperature control, high-quality InGaNaSb can be grown on a semi-insulating GaAs substrate.

**[0057]** FIG. 8 depicts a graph 800 showing the effect of the In/Sb ratio on carrier properties of InGaNaSb, as measured by the Hall effect. The graph 800 includes a carrier concentration curve 802 and a carrier mobility curve 804. Decreasing In/Sb ratio during deposition below about 6 results in higher carrier concentration, as shown by the curve 802. Increasing the In/Sb ratio during deposition above about 6 does not significantly affect the carrier concentration, also shown by the curve 802. However, hole mobility, as measured by the Hall effect, increases consistently as the In/Sb ratio increases during deposition from 2 to 14, as shown by the curve 804.

**[0058]** FIG. 9 depicts a graph 900 showing the effect of the In/Sb ratio on optical properties of InGaNaSb, as measured by photoluminescence (PL). The graph 900 includes a bandgap curve 902 and a PL intensity curve 904. The bandgap varies between approximately 0.811 eV and 0.803 eV as the In/Sb ratio varies between 2 and 14, with a minimum bandgap at an In/Sb ratio of 10. The PL intensity varies non-monotonically as the In/Sb ratio varies between 2 and 14, with a minimum at an In/Sb ratio of 2 and a maximum at an In/Sb ratio of 6. A higher PL intensity indicates a higher quality InGaNaSb layer.

**[0059]** Lower In/Sb ratios result in lower bandgaps, which can be desirable for certain applications. However, decreasing the In/Sb ratio below about 6 can result in increases in background carrier concentration, which can result in increased dark current. When the InGaNaSb material is used in p-i-n diodes as a photodetector, higher dark current can increase the background noise level, thus reducing the signal-to-noise level. Accordingly, it is desirable to decrease the bandgap while maintaining low background carrier concentrations.

**[0060]** FIG. 10 depicts a graph 1000 that shows the effect of growth temperature and As flux on the carrier concentration of InGaNaSb, as measured by the Hall effect. The graph 1000 includes curves 1002, 1004, and 1006, showing the effect of 25% increases and 25% decreases in As flux on carrier concentration at growth temperatures (i.e., substrate temperatures during growth) of 420 °C, 440 °C, and 460 °C, respectively. Higher growth temperatures result in lower background carrier concentrations. In this study, a growth temperature of 460 °C resulted in a background carrier concentration of approximately  $4 \times 10^{15} \text{ cm}^{-3}$ , as shown by the curve 1006. The As flux has a smaller impact on the background carrier concentration, but in general,

a lower As flux results in a lower background carrier concentration, as shown by the curves 1004 and 1006.

**[0061]** FIG. 11 depicts a graph 1100 that shows the effect of growth temperature and arsenic flux on the bandgap of InGaNaSb, as measured by photoluminescence. The graph 1100 includes curves 1102, 1104, and 1106, showing the effect of 25% increases and 25% decreases in As flux on bandgap at growth temperatures of 420 °C, 440 °C, and 460 °C, respectively. The bandgap of InGaNaSb exhibits only a weak dependence on growth temperature between 420 °C and 460 °C, ranging from a low of 0.79 eV to a high of 0.82 eV. The bandgap of InGaNaSb also exhibits a weak dependence on As flux, with an As flux of 1 (nominal value) generally resulting in the highest bandgap within the range of fluxes in this study.

**[0062]** FIG. 12 depicts a graph 1200 showing the effect of rapid thermal annealing (RTA) on the carrier concentration of InGaNaSb, as measured by the Hall effect. The graph 1200 includes curves 1202 and 1206 corresponding to an RTA temperature of 780 °C, curve 1208 corresponding to an RTA temperature of 800 °C, and curves 1210 and 1212 corresponding to an RTA temperature of 820 °C. In general, short anneals of InGaNaSb at lower temperatures result in lower background carrier concentrations, within the RTA parameters examined in the study. For a given RTA temperature, a shorter RTA duration resulted in a lower carrier concentration, as shown by curves 1202, 1206, 1210, and 1212. For a given RTA duration, a lower RTA temperature resulted in a lower carrier concentration, as shown by curves 1202, 1206, 1210, and 1212. The reduction in carrier concentration with RTA temperature is especially significant. Decreasing the RTA temperature from 820 °C to 780 °C reduces the carrier concentration from  $3 \times 10^{16} \text{ cm}^{-3}$  (curve 1212) to  $7 \times 10^{14} \text{ cm}^{-3}$  (curve 1202), a decrease of more than an order of magnitude.

**[0063]** FIG. 13 includes a graph 1300 showing the effect of RTA on the bandgap of InGaNaSb as measured by photoluminescence. The graph 1300 includes curves 1302 and 1306 corresponding to an RTA temperature of 780 °C, curve 1308 corresponding to an RTA temperature of 800 °C, and curves 1310 and 1312 corresponding to an RTA temperature of 820 °C. The effects of RTA on bandgap are similar to the effects on carrier concentration. For a given RTA temperature, a shorter RTA duration resulted in a lower bandgap, as shown by curves 1302, 1306, 1310, and 1312. For a given RTA duration, a lower RTA temperature resulted in a lower bandgap, as shown by curves 1302, 1306, 1310, and 1312. Decreasing the RTA

temperature from 820 °C to 780 °C reduces the bandgap from approximately 0.81 eV (curve 1312) to approximately 0.797 eV (curve 1302).

**[0064]** FIG. 14 depicts a graph 1400 that shows a photoluminescence spectrum of a 0.5  $\mu\text{m}$  layer of InGaNaSb grown on a GaAs substrate. The graph 1400 includes a scan 1402 that was measured on a 0.5  $\mu\text{m}$  layer of InGaNaSb grown on a GaAs substrate. The scan 1402 includes a peak 1404 at a wavelength of 1.5429  $\mu\text{m}$ , corresponding to an energy of 0.8036 eV. The scan 1402 includes a full width at half maximum 1406 of 121.3 nm, a narrow width that indicates good material quality.

**[0065]** FIG. 15 includes a colormap 1500 that shows cross-wafer variation in bandgap of a 0.5  $\mu\text{m}$  layer of InGaNaSb grown on a 150 mm GaAs substrate. The bandgap of the layer ranges between a minimum value of 0.799 eV at a center location 1502 and a maximum value of 0.813 eV at an edge location 1504. The average bandgap is 0.806 eV, and the standard deviation is 0.408%, or approximately 0.003 eV. These variations can be due to variations in precursor flow, substrate temperature, and/or other factors. However, the variations are relatively small and illustrate that the uniformity is good.

**[0066]** FIG. 16 illustrates several examples of p-i-n diodes formed over substrates with lattice parameters matching or nearly matching GaAs. FIG. 16 depicts semiconductors 1600, 1630, and 1660. The semiconductor 1600 includes a p-i-n diode 1602 epitaxially formed over a GaAs substrate 1606. The GaAs substrate 1606 thus provides an ideal substrate for homoepitaxy of a Ga-As-based p-i-n structure such as the p-i-n diode 1602. The substrate 1606 can include any of the substrates 114, 214, 314, and 414. The p-i-n diode 1602 can include any of the p-i-n diode comprising the layers 102, 106, and 112; the p-i-n diode comprising the layers 202, 206, 208, and 212; the p-i-n diode comprising the layers 302, 304, 306, 310, and 312; and the p-i-n diode comprising the layers 402, 404, 406, 408, 410, and 412.

**[0067]** The semiconductors 1630 and 1660 each include a lattice engineered layer over a silicon substrate. Each lattice engineered layer has a first surface nearest the silicon substrate and a second (top-most) surface opposite the silicon substrate. The first surface nearest the silicon substrate has a lattice parameter that is matched or nearly matched to that of Si. This results in a low number of defects and/or dislocations in the lattice engineered layer. The semiconductors 1630 and 1660 can include one or more layers (not shown) between the lattice engineered layer and the silicon substrate. The second surface opposite the silicon substrate has

a lattice parameter that is matched or nearly matched to that of GaAs. This results in a low number of defects and/or dislocations when epitaxially growing p-i-n layers and/or dilute nitride layers that have lattice constants that are matched or nearly matched to that of GaAs. A low number of defects can include comparable or fewer defects than would occur in an  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  layer grown on an InP substrate.

**[0068]** The semiconductor 1630 includes a graded  $\text{Si}_x\text{Ge}_{1-x}$  ( $0 \leq x \leq 1$ ) layer 1634 formed over a Si substrate 1635. The graded  $\text{Si}_x\text{Ge}_{1-x}$  layer 1634 is a lattice engineered layer. The semiconductor 1630 also includes a p-i-n diode 1632 epitaxially formed over the graded  $\text{Si}_x\text{Ge}_{1-x}$  layer 1634. The Si fraction  $x$  of the graded  $\text{Si}_x\text{Ge}_{1-x}$  layer 1634 varies from 0 to 1 through its thickness. At the interface with the Si substrate 1635,  $x = 1$  and the graded  $\text{Si}_x\text{Ge}_{1-x}$  layer 1634 substantially only contains Si. At the interface with the p-i-n diode 1632,  $x = 0$  and the graded  $\text{Si}_x\text{Ge}_{1-x}$  layer 1634 substantially only contains Ge. Thus, the graded  $\text{Si}_x\text{Ge}_{1-x}$  layer 1634 provides a transition in lattice parameter from that of the Si substrate (5.43 Å) to that of Ge (5.66 Å), which nearly matches to that of GaAs (5.65 Å). The lattice constants of Ge and GaAs are matched well enough that high-quality GaAs can be epitaxially grown on a Ge surface. Thus, the graded  $\text{Si}_x\text{Ge}_{1-x}$  layer 1634 allows growth of GaAs layers on Si substrates. Together, the graded  $\text{Si}_x\text{Ge}_{1-x}$  layer 1634 and the silicon substrate 1635 comprise a substrate 1636 having a top surface with a lattice parameter nearly matching GaAs. The substrate 1636 can include any of the substrates 114, 214, 314, and 414. The p-i-n diode 1632 can include any of the p-i-n diode comprising the layers 102, 106, and 112; the p-i-n diode comprising the layers 202, 206, 208, and 212; the p-i-n diode comprising the layers 302, 304, 306, 310, and 312; and the p-i-n diode comprising the layers 402, 404, 406, 408, 410, and 412.

**[0069]** The semiconductor 1660 includes a rare earth (RE) containing layer 1664 epitaxially formed over a silicon substrate 1665. The RE containing layer 1664 is a lattice engineered layer. Rare earth elements are a specific class of elements on the periodic table (Sc, Y, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu). The RE containing layer can contain one or more of the rare earth elements. The semiconductor 1660 also includes a p-i-n diode 1662 epitaxially formed over the RE containing layer 1664. Generically, the RE containing layer can be a rare earth oxide (REO), a rare earth silicide (RESi), or a pnictide (RE-V, where V represents a group V element from the periodic chart, namely N, P, As, Sb, or Bi) or any combination of REO, RESi, and/or pnictide. The composition of the RE containing layer can be selected to

result in a lattice parameter matching or nearly matching GaAs at its interface with the p-i-n diode 1662. For example, the layer at the interface could be  $\text{ErAs}_x\text{N}_{1-x}$ , where  $x$  is approximately 0.9, which is lattice matched or nearly matched to GaAs. The rare earth containing layer can be of constant composition or graded throughout its thickness. When graded, the layer can be engineered so that the portion nearest the Si is chemically and mechanically compatible with silicon. For example, gadolinium oxide could be employed at or near the interface between the silicon and rare earth containing layer due to its lattice match with silicon. Thus, the RE containing layer 1664 provides a template for epitaxial growth of the p-i-n diode 1662. Together, the RE containing layer 1664 and the silicon substrate 1665 comprise a substrate 1666 having a top surface with a lattice parameter matching or nearly matching GaAs.

**[0070]** The substrate 1666 can include any of the substrates 114, 214, 314, and 414. The p-i-n diode 1662 can include any of the p-i-n diode comprising the layers 102, 106, and 112; the p-i-n diode comprising the layers 202, 206, 208, and 212; the p-i-n diode comprising the layers 302, 304, 306, 310, and 312; and the p-i-n diode comprising the layers 402, 404, 406, 408, 410, and 412.

**[0071]** FIGS. 1-4 depict p-i-n structures with an n-type layer over a substrate, an optional multiplication layer over the n-type layer, an intrinsic absorber layer over the n-type layer or the optional multiplication layer, and a p-type layer over the intrinsic absorber layer. In some examples, however, the order of the layers may be different. For example, the p-type layer may be over the substrate, the intrinsic absorber layer may be over the p-type layer, and the n-type layer may be over the intrinsic absorber layer. In addition, a multiplication layer may optionally be included, either between either the p-type layer and the intrinsic absorber layer or between the intrinsic absorber layer and the n-type layer. The substrates depicted in FIGS. 1-4 and 16 may be n-type, p-type, highly doped, unintentionally doped, insulating, conducting, or a combination of these.

**[0072]** The layers of the semiconductors 100, 200, 300, 400, 1600, 1700, and 1800 can be epitaxially formed with semiconductor processing techniques such as molecular beam epitaxy (MBE), metalorganic chemical vapor deposition (MOCVD), halide vapor phase epitaxy (HVPE), physical vapor deposition (PVD), and/or sputtering. All of the layers of a semiconductor can be formed in a single chamber, or different layers of a semiconductor can be formed in different chambers. For example, epitaxial layers of the substrates 114, 214, 314, 414 1606, 1636, and

1666 can be formed in a different chamber than epitaxial layers of the corresponding p-i-n diodes. The semiconductors 100, 200, 300, 400, 1600, 1700, and 1800 are then laterally patterned using photolithography, etching, and metal deposition techniques to produce detectors.

**[0073]** From the above description of the method it is manifest that various techniques may be used for implementing the concepts of the method without departing from its scope. The described embodiments are to be considered in all respects as illustrative and not restrictive. It should also be understood that the method is not limited to the particular examples described herein, but can be implemented in other examples without departing from the scope of the claims. A first layer described and/or depicted herein as over a second layer can be immediately adjacent to the second layer, or one or more intermediate layers can be between the first and second layers. Similarly, while operations are depicted in the drawings in a particular order, this should not be understood as requiring that such operations be performed in the particular order shown or in sequential order, or that all illustrated operations be performed, to achieve desirable results.

Claims

What is claimed is:

1. A semiconductor, comprising:
  - a substrate with a lattice parameter matching or nearly matching GaAs;
  - a first doped III-V layer over the substrate;
  - an absorber layer over the first doped III-V layer, the absorber layer having:
    - a bandgap between approximately 0.7 eV and 0.95 eV, and
    - a carrier concentration less than approximately  $1 \times 10^{16} \text{ cm}^{-3}$  at room temperature;
  - and
  - a second doped III-V layer over the absorber layer.
2. The semiconductor of claim 1, wherein the absorber layer comprises a dilute nitride.
3. The semiconductor of claim 2, wherein the dilute nitride comprises  $\text{In}_x\text{Ga}_{1-x}\text{N}_y\text{As}_{1-y-z}\text{Sb}_z$  ( $0 \leq x \leq 1$ ;  $0 \leq y \leq 1$ ;  $0 \leq z \leq 1$ ).
4. The semiconductor of claim 2, wherein the dilute nitride comprises  $\text{In}_x\text{Ga}_{1-x}\text{N}_y\text{As}_{1-y-z}\text{Sb}_z$  ( $0 \leq x \leq 0.55$ ;  $0 \leq y \leq 0.1$ ;  $0 \leq z \leq 0.1$ ).
5. The semiconductor of claim 1, wherein the carrier concentration of the absorber layer is less than approximately  $5 \times 10^{15} \text{ cm}^{-3}$ .
6. The semiconductor of claim 1, wherein the carrier concentration of the absorber layer is less than approximately  $1 \times 10^{15} \text{ cm}^{-3}$ .
7. The semiconductor of claim 1, wherein a thickness of the absorber layer is between approximately 2 micrometers and approximately 10 micrometers.
8. The semiconductor of claim 1, wherein a thickness of the absorber layer is between approximately 3 micrometers and approximately 5 micrometers.

9. The semiconductor of claim 1, further comprising a multiplication layer between the absorber layer and one of the first and second doped III-V layers.
10. The semiconductor of claim 1, wherein the substrate comprises GaAs.
11. The semiconductor of claim 1, wherein the substrate comprises:  
a silicon substrate; and  
a lattice engineered layer over the silicon substrate, the surface of the lattice engineered layer opposite the silicon substrate having a lattice parameter that is matched or nearly matched to GaAs.
12. The semiconductor of claim 11, wherein the lattice engineered layer comprises a  $\text{Si}_x\text{Ge}_{1-x}$  layer, with x graded from 1 at a surface of the  $\text{Si}_x\text{Ge}_{1-x}$  layer nearest the silicon substrate to 0 at a surface of the  $\text{Si}_x\text{Ge}_{1-x}$  layer opposite the silicon substrate.
13. The semiconductor of claim 11, wherein the lattice engineered layer comprises a rare earth containing layer, the rare earth containing layer comprising one or more of Sc, Y, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, and/or Lu.
14. The semiconductor of claim 1, wherein the first doped III-V layer is n-type and the second doped III-V layer is p-type.
15. The semiconductor of claim 1, wherein the first doped III-V layer is p-type and the second doped III-V layer is n-type.
16. A method of forming a semiconductor, comprising:  
forming a first doped III-V layer over a substrate with a lattice parameter matching or nearly matching GaAs;  
forming an absorber layer over the first doped III-V layer, the absorber layer having:  
a bandgap between approximately 0.7 eV and 0.95 eV, and

a carrier concentration less than approximately  $1 \times 10^{16} \text{ cm}^{-3}$  at room temperature;  
and  
forming a second doped III-V layer over the absorber layer.

17. The semiconductor of claim 16, wherein the absorber layer comprises a dilute nitride.
18. The method of claim 17, wherein the dilute nitride comprises  $\text{In}_x\text{Ga}_{1-x}\text{N}_y\text{As}_{1-y-z}\text{Sb}_z$  ( $0 \leq x \leq 1$ ;  $0 \leq y \leq 1$ ;  $0 \leq z \leq 1$ ).
19. The method of claim 17, wherein the dilute nitride comprises  $\text{In}_x\text{Ga}_{1-x}\text{N}_y\text{As}_{1-y-z}\text{Sb}_z$  ( $0 \leq x \leq 0.55$ ;  $0 \leq y \leq 0.1$ ;  $0 \leq z \leq 0.1$ ).
20. The method of claim 16, wherein the carrier concentration of the absorber layer is less than approximately  $5 \times 10^{15} \text{ cm}^{-3}$ .
21. The method of claim 16, wherein the carrier concentration of the absorber layer is less than approximately  $1 \times 10^{15} \text{ cm}^{-3}$ .
22. The method of claim 16, wherein a thickness of the absorber layer is between approximately 2 micrometers and approximately 10 micrometers.
23. The method of claim 16, wherein a thickness of the absorber layer is between approximately 3 micrometers and approximately 5 micrometers.
24. The method of claim 16, further comprising forming a multiplication layer between the absorber layer and one of the first and second doped III-V layers.
25. The method of claim 16, wherein the substrate comprises GaAs.
26. The method of claim 16, wherein the substrate comprises:  
a silicon substrate; and

a lattice engineered layer over the silicon substrate, the surface of the lattice engineered layer opposite the silicon substrate having a lattice parameter that is matched or nearly matched to GaAs.

27. The method of claim 26, wherein the lattice engineered layer comprises a  $\text{Si}_x\text{Ge}_{1-x}$  layer, with  $x$  graded from 1 at a surface of the  $\text{Si}_x\text{Ge}_{1-x}$  layer nearest the silicon substrate to 0 at a surface of the  $\text{Si}_x\text{Ge}_{1-x}$  layer opposite the silicon substrate.

28. The method of claim 26, wherein the lattice engineered layer comprises a rare earth containing layer, the rare earth containing layer comprising one or more of Sc, Y, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, and/or Lu.

29. The method of claim 16, wherein the first doped III-V layer is n-type and the second doped III-V layer is p-type.

30. The method of claim 16, wherein the first doped III-V layer is p-type and the second doped III-V layer is n-type.

Abstract

Optoelectronic detectors having one or more dilute nitride layers on substrates with lattice parameters matching or nearly matching GaAs are described herein. A semiconductor can include a substrate with a lattice parameter matching or nearly matching GaAs and a first doped III-V layer over the substrate. The semiconductor can also include an absorber layer over the first doped III-V layer, the absorber layer having a bandgap between approximately 0.7 eV and 0.95 eV and a carrier concentration less than approximately  $1 \times 10^{16} \text{ cm}^{-3}$  at room temperature. The semiconductor can also include a second doped III-V layer over the absorber layer.

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				Application Number	Not Yet Assigned
				Filing Date	Concurrently Herewith
				First Named Inventor	Robert Yanka
				Art Unit	N/A
				Examiner Name	Not Yet Assigned
				Attorney Docket Number	111848-0002-101
Sheet	1	of	3		

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				Filing Date	Concurrently Herewith
				First Named Inventor	Robert Yanka
				Art Unit	N/A
				Examiner Name	Not Yet Assigned
Sheet	2	of	3	Attorney Docket Number	111848-0002-101

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		Cheah et al., "GaAs-Based Heterojunction p-i-n Photodetectors Using Pentanary InGaAsNSb as the Intrinsic Layer," <i>IEEE Photonics Technology Letters</i> , Vol. 17, No. 9, September 2005, 3 pages.	
		Chen, et al., "GaAsSbN/GaAs long wavelength PIN detectors," <i>Indium Phosphide and Related Materials</i> , 2008. IPRM 2008. 20th International Conference on, Versailles, 2008, 4 pages.	
		Ferguson et al., "Optical Gain in GaInNAs and GaInNAsSb Quantum Wells," <i>IEEE Journal of Quantum Electronics</i> , Vol. 47, No. 6, June 2011, 8 pages.	
		Gobet et al., "GaInNAsSb/GaAs vertical cavity surface-emitting lasers (VCSELs): Current challenges and techniques to realize multiple-wavelength laser arrays at 1.55 $\mu\text{m}$ ," <i>Proc. of SPIE</i> , Vol. 6908, February 2008, 13 pages.	
		Harris et al., Development of GaInNAsSb alloys: Growth, band structure, optical properties and applications," <i>Phys. Stat. Sol. (b)</i> 244, No. 8, 2707-2729 (2007), 23 pages.	
		Harris, J. S. Jr., "The opportunities, successes and challenges for GaInNAsSb," <i>Journal of Crystal Growth</i> 278 (2005) 2 March 2005, 15 pages.	
		Jackrel et al., "Thick lattice-matched GaInNAs films in photodetector applications," <i>Proc. of SPIE</i> , Vol. 5726, (2005), 8 pages.	
		Khalil et al., "Photoconductivity and photoluminescence under bias in GaInNAs/GaAs MQW p-i-n structures," <i>Nanoscale Research Letter</i> , 7:539 (2012), 4 pages.	
		Ng et al., "Long wavelength bulk GaInNAs p-i-n photodiodes lattice matched to GaAs," <i>Journal of Applied Physics</i> 101, (2007), 6 pages.	
		Niu et al., "GaAs-based room-temperature continuous-wave 1.59 $\mu\text{m}$ GaInNAsSb single-quantum-well laser diode grown by molecular-beam epitaxy," <i>Applied Physics Letters</i> , 5 December 2005, Vol. 87 No. 23, 4 pages.	

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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  <i>(Use as many sheets as necessary)</i>				Application Number	Not Yet Assigned
				Filing Date	Concurrently Herewith
				First Named Inventor	Robert Yanka
				Art Unit	N/A
				Examiner Name	Not Yet Assigned
Sheet	3	of	3	Attorney Docket Number	111848-0002-101

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Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		Ohnaka et al., "A Low Dark Current InGaAs/InP p-i-n Photodiode with Covered Mesa Structure," <i>IEEE Transactions on Electron Devices</i> , Vol. Ed-34, No. 2, February 1987, 6 pages.	
		Ptak et al., "Effects of temperature, nitrogen ions, and antimony on wide depletion width GaInNAs," <i>Journal of Vacuum Science &amp; Technology B</i> , Second Series, Vol. 25, No. 3, May/June 2007, 6 pages.	
		Tan et al., "Dilute nitride GaInNAs and GaInNAsSb for solar cell applications," <i>Proc. of SPIE</i> , Vol. 8256 (2012), 10 pages.	
		Tan et al., "GaInNAsSb/GaAs Photodiodes for Long-Wavelength Applications," <i>IEEE Electron Device Letters</i> Vol. 32 No. 7, July 2011, 3 pages.	
		Tan et al., "Reduction of dark current and unintentional background doping in InGaAsN photodetectors by ex situ annealing," <i>Proc. of SPIE</i> , Vol. 7726, (2010), 8 pages.	
		Wistey et al., "Monolithic, GaInNAsSb VCSELs at 1.46 $\mu$ m on GaAs by MBE," <i>Electronics Letters</i> , 11 December 2003, Vol. 39, No. 25, 2 pages.	
		Yuen et al., "The role of antimony on properties of widely varying GaInNAsSb compositions," <i>Journal of Applied Physics</i> 99, (2006), 8 pages.	

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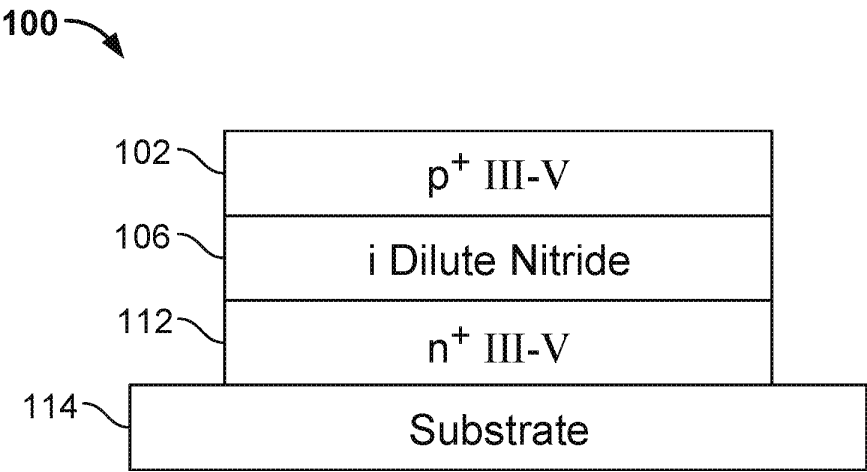


FIG. 1

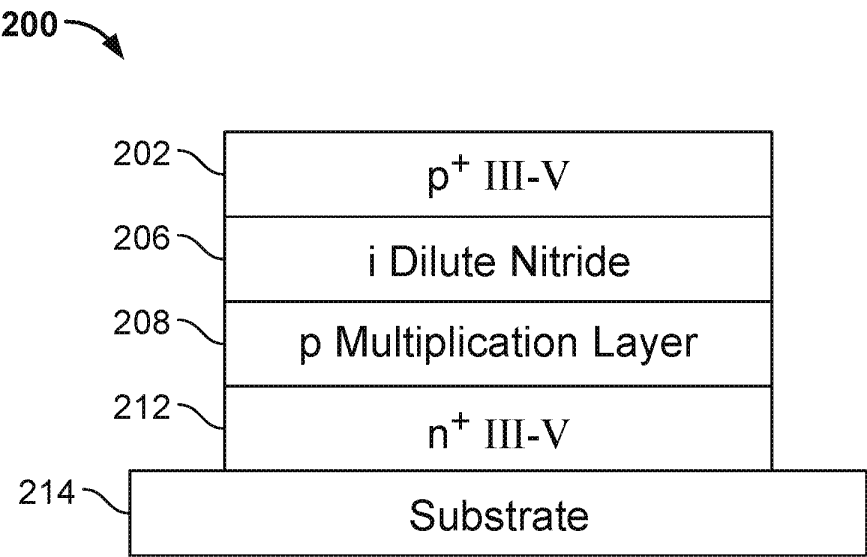


FIG. 2

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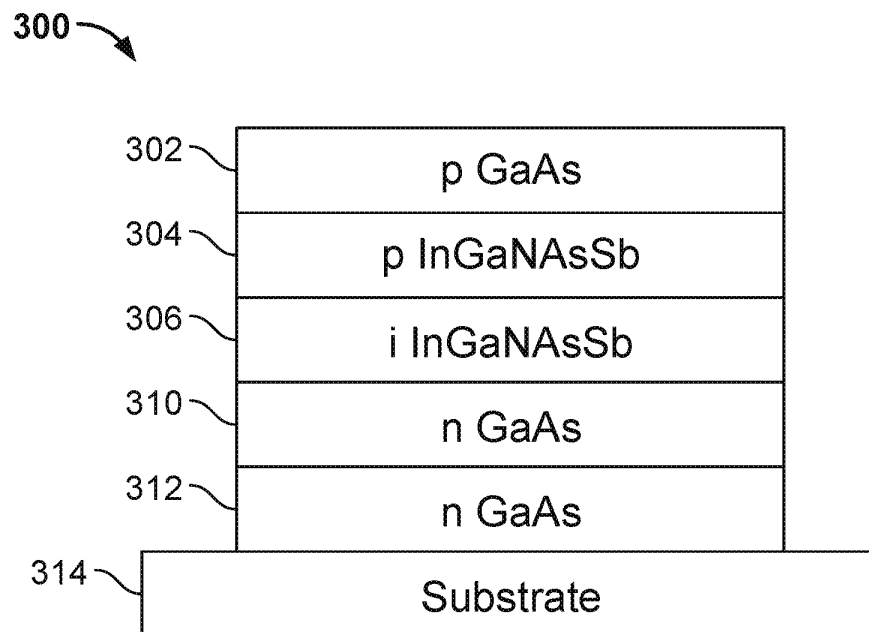


FIG. 3

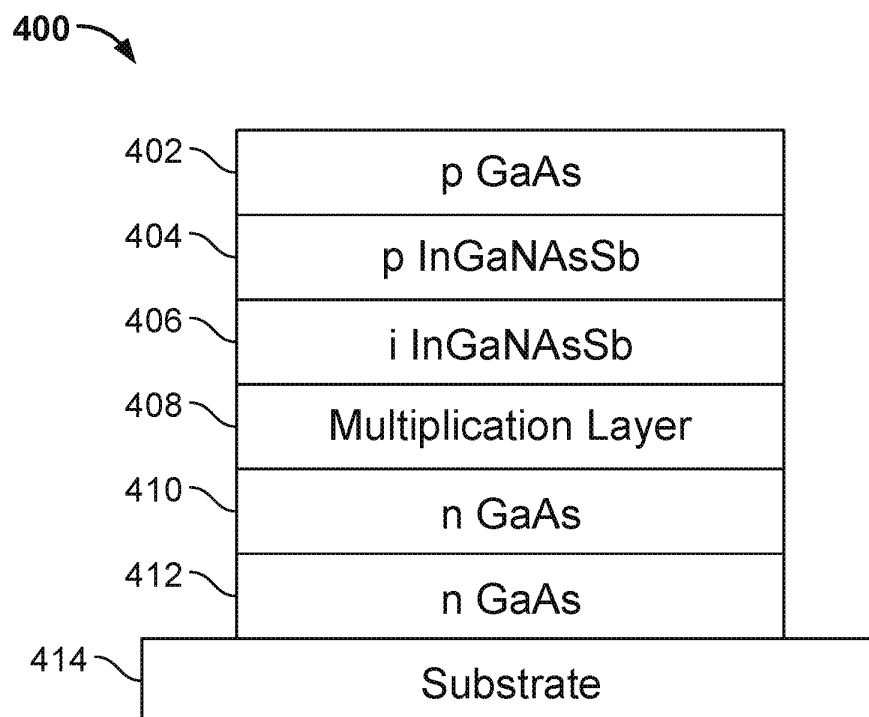


FIG. 4

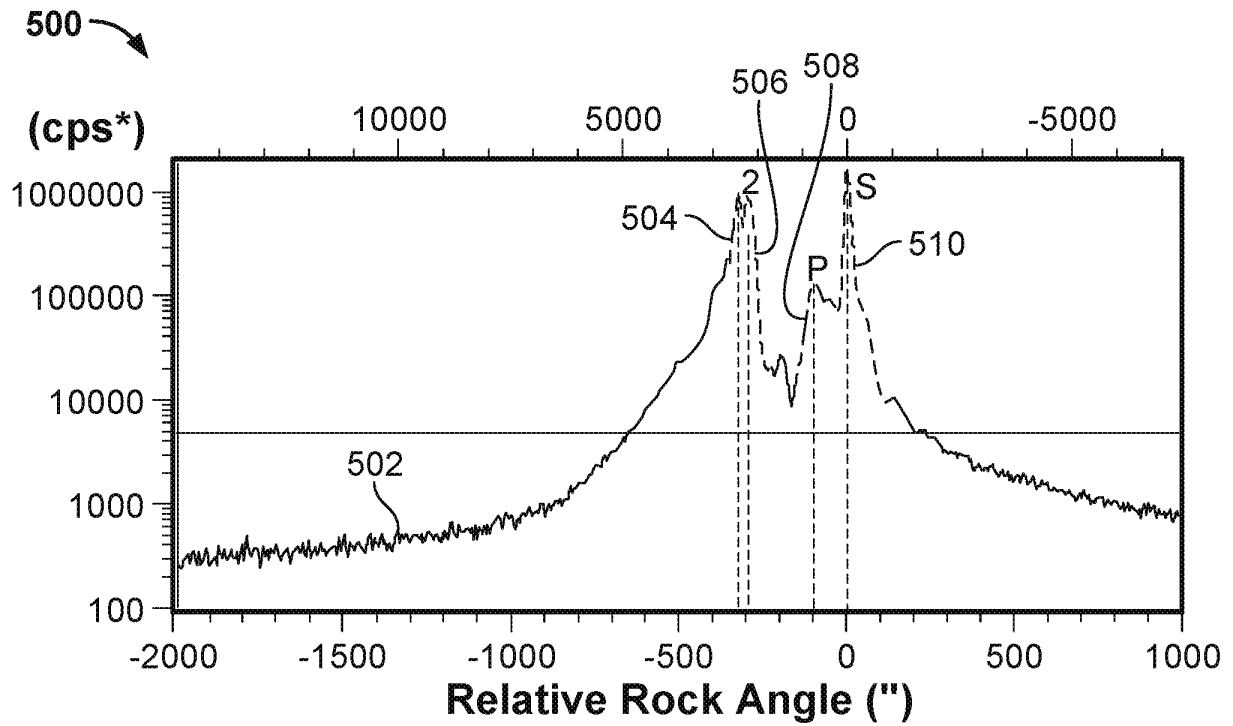


FIG. 5

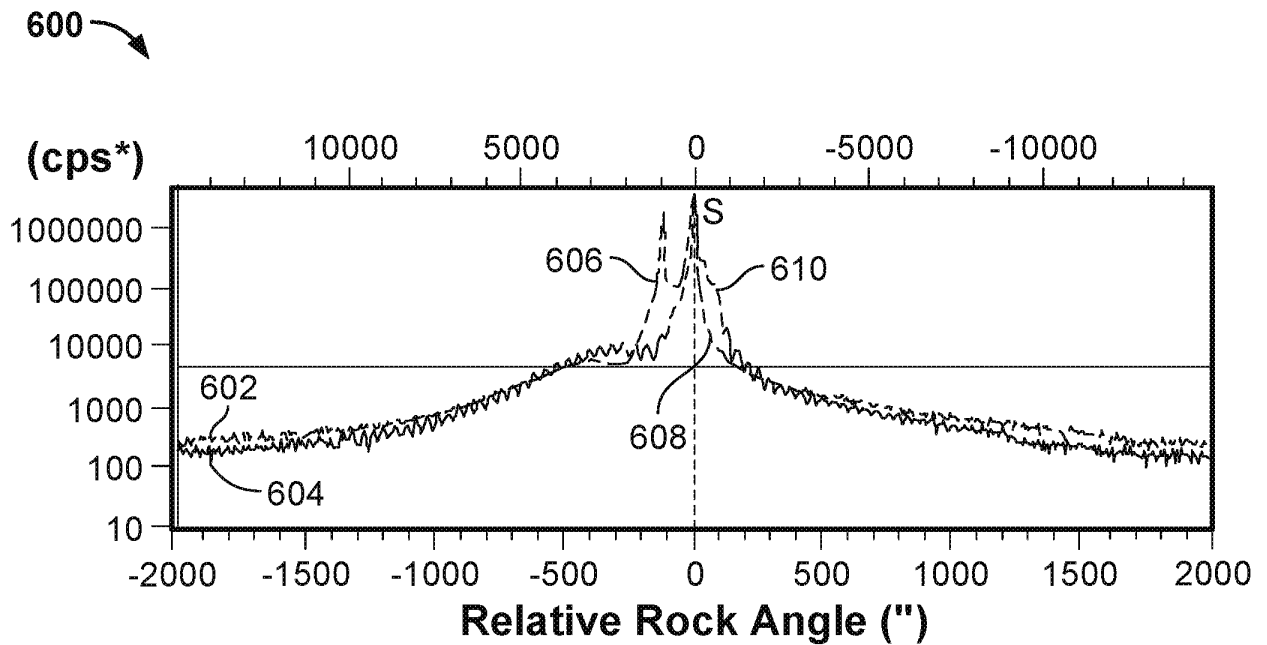


FIG. 6

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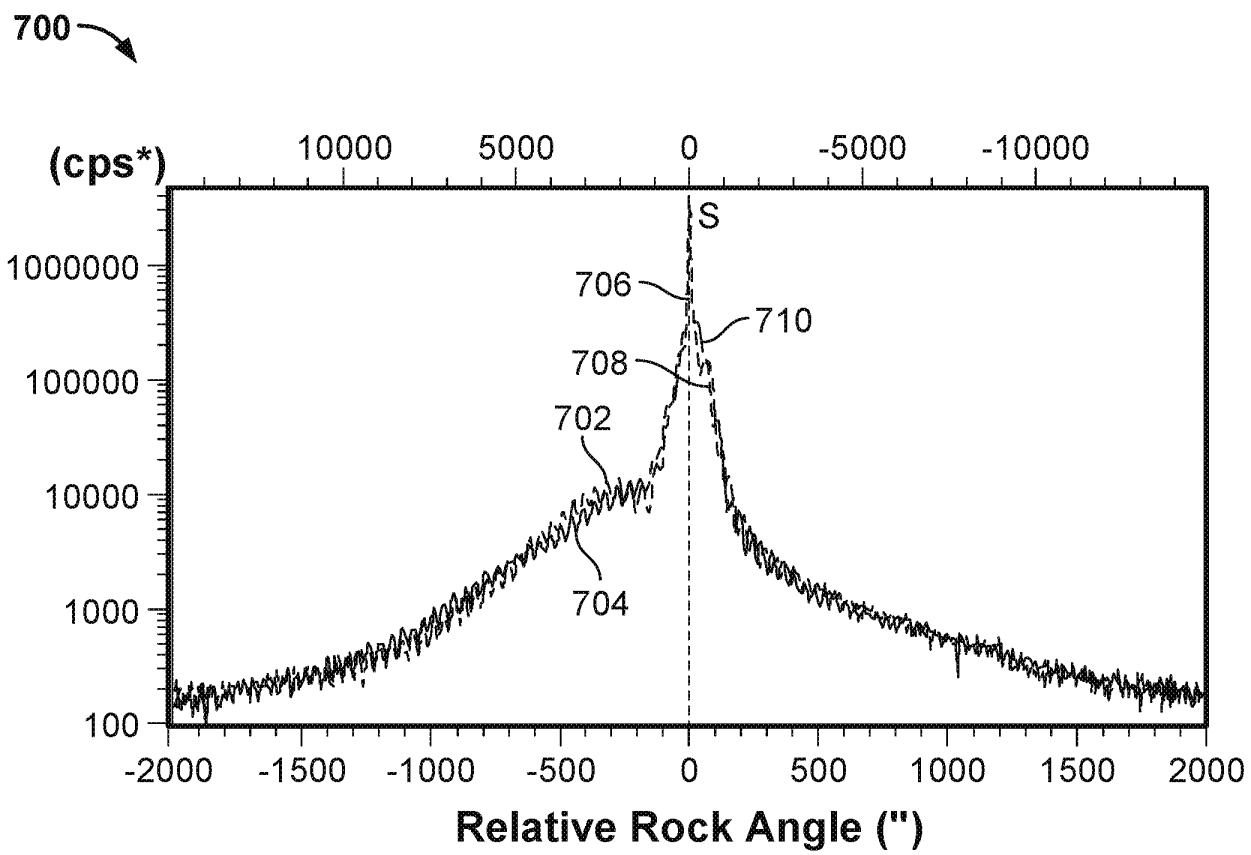


FIG. 7

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800 ↗

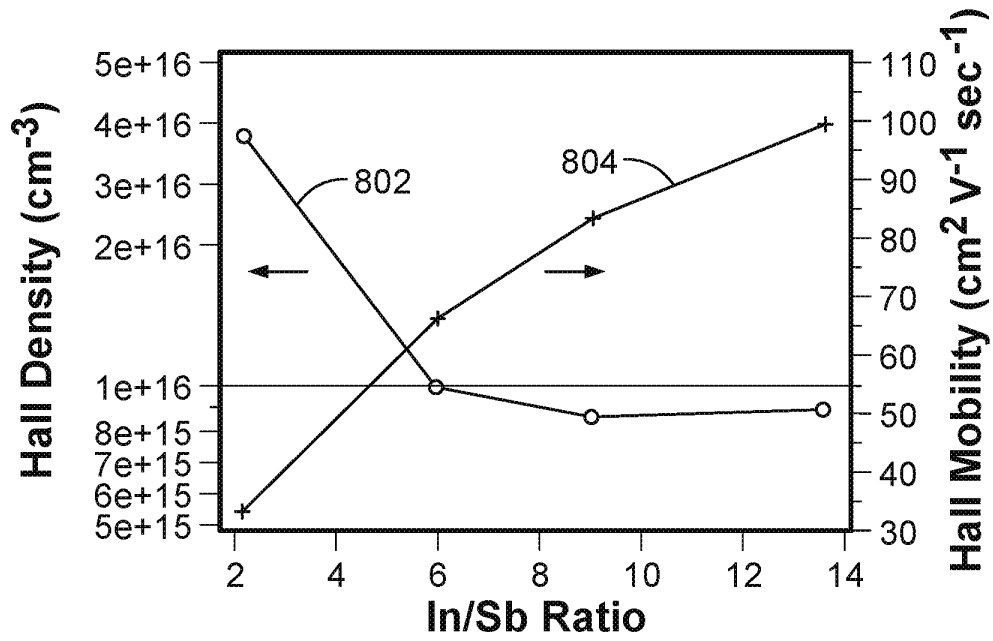


FIG. 8

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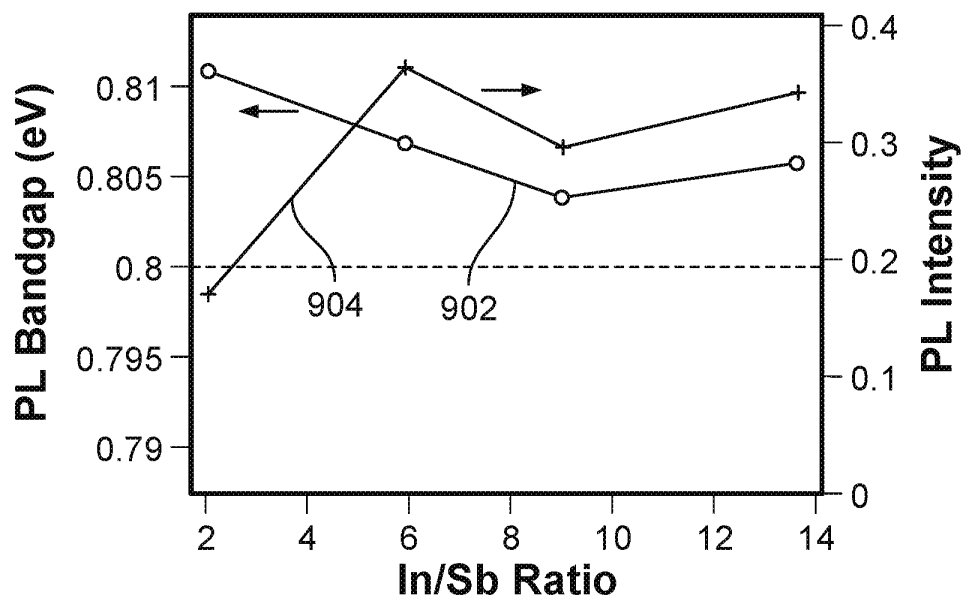


FIG. 9

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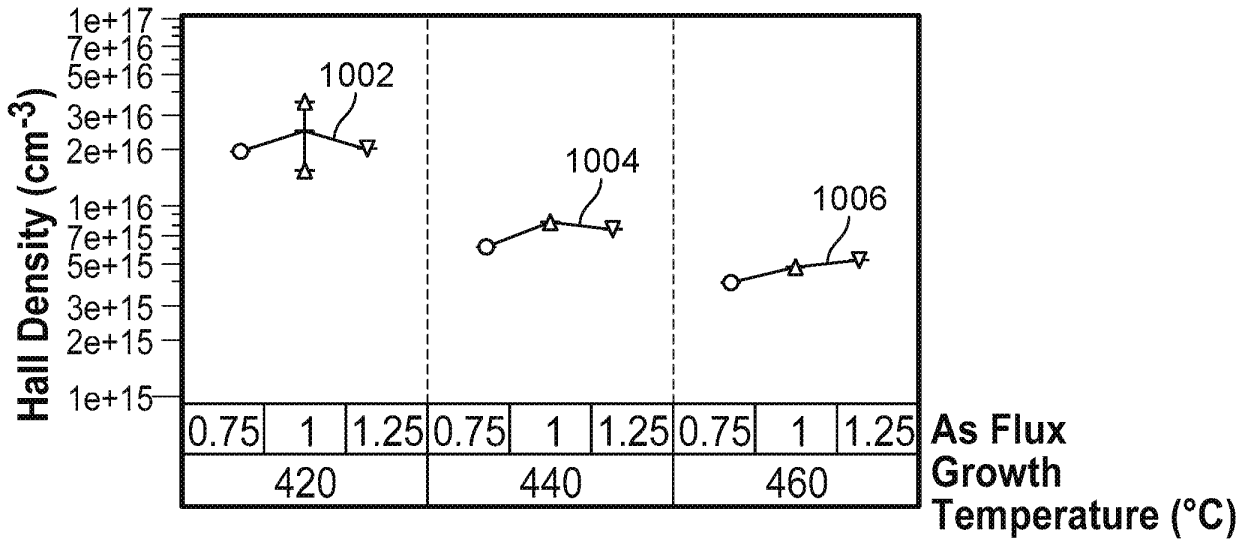


FIG. 10

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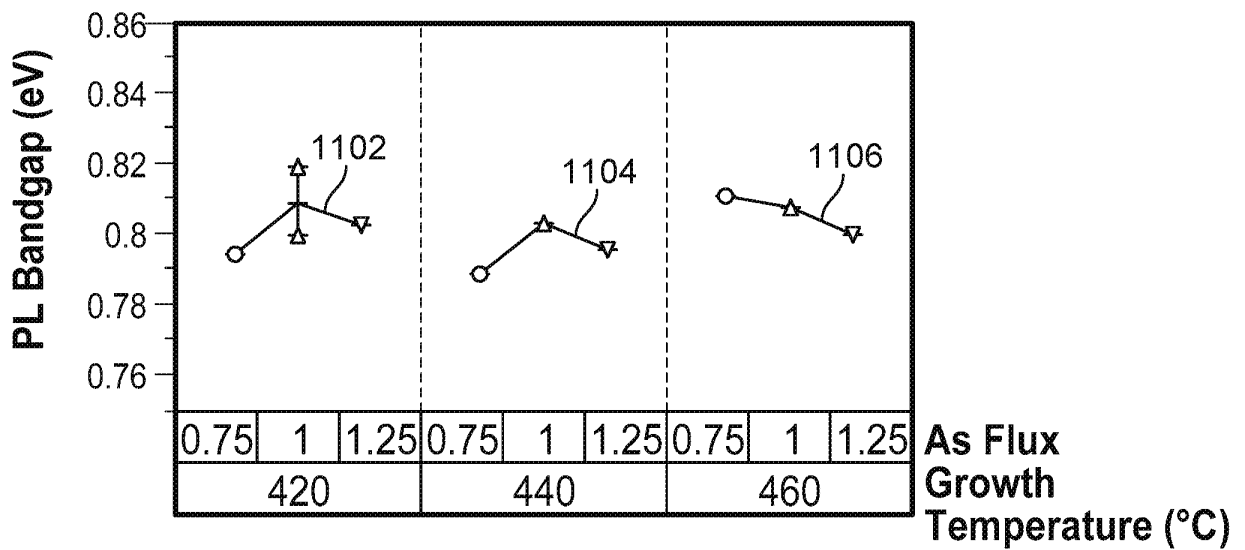


FIG. 11

7/9

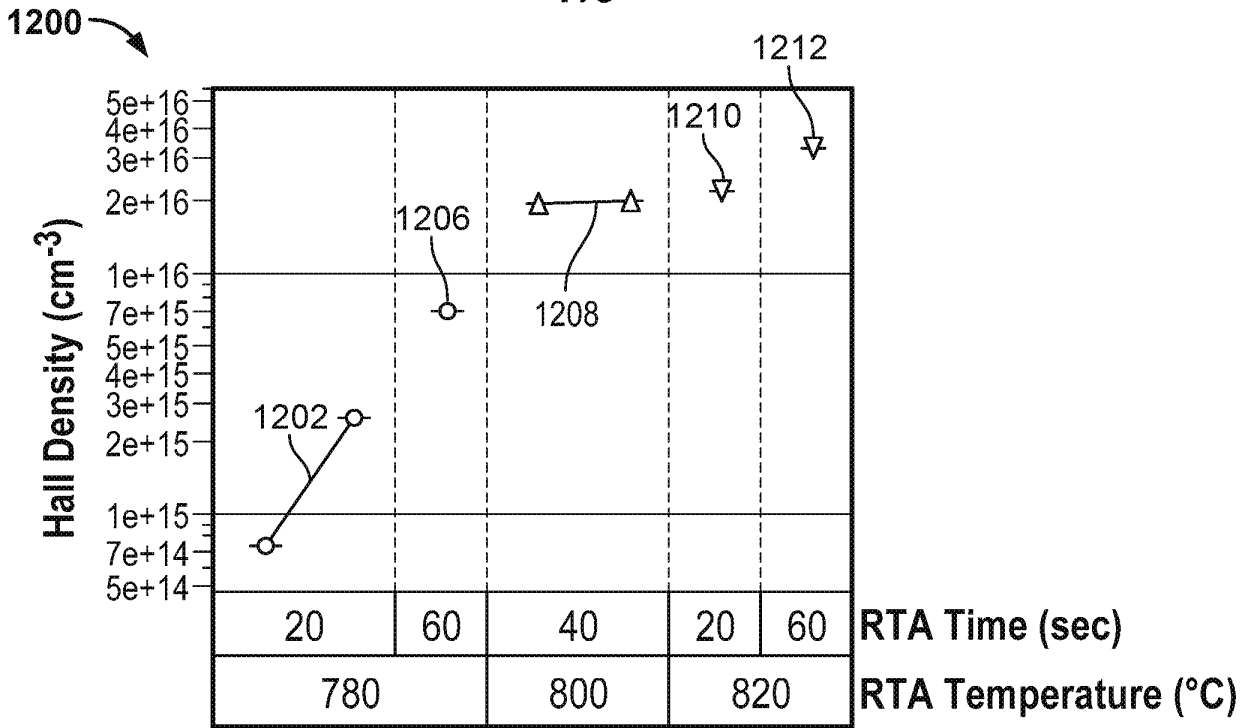


FIG. 12

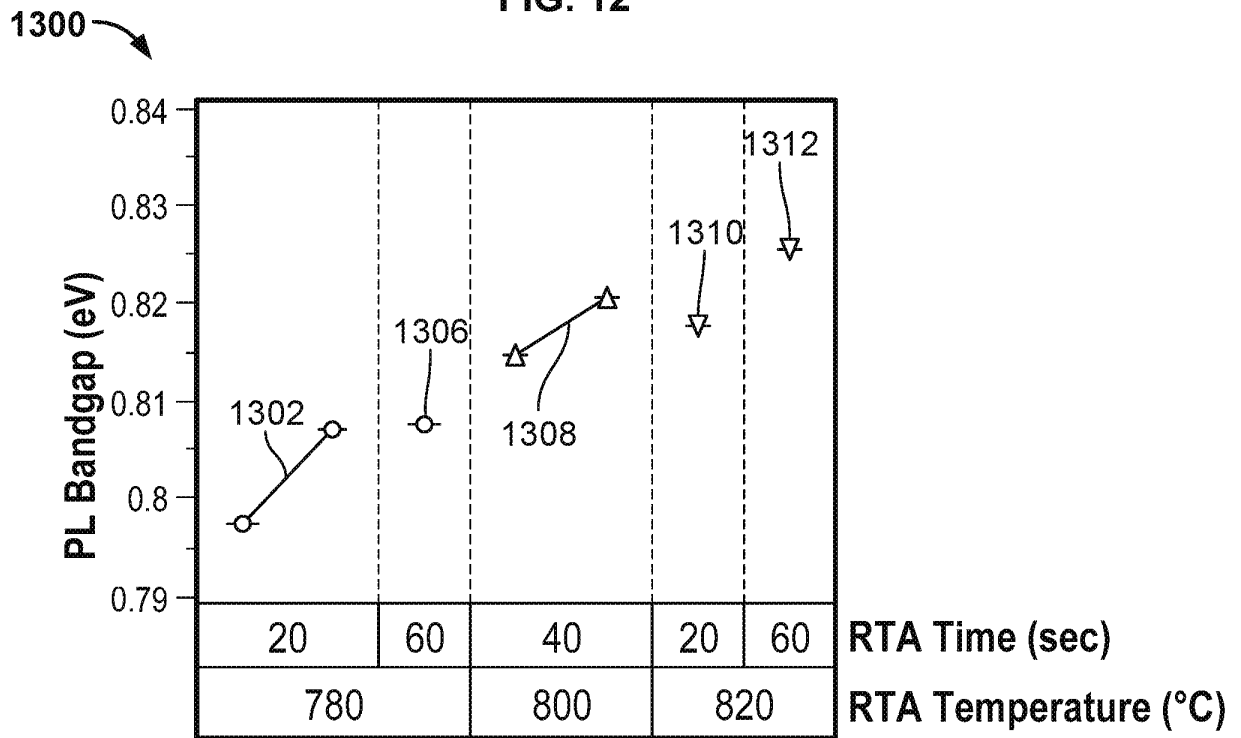


FIG. 13

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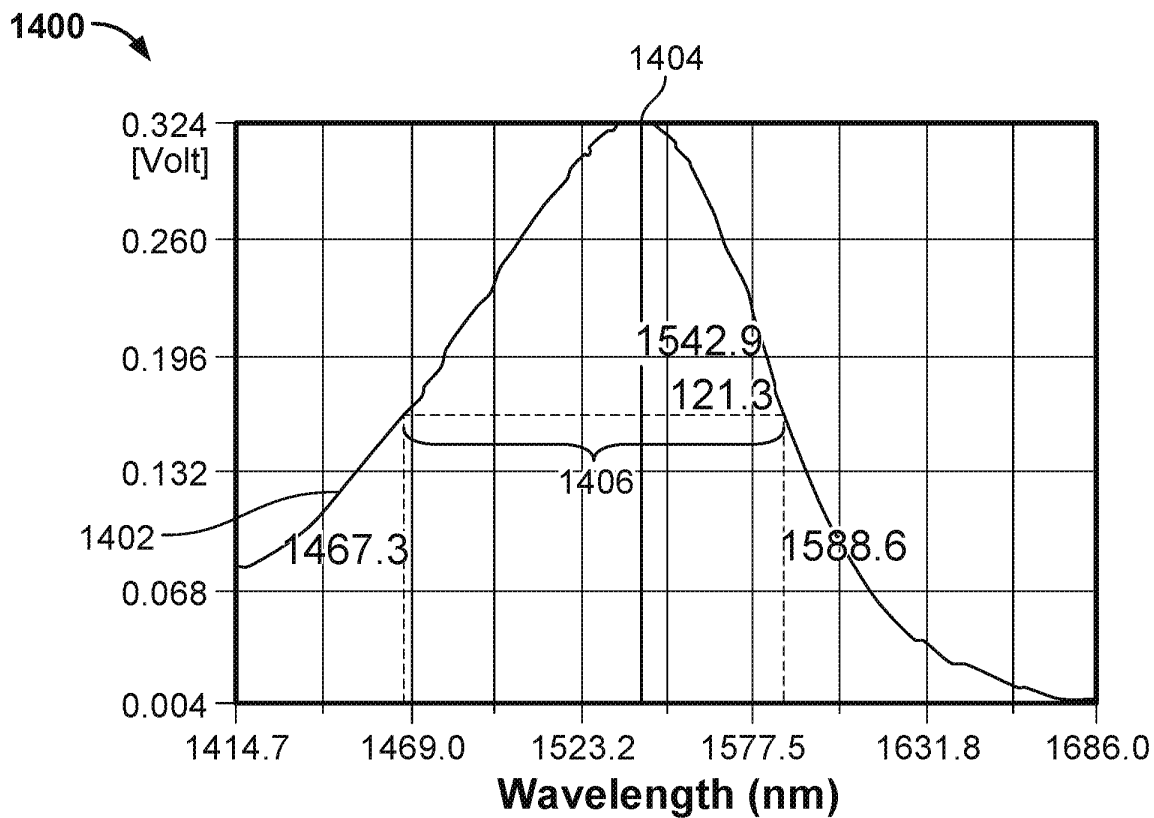


FIG. 14

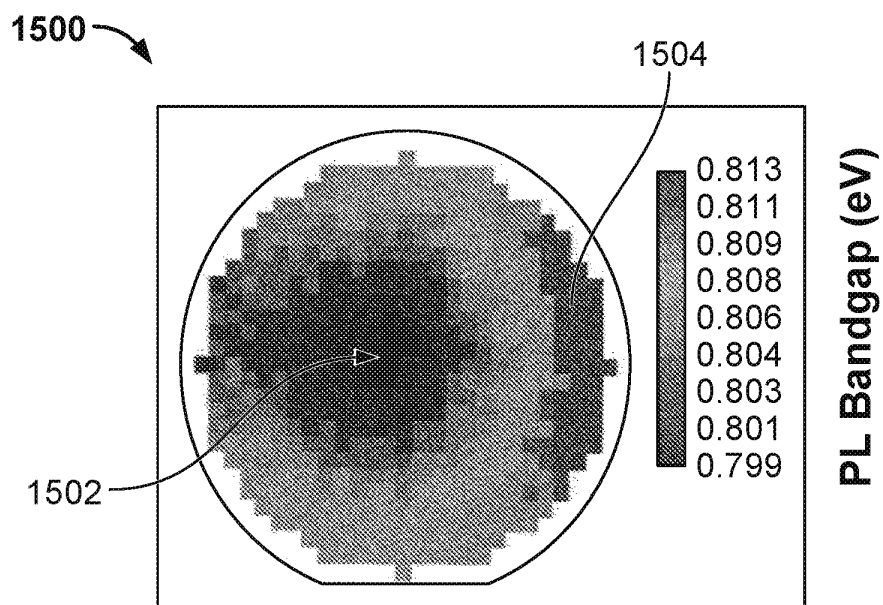


FIG. 15

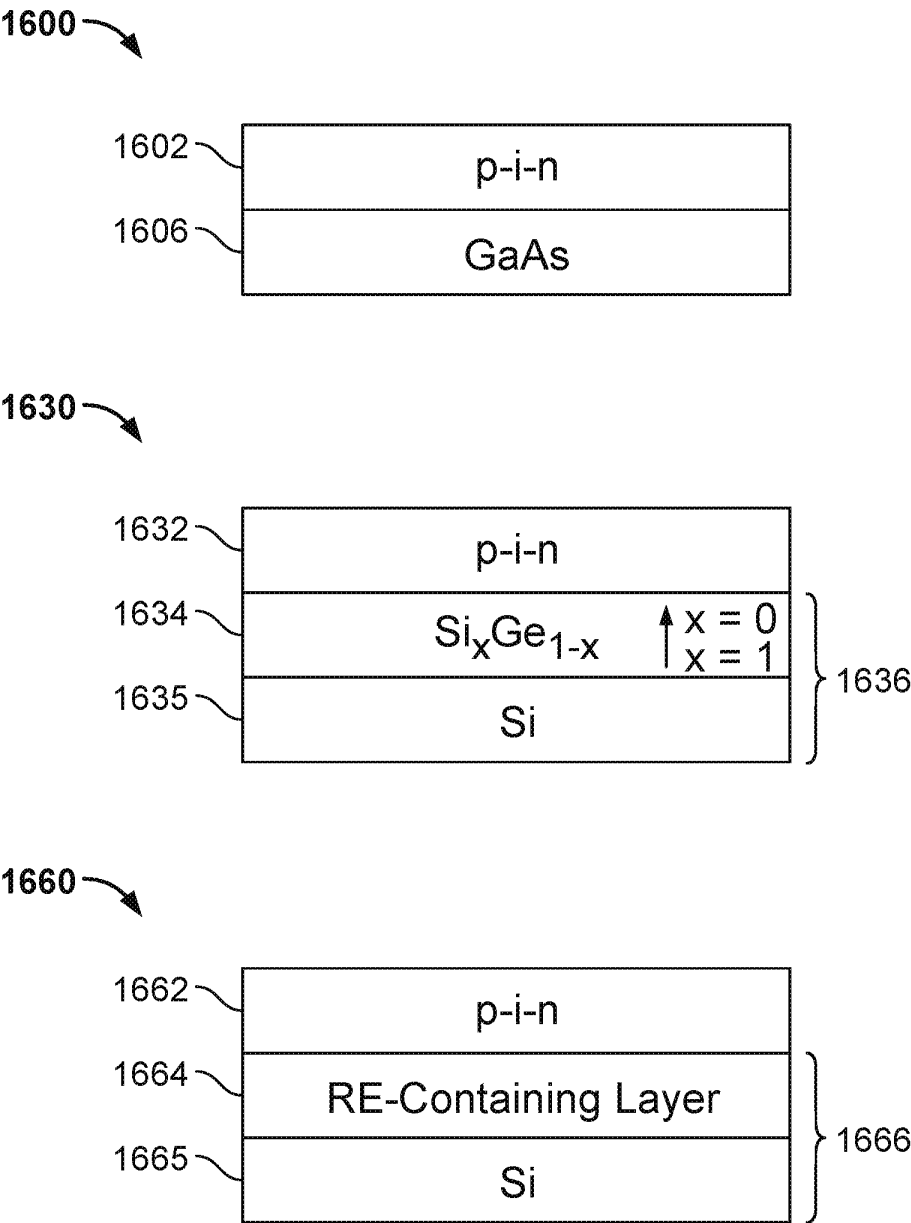


FIG. 16

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		OPTOELECTRONIC DETECTORS HAVING A DILUTE NITRIDE LAYER ON A SUBSTRATE WITH A LATTICE PARAMETER NEARLY MATCHING GAAS		
First Named Inventor/Applicant Name:		Robert Yanka		
Filer:		James Francis Mack/Pamela Harrison		
Attorney Docket Number:		111848-0002-101		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
<b>Basic Filing:</b>				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
<b>Pages:</b>				
<b>Claims:</b>				
Claims in Excess of 20	1202	10	80	800
<b>Miscellaneous-Filing:</b>				
Late Filing Fee for Oath or Declaration	1051	1	140	140

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
<b>Petition:</b>				
<b>Patent-Appeals-and-Interference:</b>				
<b>Post-Allowance-and-Post-Issuance:</b>				
<b>Extension-of-Time:</b>				
<b>Miscellaneous:</b>				
<b>Total in USD (\$)</b>				<b>2540</b>

## Electronic Acknowledgement Receipt

<b>EFS ID:</b>	26121010
<b>Application Number:</b>	15188396
<b>International Application Number:</b>	
<b>Confirmation Number:</b>	1083
<b>Title of Invention:</b>	OPTOELECTRONIC DETECTORS HAVING A DILUTE NITRIDE LAYER ON A SUBSTRATE WITH A LATTICE PARAMETER NEARLY MATCHING GAAS
<b>First Named Inventor/Applicant Name:</b>	Robert Yanka
<b>Customer Number:</b>	28120
<b>Filer:</b>	James Francis Mack/Pamela Harrison
<b>Filer Authorized By:</b>	James Francis Mack
<b>Attorney Docket Number:</b>	111848-0002-101
<b>Receipt Date:</b>	21-JUN-2016
<b>Filing Date:</b>	
<b>Time Stamp:</b>	15:51:26
<b>Application Type:</b>	Utility under 35 USC 111(a)

### Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$2540
RAM confirmation Number	3795
Deposit Account	181945
Authorized User	Mack, James
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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	111848-0002-101_IDS.pdf	82376	no	2
			c6acc6d6f6877b5d085c954c1203533c52a32346		
Warnings:					
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2	Application Data Sheet	111848-0002-101_ADS.pdf	1823020	no	9
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3	Transmittal of New Application	111848-0002-101_Utility_Transmittal.pdf	91729	no	1
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<b>Warnings:</b>					
<b>Information:</b>					
18	Non Patent Literature	Wistey.pdf	57290 aafb41075115387ca7a66add7bf2773d3245658f	no	2
<b>Warnings:</b>					
<b>Information:</b>					
19	Non Patent Literature	Yuen.pdf	223275 44158e34041c63df1d7fa722dcf38001fa8428f5	no	8
<b>Warnings:</b>					
<b>Information:</b>					
20	Non Patent Literature	Niu.pdf	1863702 cce9ed0043529d8feb83bee8c72dedb957ff1c1e	no	4
<b>Warnings:</b>					
<b>Information:</b>					
21		111848-0002-101_Specification.pdf	160379 2b0afaf87d04e9cca650cc8a2f37abe1cdc815da	yes	24
	<b>Multipart Description/PDF files in .zip description</b>				
	<b>Document Description</b>		<b>Start</b>	<b>End</b>	
	Specification		1	19	
	Claims		20	23	
	Abstract		24	24	
<b>Warnings:</b>					
<b>Information:</b>					
22	Information Disclosure Statement (IDS) Form (SB08)	111848-0002-101-SB-08.pdf	136126 785ede722cbb83422e2d625f81c8de0386546ec5	no	3
<b>Warnings:</b>					
<b>Information:</b>					
This is not an USPTO supplied IDS fillable form					
23	Drawings-only black and white line drawings	111848-0002-101_Drawings.pdf	508942 44b3c10ef44ca632880e3555558bbae3335fec771	no	9
<b>Warnings:</b>					
<b>Information:</b>					

24	Fee Worksheet (SB06)	fee-info.pdf	38598 6611f3a11702dfeab86be8d1e7814b8b7dfe59a	no	2
<b>Warnings:</b>					
<b>Information:</b>					
<b>Total Files Size (in bytes):</b>			27287156		
<p><b>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</b></p> <p><b><u>New Applications Under 35 U.S.C. 111</u></b>  If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><b><u>National Stage of an International Application under 35 U.S.C. 371</u></b>  If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><b><u>New International Application Filed with the USPTO as a Receiving Office</u></b>  If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

Docket No.: 111848-0002-101  
(PATENT)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

---

In re Patent Application of:  
Yanka et al.

Application No.: Not Yet Assigned

Confirmation No.: N/A

Filed: Concurrently Herewith

Art Unit: N/A

For: OPTOELECTRONIC DETECTORS HAVING A  
DILUTE NITRIDE LAYER ON A SUBSTRATE  
WITH A LATTICE PARAMETER NEARLY  
MATCHING GAAS

---

Examiner: Not Yet Assigned

**INFORMATION DISCLOSURE STATEMENT (IDS)**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to 37 C.F.R. § 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement accompanies the new patent application submitted herewith.

In accordance with 37 C.F.R. § 1.98(a)(2)(ii), Applicant has not submitted a copy of the U.S. patent. Applicant submits herewith copies of non-patent literature in accordance with 37 C.F.R. § 1.98(a)(2).

In accordance with 37 C.F.R. § 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 C.F.R. § 1.56(a) exists. In accordance with 37 C.F.R. § 1.97(h), the filing of this Information Disclosure Statement shall not be construed to be an admission that any patent, publication or other information referred to therein is “prior art” for this invention unless specifically designated as such.

It is submitted that the Information Disclosure Statement is in compliance with 37 C.F.R. § 1.98 and the Examiner is respectfully requested to consider the listed references.

The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 18-1945, under Order No. 111848-0002-101.

Dated: June 21, 2016

Respectfully submitted,

By /James F. Mack/  
James F. Mack

Registration No.: 74,196  
ROPES & GRAY LLP  
1900 University Avenue  
6th Floor  
East Palo Alto, California 94303-2284  
(650) 617-4000  
(617) 235-9492 (Fax)  
Agent For Applicant

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

<b>Application Data Sheet 37 CFR 1.76</b>		Attorney Docket Number	111848-0002-101
		Application Number	
Title of Invention	OPTOELECTRONIC DETECTORS HAVING A DILUTE NITRIDE LAYER ON A SUBSTRATE WITH A LATTICE PARAMETER NEARLY MATCHING GAAS		
<p>The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.</p> <p>This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.</p>			

**Secrecy Order 37 CFR 5.2:**

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

**Inventor Information:**

Inventor	1				Remove	
Legal Name						
Prefix	Given Name	Middle Name	Family Name	Suffix		
	Robert		Yanka			
Residence Information (Select One) • US Residency Non US Residency Active US Military Service						
City	Kernersville	State/Province	NC	Country of Residence	US	
Mailing Address of Inventor:						
Address 1	QE-North Carolina					
Address 2	494 Gallimore Dairy Road					
City	Greensboro	State/Province	NC			
Postal Code	27409	Country	US			
Inventor	2				Remove	
Legal Name						
Prefix	Given Name	Middle Name	Family Name	Suffix		
	Seokjae		Chung			
Residence Information (Select One) • US Residency Non US Residency Active US Military Service						
City	Oak Ridge	State/Province	NC	Country of Residence	US	
Mailing Address of Inventor:						
Address 1	QE-North Carolina					
Address 2	494 Gallimore Dairy Road					
City	Greensboro	State/Province	NC			
Postal Code	27409	Country	US			
Inventor	3				Remove	
Legal Name						
Prefix	Given Name	Middle Name	Family Name	Suffix		
	Kalyan		Nunna			
Residence Information (Select One) • US Residency Non US Residency Active US Military Service						

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

<b>Application Data Sheet 37 CFR 1.76</b>		Attorney Docket Number		111848-0002-101	
		Application Number			
Title of Invention		OPTOELECTRONIC DETECTORS HAVING A DILUTE NITRIDE LAYER ON A SUBSTRATE WITH A LATTICE PARAMETER NEARLY MATCHING GAAS			
City	High Point	State/Province	NC	Country of Residence <sup>i</sup>	US
<b>Mailing Address of Inventor:</b>					
Address 1		QE-North Carolina			
Address 2		494 Gallimore Dairy Road			
City	Greensboro	State/Province	NC		
Postal Code	27409	Country i	US		
Inventor	4				<a href="#">Remove</a>
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Rodney		Pelzel		
Residence Information (Select One) <input checked="" type="radio"/> US Residency <input type="radio"/> Non US Residency <input type="radio"/> Active US Military Service					
City	Emmaus	State/Province	PA	Country of Residence <sup>i</sup>	US
<b>Mailing Address of Inventor:</b>					
Address 1		QE-Pennsylvania			
Address 2		119 Technology Drive			
City	Bethlehem	State/Province	PA		
Postal Code	18049	Country i	US		
Inventor	5				<a href="#">Remove</a>
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Howard		Williams		
Residence Information (Select One) <input type="radio"/> US Residency <input checked="" type="radio"/> Non US Residency <input type="radio"/> Active US Military Service					
City	St. Mellons, Cardiff	Country of Residence <sup>i</sup>		GB	
<b>Mailing Address of Inventor:</b>					
Address 1		QE, plc			
Address 2		Pascal Close, IQE plc Head Office			
City	St. Mellons, Cardiff	State/Province			
Postal Code	CF3 0LW	Country i	GB		
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the <b>Add</b> button. <a href="#">Add</a>					

**Correspondence Information:**

Enter either Customer Number or complete the Correspondence Information section below.  
For further information see 37 CFR 1.33(a).

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

<b>Application Data Sheet 37 CFR 1.76</b>		Attorney Docket Number	111848-0002-101
		Application Number	
Title of Invention	OPTOELECTRONIC DETECTORS HAVING A DILUTE NITRIDE LAYER ON A SUBSTRATE WITH A LATTICE PARAMETER NEARLY MATCHING GAAS		

☐ An Address is being provided for the correspondence information of this application.

Customer Number	28120		
Email Address	USPatentMail@ropesgray.com	Add Email	Remove Email

### Application Information:

Title of the Invention	OPTOELECTRONIC DETECTORS HAVING A DILUTE NITRIDE LAYER ON A SUBSTRATE WITH A LATTICE PARAMETER NEARLY MATCHING GAAS		
Attorney Docket Number	111848-0002-101	Small Entity Status Claimed	<input type="checkbox"/>
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	9	Suggested Figure for Publication (if any)	

### Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

### Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

**Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

### Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	<input checked="" type="radio"/> Customer Number	US Patent Practitioner	<input type="radio"/> Limited Recognition (37 CFR 11.9)
Customer Number	28120		

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

<b>Application Data Sheet 37 CFR 1.76</b>		Attorney Docket Number	111848-0002-101
		Application Number	
Title of Invention	OPTOELECTRONIC DETECTORS HAVING A DILUTE NITRIDE LAYER ON A SUBSTRATE WITH A LATTICE PARAMETER NEARLY MATCHING GAAS		

**Domestic Benefit/National Stage Information:**

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Claims benefit of provisional	62/183060	2015-06-22
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the <b>Add</b> button.			Add

**Foreign Priority Information:**

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)<sup>i</sup> the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Application Number	Country <sup>i</sup>	Filing Date (YYYY-MM-DD)	Access Code <sup>i</sup> (if applicable)	Remove
Additional Foreign Priority Data may be generated within this form by selecting the <b>Add</b> button.				Add

**Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications**

<p>This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.</p> <p><input type="checkbox"/> NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.</p>
--

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

<b>Application Data Sheet 37 CFR 1.76</b>		Attorney Docket Number	111848-0002-101
		Application Number	
Title of Invention	OPTOELECTRONIC DETECTORS HAVING A DILUTE NITRIDE LAYER ON A SUBSTRATE WITH A LATTICE PARAMETER NEARLY MATCHING GAAS		

## Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

**NOTE:** This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

### 1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

**A. Priority Document Exchange (PDX)** - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

**B. Search Results from U.S. Application to EPO** - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

### 2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

**NOTE:** Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

<b>Application Data Sheet 37 CFR 1.76</b>		Attorney Docket Number	111848-0002-101
		Application Number	
Title of Invention	OPTOELECTRONIC DETECTORS HAVING A DILUTE NITRIDE LAYER ON A SUBSTRATE WITH A LATTICE PARAMETER NEARLY MATCHING GAAS		

**Applicant Information:**

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

<b>Applicant</b>	1	<input type="button" value="Remove"/>
------------------	---	---------------------------------------

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

<input checked="" type="radio"/> Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.		Person who shows sufficient proprietary interest

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	IQE, plc		
-------------------	----------	--	--

**Mailing Address Information For Applicant:**

Address 1	Pascal Close		
Address 2	IQE plc Head Office		
City	St. Mellons, Cardiff	State/Province	
Country	GB	Postal Code	CF3 0LW
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button.

**Assignee Information including Non-Applicant Assignee Information:**

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

<b>Application Data Sheet 37 CFR 1.76</b>		Attorney Docket Number	111848-0002-101
		Application Number	
Title of Invention	OPTOELECTRONIC DETECTORS HAVING A DILUTE NITRIDE LAYER ON A SUBSTRATE WITH A LATTICE PARAMETER NEARLY MATCHING GAAS		

<b>Assignee</b>	1			
Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.				
				<input type="button" value="Remove"/>
If the Assignee or Non-Applicant Assignee is an Organization check here.				<input type="checkbox"/>
Prefix	Given Name	Middle Name	Family Name	Suffix
<b>Mailing Address Information For Assignee including Non-Applicant Assignee:</b>				
Address 1				
Address 2				
City		State/Province		
Country i		Postal Code		
Phone Number		Fax Number		
Email Address				
Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.				<input type="button" value="Add"/>

**Signature:**

**NOTE:** This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). However, if this Application Data Sheet is submitted with the **INITIAL** filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

<b>Signature</b>	/James F. Mack/		Date (YYYY-MM-DD)	2016-06-21
First Name	James	Last Name	Mack	Registration Number
				74196
Additional Signature may be generated within this form by selecting the Add button.				<input type="button" value="Add"/>

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

<b>Application Data Sheet 37 CFR 1.76</b>		Attorney Docket Number	111848-0002-101
		Application Number	
Title of Invention	OPTOELECTRONIC DETECTORS HAVING A DILUTE NITRIDE LAYER ON A SUBSTRATE WITH A LATTICE PARAMETER NEARLY MATCHING GAAS		

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

## Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

- 1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
- 2 A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
- 3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
- 4 A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
- 5 A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
- 6 A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
- 7 A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
- 8 A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
- 9 A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.