

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent of Pourkeramati:

U.S. Patent No. 6,058,045

Issued: May 2, 2000

Title: SERIAL FLASH MEMORY

Petition for *Inter Partes* Review

Attorney Docket No.: 351912-22.045

Customer No.: 26379

Petitioner: Toshiba Corporation

Real Parties in Interest: Toshiba Corporation; Toshiba America, Inc.; Toshiba America Electronic Components, Inc.; Toshiba America Information Systems, Inc.

PETITION FOR *INTER PARTES* REVIEW

Mail Stop Patent Board
Patent Trial and Appeal Board
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to the provisions of 35 U.S.C. §§ 311-319, Toshiba Corporation (hereinafter “Petitioner”) hereby petitions the Patent Trial and Appeal Board to institute an *inter partes* review of claims 1 and 4 of United States Patent No. 6,058,045.

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EXHIBIT LIST

TOSH-1001	U.S. Patent No. 6,058,045 to Pourkeramati
TOSH-1002	Prosecution File History for U.S. Patent No. 6,058,045
TOSH-1003	Prosecution File History for U.S. Patent No. 5,953,254
TOSH-1004	Provisional Patent Application 60/025,698
TOSH-1005	U.S. Patent No. 5,297,029 to Nakai (“ Nakai ”)
TOSH-1006	Declaration of Robert J. Murphy
TOSH-1007	<i>A 35 ns Cycle Time 3.3 V Only 32 Mb NAND Flash EEPROM</i> , Yoshihisa Iwata et al, IEEE Journal of Solid-State Circuits (November 1995)
TOSH-1008	Declaration of Doug Wong
TOSH-1009	Datasheet for TC584000P/F/FT/TR CMOS NAND E ² PROM electrically erasable and programmable Nonvolatile Memory, published in Toshiba 1993 MOS Memory (Non-Volatile) Databook (“ 1993 Databook ”)

I. Mandatory Notices

A. Real Party-in-Interest

Pursuant to 37 C.F.R. § 42.8(b)(1), the real parties-in-interest are Toshiba Corporation; Toshiba America, Inc.; Toshiba America Electronic Components, Inc.; and Toshiba America Information Systems, Inc. (collectively “Real Parties-In-Interest”).

B. Related Matters

Pursuant to 37 C.F.R. § 42.8(b)(2), Petitioner states that Intellectual Ventures I LLC and Intellectual Ventures II LLC (“Intellectual Ventures”) is asserting U.S. Patent 6,058,045 (“the ’045 Patent”) against the Real Parties-In-Interest in a suit filed March 20, 2013, styled *Intellectual Ventures I LLC and Intellectual Ventures II LLC v. Toshiba Corporation, Toshiba America, Inc., Toshiba America Electronic Components, Inc., and Toshiba America Information Systems, Inc.*, pending in the U.S. District Court for the district of Delaware. As of the filing of this petition, no other judicial or administrative matters are known to Petitioner that would affect, or be affected by, a decision in an *inter partes* review of the ’045 Patent.

C. Lead and Back-up Counsel

Pursuant to 37 C.F.R. § 42.8(b)(3), Petitioner provides the following designation of counsel:

<u>Lead Counsel</u>	<u>Back-up Counsel</u>
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USPTO Customer No. 26379 USPTO Reg. No. 39,749	USPTO Customer No. 26379 USPTO Reg. No. 30,103

D. Service Information

Pursuant to 37 C.F.R. § 42.8(b)(4), papers concerning this matter should be served on either Alan Limbach or Gerald Sekimura identified above, and copying if appropriate the following email address:

IV-Toshiba-DLA-Team@dlapiper.com.

II. Grounds for Standing

Pursuant to 37 CFR § 42.104(a), Petitioner certifies that (i) the '045 Patent is available for *inter partes* review and (ii) Petitioner is not estopped or barred from requesting *inter partes* review challenging the '045 Patent on the grounds identified in this petition.

III. Relief Requested

Petitioner asks that the Board review the accompanying prior art and analysis, institute a trial for *inter partes* review of claims 1 and 4 of the '045 Patent, and cancel claims 1 and 4 as invalid for the reasons set forth below.

IV. The Reasons for the Requested Relief

The full statement of the reasons for relief requested is as follows:

A. Summary of Reasons

The '045 Patent relates to a flash memory cell structure and an array configuration of flash memory cells. More specifically, claims 1 and 4 of the '045 Patent are directed to the voltages used to program a specific array configuration of flash memory cells.

The flash memory array configuration, and the specific technique used to program that array configuration, as recited in claims 1 and 4, were known years before even the earliest date (September 9, 1996) to which the '045 Patent purports to claim priority. Evidence of such can be found in:

(1) Toshiba's U.S. Patent 5,297,029 to Nakai et al. ("**Nakai**"), which was filed on December 18, 1992 and issued on March 22, 1994. (TOSH-1005.)

(2) Datasheet for Toshiba's TC584000P/F/FT/TR CMOS NAND E²PROM electrically erasable and programmable nonvolatile memory,

published in its 1993 MOS Memory (Non-Volatile) Databook (“**1993 Databook**”). (TOSH-1009, pages 367-380.)

This petition demonstrates that Nakai and the 1993 Databook each anticipates claims 1 and 4 of the '045 Patent, rendering them invalid.

B. The '045 Patent

1. Overview

The '045 Patent contains 6 claims. Claims 1-3 are independent apparatus claims each of which recite the same structural configuration of an array of flash memory cells. The recited memory array configuration includes columns of serially connected flash memory cells, and various lines connected to different terminals and points within the array. Claim 1 further recites certain voltages on the various memory array lines during programming. Claim 2 further recites certain voltages on the various memory array lines during erase. Claim 3 further recites certain voltages on the various memory array lines during a programming inhibit mode. (TOSH-1001, 8:22-9:33.)

Claim 4 is an independent method claim reciting the steps of applying the certain voltages on the various memory array lines as recited in claim 1 for programming memory cells. Claim 5 is a method claim which depends from claim 4 and recites the steps of applying the certain voltages on the various memory array lines as recited in claim 2 for erasing memory cells. Claim 6 is a

method claim which depends from claim 5 and recites the steps of applying the certain voltages on the various memory array lines as recited in claim 3 for accomplishing program inhibit. (TOSH-1001, 10:1-31.)

This Petition requests review only of claims 1 and 4 and the memory array programming recited therein. Figure 4 of the '045 Patent shows the exemplary memory array circuit covered by claims 1 and 4:

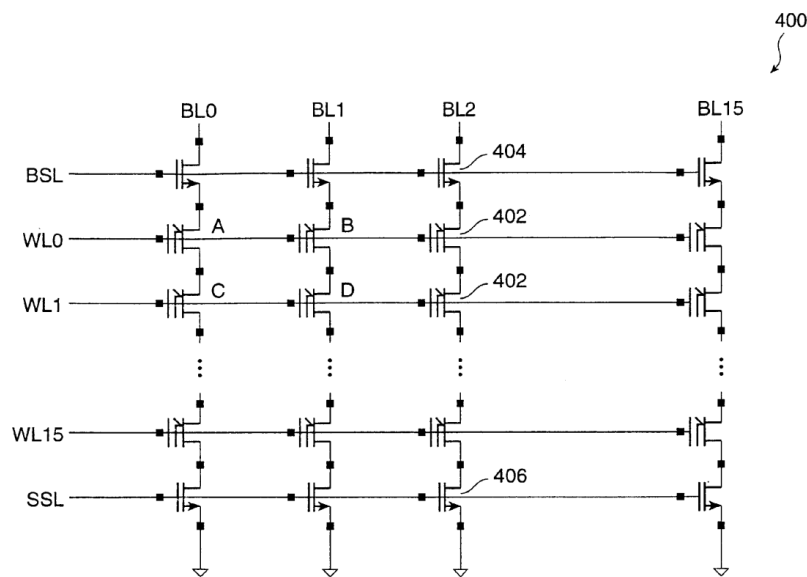


FIG. 4

(TOSH-1001, Fig. 4.)

According to the '045 Patent, the array 400 includes columns of memory cells 402 located at the intersections of word lines **WL0-WL15** and bit lines **BL0-BL15**. Bit line select transistors **404** are located at the top of each memory cell column, and couple bit lines BL0-BL15 to the memory cell columns. Source select transistors **406** are located at the bottom of each memory cell column, and couple the memory cell columns to ground (or Vss). A bit line select control line **BSL**

controls the gate terminals of the bit line select transistors 404, and the source select control line SSL controls the gate terminals of the source select transistors 406. (TOSH-1001, 6:25-33 and Fig. 4.)

Table I of the '045 Patent discloses the various voltages that are applied to selected and unselected lines of the array during erase, program and read operations:

TABLE I

	Control Line	Erase	Program	Read	Condition
40	BSL	V _{cc}	V _{cc}	V _{cc}	Selected
	SSL	V _{ss}	V _{ss}	V _{cc}	Selected
	BLO	V _{cc}	V _{ss}	1.0–1.4V	Selected
	BL1	V _{ss}	V _{cc}	0.5V	Unselected
	WL0	V _{cc}	V _{cc}	V _{cc}	Unselected
45	WL1	–12 to –15V	15–20V	V _{ss}	Selected

(TOSH-1001, 6:37-45.)

For example, during a programming operation, according to Table I, the V_{cc} voltage is applied to the selected bit line select control line BSL, the unselected bit line BL1, and the unselected word line WL0. Voltage V_{ss} is applied to the selected source select control line SSL and to the selected bit line BLO. A 15-20V voltage is applied to the selected word line WL1.

2. Prosecution History

The '045 Patent is a divisional of U.S. Patent 5,953,254 (the '254 patent), which claims priority to provisional application No. 60/025,698 (the '698 provisional application). The '045 Patent was allowed in response to a preliminary

amendment which cancelled the claims from the parent case and added the claims which issued as claims 1-6. The preliminary amendment did not include any argument or remarks on the merits. (TOSH-1002, Preliminary Amendment, May 25, 1999.)

The '254 Patent is directed to the design of the individual memory cells (as opposed to the array configuration and operational voltages). During prosecution of the '254 Patent, originally filed claims 8-10 (directed to memory array configuration and the programming, erase and program inhibit voltages) were cancelled in response to a restriction requirement, and filed in the divisional application which became the '045 Patent. (TOSH-1003, Response to Restriction Requirement, July 30, 1998.) Therefore the file history of the '254 patent does not appear relevant to the scope and validity of '045 Patent claims.

The prior art references (Nakai and 1993 Databook) that are the subject of this petition are not listed in the references cited and were not considered by the Examiner during the prosecution of the '045 Patent. (TOSH-1001, Cover Page.)

C. Identification of Challenges

1. Challenged Claims

Claims 1 and 4 of the '045 Patent are challenged in this petition.

2. Statutory Grounds for Challenges

Challenge #1: Claims 1 and 4 of the '045 Patent are anticipated and rendered invalid by Nakai under 35 U.S.C. 102(b) (pre-AIA). The Nakai patent issued on March 22, 1994 (more than one year prior to the earliest claimed priority date – September 9, 1996 – for the '045 Patent). (TOSH-1005, cover page.)

Challenge #2: Claims 1 and 4 of the '045 Patent are anticipated and rendered invalid by the 1993 Databook under 35 U.S.C. 102(b) (pre-AIA). The 1993 Databook was published in 1993, (more than one year prior to the earliest claimed priority date – September 9, 1996 – for the '045 Patent). (TOSH-1008, ¶6, and TOSH-1009.)

3. Claim Construction

Pursuant to 37 C.F.R. § 42.100(b) and 42.204(b)(3), this petition presents claim analysis in a manner that is consistent with the broadest reasonable construction in light of the specification. Claim terms are given their ordinary and accustomed meaning as would be understood by one of ordinary skill in the art, unless the inventor, as a lexicographer, has set forth a special meaning for a term. *Multiform Desiccants, Inc. v. Medzam, Ltd.*, 133 F.3d 1473 (Fed. Cir. 1998); *York Prods., Inc., v. Central Tractor Farm & Family Ctr.*, 99 F.3d 1568, 1572 (Fed. Cir. 1996).

In the '045 Patent, the inventor did not act as a lexicographer and did not provide a special meaning for any of the claim terms. Accordingly, using the broadest reasonable interpretation standard, the terms should be given their ordinary and customary meaning as understood by a person of ordinary skill in the art and consistent with the disclosure. Several key terms are discussed below:

- “*logic low voltage*”: a low voltage, such as ground or Vss. This construction is confirmed in the specification of the '045 Patent, which does not include the term “logic low voltage.” Claims 1 and 4 recite that for programming, a “logic low voltage” is applied to the selected bit line (TOSH-1001, claims 1 and 4), and the specification states that for programming, the selected bit line is grounded and at voltage Vss (TOSH-1001, 7:29 and 6:37-45). Additionally, claims 1 and 4 recite that for programming, a “logic low voltage” is applied to the source select control line, (TOSH-1001, claims 1 and 4), and the specification states for programming, the source select control line is at Vss (TOSH-1001, 6:37-45; 7:36). Also, the specification states that the source select transistors “couple ground (or Vss) to memory cells 402” (TOSH-1001, 6:29-30). One skilled in the art reviewing the '045 Patent would understand that a “logic low voltage” is a low voltage, such as ground or Vss. (TOSH-1006, ¶16).

- “*logic high voltage*”: a positive voltage higher than the logic low voltage, such as Vcc. This construction is confirmed in the specification of the '045 Patent, which does not include the term “logic high voltage.” Specifically, claims 1 and 4 recite that the “logic high voltage” is applied to the “bit line select control line” (BSL), the unselected bit line and the unselected word line during program, and the specification discloses that voltage Vcc is applied to those same lines during program (TOSH-1001, claims 1 and 4; 6:37-45; 7:26-40). One skilled in the art reviewing the '045 Patent would understand that a “logic high voltage” is a voltage higher than the logic low voltage, such as Vcc. (TOSH-1006, ¶17).
- “*boosted positive voltage*”: a positive voltage higher than the logic high voltage. This construction is confirmed in the specification of the '045 Patent, which does not include the term “boosted positive voltage.” Specifically, claims 1 and 4 recite that a boosted positive voltage is applied to the selected word line during program, and the specification discloses that a high voltage (e.g. 15 to 20V) is applied to the selected word line during program (TOSH-1001, claims 1 and 4; 6:37-45; 7:26-40). One skilled in the art reviewing the '045 Patent

would understand that a “boosted positive voltage” is a voltage higher than the logic high voltage. (TOSH-1006, ¶18).

- “*selected bit line*”: the bit line connected to the column of memory cells containing the memory cell to be operated on. “*unselected bit lines*”: the bit lines connected to the columns of memory cells not containing the memory cell to be operated on. The ’045 Patent discloses the relationship between a “selected bit line” and “unselected bit lines” by way of an example involving the programming of memory cell 402-C in Fig. 4 (i.e. the memory cell being operated on during programming). In Fig. 4, memory cell 402-C is depicted in the column of memory cells connected to bit line BL0, while the other bit lines BL1 to BL15 are not connected to the column of memory cells containing memory cell 402-C. In the description, bit line BL0 is referred to as the “selected bit line” and bit lines BL1-BL15 are referred to as the “unselected bit lines.” (TOSH-1001, 7:27-30; Fig. 4.) One skilled in the art reviewing the ’045 Patent would understand that “*selected bit line*” is the bit line connected to the column of memory cells containing the memory cell to be operated on, and “*unselected bit lines*” are the bit lines

connected to the columns of memory cells not containing the memory cell to be operated on. (TOSH-1006, ¶19).

- “*selected word line*”: the word line connected to the row of memory cells containing the memory cell to be operated on. “*unselected word lines*”: the word lines connected to the rows of memory cells not containing the memory cell to be operated on. The ’045 Patent discloses that when programming memory cell 402-C (i.e. the memory cell being operated on during programming), which is connected to word line WL1 but not connected to any of the other word lines, word line WL1 is referred to as the “selected word line” and word lines WL0 and WL2-WL15 are referred to as the “unselected word lines.” (TOSH-1001, 7:27-37; Fig. 4.) One skilled in the art reviewing the ’045 Patent would understand that “*selected word line*” is the word line connected to the row of memory cells containing the memory cell to be operated on, and “*unselected word lines* are the word lines connected to the rows of memory cells not containing the memory cell to be operated on. (TOSH-1006, ¶20).

The proposed claim constructions are presented using the broadest reasonable interpretation standard, which is applied solely for the purposes of *inter partes* review. Because the standards of claim interpretation used by the Courts in

patent litigation are different from the claim interpretation standards used by the Office in claim examination proceedings (including *inter partes* review), Petitioner reserves the right to advocate a different claim interpretation in any other forum in accordance with the claim construction standards applied in such forum.

4. Level of Ordinary Skill in the Art

With respect to the technologies disclosed and claimed in the '045 patent, one of ordinary skill in the art would have had a Bachelors of Science degree in electrical engineering and 5 years of experience, or a Masters of Science degree in electrical engineering and 3 years of experience, working in the field of non-volatile memory devices. (TOSH-1006, ¶9).

5. Identification of How the Construed Claims Are Unpatentable

i. Challenge #1: Claims 1 and 4 are anticipated by Nakai

Claims 1 and 4 of the '045 Patent are anticipated and rendered invalid by Nakai under 35 U.S.C. 102(b) (pre-AIA). Nakai discloses a NAND type EEPROM non-volatile memory array (i.e. flash memory) that includes columns of memory cells “MC” connected in series, and connected at the top to a bit line “BL” via a select transistor T1 and at the bottom to ground GND via a select transistor T2. Select lines SL(1) and SL(2) operate the row of select transistors T1 and the row of select transistors T2, respectively. The array includes word lines WL that

each connect to the select gates of one of the memory cells from each column.

(TOSH-1005, 1:20-30.) The array is shown in Fig. 22(a) of Nakai (which is

included below along-side of Fig. 4 of the '045 patent (the array configurations are

essentially the same):

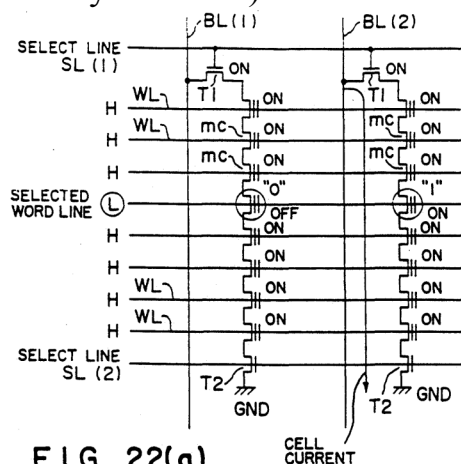


FIG. 22(a)

(TOSH-1005, Fig. 22(a).)

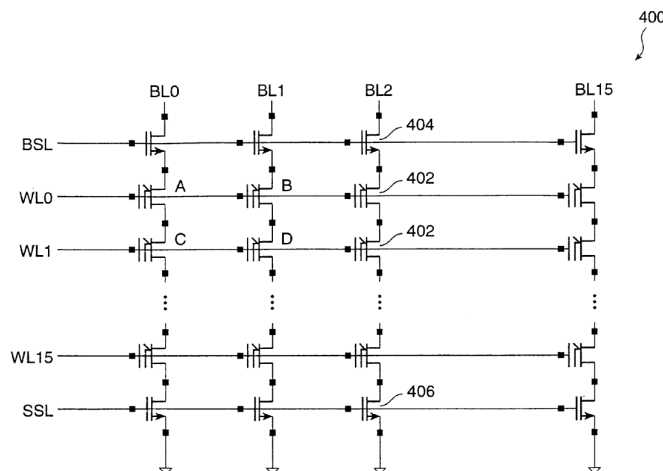


FIG. 4

(TOSH-1001, Fig. 4.)

The programming of the array in Nakai is described from column 1, line 46

to column 2, line 9, and illustrated in Fig. 23(a):

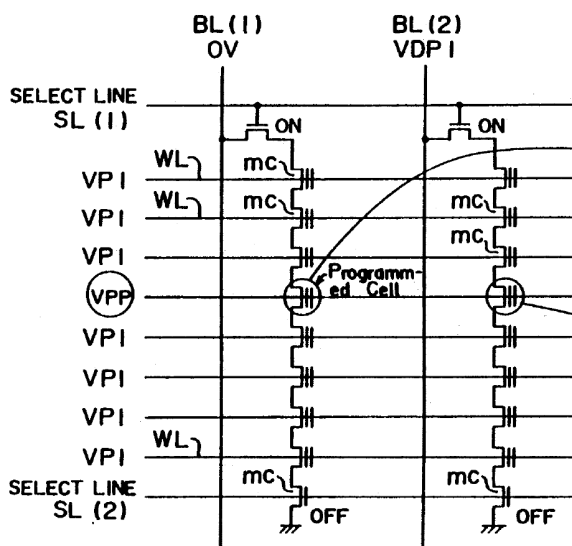


FIG. 23(a)

(TOSH-1005, Fig. 23(a).)

For programming the selected cell labeled “Programmed Cell” in Fig. 23(a), the select line SL(1) is set at 12 V (i.e. “logic high”) so that the select transistors T1 are “ON,” and the select line SL(2) is set at 0V (i.e. “logic low”) so that the select transistors T2 are “OFF.” (TOSH-1005, 1:53-57, Fig. 23(a).) The word line for the selected cell (i.e. the selected word line) is placed at voltage V_{pp} , while the remaining word lines (i.e. the unselected word lines) are placed at V_{PI} . (TOSH-1005, Fig. 23(a).) V_{pp} is a high voltage of “about 20 V” (i.e. a boosted positive voltage). (TOSH-1005, 1:47.) V_{PI} is a voltage of “about 10 V” (i.e. a logic high voltage). (TOSH-1005, 1:50.) The bit line BL(1) for the selected cell (i.e. the selected bit line) is placed at 0V (i.e. a logic low voltage), while the remaining bit lines (i.e. BL(2), the unselected bit lines) are placed at a voltage of V_{DPI} . (TOSH-1005, Fig. 23(a).) V_{DPI} is a voltage of “about 10 V” (i.e. a logic high voltage). (TOSH-1005, 2:3.)

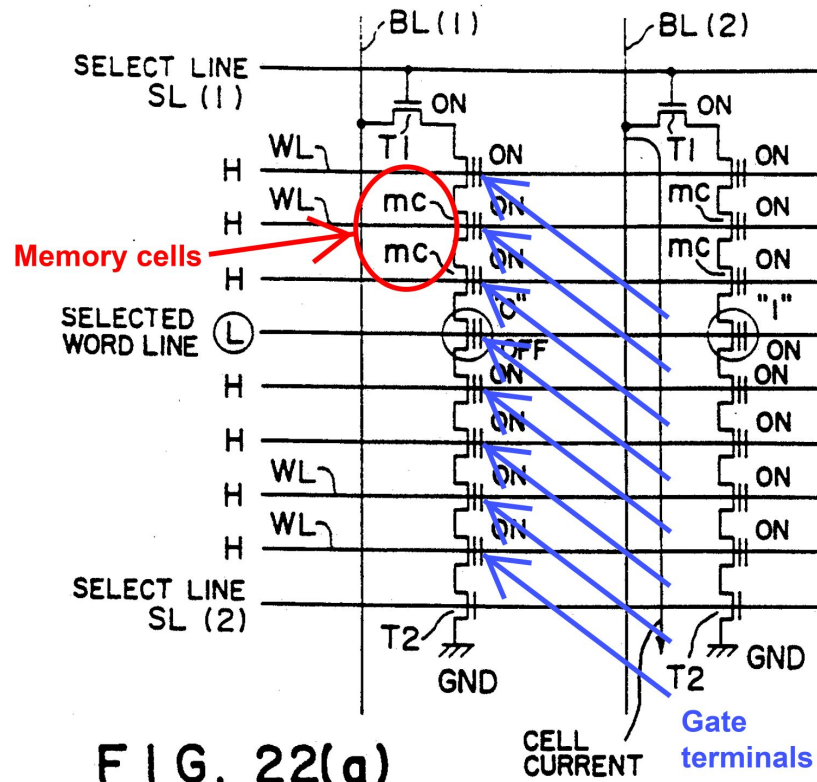
The above programming voltages disclosed in Nakai are summarized below, along with a summary of voltages recited in claims 1 and 4 of the '045 Patent:

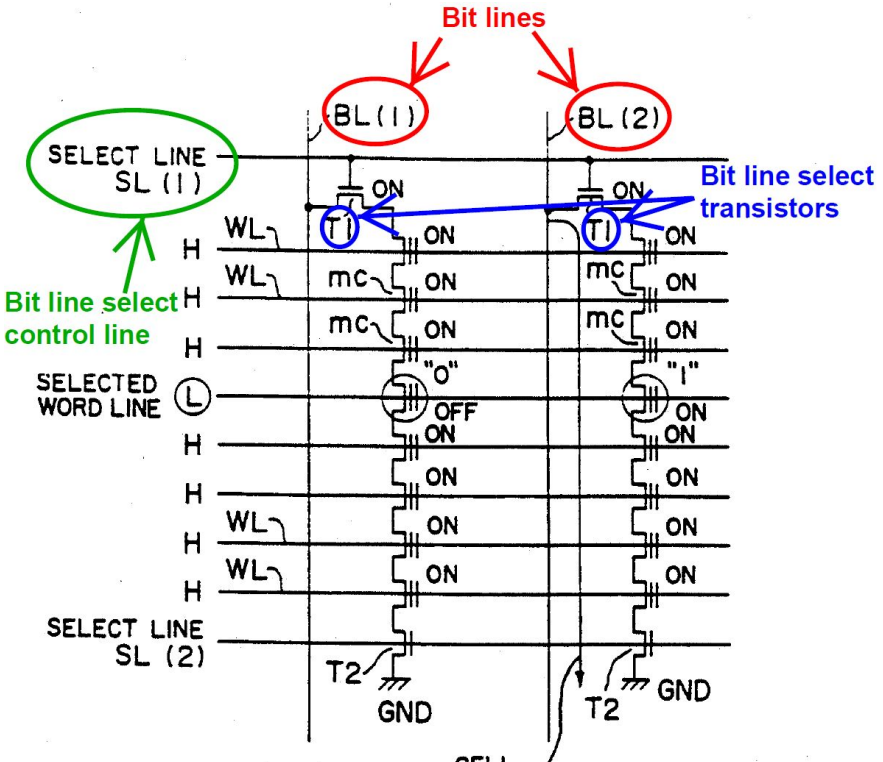
Array Element	Voltages – '045 Patent claims 1 & 4	Voltages – Nakai
BSL	Logic High	12 V on SL(1) – i.e. logic high
SSL	Logic Low	0 V on SL(2) – i.e. logic low
Selected Bit Line	Logic Low	0 V on BL(1) – i.e. logic low
Unselected Bit Lines	Logic High	VDPI (10V) on BL(2) – i.e. logic high
Selected Word Line	Boosted Positive	Vpp (20 V) on WL with Programmed Cell – i.e. boosted positive
Unselected Word Lines	Logic High	VPI (10V) on WL's without Programmed Cell – i.e. logic high

Therefore, Nakai anticipates both the memory array configuration as recited in claim 1, as well as the combination of programming voltages as recited in claims 1 and 4. Thus, claims 1 and 4 are invalid under 35 U.S.C. 102(b) (pre-AIA).

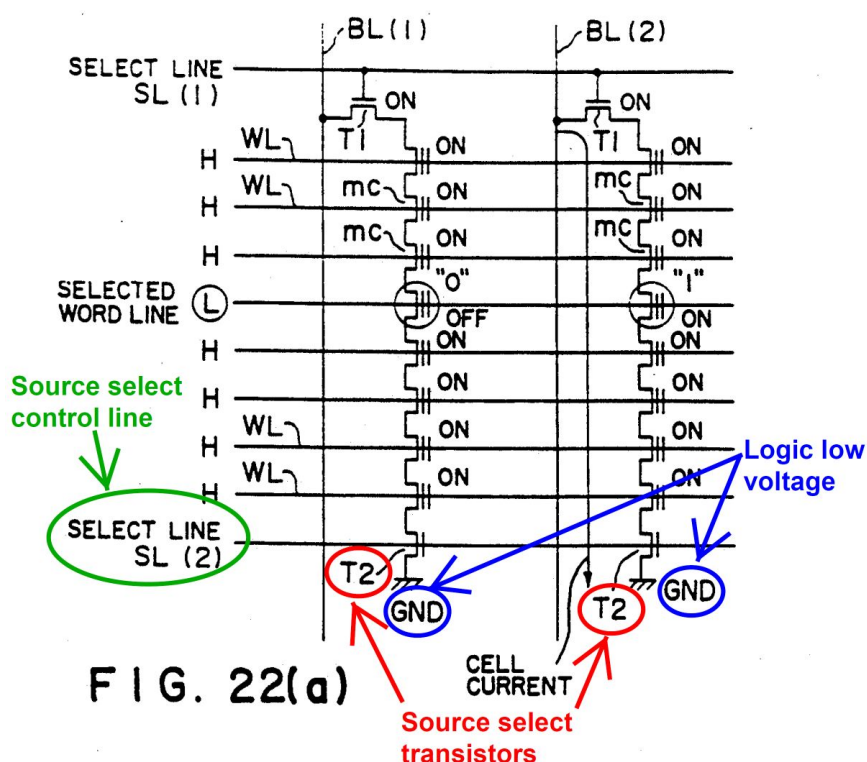
The following claim charts demonstrate, on a limitation-by-limitation basis, how claims 1 and 4 of the '045 Patent are anticipated by Nakai under 35 U.S.C. § 102(b) (pre-AIA).

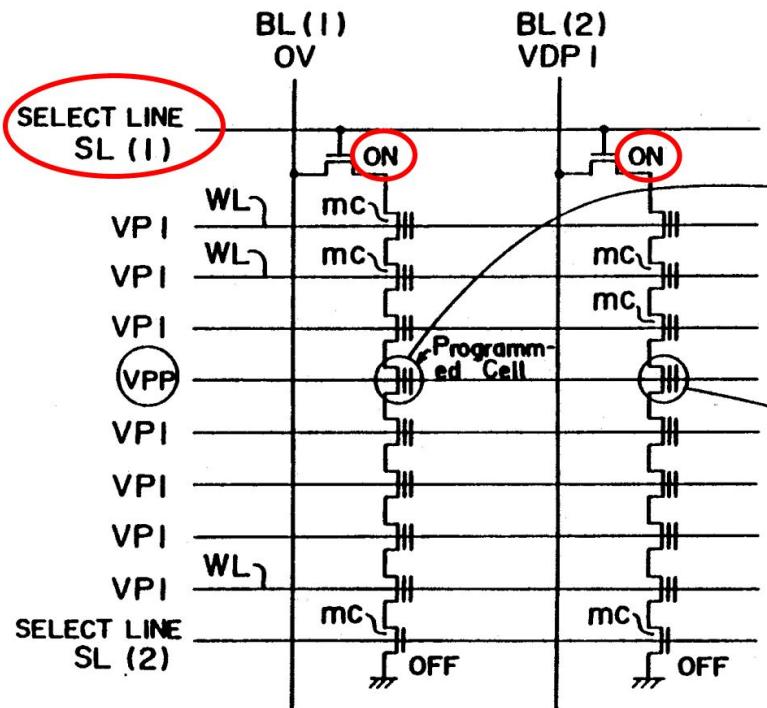
	U.S. Patent 6,058,045 - Claim 1	Correspondence to U.S. Patent No. 5,297,029 (Nakai)
Pre	1. An array of flash memory cells comprising:	Nakai discloses an array of flash memory cells: In recent electrically erasable and programmable read only memories (EEPROM), particularly <u>NAND type EEPROM, data can be read and written in unit of page</u> (256 bits to several thousands bits) because only a small current flows during data write and erase. NAND type non-volatile semiconductor memories having a capacity of 4 M bits are practically used nowadays (refer to 1988—ISSCC An Experimental 4 MB EEPROM with a NAND Structure Cell). 15 (TOSH-1005, 1:11-14.) It was well known in the art that NAND type EEPROMs were commonly referred to as “flash memory”. See at least for example the title, Abstract and disclosure in <i>A 35 ns Cycle Time 3.3 V Only 32 Mb NAND Flash EEPROM</i>, Yoshihisa Iwata et al, IEEE Journal of Solid-State Circuits (November 1995), which repeatedly refers to “NAND Flash EEPROM’s.” (TOSH-1007.) One skilled in the art would have understood that NAND type EEPROMs are flash memory cell arrays. (TOSH-1006, ¶22).

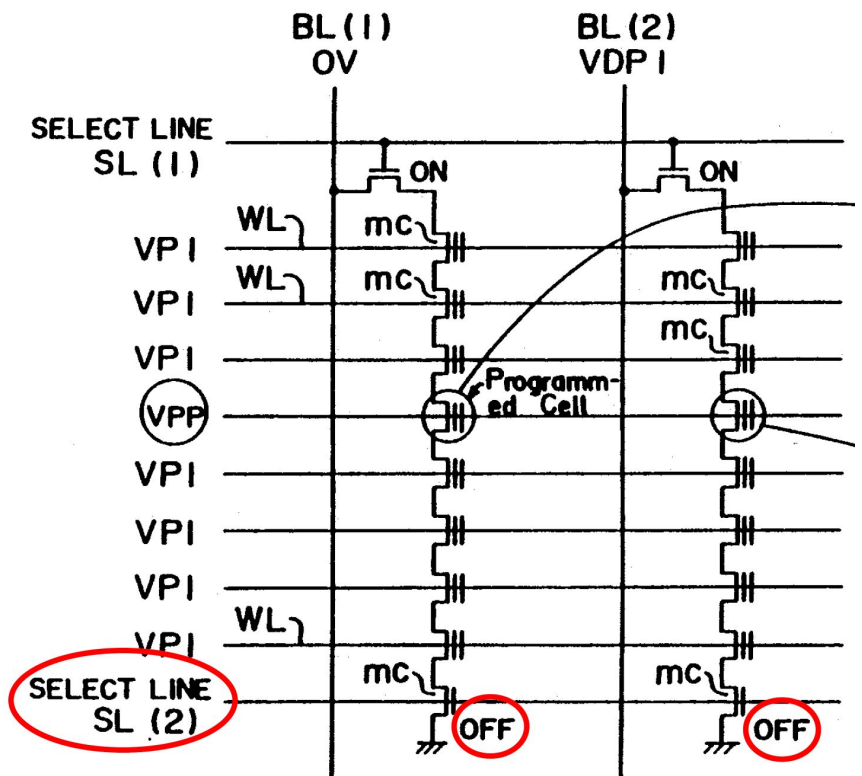
	U.S. Patent 6,058,045 - Claim 1	Correspondence to U.S. Patent No. 5,297,029 (Nakai)
1a	a plurality of columns of serially connected flash <u>memory cells</u> , each memory cell having a <u>gate terminal</u> ;	Nakai discloses columns of serially connected flash memory cells ("<u>MC</u>"), each memory cell MC has a gate terminal ("<u>select gate</u>"). FIG. 22(a) shows the structure of two NAND bundles each having <u>eight memory cells MC</u> of a floating gate structure and <u>connected between a bit line and a source</u>. The <u>select gate</u> of a memory cell selected for data read is set to a low level, and the select gates of remaining seven memory cells of the NAND bundle are set to a high level. The gate (select line SL(1)) of a (TOSH-1005, 1:20-26.)  FIG. 22(a) (TOSH-1005, FIG. 22(a).) See also TOSH-1005, FIG. 23(a).

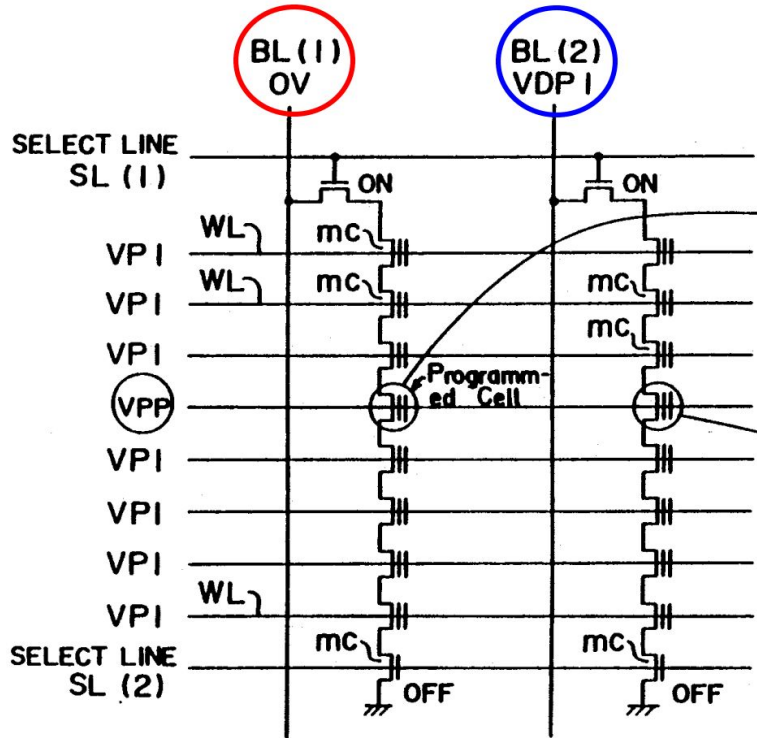
	U.S. Patent 6,058,045 - Claim 1	Correspondence to U.S. Patent No. 5,297,029 (Nakai)
1b	a plurality of bit lines respectively coupled to drain side of said plurality of columns of memory cells via a respective plurality of bit line select transistors, said plurality of bit line select transistors having gate terminals coupled to a bit line select control line;	Nakai discloses a plurality of bit lines ("BL") respectively coupled to the drain side of the memory cell columns via respective bit line select transistors ("T1") which have gate terminals coupled to a bit line select control line ("Select Line SL(1)"). FIG. 22(a) shows the structure of two NAND bundles each having eight memory cells MC of a floating gate structure and connected between a bit line and a source. The select gate of a memory cell selected for data read is set to a low level, and the select gates of remaining seven memory cells of the NAND bundle are set to a high level. The gate (select line SL(1)) of a select transistor T1 connected between the bit line and the NAND bundle, and the gate (select line SL(2)) of a select transistor T2 connected between ground GND and the NAND bundle, are both set to a high level. In (TOSH-1005, 1:20-30.)  FIG. 22(a) (TOSH-1005, FIG. 22(a).) See also TOSH-1005, FIG. 23(a).

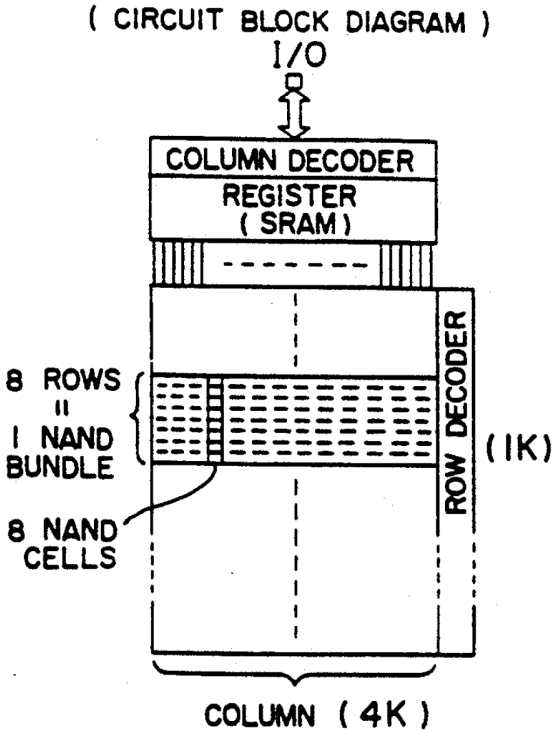
	U.S. Patent 6,058,045 - Claim 1	Correspondence to U.S. Patent No. 5,297,029 (Nakai)
1c	a plurality of <u>word lines</u> , each one coupling to a <u>gate terminal</u> of one memory cell in each of said plurality of columns to form rows of memory cells with common gate terminals; and	Nakai discloses a plurality of word lines ("<u>WL</u>") each coupled to a gate terminal (i.e. "<u>select gate</u>") of one memory cell in each of the plurality of columns to form rows of memory cells with common gate terminals. FIG. 22(a) shows the structure of two NAND bundles each having eight memory cells MC of a floating gate structure and connected between a bit line and a source. <u>The select gate of a memory cell selected for data read is set to a low level, and the select gates of remaining seven memory cells of the NAND bundle are set to a high level.</u> The gate (select line SL(1)) of a (TOSH-1005, 1:20-26.) FIG. 22(a) (TOSH-1005, FIG. 22(a).) See also TOSH-1005, FIG. 23(a).

	U.S. Patent 6,058,045 - Claim 1	Correspondence to U.S. Patent No. 5,297,029 (Nakai)
1d	a plurality of <u>source select transistors</u> respectively coupling a source side of said plurality of columns of memory cells to a <u>logic low voltage</u>, and having gate terminals coupled to a <u>source select control line</u>,	Nakai discloses a plurality of source select transistors (“T2”) that respectively couple the source side of the columns of memory cells to a logic low voltage (“ground”), and which have gate terminals coupled to a source select control line (“SL(2)”). FIG. 22(a) shows the structure of two NAND bundles each having eight memory cells MC of a floating gate structure and connected between a bit line and a source. The select gate of a memory cell selected for data read is set to a low level, and the select gates of remaining seven memory cells of the NAND bundle are set to a high level. The gate (select line SL(1)) of a select transistor T1 connected between the bit line and the NAND bundle, and the gate (select line SL(2)) of a <u>select transistor T2 connected between ground GND and the NAND bundle</u>, are both set to a high level. In 30 (TOSH-1005, 1:20-30.)  FIG. 22(a) (TOSH-1005, FIG. 22(a).) See also TOSH-1005, FIG. 23(a).

	U.S. Patent 6,058,045 - Claim 1	Correspondence to U.S. Patent No. 5,297,029 (Nakai)
1e	wherein, during programming:	Col. 1, lines 46 to col. 2, line 9, and Fig. 23(a) of Nakai describes a program operation. <u>Next, the write operation will be described. As shown in FIG. 23(a), a high voltage (V_{pp}) of about 20 V</u> (TOSH-1005, 1:46-52; Fig. 23(a).)
1f	a logic high voltage is applied to said bit line select control line to turn on bit line select transistors,	Nakai discloses applying a logic high voltage (i.e. “12 V”) to the bit line select control line to turn on the bit line select transistors. <u>The gate voltage of the select transistor between the NAND bundle containing the selected memory cell and the bit line is set to 12 V, and the gate voltage of the</u> 55 <u>select transistor between the NAND bundle and the source line is set to 0 V. When the bit line is set to 0 V</u> (TOSH-1005, 1:53-57.)  FIG. 23(a) (TOSH-1005, FIG. 23(a).)

	U.S. Patent 6,058,045 - Claim 1	Correspondence to U.S. Patent No. 5,297,029 (Nakai)
1g	a logic low voltage is applied to source select control line to turn off source select transistors;	Nakai discloses applying a logic low voltage (i.e. "0 V") to the source select control line to turn off the source select transistors. The gate voltage of the select transistor between the NAND bundle containing the selected memory cell and the bit line is set to 12 V, and the gate voltage of the 55 select transistor between the NAND bundle and the source line is set to 0 V. When the bit line is set to 0 V (TOSH-1005, 1:53-57.)  FIG. 23(a) (TOSH-1005, FIG. 23(a).)

	U.S. Patent 6,058,045 - Claim 1	Correspondence to U.S. Patent No. 5,297,029 (Nakai)
1h	a logic low voltage is applied to a selected bit line while a logic high voltage is applied to unselected bit lines, and	Nakai discloses applying a logic low voltage (i.e. "0V") to the selected bit line (BL(1)) while applying a logic high voltage (i.e. "VDPI" which is "10V") to unselected bit lines (BL(2)). source line is set to 0 V. <u>When the bit line is set to 0 V in this condition, the potentials of the drain, source, and channel of all the memory cells in the NAND bundle selected by the select transistors, become 0 V.</u> There- 60 (TOSH-1005, 1:57-60.) If a write inhibit drain voltage (VDPI) of about 10 V is applied to the bit line, the potential difference between 5 the select gate and channel of the selected memory cell becomes 10 V, and data write is not effected. In the (TOSH-1005, 2:3-6.)  FIG. 23(a) (TOSH-1005, FIG. 23(a).)

	U.S. Patent 6,058,045 - Claim 1	Correspondence to U.S. Patent No. 5,297,029 (Nakai)
		It is inherent from Nakai that Figs. 22(a) and 23(a) show only a portion of the full array, and additional columns of memory cells each connected to its own bit line are included in the full array. (TOSH-1006, ¶23). 25 FIG. 25 illustrates the operation modes of a practically used 4 M NAND structure semiconductor memory. <u>As shown in FIG. 25(a), 512 bits * 8 (I/O)=4096 bit lines are laid out in the column direction, and 128 NAND bundles * 8 bits=1024 word lines are laid out in the row direction.</u> 30 <u>In writing data in this memory, data</u> (TOSH-1005, 2:25-30.) See Fig. 25(a) showing the plurality of columns of memory cells. (CIRCUIT BLOCK DIAGRAM)  FIG. 25(a) (TOSH-1005, FIG. 25(a).)

	U.S. Patent 6,058,045 - Claim 1	Correspondence to U.S. Patent No. 5,297,029 (Nakai)
		It is also inherent that additional bit lines beyond BL(2) in Figs. 22(a) and 23(a) that were not intended to be programmed would have the same voltage (i.e. VDPI) as that being applied to BL(2), so that memory cells in those columns (i.e. “non-write cells”) are not programmed. (TOSH-1006, ¶24). FIG. 23(a) FIG. 23(b) (VDPI : WRITE INHIBITED DRAIN VOLTAGE) FIG. 23(c) (TOSH-1005, FIGS. 23(a)-23(c).) Therefore, one skilled in the art would have understood that Nakai discloses a logic low voltage is applied to a selected bit line while a logic high voltage is applied to unselected bit lines. (TOSH-1006, ¶24).

	U.S. Patent 6,058,045 - Claim 1	Correspondence to U.S. Patent No. 5,297,029 (Nakai)
1i	a logic high voltage is applied to unselected word lines, while a boosted positive voltage is applied to a selected word line.	Nakai discloses applying a logic high voltage (i.e. “VPI” which is “about 10 V”) to unselected word lines, while applying a boosted positive voltage (i.e. “Vpp” which is “about 20 V”) to a selected word line. Next, the write operation will be described. As shown in FIG. 23(a), a high voltage (V_{DD}) of about 20 V is applied from a row decoder to the select gate of a selected memory cell, and an intermediate voltage (VPI) of about 10 V is applied to the select gates of the other seven memory cells of the NAND bundle 0 V is applied to the select gates of the other NAND bundle. (TOSH-1005, 1:46-52.) FIG. 23(a) (TOSH-1005, FIG. 23(a).)

	U.S. Patent 6,058,045 - Claim 4	Correspondence to U.S. Patent No. 5,297,029 (Nakai)
Pre	4. A method of operating a flash memory device wherein programming memory cells is accomplished by the steps of:	Nakai discloses a method of operating a flash memory device involving the programming of memory cells. Nakai discloses an array of flash memory cells: In recent electrically erasable and programmable read only memories (EEPROM), particularly <u>NAND type EEPROM</u>, data can be read and written in unit of page (256 bits to several thousands bits) because only a small current flows during data write and erase. NAND ¹⁵ type non-volatile semiconductor memories having a capacity of 4 M bits are practically used nowadays (refer to 1988—ISSCC An Experimental 4 MB EEPROM with a NAND Structure Cell). (TOSH-1005, 1:11-14.) It was well known in the art that NAND type EEPROMs were commonly referred to as “flash memory”. See at least for example the title, Abstract and disclosure in <i>A 35 ns Cycle Time 3.3 V Only 32 Mb NAND Flash EEPROM</i>, Yoshihisa Iwata et al, IEEE Journal of Solid-State Circuits (November 1995), which repeatedly refers to “NAND Flash EEPROM’s.” (TOSH-1007.) Col. 1, lines 46 to col. 2, line 9, and Fig. 23(a) of Nakai describes a program operation of memory cells. <u>Next, the write operation will be described. As shown in FIG. 23(a), a high voltage (V_{pp}) of about 20 V</u> (TOSH-1005, 1:46-52; Fig. 23(a).) One skilled in the art would have understood that Nakai discloses a method of operating a flash memory device by programming memory cells. (TOSH-1006, ¶22).

	U.S. Patent 6,058,045 - Claim 4	Correspondence to U.S. Patent No. 5,297,029 (Nakai)
4a	applying a logic high voltage to a bit line select control line to turn on bit line select transistors,	See 1f for claim 1 above.
4b	applying a logic low voltage to a source select control line to turn off source select transistors;	See 1g for claim 1 above.
4c	applying a <u>logic low</u> voltage to a <u>selected bit line</u> while a <u>logic high</u> voltage is applied to <u>unselected bit lines</u> , and	See 1h for claim 1 above.
4d	applying a <u>logic high</u> voltage to <u>unselected word lines</u> , while a <u>boosted positive</u> voltage is applied to a <u>selected word line</u> .	See 1i for claim 1 above.

ii. **Challenge #2: Claims 1 and 4 are anticipated by the 1993 Databook**

Claims 1 and 4 of the '045 Patent are anticipated and rendered invalid by the 1993 Databook under 35 U.S.C. 102(b) (pre-AIA). The 1993 Databook discloses a CMOS NAND E2PROM electrically erasable and programmable nonvolatile memory (TC584000P/F/FT/TR). (TOSH-1009, pp. 367-380.) As shown in Fig. 2 (p. 379), the memory includes columns of memory cells connected in series to each other, with each column connected at the top to a bit line via a select transistor and at the bottom to ground via a select transistor. Select Line 1 and Select Line 2 operate the row of select transistors to the bit lines and the row of select transistors to ground, respectively. The array includes word lines that each connect to the gates of one of the memory cells from each column:

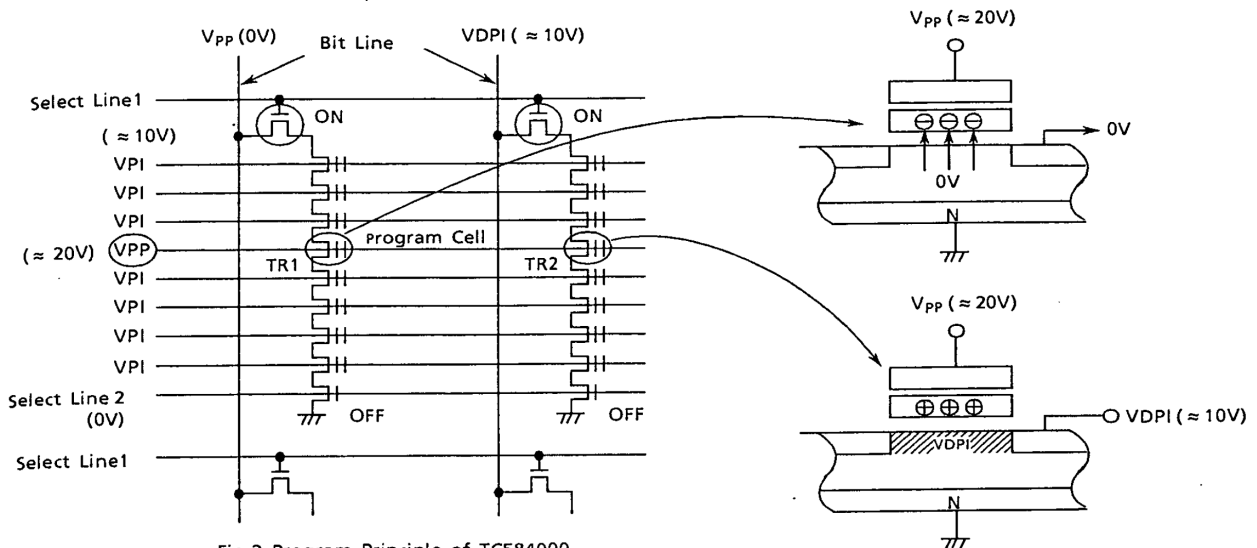
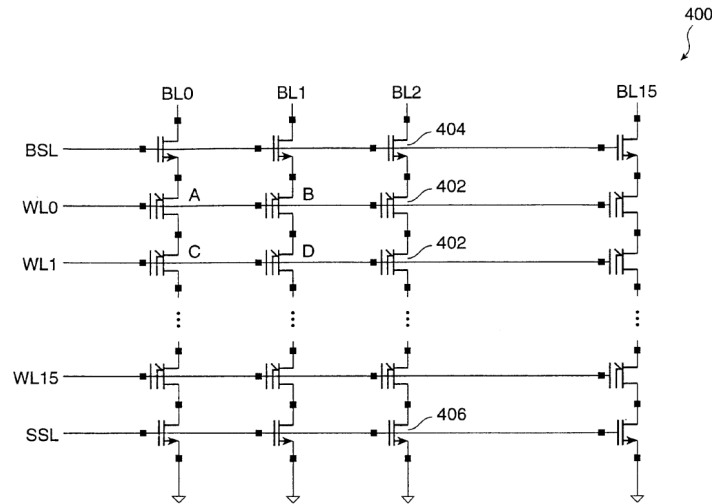


Fig.2 Program Principle of TC584000

(TOSH-1009, Fig. 2 at p. 379.)

The above configuration is essentially the same as the memory array configuration disclosed and claimed in the '045 Patent:



(TOSH-1001, Fig. 4.)

The programming of the array in the 1993 Databook is described on page 378 and shown in Fig. 2 on page 379. (TOSH-1009, pp. 378-379.) Specifically, for programming the selected cell labeled “Program Cell” in Fig. 2, the select line 1 is given “H” level (i.e. logic high) and the select line 2 is given “L” level (0V) (i.e. logic low), so that the 8 cells in the column are connected to the bit line (i.e. bit line select transistors are “on”) and isolated from ground (i.e. the source line select transistors are “off”). (TOSH-1009, p. 378, Fig. 2 on p. 379). The word line for the selected cell (i.e. the selected word line) is placed at voltage V_{pp} , while the remaining word lines (i.e. the unselected word lines) are placed at V_{PI} . (TOSH-1009, p. 378, Fig. 2 on p. 379). V_{pp} is a high voltage of “approximately 20 V” (i.e. a boosted positive voltage). (TOSH-1009, p. 378.) V_{PI} is a voltage of

“approximately 10 V” (i.e. a logic high voltage). (TOSH-1009, p. 378.) The bit line for the selected cell (i.e. the selected bit line) is placed at 0V (i.e. a logic low voltage), while the remaining bit lines (i.e. the unselected bit lines) are placed at a voltage of VDPI. (TOSH-1009, p. 378, Fig. 2 on p. 379.) VDPI is a voltage of “approximately 10 V” (i.e. a logic high voltage). (TOSH-1009, p. 378.)

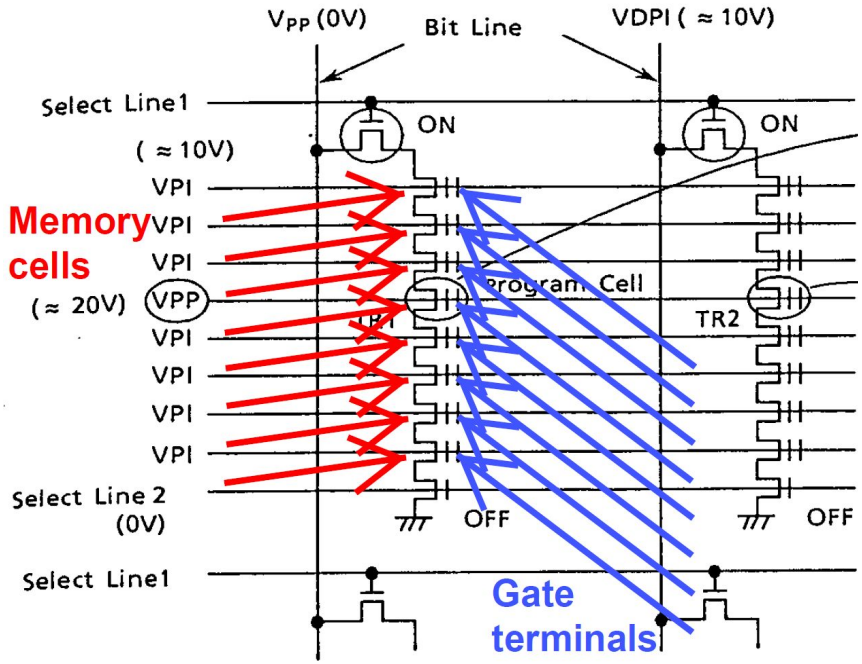
The above programming voltages disclosed in the 1993 Databook are summarized below, along with a summary of voltages recited in claims 1 and 4 of the '045 Patent:

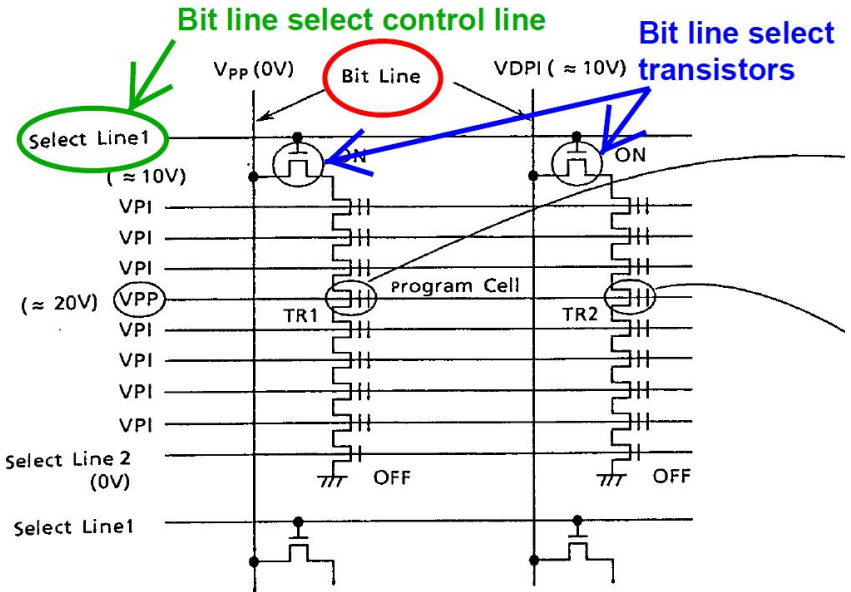
Array Element	Voltages – '045 Patent claims 1 & 4	Voltages – 1993 Databook
BSL	Logic High	H level on Select Line 1– i.e. logic high
SSL	Logic Low	L level (0V) on Select Line 2– i.e. logic low
Selected Bit Line	Logic Low	0 V – i.e. logic low
Unselected Bit Lines	Logic High	VDPI (~10V) – i.e. logic high
Selected Word Line	Boosted Positive	Vpp (~20 V) on WL containing “Program Cell”– i.e. boosted positive
Unselected Word Lines	Logic High	VPI (~10V) on WL’s not containing “Program Cell” – i.e. logic high

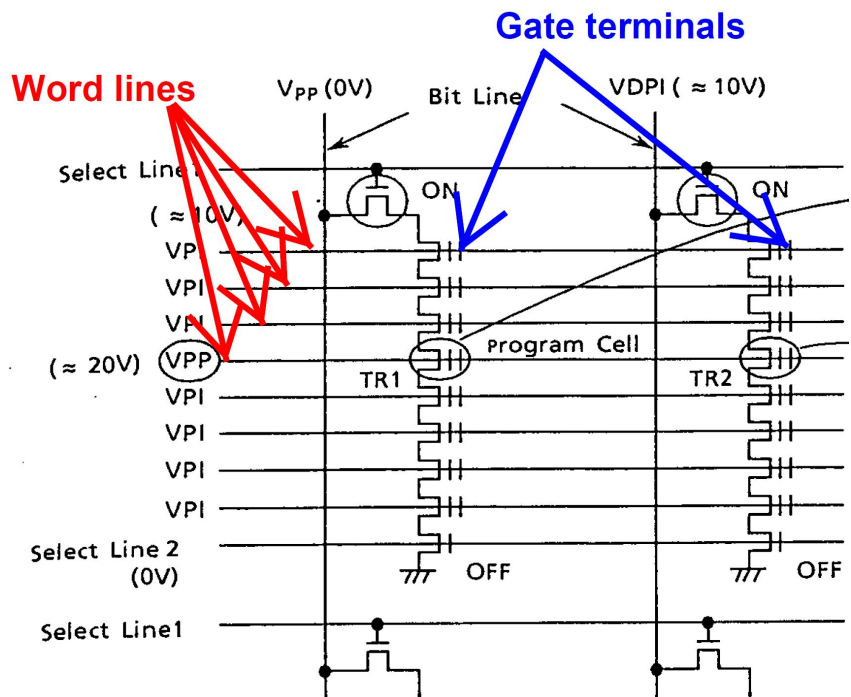
Therefore, the 1993 Databook anticipates both the memory array configuration as recited in claim 1, as well as the combination of programming voltages as recited in claims 1 and 4. Thus, claims 1 and 4 are invalid under 35 U.S.C. 102(b) (pre-AIA).

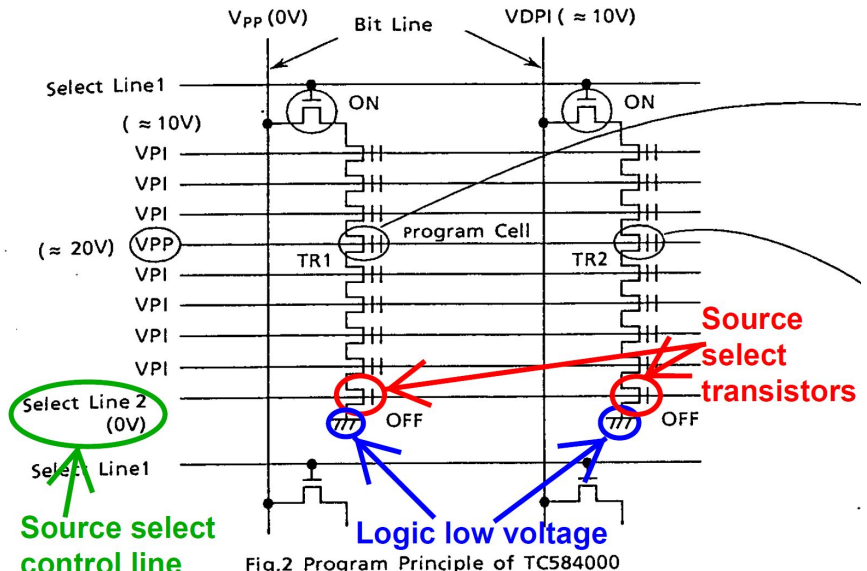
The following claim charts demonstrate, on a limitation-by-limitation basis, how claims 1 and 4 of the '045 Patent are anticipated by the 1993 Databook under 35 U.S.C. § 102(b) (pre-AIA).

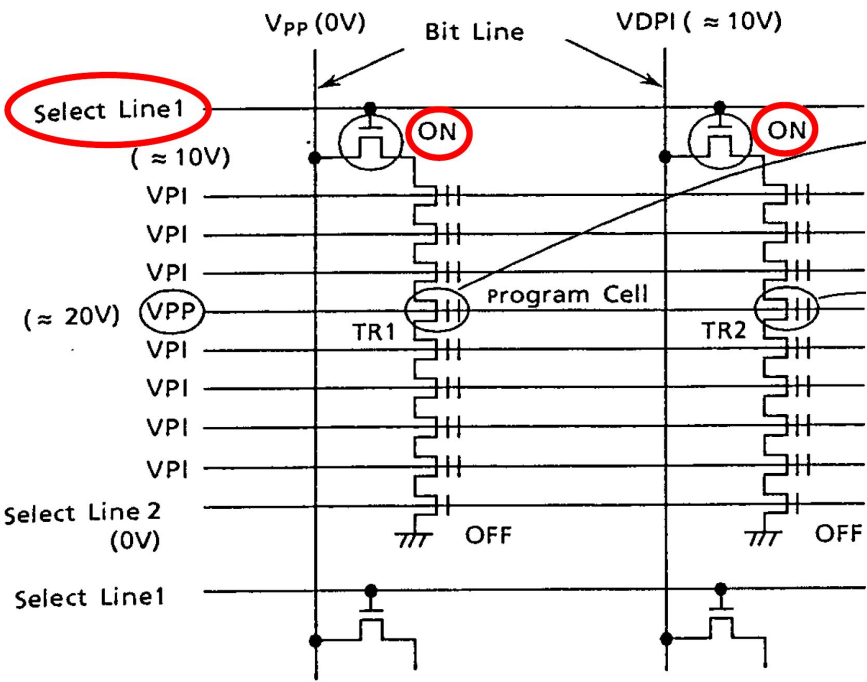
	U.S. Patent 6,058,045 - Claim 1	Correspondence to the 1993 Databook
Pre	1. An array of flash memory cells comprising:	The 1993 Databook discloses an array of flash memory cells: 4MEGA BIT (524,288 WORD×8 BIT) <u>CMOS NAND E²PROM</u> <u>DESCRIPTION</u> The TC584000P/F/FT/TR is a 4M bits electrically erasable and programmable nonvolatile memory equipped with a 512K×8 nonvolatile memory array and a 512K×8 data register, which can operate with a single 5V power supply. It has a 512-byte data register inside. A program operation and a read operation are performed by transferring the 512 byte page of data between the register and the memory cell array. Data in the register can be clocked out at a very high speed during page read operations. <u>An erase operation can be performed on either a 4K-byte block or the whole chip.</u> <u>The TC584000P/F/FT/TR is suitable for large capacity buffer memory applications such as semiconductor disk, voice recording and replaying, digital still camera, and so on where nonvolatility is necessary.</u> (TOSH-1009, p. 378.) It was well known in the art that NAND type E²PROMs were commonly referred to as “flash memory”. See at least for example the title, Abstract and disclosure in <i>A 35 ns Cycle Time 3.3 V Only 32 Mb NAND Flash EEPROM</i>, Yoshihisa Iwata et al, IEEE Journal of Solid-State Circuits (November 1995), which repeatedly refers to “NAND Flash EEPROM’s.” TOSH-1007. One skilled in the art would have understood that NAND type E²PROMs are flash memory cell arrays. (TOSH-1006, ¶26).

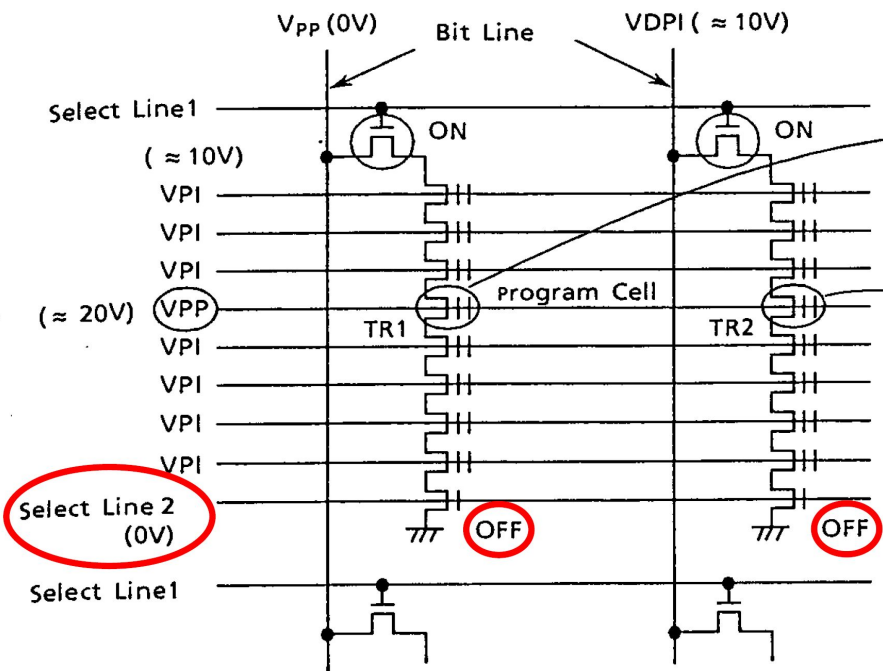
	U.S. Patent 6,058,045 - Claim 1	Correspondence to the 1993 Databook
1a	a plurality of columns of serially connected flash memory cells , each memory cell having a gate terminal ;	The 1993 Databook discloses columns of serially connected flash memory cells, each memory cell has a gate terminal.  Fig.2 Program Principle of TC584000 (TOSH-1009, Fig. 2 on p. 379.)

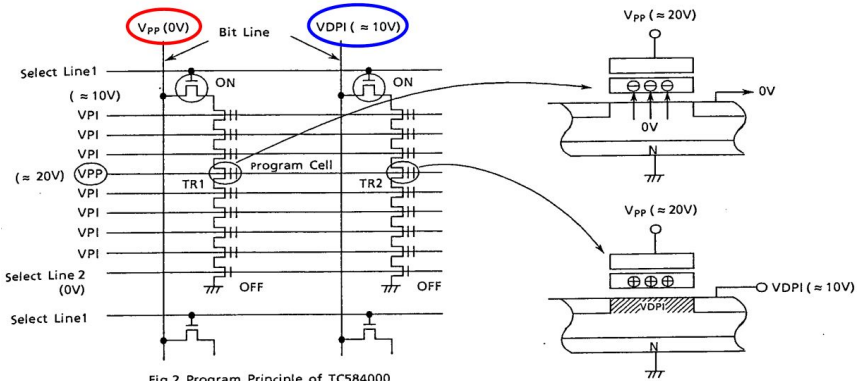
	U.S. Patent 6,058,045 - Claim 1	Correspondence to the 1993 Databook
1b	a plurality of bit lines respectively coupled to drain side of said plurality of columns of memory cells via a respective plurality of bit line select transistors, said plurality of bit line select transistors having gate terminals coupled to a bit line select control line;	The 1993 Databook discloses a plurality of bit lines (“Bit Line”) respectively coupled to the drain side of the memory cell columns via respective bit line select transistors which have gate terminals coupled to a bit line select control line (“Select Line 1”).  Fig.2 Program Principle of TC584000 (TOSH-1009, Fig. 2 on p. 379.)

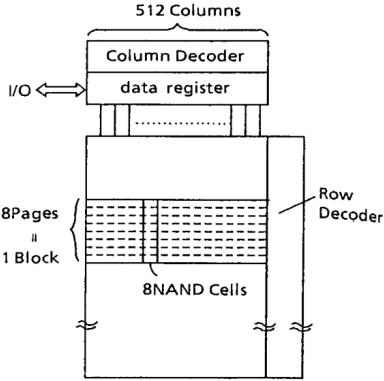
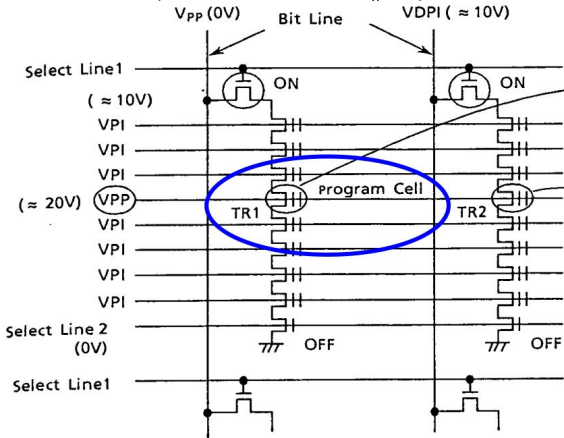
	U.S. Patent 6,058,045 - Claim 1	Correspondence to the 1993 Databook
1c	a plurality of <u>word lines</u> , each one coupling to a <u>gate terminal</u> of one memory cell in each of said plurality of columns to form rows of memory cells with common gate terminals; and	The 1993 Databook discloses a plurality of word lines each coupled to a gate terminal of one memory cell in each of the plurality of columns to form rows of memory cells with common gate terminals.  Fig.2 Program Principle of TC584000 (TOSH-1009, Fig. 2 on p. 379.)

	U.S. Patent 6,058,045 - Claim 1	Correspondence to the 1993 Databook
1d	a plurality of <u>source select transistors</u> respectively coupling a source side of said plurality of columns of memory cells to a <u>logic low voltage</u> , and having gate terminals coupled to a <u>source select control line</u> ,	The 1993 Databook discloses a plurality of source select transistors that respectively couple the source side of the columns of memory cells to a logic low voltage (ground), and which have gate terminals coupled to a source select control line (“Select Line 2”).  Fig.2 Program Principle of TC584000 (TOSH-1009, Fig. 2 on p. 379.)
1e	wherein, during programming:	Page 378, and Fig. 2 on page 379 of the 1993 Databook describes a program operation. OPERATION PRINCIPLE <u>PROGRAM OPERATION</u> <u>Fig. 2 shows the program operation principle of the TC584000P/F/FT/TR.</u> (TOSH-1009, p. 378 and Fig. 2 on p. 379.)

	U.S. Patent 6,058,045 - Claim 1	Correspondence to the 1993 Databook
1f	a logic high voltage is applied to said bit line select control line to turn on bit line select transistors,	The 1993 Databook discloses applying a logic high voltage (i.e. “H level”) to the bit line select control line to turn on the bit line select transistors. <u>The select line 1 is given ‘H’ level and the select line 2 is given ‘L’ level so that 8 cells in the NAND are connected to the bit line and isolated from GND. Then V_{pp} (approximately 20V) is given to the word line of the selected page and V_{pi} (approximately 10V) is given to the word line of the other unselected pages.</u> (TOSH-1009, p. 178.)  Fig.2 Program Principle of TC584000 (TOSH-1009, Fig. 2 on page 379.)

	U.S. Patent 6,058,045 - Claim 1	Correspondence to the 1993 Databook
1g	a logic low voltage is applied to source select control line to turn off source select transistors;	The 1993 Databook discloses applying a logic low voltage (i.e. “L level,” “0V”) to the source select control line to turn off the source select transistors. <u>The select line 1 is given ‘H’ level and the select line 2 is given ‘L’ level so that 8 cells in the NAND are connected to the bit line and isolated from GND.</u> Then Vpp (approximately 20V) is given to the word line of the selected page and Vpi (approximately 10V) is given to the word line of the other unselected pages. (TOSH-1009, p. 378.)  Fig.2 Program Principle of TC584000 (TOSH-1009, Fig. 2 on page 379.)

	U.S. Patent 6,058,045 - Claim 1	Correspondence to the 1993 Databook
1h	a logic low voltage is applied to a selected bit line while a logic high voltage is applied to unselected bit lines, and	The 1993 Databook discloses applying a logic low voltage (i.e. “0V”) to the selected bit line (i.e. the bit line containing TR1) while applying a logic high voltage (i.e. “VDPI” which is “~10V”) to unselected bit lines (i.e. the bit line not containing TR1). On the other hand, 0V is given to the bit line connected to the NAND that has TR1 in which data ‘0’ is going to be programmed and V_{DDI} (approximately 10V) is given to the bit line connected to the NAND that has TR2 in which data ‘1’ is going to be programmed. (TOSH-1009, p. 378.) TR1 is shown to be the cell that is programmed with the “0” data, whereas TR2 is shown to be the cell that is not programmed (i.e. it retains the “1” data from the previous erase):  Fig.2 Program Principle of TC584000 (TOSH-1009, Fig. 2 on page 379.) PROGRAM OPERATION Fig. 2 shows the program operation principle of the TC584000P/F/FT/TR. The program operation is to program data ‘0’s into cells in the erased state (data ‘1’) by employing tunneling phenomenon. The (TOSH-1009, Fig. 2 on page 379.) It is inherent from the 1993 Databook that Fig. 2 shows only a portion of the full array, and that additional columns of memory cells each connected to its own bit line are included in the full array. (TOSH-1006, ¶27). FEATURES Organization Memory Cell Array : 512K × 8 Register : 512 × 8 (TOSH-1009, p. 367.)

	U.S. Patent 6,058,045 - Claim 1	Correspondence to the 1993 Databook
		 Fig.1 Structure of TC584000 (TOSH-1009, Fig. 1 on page 376.) It is also inherent that additional bit lines beyond the two bit lines shown in Fig. 2 that were not intended to be programmed (i.e. to be left as data “1”) would have the same voltage (i.e. VDPI) as that being applied to the second bit line (i.e. the bit line on the right in Fig. 2), so that memory cells in those columns are not programmed with the ‘0’ data. (TOSH-1006, ¶28).  Fig.2 Program Principle of TC584000 (TOSH-1009, Fig. 2 on page 379.) Therefore, one skilled in the art would have understood that the 1993 Databook discloses a logic low voltage is applied to a selected bit line while a logic high voltage is applied to unselected bit lines. (TOSH-1006, ¶28).

	U.S. Patent 6,058,045 - Claim 1	Correspondence to the 1993 Databook
1i	a logic high voltage is applied to unselected word lines, while a boosted positive voltage is applied to a selected word line.	The 1993 Databook discloses applying a logic high voltage (i.e. “VPI” which is “approximately 10 V”) to unselected word lines, while applying a boosted positive voltage (i.e. “Vpp” which is “approximately 20 V”) to a selected word line. are connected to the bit line and isolated from GND. <u>Then Vpp (approximately 20V) is given to the word line of the selected page and Vpi (approximately 10V) is given to the word line of the other unselected pages.</u> (TOSH-1009, p. 378.) Fig.2 Program Principle of TC584000 (TOSH-1009, FIG. 2 on page 379.)

	U.S. Patent 6,058,045 - Claim 4	Correspondence to the 1993 Databook
Pre	4. A method of operating a flash memory device wherein programming memory cells is accomplished by the steps of:	The 1993 Databook discloses a method of operating a flash memory device involving the programming of memory cells. The 1993 Databook discloses an array of flash memory cells: 4MEGA BIT (524,288 WORD×8 BIT) <u>CMOS NAND E²PROM</u> <u>DESCRIPTION</u> The TC584000P/F/FT/TR is a 4M bits electrically erasable and programmable nonvolatile memory equipped with a 512K×8 nonvolatile memory array and a 512K×8 data register, which can operate with a single 5V power supply. It has a 512-byte data register inside. A program operation and a read operation are performed by transferring the 512 byte page of data between the register and the memory cell array. Data in the register can be clocked out at a very high speed during page read operations. <u>An erase operation can be performed on either a 4K-byte block or the whole chip.</u> The TC584000P/F/FT/TR is suitable for large capacity buffer memory applications such as semiconductor disk, voice recording and replaying, digital still camera, and so on where nonvolatility is necessary. (TOSH-1009, p. 378.) It was well known in the art that NAND type E²PROMs were commonly referred to as “flash memory”. See at least for example the title, Abstract and disclosure in <i>A 35 ns Cycle Time 3.3 V Only 32 Mb NAND Flash EEPROM</i>, Yoshihisa Iwata et al, IEEE Journal of Solid-State Circuits (November 1995), which repeatedly refers to “NAND Flash EEPROM’s.” (TOSH-1007.) Page 378, and Fig. 2 on page 379 of the 1993 Databook describes a program operation. OPERATION PRINCIPLE <u>PROGRAM OPERATION</u> <u>Fig. 2 shows the program operation principle of the TC584000P/F/FT/TR.</u> (TOSH-1009, p. 378 and Fig. 2 on p. 379.) One skilled in the art would have understood that the 1993 Databook discloses a method of operating a flash memory device by programming memory cells. (TOSH-1006, ¶26).

	U.S. Patent 6,058,045 - Claim 4	Correspondence to the 1993 Databook
4a	applying a logic high voltage to a bit line select control line to turn on bit line select transistors,	See 1f for claim 1 above.
4b	applying a logic low voltage to a source select control line to turn off source select transistors;	See 1g for claim 1 above.
4c	applying a <u>logic low</u> voltage to a <u>selected bit line</u> while a <u>logic high</u> voltage is applied to <u>unselected bit lines</u> , and	See 1h for claim 1 above.
4d	applying a <u>logic high</u> voltage to <u>unselected word lines</u> , while a <u>boosted positive</u> voltage is applied to a <u>selected word line</u> .	See 1i for claim 1 above.

V. Conclusion

Petitioner has established that claims 1 and 4 of the '045 Patent are invalid as anticipated by prior art not yet considered by the Patent Office for the reasons set forth above. There is a reasonable likelihood that Petitioner will prevail as to each of the claims. Therefore, Petitioner requests that the Patent Office order an *inter partes* review trial, and then proceed to cancel claims 1 and 4 of the '045 Patent.

VI. Payment of Fees

The undersigned authorizes payment for any additional fees that might be due in connection with this Petition, or any credit for overpayment, to Deposit Account No. 07-1896 referencing Attorney Docket No. 351912-22.045.

Respectfully submitted,

Dated: October 31, 2013

/Alan A. Limbach/

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CERTIFICATE OF SERVICE

The undersigned certifies service pursuant to 37 C.F.R. 37 C.F.R. §§ 42.6(e) and 42.105(b) on the Patent Owner by Express Mail of a copy of this Petition for *Inter Partes* Review and supporting materials at the following correspondence address of record for the '045 Patent:

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