

IPR2014-00113  
U.S. Patent No. 6,058,045  
Patent Owner Dkt. No. 3059.702IPR2

**UNITED STATES PATENT AND TRADEMARK OFFICE**

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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TOSHIBA CORPORATION  
Petitioner

v.

INTELLECTUAL VENTURES I LLC  
Patent Owner

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Case IPR2014-00113  
U.S. Patent No. 6,058,045

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**PATENT OWNER PRELIMINARY RESPONSE**

Mail Stop PATENT BOARD  
Patent Trial and Appeal Board  
U.S. Patent & Trademark Office  
P.O. Box 1450  
Alexandria, VA 22313-1450

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## **I. Introduction**

The Patent Trial and Appeal Board can, at its discretion, decline to initiate trial over unpatentability grounds that are redundant to other grounds. *See* 37 C.F.R. § 42.108(b). Here, the petitioner Toshiba proposed two grounds of unpatentability that rely on nearly identical references. Toshiba did not articulate any differences between them or explain their relative strengths and weaknesses. Thus, in the “interest of a just, speedy, and inexpensive” resolution, the Board should deny at least one of these grounds.

## **II. Overview of Toshiba’s Petition**

Toshiba proposes two grounds of alleged unpatentability for the ’045 patent: (1) claims 1 and 4 are allegedly anticipated under 35 U.S.C. § 102(b) by the Nakai patent<sup>1</sup> (the “First Ground”), and (2) claims 1 and 4 are allegedly anticipated under 35 U.S.C. § 102(b) by the 1993 Databook<sup>2</sup> (the “Second Ground”). Circuit

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<sup>1</sup> U.S. Patent No. 5,297,029 to Nakai et al. (TOSH-1005) (“Nakai”).

<sup>2</sup> Datasheet for TC584000P/F/FT/TR CMOS NAND E<sup>2</sup>PROM electrically erasable and programmable nonvolatile memory, allegedly published in Toshiba 1993 MOS Memory (Non-Volatile) Databook (TOSH-1009, pp. 367-380) (“1993 Databook”).

diagrams for the devices described in Nakai and the 1993 Databook are provided below.

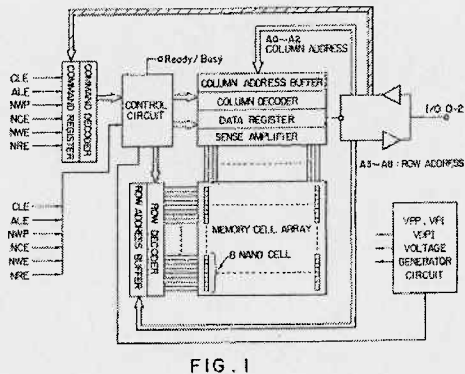
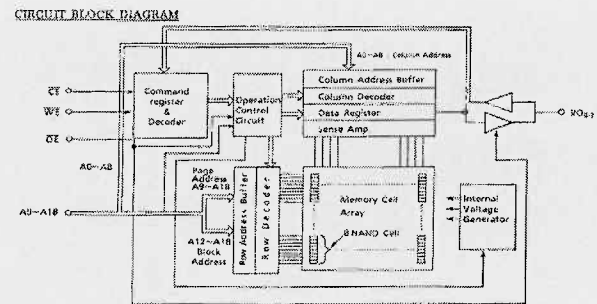


FIG. 1 of Nakai



Circuit Diagram of 1993 Databook,  
p. 368.

Nakai is assigned on its face to Toshiba, while the 1993 Databook describes Toshiba's TC584000P/F/FT/TR memory. (See Nakai, cover page; 1993 Databook, p. 3.) In its petition, Toshiba characterizes both Nakai and the 1993 Databook as teaching electrically-erasable, non-volatile NAND memories. (See Petition, pp. 13 and 30.). Based on the similarities between the references, it appears as though Toshiba's Nakai patent was drafted to cover products described by its 1993 Databook.

### III. The Board should deny the First Ground because it is redundant to the Second Ground

The Board should not initiate trial on multiple grounds of unpatentability, where one of the grounds is redundant to another. Here, Toshiba's Nakai patent

and its 1993 Databook are substantively identical. Toshiba's petition presents the two grounds in an entirely redundant manner. And Toshiba does not evaluate or compare the strengths and weaknesses of the two references. Toshiba's First and Second Grounds are therefore redundant. In the interest of securing a "just, speedy, and inexpensive" resolution, the Board should deny at least one of these redundant grounds. If trial is instituted, the Board should deny the First Ground as redundant over the Second Ground, as discussed below.

**A. Toshiba bears the burden of showing why it is entitled to a trial on multiple grounds of unpatentability.**

A petitioner bears the burden of proof to establish that it is entitled to the relief sought in the petition. *See* 37 C.F.R. § 42.20(c). In making its trial determination, Board proceeds on a ground-by-ground basis. *See id.*, § 42.108. As a result, a petitioner may not be entitled to consideration of all grounds presented in a petition. Rather, "[a]t any time prior to institution of *inter partes* review, the Board may deny some or all grounds for unpatentability for some or all of the challenged claims." *Id.*, § 42.108(b).

For example, the Board can decide to deny one or more grounds as being redundant to grounds already presented. As the Board explained on the behalf of an expanded panel of nine judges, "multiple grounds, which are presented in a

redundant manner by a petitioner who makes no meaningful distinction between them, are contrary to the regulatory and statutory mandates, and therefore are not all entitled to consideration.” *Liberty Mut. Ins. Co. v. Progressive Cas. Inc. Co.*, CBM2012-00003 (Paper No. 7), at \*2 (P.T.A.B., Oct. 25, 2012). Cited references need not be identical to be redundant, so long as they are cited for the same facts. *Illumina, Inc. v. Trs. of Columbia Univ. in the City of New York*, IPR2012-00006 (Paper No. 43), at \*12 (P.T.A.B., May 10, 2013). Hence, the onus is on the petitioner Toshiba to “articulate[] a meaningful distinction in terms of relative strengths and weaknesses with respect to the application of the prior art disclosures to one or more claim limitations.” *Ultratec, Inc. v. Sorenson Commc’ns, Inc.*, IPR2013-00288 (Paper No. 23), at \*4 (P.T.A.B., Jan. 10, 2014) citing *Liberty Mut. Ins. Co. v. Progressive Cas. Ins. Co.*, CBM2012-00003 (Paper No. 7), at \*2 (P.T.A.B., Oct. 25, 2012).

The Board has discretion to deny redundant grounds of unpatentability. 37 C.F.R. § 42.108(b). In exercising that discretion, the Board must keep in mind its goal of securing the “just, speedy, and inexpensive” resolution of every dispute. 37 C.F.R. § 42.1(b). As the Board has explained, the discretion of 37 C.F.R. § 42.108(b) “stems directly from 35 U.S.C. § 316(b), which recognizes, among other things, that *inter partes* review proceedings must be conducted to ensure the

ability of the Office to complete timely the proceedings.” *Schrader-Bridgeport Int’l, Inc. v. Cont’l Auto. Sys. US, Inc.*, IPR2013-00014 (Paper No. 15), at \*4 (P.T.A.B., Apr. 10, 2013). To that end, the Board has recognized that “considering multiple rejections for the same unpatentability issue would unnecessarily consume the time and resources of all parties involved.” *Illumina, Inc. v. Trs. of Columbia Univ. in the City of New York*, IPR2012-00006 (Paper No. 43), at \*12 (P.T.A.B., May 10, 2013).

Here, the Board should exercise its discretion and deny trial for at least one of Toshiba’s two proposed grounds of rejection. In particular, if trial is instituted, the Board should deny the First Ground as redundant over the Second Ground, as discussed below.

**B. Toshiba’s proposed grounds are redundant, and Toshiba did not meet its burden to show why it is entitled to trial on both grounds.**

Throughout its petition, Toshiba describes its Nakai patent and its 1993 Databook independently. Toshiba never compares or evaluates these two references in view of one another. To be entitled to a trial on both grounds, it is Toshiba’s burden to identify relative strengths or weaknesses with respect to challenged claims 1 and 4 of the ’045 Patent. Toshiba did not do this.

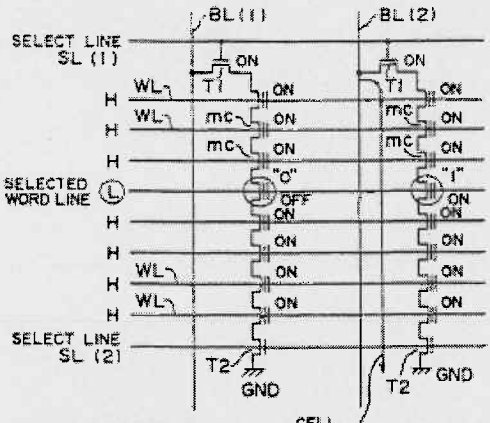
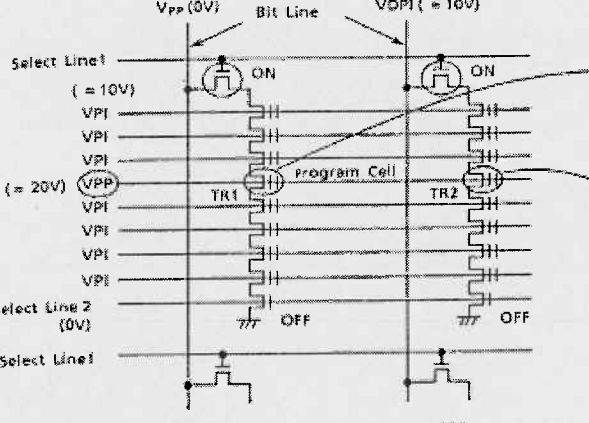


Instead, the petition cites to nearly identical teachings in Nakai and the 1993 Databook as the basis for the alleged grounds of unpatentability. For example, the Petitioner characterizes Nakai and the 1993 Databook in a nearly identical manner:

<b><u>DISCUSSION OF NAKAI</u></b>	<b><u>DISCUSSION OF 1993 DATABOOK</u></b>
<p>Nakai discloses a NAND type EEPROM non-volatile memory array (<i>i.e.</i>, flash memory) that includes columns of memory cells “MC” connected in series, and connected at the top to a bit line “BL” via a select transistor T1 and at the bottom to ground GND via a select transistor T2. Select lines SL(1) and SL(2) operate the row of select transistors T1 and the row of select transistors T2, respectively. The array includes word lines WL that each connect to the select gates of one of the memory cells from each column. (TOSH-1005, 1:20-30.) The array is shown in Fig. 22(a) of Nakai (which is included below along-side of Fig. 4 of the '045 patent (the array configurations are essentially the same):</p>	<p>The 1993 Databook discloses a CMOS NAND E2PROM electrically erasable and programmable nonvolatile memory (TC584000P/F/FT/TR). (TOSH-1009, pp. 367-380.) As shown in Fig. 2 (p. 379), the memory includes columns of memory cells connected in series to each other, with each column connected at the top to a bit line via a select transistor and at the bottom to ground via a select transistor. Select Line 1 and Select Line 2 operate the row of select transistors to the bit lines and the row of select transistors to ground, respectively. The array includes word lines that each connect to the gates of one of the memory cells from each column: (Petition, p. 30.)</p>

(Petition, pp. 13-14.)

Toshiba's descriptions of Nakai and the 1993 Databook further rely on nearly identical circuit diagrams from each reference:

<u>DISCUSSION OF NAKAI</u>	<u>DISCUSSION OF 1993 DATABOOK</u>
 <p><b>FIG. 22(a)</b></p> <p>FIG. 22 of Nakai cited on p. 14 of the petition.</p>	 <p><b>Fig.2 Program Principle of TC584000</b></p> <p>FIG. 2 of the 1993 Databook cited on p. 30 of the petition.</p>

Toshiba further characterizes the programming methods used in Nakai and the 1993 Databook in nearly identical terms:

<u>DISCUSSION OF NAKAI</u>	<u>DISCUSSION OF 1993 DATABOOK</u>
<p>For programming the selected cell labeled "Programmed Cell" in Fig. 23(a),</p>	<p>Specifically, for programming the selected cell labeled "Program</p>

<p>the select line SL(1) is set at 12 V (i.e. “logic high”) so that the select transistors T1 are “ON,” and the select line SL(2) is set at 0V (i.e. “logic low”) so that the select transistors T2 are “OFF.” (TOSH-1005, 1:53-57, Fig. 23(a).)</p> <p>The word line for the selected cell (i.e. the selected word line) is placed at voltage <math>V_{pp}</math>, while the remaining word lines (i.e. the unselected word lines) are placed at VPI. (TOSH-1005, Fig. 23(a).) (TOSH-1005, Fig. 23(a).)</p> <p><math>V_{pp}</math> is a high voltage of “about 20 V” (i.e. a boosted positive voltage).</p>	<p>Cell” in Fig. 2, the select line 1 is given “H” level (i.e. logic high) and the select line 2 is given “L” level (0V) (i.e. logic low), so that the 8 cells in the column are connected to the bit line (i.e. bit line select transistors are “on”) and isolated from ground (i.e. the source line select transistors are “off”). (TOSH-1009, p. 378, Fig. 2 on p. 379).</p> <p>The word line for the selected cell (i.e. the selected word line) is placed at voltage <math>V_{pp}</math>, while the remaining word lines (i.e. the unselected word lines) are placed at VPI. (TOSH-1009, p. 378, Fig. 2 on p. 379).</p> <p><math>V_{pp}</math> is a high voltage of “approximately 20 V” (i.e. a boosted</p>
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<p>(TOSH-1005, 1:47.)</p> <p>VPI is a voltage of “about 10 V” (i.e. a logic high voltage). (TOSH-1005, 1:50.)</p> <p>The bit line BL(1) for the selected cell (i.e. the selected bit line) is placed at 0V (i.e. a logic low voltage), while the remaining bit lines (i.e. BL(2), the unselected bit lines) are placed at a voltage of VDPI. (TOSH-1005, Fig. 23(a).)</p> <p>VDPI is a voltage of “about 10 V” (i.e. a logic high voltage). (TOSH-1005, 2:3.)</p> <p>(Petition, p. 15.)</p>	<p>positive voltage). (TOSH-1009, p. 378.)</p> <p>VPI is a voltage of “approximately 10 V” (i.e. a logic high voltage). (TOSH-1009, p. 378.)</p> <p>The bit line for the selected cell (i.e. the selected bit line) is placed at 0V (i.e. a logic low voltage), while the remaining bit lines (i.e. the unselected bit lines) are placed at a voltage of VDPI. (TOSH-1009, p. 378, Fig. 2 on p. 379.)</p> <p>VDPI is a voltage of “approximately 10 V” (i.e. a logic high voltage). (TOSH-1009, p. 378.)</p> <p>(Petition, pp. 31-32.)</p>
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The tables of programming voltages that Toshiba provided as evidence for the teaching of the elements of claims 1 and 4 of the '045 Patent are also nearly identical:

**Discussion of Nakai**

Array Element	Voltages – '045 Patent claims 1 & 4	Voltages – Nakai
BSL	Logic High	12 V on SL(1) – i.e. logic high
SSL	Logic Low	0 V on SL(2) – i.e. logic low
Selected Bit Line	Logic Low	0 V on BL(1) – i.e. logic low
Unselected Bit Lines	Logic High	VDPI (10V) on BL(2) – i.e. logic high
Selected Word Line	Boosted Positive	Vpp (20 V) on WL with Programmed Cell – i.e. boosted positive
Unselected Word Lines	Logic High	VPI (10V) on WL's without Programmed Cell – i.e. logic high

Petition, p. 16, referencing Nakai.

**Discussion of the 1993 Databook**

Array Element	Voltages – '045 Patent claims 1 & 4	Voltages – 1993 Databook
BSL	Logic High	H level on Select Line 1– i.e. logic high
SSL	Logic Low	L level (0V) on Select Line 2– i.e. logic low
Selected Bit Line	Logic Low	0 V – i.e. logic low
Unselected Bit Lines	Logic High	VDPI (~10V) – i.e. logic high
Selected Word Line	Boosted Positive	Vpp (~20 V) on WL containing “Program Cell”– i.e. boosted positive
Unselected Word Lines	Logic High	VPI (~10V) on WL's not containing “Program Cell” – i.e. logic high

Petition, p. 32, referencing the 1993 Databook.

In view of the above tables and excerpts from Toshiba's petition, Ground 1 and Ground 2 are entirely redundant. Toshiba provides no explanation for why it should be entitled to a trial on both grounds.

**C. Because the 1993 Databook published before Nakai was patented, the Board should deny the First Ground.**

Without an expressed preference from a petitioner, the Board may consider the publication date of the reference(s) relied upon in each ground in determining which redundant ground(s) to deny. In at least one proceeding, absent petitioner's expressed preference, the Board's default position is to select the ground based on the reference with the earliest apparent publication date. *See Liberty Mut. Ins. Co. v. Progressive Cas. Ins. Co.*, CBM2012-00003 (Paper No. 7), at \*7 (P.T.A.B., Oct. 25, 2012) (granting trial over the earlier of two references). Here, Nakai was patented on March 22, 1994, while the 1993 Databook appears to have been published in 1993.<sup>3</sup> (Nakai, cover page; 1993 Databook, p. 3.) Thus absent any expressed preference by Toshiba, the Board should at least deny the ground of

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<sup>3</sup> Although Nakai has a filing date that predates the publication of the 1993 Databook, this filing date is not relevant under 35 U.S.C. § 102(b). Rather, under Section 102(b), the relevant date is when a reference was "patented" or "published."

unpatentability based on Nakai as redundant over the ground of unpatentability based on the 1993 Databook.

#### **IV. Conclusion**

Toshiba's two primary references—Nakai and the 1993 Databook—are redundant. Toshiba did not meet its burden to show why it should be entitled to a trial on both grounds. In the interest of securing a "just, speedy, and inexpensive" resolution of this proceeding, the Board should deny at least one of the grounds presented in the petition as being redundant to the other. As a result, Patent Owner Intellectual Ventures I respectfully requests that the Board deny at least one of the petitioner Toshiba's two proposed grounds of unpatentability.

Respectfully submitted,

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/Jon E. Wright/

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**CERTIFICATION OF SERVICE**

The undersigned hereby certifies that the foregoing **PATENT OWNER PRELIMINARY RESPONSE** was served electronically via e-mail on February 7, 2014, in its entirety on the following:

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