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SECTOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
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ISSUING CLASSIFICATION

ORIGINAL				CROSS REFERENCE(S)							
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<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg. 4	Figs. Drwg. 6	Print Fig. 4	Total Claims 6	Print Claim for O.G. 1
<input type="checkbox"/> a) The term of this patent subsequent to _____ (date) has been disclaimed. <input type="checkbox"/> b) The term of this patent shall not extend beyond the expiration date, of U.S Patent. No. _____	_____ (Assistant Examiner) (Date)			NOTICE OF ALLOWANCE MAILED	
	Phaw Brong TRONG PHAN PRIMARY EXAMINER _____ (Primary Examiner)			11-16-99 ISSUE FEE Amount Due Date Paid \$605.00 2-9-00	
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~~Formal Drawings (____ sn(s) set~~

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PATENT APPLICATION



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CONTENTS

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1. Application <u>4</u> papers.		42.	
2. <u>S.D.S.</u>	<u>5-25-99</u>	43.	
3. <u>Pre-Andt. A</u>	<u>5-25-99</u>	44.	
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09/318,200	05/25/1999	365	2818	17822-1-2US
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CONTINUING DOMESTIC DATA*** VERIFIED THIS APPLN IS A DIV OF 08/926,576 09/04/1997 PAT 5,953,254 <i>Provisional No. 60/025,698 09/09/1996</i>				
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Foreign priority claimed <input type="radio"/> yes <input type="radio"/> no 35 USC 119 (a-d) conditions met <input type="radio"/> yes <input type="radio"/> no <input type="radio"/> Met after Allowance		STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS
Verified and acknowledged Examiner's Name Initials		CA	4	6
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TITLE SERIAL FLASH MEMORY				
FILING FEE RECEIVED \$**419	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT NO. _____ for the following:		<input type="radio"/> All Fees <input type="radio"/> 1.16 Fees (Filing) <input type="radio"/> 1.17 Fees (Processing Ext. of Time) <input type="radio"/> 1.18 Fees (Issue) <input type="radio"/> Other _____ <input type="radio"/> Credit	

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09/318,200	05/25/99	365	2818	17822-1-2US

APPLICANT
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TITLE
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Sir:

Transmitted herewith for filing is the

☒ divisional patent application of ALI POURKERMATI
For: SERIAL FLASH MEMORY

☒ This application claims priority from each of the following Application Nos./filing dates:
60/025,698/September 9, 1996 and 08/926,576/September 4, 1997

the disclosure(s) of which is (are) incorporated by reference.

☒ Please amend this application by adding the following before the first sentence: "This application is a ☒ division of and claims the benefit of U.S. Provisional Application No. 60/025,698, filed September 9, 1996 and U.S. Application No. 08/926,576, the disclosures of which are incorporated by reference."

Enclosed are:

- ☒ 4 sheet(s) of ☐ formal ☒ informal drawing(s).
☒ A ☒ signed ☐ unsigned Declaration, Power of Attorney by Assignee & Certificate Under 37 C.F.R. §3.73(b)
☒ A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27 ☐ is enclosed ☒ was filed in the prior application and small entity status is still proper and desired.
☒ Information Disclosure Statement under 37 CFR 1.97.
☒ Preliminary Amendment

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INDEP. CLAIMS	4 - 3	= *1	
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Respectfully submitted,

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Attorney Docket No. 017822-00011

PATENT APPLICATION

SERIAL FLASH MEMORY

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SERIAL FLASH MEMORY

This appl is a Divisional of Ser. No. 08/926,576 filed Sept. 4, 1997, SN. 5953,254 and also claims the benefit of US Provisional No. 60/025,698 filed Sept. 9, 1996.

BACKGROUND OF THE INVENTION

The present invention relates in general to semiconductor memories, and in particular to an improved flash memory circuit and method of manufacture.

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Figure 1 shows a schematic cross-section of an example of a single-transistor double poly stacked gate flash cell. The cell includes a floating gate 100 made of a first polysilicon layer (poly-1), a control gate 102 made of a second polysilicon layer (poly-2), an N+ drain region 106 and an N++ source region 104 inside a P-well region 108. A thin layer of silicon dioxide of approximately 70 to 120 Angstroms forms the tunnel oxide 110 between the floating gate poly-1 and the channel, and a 150 to 300 Angstroms thick film made of an oxide-nitride-oxide (ONO) sandwich 112 separates the two poly gates 100 and 102.

This cell is programmed by grounding the source terminal, applying a 5 to 10 volt signal to the drain terminal or the bit line ($V_{BL}=5v$), and applying a high programming voltage V_{pp} of, for example, 18 to 20 volts to control gate 102 ($V_{CG}=V_{pp}$). The high voltage on V_{CG} creates a high electric field across tunnel oxide 110 generating hot electrons in the channel with enough energy to cross the tunnel oxide. These hot electrons are then trapped in the floating gate poly-1 layer 100 resulting in a higher threshold voltage for the transistor. The cell is thus programmed into an OFF (non-conducting) state.

2

Erasing of the cell is performed by grounding the control gate and the drain terminal and applying V_{pp} to the source terminal. The large gate to source voltage causes the trapped electrons on the floating poly 100 to tunnel through the thin oxide layer 110 by a mechanism known as Fowler-Nordheim.

5 The electrons are collected by the source region 104.

The flash memory cell shown in Figure 1, however, suffers from a number of drawbacks in terms of its overall performance. Because the source region 104 is subject to very high erase voltages (V_{pp}), this cell requires a carefully engineered high-voltage junction process. As shown in Figure 1, the

10 source region 104 is made deeper than the drain region 106 and has a higher doping concentration. The high-voltage junction requirement results in a more complex and therefore more expensive process. Further, the high-voltage junction requirement results in a cell that is not scaleable. That is, the high-

15 voltage diffusion to high-voltage diffusion spacing requirements increases the cell layout pitch. Lower endurance is another drawback of the high-voltage junction, since under high voltage conditions, the source region 104 cannot withstand a large number of erasures.

20 Furthermore, applying the high V_{pp} voltage to the source region 104 generates hot holes that are released into the P-well 108 and then collected and trapped inside the tunnel oxide 110. This phenomenon, sometimes referred to as band bending, not only deteriorates the endurance of the cell, it also results in unpredictable erase threshold voltage over time. Additional erase threshold

25 voltage verification circuitry are thus necessary for proper operation of the cell.

Finally, because the tunnel oxide region 110 is the same size as the channel, its capacitance is relatively larger, and thus the cell coupling capacitance is lower. Lower cell coupling capacitance requires larger program and erase

30 voltages. Larger program and erase voltages not only lower the endurance of the cell, they also add to the circuitry as they require large pump circuits.

An improvement to the flash cell shown in Figure 1 splits the erase voltage between the control gate 102 and the source 104. Instead of applying a high voltage to the source region 104, the control gate 102 is negatively biased with respect to the source terminal. Thus, in this embodiment, programming voltages remain the same, but during erase, a negative voltage is applied to the control gate ($V_{CG} = -V_{PP}$) while the source terminal connects to the positive power supply voltage (typically 3 to 5 volts). This allows the source junction to be the same size as the drain junction, and eliminates the high-voltage junction process requirements. However, this cell requires an additional negative pump circuit and still suffers from the hot hole injection and the resulting erratic erase threshold voltage.

Various other implementations of a single-transistor flash cell have been proposed each improving on some aspects of the cell performance, but with trade-offs in other aspects. For example, one approach that eliminates performance degradations caused by the hot hole injection, places the P-well 108 inside another N-well. This allows the P-well 108 to be biased to a positive voltage along with the source and drain regions, while the control gate is biased negatively for an erase operation. This type of flash cell, however, requires a triple well technology that is much more complex and costly to manufacture. Further, the cell still requires a negative pump circuit to bias the control gate during erase.

While there have been numerous variations on the double poly stacked gate single-transistor flash cell, there is room for improvement of the structure and design of the cell in terms of endurance, speed, reliability and cost of manufacture.

SUMMARY OF THE INVENTION

The present invention provides a novel scaleable flash memory cell structure and method of manufacture that improves data retention, increases capacitive coupling and speed of operation, and improves reliability among other advantages. The flash cell of the present invention permits implementation of arrays of flash memory cells that allow the designer to program and/or erase individual bytes of memory as well as blocks of memory. Therefore, the non-volatile memory circuit of the present invention combines the advantages of conventional EEPROM technology with that flash technology.

Broadly, the flash cell according to the present invention limits the tunnel oxide to a window having dimensions at the minimum feature size located over the drain side of the transistor. The tunnel oxide window is separated from the field oxide and has no edges abutting field oxide. Thus, leakage due to defects caused by the field edge is eliminated, resulting in higher data retention rates for the cell. The reduced dimensions of the tunnel oxide region significantly increase the gate capacitive coupling ratio of the cell. The higher gate coupling allows the cell to be smaller yet operate at higher speed (larger read current). The higher coupling ratio also reduces the level of the maximum required voltage resulting in higher endurance.

Accordingly, in one embodiment, the present invention provides a memory cell including a source region and a drain region forming a channel therebetween; a channel oxide layer disposed on top of the channel; a floating gate layer disposed on top of the channel oxide layer, where the floating gate layer and channel oxide layer define a window wherein a thickness of the channel oxide is substantially smaller than the remaining portion of the channel oxide. The memory cell further includes a control gate layer disposed on top of and separated from the floating gate layer by a dielectric film, wherein the window is located on a drain side of the channel and has dimensions at minimum feature size.

In another embodiment, the present invention provides a method of manufacturing a memory cell including the steps of

5 A better understanding of the nature and advantages of the flash memory of the present invention may be had with reference to the drawings and detailed description below.

BRIEF DESCRIPTION OF THE DRAWINGS

10 Figure 1 shows an exemplary prior art double poly stacked gate single transistor flash memory cell;

15 Figure 2A shows a top view of a specific embodiment of a single flash cell as initially laid out, while Figures 2B and 2C show top views of two different embodiments of the cell after it has been formed;

20 Figure 3 illustrates the cross section of two flash memory cells perpendicular to word line and a high voltage transistor switch according to the present invention;

25 Figure 4 is a circuit schematic for an exemplary memory array made of flash cells according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

30 Various aspects of the flash memory according to the present invention will be described in detail hereinafter.

Cell Structural Design

Referring to Figures 2A and 2B, there are shown top views of a specific embodiment of a single flash cell of the present invention as initially laid out, and a of the cell after it has been formed, respectively. In a preferred embodiment, each flash cell is implemented in a double poly, single metal, twin

well CMOS process. As shown in Figure 2A, active area 20 (e.g., N+) is diffused into a well region (e.g., P-well). A control gate polysilicon layer 25 is laid out perpendicular to active region 20 and defines drain and source regions 21 and 22, respectively. The overlap area between control gate polysilicon 25 and active area 20 forms the transistor channel region 26. A non-self aligned tunnel window 23 is formed on the drain side (21) of each memory cell as depicted. A floating polysilicon layer 24 overlaps active area 20.

As shown in Figure 2A, tunnel area 23 partially extends over drain region 23 such that it has a first region 23A under gate poly 25 (i.e., over the channel) and a second region 23B over drain 21. The overlap region 23B of tunnel window 23 will be removed during subsequent steps in the process.

Figure 2B shows a top view of the flash cell as formed at the completion of the process. As depicted in Figure 2B, both tunnel window 23 and floating gate poly 24 are etched back to within the area of channel region 26. Note that the area defining tunnel window 23 does not coincide with the area defining channel region 26. This appreciably increases the gate capacitive coupling ratio of the cell allowing faster operation. Furthermore, in the preferred embodiment shown, tunnel oxide window 23 as thus formed is separated from the field oxide (not shown) and has no edges abutting field oxide, eliminating potential leakage caused by defects at the field edge. Tunnel oxide window 23 may alternatively extend all the way to the field edges of the channel as shown in Figure 2C. The memory cell embodiment shown in Figure 2C still exhibits the higher gate capacitive ratio because tunnel window 23 does not coincide with the entire area defining channel region 26.

Referring to Figure 3, there is shown a cross section of two flash memory cells 200-1 and 200-2 in a direction perpendicular to the word line, and a high voltage transistor switch 216 according to one embodiment of the present invention. In this exemplary implementation, N+ source drain regions are

diffused into a p-well region 208, and the drain region for one cell acts as the source for the adjacent cell. That is, N+ region 211 forms the source terminal of cell 200-1, N+ region 209 forms the drain terminal of cell 200-1 as well as the source terminal of cell 200-2, and N+ region 215 forms the drain terminal of cell 200-2. Tunnel window 210 is formed on the drain side of each cell and is preferably of minimum feature size. As mentioned above, in a preferred embodiment, tunnel window 210 is fieldless (i.e., does not abut field oxide) which helps increase endurance. The active area surrounding the tunnel window is covered by relatively thicker cell gate oxide 212 of, for example, about 100-300 Angs. Tunnel window 210 comprises a thin, for example, 70- 100 Angs thermal dielectric. Thus, the cell channel region (26 in Figure 2B) is covered by both tunnel oxide window 210 (23A in Figure 2B) and relatively thicker gate oxide 212. The tunnel window/active area edge has a gradual step of, for example, 30-200 Angstroms thick.

A first preferably multiple stack polysilicon layer (poly-1 201 and 202 as shown in Figure 3), forming the memory cell floating polysilicon (i.e., charge storage layer), is formed on top of gate oxide (210 and 212). The total thickness of the multiple stack floating polysilicon 201/202 is preferably about, for example, 500 Angstroms, with typical grain size at the tunnel oxide boundary of approximately less than 100 Angstroms. The control gate terminal (connected to the word line) is formed by a second polysilicon (poly-2) layer 206 preferably combined with a polycide layer 207, that form a combined thickness of approximately 1000-2000 Angstroms. Poly-1 layer 201/202 and silicided poly-2 layer 206/207 are separated by, for example, 150-200 Angstroms thick Oxide-Nitride-Oxide (ONO) 203/204/205 dielectric stack. The memory as thus constructed includes a structure having a substrate>well>tunnel oxide>poly-1>ONO>poly2-polycide stack. Exemplary value for the size of the stack may be approximately 0.28-.34 μm .

Cell Process Flow

The cell formation according to one embodiment of the present invention begins with a p-type silicon substrate 214. After the typical CMOS steps forming N- and P-well regions, active areas (36 in Figure 2B) are defined by masking and etching steps. This is preferably followed by a field implant to increase the parasitic field threshold voltage. A thick field oxide of, for example, 3000-5000 Angstroms is then grown all over the wafer to isolate different active areas followed by nitride strip and kooi oxide growth. A p-well protect mask is then used to block p-well formation from areas where high voltage circuit blocks will be built. This is to avoid high back-biased threshold voltages of highly doped p-well.

After resist strip and an oxide clean step, gate oxide 212 is formed by growing a high quality thermal oxide (e.g., 150-190 Angstroms thick) all over the wafer. This is followed by a cell threshold voltage (Vt) adjust mask and an implant (using e.g., Boron) to adjust the cell threshold to appropriate value between the programmed and the erased Vt distribution target. After implant the resist is stripped.

The wafers are then masked to form tunnel windows 210 for the memory cells. This mask is a critical mask as this term is used in the art. The wafers are then subjected to a short (e.g., 10-25 sec.) wet oxide cleaning step to clean the tunnel windows with non roughening characteristics. The resist is removed from the wafers and the surface is cleaned again to remove organic, metallic and hydrocarbons from the surface.

The next step involves forming the tunnel oxide by growing a high quality thermal oxide, of for example 70-85 Angstroms to cover the whole wafer. This is followed by deposition of the first of several layers of polysilicon layers to form the floating polysilicon having layers that are each engineered with varying grain sizes. The top layer of poly (layer 202) is preferably implanted

with N⁺ dopants to amorphize the poly and dope it to achieve for example 200-500 ohms/square sheet resistivity.

The wafers are then oxidized (at e.g., 900-1050 C) to grow thermal oxide of for example 100 Angstroms. This step forms oxide layer 203 and is followed by deposition of about 75-90 Angstroms of silicon-nitride (layer 204) grown at exemplary temperatures of 650-700 C. The wafers are then subjected to a wet oxidation to cover the nitride surface with 30-50 Angstroms of blocking oxide (1000 C wet oxidation to grow 3500-4000 Angs on bare silicon). This series of steps forms ONO layers 203/204/205.

Next, the wafers are masked again to etch ONO/poly-1/gate-tunnel islands in the memory array. This etch is preferably performed anisotropically and is designed to endpoint on the tunnel oxide. The polysilicon/ONO/gate oxide stack on high voltage transistors 216 are also masked in this step to protect the high voltage (HV) transistor gates 222. After resist strip the wafers are subjected to a light oxidation at 800-900 C in a dry ambient. This oxidation is done to seal off the exposed edges of floating gate 201/202 that is freshly exposed after the etch.

The memory array core is then masked to clean the periphery with a wet/dry etch. The memory array core mask is also used to protect the high voltage circuit areas. After the etch, the resist is stripped and the wafers are masked again to form self-aligned high voltage graded junctions for the HV enhancement transistors. The high voltage implant could be for example a Phosphorus 31 implant 5E13-5E14 #/cm² or a double-diffused Phosphorus/arsenic combination implant.

After the implant, the resist is stripped and the wafers are subjected to a low voltage threshold adjust mask or blanket, and implant sequence followed by a high quality wet gate oxidation to grow about 70-110 Angstroms of oxide in

the periphery active areas. The wafers are then covered with approximately 1.5 kA to 2.0 kA polysilicon layer that forms the gate of the periphery transistors and the first poly layer (206) of the word line for memory cell array. To reduce heat generation and resistivity of the word line poly, a 1000-2000 Angstrom layer of WSi_x is deposited over the entire wafer that forms the top layer 207 for the control gate of the memory cell. Next, the wafers are subjected to re-oxidation at about 900-950 C for approximately 30-50 minutes.

The memory cell stack is then defined by a masking step that also protects the periphery. The stacked array mask etch is used to etch the polycide/ONO/poly-1/tunnel sandwich 200. After the etch, wafers are cleaned to remove organics, hydrocarbons and post etch residues. The high voltage transistors are covered with resist during this etch.

The wafers are masked again to define the gate polycide of the periphery low voltage transistors. After the gate poly etch the resist is stripped. The high voltage transistors are exposed during this etch. Both the polycide and the poly are etched away. About 100 Angstroms of ONO is etched away also leaving a 50-100 Angstroms of dielectric on the HV gates.

The n-tip mask is then used to form the lightly doped drain (LDD) tips of the NMOS transistor followed by p-tip mask and implant. The n-tip mask is blocked from memory array and HV transistors. The spacer deposition is followed by spacer etch and N+ and P+ source drain formation. The first interlayer dielectric is then formed by either BPSG, BPTEOS with 4/4 B/P, or the like. The inter layer dielectric (ILD) is then reflowed at about 850-920 C and SOG planarized and the contacts are masked and opened.

This is followed by barrier metal deposition followed by tungsten plug formation and first metal (metal-1) deposition. The metal-1 mask is then used to define the interconnect and memory array bit lines. Finally, metal-1

layer is covered with thick ILD and passivation oxynitride is deposited and etched using the pad mask.

Cell Electrical Design

5 In a preferred embodiment of the present invention cells are programmed (e.g., high cell V_t) and erased (e.g., low cell V_t) by Fowler Nordhiem tunneling to and from the same tunnel window on the drain side. The various modes of operation, including programming, erase and read will be described in connection with the exemplary memory array circuit shown in Figure 4. Referring to Figure 4 there is shown an exemplary circuit schematic for an array 400 made of flash memory cells according to the present invention. Array 400 includes memory cells 402 located at intersection of 16 word lines (WL0-WL15) and 16 bit lines (BL0-BL15). Bit line select transistors 404 respectively couple bit lines BL0-BL15 to memory cells 402. Source select transistors 406 couple ground (or V_{ss}) to memory cells 402. A bit line select control line BSL controls gate terminals of bit select transistors 404, and a source select control line SSL controls gate terminals of source select transistors 406.

20 Table I below sets forth a preferred biasing scheme for various cell operations for an individual cell according to the present invention.

Table I

<u>Control Line</u>	<u>Erase</u>	<u>Program</u>	<u>Read</u>	<u>Condition</u>
BSL	V_{cc}	V_{cc}	V_{cc}	Selected
SSL	V_{ss}	V_{ss}	V_{cc}	Selected
25 BL0	V_{cc}	V_{ss}	1.0-1.4V	Selected
BL1	V_{ss}	V_{cc}	0.5V	Unselected
WL0	V_{cc}	V_{cc}	V_{cc}	Unselected
WL1	-12 to -15V	15-20V	V_{ss}	Selected

30 Erase Operation:

In the exemplary biasing convention described herein, cells are erased by the action of applying negative gate voltage of, for example, -12 to -15 volts on the selected word lines or a single word line (WL1), and applying a voltage approximately equal to V_{cc} (e.g., $V_{cc}-2V_{tn}$ to V_{cc}) on the selected bit lines or a single bit line (e.g., BL0). A voltage of about V_{cc} is applied to bit line select control line BSL, while source select control line SSL is coupled to ground or V_{ss} . This condition generates the necessary electrical field to force electrons to leave the floating gate through the cell tunnel oxide drain interface. This results in a reduced threshold voltage for the cell.

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memory cell of the present invention limits the threshold variation. The threshold voltage of the thick gate oxide portion of the cell helps to improve the punch-through margin of the cell.

5 Typical erase current depends on the block size and is of the order of a few mA. The erase speed is primarily a function of the field across tunnel oxide which can be, for example, approximately 8.5 to 10 MV/cm to achieve block erasure in less than for example 1 msec.

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Programming operation:

 The programming operation is done by applying a high voltage (e.g., 15 to 20 V) on the selected word line (WL1) and grounding the selected bit line (BL0), while the unselected bit lines (BL1-BL15) are at Vcc. Referring to Figure 4, to program memory cell 402-C, a high voltage of for example 15 to 20 volts is applied to WL1. Vcc is applied to BSL control line and WL0 to couple BL0 to the drain terminal of memory cell 402-C. With BL0 grounded, the drain terminal of cell 402-C receives ground potential. Control line SSL remains at VSS and unselected word lines WL2-WL15 receive VCC. Thus, the cells are programmed serially in a NAND type structure by passing Vss to the selected cells as the pass (unselected) word lines are pulled up to pass Vss.

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25 The typical programming current for the memory cell of the present invention may be, for example, as low as about 100 pA/cell. The typical programming current required by convention ETOX cells, on the other hand, is around 1 mA. The lower programming current requirement of the present invention allows for the pump circuits to be aggressively down sized, for a more compact overall design.

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Another advantageous feature of the present invention is that it provides for the ability to erase and/or program on a byte by byte basis. Because neither erase nor programming operations require shifting the potential supplied to the entire bulk (substrate) for the array of cells, erase or programming of memory array 400 need not be limited to the entire block.

Read Operation:

The read operation is accomplished by grounding the selected word line $WL1=V_{ss}$ and applying a low voltage of, for example, 1.0-1.5 volts to the selected bit line $BL0$. Unselected bit lines ($BL1-BL15$) receive a voltage in the range of V_{ss} to 0.5 volts. Unselected word lines $WL0$ and $WL2-WL15$ receive V_{cc} which allows their memory cells 402 to pass V_{ss} to the selected cell, e.g., 402-C, and couple the drain terminal of selected memory cell 402-C to selected bit line $BL0$. If memory cell 402-C is programmed (i.e., high V_t), then the voltage on selected bit line $BL0$ remains unaffected. If memory cell 402-C is not programmed (i.e., low V_t), selected bit line $BL0$ is pulled down to V_{ss} .

Finally, when changing from one mode (e.g., erase) to another (e.g., program, the memory array first enters the program inhibit mode of operation. The program inhibit mode avoids accidental programming of the cell during the transition from one mode of operation to another. In program inhibit mode, according to the present invention, the entire array enters an unselected condition by applying V_{ss} to BSLs, SSLs and BLs, and V_{cc} to WLs.

In conclusion, the present invention offers a single transistor, double-poly flash cell and a method of manufacture for the same that improves data retention, increases capacitive coupling and speed of operation, and improves reliability among other advantages. While the above is a complete description of the preferred embodiment of the present invention, it is possible to use various alternatives, modifications and equivalents. Therefore, the scope of the present invention should be determined not with reference to the above

WHAT IS CLAIMED IS:

- 1 1. A memory cell comprising:
2 a source region and a drain region forming a channel therebetween;
3 a channel dielectric layer disposed on top of said channel;
4 a floating polysilicon layer disposed on top of said channel
5 dielectric layer, said floating polysilicon layer and channel dielectric layer
6 defining a window within an area of said channel wherein a thickness of said
7 channel dielectric layer in said window is smaller than that of a remaining
8 portion of said channel dielectric layer; and
9 a control gate layer disposed on top of and separated from said
10 floating gate layer by a dielectric film,
11 wherein said window is located on a drain side of said channel.
12
- 13 2. The memory cell of claim 1 wherein a dimension of said
14 window is of minimum process feature size.
- 15 3. The memory cell of claim 1 further comprising field
16 dielectric layer substantially surrounding first and second sides of said channel,
17 and wherein, said window has no sides abutting said field dielectric layer.
- 18 4. The memory cell of claim 1 further comprising field
19 dielectric layer substantially surrounding first and second sides of said channel,
20 and wherein said sides of said window abut said field dielectric layer.
- 21 5. The memory cell of claim 1 wherein said channel dielectric
22 layer comprises silicon dioxide material, said control gate layer comprises
23 polysilicon material, and said dielectric film comprises a layer of nitride material
24 sandwiched between first and second silicon dioxide layers.

1 6. The memory cell of claim 5 wherein said control gate layer
2 further comprises a polycide layer on top of said polysilicon layer.

1 7. An array of flash memory cells, comprising:
2 a plurality of memory cells as defined in claim 1 arranged in a
3 plurality of columns, each column of memory cells comprising:
4 a bit line select transistor having a first current-carrying
5 terminal coupled to a bit line, and a gate terminal coupled to a bit line
6 select control line;
7 a predefined number of memory cells coupled in series with a
8 drain end coupling to a second current-carrying terminal of said bit line
9 select transistor, said predefined number of memory cells being serially
10 coupled such that a drain node of a memory cell acts as a source node of
11 an adjacent memory cell, and
12 a source line select transistor having a first current-carrying
13 terminal coupled to a source end of said predefined number of memory
14 cells, a gate terminal coupled to a source select line and a second current
15 carrying terminal coupled to a low potential.

1 8. An array of flash memory cells comprising:
2 a plurality of columns of serially connected flash memory cells,
3 each memory cell having a gate terminal;
4 a plurality of bit lines respectively coupled to drain side of said
5 plurality of columns of memory cells via a respective plurality of bit line select
6 transistors, said plurality of bit line select transistors having gate terminals
7 coupled to a bit line select control line;
8 a plurality of word lines, each one coupling to a gate terminal of
9 one memory cell in each of said plurality of columns to form rows of memory
10 cells with common gate terminals; and

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11 a plurality of source select transistors respectively coupling a source
 12 side of said plurality of columns of memory cells to a logic low voltage, and
 13 having gate terminals coupled to a source select control line,

14 wherein, during programming:

15 a logic high voltage is applied to said bit line select control line to
 16 turn on bit line select transistors,

17 a logic low voltage is applied to source select control line to turn
 18 off source select transistors;

19 a logic low voltage is applied to a selected bit line while a logic
 20 high voltage is applied to unselected bit lines, and

21 a logic high voltage is applied to unselected word lines, while a
 22 boosted positive voltage is applied to a selected word line.

23 *2x* An array of flash memory cells comprising:

24 a plurality of columns of serially connected flash memory cells,
 25 each memory cell having a gate terminal;

26 a plurality of bit lines respectively coupled to drain side of said
 27 plurality of columns of memory cells via a respective plurality of bit line select
 28 transistors, said plurality of bit line select transistors having gate terminals
 29 coupled to a bit line select control line;

30 a plurality of word lines, each one coupling to a gate terminal of
 31 one memory cell in each of said plurality of columns to form rows of memory
 32 cells with common gate terminals; and

33 a plurality of source select transistors respectively coupling a source
 34 side of said plurality of columns of memory cells to a logic low voltage, and
 35 having gate terminals coupled to a source select control line,

36 wherein, during erase:

37 a logic high voltage is applied to said bit line select control line to
 38 turn on bit line select transistors,

39 a logic low voltage is applied to source select control line to turn
 40 off source select transistors;

19 a logic high voltage is applied to a selected bit line while a logic
 20 low voltage is applied to unselected bit lines, and
 21 a logic high voltage is applied to unselected word lines, while a
 22 boosted negative voltage is applied to a selected word line.

1 ³ 10. An array of flash memory cells comprising:
 2 a plurality of columns of serially connected flash memory cells,
 3 each memory cell having a gate terminal;
 4 a plurality of bit lines respectively coupled to drain side of said
 5 plurality of columns of memory cells via a respective plurality of bit line select
 6 transistors, said plurality of bit line select transistors having gate terminals
 7 coupled to a bit line select control line;
 8 a plurality of word lines, each one coupling to a gate terminal of
 9 one memory cell in each of said plurality of columns to form rows of memory
 10 cells with common gate terminals; and
 11 a plurality of source select transistors respectively coupling a source
 12 side of said plurality of columns of memory cells to a logic low voltage, and
 13 having gate terminals coupled to a source select control line,
 14 wherein, during program inhibit a logic low voltage is applied to
 15 said bit line select control line, source select control line, and bit lines, while a
 16 logic high voltage is applied to word lines.

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SERIAL FLASH MEMORY

ABSTRACT OF THE DISCLOSURE

5 A scalable flash memory cell structure and method of manufacture is disclosed that improves data retention, increases capacitive coupling and speed of operation, and improves reliability among other advantages. The flash cell according to the present invention limits the tunnel oxide to a window having dimensions at the minimum feature size located over the drain side of the transistor. The tunnel oxide window is separated from the field oxide and has no
10 edges abutting field oxide.

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002

Attorney Docket No. 17822-1-1

DECLARATION

As a below named inventor, I declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **SERIAL FLASH MEMORY** the specification of which is attached hereto or X was filed on 9/4/97 as Application No. 08/926,576 and was amended on (if applicable).

I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56. I claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

Country	Application No.	Date of Filing	Priority Claimed Under 35 USC 119
			Yes <u> </u> No <u> </u>
			Yes <u> </u> No <u> </u>

I hereby claim the benefit under Title 35, United States Code §119(e) of any United States provisional application(s) listed below:

Application No.	Filing Date
60/025,698	9/9/96

I claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, section 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application No.	Date of Filing	Status
		<u> </u> Patented <u> </u> Pending <u> </u> Abandoned
		<u> </u> Patented <u> </u> Pending <u> </u> Abandoned

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003

Full Name of Inventor 1	Last Name POURKERAMATI	First Name ALI	Middle Name or Initial	
Residence & Citizenship	City Redwood City	State/Foreign Country CA	Country of Citizenship U.S.	
Post Office Address	Post Office Address 3979 Brookline Way	City Redwood City	State/Country CA	Zip Code 94062
Full Name of Inventor 2	Last Name	First Name	Middle Name or Initial	
Residence & Citizenship	City	State/Foreign Country	Country of Citizenship	
Post Office Address	Post Office Address	City	State/Country	Zip Code
Full Name of Inventor 3	Last Name	First Name	Middle Name or Initial	
Residence & Citizenship	City	State/Foreign Country	Country of Citizenship	
Post Office Address	Post Office Address	City	State/Country	Zip Code

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signature of Inventor 1  ALI POURKERAMATI	Signature of Inventor 2	Signature of Inventor 3
Date 3. 4. 98	Date	Date

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008

Attorney Docket No. 17822-1-1

POWER OF ATTORNEY BY ASSIGNEE

AZALEA MICROELECTRONICS CORP. is the Assignee of the invention entitled: SERIAL FLASH MEMORY, the specification of which ___ is attached hereto or X was filed on 9/4/97 as Application Serial No. 08/926,576.

Assignee hereby appoints the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

David N. Slope, Reg. No. 28,572
Babak S. Sani, Reg. No. 37,495

Send Correspondence to:

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, CA 94111-3834

Direct Telephone Calls to:
(Name, reg. no., tele. no.)

Babak S. Sani
Reg. No. 37,495
(415) 576-0200

AZALEA MICROELECTRONICS CORP.

Date: 3.9.98

By: Ali Pourkeramati

(Signature)

Name: Ali Pourkeramati
Title: President

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008

Atty. Docket No. 17822-1-1

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS
(37 CFR 1.9(f) & 1.27(c)) - SMALL BUSINESS CONCERN

Applicant or Patentee: Ali Pourkeramati

Application or Patent No.: 08/926,576

Filed or Issued: 9/4/97

Title: SERIAL FLASH MEMORY

I hereby declare that I am:

- ☐ the owner of the small business concern identified below:
☒ an official of the small business concern empowered to act on behalf of the concern identified below:

Name of Small Business Concern: Azalea Microelectronics Corp.

Address of Small Business Concern: 3080 Olcott Street, Suite 130-D
Santa Clara, CA 95054

I hereby declare that the above-identified small business concern qualifies as a small business concern as defined in 13 CFR 121.12, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees to the United States Patent and Trademark Office, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention, entitled by inventor(s) Ali Pourkeramati described in:

- ☐ the specification filed herewith.
☒ Application No. 08/926,576, filed 9/4/97.
☐ Patent No. _____, issued _____.

If the rights held by the above identified small business concern are not exclusive, each individual, concern or organization having rights in the invention is listed below* and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person made the invention, or by any concern that would not qualify as a small business concern under 37 CFR 1.9(d), or a nonprofit organization under 37 CFR 1.9(c).

*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

Name _____

Address _____

☐ Individual ☒ Small Business Concern ☐ Nonprofit Organization

Name _____

Address _____

☐ Individual ☐ Small Business Concern ☐ Nonprofit Organization

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b)).

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

Name of Person Signing: Ali Pourkeramati

Title of Person if Other than Owner: President

Address of Person Signing: 3979 Brookline Way
Redwood City, CA 94062

Signature Ali Pourkeramati

Date 3.4.98

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007

CERTIFICATE UNDER 37 C.F.R. § 3.73(b)

Applicant: Ali Pourkeramati

Application No.: 08/926,576

Filed: 9/4/97

For: SERIAL FLASH MEMORY

Azalea Microelectronics Corp., a California corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

certifies that it is the assignee of the entire right, title and interest in the patent application identified above by virtue of either:

A. ☒ An assignment from the inventor(s) of the patent application identified above. The assignment was recorded in the Patent and Trademark Office at Reel _____, Frame(s) _____, or for which a copy thereof is attached.

OR

B. ☐ A chain of title from the inventor(s), of the patent application identified above, to the current assignee as shown below:

1. From: _____ To: _____
The document was recorded in the Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.
2. From: _____ To: _____
The document was recorded in the Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.
3. From: _____ To: _____
The document was recorded in the Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet.

☐ Copies of assignments or other documents in the chain of title are attached.

The undersigned has reviewed all the documents in the chain of title of the patent application identified above and, to the best of undersigned's knowledge and belief, title is in the assignee identified above.

The undersigned (whose title is supplied below) is empowered to act on behalf of the assignee.

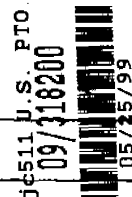
I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further, that these statements are made with the knowledge that willful false statements, and the like so made, are punishable by fine or imprisonment, or both, under Section 1001, Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date : 3.4.98

Name : Ali Pourkeramati

Title : President

Signature : Ali Pourkeramati





TOWNSEND & TOWNSEND
& CREW

MAY 14, 1998

98 MAY 21 AM 8:45
TOWNSEND AND TOWNSEND AND CREW LLP
BABAK S. SANI
TWO EMBARCADERO CENTER, 8TH FLOOR
SAN FRANCISCO, CA 94111-3834

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UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
ASSISTANT SECRETARY AND COMMISSIONER
OF PATENTS AND TRADEMARKS
Washington, D.C. 20231



UNITED STATES PATENT AND TRADEMARK OFFICE
NOTICE OF RECORDATION OF ASSIGNMENT DOCUMENT

THE ENCLOSED DOCUMENT HAS BEEN RECORDED BY THE ASSIGNMENT DIVISION OF THE U.S. PATENT AND TRADEMARK OFFICE. A COMPLETE MICROFILM COPY IS AVAILABLE AT THE ASSIGNMENT SEARCH ROOM ON THE REEL AND FRAME NUMBER REFERENCED BELOW.

PLEASE REVIEW ALL INFORMATION CONTAINED ON THIS NOTICE. THE INFORMATION CONTAINED ON THIS RECORDATION NOTICE REFLECTS THE DATA PRESENT IN THE PATENT AND TRADEMARK ASSIGNMENT SYSTEM. IF YOU SHOULD FIND ANY ERRORS OR HAVE QUESTIONS CONCERNING THIS NOTICE, YOU MAY CONTACT THE EMPLOYEE WHOSE NAME APPEARS ON THIS NOTICE AT 703-308-9723. PLEASE SEND REQUEST FOR CORRECTION TO: U.S. PATENT AND TRADEMARK OFFICE, ASSIGNMENT DIVISION, BOX ASSIGNMENTS, CG-4, 1213 JEFFERSON DAVIS HWY, SUITE 320, WASHINGTON, D.C. 20231.

RECORDATION DATE: 03/10/1998

REEL/FRAME: 9039/0091
NUMBER OF PAGES: 3

BRIEF: ASSIGNMENT OF ASSIGNOR'S INTEREST (SEE DOCUMENT FOR DETAILS).

ASSIGNOR:
POURKERMATI, ALI

DOC DATE: 03/04/1998

ASSIGNEE:
AZALEA MICROELECTRONICS CORP.
3080 OLCOTT ST. SUITE 130-D
SANTA CLARA, CALIFORNIA 95054

SERIAL NUMBER: 08926576
PATENT NUMBER:

FILING DATE: 09/04/1997
ISSUE DATE:

STEVEN POST, EXAMINER
ASSIGNMENT DIVISION
OFFICE OF PUBLIC RECORDS

FORM PTO-1595
(Rev. 6-93)

03-20-1998

Attorney Docket No. 17822-1-1



U.S. DEPARTMENT OF COMMERCE
Patent and Trademark Office

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MAR 10 1998

To the Honorable Asst. Commissioner

1. Name of conveying party(ies):

ALI POURKERMATI

2. Name and address of receiving party(ies):

Name: AZALEA MICROELECTRONICS CORP.

Internal Address: SUITE 130-D

Street Address: 3080 OLCOTT ST.

City: SANTA CLARA State: CA ZIP: 95054

3. Nature of conveyance:



Assignment



Merger



Security Agreement



Change of Name



Other:

Execution Date: 3/4/98

Additional name(s) & address(es) attached? ☐ Yes ☒ No

4. Application number(s) or patent number(s). **MRD 3.10.98**

If this document is being filed together with a new application, the execution date of the application is:

A. Patent Application No.(s) 08/926,576

B. Patent No.(s)

Additional numbers attached? ☐ Yes ☒ No

5. Name and address of party to whom correspondence concerning document should be mailed:

Name: Babak S. Sani
TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
(415) 576-0200

6. Total number of applications and patents involved: **1**

7. Total fee (37 CFR 3.41):..... \$ 40.00



Enclosed



Charge Fees to Deposit Account



Charge any additional fees associated with this paper or during the pendency of this application, or credit any overpayment, to deposit account

8. Deposit account number: 20-1430

03/20/1998 DCDATES 00000026 MAR:201430 08926576
01 FC:581 40.00 CH

DO NOT USE THIS SPACE

9. Statement and signature.

To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.

Babak S. Sani

Name of Person Signing

Signature

3/9/98

Date

Atty. Reg. No. 37,495

Total number of pages including cover sheet, attachments, and document: **3**

10. Change Correspondence Address to that of Part 5? ☒ Yes ☐ No

OMB No. 0651-0011 (exp. 4/94)

Mail documents to be recorded with required cover sheet information to:

Do not detach this portion

Asst. Commissioner for Patents
Box Assignments
Washington, D.C. 20231

Attorney Docket No. 17822-1-1

ASSIGNMENT OF PATENT APPLICATION

SOLE

WHEREAS, ALI POURKERAMATI of 3979 Brookline Way, Redwood City, CA 94062, hereinafter referred to as "Assignor," is the inventor of the invention described and set forth in the below identified application for United States Letters Patent:

Title of the Invention: **SERIAL FLASH MEMORY**

Date(s) of execution of Declaration: 3-4-98

Filing date: 9/4/97 Application No.: 08/926,576; and

WHEREAS, AZALEA MICROELECTRONICS CORP. a California corporation, located at 3080 Olcott Street, Suite 130-D, Santa Clara, CA 95054, hereinafter referred to as "Assignee," is desirous of acquiring an interest in the invention and application and in any Letters Patent and Registrations which may be granted on the same;

For good and valuable consideration, receipt of which is hereby acknowledged by Assignor, Assignor has assigned, and by these presents does assign to Assignee all right, title and interest in and to the invention and application and to all foreign counterparts (including patent, utility model and industrial designs), and in and to any Letters Patent and Registrations which may hereafter be granted on the same in the United States and all countries throughout the world, and to claim the priority from the application as provided by the Paris Convention. The right, title and interest is to be held and enjoyed by Assignee and Assignee's successors and assigns as fully and exclusively as it would have been held and enjoyed by Assignor had this assignment not been made, for the full term of any Letters Patent and Registrations which may be granted thereon, or of any division, renewal, continuation in whole or in part, substitution, conversion, reissue, prolongation or extension thereof.

Assignor further agrees that Assignor will, without charge to Assignee, but at Assignee's expense, (a) cooperate with Assignee in the prosecution of U.S. Patent applications and foreign counterparts on the invention and any improvements, (b) execute, verify, acknowledge and deliver all such further papers, including patent applications and instruments of transfer and (c) perform such other acts as Assignee lawfully may request to obtain or maintain Letters Patent and Registrations for the invention and improvements in any and all countries, and to vest title thereto in Assignee, or Assignee's successors and assigns.

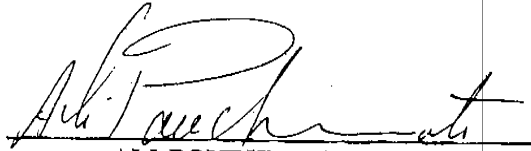
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IN TESTIMONY WHEREOF, Assignor has signed his/her name on the date indicated.

Date: 3-4-98


ALI POURKERAMATI

STATE OF _____

COUNTY OF _____

On _____, before me, _____,
a Notary Public, personally appeared ALI POURKERAMATI, personally known to me
(or proved to me on the basis of satisfactory evidence) to be the person whose name is
subscribed to the within instrument and acknowledged to me that he/she executed the same
in his/her authorized capacity, and that by his/her signature on the instrument the person,
or the entity upon behalf of which the person acted, executes the instrument.

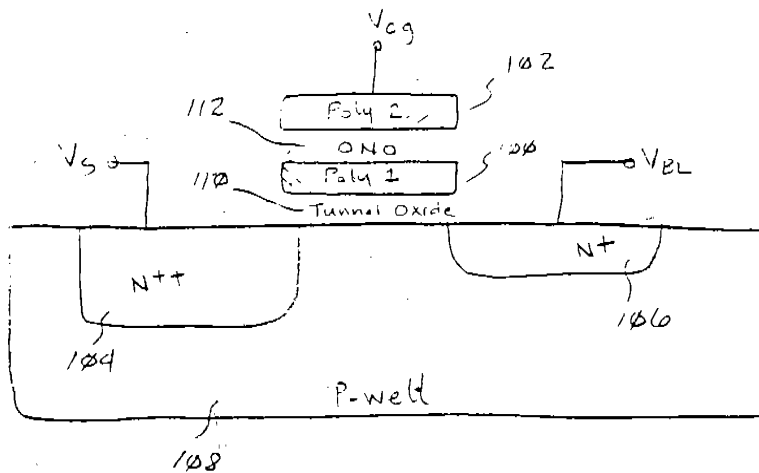
WITNESS my hand and official seal.

Signature _____ (Seal)

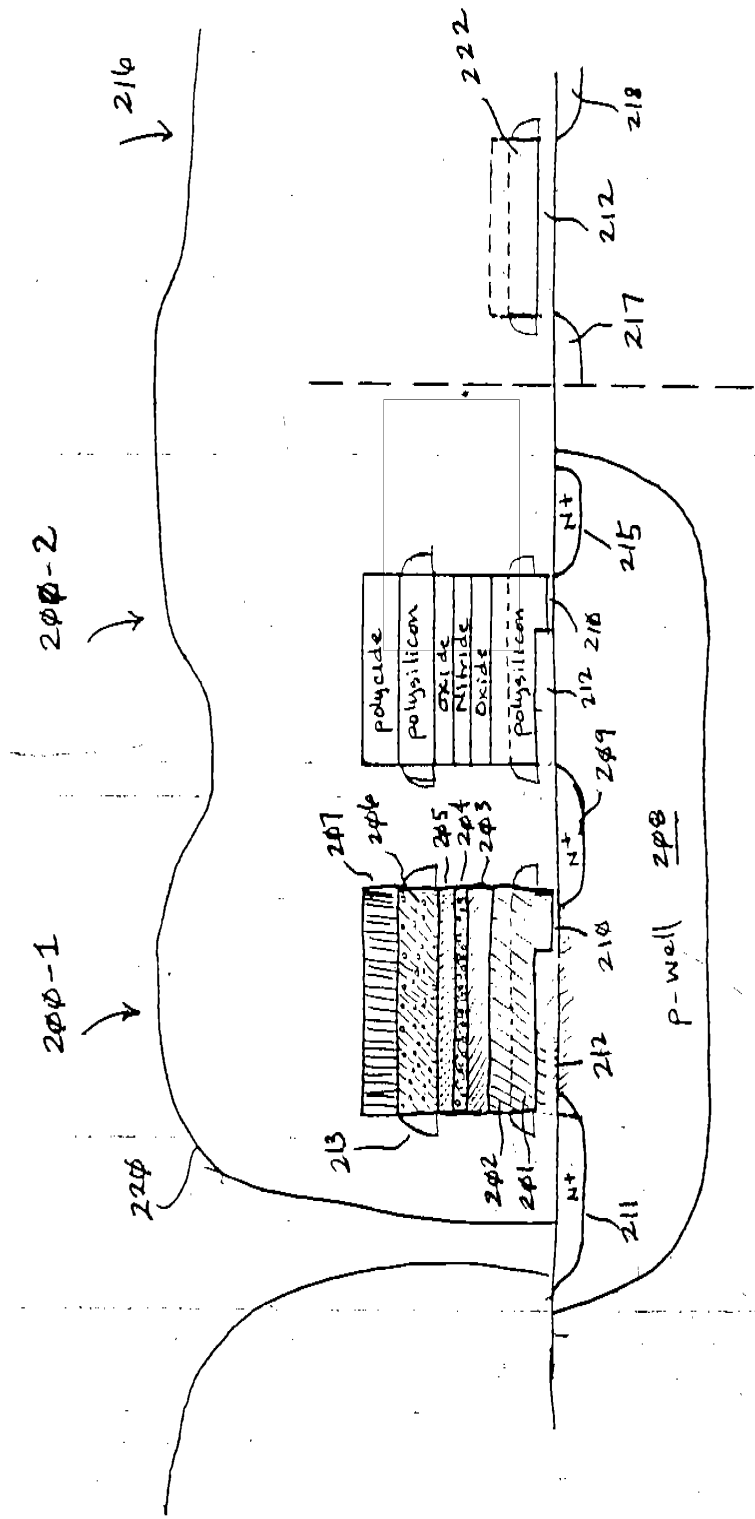
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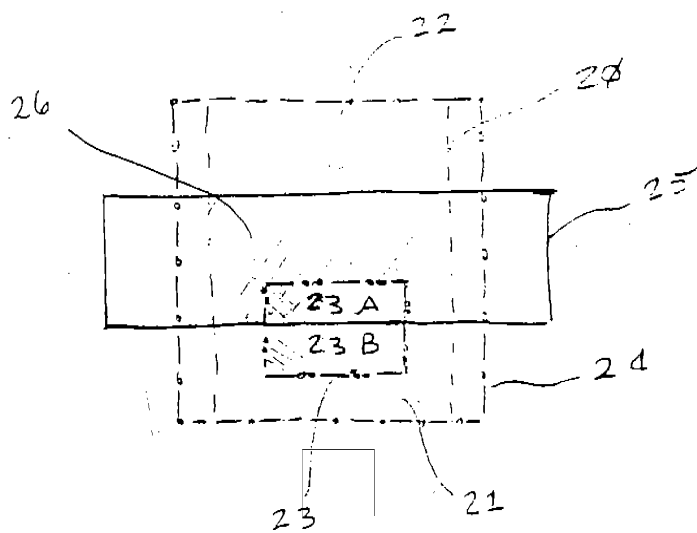


- FIGURE 1 -
(PRIOR ART)

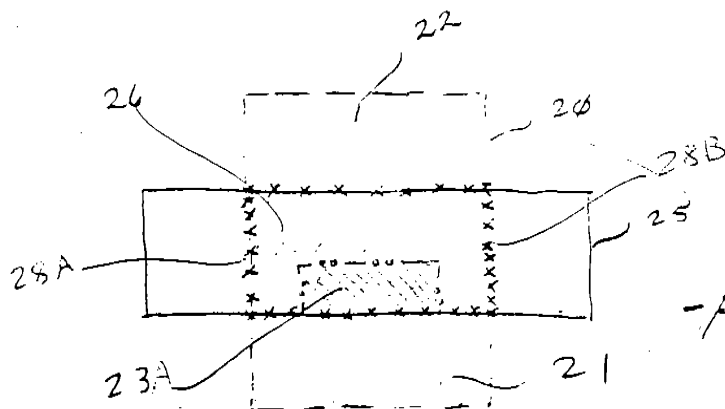


P-substrate 214

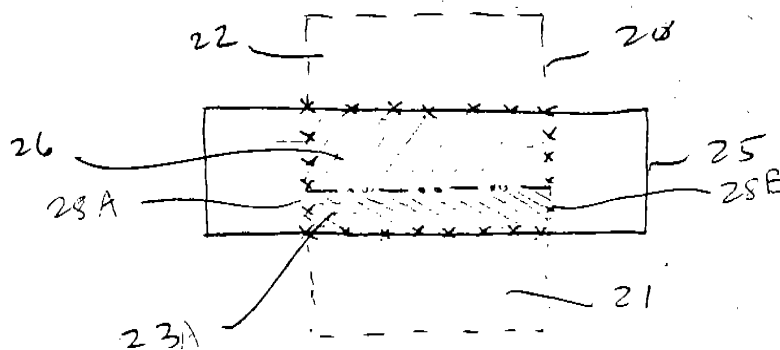
- FIG. 2 -



- FIG. 2A -



- FIG. 2B -

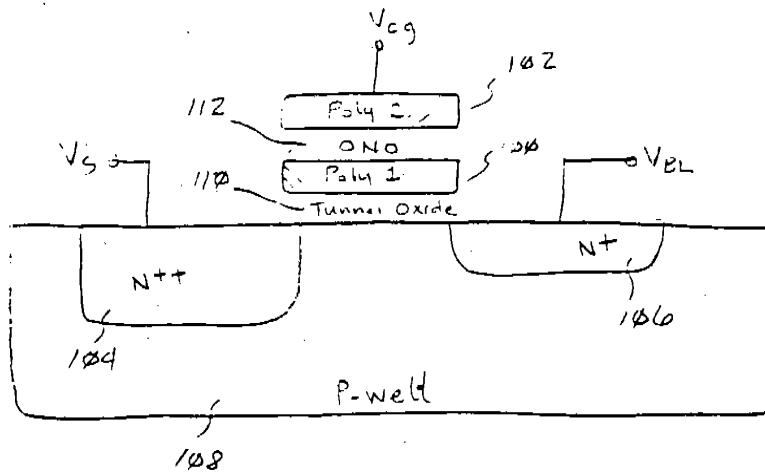


- FIG. 2C -

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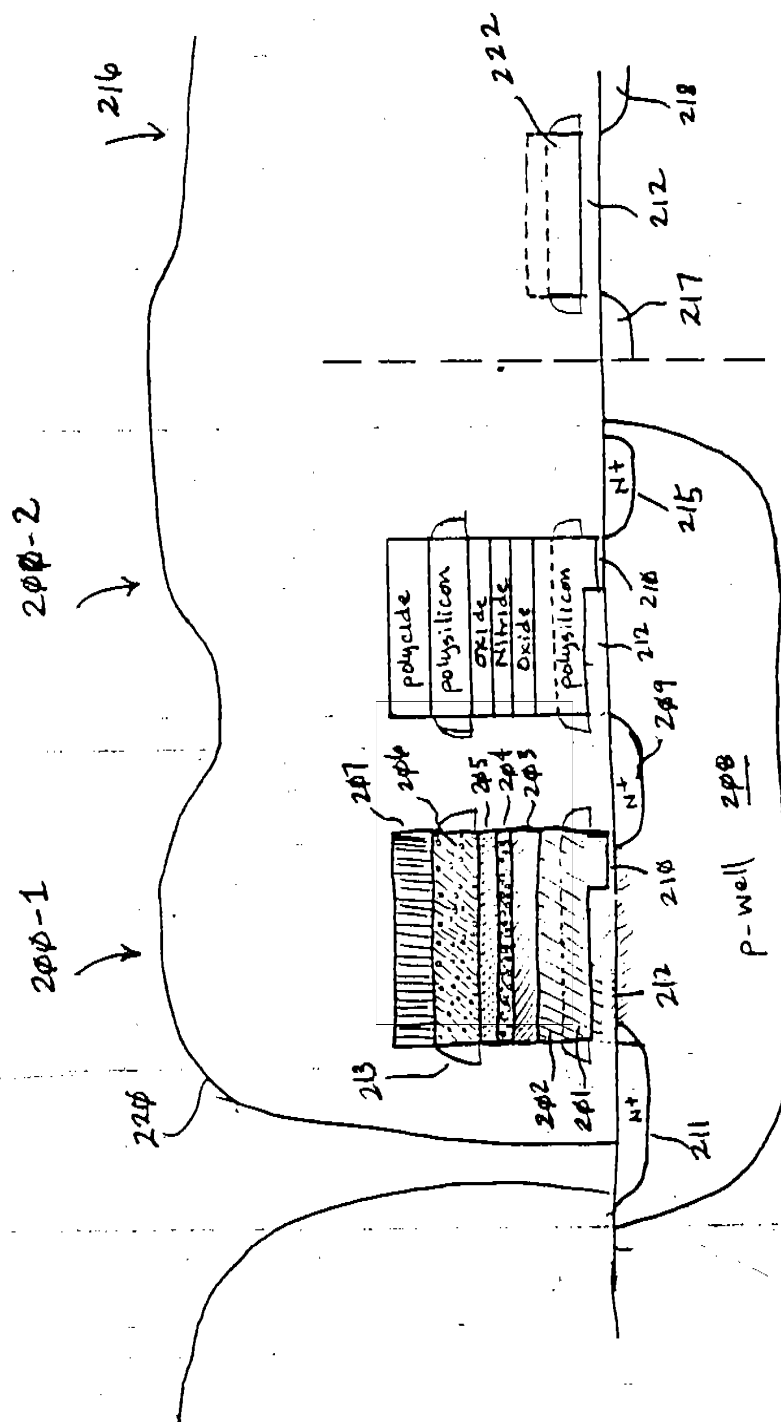


- FIGURE 1 -
(PRIOR ART)

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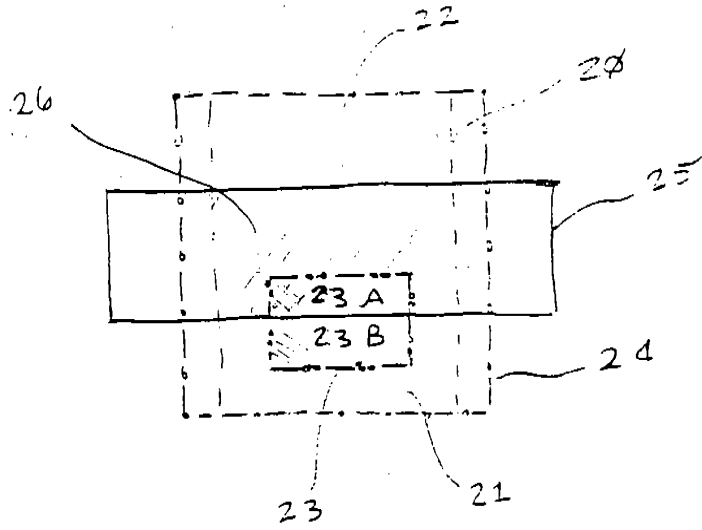


22-141 50 SHEETS
22-142 100 SHEETS
22-144 200 SHEETS

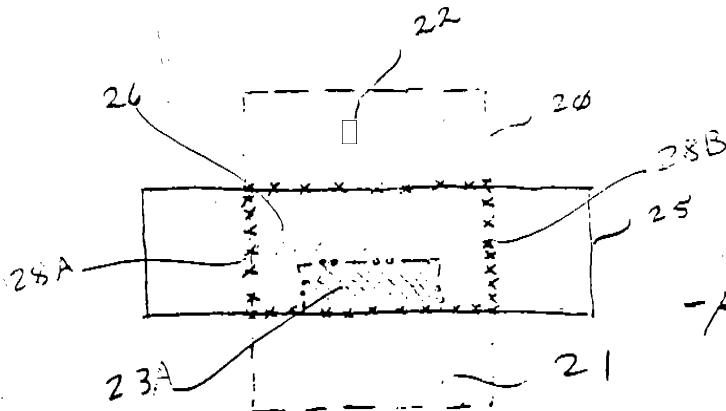


p-substrate 214

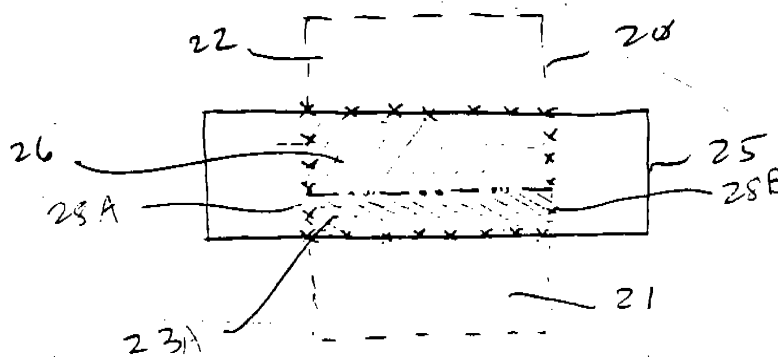
-FIG. 3-



- FIG. 2A -

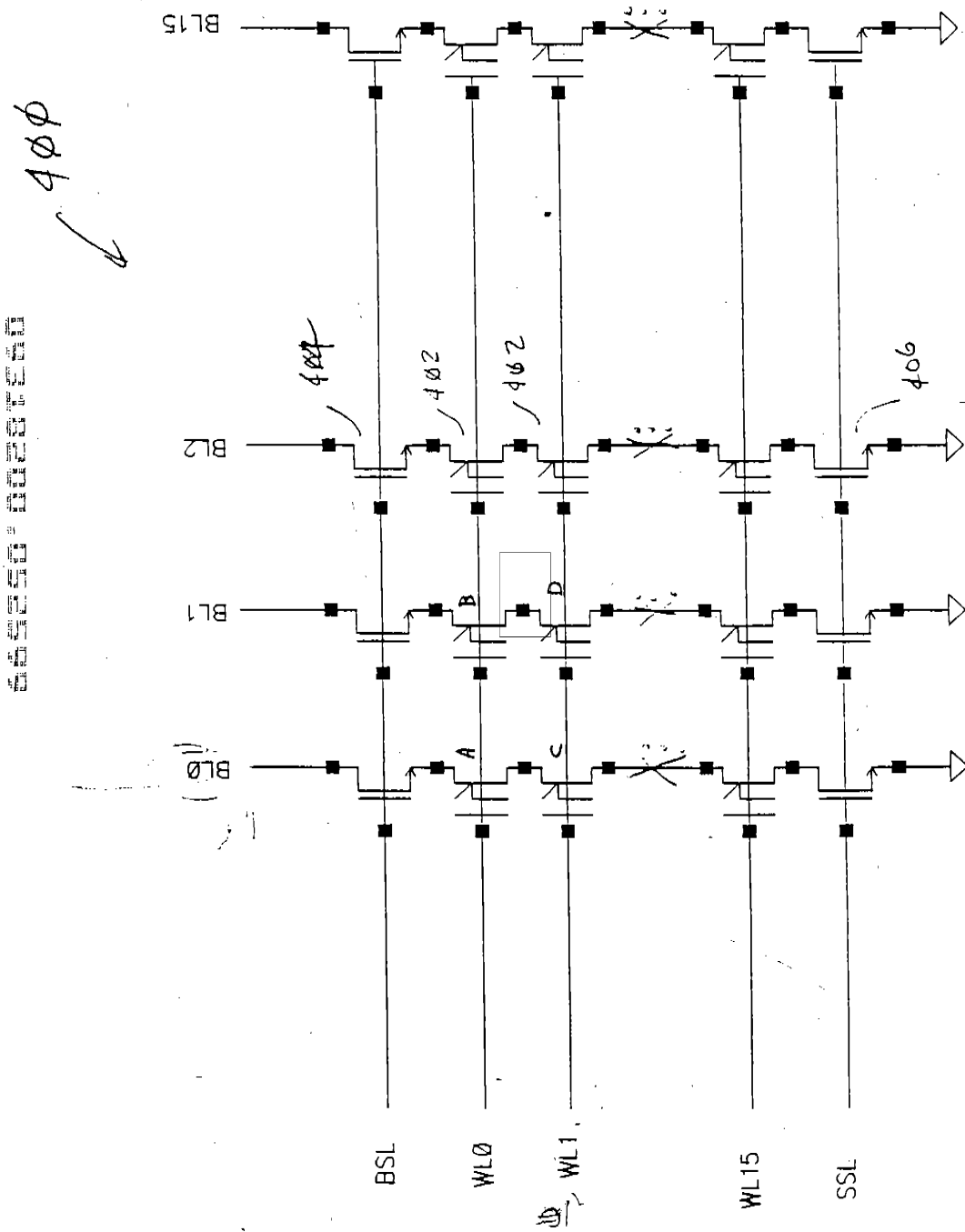


- FIG. 2B -



- FIG. 2C -

PRINT OF DRAWING
AS ORIGINALLY F



-FIGURE 4-

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

Assistant Commissioner for Patents
Washington, D.C. 20231

On May 25, 1999

TOWNSEND and TOWNSEND and CREW LLP

By: Sherry Barton

2/2.5.5
P-25-99
17822-1-2US
ALI POURKERAMATI

jc511 U.S. PTO
09/318200
05/25/99

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

ALI POURKERAMATI

Application No.: NEW

Filed: May 25, 1999

For: SERIAL FLASH MEMORY

Examiner: Trong Phan

Art Unit: 2818

INFORMATION DISCLOSURE
STATEMENT UNDER 37 CFR §1.97 and
§1.98

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

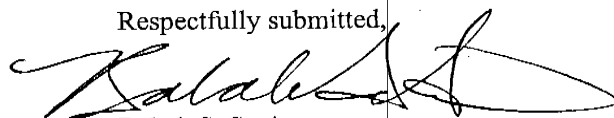
The references cited on attached form PTO-1449 are being called to the attention of the Examiner. Copies of the references are enclosed. It is respectfully requested that the cited information be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "references cited" on any patent to issue therefrom.

ALI POURKERAMATI
Application No.: NEW
Page 2

PATENT

Applicant believes that no fee is required for submission of this statement, since it is being submitted prior to the first Office Action. However, if a fee is required, the Commissioner is authorized to deduct such fee from the undersigned's Deposit Account No. 20-1430. Please deduct any additional fees from, or credit any overpayment to, the above-noted Deposit Account.

Respectfully submitted,



Babak S. Sani
Reg. No. 37,495

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: (415) 576-0200
Fax: (415) 576-0300

SF 221973 v1

FORM PTO-1449 (Modified)		Docket 17822-1-2		Application No.: NEW	
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		Applicant: ALI POURKERAMATI		09/318,100	
		Filing Date: May 25, 1999		Group: 2818	
Reference Designation		U.S. PATENT DOCUMENTS			Page 1
Examiner Initial	Document No.	Date	Name	Class	Filing Date (If Appropriate)
AA TP	4,894,402	Jan. 1990	Hsia et al.	257	321
AB TP	4,924,119	May 1990	Lee	257	321
AC TP	5,008,721	April 1991	Gill et al.	365	185.33
AD TP	5,216,270	June 1993	Kaya et al.	257	321
AE TP	5,460,991	Oct. 1995	Hong	438	261
AF TP	5,666,307	Sept. 1997	Chang	365	185.33
AG TP	5,734,609	March 1998	Choi et al.	365	185.17
AH TP	5,838,616	Nov. 1998	Randazzo	365	185.26
AI					
FOREIGN PATENT DOCUMENTS					
	Document No.	Date	Country	Class	Translation (Yes/No)
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)					
TP AJ	"Semiconductor Memories," Betty Price, Texas Instruments USA, 2 nd Ed., 1983, 1991, John Wiley & Sons, Chichester, New York, Brisbane, Toronto, Singapore, pp. 586-604				
TP AK	"A 3.3 V 32 Mb NAND Flash Memory with Incremental Step Pulse Programming Scheme," Suh et al., <u>IEEE Journal of Solid-State Circuits</u> , Vol. 30, No. 11, 11/95, pp. 1149-1156				
TP AL	"A 35 ns Cycle Time 3.3 V Only 32 Mb NAND Flash EEPROM," Iwata et al., <u>IEEE Journal of Solid-State Circuits</u> , Vol. 30, No. 11, 11/95, pp. 1157-1162				
TP AM	"Advanced Salicided EECMOS Technology for Complex PLDS," Advanced Micro Devices, USA, <u>The 14th Annual IEEE Nonvolatile Semiconductor Memory Workshop</u> , Monterey, CA 8/13-16, 1995				
TP AN	"Process Technology and Device Built in Reliability in NOR Virtual Ground (NVG TM) Flash Memories," National Semiconductor, U.S.A., <u>The 14th Annual IEEE Nonvolatile Semiconductor Memory Workshop</u> , Monterey, CA 8/13-16, 1995				
TP AO	"High Density 'AND' Cell Technology for 32Mbit Flash Memory," Hitachi, Japan / Mitsubishi, Japan, <u>The 14th Annual IEEE Nonvolatile Semiconductor Memory Workshop</u> , Monterey, CA 8/13-16, 1995				
TP AP	"Effective In-Process Plasma Damage Screening of Tunnel Oxide for Nonvolatile Memory Applications," Motorola, U.S.A., <u>The 14th Annual IEEE Nonvolatile Semiconductor Memory Workshop</u> , Monterey, CA 8/13-16, 1995				
TP AQ	"Sidewall Sealing Effects on Flash EEPROM," SGS-Thomson, Italy, <u>The 14th Annual IEEE Nonvolatile Semiconductor Memory Workshop</u> , Monterey, CA 8/13-16, 1995				
EXAMINER TRONG PHAN DATE CONSIDERED 11/15/99					
PRIMARY EXAMINER					

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

I hereby certify that the response is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

Assistant Commissioner for Patents
Washington, D.C. 20231

On May 25, 1999

TOWNSEND and TOWNSEND and CREW LLP

By: Sherry Barton

PATENT
Attorney Docket No.: 17822-1-2US

3/Pre Amended
A
8.25.99

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

ALI POURKERMATI

Application No.: NEW

Filed: May 25, 1999

For: SERIAL FLASH MEMORY

Examiner: Unassigned

Art Unit: Unassigned

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination of the above-referenced application, please enter the following amendments and remarks.

IN THE CLAIMS:

Please cancel claims 1-7, and add new claims 11-13. For convenient reference, all pending claims are reproduced below.

- 1 8. An array of flash memory cells comprising:
2 a plurality of columns of serially connected flash memory cells, each
3 memory cell having a gate terminal;

4 a plurality of bit lines respectively coupled to drain side of said plurality
5 of columns of memory cells via a respective plurality of bit line select transistors, said plurality
6 of bit line select transistors having gate terminals coupled to a bit line select control line;
7 a plurality of word lines, each one coupling to a gate terminal of one
8 memory cell in each of said plurality of columns to from rows of memory cells with common
9 gate terminals; and

10 a plurality of source select transistors respectively coupling a source side
11 of said plurality of columns of memory cells to a logic low voltage, and having gate terminals
12 coupled to a source select control line,

13 wherein, during programming:

14 a logic high voltage is applied to said bit line select control line to turn
15 on bit line select transistors,

16 a logic low voltage is applied to source select control line to turn off
17 source select transistors;

18 a logic low voltage is applied to a selected bit line while a logic high
19 voltage is applied to unselected bit lines, and

20 a logic high voltage is applied to unselected word lines, while a boosted
21 positive voltage is applied to a selected word line.

1 9. An array of flash memory cells comprising:

2 a plurality of columns of serially connected flash memory cells, each
3 memory cell having a gate terminal;

4 a plurality of bit lines respectively coupled to drain side of said plurality
5 of columns of memory cells via a respective plurality of bit line select transistors, said plurality
6 of bit line select transistors having gate terminals coupled to a bit line select control line;

7 a plurality of word lines, each one coupling to gate terminal of one
8 memory cell in each of said plurality of columns to from rows of memory cells with common
9 gate terminals; and

10 a plurality of source select transistors respectively coupling a source side
11 of said plurality of columns of memory cells to a logic low voltage, and having gate terminals
12 coupled to a source select control line,

13 wherein, during erase:

14 a logic high voltage is applied to said bit line select control line to turn
15 on bit line select transistors,

16 a logic low voltage is applied to source select control line to turn off
17 source select transistors;

18 a logic high voltage is applied to a selected bit line while a logic low
19 voltage is applied to unselected bit lines, and

20 a logic high voltage is applied to unselected word lines, while a boosted
21 negative voltage is applied to a selected word line.

1 10. An array of flash memory cells comprising:

2 a plurality of columns of serially connected flash memory cells, each
3 memory cell having a gate terminal;

4 a plurality of bit lines respectively coupled to drain side of said plurality
5 of columns of memory cells via a respective plurality of bit line select transistors, said plurality
6 of bit line select transistors having gate terminals coupled to a bit line select control line;

7 a plurality of word lines, each one coupling to a gate terminal of one
8 memory cell in each of said plurality of columns to form rows of memory cells with common
9 gate terminals; and

10 a plurality of source select transistors respectively coupling a source
11 side of said plurality of columns of memory cells to a logic low voltage, and having gate
12 terminals coupled to a source select control line,

13 wherein, during program inhibit a logic low voltage is applied to said
14 bit line select control line, source select control line, and bit lines, while a logic high voltage is
15 applied to word lines.

1 ~~4-11~~ (New) A method of operating a flash memory device wherein
2 programming memory cells is accomplished by the steps of:
3 applying a logic high voltage to a bit line select control line to turn on
4 bit line select transistors,
5 applying a logic low voltage to a source select control line to turn off
6 source select transistors;
7 applying a logic low voltage to a selected bit line while a logic high
8 voltage is applied to unselected bit lines, and
9 applying a logic high voltage to unselected word lines, while a boosted
10 positive voltage is applied to a selected word line.

AI TP 1 ~~5-12~~ (New) The method of operating a ~~flash~~ flash memory device as in claim ~~11~~ 4
2 wherein erasing memory cells is accomplished by the steps of:
3 applying a logic high voltage to a bit line select control line to turn on
4 bit line select transistors,
5 applying a logic low voltage to a source select control line to turn off
6 source select transistors;
7 applying a logic high voltage to a selected bit line while a logic low
8 voltage is applied to unselected bit lines, and
9 applying a logic high voltage to unselected word lines, while a boosted
10 negative voltage is applied to a selected word line.

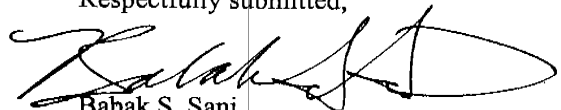
TP 1 ~~6-13~~ (New) The method of operating a ~~flash~~ flash memory device as in claim ~~12~~ 5
2 wherein program inhibit is accomplished by a step of applying a logic low voltage to a bit line
3 select control line, source select control line, and bit lines, while a logic high voltage is applied
4 to word lines. --

ALI POURKEHATI
Application No.: NEW
Page 5

PATENT

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



Babak S. Sani
Reg. No. 37,495

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Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: (415) 576-0200
Fax: (415) 576-0300
BSS:sb

SF 222891 v1



**UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office**

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

AK

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/318,200 05/25/99 POURKERAMATI

A 17822-1-2US

MM12/1116
TOWNSEND AND TOWNSEND AND CREW LLP
8TH FLOOR
TWO EMBARCADERO CENTER
SAN FRANCISCO CA 94111-3834

EXAMINER

PHAN, T
ART UNIT PAPER NUMBER

2818
DATE MAILED:

11/16/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Notice of AllowabilityApplication No.
09/318,200Applicant(s)
POURKERAMATIExaminer
TRONG PHANGroup Art Unit
2818

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance and Issue Fee Due or other appropriate communication will be mailed in due course.

- ☒ This communication is responsive to 5/25/99.
- ☒ The allowed claim(s) is/are 8-13.
- ☒ The drawings filed on May 25, 1999 are acceptable.
- ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
- ☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been
- ☐ received.
- ☐ received in Application No. (Series Code/Serial Number) _____.
- ☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

- ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

A SHORTENED STATUTORY PERIOD FOR RESPONSE to comply with the requirements noted below is set to EXPIRE **THREE MONTHS** FROM THE "DATE MAILED" of this Office action. Failure to timely comply will result in ABANDONMENT of this application. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

- ☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.
- ☒ Applicant **MUST** submit **NEW FORMAL DRAWINGS**
- ☒ because the originally filed drawings were declared by applicant to be informal.
- ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review, PTO-948, attached hereto or to Paper No. _____.
- ☐ including changes required by the proposed drawing correction filed on _____, which has been approved by the examiner.
- ☐ including changes required by the attached Examiner's Amendment/Comment.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the reverse side of the drawings. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

- ☐ Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Any response to this letter should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included.

Attachment(s)

- ☒ Notice of References Cited, PTO-892
- ☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 4
- ☒ Notice of Draftsperson's Patent Drawing Review, PTO-948
- ☐ Notice of Informal Patent Application, PTO-152
- ☐ Interview Summary, PTO-413
- ☐ Examiner's Amendment/Comment
- ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
- ☒ Examiner's Statement of Reasons for Allowance

Phan Trong

**TRONG PHAN
PRIMARY EXAMINER**

Application/Control Number: 09/318,200

Page 2

Art Unit: 2818

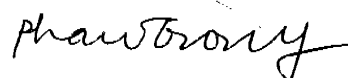
REASONS FOR ALLOWANCE

1. The following is an examiner's statement of reasons for allowance:

The flash memory device having steps of operating as recited in claims 8-13 has not been found in the prior art references.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trong Phan whose telephone number is (703) 308-4870.



TRONG PHAN
PRIMARY EXAMINER

November 15, 1999

09/318200

NOTICE OF DRAFTSPERSON'S
PATENT DRAWING REVIEWThe drawing(s) filed (insert date) 5/25/99 are:A. ☐ approved by the Draftsperson under 37 CFR 1.84 or 1.152.B. ☐ objected to by the Draftsperson under 37 CFR 1.84 or 1.152 for the reasons indicated below. The Examiner will require submission of new, corrected drawings when necessary. Corrected drawing must be submitted according to the instructions on the back of this notice.

<p>1. DRAWINGS. 37 CFR 1.84(a): Acceptable categories of drawings:</p> <p>Black ink. Color.</p> <p>Color drawings are not acceptable until petition is granted. Fig(s) _____</p> <p>Pencil and non black ink not permitted. Fig(s) _____</p> <p>2. PHOTOGRAPHS. 37 CFR 1.84 (b)</p> <p>1 full-tone set is required. Fig(s) _____</p> <p>Photographs not properly mounted (must use bristol board or photographic double-weight paper). Fig(s) _____</p> <p>Poor quality (half-tone). Fig(s) _____</p> <p>3. TYPE OF PAPER. 37 CFR 1.84(e)</p> <p>Paper not flexible, strong, white, and durable. Fig(s) _____</p> <p>Erasures, alterations, overwritings, interlineations, folds, copy machine marks not accepted. Fig(s) _____</p> <p>Mylar, velum paper is not acceptable (too thin). Fig(s) _____</p> <p>4. SIZE OF PAPER. 37 CFR 1.84(f): Acceptable sizes:</p> <p>21.0 cm by 29.7 cm (DIN size A4)</p> <p>21.6 cm by 27.9 cm (8 1/2 x 11 inches)</p> <p>All drawing sheets not the same size. Sheet(s) _____</p> <p>Drawings sheets not an acceptable size. Fig(s) _____</p> <p>5. MARGINS. 37 CFR 1.84(g): Acceptable margins:</p> <p>Top 2.5 cm Left 2.5cm Right 1.5 cm Bottom 1.0 cm</p> <p>SIZE: A4 Size</p> <p>Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm</p> <p>SIZE: 8 1/2 x 11</p> <p>Margins not acceptable. Fig(s) _____</p> <p>Top (T) _____ Left (L) _____</p> <p>Right (R) _____ Bottom (B) _____</p> <p>6. VIEWS. 37 CFR 1.84(h)</p> <p>REMINDER: Specification may require revision to correspond to drawing changes.</p> <p>Partial views. 37 CFR 1.84(h)(2)</p> <p>Brackets needed to show figure as one entity. Fig(s) _____</p> <p>Views not labeled separately or properly. Fig(s) _____</p> <p>Enlarged view not labeled separately or properly. Fig(s) _____</p> <p>7. SECTIONAL VIEWS. 37 CFR 1.84 (h)(3)</p> <p>Hatching not indicated for sectional portions of an object. Fig(s) _____</p> <p>Sectional designation should be noted with Arabic or Roman numbers. Fig(s) _____</p>	<p>8. ARRANGEMENT OF VIEWS. 37 CFR 1.84(i)</p> <p>Words do not appear on a horizontal, left-to-right fashion when page is either upright or turned so that the top becomes the right side, except for graphs. Fig(s) _____</p> <p>9. SCALE. 37 CFR 1.84(k)</p> <p>Scale not large enough to show mechanism without crowding when drawing is reduced in size to two-thirds in reproduction. Fig(s) _____</p> <p>10. CHARACTER OF LINES, NUMBERS, & LETTERS. 37 CFR 1.84(i)</p> <p>Lines, numbers & letters not uniformly thick and well defined, clean, durable, and black (poor line quality). Fig(s) <u>All</u></p> <p>11. SHADING. 37 CFR 1.84(m)</p> <p>Solid black areas pale. Fig(s) _____</p> <p>Solid black shading not permitted. Fig(s) _____</p> <p>Shade lines, pale, rough and blurred. Fig(s) _____</p> <p>12. NUMBERS, LETTERS, & REFERENCE CHARACTERS. 37 CFR 1.84(p)</p> <p>Numbers and reference characters not plain and legible. Fig(s) <u>All</u></p> <p>Figure legends are poor. Fig(s) <u>All</u></p> <p>Numbers and reference characters not oriented in the same direction as the view. 37 CFR 1.84(p)(1) Fig(s) _____</p> <p>English alphabet not used. 37 CFR 1.84(p)(2) Fig(s) _____</p> <p>Numbers, letters and reference characters must be at least .32 cm (1/8 inch) in height. 37 CFR 1.84(p)(3) Fig(s) _____</p> <p>13. LEAD LINES. 37 CFR 1.84(q)</p> <p>Lead lines cross each other. Fig(s) _____</p> <p>Lead lines missing. Fig(s) _____</p> <p>14. NUMBERING OF SHEETS OF DRAWINGS. 37 CFR 1.84(i)</p> <p>Sheets not numbered consecutively, and in Arabic numerals beginning with number 1. Sheet(s) _____</p> <p>15. NUMBERING OF VIEWS. 37 CFR 1.84(u)</p> <p>Views not numbered consecutively, and in Arabic numerals, beginning with number 1. Fig(s) _____</p> <p>16. CORRECTIONS. 37 CFR 1.84(w)</p> <p>Corrections not made from prior PTO-948 dated _____</p> <p>17. DESIGN DRAWINGS. 37 CFR 1.152</p> <p>Surface shading shown not appropriate. Fig(s) _____</p> <p>Solid black shading not used for color contrast. Fig(s) _____</p>
<p>COMMENTS <u>Remove border lines</u></p>	

REVIEWER

CB/R

DATE

6/22/99

TELEPHONE NO.

703 3038406

ATTACHMENT TO PAPER NO.

4

FORM PTO-892		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		SERIAL NO. 09/318,200	GROUP ART UNIT 2818	ATTACHMENT TO PAPER NO.	4
NOTICE OF REFERENCES CITED				APPLICANT(S) POURKERAMATI			
U.S. PATENT DOCUMENTS							
*		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
*	A	5,898,616	4/1999	Ono	365	185.17	
*	B	5,978,267	11/1999	Chen et al.	365	185.17	
*	C	5,909,392	6/1999	Chang et al	365	185.17	
	D						
	E						
	F						
	G						
	H						
	I						
	J						
	K						
FOREIGN PATENT DOCUMENTS							
*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS
	L						
	M						
	N						
	O						
	P						
	Q						
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)							
	R						
	S						
	T						
	U						
EXAMINER TRONG PHAN		DATE November 15, 1999		Form892ccs2106b			
* A copy of this reference is not being furnished with this office action. (See Manual of Patent Examining Procedure, section 707.05(a).)							



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

NOTICE OF ALLOWANCE AND ISSUE FEE DUE

PM12/1116
TOWNSEND AND TOWNSEND AND CREW LLP
8TH FLOOR
TWO EMERALD CENTER
SAN FRANCISCO CA 94111-3834

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
09/310,200	05/25/99	006	PHAN, T	2816 11/16/99
First Named Applicant	FOURTEENTH	35 USC 134(b) Term ext. to	A. Davis	

TITLE OF INVENTION SERIAL FLASH MEMORY

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
2 17503-1-206	365-185,260	E 33	UTILITY	YES	\$605.00	02/16/00

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.

HOW TO RESPOND TO THIS NOTICE:

- I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is changed, pay twice the amount of the FEE DUE shown above and notify the Patent and Trademark Office of the change in status, or

B. If the status is the same, pay the FEE DUE shown above.
- If the SMALL ENTITY is shown as NO:

A. Pay FEE DUE shown above, or

B. File verified statement of Small Entity Status before, or with, payment of 1/2 the FEE DUE shown above.
- II. Part B-Issue Fee Transmittal should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B Issue Fee Transmittal should be completed and returned. If you are charging the ISSUE FEE to your deposit account, section "4b" of Part B-Issue Fee Transmittal should be completed and an extra copy of the form should be submitted.
- III. All communications regarding this application must give application number and batch number. Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PATENT AND TRADEMARK OFFICE COPY

PTOL-85 (REV. 10-96) Approved for use through 08/30/99. (0851-0033)

*U.S. GPO: 1999-454-457/24601



#5M

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Box Issue Fee, Assistant Commissioner for Patents, Washington, D.C. 20231, on Feb. 2000

[Signature]

PATENT

Attorney Docket No.: 17822-1-2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

POURKERAMATI

Serial No.: 09/318,200

Filed: 5/25/99

For: SERIAL FLASH MEMORY

Examiner: T. Phan

Art Unit: 2818

Batch No.: E33

LETTER TO OFFICIAL DRAFTSPERSON

Box Issue Fee
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Pursuant to the Notice of Allowability dated November 16, 1999, applicant submits four sheets of formal drawings to be made of record in the above-identified case.

Respectfully submitted,

[Signature]

Babak S. Sani
Reg. No. 37,495

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
(415) 576-0200 / Fax (415) 576-0300
BSS:db
SF 151764 v1

1/4

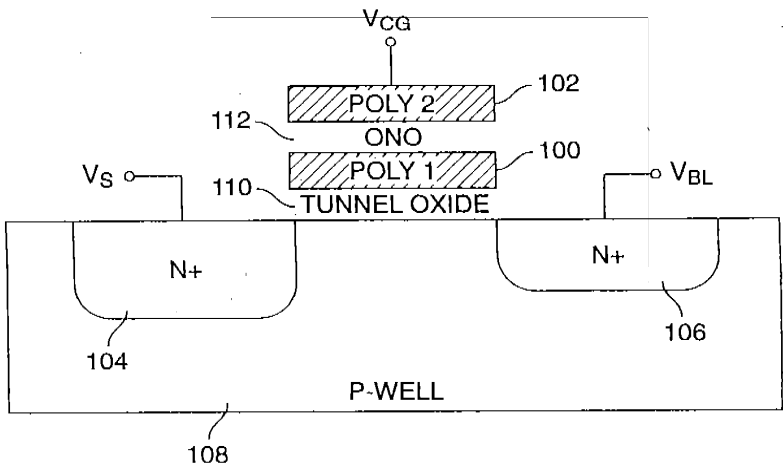


FIG. 1
(PRIOR ART)

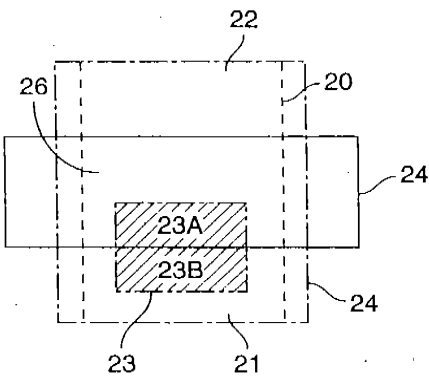


FIG. 2A

2/4

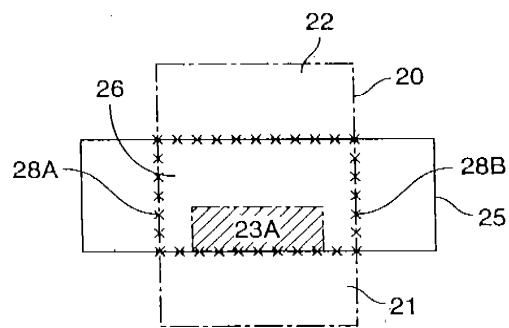


FIG. 2B

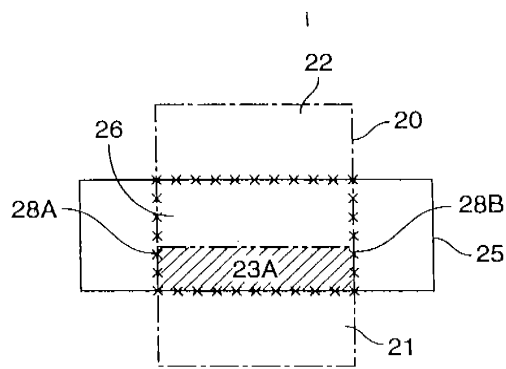


FIG. 2C

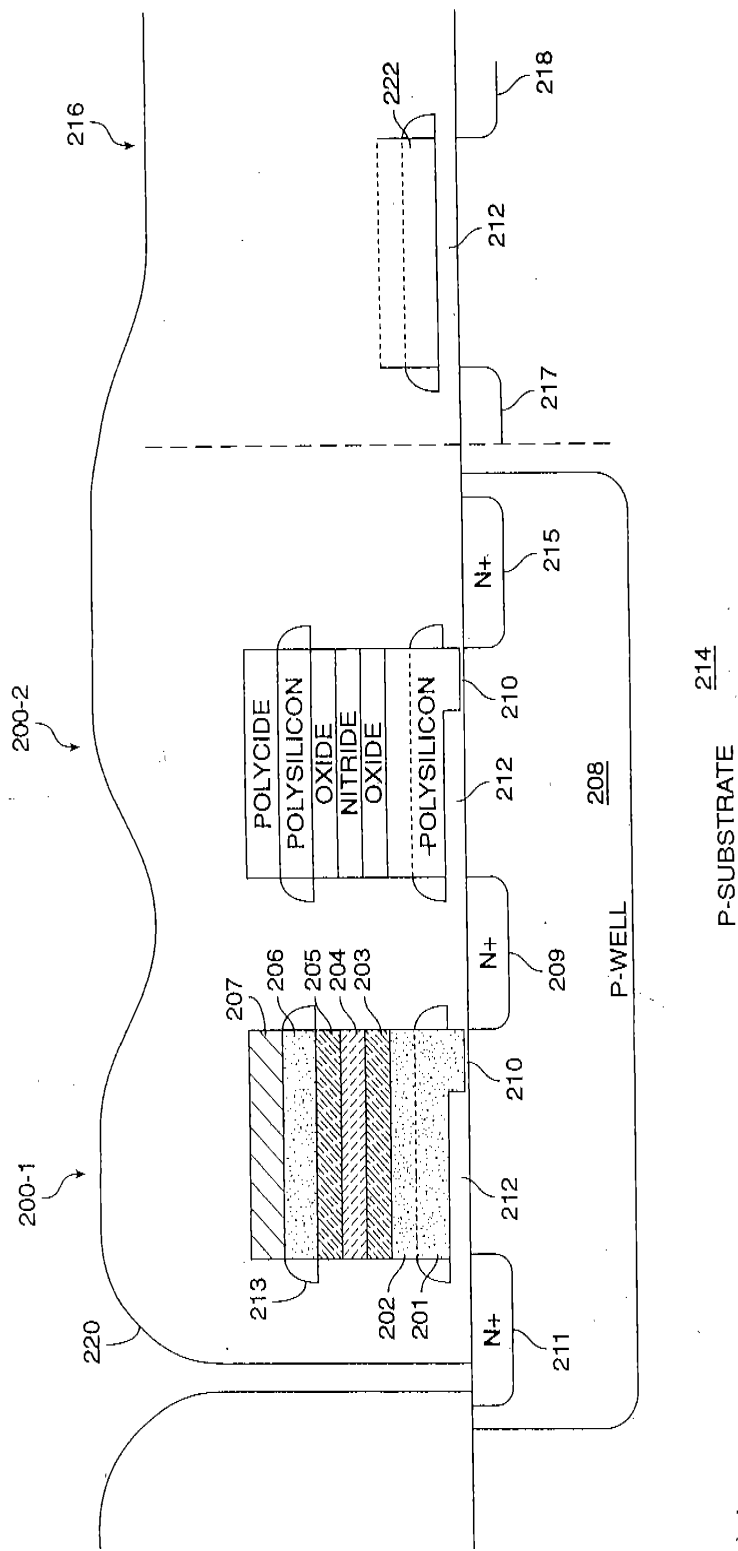


FIG. 3

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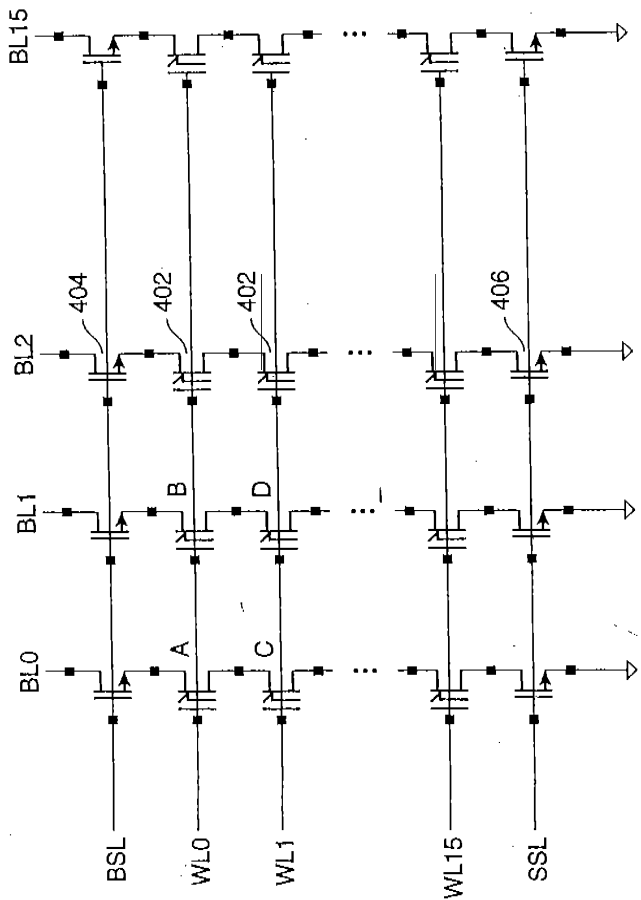


FIG. 4

PART B—ISSUE FEE TRANSMITTAL

complete and mailable form, together with applicable fees, to:

Box ISSUE FEE
Assistant Commissioner for Patents
Washington, D.C. 20231

#B

MAKING INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE. Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Issue Fee Receipt, the Patent Advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

MM12/1116
TOWNSEND AND TOWNSEND AND CREW LLP
8TH FLOOR
TWO EMBARCADERO CENTER
SAN FRANCISCO CA 94111-3834

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Certificate of Mailing

I hereby certify that this Issue Fee Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above on the date indicated below.

D. Bullock

(Depositor's name)

1-28-90

(Signature)

1-28-90

(Date)

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
09/318,200	05/25/99	006	PHAN, T	2818 11/16/99
First Named Applicant	POURKERAMATI,	35 USC 154(b) term ext. =	0 Days.	

TITLE OF INVENTION SERIAL FLASH MEMORY

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
2	17822-1-2US	365-185,260	E33	UTILITY	YES	\$605.00 02/16/00

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.383). Use of PTO form(s) and Customer Number are recommended, but not required.

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" indication form PTO/SB/47) attached.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 RECEIVED
2 60-01111 02 NOV 99
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)
PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the PTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE Azalea Microelectronics

(B) RESIDENCE: (CITY & STATE OR COUNTRY) Santa Clara, CA

Please check the appropriate assignee category indicated below (will not be printed on the patent)
☐ Individual ☒ Corporation or other private group entity ☐ government

4a. The following fees are enclosed (make check payable to Commissioner of Patents and Trademarks):

- ☐ Issue Fee
☐ Advance Order - # of Copies _____

4b. The following fees or deficiency in these fees should be charged to:

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(ENCLOSE AN EXTRA COPY OF THIS FORM)

- ☒ Issue Fee
☒ Advance Order - # of Copies 10

The COMMISSIONER OF PATENTS AND TRADEMARKS IS requested to apply the Issue Fee to the application identified above.

(Authorized Signature) Babak S. Sanjivani

(Date)

1-28-00

NOTE: The Issue Fee will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the Patent and Trademark Office.

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending on the needs of the individual case. Any comments on the amount of time required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND FEES AND THIS FORM TO: Box Issue Fee, Assistant Commissioner for Patents, Washington D.C. 20231

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09/11/2000 10:00:00 AM 00000007 201430 09/11/2000
01 00:00:00 00:00:00
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PTOL-85B (REV.10-96) Approved for use through 06/30/99. OMB 0651-0033

Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

06/29/2005 12:09 FAX 415 576 0300

60-81045

001/003

Atty Docket No. 022193-120120US

PTO FAX NO.: 703-308-5077 and 703 872 9306

ATTENTION: Trong Q PHAN

Group Art Unit: 2818

**OFFICIAL COMMUNICATION
FOR THE STATUS AND ENTITY BRANCH**

CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that the following documents in re Application of, 09/318,200, filed May 25, 1999 for SERIAL FLASH MEMORY are being facsimile transmitted to the Patent and Trademark Office on the date shown below.

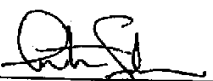
Documents Attached

1. Transmittal Form (1 page)
2. Notification of Loss of Entitlement to Small Entity Status (1 page)

COMPLETED

Number of pages being transmitted, including this page: 3

Dated: June 21, 2005


Katherine Parkas

**PLEASE CONFIRM RECEIPT OF THIS PAPER BY
RETURN FACSIMILE AT (415) 576-0300**

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, CA 94111-3834
Telephone: 415-576-0200
Fax: 415-576-0300

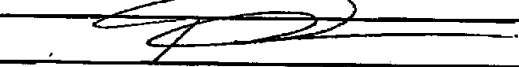
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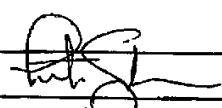
06/29/2005 12:09 FAX 415 576 0300

002/003

TRANSMITTAL FORM <small>(to be used for all correspondence after initial filing)</small>	Application Number	09/318,200
	Filing Date	May 25, 1999
	First Named Inventor	Ali POURKERAMATI
	Art Unit	2818
	Examiner Name	Trong Q PHAN
	Attorney Docket Number	022193-120120US
Total Number of Pages in This Submission		3

ENCLOSURES (Check all that apply)		
<input type="checkbox"/> Fee Transmittal Form <input type="checkbox"/> Fee Attached <input type="checkbox"/> Amendment/Reply <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declaration(s) <input type="checkbox"/> Extension of Time Request <input type="checkbox"/> Express Abandonment Request <input type="checkbox"/> Information Disclosure Statement <input type="checkbox"/> Certified Copy of Priority Document(s) <input type="checkbox"/> Reply to Missing Parts/ Incomplete Application <input type="checkbox"/> Reply to Missing Parts under 37 CFR 1.52 or 1.53	<input type="checkbox"/> Drawing(s) <input type="checkbox"/> Licensing-related Papers <input type="checkbox"/> Petition <input type="checkbox"/> Petition to Convert to a Provisional Application <input type="checkbox"/> Power of Attorney, Revocation Change of Correspondence Address <input type="checkbox"/> Terminal Disclaimer <input type="checkbox"/> Request for Refund <input type="checkbox"/> CD, Number of CD(s) _____ <input type="checkbox"/> Landscape Table on CD	<input type="checkbox"/> After Allowance Communication to TC <input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences <input type="checkbox"/> Appeal Communication to TC (Appeal Notice, Brief, Reply Brief) <input type="checkbox"/> Proprietary Information <input type="checkbox"/> Status Letter <input checked="" type="checkbox"/> Other Enclosure(s) (please identify below): Notification of Loss Of Entitlement to Small Entity Status
Remarks The Commissioner is authorized to charge any additional fees to Deposit Account 20-1430.		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT			
Firm Name	Townsend and Townsend and Crew LLP		
Signature			
Printed name	Patrick R. Jewik		
Date	June 27, 2005	Reg. No.	40,456

CERTIFICATE OF TRANSMISSION/MAILING			
I hereby certify that this correspondence is being facsimile transmitted to the USPTO at (703) 308-5077 on the date shown below. AAA (703) 872-9306			
Signature			
Typed or printed name	Katherine Farkas	Date	June 27, 2005

60526653 v1

06/29/2005 12:10 FAX 415 576 0300

003/003

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JUN 29 2005

PATENT

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attention Status and Entity Branch via facsimile to the following number:
(703) 308-5077 703 872 9300

Attorney Docket No.: 022193-120120US

on 6/29/05

TOWNSEND and TOWNSEND and CREW LLP

By 
Katherine Parkes

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Examiner: Trong Q PHAN
Art Unit: 2818

Serial Number: 09/318,200
Filed: May 25, 1999

NOTIFICATION OF
LOSS OF ENTITLEMENT TO
SMALL ENTITY STATUS

Patent No.: 6,058,045 ✓
Issued: May 2, 2000

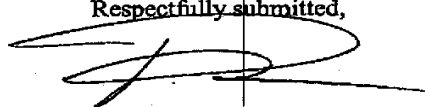
For: SERIAL FLASH MEMORY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 C.F.R. 1.27(g)(2), notification is hereby given that small entity
status is no longer appropriate in connection with the above-identified application. Please note
that the owner of the above referenced patent now qualifies as LARGE entity.

Respectfully submitted,


Patrick Jewik
Reg. No. 40,456

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
(415) 576-0200
Fax (415) 576-0300
PRJ/klf
60526644 v1

PATENT APPLICATION FEE DETERMINATION RECORD
Effective November 10, 1998

Application or Docket Number

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
FOR	NUMBER FILED	NUMBER EXTRA
BASIC FEE		
TOTAL CLAIMS	6 minus 20= *	
INDEPENDENT CLAIMS	4 minus 3= *	1
MULTIPLE DEPENDENT CLAIM PRESENT		

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	* 4	Minus **	=
Independent	* 1	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM			

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus **	=
Independent	*	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM			

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT C	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus **	=
Independent	*	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM			

- * If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

SMALL ENTITY
TYPE ☐

OR
OTHER THAN
SMALL ENTITY

RATE	FEE		RATE	FEE
	380.00	OR		760.00
X\$ 9=		OR	X\$18=	
X39=	39	OR	X78=	✓
+130=		OR	+260=	
TOTAL	419	OR	TOTAL	

SMALL ENTITY

OR
OTHER THAN
SMALL ENTITY

RATE	ADDI- TIONAL FEE		RATE	ADDI- TIONAL FEE
X\$ 9=		OR	X\$18=	
X39=		OR	X78=	
+130=		OR	+260=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

RATE	ADDI- TIONAL FEE		RATE	ADDI- TIONAL FEE
X\$ 9=		OR	X\$18=	
X39=		OR	X78=	
+130=		OR	+260=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

RATE	ADDI- TIONAL FEE		RATE	ADDI- TIONAL FEE
X\$ 9=		OR	X\$18=	
X39=		OR	X78=	
+130=		OR	+260=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

ISSUE SLIP STAPLE AREA (for additional cross references)

7

POSITION	INITIALS	ID NO.	DATE
FEE DETERMINATION	<i>SL</i>	<i>62607</i>	<i>6/4/99</i>
O.I.P.E. CLASSIFIER			<i>6-9-99</i>
FORMALITY REVIEW		<i>70608</i>	<i>6-15-99</i>

INDEX OF CLAIMS

✓ Rejected N Non-elected
= Allowed I Interference
- (Through numeral)... Canceled A Appeal
+ Restricted O Objected

Claim	Date
Final	
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1	<i>11/15/94</i>
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If more than 150 claims or 10 actions
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