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204 U.S. рто 08/926576 APPROVED FOR LICENSE PATENT APPLICATION INITIALS OC 9 7 08926576 Date Entered Date Received CONTENTS or Counted or Malled 1. Application 4 Sheets papers. 100 Sile 2. / m 1I 3. C 4. 25 -9 5. assigner 6. 7. 00 -98 Iniction 7-1-18 RG. 8. lone onthl 18-2/54 etim 8 3-98 9. 5=98 10. jection months 8 99 11. 11-14 0 \mathcal{O}_{1} \mathcal{D} NYU 12. 13. PTOL. 37 Format Ornwings (Lahis) set 1 8-117 14. 15. _ 16. __ _ 17. _ _ 18. _ __ 19. _ __ 20. _____ _ 21. _ _ 22. _ ر 23. 24. ſ 1 25. 26. 27. 28. _ 29. _ . _ 30. _ _ 31. _ _ 32. __ (FRONT)

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WWNSEND and TOWNSEND and CREW LLP Embarcadero Center, 8th Floor Francisco, CA 94111-3834 576-0200

PATENT APPLICATION ASSISTANT COMMISSIONER FOR PATENTS Washington, D. C. 20231

Sir:

Transmitted herewith for filing is the [x] patent application, [] design patent application, [] continuation-in-part patent application of

Inventor(s): Ali Pourkeramati

For: SERIAL FLASH MEMORY

Atty. Docket No. 17822-1-1

"Express Mail" Label No. EM575720486US

Date of Deposit September 4, 1997

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to:

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By

[] This application claims priority from each of the following Application Nos./filing dates:

[4] Please amend this application by adding the following before the first sentence: --This application claims the benefit of U.S. Provisional Application No. 60/025,698, filed September 9, 1996, the disclosure of which is incorporated by reference.--[X]

Enclosed are:

- [x]
 4
 sheet(s) of [] formal [x] informal drawing(s).

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 An assignment of the invention to

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[] A petition to extend time to respond in the parent application of this continuation-in-part application. [x] The filing fee has been calculated as shown below: OTHER THAN A

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Respectfully submitted,	
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Reg. No.: 37,495 Attorneys for Applicant

SMALL ENTITY

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Attorney Docket No. 017822-00011

PATENT APPLICATION

SERIAL FLASH MEMORY

Inventors:

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<u>PATENT</u>

Attorney Docket No. 017822-00011

SERIAL FLASH MEMORY

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BACKGROUND OF THE INVENTION

The present invention relates in general to semiconductor memories, and in particular to an improved flash memory circuit and method of manufacture.

Figure 1 shows a schematic cross-section of an example of a singletransistor double poly stacked gate flash cell. The cell includes a floating gate 100 made of a first polysilicon layer (poly-1), a control gate 102 made of a second polysilicon layer (poly-2), an N+ drain region 106 and an N++ source region 104 inside a P-well region 108. A thin layer of silicon dioxide of approximately 70 to 120 Angstroms forms the tunnel oxide 110 between the floating gate poly-1 and the channel, and a 150 to 300 Angstroms thick film made of an oxide-nitride-oxide (ONO) sandwich 112 separates the two poly gates 100 and 102.

This cell is programmed by grounding the source terminal, applying a 5 to 10 volt signal to the drain terminal or the bit line (V_{BL} =5v), and applying a high programming voltage V_{PP} of, for example, 18 to 20 volts to control gate 102 (V_{CG} = V_{PP}). The high voltage on V_{CG} creates a high electric filed across tunnel oxide 110 generating hot electrons in the channel with enough energy to cross the tunnel oxide. These hot electrons are then trapped in the floating gate poly-1 layer 100 resulting in a higher threshold voltage for the transistor. The cell is thus programmed into an OFF (non-conducting) state.

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Erasing of the cell is performed by grounding the control gate and the drain terminal and applying V_{PP} to the source terminal. The large gate to source voltage causes the trapped electrons on the floating poly 100 to tunnel through the thin oxide layer 110 by a mechanism known as Fowler-Nordhiem. The electrons are collected by the source region 104.

The flash memory cell shown in Figure 1, however, suffers from a number of drawbacks in terms of its overall performance. Because the source region 104 is subject to very high erase voltages (V_{PP}), this cell requires a carefully engineered high-voltage junction process. As shown in Figure 1, the source region 104 is made deeper than the drain region 106 and has a higher doping concentration. The high-voltage junction requirement results in a more complex and therefore more expensive process. Further, the high-voltage junction requirement results in a cell that is not scaleable. That is, the high-voltage diffusion to high-voltage diffusion spacing requirements increases the cell layout pitch. Lower endurance is another drawback of the high-voltage junction, since under high voltage conditions, the source region 104 cannot withstand a large number of erasures.

Furthermore, applying the high V_{pp} voltage to the source region 104 generates hot holes that are released into the P-well 108 and then collected and trapped inside the tunnel oxide 110. This phenomenon, sometimes referred to as band bending, not only deteriorates the endurance of the cell, it also results in unpredictable erase threshold voltage over time. Additional erase threshold voltage verification circuitry are thus necessary for proper operation of the cell.

Finally, because the tunnel oxide region 110 is the same size as the channel, its capacitance is relatively larger, and thus the cell coupling capacitance is lower. Lower cell coupling capacitance requires larger program and erase voltages. Larger program and erase voltages not only lower the endurance of the cell, they also add to the circuitry as they require large pump circuits.

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An improvement to the flash cell shown in Figure 1 splits the erase voltage between the control gate 102 and the source 104. Instead of applying a high voltage to the source region 104, the control gate 102 is negatively biased with respect to the source terminal. Thus, in this embodiment, programming voltages remain the same, but during erase, a negative voltage is applied to the control gate (V_{CG} =- V_{PP}) while the source terminal connects to the positive power supply voltage (typically 3 to 5 volts). This allows the source junction to be the same size as the drain junction, and eliminates the high-voltage junction process requirements. However, this cell requires an additional negative pump circuit and still suffers from the hot hole injection and the resulting erratic erase threshold voltage.

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Various other implementations of a single-transistor flash cell have been proposed each improving on some aspects of the cell performance, but with trade-offs in other aspects. For example, one approach that eliminates performance degradations caused by the hot hole injection, places the P-well 108 inside another N-well. This allows the P-well 108 to be biased to a positive voltage along with the source and drain regions, while the control gate is biased negatively for an erase operation. This type of flash cell, however, requires a triple well technology that is much more complex and costly to manufacture. Further, the cell still requires a negative pump circuit to bias the control gate during erase.

While there have been numerous variations on the double poly stacked gate single-transistor flash cell, there is room for improvement of the structure and design of the cell in terms of endurance, speed, reliability and cost of manufacture.

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SUMMARY OF THE INVENTION

The present invention provides a novel scaleable flash memory cell structure and method of manufacture that improves data retention, increases capacitive coupling and speed of operation, and improves reliability among other advantages. The flash cell of the present invention permits implementation of arrays of flash memory cells that allow the designer to program and/or erase individual bytes of memory as well as blocks of memory. Therefore, the nonvolatile memory circuit of the present invention combines the advantages of conventional EEPROM technology with that flash technology.

Broadly, the flash cell according to the present invention limits the tunnel oxide to a window having dimensions at the minimum feature size located over the drain side of the transistor. The tunnel oxide window is separated from the field oxide and has no edges abutting field oxide. Thus, leakage due to defects caused by the field edge is eliminated, resulting in higher data retention rates for the cell. The reduced dimensions of the tunnel oxide region significantly increase the gate capacitive coupling ratio of the cell. The higher gate coupling allows the cell to be smaller yet operate at higher speed (larger read current). The higher coupling ratio also reduces the level of the maximum required voltage resulting in higher endurance.

Accordingly, in one embodiment, the present invention provides a memory cell including a source region and a drain region forming a channel therebetween; a channel oxide layer disposed on top of the channel; a floating gate layer disposed on top of the channel oxide layer, where the floating gate layer and channel oxide layer define a window wherein a thickness of the channel oxide is substantially smaller than the remaining portion of the channel oxide. The memory cell further includes a control gate layer disposed on top of and separated from the floating gate layer by a dielectric film, wherein the window is located on a drain side of the channel and has dimensions at minimum feature size.

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In another embodiment, the present invention provides a method of manufacturing a memory cell including the steps of

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A better understanding of the nature and advantages of the flash memory of the present invention may be had with reference to the drawings and detailed description below.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows an exemplary prior art double poly stacked gate single transistor flash memory cell;

Figure 2A shows a top view of a specific embodiment of a single flash cell as initially laid out, while Figures 2B and 2C show top views of two different embodiments of the cell after it has been formed;

Figure 3 illustrates the cross section of two flash memory cells perpendicular to word line and a high voltage transistor switch according to the present invention;

Figure 4 is a circuit schematic for an exemplary memory array made of flash cells according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Various aspects of the flash memory according to the present invention will be described in detail hereinafter.

Cell Structural Design

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Referring to Figures 2A and 2B, there are shown top views of a specific embodiment of a single flash cell of the present invention as initially laid out, and a of the cell after it has been formed, respectively. In a preferred embodiment, each flash cell is implemented in a double poly, single metal, twin

well CMOS process. As shown in Figure 2A, active area 20 (e.g., N+) is diffused into a well region (e.g., P-well). A control gate polysilicon layer 25 is laid out perpendicular to active region 20 and defines drain and source regions 21 and 22, respectively. The overlap area between control gate polysilicon 25 and active area 20 forms the transistor channel region 26. A non-self aligned tunnel window 23 is formed on the drain side (21) of each memory cell as depicted. A floating polysilicon layer 24 overlaps active area 20.

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As shown in Figure 2A, tunnel area 23 partially extends over drain region 23 such that it has a first region 23A under gate poly 25 (i.e., over the channel) and a second region 23B over drain 21. The overlap region 23B of tunnel window 23 will be removed during subsequent steps in the process.

Figure 2B shows a top view of the flash cell as formed at the completion of the process. As depicted in Figure 2B, both tunnel window 23 and floating gate poly 24 are etched back to within the area of channel region 26. Note that the area defining tunnel window 23 does not coincide with the area defining channel region 26. This appreciably increases the gate capacitive coupling ratio of the cell allowing faster operation. Furthermore, in the preferred embodiment shown, tunnel oxide window 23 as thus formed is separated from the field oxide, (not shown) and has no edges abutting field oxide, eliminating potential leakage caused by defects at the field edge. Tunnel oxide window 23 may alternatively extend all the way to the field edges of the channel as shown in Figure 2C. The memory cell embodiment shown in Figure 2C still exhibits the higher gate capacitive ratio because tunnel window 23 does not coincide with the entire area defining channel region 26.

Referring to Figure 3, there is shown a cross section of two flash memory cells 200-1 and 200-2 in a direction perpendicular to the word line, and a high voltage transistor switch 216 according to one embodiment of the present invention. In this exemplary implementation, N+ source drain regions are

> TOSHIBA CORP. EXHIBIT 1003 - PAGE 0011

diffused into a p-well region 208, and the drain region for one cell acts as the source for the adjacent cell. That is, N+ region 211 forms the source terminal of cell 200-1, N+ region 209 forms the drain terminal of cell 200-1 as well as the source terminal of cell 200-2, and N+ region 215 forms the drain terminal of cell 200-2. Tunnel window 210 is formed on the drain side of each cell and is preferably of minimum feature size. As mentioned above, in a preferred embodiment, tunnel window 210 is fieldless (i.e., does not abut field oxide) which helps increase endurance. The active area surrounding the tunnel window is covered by relatively thicker cell gate oxide 212 of, for example, about 100-300 Angs. Tunnel window 210 comprises a thin, for example, 70- 100 Angs thermal dielectric. Thus, the cell channel region (26 in Figure 2B) is covered by both tunnel oxide window 210 (23A in Figure 2B) and relatively thicker gate oxide 212. The tunnel window/active area edge has a gradual step of, for example, 30-200 Angstroms thick.

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A first preferably multiple stack polysilicon layer (poly-1 201 and 202 as shown in Figure 3), forming the memory cell floating polysilicon (i.e., charge storage layer), is formed on top of gate oxide (210 and 212). The total thickness of the multiple stack floating polysilicon 201/202 is preferably about, for example, 500 Angstroms, with typical grain size at the tunnel oxide boundary of approximately less than 100 Angstroms. The control gate terminal (connected to the word line) is formed by a second polysilicon (poly-2) layer 206 preferably combined with a polycide layer 207, that form a combined thickness of approximately 1000-2000 Angstroms. Poly-1 layer 201/202 and silicided poly-2 layer 206/207 are separated by, for example, 150-200 Angstroms thick Oxide-Nitride-Oxide (ONO) 203/204/205 dielectric stack. The memory as thus constructed includes a structure having a substrate>well>tunnel oxide>poly-1>ONO>poly2-polycide stack. Exemplary value for the size of the stack may be approximately 0.28-.34 μ m.

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Cell Process Flow

The cell formation according to one embodiment of the present invention begins with a p-type silicon substrate 214. After the typical CMOS steps forming N- and P-well regions, active areas (36 in Figure 2B) are defined by masking and etching steps. This is preferably followed by a field implant to increase the parasitic field threshold voltage. A thick field oxide of, for example, 3000-5000 Angstroms is then grown all over the wafer to isolate different active areas followed by nitride strip and kooi oxide growth. A p-well protect mask is then used to block p-well formation from areas where high voltage circuit blocks will be built. This is to avoid high back-biased threshold voltages of highly doped p-well.

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After resist strip and an oxide clean step, gate oxide 212 is formed by growing a high quality thermal oxide (e.g., 150-190 Angstroms thick) all over the wafer. This is followed by a cell threshold voltage (Vt) adjust mask and an implant (using e.g., Boron) to adjust the cell threshold to appropriate value between the programmed and the erased Vt distribution target. After implant the resist is stripped.

The wafers are then masked to form tunnel windows 210 for the memory cells. This mask is a critical mask as this term is used in the art. The wafers are then subjected to a short (e.g., 10-25 sec.) wet oxide cleaning step to clean the tunnel windows with non roughening characteristics. The resist is removed from the wafers and the surface is cleaned again to remove organic, metallic and hydrocarbons from the surface.

The next step involves forming the tunnel oxide by growing a high quality thermal oxide, of for example 70-85 Angstroms to cover the whole wafer. This is followed by deposition of the first of several layers of polysilicon layers to form the floating polysilicon having layers that are each engineered with varying grain sizes. The top layer of poly (layer 202) is preferably implanted

with N+ dopants to amorphize the poly and dope it to achieve for example 200-500 ohms/square sheet resistivity.

The wafers are then oxidized (at e.g., 900-1050 C) to grow thermal oxide of for example 100 Angstroms. This step forms oxide layer 203 and is followed by deposition of about 75-90 Angstroms of silicon-nitride (layer 204) grown at exemplary temperatures of 650-700 C. The wafers are then subjected to a wet oxidation to cover the nitride surface with 30-50 Angstroms of blocking oxide (1000 C wet oxidation to grow 3500-4000 Angs on bare silicon). This series of steps forms ONO layers 203/204/205.

Next, the wafers are masked again to etch ONO/poly-1/gate-tunnel islands in the memory array. This etch is preferably performed anisotropically and is designed to endpoint on the tunnel oxide. The polysilicon/ONO/gate oxide stack on high voltage transistors 216 are also masked in this step to protect the high voltage (HV) transistor gates 222. After resist strip the wafers are subjected to a light oxidation at 800-900 C in a dry ambient. This oxidation is done to seal off the exposed edges of floating gate 201/202 that is freshly exposed after the etch.

The memory array core is then masked to clean the periphery with a wet/dry etch. The memory array core mask is also used to protect the high voltage circuit areas. After the etch, the resist is stripped and the wafers are masked again to form self-aligned high voltage graded junctions for the HV enhancement transistors. The high voltage implant could be for example a Phosphorus 31 implant 5E13-5E14 #/cm2 or a double-diffused Phosphorus/arsenic combination implant.

After the implant, the resist is stripped and the wafers are subjected to a low voltage threshold adjust mask or blanket, and implant sequence followed by a high quality wet gate oxidation to grow about 70-110 Angstroms of oxide in

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the periphery active areas. The wafers are then covered with approximately 1.5 kA to 2.0 kA polysilicon layer that forms the gate of the periphery transistors and the first poly layer (206) of the word line for memory cell array. To reduce heat generation and resistivity of the word line poly, a 1000-2000 Angstrom layer of WSi_x is deposited over the entire wafer that forms the top layer 207 for the control gate of the memory cell. Next, the wafers are subjected to re-oxidation at about 900-950 C for approximately 30-50 minutes.

The memory cell stack is then defined by a masking step that also protects the periphery. The stacked array mask etch is used to etch the polycide/ONO/poly-1/tunnel sandwich 200. After the etch, wafers are cleaned to remove organics, hydrocarbons and post etch residues. The high voltage transistors are covered with resist during this etch.

The wafers are masked again to define the gate polycide of the periphery low voltage transistors. After the gate poly etch the resist is stripped. The high voltage transistors are exposed during this etch. Both the polycide and the poly are etched away. About 100 Angstroms of ONO is etched away also leaving a 50-100 Angstroms of dielectric on the HV gates.

The n-tip mask is then used to form the lightly doped drain (LDD) tips of the NMOS transistor followed by p-tip mask and implant. The n-tip mask is blocked from memory array and HV transistors. The spacer deposition is followed by spacer etch and N+ and P+ source drain formation. The first interlayer dielectric is then formed by either BPSG, BPTEOS with 4/4 B/P, or the like. The inter layer dielectric (ILD) is then reflowed at about 850-920 C and SOG planarized and the contacts are masked and opened.

This is followed by barrier metal deposition followed by tungsten plug formation and first metal (metal-1) deposition. The metal-1 mask is then used to define the interconnect and memory array bit lines. Finally, metal-1

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layer is covered with thick ILD and passivation oxynitride is deposited and etched using the pad mask.

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Cell Electrical Design

In a preferred embodiment of the present invention cells are programmed (e.g., high cell Vt) and erased (e.g., low cell Vt) by Fowler Nordhiem tunneling to and from the same tunnel window on the drain side. The various modes of operation, including programming, erase and read will be described in connection with the exemplary memory array circuit shown in Figure 4. Referring to Figure 4 there is shown an exemplary circuit schematic for an array 400 made of flash memory cells according to the present invention. Array 400 includes memory cells 402 located at intersection of 16 word lines (WL0-WL15) and 16 bit lines (BL0-BL15). Bit line select transistors 404 respectively couple bit lines BL0-BL15 to memory cells 402. Source select transistors 406 couple ground (or Vss) to memory cells 402. A bit line select control line BSL controls gate terminals of bit select transistors 404, and a source select control line SSL controls gate terminals of source select transistors 406.

Table I below sets forth a preferred biasing scheme for various cell operations for an individual cell according to the present invention.

T-1-1- T

		Table 1		
Control Line	<u>Erase</u>	<u>Program</u>	<u>Read</u>	Condition
BSL	Vcc	Vcc	Vcc	Selected
SSL	Vss	Vss	Vcc	Selected
BLO	Vcc	Vss	1.0-1.4V	Selected
BL1	Vss	Vcc	0.5V	Unselected
WL0	Vcc	Vcc	Vcc	Unselected
WL1	-12 to -15V	15-20V	Vss	Selected

Erase Operation:

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TOSHIBA CORP. EXHIBIT 1003 - PAGE 0016 In the exemplary biasing convention described herein, cells are erased by the action of applying negative gate voltage of, for example, -12 to -15 volts on the selected word lines or a single word line (WL1), and applying a voltage approximately equal to Vcc (e.g., Vcc-2Vtn to Vcc) on the selected bit lines or a single bit line (e.g., BL0). A voltage of about Vcc is applied to bit line select control line BSL, while source select control line SSL is coupled to ground or Vss. This condition generates the necessary electrical field to force electrons to leave the floating gate through the cell tunnel oxide drain interface. This results in a reduced threshold voltage for the cell.

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The bit line voltage level is selected to ensure suppression of band bending and hot hole injection from the cell drain into the tunnel oxide. However, due to the reduced tunnel area of the cell of the present invention and the resulting increase in cell coupling ratio, the voltage applied to the bit line can be as low as Vcc.

The erase coupling is adequate to achieve read/erase threshold voltage Vtrde of, for example, about -2.5 V. A Vtrde of -2.5 volts helps achieve adequate read current with a lower word line voltage. Further, even with a Vtrde of -2.5 V, the cell of the present invention does not suffer from over-erasure. Conventional memory cells, such as single transistor ETOX cells, however, do suffer from over-erasure when negative threshold voltages are used (i.e., cells are driven into deep depletion). Such over-erasure leads to significant performance drawbacks such as program inhibit and/or wide erase threshold variations. The flash cell according to the present invention is less sensitive to both these problems.

The engineering of the erase interface (floating poly/tunnel oxide) in the flash cell of the present invention is controlled by limiting the fluctuation of the local barrier height seen by electrons. This allows a tight threshold convergence without relying on algorithm circuits. Secondly, the nature of the

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memory cell of the present invention limits the threshold variation. The threshold voltage of the thick gate oxide portion of the cell helps to improve the punch-through margin of the cell.

Typical erase current depends on the block size and is of the order of a few mA. The erase speed is primarily a function of the field across tunnel oxide which can be, for example, approximately 8.5 to 10 MV/cm to achieve block erasure in less than for example 1 msec.

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Programming operation:

The programming operation is done by applying a high voltage (e.g., 15 to 20 V) on the selected word line (WL1) and grounding the selected bit line (BL0), while the unselected bit lines (BL1-BL15) are at Vcc. Referring to Figure 4, to program memory cell 402-C, a high voltage of for example 15 to 20 volts is applied to WL1. Vcc is applied to BSL control line and WL0 to couple BL0 to the drain terminal of memory cell 402-C. With BL0 grounded, the drain terminal of cell 402-C receives ground potential. Control line SSL remains at VSS and unselected word lines WL2-WL15 receive VCC. Thus, the cells are programmed serially in a NAND type structure by passing Vss to the selected cells as the pass (unselected) word lines are pulled up to pass Vss.

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The typical programming current for the memory cell of the present invention may be, for example, as low as about 100 pA/cell. The typical programming current required by convention ETOX cells, on the other hand, is around 1 mA. The lower programming current requirement of the present invention allows for the pump circuits to be aggressively down sized, for a more compact overall design.

Another advantageous feature of the present invention is that it provides for the ability to erase and/or program on a byte by byte basis. Because neither erase nor programming operations require shifting the potential supplied to the entire bulk (substrate) for the array of cells, erase or programming of memory array 400 need not be limited to the entire block.

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Read Operation;

The read operation is accomplished by grounding the selected word line WL1=Vss and applying a low voltage of, for example, 1.0-1.5 volts to the selected bit line BL0. Unselected bit lines (BL1-BL15) receive a voltage in the range of Vss to 0.5 volts. Unselected word lines WL0 and WL2-WL15 receive Vcc which allows their memory cells 402 to pass Vss to the selected cell, e.g., 402-C, and couple the drain terminal of selected memory cell 402-C to selected bit line BL0. If memory cell 402-C is programmed (i.e, high Vt), then the voltage on selected bit line BL0 remains unaffected. If memory cell 402-C is not programmed (i.e., low Vt), selected bit line BL0 is pulled down to Vss.

Finally, when changing from one mode (e.g., erase) to another (e.g., program, the memory array first enters the program inhibit mode of operation. The program inhibit mode avoids accidental programming of the cell during the transition from one mode of operation to another. In program inhibit mode, according to the present invention, the entire array enters an unselected condition by applying Vss to BSLs, SSLs and BLs, and Vcc to WLs.

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In conclusion, the present invention offers a single transistor, double-poly flash cell and a method of manufacture for the same that improves data retention, increases capacitive coupling and speed of operation, and improves reliability among other advantages. While the above is a complete description of the preferred embodiment of the present invention, it is possible to use various alternatives, modifications and equivalents. Therefore, the scope of the present invention should be determined not with reference to the above

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description but should, instead, be determined with reference to the appended claims, along with their full scope of equivalents.

EXHIBIT 1003 - PAGE 0020

WHAT IS CLAIMED IS:

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3 4 A memory cell comprising:

a source region and a drain region forming a channel therebetween; a channel dielectric layer disposed on top of said channel; a floating polysilicon layer disposed on top of said channel

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dielectric layer, said floating polysilicon layer and channel dielectric layer defining a window within an area of said channel wherein a thickness of said channel dielectric layer in said window is smaller than that of a remaining portion of said channel dielectric layer; and

a control gate layer disposed on top of and separated from said floating gate layer by a dielectric film,

wherein said window is located on a drain side of said channel.

2. The memory cell of claim 1 wherein a dimension of said window is of minimum process feature size.

3. The memory cell of claim 1 further comprising field dielectric layer substantially surrounding first and second sides of said channel, and wherein, said window has no sides abutting said field dielectric layer.

4. The memory cell of claim 1 further comprising filed dielectric layer substantially surrounding first and second sides of said channel, and wherein said sides of said window abut said field dielectric layer.

5. The memory cell of claim 1 wherein said channel dielectric layer comprises silicon dioxide material, said control gate layer comprises polysilicon material, and said dielectric film comprises a layer of nitride material sandwiched between first and second silicon dioxide layers.

17 The memory cell of claim 5 wherein said control gate layer 6. further comprises a polycide layer on top of said polysilicon layer. An array of flash memory cells, comprising: 7. a plurality of memory cells as defined in claim 1 arranged in a plurality of columns, each column of memory cells comprising: a bit line select transistor having a first current-carrying terminal coupled to a bit line, and a gate terminal coupled to a bit line select control line; a predefined number of memory cells coupled in series with a drain end coupling to a second current-carrying terminal of said bit line select transistor, said predefined number of memory cells being serially coupled such that a drain node of a memory cell acts as a source node of an adjacent memory cell; and a source line select transistor having a first current-carrying terminal coupled to a source end of said predefined number of memory line cells, a gate terminal coupled to a source select Hern and a second current тP carrying terminal coupled to a low potential. An array of flash memory cells comprising: 1 8. a plurality of columns of serially connected flash memory cells, 2 3 each memory cell having a gate terminal; a plurality of bit lines respectively coupled to drain side of said 4 plurality of columns of memory dells via a respective plurality of bit line select 5 transistors, said plurality of bit line select transistors having gate terminals 6 coupled to a bit line select control line; 7 a plurality of word lines, each one coupling to a gate terminal of 8 one memory cell in each of said plurality of columns to from rows of memory 9 cells with common gate terminals; and 10

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11	a plurality of source select transistors respectively coupling a source
12	side of said plurality of columns of memory cells to a logic low voltage, and
13	having gate terminals coupled to a source select control line,
14	wherein, during programming:
15	a logic high voltage is applied to said bit line select control line to
16	turn on bit line select transistors,
17	a logic low voltage is applied to source select control line to turn
18	off source select transistors;
19	a logic low voltage is applied to a selected bit line while a logic
20	high voltage is applied to unselected bit lines, and
21	a logic high voltage is applied to unselected word lines, while a
22	boosted positive voltage is applied to a selected word line.
0	9. An array of flash memory cells comprising:
	a plurality of columns of serially connected flash memory cells,
# 3	each memory cell having a gate terminal;
¹ аний Ц Д лация	a plurality of bit lines respectively coupled to drain side of said
, þ	plurality of columns of memory cells yia a respective plurality of bit line select
Š	transistors, said plurality of bit line select transistors having gate terminals
7	coupled to a bit line select control line;
-8	a plurality of word lines, each one coupling to a gate terminal of
9	one memory cel in each of said plurality of columns to from rows of memory
10	cells with common gate terminals; and
11	a plurality of source select transistors respectively coupling a source
12	side of said plurality of columns of memory cells to a logic low voltage, and
13	having gate terminals coupled to a source select control line,
14	wherein, during erase:
15	a logic high voltage is applied to said bit line select control line to
16	turn on bit line select transistors,
17	a logic low voltage is applied to source select control line to turn
18	off source select transistors;
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a logic high voltage is applied to a selected bit line while a logic 19 low voltage is applied to unselected bit lines, and 20 a logic high voltage is applied to unselected word lines, while a 21 boosted negative voltage is applied to a selected word line. 22 An array of flash memory cells comprising: 10. 1 a plurality of dolumns of serially connected flash memory cells, 2 each memory cell having a/gate terminal; 3 a plurality of bit lines respectively coupled to drain side of said 4 plurality of columns of memory cells via a respective plurality of bit line select 5 transistors, said plurality of bit line select transistors having gate terminals coupled to a bit line select control line; a plurality of word lines, each one coupling to a gate terminal of one memory cell in each of said plurality of columns to from rows of memory cells with common gate terminals; and a plurality of source select transistors respectively coupling a source

side of said plurality of columns of memory cells to a logic low voltage, and having gate terminals coupled to a source select control line,

wherein, during program inhibit a logic low voltage is applied to said bit line select control line, source select control line, and bit lines, while a logic high voltage is applied to word lines.

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SERIAL FLASH MEMORY

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ABSTRACT OF THE DISCLOSURE

A scalable flash memory cell structure and method of manufacture is disclosed that improves data retention, increases capacitive coupling and speed of operation, and improves reliability among other advantages. The flash cell according to the present invention limits the tunnel oxide to a window having dimensions at the minimum feature size located over the drain side of the transistor. The tunnel oxide window is separated from the field oxide and has no edges abutting field oxide.

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Attorney Docket No. 17822-1-1

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that:

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My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: SERIAL FLASH MEMORY the specification of which \underline{x} is attached hereto or ____ was filed on ____ as Application No. ____ and was amended on _____ (if applicable).

I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56. I claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign applications(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign	Application(s)		• 	
2	Country	Application No.	Date of Filing	Priority Claimed Under 35 USC 119
				Yes No _
				Yes No

I hereby claim the benefit under Title 35, United States Code §119(e) of any United States provisional application(s) listed below:

Application No.	Filing Date
60/025,698	September 9, 1996

I ctaim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application No.	Date of Filing	Status
		_ Patented _ Pending _ Abandoned
		Patented Pending Abandoned

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

Rabalz	C	Sant	Deg	No	37 405
Dabak	ο.	sam,	rcg.	140.	37,495

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Residence & Citizenship	City	State/Foreign Country	Country of Citi	zenship
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Full Name of Inventor 3	Last Name	First Name	Middle Name o	or Initial
Residence & Citizenship	City	State/Foreign Country	Country of Citi	zenship
Rost Office Address	Post Office Address	City	State/Country	Zip Code

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signature of Inventor 1	Signature of Inventor 2	Signature of Inventor 3
ALI POURKERAMATI		
Date	Date	Date

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Attn: Box Missing Parts, Washington, D.C. 20231, OD 3-9-95

PATENT

Attorney Docket No. 17822-1-1

Examiner: Unassigned

TRANSMITTAL LETTER - RESPONSE TO NOTICE OF MISSING PARTS

Art Unit: 2511

TOWNSEND and TOWNSEND and CREW LLP Sulph ву_0

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

ALI POURKERMATI

Serial No.: 08/926,576

Filed: 9/4/97

For: SERIAL FLASH MEMORY

Attn: Box Missing Parts Assistant Commissioner for Patents Washington, D.C. 20231

Sir:

61 P

MAR 1 3 1998

TADENAN"

Pursuant to the Notice to File Missing Parts of Application - Filing Date Granted dated January 23, 1998, enclosed are the following to be made of record in the above-identified application:

- 1) Executed Declaration
- 2) 3)
- Power of Attorney Verified Statement Claiming Small Entity Status 4) Copy of Notice of Missing Parts

Please charge Deposit Account No. 20-1430 for the following fees: Missing Parts Surcharge (§1.16(e)) (a) 65.00 TOTAL FEES TO BE CHARGED \$65.00

The Commissioner is hereby authorized to charge any additional fees associated with this paper or during the pendency ALI POURKERMATI Serial No.: 08/926,576 Page 2

- التصليم

of this application, or credit any overpayment to Deposit Account No. 20-1430 for this paper and during the prosecution of this application. This Transmittal Letter is submitted in triplicate. Respectfully submitted,

ala Babak S. Sani Reg. No. 37,495

TOWNSEND and TOWNSEND and CREW LLP Two Embarcadero Center, 8th Floor San Francisco, California 94111-3834 (415) 576-0200 Fax (415) 576-0300 BSS:db

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PATEL

中的計算 出版 化二乙基 建石油 all a start of the start of the ۱P UNITED STATE **PARTMENT OF COMMERCE** hark Office MAR 1 3 1998 86: COMMISSIONER OF PATENTS AND TRADEMARKS Washington, D.C. 20231 APPUICATION NUMBER FILING/RECEIPT DATE FIRST NAMED APPLICANT ATTORNEY DOCKET NO./TITLE 08/926,576 09/04/97 POURKERMATT 1782215 026270123 BABAK SYSANT NOT ASSIGNED TOWNSEND AND TOWNSEND AND CREW TWO EMBARCADERO CENTER STH FLOOR SAN FRANCISCO CA 94111 2511 DATE MAILED: 01/23/98 NOTICE TO FILE MISSING PARTS OF APPLICATION Filing Date Granted An Application Number and Filing Date have been assigned to this application. However, the items indicated below are missing. The required items and fees identified below must be timely submitted ALONG WITH THE PAYMENT OF A SURCHARGE for items 1 and any tees required above to avoid abandoment. Extensions of time may be obtained by filing a petition accompanied by the extension tee under the provisions of 37 CER 1 136(a). 23 The statutory basic filing fee is: 25% 🗇 missing. 173 🗍 insufficient. to complete the basic filling fee and/or file a verified small entity. Applicant must submit \$ statement claiming such status (37 CFR 1.27). Additional claim fees of \$_____, including any multiple dependent claim fees, are required. Applicant must either submit the additional claim fees or cancel additional claims for which fees are due. 2. Additional claim fees of \$ 60 3. The oath or declaration: rγ Is missing. Ċ. does not cover the newly submitted items. does not identify the application to which it applies. Open not include the city and state or foreign country of applicant strestdence. An oath or declaration in compliance with 37 CFR 1 63, including residence information and identifying the application by the above Application Number and Filing Date is required The signature(s) to the oath or declaration is/are: missing. 03/18/1998 GASHUP TO THE INVENTOR OF DECISION OF DECISION QUALIFIED UNDER STORE 1.42, 1.43, or 1.47, 01 F01205 Application Number and Filing Date, is required. □ 5. The signature of the following joint inventor(s) is missing from the oath or declaration: An oath or declaration listing the names of all inventors and signed by the omitted inventor(s), identifying this application by the above Application Number and Filing Date, is required. 6 A \$ processing fee is required since your check was returned without payment (37 CFR 1.21(m)). D 7. Your filing receipt was mailed in error because your check was returned without payment. 8. The application does not comply with the Sequence Rules. See attached "Notice to Comply with Sequence Rules 87 CFR 1.821-1.825." 🧖 🛄 9. OTHER: Direct the response and any questions about this notice to "Attention; Box Missing Parts." A copy of this notice MUST be returned with the response. -M 120 o Center Quistomer Servic Initial Patent Examination Division (703) 308-1202 FORM PTO-1633 (REV.7-96) PART 2-COPY TO BE RETURNED WITH RESPONSE

0.3/04/98 WED 16:10 FAT 415 570 MAR 1 3 1998

TRADENSA?

DECLARATION

TOWNSEND SF

As a below named inventor, I declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: SERIAL FLASH MEMORY the specification of which ______ is attached hereto or __X___ was filed on __9/4/97__ as Application No. __08/926.576__ and was amended on _____ (if applicable).

I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56. I claim foreign priority benefits under Title 35, United States Code', Section 119 of any foreign applications(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Applicatio	n(s)	·····	
Country	Application No.	Date of Filing	Priority Claimed Under 35 USC 119
			Yes No
			Yes No

Eneroby claim the benefit under Title 35, United States Code §119(c) of any United States provisional application(s) listed below:

Application No.	Filing Date
60/025,698	9/9/96

f along the benefit under Title 35. United States Code, Section 120 of any United States application(s) listed below and, insofar as f and subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner $\rho regulated$ by the first paragraph of Title 35, United States Code, section 112, 1 acknowledge the duty to disclose material information as section 1 Title 37. Code of Federal Regulations, section 1.56 which occurred between the filing date of the prior application and the stational or PCT international filing date of this application:

Application No.	Date of Filing	Status
		_ Patented _ Pending _ Abandoned
		Patented Pending Abandoned

Ø 002

Attorney Docket No. 17822-1-1

03/04/93 WE	D 16:11 FAX 415 576	TOWNSEND SF		វីភ្លិ ១០
Full Name of Inventor	Last Namé 1 POURKERAMATI	First Name	Middle Name	or Initial
Residence a Citizenship	city Redwood City	State/Foreign Country CA	Country of Cit	izenship
Post Office Address	Post Office Address 3979 Brookline Way	City Redwood City	State/Country CA	Zip Code
Full Name of Inventor	Last Name 2	First Name	Middle Name o	94062 or Initial
Residence & Citizenship	: City	State/Foreign Country	Country of Citi	zenship
Post Office Address	Post Office Address	City	State/Country	Zip Code
Full Name of Inventor	Last Name	, First Name	Middle Name o	r Initial
Residence & Citizenship	City	State/Foreign Country	Country of Citi	zenship
Post Office Address	Post Office Address	Спу	.State/Country	Zip Code

Surther declare that all statements made herein of my own knowledge are true and that all statements made on information and belief believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so le are punishable by fine or imprisonment, or both, under section 1061 of Title 18 of the United States Code, and that such willful er statements may jeopardize the validity of the application or any patent issuing thereon.

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102 intege of Inventor 1	-	Signature of Inventor 3	·
Hy auto			
Date 3, 4, 98	Date	Date	<u></u>

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2-101-11-0 1. 2008 1061 SEND SF 03/04/98 MED 16:14 FAX 61PE 1 3020-MAR 1 3 1998 Atty, Docket No. 17822-1-1 挄 VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS (37 CFR 1.9(f) & 1.27(c)) - SMALL BUSINESS CONCERN ant or Death pplicant or Patentee: <u>Ati Pourkeramati</u> pplication or Patent No.: <u>08/926,576</u> iled or Issued: <u>9/4/97</u> Hile. SERIAL FLASH MEMORY hereby declare that I am: the owner of the small business concern identified below: ίΧj an official of the small business concern empowered to act on behalf of the concern identified below: ame of Small Business Concern: Address of Small Business Concern: <u>Azalea Microelectronics Corp.</u> Address of Small Business Concern: <u>3080 Olcott Street, Suite</u> 130-D <u>Santa Clara</u> CA 95054 a 1963 declare that organs under concrete of invinse, warm concepts of on a remain with the small basiness concern identified above with regard of orienters, entried by inventor of the Pagilignetic devetored of one sporter a carrière accessante Apphenere No. *Celob<u>an 176</u> e las <u>e 4397</u> Patere No. <u>-</u> Source* [] [..] ; 1 Instituted by the the destined splay data determined by an order of each individual, concern or organization having rights in the true of the invention of a right of the invention of the inventor, who would not qualify as an independent true based by the true of the inventor of the inventor, who would not qualify as an independent true based of TSR (1967) if that person made the true from order to the inventor of the inventor of the inventor of the inventor of the inventor, who would not qualify as an independent to be one to be one to be one to be inventor of the inventor, who would not qualify as an independent to be one of the inventor of t di for a month for organization under 57 CFR 1. confied statements are conjugate from each furners precising concerns in organization having rights to the invention of second entities, GU CTR 2011 _____ and a second ····· m _____ ------·· · ···· ------. , Letter schal 1.J. Small Husiness Constra . Programania integrable provide the model of p_1 , in the parameter problem of p_2 , in the parameter of p_2 , in the true of paying the earlies of the issue too or an increase of the issue too or an increase of p_2 , p_3 , p_3 , p_4 , scrutting in an of entry and To small entity status after the date on which istatus as a small entity Prevate that all statements made herein of my starts accessed use not that all automated stade on information and balled are believed. To d further than these statements were made with the horowardge transmitted for excession as the file to encode with the horowardge transmitted for excession as the file to encode with the horowardge transmitted for excession as the file to encode with the horowardge transmitted for excession as the file to encode with the horowardge transmitted for excession as the file to encode with the horowardge transmitted for excession as the file to encode the horoward excession and be within the excession and be within the excession and the horoward excession and thoroward excession an Owner, <u>Presids</u> Swner, <u>Presids</u> SP'S Boothling 5 av Redwood Criv, 5 a 東山 -----...... aur Date 3, 9. 98

GP.2511 I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on PATENT Ñ١٥ Attorney Docket No. 17822-1-1 4-14-22 APR 1 7 199 TOWNSEND and CREW LLP TOWNSEND RADEMAR 25 IN THE UNITED STATES PATENT AND TRADEMARK OFFICE In re application of: Examiner: To be announced ALI POURKERMATI Art Unit: 2511 Application No.: 08/926,576 INFORMATION DISCLOSURE Filed: 9/4/97 STATEMENT UNDER R §1.97 and RECEIVED 98 <u>37 CFR §1.97</u> For: SERIAL FLASH MEMORY APR 2 2 1998 Assistant Commissioner for Patents Washington, D.C. 20231 GROUP 2500 The references cited on attached form PTO-1449 (copies sir: enclosed) are being called to the attention of the Examiner. It is respectfully requested that the cited information be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "references cited" on any patent to issue therefrom. Applicant believes that no fee is required for submission of this statement, since it is being submitted prior to the first Office Action. However, if a fee is required, the Commissioner is authorized to charge such fee to Deposit Account No. 20-1430. Please charge any additional fees or credit any overpayment to the above-noted deposit account. Respectfully submitted, T 1 S. Sani Babak Reg. No. 37,495 TOWNSEND and TOWNSEND and CREW LLP Two Embarcadero Center, 8th Floor San Francisco, California 94111-3834 (415) 576-0200 Fax (415) 576-0300 BSS:db i:\bss\share\azalea\1\-1.Ids

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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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TOWNSEND SF WED 16:13 FAX 415 576 0300 04/98 PE ١ n MAR 1 3 1998 Attorney Docket No. 1782 TRADENIN^S POWER OF ATTORNEY BY ASSIGNEE AZALEA MICROELECTRONICS CORP is the Assignee of the invention entitled: <u>SERIAL FLASH</u> <u>MEMORY</u>, the specification of which ______is attached hereto or X___was filed on $\underline{-9/4/97}$ as Application Serial No. 08/926 576 Assignce hereby appoints the following attainey(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. ł. RECEIVED David N. Slone, Roy No. 28,572. Babak S. Sani, Reg. No. 37 495 MAY 0 4 1998 Send Correspondence to Direct Telephone GROUP 2100 FOWNSEND and FOWNSEND and CREW LLP Two Embarcadero Center, 8th Floor Babak S. Sam Peg. No. 37,495 (415) 576-0200 San Francisco, CA 94111-3834 AZALEA MICROELECTRONICS CORP. Date: 3, 9, 98 B١ (Signature) Name: Ali Pourkeramati Title President Noshata i kina d 1, 11

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ASSIGNMENT OF PATENT APPLICATION

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WHEREAS, ALI POURKERAMATI of 3979 Brookline Way, Redwood City, CA 94062, hereinafter referred to as "Assignor," is the inventor of the invention described and set forth in the below identified application for United States Letters Patent:

Title of the Invention:

SERIAL FLASH MEMORY

Date(s) of execution of Declaration: 3-4-98

Filing date: <u>9/4/97</u> Application No.: <u>08/926.576</u>; and

WHEREAS, AZALEA MICROELECTRONICS CORP. a California corporation, located at 3080 Olcott Street, Suite 130-D, Santa Clara, CA 95054, hereinafter referred to as "Assignee," is desirous of acquiring an interest in the invention and application and in any Letters Patent and Registrations which may be granted on the same;

For good and valuable consideration, receipt of which is hereby acknowledged by Assignor. Assignor has assigned, and by these presents does assign to Assignee all right, title and interest in and to the invention and application and to all foreign counterparts (including patent, utility model and industrial designs), and in and to any Letters Patent and Registrations which may hereafter be granted on the same in the United States and all countries throughout the world, and to claim the priority from the application as provided by the Paris Convention. The right, title and interest is to be held and enjoyed by Assignee and Assignee's successors and assigns as fully and exclusively as it would have been held and enjoyed by Assignor had this assignment not been made, for the full term of any Letters Patent and Registrations which may be granted thereon, or of any division, renewal, continuation in whole or in part, substitution, conversion, reissue, prolongation or extension thereof.

Assignor further agrees that Assignor will, without charge to Assignee, but at Assignee's expense, (a) cooperate with Assignee in the prosecution of U.S. Patent applications and foreign counterparts on the invention and any improvements, (b) execute, verify, acknowledge and deliver all such further papers, including patent applications and instruments of transfer and (c) perform such other acts as Assignee lawfully may request to obtain or maintain Letters Patent and Registrations for the invention and improvements in any and all countries, and to vest title thereto in Assignee, or Assignee's successors and assigns.

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application to become abandoned. (35 U.S.C. § 13) 37 CFR 1.136(a).	 Extensions of time may 	be obtaine	ed under the pro	visions of
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Election/Restriction

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

 Claims 1-7, drawn to the array of flash memory cell having tunnel window, classified in class 365, subclass 185.26.

II. Claims 8-10, drawn to the array of flash memory cell operating in programming, erase and read modes, classified in class 365, subclass 185.33.
2. The inventions are distinct, each from the other because of the following reasons: Inventions I and II are unrelated. Inventions are unrelated if it can be shown that they are not disclosed as capable of use together, or they have different modes of operation, or they have different functions, or they have different effects. (MPEP § 806.04, MPEP § 808.01). In the instant case, the flash memory cell having tunnel window in the invention of Group I is not disclosed as capable of use together modes of operation, different the array of flash memory cell in the invention of Group II, therefore, they have different modes of operation, different functions, and different effects.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

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4. Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trong Phan whose telephone number is (703) 308-4870.

phanstrong

June 30, 1998

AV I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on **TENT** Attorney Docket No. 17822-1-1 on - 30-9 # 9 OTP TOWNSEND and TOWNSEND and CREW LLP Lection E O OULA ALLEN E JEAN IN THE UNITED STATES PATENT AND TRADEMARK OFFICE In re application of: Examiner: Pourkeramati ALI POURKERMATI Art Unit: 2818 Application No.: 08/926,576 , RESPONSE TO RESTRICTION Filed: 9/4/97 REQUIREMENT For: SERIAL FLASH MEMORY RECEIVED Assistant Commissioner for Patents Washington, D.C. 20231 AUG 0 6 1998 Sir: In response to the restriction personal mailed July 2, 1998, applicant elects for prosecution Group 1 claims 1-7. Respectfully submitted, alas S. Sani Babak Reg. No. 37,495 TOWNSEND and TOWNSEND and CREW LLP Two Embarcadero Center, 8th Floor San Francisco, California 94111-3834 (415) 576-0200 Fax (415) 576-0300 BSS:db i:\bss\share\azalea\1\-1rstrct.rsp

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X Responsive to communication(s) filed on <u>Aug 3, 1998</u>	3			<u> </u>
This action is FINAL.		6		
Since this application is in condition for allowance exc	ept for formal matters	, prosecutio	n as to the me	rits is closed
in accordance with the practice under Ex parte Quayle	9, 1935 C.D. 11; 453	0.G. 213.		
A shortened statutory period for response to this action is is longer, from the mailing date of this communication. F application to become abandoned. (35 U.S.C. § 133). E 37 CFR 1.136(a).	ailure to respond with	in the period	for response	will cause the
Disposition of Claims				
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Priority under 35 U.S.C. § 119				
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Drawings

1. The drawings are objected to because Fig. 2 should be labeled as Fig. 3 in order to be consistent with the disclosure. Correction is required.

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the feature "said window has no sides abutting said field dielectric layer" as recited in claim 3 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

3. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee, 4,924,119, in view of Hong, 5,460,991.

Lee, 4,924,119, discloses in Fig. 1 an EEPROM cell comprising: *

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source region 18 and drain region 19;

floating gate of polysilicon 15;

tunnel window 23 being located on the side of drain region 19 and abutting a thin layer of oxide (see lines 23-27, column 3);

control gate 18 of polysilicon;

dielectric layer between floating gate of polysilicon 15 and control gate of polysilicon 18.

What is not shown in Fig. 1 of Lee, 4,924,119, is the dielectric film comprising a layer of nitride sandwiched between the first and second silicon dioxide layers as recited in claim 5.

Hong, 5,460,991, discloses in Fig. 7 an EEPROM cell having an interpolysilicon dielectric layer 12 of ONO (oxide-nitride-oxide) (see lines 50-52, column 3).

It would have been obvious under 35 U.S.C. 103(a) to one of ordinary skilled in the art at the time of the invention was made to utilize the interpolysilicon dielectric layer 12 of ONO (oxide-nitride-oxide) in Fig. 7 of Hong, 5,460,991, for the dielectric layer in Fig. 1 of Lee, 4,924,119, for the purpose of having a good insulating layer.

What is not shown in Fig. 1 of Lee, 4,924,119, is the control gate comprising a polycide layer on top of the polysilicon layer as recited in claim 6.

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Hong, 5,460,991, discloses in Fig. 8 an EEPROM cell having control gate 13 comprising a polycide layer disposed over polysilicon layer (see lines 6-8, column 4).

It would have been obvious under 35 U.S.C. 103(a) to one of ordinary skilled in the art at the time of the invention to utilize the control gate 13 in Fig. 8 of Hong, 5,460,991, for the control gate 18 in Fig. 1 of Lee, 4,924,119, for the purpose of having a good control gate.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al., 5,734,609, in view of Lee, 4,924,119.

Choi et al., 5,734,609, discloses in Fig. 4 Prior Art a flash EEPROM device comprising:

a plurality of series-connected EEPROM cells C1-Cn and C1'-Cn';

bit line select transistors S1 and S1';

source line transistors S2 and S2'.

What is not shown in Fig. 4 Prior Art of Choi et al., 5,734,609, is the specific structure of the memory cell.

Lee, 4,924,119, discloses in Fig. 1 an EEPROM cell comprising: source region 18 and drain region 19; floating gate of polysilicon 15;

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tunnel window 23 being located on the side of drain region 19 and abutting a thin layer of oxide (see lines 23-27, column 3);

control gate 18 of polysilicon;

dielectric layer between floating gate of polysilicon 15 and control gate of polysilicon 18.

It would have been obvious under 35 U.S.C. 103(a) to one of ordinary skilled in the art at the time of the invention to utilize the EEPROM cell in Fig. 1 of Lee, 4,924,119, for each of the EEPROM cells in Fig. 4 Prior Art of Choi et al., 5,734,609, for the purpose of providing EEPROM cells having the Vt of the transistor that can be shifted to a value of approximately 10 volts (see lines 27-34, column 3 of Lee, 4,924,119).

7. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsia et al., 4,894,802, in view of Hong, 5,460,991.

Hsia et al., 4,894,802, discloses in Fig. 3b an EEPROM cell comprising: source region 22 and drain region 21;

floating polysilicon layer 17;

field oxide 19 (see line 40, column 4);

tunnel window 27 being located on the side of drain region 21 and abutting field oxide 19;

control gate 18 of polycrystalline silicon (see lines 55-58, column 6);

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dielectric layer 29 of interpoly oxide (see lines 9-10, column 5).

What is not shown in Fig. 3b of Hsia et al., 4,894,802, is the dielectric film comprising a layer of nitride sandwiched between the first and second silicon dioxide layers as recited in claim 5.

Hong, 5,460,991, discloses in Fig. 7 an EEPROM cell having an interpolysilicon dielectric layer 12 of ONO (oxide-nitride-oxide) (see lines 50-52, column 3).

It would have been obvious under 35 U.S.C. 103(a) to one of ordinary skilled in the art at the time of the invention was made to utilize the interpolysilicon dielectric layer 12 of ONO (oxide-nitride-oxide) in Fig. 7 of Hong, 5,460,991, for the dielectric layer 29 of interpoly oxide in Fig. 3b of Hsia, 4,894,802, for the purpose of having a good insulating layer,

What is not shown in Fig. 3b of Hsia, 4,894,802, is the control gate comprising a polycide layer on top of the polysilicon layer as recited in claim 6.

Hong, 5,460,991, discloses in Fig. 8 an EEPROM cell having control gate 13 comprising a polycide layer disposed over polysilicon layer (see lines 6-8, column 4).

It would have been obvious under 35 U.S.C. 103(a) to one of ordinary skilled in the art at the time of the invention to utilize the control gate 13 in Fig. 8

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of Hong, 5,460,991, for the control gate 18 in Fig. 3b of Hsia et al., 4,894,802, for the purpose of having a good control gate.

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al., 5,734,609, in view of Hsia et al., 4,894,802.

Choi et al., 5,734,609, discloses in Fig. 4 Prior Art a flash EEPROM device comprising:

a plurality of series-connected EEPROM cells C1-Cn and C1'-Cn';

bit line select transistors S1 and S1';

source line transistors S2 and S2'.

What is not shown in Fig. 4 Prior Art of Choi et al., 5,734,609, is the specific structure of the memory cell.

Hsia et al., 4,894,802, discloses in Fig. 3b an EEPROM cell comprising:

source region 22 and drain region 21;

floating polysilicon layer 17;

field oxide 19 (see line 40, column 4);

tunnel window 27 being located on the side of drain region 21 and abutting field oxide 19;

control gate 18 of polycrystalline silicon (see lines 55-58, column 6); dielectric layer 29 of interpoly oxide (see lines 9-10, column 5).

Page 8

Art Unit: 2818

It would have been obvious under 35 U.S.C. 103(a) to one of ordinary skilled in the art at the time of the invention to utilize the EEPROM cell in Fig. 3b of Hsia et al., 4,894,802, for each of the EEPROM cells in Fig. 4 Prior Art of Choi 'et al., 5,734,609, for the purpose of providing EEPROM cells having improved programming efficiency and improved program/erase endurance (see lines 9-11, column 3 of Hsia et al., 4,894,802).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See Gill et al., 5,008,721, Kaya et al., 5,216,270, and Chang, 5,666,307, generally, for the Flash EEPROM cell.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trong Phan whose telephone number is (703) 308-4870.

phan trong

August 19, 1998

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			U.	S. PATENT DOCUMENTS					
		DOCUMENT NO.	DATE	NAM	E		CLASS	SUBCLAS	
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	в	4,924,119	May 1990	Lee	3		257	321	
	c	5,008,721	Apr. 1991	Gill et	al.		305	185.33	
	D	5,216,270	Jun. 1993	Кауа е	vtal.		257	321	
	E	5,460,991	Oct. 1995	Hor	g		438	261	
	F	5,666,307	Sep. 1997	Cha	יק		365	185.33	
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	IN THE UNITED STATES PAT	TENT AND TRADEMARK OFFICE $777/817$
-	In re application of:	Examiner: T. Chan 375194
•	ALI POURKERMATI	Art Unit: 2818
	Application No.: 08/926,576	PETITION TO EXTEND TIME
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÷	For: SERIAL FLASH MEMORY	
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	Washington, D.C. 20231	
	Sir:	
	:	t Commissioner of Patents to extend the time for
	response to the Office Action dated August 25,	1998 for three months, from November 25, 1998
	to February 25, 1999. An appropriate response	in the form of an amendment is enclosed
	herewith.	
	Please charge the fee of \$475 to	the undersigned's Deposit Account No. 20-1430.
	Please charge any additional fees or credit over	payment to the above deposit account. This
	petition is submitted in triplicate.	
		Respectfully submitted,
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

ALI POURKERMATI Application No.: 08/926,576

Filed: September 4, 1997

For: SERIAL FLASH MEMORY

Examiner: T. Phan

Art Unit: 2818

AMENDMENT

Assistant Commissioner for Patents Washington, D.C. 20231

Sir:

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In response to the Office Action mailed August 25, 1998, please amend the above-identified application as follows:

3/1999 SSURLES 00000001 **INTHE DRAWINGS**:

To bring the labeling of the figures in conformity with the specification, the legend "FIG. 2" has been changed to -- FIG. 3 --. Further, Figures 2B and 2C have been amended to replace the reference numeral "23" with -- 23B --, and add new reference numerals -- 28A -- and -- 28B -- to clearly identify field oxide edges of the memory cell. Figure 4 has been amended to replace the continuous line that connects the memory cells between WL1 and WL15 with a dotted line to more accurately depict the invention. Submitted herewith are substitute drawings for Figures 3, 2B, 2C, and 4 which show the proposed corrections in red

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ink. Applicant respectfully requests deferral of submission of formal drawings until allowable subject matter is indicated.

IN THE SPECIFICATION:

Please amend the specification as follows:

At page 6, line 21, replace "the field oxide (not shown)" with -- field oxide edges 28A and 28B, --.

At page 6 line 23, replace "the field edges" with -- field edges 28A and 28B---.

At page 8, line 3, replace "36" with -- 26 --.

IN THE CLAIMS:

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Please amend claim 1, and add new claims 8-10 as follows:

1	1. (Once Amended) A memory cell comprising:
2	a source region and a drain region forming a channel therebetween;
3	a channel dielectric layer disposed on top of said channel;
4	a floating polysilicon layer disposed on top of, and substantially covering an
5	area defined by, said channel dielectric layer, said floating polysilicon layer and channel
6	dielectric layer defining a <u>tunnel</u> window within an area of said channel wherein a thickness of
7	said channel dielectric layer in said <u>tunnel</u> window is smaller than that of a remaining portion
8	of said channel dielectric layer; and
9	a control gate layer disposed on top of and separated from said floating gate
10	layer by a dielectric film,
11	wherein an etch step that defines edges of said floating
12	polysilicon layer is performed such that one edge of said tunnel window is [located on a drain
13	side of said channel] defined by an edge of said floating polysilicon layer located substantially
14	at a channel-drain junction.

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1-18. (New) The memory cell of claim 1 wherein a window mask used during manufacturing of the memory cell is larger than said tunnel window, and includes a portion that overlaps said drain region.

By F 9. (New) The memory cell of claim & wherein said etch step removes said portion of said window that overlaps said drain region.

رور (New) A flash memory cell comprising: عن المحرور (New) A flash memory cell comprising: a source region and a drain region forming a channel therebetween;

a channel oxide layer formed on top of said channel, said channel oxide layer having a first portion with a first thickness and a tunnel window portion on a side of said drain region, having a second thickness less than said first thickness;

a floating polysilicon layer formed on top of said channel oxide layer;

a dielectric oxide-nitride-oxide sandwich layer formed on top of said floating polysilicon layer; and

a gate polysilicon layer formed on top of said dielectric oxide-nitride-oxide sandwich layer,

wherein, said tunnel window portion of said channel oxide layer is initially formed inside a window overlapping said drain region, and then etched back to an edge of said floating polysilicon layer.

REMARKS

Upon entry of this amendment which amends claim 1 and adds new claims 8-10, claims 1-10 remain pending. Previously examined claims 1-6 were rejected under 35 U.S.C. §103(a) as being unpatentable over Lee '119 in view of Hong '991, as well as over Hsia '802 in view of Hong '991, and claim 7 was rejected under 35 U.S.C. §103(a) as being unpatentable over Choi '609 in view of Lee '119, as well as over Choi '609 in view of Hsia

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"802. Reconsideration of the claims in view of the above amendments and the comments below is respectfully requested.

Objections

The drawings were objected to for mislabeling FIG. 3 as FIG. 2, and for failing to show a claimed aspect of the present invention. Figure 3 has been amended replacing the legend "FIG. 2" with FIG. 3 to bring it in conformity with the specification. Further, reference numerals 28A and 28B have been added to Figures 2A and 2B as well as to the relevant parts of the specification to clearly identify the edges of the filed oxide around the memory cell. It is respectfully submitted that no new matter has been added by this amendment as should be clear from the nature of the changes to the specification. Withdrawal of the objections in lights o these amendments is respectfully requested.

Rejections

- Section 103(a): Lee '119 in view of Hong '991

Claims 1-6 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Lee '119 in view of Hong '991. The rejection states that Lee '119 in Figure 1 discloses a memory cell with all of the limitations set forth in claim 1, and that Hong '991 suggest the limitations recited in the remaining dependent claims.

It is respectfully submitted that the memory cell shown in Figure 1 of Lee '119 differs from the claimed memory cell of the present invention in at least one significant respect. As clearly shown in Figure 1 of Lee '119, the tunnel window (23) is formed "close to the drain 19" (col. 3, line 25), but is neither at the channel-drain junction, nor does it abut the edge of floating poly 15. That is, tunnel window 23 is formed wholly within the channel region such that the sidewalls of the tunnel must be defined by the tunnel window itself.

In contrast to the Lee '119 memory cell, the memory cell of the present invention as claimed has a tunnel window that has an edge defined by the edge of the floating polysilicon layer located at the drain-channel junction. Claim 1 has been amended to highlight

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this distinguishing feature of the present invention. As amended, claim 1 recites a memory cell "wherein an etch step that defines edges of [the] floating polysilicon layer is performed such that one edge of [the] tunnel window is defined by an edge of [the] floating polysilicon layer located substantially at a channel-drain junction." This aspect of the invention is described in the specification, for example, at page 6, lines 9-16, and at page 9, lines 12-14. Lee '119 as well as the other cited references, or any combination thereof, fail to teach such a combination with the claimed structure for a tunnel window. This distinguishing feature is significant and non-obvious for a number of reasons. The performance of the memory cell (capacitive coupling ratio) is highly dependent on the size of the tunnel window, which is often required to be at minimum process feature size. The tunnel window mask is therefore often a critical mask. The memory cell of Lee '119 requires the tunnel window to be defined entirely by the window mask and thus demands a high resolution process to accurately implement the tunnel window. This places severe demands on the manufacturing process when it is scaled down to lower dimensions.

The boundaries of the tunnel window according to the memory cell of the present invention, in contrast, are not wholly defined by the window mask. Referring to Figure 2A of the instant application, there is shown the initial window (23) that overlaps the channel region (26) as well as the drain region (21). After the tunnel oxide and the overlying floating polysilicon layer are formed, the floating poly layer is patterned and etched along with the overlapping portion (23B) of the tunnel oxide (e.g., see specification, page 9, lines 12-14). Since the area of the actual tunnel window of the memory cell of the present invention does not correspond to the tunnel window mask, the present invention provides a significant degree of flexibility in manufacturability of the cell.

Lee '119 therefore clearly fails to teach or suggest a tunnel window whose one edge is defined by the etch step that etches the floating polysilicon layer. Claim 1 as amended is therefore clearly distinguished over the cited references. Claims 2-9 depend from claim 1 and thus derive patentability therefrom. These claims, however, recite additional novel and non-obvious features that further distinguish over the cited prior art. Claims 3 and 4, for

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example, define alternative embodiments wherein the window either abuts field oxide or it does not. The rejection does not point to any part of the cited reference as suggesting these variations because Lee '119 does not teach or suggest such a structure one way or the other. Furthermore, newly added claims 8 and 9 expressly recite a tunnel window mask that is larger than the actual tunnel window and that the floating poly etch step defines one edge of the tunnel window. No such structure is taught or suggested by any combination of the cited references. Claims 1-6 are therefore clearly distinguished over the combination of Lee '119 and Hng '991. Withdrawal of this rejection is respectfully requested.

- Section 103(a): Choi '609 over Lee '119

Claim 7 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Choi '609 in view of Lee '119. Claim 7 depends from claim 1 and therefore derives patentability therefrom. As explained above, amended claim 1 is patentably distinguished over the teachings of Lee '119. Claim 7 depending from claim 1, therefore is patentably distinguished for at least the same reasons as above. Withdrawal of this rejection is respectfully requested.

- Section 103(a): Hsai '802 over Hong '991

Claims 1-6 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Hsia '802 in view of Hong '991. The rejection states that Hsai '802 in Figure 3b discloses a memory cell with all of the limitations set forth in claim 1, and that Hong '991 suggest the limitations recited in the remaining dependent claims.

It is respectfully submitted that Hsia '802 discloses in Figures 3a and 3b what is known by those skilled in this art as a "split-gate" memory cell. This renders the Hsia '802 memory cell quite different from the claimed memory cell of the present invention in a number of respects. First, according to the split gate Hsia '802 memory cell there are portions of the channel oxide that are covered by the gate poly (18 in Figure 3a) and other portions that are covered by the floating poly (17 in Figure 3a). This is the definition of a split gate cell and is clearly demonstrated in Figures 3, and 3a.
ALI POURKERMATI Application No.: 08/926,576 Page 7 PATENT

In contrast to the Hsia '802 memory cell, the memory cell of the present invention is not of split gate type. Claim 1 has been amended to highlight this aspect of the present invention. Amended claim 1 recites "a floating polysilicon layer disposed on top of, and substantially covering an area defined by, said channel dielectric layer," This clearly distinguished claim 1 from Hsia. which teaches a memory cell with a control gate (18) that "extends above source region 22 ... in order to achieve split gate operation." [Col. 4, lines 45-53]. Furthermore, similar to the tunnel window in the Lee '119 memory cell, the tunnel window in Hsia '802 is wholly defined by the tunnel window mask (26 in Fig. 3), and is not etched back to the channel-drain junction. 'Amended claim 1 is thus further distinguished as it recites an edge of the tunnel window being "located substantially at a channel-drain junction."

Claim 1 as amended is thus patentably distinguished over Hsia '802 based at least on these two differentiating features. Claims 2-10 depend from claim 1 and thus derive patentability therefrom. These claims, however, recite additional non-obvious and novel features that further distinguish over the cited art. Claims 3 and 4, for example, define alternative embodiments wherein the window either abuts field oxide or it does not. Field oxide is defined as "substantially surrounding first and second sides of [the] channel." The only thick oxide (19 in Fig. 3b) shown by Hsia '802 extends <u>under</u> the channel abutting the tunnel window. The memory cell of the present invention, in contrast, does not include any filed oxide under the channel (i.e., between the source-drain regions), and instead surrounds the channel as claimed. Furthermore, newly added claims 8 and 9 expressly recite a tunnel window mask that is larger than the actual tunnel window and that the floating poly etch step defines one edge of the tunnel window. No such structure is taught or suggested by any combination of the cited references. Claims 1-6 are therefore clearly distinguished over the combination of Hsia '802 and Hng '991. Withdrawal of this rejection is respectfully requested.

- Section 103(a): Choi '609 over Hsia '802

Claim 7 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Choi '609 in view of Hsia '802. Claim 7 depends from claim 1 and therefore derives ALI POURKERMATI Application No.: 08/926,576 Page 8 <u>PATENT</u>

patentability therefrom. As explained above, amended claim 1 is patentably distinguished over the teachings of Hsia '802. Claim 7 depending from claim 1, therefore is patentably distinguished for at least the same reasons as above. Withdrawal of this rejection is respectfully requested.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted, alal Babak S. Sani Reg. No. 37,495

TOWNSEND and TOWNSEND and CREW LLP Two Embarcadero Center, 8th Floor San Francisco, California 94111-3834 Tel: (415) 576-0200 Fax: (415) 576-0300 BSS:deb SF 198871 v1







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Including changes required by the proposed drawing correction filed on2/25/99, which has been approved by the examiner. Including changes required by the attached Examiner's Amendment/Comment. Identifying indicie such as the application number (see 37 CFR 1.84(c)) should be written on the reverse side of the drawings. The drawings should be filed as a separate paper with a transmittel letter addressed to the Official Draftsperson. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL. Any response to this letter should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included. Attachment(s) Information Disclosure Statement(s), PTO-1449, Paper No(s) Notice of References Cited, PTO-892 Information Disclosure Statement(s), PTO-1449, Paper No(s) Notice of Informal Patent Application, PTO-152 MAXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX		ftsperson's Patent Drawin	ig Review, I	PTO-948, attac	hed hereto or	
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TOSHIBA CORP. EXHIBIT 1003 - PAGE 0079 Application/Control Number: 08/926,576

Page 2

Art Unit: 2818

2.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

In the specification, line 1 of page 1, the sentence -- This application claims

the benefit of U.S. Provisional Application No. 60/025,698, filed September 9, 1996, the disclosure of which is incorporated by reference has been inserted.

Claim 7, line 14, the word "lien" has been changed to ---line---. Non-elected claims 8-10 have been canceled.

Newly added claims 8-10 have been changed to claims 11-13.

All above changes have been made by the examiner in order to place the

case in condition for allowance.

3. The following is an examiner's statement of reasons for allowance:

The memory cell having one edge of the tunnel window being defined by an edge of the floating polysilicon layer located substantially at a channel-drain junction as recited in claims 1-7 and 11-13 has not been found in the prior art references.

Application/Control Number: 08/926,576

Page 3

Art Unit: 2818

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications 4. from the examiner should be directed to Trong Phan whose telephone number is (703) 308-4870.

phan Grony

Trong Phan Patent Examiner Art Unit 2818

March 14, 1999

		Notice of Refer	ences Cited	Application No 08/926,5				
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NOTICE OF ALLOWANCE AND ISSUE FEE DUE

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IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

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Attorney Docket No.: 17822-000110

LETTER TO OFFICIAL DRAFTSPERSON

Box Issue Fee

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Assistant Commissioner for Patents, may. 18, 1999. Washington, D.C. 20231, on _ TOWNSEND and TOWNSEND and CREW LLP

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

ALI POURKERAMATI

Serial No.: 08/926,576

Filed: September 4, 1997

For: SERIAL FLASH MEMORY

Box Issue Fee Assistant Commissioner for Patents Washington, D.C. 20231

Sir:

Pursuant to the Notice of Allowability dated March 15, 1999, applicant submits four sheets of formal drawings to be made of record in the above-identified case.

Respectfully submitted, A. Babak S. Sani

Examiner: Trong Phan

Art Unit: 2818

Batch No.: Q30

Babak S. Sani Reg. No. 37,495

TOWNSEND and TOWNSEND and CREW LLP Two Embarcadero Center, 8th Floor San Francisco, California 94111-3834 (415) 576-0200 Fax (415) 576-0300 BSS/sb SF 220191 v1







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08/926 5-76 Atty Docket No. 022193-120110US

PTO FAX NO.: 703-872-9306

Examiner T. PHAN

ATTENTION:

Group Art Unit 2818

OFFICIAL COMMUNICATION

FOR THE PERSONAL ATTENTION OF

EXAMINER T. PHAN

CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that the following documents in re Application of Ali POURKERAMATI, Application No. 08/926,576, filed on September 4, 1997 for SERIAL FLASH MEMORYare being facsimile transmitted to the Patent and Trademark Office on the date shown below.

Documents Attached

1. Power of Attorney (1 page)

2. Statement Under 37 CFR 3.73(b) (1 page)

Number of pages being transmitted, including this page: 3

Dated: February 2, 2005

Katherine Farkas

PLEASE CONFIRM RECEIPT OF THIS PAPER BY RETURN FACSIMILE AT (415) 576-0300

TOWNSEND and TOWNSEND and CREW LLP Two Embarcadero Center, Eighth Floor San Francisco, CA 94111-3834 Telephone: 415-576-0200 Fax: 415-576-0300

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PAGE 1/3 * RCVD AT 2/2/2005 2:51:31 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * C8ID:415 578 0300 * DURATION (mm-ss):03-10

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Date Mailed: 09/07/2006

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

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This is in response to the Power of Attorney filed 02/02/2005.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

MARGARET W STEVENS OIPE (703) 308-9010 EXT 184

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201.04(b) Provisional Application [R - 3]

35 U.S.C. III APPLICATION.

(B) PROVISIONAL APPLICATION,-

(1) AUTHORIZATION.-A PROVISIONAL APPLICATION FOR PATENT SHALL BE MADE OR AUTHORIZED TO BE MADE BY THE INVENTOR, EXCEPT AS OTHERWISE PROVIDED IN THIS TITLE, IN WRITING TO THE COMMISSIONER. SUCH APPLICATION SHALL INCLUDE-

* * *

(A) A SPECIFICATION AS PRESCRIBED BY THE FIRST PARAGRAPH OF SECTION 1 2 OF THIS TITLE; AND

(B) A DRAWING AS PRESCRIBED BY SECTION 113 OF THIS TITLE.

(2) CLAIM.-A CLAIM, AS REQUIRED BY THE SECOND THROUGH FIFTH PARAGRAPHS OF SECTION 112, SHALL NOT BE REQUIRED IN A PROVISIONAL APPLICATION.

(3) FEE.-(A) THE APPLICATION MUST BE ACCOMPANIED BY THE FEE REQUIRED BY LAW.

(B) The FEE may be submitted after the specification and any required drawing are submitted, within such period and under such conditions, including the payment of a surcharge, as may be prescribed by the Commissioner.

(C) Upon failure to submit the fee within such prescribed period, the application shall be regarded as abandoned, unless it is shown to the satisfaction of the Commissioner that the delay in submitting the fee was unavoidable or unintentional.

(4) FILING DATE. -THE FILING DATE OF A PROVISIONAL APPLICATION SHALL BE THE DATE ON WHICH THE SPECIFICATION AND ANY REQUIRED DRAWING ARE RECEIVED IN THE PATENT AND TRADEMARK OFFICE.

(5) ABANDONMENT, THE PROVISIONAL APPLICATION SHALL BE REGARDED AS ABANDONED 12 MONTHS AFTER THE FILING DATE OF SUCH APPLICATION AND SHALL NOT BE SUBJECT TO REVIVAL THEREAFTER.

(6) OTHER BASIS FOR PROVISIONAL APPLICATION.-SUBJECT TO ALL THE CONDITIONS IN THIS SUBSECTION AND SECTION I I 9(E) OF THIS TITLE, AND AS PRESCRIBED BY THE COMMISSIONER, AN APPLICATION FOR PATENT FILED UNDER SUBSECTION (A) MAY BE TREATED AS A PROVISIONAL APPLICATION FOR PATENT.

(7) NO RIGHT OF PRIORITY OR BENEFIT OF EARLIEST FILING DATE. A PROVISIONAL APPLICATION SHALL NOT BE ENTITLED TO THE RIGHT OF PRIORITY OF ANY OTHER APPLICATION UNDER SECTION 1/9 OR 365(A) OF THIS TITLE OR TO THE BENEFIT OF AN EARLIER FILING DATE IN THE UNITED STATES UNDER SECTION 1/20, 1/21, OR 365(C) OF THIS TITLE.

(8) APPLICABLE PROVISIONS. THE PROVISIONS OF THIS TITLE RELATING TO APPLICATIONS FOR PATENT SHALL APPLY TO PROVISIONAL APPLICATIONS FOR PATENT, EXCEPT AS OTHERWISE PROVIDED, AND EXCEPT THAT PROVISIONAL APPLICATIONS FOR PATENT SHALL NOT BE SUBJECT TO SECTIONS [15, 13], 135, AND 157 OF THIS TITLE.

37 CFR 1.9 Definitions.

(a)(1) A national application as used in this chapter means a U.S. application for patent which was either filed in the Office under 35 U.S.C. 111, or which entered the national stage from an international application after compliance with 35 U.S.C. 371.

(2) A provisional application as used in this chapter means a U.S. national application for patent filed in the Office under 35 U.S.C. 111(b).

(3) A nonprovisional application as used in this chapter means a U.S. national application for patent which was either filed in the Office under 35 U.S.C. 111(a), or which entered the national stage from an international application after compliance with 35 U.S.C. 371.

37 CFR 1.53 Serial number, filing date, and completion of application.

(b)(2) The filing date of a provisional application is the date on which: a specification as prescribed by 35 U.S.C. 112, first paragraph; and any drawing required by § 1.81(a), are filed in the Patent and Trademark Office in the name of the actual inventor or inventors as required by § 1.41. No amendment, other than to make the provisional application comply with all applicable regulations, may be made to the provisional application after the filing date of the provisional application. If all the names of the actual inventor or inventors are not supplied when the specification and any required drawing are filed, the provisional application will not be given a filing date earlier than the date upon which the names are supplied unless a petition with the fee set forth in § 1.17(q) is filed which sets forth the reasons the delay in supplying the names should be excused.

One of the provisions of the Uruguay Round Agreements Act which is effective as of June 8, 1995, is the establishment of a domestic priority system. The Act provides a mechanism to enable domestic applicants to quickly and inexpensively file provisional applications. Under the provisions of 35 U.S.C. 119(e), applicants are entitled to claim the benefit of priority in a given application in the United States. The domestic priority period will not count in the measurement of the 20 - year patent term. See 35 U.S.C. 154(a)(3). Thus, domestic applicants are placed on equal footing with foreign applicants with respect to the patent term.

The parts of a provisional application that are required are set forth in 37 CFR 1.51(a)(2) and MPEP § 601.01 and § 601.01(b). The filing date of a provisional application is the date on which (1) a specification which complies with 35 U.S.C. 112, first paragraph, and (2) any drawing required by 37 CFR 1.81(a) are filed in the name of the actual inventor or inventors as required by 37 CFR 1.41. A provisional application must also include a cover sheet identifying the application as a provisional application. Otherwise, the application will be treated as an application filed under 37 CFR 1.53(b)(1). The filing fee is set forth in 37 CFR 1.16(k).

Note:

(1) No claim is required in a provisional application.

(2) No oath or declaration is required in a provisional application.

(3) Provisional applications will not be examined for patentability,

placed in an interference, or made the subject of a statutory invention registration.

A provisional application will automatically be abandoned 12 months after its filing date and will not be subject to revival to restore it to pending status thereafter. Since a provisional application can be pending for no more than 12 months, if the last day of pendency is on a Saturday, Sunday, or Federal holiday, copendency would require that the later filed nonprovisional application be filed prior to the Saturday, Sunday, or Federal holiday. See 37 CFR 1.78(a)(3). > For example, if a provisional application was filed on June 28, 1996, the last day of pendency of the provisional application under 35 U.S.C. 111(b)(5) is June 28, 1997. Since June 28, 1997 is a Saturday, a nonprovisional application claiming the benefit of the provisional application must be filed on the Friday, June 27, 1997, prior to the Saturday (See 37 CFR 1.78(a)(3)). However, note that new patent applications filed in accordance with 37 CFR 1.10 will be stamped by the Office with the date of deposit as "Express Mail" with the United States Postal Service. For example, if a new patent application is deposited in "Express Mail" in accordance with 37 CFR 1.10 on a Saturday and the United States Postal Service gives it a date of deposit of Saturday, the Office will accord and stamp the correspondence with the Saturday date. 37 CFR 1.6(a)(2).< A provisional application is not entitled to claim priority benefits based on any other application under 35 U.S.C. 119, 120, 121, or 365.

An application filed under 37 CFR 1.53(b)(1) may be converted to a provisional application provided a petition requesting the conversion is submitted along with the fee as set forth in 37 CFR 1.17(q). The petition and fee must be submitted prior to the earlier of the abandonment of the nonprovisional application, the payment of the issue fee, the expiration of 12 months after the filing date of the nonprovisional application, or the filing of a request for statutory invention registration. The grant of any such petition will not entitle applicant to a refund of the fees which were properly paid in the application filed under 37 CFR 1.53(b)(1).

Design applications may not make a claim for priority of a provisional application under 37 CFR 1.78(a)(3).

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