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SERIAL FLASH MEMORY

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PATENT APPLICATION



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PATENT APPLICATION
ASSISTANT COMMISSIONER FOR PATENTS
Washington, D. C. 20231

Sir:
Transmitted herewith for filing is the ☒ patent application,
☐ design patent application, ☐ continuation-in-part patent
application of

Inventor(s): Ali Pourkeramati

For: SERIAL FLASH MEMORY

☐ This application claims priority from each of the following Application Nos./filing dates:

☒ Please amend this application by adding the following before the first sentence: --This application claims the benefit of U.S.
Provisional Application No. 60/025,698, filed September 9, 1996, the disclosure of which is incorporated by reference.--

Enclosed are:

☒ 4 sheet(s) of ☐ formal ☒ informal drawing(s).

☐ An assignment of the invention to

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☐ A ☐ signed ☐ unsigned Declaration.

☐ A Power of Attorney by Assignee with Certificate Under 37 C.F.R. Section 3.73(b).

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RATE	FEE
	\$385
x11=	\$ --
x40=	\$ 40
+130=	\$
TOTAL	\$425

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OR

OR

OR

OR

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RATE	FEE
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x22=	\$
x80=	\$
+260=	\$
TOTAL	\$

Respectfully submitted,
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Reg. No.: 37,495
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PATENT APPLICATION

SERIAL FLASH MEMORY

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SERIAL FLASH MEMORY

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BACKGROUND OF THE INVENTION

The present invention relates in general to semiconductor memories, and in particular to an improved flash memory circuit and method of manufacture.

10

Figure 1 shows a schematic cross-section of an example of a single-transistor double poly stacked gate flash cell. The cell includes a floating gate 100 made of a first polysilicon layer (poly-1), a control gate 102 made of a second polysilicon layer (poly-2), an N⁺ drain region 106 and an N⁺⁺ source region 104 inside a P-well region 108. A thin layer of silicon dioxide of approximately 70 to 120 Angstroms forms the tunnel oxide 110 between the floating gate poly-1 and the channel, and a 150 to 300 Angstroms thick film made of an oxide-nitride-oxide (ONO) sandwich 112 separates the two poly gates 100 and 102.

20

This cell is programmed by grounding the source terminal, applying a 5 to 10 volt signal to the drain terminal or the bit line ($V_{BL}=5v$), and applying a high programming voltage V_{PP} of, for example, 18 to 20 volts to control gate 102 ($V_{CG}=V_{PP}$). The high voltage on V_{CG} creates a high electric field across tunnel oxide 110 generating hot electrons in the channel with enough energy to cross the tunnel oxide. These hot electrons are then trapped in the floating gate poly-1 layer 100 resulting in a higher threshold voltage for the transistor. The cell is thus programmed into an OFF (non-conducting) state.

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Erasing of the cell is performed by grounding the control gate and the drain terminal and applying V_{pp} to the source terminal. The large gate to source voltage causes the trapped electrons on the floating poly 100 to tunnel through the thin oxide layer 110 by a mechanism known as Fowler-Nordhiem.

5 The electrons are collected by the source region 104.

10 The flash memory cell shown in Figure 1, however, suffers from a number of drawbacks in terms of its overall performance. Because the source region 104 is subject to very high erase voltages (V_{pp}), this cell requires a carefully engineered high-voltage junction process. As shown in Figure 1, the source region 104 is made deeper than the drain region 106 and has a higher doping concentration. The high-voltage junction requirement results in a more complex and therefore more expensive process. Further, the high-voltage junction requirement results in a cell that is not scaleable. That is, the high-voltage diffusion to high-voltage diffusion spacing requirements increases the cell layout pitch. Lower endurance is another drawback of the high-voltage junction, since under high voltage conditions, the source region 104 cannot withstand a large number of erasures.

20 Furthermore, applying the high V_{pp} voltage to the source region 104 generates hot holes that are released into the P-well 108 and then collected and trapped inside the tunnel oxide 110. This phenomenon, sometimes referred to as band bending, not only deteriorates the endurance of the cell, it also results in unpredictable erase threshold voltage over time. Additional erase threshold
25 voltage verification circuitry are thus necessary for proper operation of the cell.

30 Finally, because the tunnel oxide region 110 is the same size as the channel, its capacitance is relatively larger, and thus the cell coupling capacitance is lower. Lower cell coupling capacitance requires larger program and erase voltages. Larger program and erase voltages not only lower the endurance of the cell, they also add to the circuitry as they require large pump circuits.

An improvement to the flash cell shown in Figure 1 splits the erase voltage between the control gate 102 and the source 104. Instead of applying a high voltage to the source region 104, the control gate 102 is negatively biased with respect to the source terminal. Thus, in this embodiment, programming
5 voltages remain the same, but during erase, a negative voltage is applied to the control gate ($V_{CG} = -V_{PP}$) while the source terminal connects to the positive power supply voltage (typically 3 to 5 volts). This allows the source junction to be the same size as the drain junction, and eliminates the high-voltage junction process requirements. However, this cell requires an additional negative pump circuit
10 and still suffers from the hot hole injection and the resulting erratic erase threshold voltage.

Various other implementations of a single-transistor flash cell have been proposed each improving on some aspects of the cell performance, but with trade-offs in other aspects. For example, one approach that eliminates performance degradations caused by the hot hole injection, places the P-well 108
15 inside another N-well. This allows the P-well 108 to be biased to a positive voltage along with the source and drain regions, while the control gate is biased negatively for an erase operation. This type of flash cell, however, requires a triple well technology that is much more complex and costly to manufacture.
20 Further, the cell still requires a negative pump circuit to bias the control gate during erase.

While there have been numerous variations on the double poly
25 stacked gate single-transistor flash cell, there is room for improvement of the structure and design of the cell in terms of endurance, speed, reliability and cost of manufacture.

SUMMARY OF THE INVENTION

The present invention provides a novel scaleable flash memory cell structure and method of manufacture that improves data retention, increases capacitive coupling and speed of operation, and improves reliability among other advantages. The flash cell of the present invention permits implementation of arrays of flash memory cells that allow the designer to program and/or erase individual bytes of memory as well as blocks of memory. Therefore, the non-volatile memory circuit of the present invention combines the advantages of conventional EEPROM technology with that flash technology.

Broadly, the flash cell according to the present invention limits the tunnel oxide to a window having dimensions at the minimum feature size located over the drain side of the transistor. The tunnel oxide window is separated from the field oxide and has no edges abutting field oxide. Thus, leakage due to defects caused by the field edge is eliminated, resulting in higher data retention rates for the cell. The reduced dimensions of the tunnel oxide region significantly increase the gate capacitive coupling ratio of the cell. The higher gate coupling allows the cell to be smaller yet operate at higher speed (larger read current). The higher coupling ratio also reduces the level of the maximum required voltage resulting in higher endurance.

Accordingly, in one embodiment, the present invention provides a memory cell including a source region and a drain region forming a channel therebetween; a channel oxide layer disposed on top of the channel; a floating gate layer disposed on top of the channel oxide layer, where the floating gate layer and channel oxide layer define a window wherein a thickness of the channel oxide is substantially smaller than the remaining portion of the channel oxide. The memory cell further includes a control gate layer disposed on top of and separated from the floating gate layer by a dielectric film, wherein the window is located on a drain side of the channel and has dimensions at minimum feature size.

In another embodiment, the present invention provides a method of manufacturing a memory cell including the steps of

A better understanding of the nature and advantages of the flash memory of the present invention may be had with reference to the drawings and detailed description below.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows an exemplary prior art double poly stacked gate single transistor flash memory cell;

Figure 2A shows a top view of a specific embodiment of a single flash cell as initially laid out, while Figures 2B and 2C show top views of two different embodiments of the cell after it has been formed;

Figure 3 illustrates the cross section of two flash memory cells perpendicular to word line and a high voltage transistor switch according to the present invention;

Figure 4 is a circuit schematic for an exemplary memory array made of flash cells according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Various aspects of the flash memory according to the present invention will be described in detail hereinafter.

Cell Structural Design

Referring to Figures 2A and 2B, there are shown top views of a specific embodiment of a single flash cell of the present invention as initially laid out, and a of the cell after it has been formed, respectively. In a preferred embodiment, each flash cell is implemented in a double poly, single metal, twin

well CMOS process. As shown in Figure 2A, active area 20 (e.g., N+) is diffused into a well region (e.g., P-well). A control gate polysilicon layer 25 is laid out perpendicular to active region 20 and defines drain and source regions 21 and 22, respectively. The overlap area between control gate polysilicon 25 and active area 20 forms the transistor channel region 26. A non-self aligned tunnel window 23 is formed on the drain side (21) of each memory cell as depicted. A floating polysilicon layer 24 overlaps active area 20.

As shown in Figure 2A, tunnel area 23 partially extends over drain region 23 such that it has a first region 23A under gate poly 25 (i.e., over the channel) and a second region 23B over drain 21. The overlap region 23B of tunnel window 23 will be removed during subsequent steps in the process.

Figure 2B shows a top view of the flash cell as formed at the completion of the process. As depicted in Figure 2B, both tunnel window 23 and floating gate poly 24 are etched back to within the area of channel region 26. Note that the area defining tunnel window 23 does not coincide with the area defining channel region 26. This appreciably increases the gate capacitive coupling ratio of the cell allowing faster operation. Furthermore, in the preferred embodiment shown, tunnel oxide window 23 as thus formed is separated from the field oxide ^{edges 28A and 28B} (not shown) and has no edges abutting field oxide, eliminating potential leakage caused by defects at the field edge. Tunnel oxide window 23 may alternatively extend all the way to the field edges ^{28A and 28B} of the channel as shown in Figure 2C. The memory cell embodiment shown in Figure 2C still exhibits the higher gate capacitive ratio because tunnel window 23 does not coincide with the entire area defining channel region 26.

Referring to Figure 3, there is shown a cross section of two flash memory cells 200-1 and 200-2 in a direction perpendicular to the word line, and a high voltage transistor switch 216 according to one embodiment of the present invention. In this exemplary implementation, N+ source drain regions are

diffused into a p-well region 208, and the drain region for one cell acts as the source for the adjacent cell. That is, N+ region 211 forms the source terminal of cell 200-1, N+ region 209 forms the drain terminal of cell 200-1 as well as the source terminal of cell 200-2, and N+ region 215 forms the drain terminal of cell 200-2. Tunnel window 210 is formed on the drain side of each cell and is preferably of minimum feature size. As mentioned above, in a preferred embodiment, tunnel window 210 is fieldless (i.e., does not abut field oxide) which helps increase endurance. The active area surrounding the tunnel window is covered by relatively thicker cell gate oxide 212 of, for example, about 100-300 Angs. Tunnel window 210 comprises a thin, for example, 70- 100 Angs thermal dielectric. Thus, the cell channel region (26 in Figure 2B) is covered by both tunnel oxide window 210 (23A in Figure 2B) and relatively thicker gate oxide 212. The tunnel window/active area edge has a gradual step of, for example, 30-200 Angstroms thick.

A first preferably multiple stack polysilicon layer (poly-1 201 and 202 as shown in Figure 3), forming the memory cell floating polysilicon (i.e., charge storage layer), is formed on top of gate oxide (210 and 212). The total thickness of the multiple stack floating polysilicon 201/202 is preferably about, for example, 500 Angstroms, with typical grain size at the tunnel oxide boundary of approximately less than 100 Angstroms. The control gate terminal (connected to the word line) is formed by a second polysilicon (poly-2) layer 206 preferably combined with a polycide layer 207, that form a combined thickness of approximately 1000-2000 Angstroms. Poly-1 layer 201/202 and silicided poly-2 layer 206/207 are separated by, for example, 150-200 Angstroms thick Oxide-Nitride-Oxide (ONO) 203/204/205 dielectric stack. The memory as thus constructed includes a structure having a substrate>well>tunnel oxide>poly-1>ONO>poly2-polycide stack. Exemplary value for the size of the stack may be approximately 0.28-.34 μm .

Cell Process Flow

The cell formation according to one embodiment of the present invention begins with a p-type silicon substrate 214. After the typical CMOS steps forming N- and P-well regions, active areas ³⁶(36 in Figure 2B) are defined by masking and etching steps. This is preferably followed by a field implant to increase the parasitic field threshold voltage. A thick field oxide of, for example, 3000-5000 Angstroms is then grown all over the wafer to isolate different active areas followed by nitride strip and kooi oxide growth. A p-well protect mask is then used to block p-well formation from areas where high voltage circuit blocks will be built. This is to avoid high back-biased threshold voltages of highly doped p-well.

After resist strip and an oxide clean step, gate oxide 212 is formed by growing a high quality thermal oxide (e.g., 150-190 Angstroms thick) all over the wafer. This is followed by a cell threshold voltage (Vt) adjust mask and an implant (using e.g., Boron) to adjust the cell threshold to appropriate value between the programmed and the erased Vt distribution target. After implant the resist is stripped.

The wafers are then masked to form tunnel windows 210 for the memory cells. This mask is a critical mask as this term is used in the art. The wafers are then subjected to a short (e.g., 10-25 sec.) wet oxide cleaning step to clean the tunnel windows with non roughening characteristics. The resist is removed from the wafers and the surface is cleaned again to remove organic, metallic and hydrocarbons from the surface.

The next step involves forming the tunnel oxide by growing a high quality thermal oxide, of for example 70-85 Angstroms to cover the whole wafer. This is followed by deposition of the first of several layers of polysilicon layers to form the floating polysilicon having layers that are each engineered with varying grain sizes. The top layer of poly (layer 202) is preferably implanted

with N+ dopants to amorphize the poly and dope it to achieve for example 200-500 ohms/square sheet resistivity.

5 The wafers are then oxidized (at e.g., 900-1050 C) to grow thermal oxide of for example 100 Angstroms. This step forms oxide layer 203 and is followed by deposition of about 75-90 Angstroms of silicon-nitride (layer 204) grown at exemplary temperatures of 650-700 C. The wafers are then subjected to a wet oxidation to cover the nitride surface with 30-50 Angstroms of blocking oxide (1000 C wet oxidation to grow 3500-4000 Angs on bare silicon). This series of steps forms ONO layers 203/204/205.

10 Next, the wafers are masked again to etch ONO/poly-1/gate-tunnel islands in the memory array. This etch is preferably performed anisotropically and is designed to endpoint on the tunnel oxide. The polysilicon/ONO/gate oxide stack on high voltage transistors 216 are also masked in this step to protect the high voltage (HV) transistor gates 222. After resist strip the wafers are subjected to a light oxidation at 800-900 C in a dry ambient. This oxidation is done to seal off the exposed edges of floating gate 201/202 that is freshly exposed after the etch.

20 The memory array core is then masked to clean the periphery with a wet/dry etch. The memory array core mask is also used to protect the high voltage circuit areas. After the etch, the resist is stripped and the wafers are masked again to form self-aligned high voltage graded junctions for the HV enhancement transistors. The high voltage implant could be for example a Phosphorus 31 implant 5E13-5E14 #/cm2 or a double-diffused Phosphorus/arsenic combination implant.

25 After the implant, the resist is stripped and the wafers are subjected to a low voltage threshold adjust mask or blanket, and implant sequence followed by a high quality wet gate oxidation to grow about 70-110 Angstroms of oxide in

the periphery active areas. The wafers are then covered with approximately 1.5 kA to 2.0 kA polysilicon layer that forms the gate of the periphery transistors and the first poly layer (206) of the word line for memory cell array. To reduce heat generation and resistivity of the word line poly, a 1000-2000 Angstrom layer of WSi_x is deposited over the entire wafer that forms the top layer 207 for the control gate of the memory cell. Next, the wafers are subjected to re-oxidation at about 900-950 C for approximately 30-50 minutes.

The memory cell stack is then defined by a masking step that also protects the periphery. The stacked array mask etch is used to etch the polycide/ONO/poly-1/tunnel sandwich 200. After the etch, wafers are cleaned to remove organics, hydrocarbons and post etch residues. The high voltage transistors are covered with resist during this etch.

The wafers are masked again to define the gate polycide of the periphery low voltage transistors. After the gate poly etch the resist is stripped. The high voltage transistors are exposed during this etch. Both the polycide and the poly are etched away. About 100 Angstroms of ONO is etched away also leaving a 50-100 Angstroms of dielectric on the HV gates.

The n-tip mask is then used to form the lightly doped drain (LDD) tips of the NMOS transistor followed by p-tip mask and implant. The n-tip mask is blocked from memory array and HV transistors. The spacer deposition is followed by spacer etch and N+ and P+ source drain formation. The first interlayer dielectric is then formed by either BPSG, BPTEOS with 4/4 B/P, or the like. The inter layer dielectric (ILD) is then reflowed at about 850-920 C and SOG planarized and the contacts are masked and opened.

This is followed by barrier metal deposition followed by tungsten plug formation and first metal (metal-1) deposition. The metal-1 mask is then used to define the interconnect and memory array bit lines. Finally, metal-1

layer is covered with thick ILD and passivation oxynitride is deposited and etched using the pad mask.

Cell Electrical Design

5 In a preferred embodiment of the present invention cells are programmed (e.g., high cell Vt) and erased (e.g., low cell Vt) by Fowler Nordhiem tunneling to and from the same tunnel window on the drain side. The various modes of operation, including programming, erase and read will be described in connection with the exemplary memory array circuit shown in Figure 4. Referring to Figure 4 there is shown an exemplary circuit schematic for an array 400 made of flash memory cells according to the present invention. Array 400 includes memory cells 402 located at intersection of 16 word lines (WL0-WL15) and 16 bit lines (BL0-BL15). Bit line select transistors 404 respectively couple bit lines BL0-BL15 to memory cells 402. Source select transistors 406 couple ground (or Vss) to memory cells 402. A bit line select control line BSL controls gate terminals of bit select transistors 404, and a source select control line SSL controls gate terminals of source select transistors 406.

20 Table I below sets forth a preferred biasing scheme for various cell operations for an individual cell according to the present invention.

Table I

<u>Control Line</u>	<u>Erase</u>	<u>Program</u>	<u>Read</u>	<u>Condition</u>
BSL	Vcc	Vcc	Vcc	Selected
SSL	Vss	Vss	Vcc	Selected
25 BL0	Vcc	Vss	1.0-1.4V	Selected
BL1	Vss	Vcc	0.5V	Unselected
WL0	Vcc	Vcc	Vcc	Unselected
WL1	-12 to -15V	15-20V	Vss	Selected

30 Erase Operation:

In the exemplary biasing convention described herein, cells are erased by the action of applying negative gate voltage of, for example, -12 to -15 volts on the selected word lines or a single word line (WL1), and applying a voltage approximately equal to V_{cc} (e.g., $V_{cc}-2V_{tn}$ to V_{cc}) on the selected bit lines or a single bit line (e.g., BL0). A voltage of about V_{cc} is applied to bit line select control line BSL, while source select control line SSL is coupled to ground or V_{ss} . This condition generates the necessary electrical field to force electrons to leave the floating gate through the cell tunnel oxide drain interface. This results in a reduced threshold voltage for the cell.

The bit line voltage level is selected to ensure suppression of band bending and hot hole injection from the cell drain into the tunnel oxide. However, due to the reduced tunnel area of the cell of the present invention and the resulting increase in cell coupling ratio, the voltage applied to the bit line can be as low as V_{cc} .

The erase coupling is adequate to achieve read/erase threshold voltage V_{trde} of, for example, about -2.5 V. A V_{trde} of -2.5 volts helps achieve adequate read current with a lower word line voltage. Further, even with a V_{trde} of -2.5 V, the cell of the present invention does not suffer from over-erase. Conventional memory cells, such as single transistor ETOX cells, however, do suffer from over-erase when negative threshold voltages are used (i.e., cells are driven into deep depletion). Such over-erase leads to significant performance drawbacks such as program inhibit and/or wide erase threshold variations. The flash cell according to the present invention is less sensitive to both these problems.

The engineering of the erase interface (floating poly/tunnel oxide) in the flash cell of the present invention is controlled by limiting the fluctuation of the local barrier height seen by electrons. This allows a tight threshold convergence without relying on algorithm circuits. Secondly, the nature of the

memory cell of the present invention limits the threshold variation. The threshold voltage of the thick gate oxide portion of the cell helps to improve the punch-through margin of the cell.

5 Typical erase current depends on the block size and is of the order of a few mA. The erase speed is primarily a function of the field across tunnel oxide which can be, for example, approximately 8.5 to 10 MV/cm to achieve block erasure in less than for example 1 msec.

10

Programming operation:

15 The programming operation is done by applying a high voltage (e.g., 15 to 20 V) on the selected word line (WL1) and grounding the selected bit line (BL0), while the unselected bit lines (BL1-BL15) are at Vcc. Referring to Figure 4, to program memory cell 402-C, a high voltage of for example 15 to 20 volts is applied to WL1. Vcc is applied to BSL control line and WL0 to couple BL0 to the drain terminal of memory cell 402-C. With BL0 grounded, the drain terminal of cell 402-C receives ground potential. Control line SSL remains at VSS and unselected word lines WL2-WL15 receive VCC. Thus, the cells are programmed serially in a NAND type structure by passing Vss to the selected cells as the pass (unselected) word lines are pulled up to pass Vss.

20

25 The typical programming current for the memory cell of the present invention may be, for example, as low as about 100 pA/cell. The typical programming current required by convention ETOX cells, on the other hand, is around 1 mA. The lower programming current requirement of the present invention allows for the pump circuits to be aggressively down sized, for a more compact overall design.

30

Another advantageous feature of the present invention is that it provides for the ability to erase and/or program on a byte by byte basis. Because neither erase nor programming operations require shifting the potential supplied to the entire bulk (substrate) for the array of cells, erase or programming of memory array 400 need not be limited to the entire block.

Read Operation:

The read operation is accomplished by grounding the selected word line $WL1=V_{ss}$ and applying a low voltage of, for example, 1.0-1.5 volts to the selected bit line $BL0$. Unselected bit lines ($BL1-BL15$) receive a voltage in the range of V_{ss} to 0.5 volts. Unselected word lines $WL0$ and $WL2-WL15$ receive V_{cc} which allows their memory cells 402 to pass V_{ss} to the selected cell, e.g., 402-C, and couple the drain terminal of selected memory cell 402-C to selected bit line $BL0$. If memory cell 402-C is programmed (i.e., high V_t), then the voltage on selected bit line $BL0$ remains unaffected. If memory cell 402-C is not programmed (i.e., low V_t), selected bit line $BL0$ is pulled down to V_{ss} .

Finally, when changing from one mode (e.g., erase) to another (e.g., program, the memory array first enters the program inhibit mode of operation. The program inhibit mode avoids accidental programming of the cell during the transition from one mode of operation to another. In program inhibit mode, according to the present invention, the entire array enters an unselected condition by applying V_{ss} to BSLs, SSLs and BLs, and V_{cc} to WLs.

In conclusion, the present invention offers a single transistor, double-poly flash cell and a method of manufacture for the same that improves data retention, increases capacitive coupling and speed of operation, and improves reliability among other advantages. While the above is a complete description of the preferred embodiment of the present invention, it is possible to use various alternatives, modifications and equivalents. Therefore, the scope of the present invention should be determined not with reference to the above

description but should, instead, be determined with reference to the appended claims, along with their full scope of equivalents.

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WHAT IS CLAIMED IS:

- 1 *Sub a1* 1. A memory cell comprising:
2 a source region and a drain region forming a channel therebetween;
3 a channel dielectric layer disposed on top of said channel;
4 a floating polysilicon layer disposed on top of said channel
5 dielectric layer, said floating polysilicon layer and channel dielectric layer
6 defining a window within an area of said channel wherein a thickness of said
7 channel dielectric layer in said window is smaller than that of a remaining
8 portion of said channel dielectric layer; and
9 a control gate layer disposed on top of and separated from said
10 floating gate layer by a dielectric film,
11 wherein said window is located on a drain side of said channel.
2. The memory cell of claim 1 wherein a dimension of said
window is of minimum process feature size.
3. The memory cell of claim 1 further comprising field
dielectric layer substantially surrounding first and second sides of said channel,
and wherein, said window has no sides abutting said field dielectric layer.
4. The memory cell of claim 1 further comprising filed
dielectric layer substantially surrounding first and second sides of said channel,
and wherein said sides of said window abut said field dielectric layer.
5. The memory cell of claim 1 wherein said channel dielectric
layer comprises silicon dioxide material, said control gate layer comprises
polysilicon material, and said dielectric film comprises a layer of nitride material
sandwiched between first and second silicon dioxide layers.

1 6. The memory cell of claim 5 wherein said control gate layer
2 further comprises a polycide layer on top of said polysilicon layer.

1 7. An array of flash memory cells, comprising:
2 a plurality of memory cells as defined in claim 1 arranged in a
3 plurality of columns, each column of memory cells comprising:
4 a bit line select transistor having a first current-carrying
5 terminal coupled to a bit line, and a gate terminal coupled to a bit line
6 select control line;
7 a predefined number of memory cells coupled in series with a
8 drain end coupling to a second current-carrying terminal of said bit line
9 select transistor, said predefined number of memory cells being serially
10 coupled such that a drain node of a memory cell acts as a source node of
11 an adjacent memory cell; and
12 a source line select transistor having a first current-carrying
13 terminal coupled to a source end of said predefined number of memory
14 cells, a gate terminal coupled to a source select ^{line} ~~line~~ and a second current
15 carrying terminal coupled to a low potential.

1 8. An array of flash memory cells comprising:
2 a plurality of columns of serially connected flash memory cells,
3 each memory cell having a gate terminal;
4 a plurality of bit lines respectively coupled to drain side of said
5 plurality of columns of memory cells via a respective plurality of bit line select
6 transistors, said plurality of bit line select transistors having gate terminals
7 coupled to a bit line select control line;
8 a plurality of word lines, each one coupling to a gate terminal of
9 one memory cell in each of said plurality of columns to form rows of memory
10 cells with common gate terminals; and

11 a plurality of source select transistors respectively coupling a source
 12 side of said plurality of columns of memory cells to a logic low voltage, and
 13 having gate terminals coupled to a source select control line,

14 wherein, during programming:

15 a logic high voltage is applied to said bit line select control line to
 16 turn on bit line select transistors,

17 a logic low voltage is applied to source select control line to turn
 18 off source select transistors;

19 a logic low voltage is applied to a selected bit line while a logic
 20 high voltage is applied to unselected bit lines, and

21 a logic high voltage is applied to unselected word lines, while a
 22 boosted positive voltage is applied to a selected word line.

9. An array of flash memory cells comprising:

a plurality of columns of serially connected flash memory cells,
 each memory cell having a gate terminal;

a plurality of bit lines respectively coupled to drain side of said
 plurality of columns of memory cells via a respective plurality of bit line select
 transistors, said plurality of bit line select transistors having gate terminals
 coupled to a bit line select control line;

a plurality of word lines, each one coupling to a gate terminal of
 one memory cell in each of said plurality of columns to form rows of memory
 cells with common gate terminals; and

a plurality of source select transistors respectively coupling a source
 side of said plurality of columns of memory cells to a logic low voltage, and
 having gate terminals coupled to a source select control line,

wherein, during erase:

a logic high voltage is applied to said bit line select control line to
 turn on bit line select transistors,

a logic low voltage is applied to source select control line to turn
 off source select transistors;

19 a logic high voltage is applied to a selected bit line while a logic
20 low voltage is applied to unselected bit lines, and
21 a logic high voltage is applied to unselected word lines, while a
22 boosted negative voltage is applied to a selected word line.

- 1 10. An array of flash memory cells comprising:
2 a plurality of columns of serially connected flash memory cells,
3 each memory cell having a gate terminal;
4 a plurality of bit lines respectively coupled to drain side of said
5 plurality of columns of memory cells via a respective plurality of bit line select
6 transistors, said plurality of bit line select transistors having gate terminals
7 coupled to a bit line select control line;
8 a plurality of word lines, each one coupling to a gate terminal of
9 one memory cell in each of said plurality of columns to form rows of memory
10 cells with common gate terminals; and
11 a plurality of source select transistors respectively coupling a source
12 side of said plurality of columns of memory cells to a logic low voltage, and
13 having gate terminals coupled to a source select control line,
14 wherein, during program inhibit a logic low voltage is applied to
15 said bit line select control line, source select control line, and bit lines, while a
16 logic high voltage is applied to word lines.
- add a2*

A scalable flash memory cell structure and method of manufacture is disclosed that improves data retention, increases capacitive coupling and speed of operation, and improves reliability among other advantages. The flash cell according to the present invention limits the tunnel oxide to a window having dimensions at the minimum feature size located over the drain side of the transistor. The tunnel oxide window is separated from the field oxide and has no edges abutting field oxide.

10

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **SERIAL FLASH MEMORY** the specification of which X is attached hereto or was filed on as Application No. and was amended on (if applicable).

I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56. I claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign applications(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

Country	Application No.	Date of Filing	Priority Claimed Under 35 USC 119
			Yes <input type="checkbox"/> No <input type="checkbox"/>
			Yes <input type="checkbox"/> No <input type="checkbox"/>

I hereby claim the benefit under Title 35, United States Code §119(e) of any United States provisional application(s) listed below:

Application No.	Filing Date
60/025,698	September 9, 1996

I claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application No.	Date of Filing	Status
		<input type="checkbox"/> Patented <input type="checkbox"/> Pending <input type="checkbox"/> Abandoned
		<input type="checkbox"/> Patented <input type="checkbox"/> Pending <input type="checkbox"/> Abandoned

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

Babak S. Sani, Reg. No. 37,495

Send Correspondence to: Babak S. Sani TOWNSEND and TOWNSEND and CREW LLP Two Embarcadero Center, 8th Floor San Francisco, CA 94111-3834	Direct Telephone Calls to: (Name, Reg. No., Telephone No.) Name: Babak S. Sani Reg. No.: 37,495 Telephone: 415/576-0200
---	--

Full Name of Inventor 1	Last Name POURKERAMATI	First Name ALI	Middle Name or Initial	
Residence & Citizenship	City Palo Alto	State/Foreign Country CA	Country of Citizenship U.S.	
Post Office Address	Post Office Address 580 Channing Ave.	City Palo Alto	State/Country CA	Zip Code 94301
Full Name of Inventor 2	Last Name	First Name	Middle Name or Initial	
Residence & Citizenship	City	State/Foreign Country	Country of Citizenship	
Post Office Address	Post Office Address	City	State/Country	Zip Code
Full Name of Inventor 3	Last Name	First Name	Middle Name or Initial	
Residence & Citizenship	City	State/Foreign Country	Country of Citizenship	
Post Office Address	Post Office Address	City	State/Country	Zip Code

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

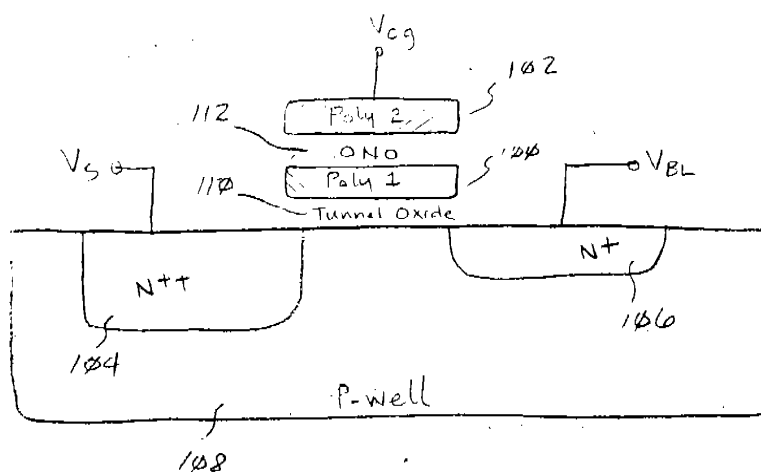
Signature of Inventor 1 ALI POURKERAMATI	Signature of Inventor 2	Signature of Inventor 3
Date	Date	Date

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22-141 50 SHEETS
22-142 100 SHEETS
22-144 200 SHEETS



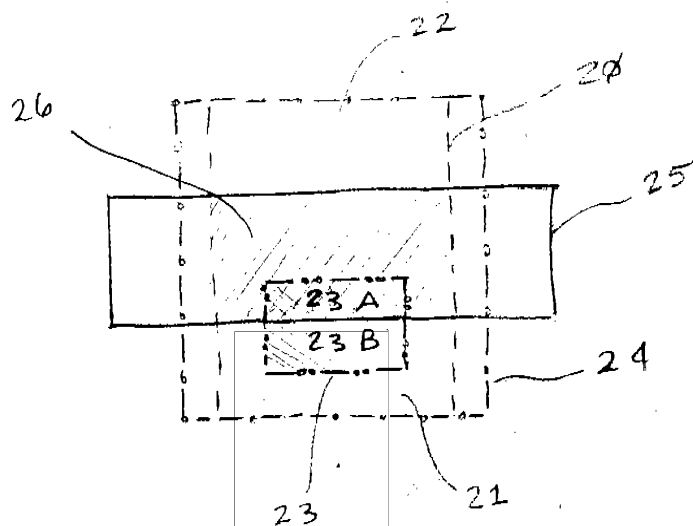
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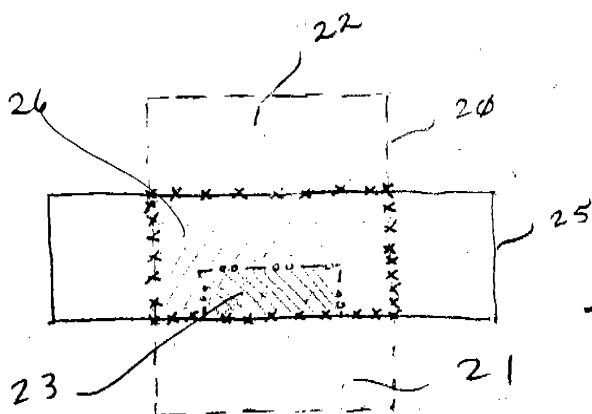
- FIGURE 1 -
(PRIOR ART)



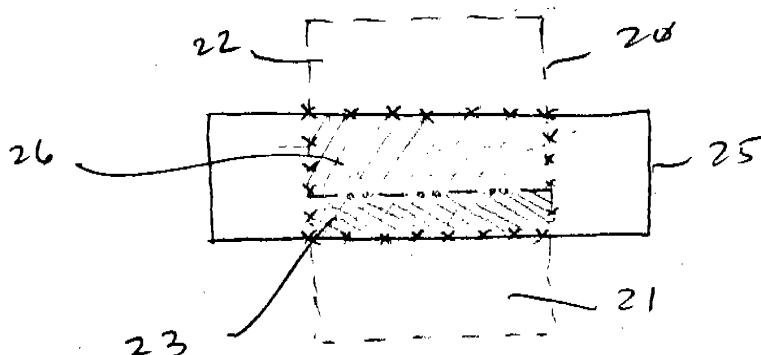
-FIG. 2-



- FIG. 2A -



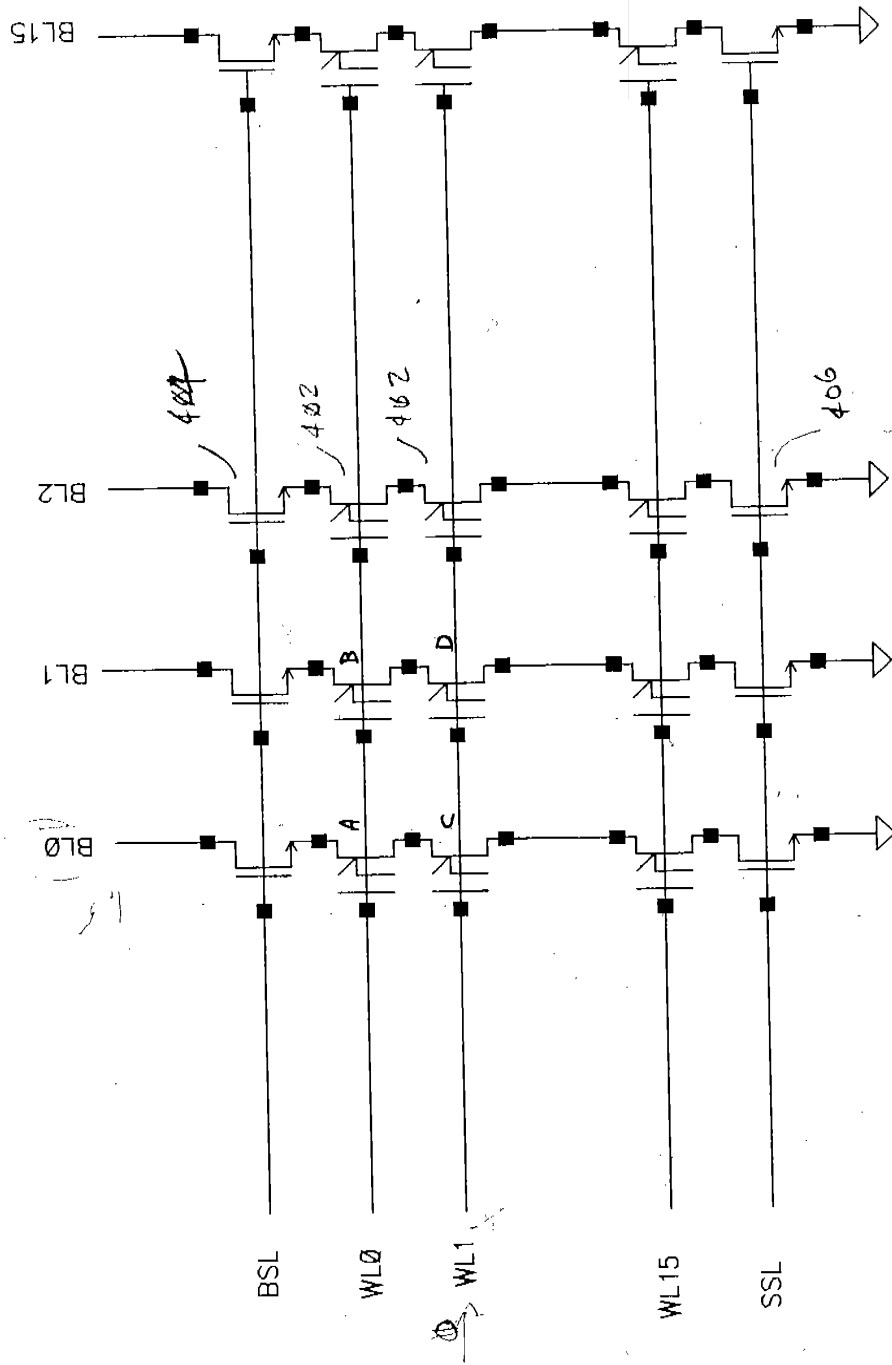
- FIG. 2B -



- FIG. 2C -

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264060-92592680

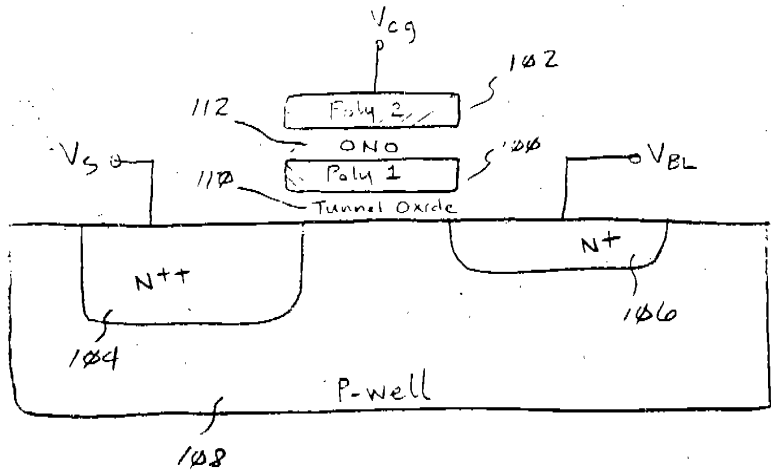
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-FIGURE 4-

PRINT OF DRAWINGS
AS ORIGINAL FILED

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365/185.18



- FIGURE 1 -
(PRIOR ART)

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22-142 100 SHEETS
22-144 200 SHEETS

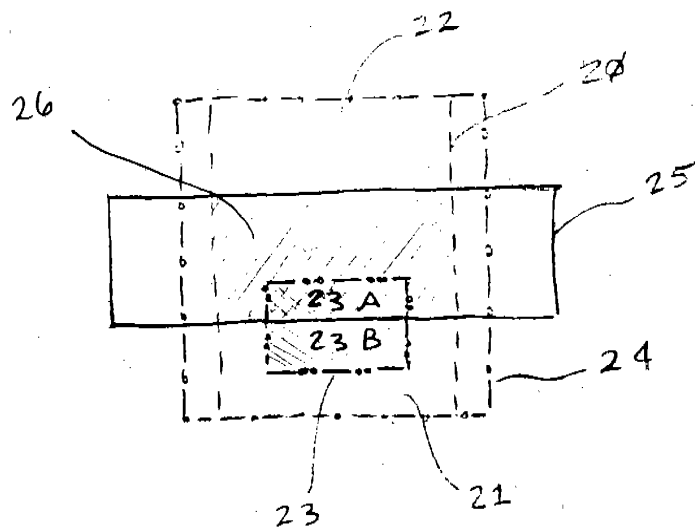


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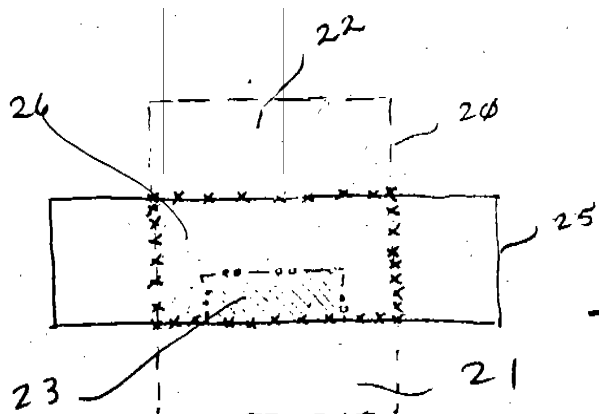
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22-142 100 SHEETS
22-144 200 SHEETS



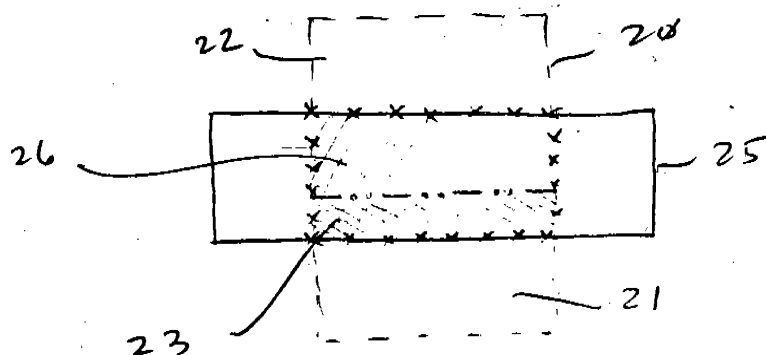
201000-92592680



- FIG. 2A -



- FIG. 2B -

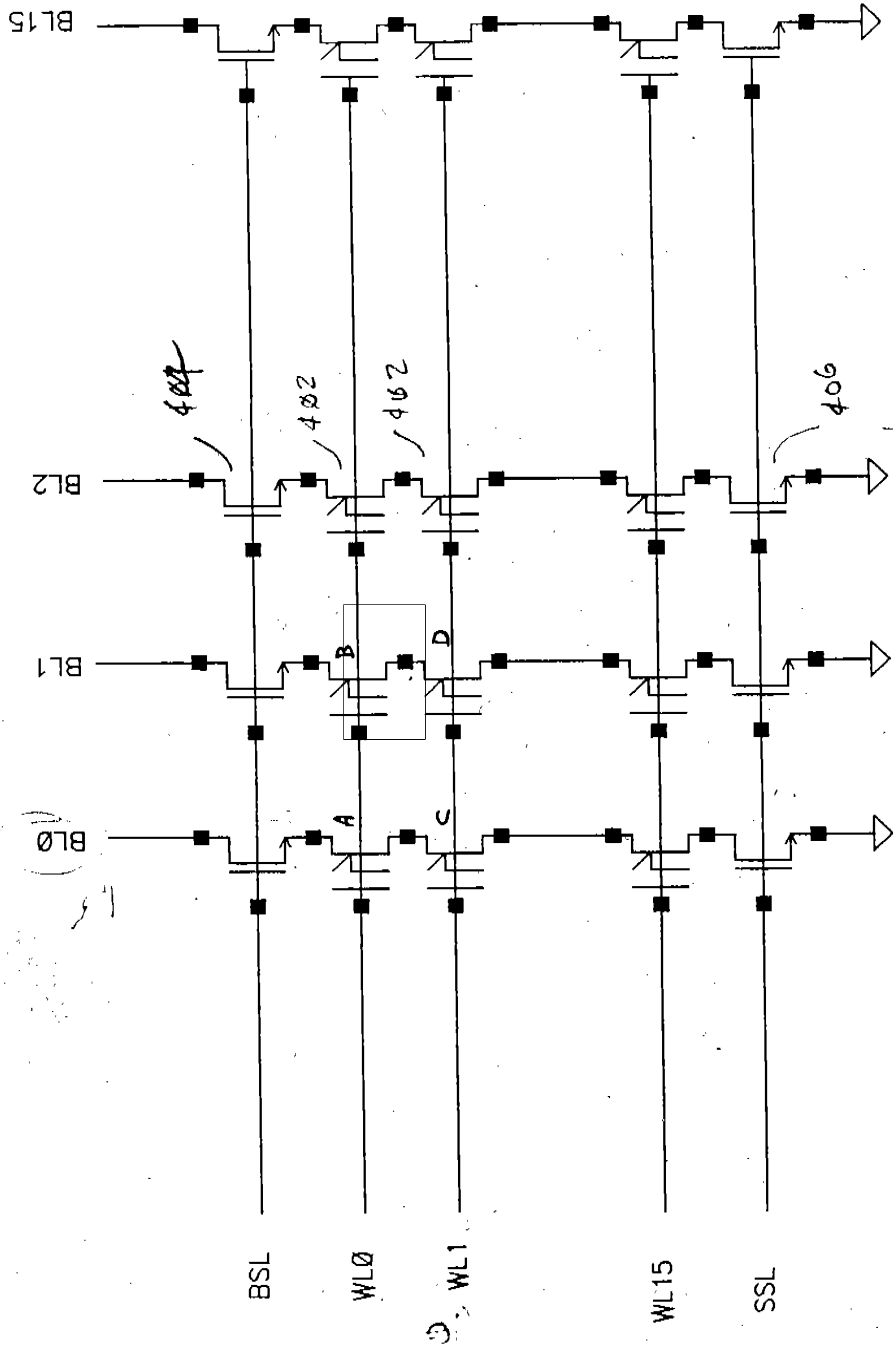


- FIG. 2C -

PRINT OF DRAWINGS
AS ORIGINAL FILED

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400



-FIGURE 4-



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO./TITLE
--------------------	---------------------	-----------------------	---------------------------

08/926,576 09/04/97 POURKERMATI

A 1782211

0262/0123

BABAK S SANI
TOWNSEND AND TOWNSEND AND CREW
TWO EMBARCADERO CENTER 8TH FLOOR
SAN FRANCISCO CA 94111

NOT ASSIGNED

DATE MAILED:

2511

01/23/98

NOTICE TO FILE MISSING PARTS OF APPLICATION
Filing Date Granted

An Application Number and Filing Date have been assigned to this application. However, the items indicated below are missing. The required items and fees identified below must be timely submitted **ALONG WITH THE PAYMENT OF A SURCHARGE** for items 1 and 3-6 only of \$ 130 for a ☒ large entity ☐ small entity in compliance with 37 CFR 1.27. The surcharge is set forth in 37 CFR 1.16(e). Applicant is given **TWO MONTHS FROM THE DATE OF THIS NOTICE** within which to file all required items and pay any fees required above to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

If all required items on this form are filed within the period set above, the total amount owed by applicant as a
☒ large entity ☐ small entity (verified statement filed), is \$ 130.

☐ 1. The statutory basic filing fee is:

- ☐ missing.
☐ insufficient.

Applicant must submit \$ _____ to complete the basic filing fee and/or file a verified small entity statement claiming such status (37 CFR 1.27).

☐ 2. Additional claim fees of \$ _____, including any multiple dependent claim fees, are required.

Applicant must either submit the additional claim fees or cancel additional claims for which fees are due.

☐ 3. The oath or declaration:

- ☐ is missing.
☐ does not cover the newly submitted items.
☐ does not identify the application to which it applies.
☐ does not include the city and state or foreign country of applicant's residence.

An oath or declaration in compliance with 37 CFR 1.63, including residence information and identifying the application by the above Application Number and Filing Date is required.

☒ 4. The signature(s) to the oath or declaration is/are:

- ☐ missing.
☐ by a person other than inventor or person qualified under 37 CFR 1.42, 1.43, or 1.47.

A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.

☐ 5. The signature of the following joint inventor(s) is missing from the oath or declaration:

An oath or declaration listing the names of all inventors and signed by the omitted inventor(s), identifying this application by the above Application Number and Filing Date, is required.

☐ 6. A \$ _____ processing fee is required since your check was returned without payment (37 CFR 1.21(m)).

☐ 7. Your filing receipt was mailed in error because your check was returned without payment.

☐ 8. The application does not comply with the Sequence Rules.

See attached "Notice to Comply with Sequence Rules 37 CFR 1.821-1.825."

☐ 9. OTHER:

Direct the response and any questions about this notice to "Attention: Box Missing Parts."

A copy of this notice MUST be returned with the response.

Customer Service Center
Initial Patent Examination Division (703) 308-1202

FORM PTO-1533 (REV.7-98)

PART 3 - OFFICE COPY

U.S. GPO: 1995-404-490/40515



I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Attn: Box Missing Parts, Washington, D.C. 20231, on

3-9-98

TOWNSEND and TOWNSEND and CREW LLP.

By [Signature]

part Director #3

PATENT

Attorney Docket No. 17822-1-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:)	
ALI POURKERMATI)	Examiner: Unassigned
Serial No.: 08/926,576)	Art Unit: 2511
Filed: 9/4/97)	TRANSMITTAL LETTER - RESPONSE
For: SERIAL FLASH MEMORY)	<u>TO NOTICE OF MISSING PARTS</u>

Attn: Box Missing Parts
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Pursuant to the Notice to File Missing Parts of Application - Filing Date Granted dated January 23, 1998, enclosed are the following to be made of record in the above-identified application:

- 1) Executed Declaration
- 2) Power of Attorney
- 3) Verified Statement Claiming Small Entity Status
- 4) Copy of Notice of Missing Parts

Please charge Deposit Account No. 20-1430 for the following fees:

(a) Missing Parts Surcharge (\$1.16(e))	65.00
TOTAL FEES TO BE CHARGED	\$65.00

The Commissioner is hereby authorized to charge any additional fees associated with this paper or during the pendency

ALI POURKERMATI
Serial No.: 08/926,576
Page 2

PATEA

of this application, or credit any overpayment to Deposit Account No. 20-1430 for this paper and during the prosecution of this application. This Transmittal Letter is submitted in triplicate.

Respectfully submitted,


Babak S. Sani
Reg. No. 37,495

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
(415) 576-0200
Fax (415) 576-0300
BSS:db

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UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

#3

APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO./TITLE
--------------------	---------------------	-----------------------	---------------------------

08/926,576	09/04/97	POURKERMATI	A 1782211
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BABAK S. SANI
TOWNSEND AND TOWNSEND AND CREW
TWO EMBARCADERO CENTER, 8TH FLOOR
SAN FRANCISCO CA 94111

0262/0123

NOT ASSIGNED

DATE MAILED: 2511

01/23/98

NOTICE TO FILE MISSING PARTS OF APPLICATION
Filing Date Granted

An Application Number and Filing Date have been assigned to this application. However, the items indicated below are missing. The required items and fees identified below must be timely submitted **ALONG WITH THE PAYMENT OF A SURCHARGE** for items 1 and 3-6 only of \$ 130 for a ☒ large entity ☐ small entity in compliance with 37 CFR 1.27. The surcharge is set forth in 37 CFR 1.16(e). Applicant is given **TWO MONTHS FROM THE DATE OF THIS NOTICE** within which to file all required items and pay any fees required above to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

If all required items on this form are filed within the period set above, the total amount owed by applicant as a ☒ large entity ☐ small entity (verified statement filed), is \$ 130.

1. The statutory basic filing fee is:

- ☐ missing.
☐ insufficient.

Applicant must submit \$ _____ to complete the basic filing fee and/or file a verified small entity statement claiming such status (37 CFR 1.27).

☐ 2. Additional claim fees of \$ _____, including any multiple dependent claim fees, are required.

Applicant must either submit the additional claim fees or cancel additional claims for which fees are due.

☐ 3. The oath or declaration:

- ☐ is missing.
☐ does not cover the newly submitted items.
☐ does not identify the application to which it applies.
☒ does not include the city and state or foreign country of applicant's residence.

An oath or declaration in compliance with 37 CFR 1.63, including residence information and identifying the application by the above Application Number and Filing Date is required.

☒ 4. The signature(s) to the oath or declaration is/are:

☐ missing.

by a person other than inventor or person qualified under 37 CFR 1.42, 1.43, or 1.47.

03/18/1998
01-FC4205

A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.

☐ 5. The signature of the following joint inventor(s) is missing from the oath or declaration:

An oath or declaration listing the names of all inventors and signed by the omitted inventor(s), identifying this application by the above Application Number and Filing Date, is required.

☐ 6. A \$ _____ processing fee is required since your check was returned without payment (37 CFR 1.21(m)).

☐ 7. Your filing receipt was mailed in error because your check was returned without payment.

☐ 8. The application does not comply with the Sequence Rules.

See attached "Notice to Comply with Sequence Rules 37 CFR 1.821-1.825."

☒ 9. OTHER:

Direct the response and any questions about this notice to "Attention: Box Missing Parts."

A copy of this notice MUST be returned with the response.

Customer Service Center
Initial Patent Examination Division (703) 308-1202

03/04/98 WED 18:10 FAX 415 576 400

TOWNSEND SF

#3 002



Attorney Docket No. 17822-1-1

DECLARATION

As a below named inventor, I declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **SERIAL FLASH MEMORY** the specification of which is attached hereto or X was filed on 9/4/97 as Application No. 08/926,576 and was amended on (if applicable).

I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56. I claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

Country	Application No.	Date of Filing	Priority Claimed Under 35 USC 119
			Yes <u> </u> No <u> </u>
			Yes <u> </u> No <u> </u>

I hereby claim the benefit under Title 35, United States Code §119(e) of any United States provisional application(s) listed below:

Application No.	Filing Date
60/025,698	9/9/96

I claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, section 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application No.	Date of Filing	Status
		<u> </u> Patented <u> </u> Pending <u> </u> Abandoned
		<u> </u> Patented <u> </u> Pending <u> </u> Abandoned

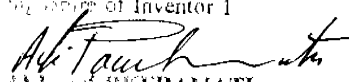
03/04/93 WED 16:11 FAX 415 570 0000

TOWNSEND SF

003

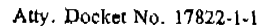
Full Name of Inventor 1	Last Name POURKERAMATI	First Name ALI	Middle Name or Initial	
Residence & Citizenship	City Redwood City	State/Foreign Country CA	Country of Citizenship U.S.	
Post Office Address	Post Office Address 3979 Brookline Way	City Redwood City	State/Country CA	Zip Code 94062
Full Name of Inventor 2	Last Name	First Name	Middle Name or Initial	
Residence & Citizenship	City	State/Foreign Country	Country of Citizenship	
Post Office Address	Post Office Address	City	State/Country	Zip Code
Full Name of Inventor 3	Last Name	First Name	Middle Name or Initial	
Residence & Citizenship	City	State/Foreign Country	Country of Citizenship	
Post Office Address	Post Office Address	City	State/Country	Zip Code

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful statements may jeopardize the validity of the application or any patent issuing thereon.

Signature of Inventor 1  ALI POURKERAMATI	Signature of Inventor 2	Signature of Inventor 3
Date 3. 4. 98	Date	Date

THEY SEND SF

008



Applicant or Patentee: Ali Pourkeramati
Application or Patent No.: 08/926,576
Filed or Issued: 9/4/97
Title: SERIAL FLASH MEMORY

hereby declare that I am:

- ☐ the owner of the small business concern identified below;
- ☒ an official of the small business concern empowered to act on behalf of the concern identified below;

Name of Small Business Concern: Azalea Microelectronics Corp.
Address of Small Business Concern: 3080 Olcott Street, Suite 130-D
Santa Clara, CA 95054

I hereby declare that the above-identified small business concern qualifies as a small business concern as defined in 13 CFR 121.101, as produced, 37 CFR 1.90(d), for purposes of paying reduced fees to the United States Patent and Trademark Office, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern, of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns and affiliates of each other when either, directly or indirectly, one concern controls or has power to control the other, or a third party or parties, which do, has the power to control both.

_____, hereby declare that rights under copyright in the above work have, up to the attention entitled by inventor(s) to Booth, and is described in

- Application No. 00-020176 Filed 04/07
Patent No. _____ Issued _____

inventions need not be made by a "defined small business" or by a "small" or "medium" sized individual, concern or organization having rights in the invention. It is sufficient that the right to the invention be held, by any person, other than the inventor, who would not qualify as an independent inventor under 37 CFR 1.56(a), by that person made, or by any concern that would not qualify as a small business concern under 37 CFR 1.56(b), for or on behalf of an organization under 37 CFR 1.56(c).

These certified statements are required from an "eligible person" (owner, inventor, or organization having rights to the invention) of small entities. (37 CFR 1.01)

(x) Small Business Concern ☐ Nonprofit Organization ☐

Small Business Corporation

On the date of the transfer, the transferee entity is not a small entity, resulting in an effective loss of small entity status. The transferee entity will be treated as a small entity for the first day on which it is a small entity after the date on which status as a small entity is lost.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true and that these statements were made with due knowledge of the lawful consequences of the falsity of the same and punishable by fine and imprisonment under section 1001 of Title 18 of the United States Code, and that each lawful false statement made herein and the validity of each lawful statement made herein are true and that each false statement is false.

Owner, Ali P. ...
President ...
3998 Brookline Way
Redwood City, CA 94061

Redwood City, Cal. 94061

Mr. F. J. [Signature]

Date 3.4.98



I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:
Assistant Commissioner for Patents,
Washington, D.C. 20231,

TOWNSEND and TOWNSEND and CREW LLP

By [Signature]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

ALI POURKERMATI

Application No.: 08/926,576

Filed: 9/4/97

For: SERIAL FLASH MEMORY

Examiner: To be announced

Art Unit: 2511

INFORMATION DISCLOSURE
STATEMENT UNDER
37 CFR \$1.97 and \$1.98

RECEIVED

APR 22 1998

GROUP 2500

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

The references cited on attached form PTO-1449 (copies enclosed) are being called to the attention of the Examiner. It is respectfully requested that the cited information be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "references cited" on any patent to issue therefrom.

Applicant believes that no fee is required for submission of this statement, since it is being submitted prior to the first Office Action. However, if a fee is required, the Commissioner is authorized to charge such fee to Deposit Account No. 20-1430. Please charge any additional fees or credit any overpayment to the above-noted deposit account.

Respectfully submitted,

[Signature]
Babak S. Sani
Reg. No. 37,495

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
(415) 576-0200 Fax (415) 576-0300
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GP.2511

PATENT

Attorney Docket No. 17822-1-1

#5
D. Sani
4-25-98

FORM PTO-1449 (Modified) 17 1998 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		Attorney Docket No. 17822-1-1	Serial No.: 08/926,576
Applicant: ALI POURKERMATI		Filing Date: 9/4/97	
Group: 2511 28/8			

Reference Designation U.S. PATENT DOCUMENTS						
Examiner Initial	Document No.	Date	Name	Class	Sub-class	Filing Date (If Appropriate)
AA						
AB						
AC						
AD						

FOREIGN PATENT DOCUMENTS						
	Document No.	Date	Country	Class	Sub-class	Translation (yes/no)
AE						
AF						
AG						
AH						

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)	
<u>TP</u> AI	"Semiconductor Memories," Betty Price, Texas Instruments USA, 2nd Ed., 1983, 1991, John Wiley & Sons, Chichester, New York, Brisbane, Toronto, Singapore, pp. 586-604
<u>TP</u> AJ	"A 3.3 V 32 Mb NAND Flash Memory with Incremental Step Pulse Programming Scheme," Suh et al., IEEE Journal of Solid-State Circuits, Vol. 30, No. 11, 11/95, pp. 1149-1156
<u>TP</u> AK	"A 35 ns Cycle Time 3.3 V Only 32 Mb NAND Flash EEPROM," Iwata et al., IEEE Journal of Solid-State Circuits, Vol. 30, No. 11, 11/95, pp. 1157-1162
<u>TP</u> AL	"Advanced Salicided BECMOS Technology for Complex PLDS," Advanced Micro Devices, USA, The 14th Annual IEEE Nonvolatile Semiconductor Memory Workshop, Monterey, CA 8/13-16, 1995
<u>TP</u> AM	"Process Technology and Device Built in Reliability in NOR Virtual Ground (NVG™) Flash Memories," National Semiconductor, U.S.A., The 14th Annual IEEE Nonvolatile Semiconductor Memory Workshop, Monterey, CA 8/13-16, 1995
<u>TP</u> AN	"High Density 'AND' Cell Technology for 32Mbit Flash Memory," Hitachi, Japan / Mitsubishi, Japan, The 14th Annual IEEE Nonvolatile Semiconductor Memory Workshop, Monterey, CA 8/13-16, 1995
<u>TP</u> AO	"Effective In-Process Plasma Damage Screening of Tunnel Oxide for Nonvolatile Memory Applications," Motorola, U.S.A., The 14th Annual IEEE Nonvolatile Semiconductor Memory Workshop, Monterey, CA 8/13-16, 1995
<u>TP</u> AP	"Sidewall Sealing Effects on Flash EEPROM," SGS-Thomson, Italy, The 14th Annual IEEE Nonvolatile Semiconductor Memory Workshop, Monterey, CA 8/13-16, 1995

EXAMINER <u>Fong Phan</u>	DATE CONSIDERED <u>6/30/98</u>
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

03/04/98 WED 10:13 FAX 415 576 0300

TOWNSEND SF



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0066

#6
6-30-98
AB

Attorney Docket No. 17822-1-1

POWER OF ATTORNEY BY ASSIGNEE

AZALEA MICROELECTRONICS CORP. is the Assignee of the invention entitled: SERIAL FLASH
MEMORY, the specification of which is attached hereto or X was filed on 9/4/97 as Application Serial No.
08/926,576

Assignee hereby appoints the following attorney(s) and/or agent(s) to prosecute this application and transact
all business in the Patent and Trademark Office connected therewith.

David N. Stone, Reg. No. 28,572
Babak S. Sami, Reg. No. 37,495

RECEIVED
MAY 04 1998

Send Correspondence to:

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, CA 94111-3834

Direct Telephone **GROUP 2100**
(Name, reg. no., tele. no.)
Babak S. Sami
Reg. No. 37,495
(415) 576-0200

AZALEA MICROELECTRONICS CORP.

Date: 3.4.98

By: Ali Pourkeramati
(Signature)

Name: Ali Pourkeramati
Title: President

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TOWNSEND SF



0007

CERTIFICATE UNDER 37 C.F.R. § 3.73(b)

Applicant: Ali Pourkeramati

Application No.: 08/926,576

Filed: 9/4/97

For: SERIAL FLASH MEMORY

Azalca Microelectronics Corp.

a California corporation

(Name of assignee)

(Inventor, partnership, university, government agency, etc.)

certifies that it is the assignee of the entire right, title, and interest in the patent application identified above by virtue of either:

A. ☒ An assignment from the inventor of the patent application identified above. The assignment was recorded in the Patent and Trademark Office at Rec. _____ (Date) _____ or for which a copy thereof is attached.

OR

B. ☐ A chain of title from the inventor(s) of the patent application identified above to the current assignee as shown below:

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GROUP 2100

1. From _____
The document was recorded in the Patent and Trademark Office at Rec. _____ (Date) _____ with a copy thereof is attached.

2. From _____
The document was recorded in the Patent and Trademark Office at Rec. _____ (Date) _____ with a copy thereof is attached.

3. From _____
The document was recorded in the Patent and Trademark Office at Rec. _____ (Date) _____ with a copy thereof is attached.

☐ Additional documents in the chain of title are noted on a supplemental sheet.

☐ Copies of assignments or other documents in the chain of title are attached.

The undersigned has reviewed all the documents in the chain of title of the patent application identified above and, to the best of the undersigned's knowledge and belief, title is in the assignee identified above.

The undersigned (whose title is supplied below) is empowered to act on behalf of the assignee.

I hereby declare that all statements made herein on my own knowledge are true, and that all statements made on information and belief are believed to be true, and declare that these statements are made with the knowledge that willful false statements are punishable by fine or imprisonment, or both, under Section 1001, Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: 3.9.98

Name: Ali Pourkeramati

Title: President

Signature: Ali Pourkeramati

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004

Attorney Docket No. 17822-1-1

ASSIGNMENT OF PATENT APPLICATION

SOLE

WHEREAS, ALI POURKERAMATI of 3979 Brookline Way, Redwood City, CA 94062, hereinafter referred to as "Assignor," is the inventor of the invention described and set forth in the below identified application for United States Letters Patent:

Title of the Invention: **SERIAL FLASH MEMORY**

Date(s) of execution of Declaration: 3-4-98

Filing date: 9/4/97 Application No.: 08/926,576; and

WHEREAS, AZALEA MICROELECTRONICS CORP. a California corporation, located at 3080 Olcott Street, Suite 130-D, Santa Clara, CA 95054, hereinafter referred to as "Assignee," is desirous of acquiring an interest in the invention and application and in any Letters Patent and Registrations which may be granted on the same;

For good and valuable consideration, receipt of which is hereby acknowledged by Assignor, Assignor has assigned, and by these presents does assign to Assignee all right, title and interest in and to the invention and application and to all foreign counterparts (including patent, utility model and industrial designs), and in and to any Letters Patent and Registrations which may hereafter be granted on the same in the United States and all countries throughout the world, and to claim the priority from the application as provided by the Paris Convention. The right, title and interest is to be held and enjoyed by Assignee and Assignee's successors and assigns as fully and exclusively as it would have been held and enjoyed by Assignor had this assignment not been made, for the full term of any Letters Patent and Registrations which may be granted thereon, or of any division, renewal, continuation in whole or in part, substitution, conversion, reissue, prolongation or extension thereof.

Assignor further agrees that Assignor will, without charge to Assignee, but at Assignee's expense, (a) cooperate with Assignee in the prosecution of U.S. Patent applications and foreign counterparts on the invention and any improvements, (b) execute, verify, acknowledge and deliver all such further papers, including patent applications and instruments of transfer and (c) perform such other acts as Assignee lawfully may request to obtain or maintain Letters Patent and Registrations for the invention and improvements in any and all countries, and to vest title thereto in Assignee, or Assignee's successors and assigns.

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IN TESTIMONY WHEREOF, Assignor has signed his/her name on the date indicated.

Date: 3-4-98


ALI POURKERAMATI

STATE OF _____

COUNTY OF _____

On _____, before me, _____,
a Notary Public, personally appeared ALI POURKERAMATI, personally known to me
(or proved to me on the basis of satisfactory evidence) to be the person whose name is
subscribed to the within instrument and acknowledged to me that he/she executed the same
in his/her authorized capacity, and that by his/her signature on the instrument the person,
or the entity upon behalf of which the person acted, executes the instrument.

WITNESS my hand and official seal.

Signature _____ (Seal)

LABSS\SHARE\AZALEAM\IASGN



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
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08/926576

09/04/97

POURKERAMATI

1782211

EXAMINER

ART UNIT PHAN PAPER NUMBER

BABAK S SANI
TOWNSEND AND TOWNSEND AND CREW
TWO EMBARCADERO CENTER 8TH FLOOR
SAN FRANCISCO CA 94111

DATE MAILED: 2818

06/29/98

This is in response to the Power of Attorney filed

03/13/98

- ☐ 1. The Power of Attorney to you in this application **has been revoked** by the applicant. Future correspondence will be mailed to the new address of record. 37 CFR 1.33.
- ☐ 2. The Power of Attorney to you in this application **has been revoked** by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record. (37 CFR 1.33).
- ☐ 3. The withdrawal as attorney in this application **has been accepted**. Future correspondence will be mailed to the new address of record. 37 CFR 1.33.

Disha Bailey
This is a communication from the
Patent and Trademark Office

- ☒ 4. The Power of Attorney in this application **is accepted**. Correspondence in this application will be mailed to the below-noted address as provided by 37 CFR 1.33.
- ☐ 5. The Power of Attorney in this application **is not accepted** for the reason(s) checked below:
- ☐ a. The Power of Attorney is from an assignee and the Certificate required by 37 CFR 3.73 (b) has not been received.
- ☐ b. The person signing for the assignee has omitted their empowerment to sign on behalf of the assignee.
- ☐ c. The inventor(s) is without authority to appoint attorneys since the assignee has intervened as provided by 37 CFR 3.71.
- ☐ d. The signature of _____, a co-inventor in this application, has been omitted. The Power of Attorney will be entered upon receipt of confirmation signed by said co-inventor.
- ☐ e. The person(s) appointed in the Power of Attorney is not registered to practice before the U.S. Patent & Trademark Office.
- ☐ f. The revocation is not signed by the applicant, the assignee of the entire interest, or **one** particular principal attorney having the authority to revoke.

BABAK S. SANI
TOWNSEND AND TOWNSEND AND CREW
TWO EMBARCADERO CENTER 8TH FLOOR
SAN FRANCISCO CA 94111

Disha Bailey
This is a communication from the
Patent and Trademark Office

RETAIN THIS COPY IN THE APPLICATION FILE COPY A



**UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office**

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/926,576	09/04/97	POURKERAMATI	A 1782211

MM11/0702
BABAK S. SANI
TOWNSEND AND TOWNSEND AND CREW
TWO EMBARCADERO CENTER 8TH FLOOR
SAN FRANCISCO CA 94111


EXAMINER
PHAN, T

ART UNIT 2818	PAPER NUMBER 8
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DATE MAILED: 07/02/98

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 08/926,576	Applicant(s) ALI POURKERAMATI	
	Examiner Trong Phan	Group Art Unit 2818	

☒ Responsive to communication(s) filed on Sep 4, 1997

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire one (1) month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) 1-10 is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☐ Claim(s) _____ is/are rejected.

☐ Claim(s) _____ is/are objected to.

☒ Claims 1-10 are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 8

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

Serial Number: 08/926,576

Page 2

Art Unit: 2818

Election/Restriction

1. Restriction to one of the following inventions is required

under 35 U.S.C. 121:

I. Claims 1-7, drawn to the array of flash memory cell having tunnel window, classified in class 365, subclass 185.26.

II. Claims 8-10, drawn to the array of flash memory cell operating in programming, erase and read modes, classified in class 365, subclass 185.33.

2. The inventions are distinct, each from the other because of the following reasons: Inventions I and II are unrelated. Inventions are unrelated if it can be shown that they are not disclosed as capable of use together, or they have different modes of operation, or they have different functions, or they have different effects. (MPEP § 806.04, MPEP § 808.01). In the instant case, the flash memory cell having tunnel window in the invention of Group I is not disclosed as capable of use together with the array of flash memory cell in the invention of Group II, therefore, they have different modes of operation, different functions, and different effects.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

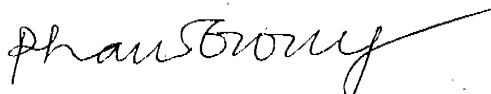
Serial Number: 08/926,576

Page 3

Art Unit: 2818

4. Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trong Phan whose telephone number is (703) 308-4870.

A handwritten signature in cursive script, appearing to read "Trong Phan", with a long horizontal stroke extending to the right.

June 30, 1998

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on 7-30-98

TOWNSEND and TOWNSEND and CREW LLP

By [Signature]



CAV 2818
L. Spruell
8-11-98

PATENT

Attorney Docket No. 17822-1-1

9/
Election

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:)	
ALI POURKERMATI)	Examiner: Pourkeramati
Application No.: 08/926,576)	Art Unit: 2818
Filed: 9/4/97)	RESPONSE TO RESTRICTION
For: SERIAL FLASH MEMORY)	<u>REQUIREMENT</u>

Assistant Commissioner for Patents
Washington, D.C. 20231

RECEIVED

AUG 06 1998

Sir:

In response to the restriction requirement mailed July 2, 1998, applicant elects for prosecution Group 1 claims 1-7.

GROUP 2500

Respectfully submitted,

[Signature]
Babak S. Sani
Reg. No. 37,495

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
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**UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office**

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/926,576	09/04/97	POURKERAMATI	A 1782211

MM11/0825
BABAK S. SANI
TOWNSEND AND TOWNSEND AND CREW
TWO EMBARCADERO CENTER 8TH FLOOR
SAN FRANCISCO CA 94111

EXAMINER

PHAN, T

ART UNIT


2818

PAPER NUMBER

DATE MAILED: 08/25/98

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 08/926,576	Applicant(s) ALI POURKERAMATI	
	Examiner Trong Phan	Group Art Unit 2818	

☒ Responsive to communication(s) filed on Aug 3, 1998

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire three (3) month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) 1-10 is/are pending in the application.

Of the above, claim(s) 8-10 is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-7 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

Application/Control Number: 08/926,576

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Drawings

1. The drawings are objected to because Fig. 2 should be labeled as Fig. 3 in order to be consistent with the disclosure. Correction is required.
2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the feature "said window has no sides abutting said field dielectric layer" as recited in claim 3 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.
3. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee, 4,924,119, in view of Hong, 5,460,991.

Lee, 4,924,119, discloses in Fig. 1 an EEPROM cell comprising:

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source region 18 and drain region 19;

floating gate of polysilicon 15;

tunnel window 23 being located on the side of drain region 19 and abutting a thin layer of oxide (see lines 23-27, column 3);

control gate 18 of polysilicon;

dielectric layer between floating gate of polysilicon 15 and control gate of polysilicon 18.

What is not shown in Fig. 1 of Lee, 4,924,119, is the dielectric film comprising a layer of nitride sandwiched between the first and second silicon dioxide layers as recited in claim 5.

Hong, 5,460,991, discloses in Fig. 7 an EEPROM cell having an inter-polysilicon dielectric layer 12 of ONO (oxide-nitride-oxide) (see lines 50-52, column 3).

It would have been obvious under 35 U.S.C. 103(a) to one of ordinary skilled in the art at the time of the invention was made to utilize the inter-polysilicon dielectric layer 12 of ONO (oxide-nitride-oxide) in Fig. 7 of Hong, 5,460,991, for the dielectric layer in Fig. 1 of Lee, 4,924,119, for the purpose of having a good insulating layer.

What is not shown in Fig. 1 of Lee, 4,924,119, is the control gate comprising a polycide layer on top of the polysilicon layer as recited in claim 6.

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Hong, 5,460,991, discloses in Fig. 8 an EEPROM cell having control gate 13 comprising a polycide layer disposed over polysilicon layer (see lines 6-8, column 4).

It would have been obvious under 35 U.S.C. 103(a) to one of ordinary skilled in the art at the time of the invention to utilize the control gate 13 in Fig. 8 of Hong, 5,460,991, for the control gate 18 in Fig. 1 of Lee, 4,924,119, for the purpose of having a good control gate.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al., 5,734,609, in view of Lee, 4,924,119.

Choi et al., 5,734,609, discloses in Fig. 4 Prior Art a flash EEPROM device comprising:

a plurality of series-connected EEPROM cells C1-Cn and C1'-Cn';

bit line select transistors S1 and S1';

source line transistors S2 and S2'.

What is not shown in Fig. 4 Prior Art of Choi et al., 5,734,609, is the specific structure of the memory cell.

Lee, 4,924,119, discloses in Fig. 1 an EEPROM cell comprising:

source region 18 and drain region 19;

floating gate of polysilicon 15;

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tunnel window 23 being located on the side of drain region 19 and abutting a thin layer of oxide (see lines 23-27, column 3);

control gate 18 of polysilicon;

dielectric layer between floating gate of polysilicon 15 and control gate of polysilicon 18.

It would have been obvious under 35 U.S.C. 103(a) to one of ordinary skilled in the art at the time of the invention to utilize the EEPROM cell in Fig. 1 of Lee, 4,924,119, for each of the EEPROM cells in Fig. 4 Prior Art of Choi et al., 5,734,609, for the purpose of providing EEPROM cells having the V_t of the transistor that can be shifted to a value of approximately 10 volts (see lines 27-34, column 3 of Lee, 4,924,119).

7. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsia et al., 4,894,802, in view of Hong, 5,460,991.

Hsia et al., 4,894,802, discloses in Fig. 3b an EEPROM cell comprising:
source region 22 and drain region 21;
floating polysilicon layer 17;
field oxide 19 (see line 40, column 4);
tunnel window 27 being located on the side of drain region 21 and abutting field oxide 19;
control gate 18 of polycrystalline silicon (see lines 55-58, column 6);

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dielectric layer 29 of interpoly oxide (see lines 9-10, column 5).

What is not shown in Fig. 3b of Hsia et al., 4,894,802, is the dielectric film comprising a layer of nitride sandwiched between the first and second silicon dioxide layers as recited in claim 5.

Hong, 5,460,991, discloses in Fig. 7 an EEPROM cell having an inter-polysilicon dielectric layer 12 of ONO (oxide-nitride-oxide) (see lines 50-52, column 3).

It would have been obvious under 35 U.S.C. 103(a) to one of ordinary skilled in the art at the time of the invention was made to utilize the inter-polysilicon dielectric layer 12 of ONO (oxide-nitride-oxide) in Fig. 7 of Hong, 5,460,991, for the dielectric layer 29 of interpoly oxide in Fig. 3b of Hsia, 4,894,802, for the purpose of having a good insulating layer.

What is not shown in Fig. 3b of Hsia, 4,894,802, is the control gate comprising a polycide layer on top of the polysilicon layer as recited in claim 6.

Hong, 5,460,991, discloses in Fig. 8 an EEPROM cell having control gate 13 comprising a polycide layer disposed over polysilicon layer (see lines 6-8, column 4).

It would have been obvious under 35 U.S.C. 103(a) to one of ordinary skilled in the art at the time of the invention to utilize the control gate 13 in Fig. 8

Art Unit: 2818

of Hong, 5,460,991, for the control gate 18 in Fig. 3b of Hsia et al., 4,894,802, for the purpose of having a good control gate.

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al., 5,734,609, in view of Hsia et al., 4,894,802.

Choi et al., 5,734,609, discloses in Fig. 4 Prior Art a flash EEPROM device comprising:

a plurality of series-connected EEPROM cells C1-Cn and C1'-Cn';

bit line select transistors S1 and S1';

source-line transistors S2 and S2'.

What is not shown in Fig. 4 Prior Art of Choi et al., 5,734,609, is the specific structure of the memory cell.

Hsia et al., 4,894,802, discloses in Fig. 3b an EEPROM cell comprising:

source region 22 and drain region 21;

floating polysilicon layer 17;

field oxide 19 (see line 40, column 4);

tunnel window 27 being located on the side of drain region 21 and abutting field oxide 19;

control gate 18 of polycrystalline silicon (see lines 55-58, column 6);

dielectric layer 29 of interpoly oxide (see lines 9-10, column 5).

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Page 8

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It would have been obvious under 35 U.S.C. 103(a) to one of ordinary skilled in the art at the time of the invention to utilize the EEPROM cell in Fig. 3b of Hsia et al., 4,894,802, for each of the EEPROM cells in Fig. 4 Prior Art of Choi et al., 5,734,609, for the purpose of providing EEPROM cells having improved programming efficiency and improved program/erase endurance (see lines 9-11, column 3 of Hsia et al., 4,894,802).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See Gill et al., 5,008,721, Kaya et al., 5,216,270, and Chang, 5,666,307, generally, for the Flash EEPROM cell.

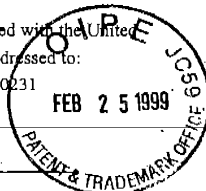
10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trong Phan whose telephone number is (703) 308-4870.

Phan Trong

August 19, 1998

Notice of References Cited		Application No. 08/926,576	Applicant(s) ALI POURKERAMATI			
		Examiner Trong Phan	Group Art Unit 2818	Page 1 of 1		
U.S. PATENT DOCUMENTS						
		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS
	A	4,894,402	Jan. 1990	Heia et al.	257	321
	B	4,924,119	May 1990	Lee	257	321
	C	5,008,721	Apr. 1991	Gill et al.	365	185.33
	D	5,216,270	Jun. 1993	Kaya et al.	257	321
	E	5,460,991	Oct. 1995	Hong	438	261
	F	5,666,307	Sep. 1997	Chang	365	185.33
	G	5,734,609	Mar. 1998	Choi et al.	365	185.17
	H					
	I					
	J					
	K					
	L					
	M					
FOREIGN PATENT DOCUMENTS						
		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS
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	P					
	Q					
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	S					
	T					
NON-PATENT DOCUMENTS						
		DOCUMENT (Including Author, Title, Source, and Pertinent Pages)				DATE
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	V					
	W					
	X					

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:
Assistant Commissioner for Patents Washington, D.C. 20231
on 2-22-99



PATENT
Attorney Docket No.: 17822-1-1US

By: [Signature]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

ALI POURKERMATI

Application No.: 08/926,576

Filed: September 4, 1997

For: SERIAL FLASH MEMORY

Examiner: T. Chan

Art Unit: 2818

PETITION TO EXTEND TIME

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Applicant petitions the Assistant Commissioner of Patents to extend the time for response to the Office Action dated August 25, 1998 for three months, from November 25, 1998 to February 25, 1999. An appropriate response in the form of an amendment is enclosed herewith.

Please charge the fee of \$475 to the undersigned's Deposit Account No. 20-1430. Please charge any additional fees or credit overpayment to the above deposit account. This petition is submitted in triplicate.

Respectfully submitted,

Babak S. Sani
Reg. No. 37,495

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TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: (415) 576-0200 / Fax: (415) 576-0300
BSS:db SF 150963 v1

GP. 2818\$

Amendment

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
(415) 576-0200

Attorney Docket No. 17822-1-IUS

In re application of: ALI POURKERMATI

Date: February 22, 1999

Application No.: 08/926,576

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Filed: Sep 04, 1997

Assistant Commissioner for Patents
Washington, D.C. 20231

Group Art Unit: 2818

For: SERIAL FLASH MEMORY

Date: 2-22-99
JL Gullet

THE ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

Sir:

Transmitted herewith is an amendment in the above-identified application.

- [X] Enclosed is a petition to extend time to respond.
[X] Small entity status of this application under 37 CFR 1.9 and 1.27 has been established by a verified statement previously submitted.
[X] Three sheets of proposed drawing amendments are enclosed.

If any extension of time is needed, then this response should be considered a petition therefor.
The filing fee has been calculated as shown below:

	(Col. 1)		(Col. 2)		(Col. 3)
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NO. PREVIOUSLY PAID FOR		PRESENT EXTRA
TOTAL	13 * 10	MINUS	** 20	=	0
INDEP.	5 * 2	MINUS	*** 4	=	10
[] FIRST PRESENTATION OF MULTIPLE DEP. CLAIM					

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDIT. FEE		RATE	ADDIT. FEE
x \$9.00 =	\$0.00	OR	x \$18.00 =	
x \$39.00 =	\$0.00		x \$78.00 =	
+ \$130.00 =			+ \$260.00 =	
TOTAL ADDIT. FEE	\$0.00	OR	TOTAL	

- * If the entry in Col. 1 is less than the entry in Col. 2, write "0" in Col. 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, write "20" in this space.
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, then write "3" in this space. The "Highest Number Previously Paid For" (Total or Independent) is the highest number found from the equivalent box in Col. 1 of a prior amendment or the number of claims originally filed.

[X] No fee is due.

Please charge Deposit Account No. 20-1430 as follows:

[] Claims fee \$
[X] Any additional fees associated with this paper or during the pendency of this application.

no extra copies of this sheet are enclosed.

TOWNSEND and TOWNSEND and CREW LLP

Babak S. Sani, Reg. No.: 37,495
Attorneys for Applicant

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PATENT
Attorney Docket No.: 17822-1-1US

Assistant Commissioner for Patents
Washington, D.C. 20231



Smiles
#12/a
3/5/99

On 2-22-99

TOWNSEND and TOWNSEND and CREW LLP

By: *dl Sullivan*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

ALI POURKERMATI

Application No.: 08/926,576 ✓

Filed: September 4, 1997 ✓

For: SERIAL FLASH MEMORY ✓

Examiner: T. Phan

Art Unit: 2818

AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action mailed August 25, 1998, please amend the above-identified application as follows:

IN THE DRAWINGS:

To bring the labeling of the figures in conformity with the specification, the legend "FIG. 2" has been changed to -- FIG. 3 --. Further, Figures 2B and 2C have been amended to replace the reference numeral "23" with -- 23B --, and add new reference numerals -- 28A -- and -- 28B -- to clearly identify field oxide edges of the memory cell. Figure 4 has been amended to replace the continuous line that connects the memory cells between WL1 and WL15 with a dotted line to more accurately depict the invention. Submitted herewith are substitute drawings for Figures 3, 2B, 2C, and 4 which show the proposed corrections in red

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ink. Applicant respectfully requests deferral of submission of formal drawings until allowable subject matter is indicated.

IN THE SPECIFICATION:

Please amend the specification as follows:

At page 6, line 21, replace “the field oxide (not shown)” with -- field oxide edges 28A and 28B, --.

At page 6 line 23, replace “the field edges” with -- field edges 28A and 28B--.

At page 8, line 3, replace “36” with -- 26 --.

IN THE CLAIMS:

Please amend claim 1, and add new claims 8-10 as follows:

91

- | | |
|----|---|
| 1 | 1. (Once Amended) A memory cell comprising: |
| 2 | a source region and a drain region forming a channel therebetween; |
| 3 | a channel dielectric layer disposed on top of said channel; |
| 4 | a floating polysilicon layer disposed on top of, <u>and substantially covering an</u> |
| 5 | <u>area defined by,</u> said channel dielectric layer, said floating polysilicon layer and channel |
| 6 | dielectric layer defining a <u>tunnel</u> window within an area of said channel wherein a thickness of |
| 7 | said channel dielectric layer in said <u>tunnel</u> window is smaller than that of a remaining portion |
| 8 | of said channel dielectric layer; and |
| 9 | a control gate layer disposed on top of and separated from said floating gate |
| 10 | layer by a dielectric film, |
| 11 | wherein an etch step that defines edges of said floating |
| 12 | polysilicon layer is performed such that one edge of said tunnel window is [located on a drain |
| 13 | side of said channel] <u>defined by an edge of said floating polysilicon layer located substantially</u> |
| 14 | <u>at a channel-drain junction.</u> |

1 ^{7H}
2 ~~8~~. (New) The memory cell of claim 1 wherein a window mask used during
3 manufacturing of the memory cell is larger than said tunnel window, and includes a portion
that overlaps said drain region.

1 ^{8H}
2 ^{7H}
3 ~~9~~. (New) The memory cell of claim ~~8~~ wherein said etch step removes said
4 portion of said window that overlaps said drain region.

1 ^{10H}
2 ~~10~~. (New) A flash memory cell comprising:
3 a source region and a drain region forming a channel therebetween;
4 a channel oxide layer formed on top of said channel, said channel oxide layer
5 having a first portion with a first thickness and a tunnel window portion on a side of said drain
6 region, having a second thickness less than said first thickness;
7 a floating polysilicon layer formed on top of said channel oxide layer;
8 a dielectric oxide-nitride-oxide sandwich layer formed on top of said floating
9 polysilicon layer; and
10 a gate polysilicon layer formed on top of said dielectric oxide-nitride-oxide
11 sandwich layer,
12 wherein, said tunnel window portion of said channel oxide layer
13 is initially formed inside a window overlapping said drain region, and then etched back to an
edge of said floating polysilicon layer.

REMARKS

Upon entry of this amendment which amends claim 1 and adds new claims 8-10, claims 1-10 remain pending. Previously examined claims 1-6 were rejected under 35 U.S.C. §103(a) as being unpatentable over Lee '119 in view of Hong '991, as well as over Hsia '802 in view of Hong '991, and claim 7 was rejected under 35 U.S.C. §103(a) as being unpatentable over Choi '609 in view of Lee '119, as well as over Choi '609 in view of Hsia

"802. Reconsideration of the claims in view of the above amendments and the comments below is respectfully requested.

Objections

The drawings were objected to for mislabeling FIG. 3 as FIG. 2, and for failing to show a claimed aspect of the present invention. Figure 3 has been amended replacing the legend "FIG. 2" with FIG. 3 to bring it in conformity with the specification. Further, reference numerals 28A and 28B have been added to Figures 2A and 2B as well as to the relevant parts of the specification to clearly identify the edges of the filed oxide around the memory cell. It is respectfully submitted that no new matter has been added by this amendment as should be clear from the nature of the changes to the specification. Withdrawal of the objections in light of these amendments is respectfully requested.

Rejections

- Section 103(a): Lee '119 in view of Hong '991

Claims 1-6 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Lee '119 in view of Hong '991. The rejection states that Lee '119 in Figure 1 discloses a memory cell with all of the limitations set forth in claim 1, and that Hong '991 suggest the limitations recited in the remaining dependent claims.

It is respectfully submitted that the memory cell shown in Figure 1 of Lee '119 differs from the claimed memory cell of the present invention in at least one significant respect. As clearly shown in Figure 1 of Lee '119, the tunnel window (23) is formed "close to the drain 19" (col. 3, line 25), but is neither at the channel-drain junction, nor does it abut the edge of floating poly 15. That is, tunnel window 23 is formed wholly within the channel region such that the sidewalls of the tunnel must be defined by the tunnel window itself.

In contrast to the Lee '119 memory cell, the memory cell of the present invention as claimed has a tunnel window that has an edge defined by the edge of the floating polysilicon layer located at the drain-channel junction. Claim 1 has been amended to highlight

this distinguishing feature of the present invention. As amended, claim 1 recites a memory cell “wherein an etch step that defines edges of [the] floating polysilicon layer is performed such that one edge of [the] tunnel window is defined by an edge of [the] floating polysilicon layer located substantially at a channel-drain junction.” This aspect of the invention is described in the specification, for example, at page 6, lines 9-16, and at page 9, lines 12-14. Lee ‘119 as well as the other cited references, or any combination thereof, fail to teach such a combination with the claimed structure for a tunnel window. This distinguishing feature is significant and non-obvious for a number of reasons. The performance of the memory cell (capacitive coupling ratio) is highly dependent on the size of the tunnel window, which is often required to be at minimum process feature size. The tunnel window mask is therefore often a critical mask. The memory cell of Lee ‘119 requires the tunnel window to be defined entirely by the window mask and thus demands a high resolution process to accurately implement the tunnel window. This places severe demands on the manufacturing process when it is scaled down to lower dimensions.

The boundaries of the tunnel window according to the memory cell of the present invention, in contrast, are not wholly defined by the window mask. Referring to Figure 2A of the instant application, there is shown the initial window (23) that overlaps the channel region (26) as well as the drain region (21). After the tunnel oxide and the overlying floating polysilicon layer are formed, the floating poly layer is patterned and etched along with the overlapping portion (23B) of the tunnel oxide (e.g., see specification, page 9, lines 12-14). Since the area of the actual tunnel window of the memory cell of the present invention does not correspond to the tunnel window mask, the present invention provides a significant degree of flexibility in manufacturability of the cell.

Lee ‘119 therefore clearly fails to teach or suggest a tunnel window whose one edge is defined by the etch step that etches the floating polysilicon layer. Claim 1 as amended is therefore clearly distinguished over the cited references. Claims 2-9 depend from claim 1 and thus derive patentability therefrom. These claims, however, recite additional novel and non-obvious features that further distinguish over the cited prior art. Claims 3 and 4, for

example, define alternative embodiments wherein the window either abuts field oxide or it does not. The rejection does not point to any part of the cited reference as suggesting these variations because Lee '119 does not teach or suggest such a structure one way or the other. Furthermore, newly added claims 8 and 9 expressly recite a tunnel window mask that is larger than the actual tunnel window and that the floating poly etch step defines one edge of the tunnel window. No such structure is taught or suggested by any combination of the cited references. Claims 1-6 are therefore clearly distinguished over the combination of Lee '119 and Hng '991. Withdrawal of this rejection is respectfully requested.

- Section 103(a): Choi '609 over Lee '119

Claim 7 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Choi '609 in view of Lee '119. Claim 7 depends from claim 1 and therefore derives patentability therefrom. As explained above, amended claim 1 is patentably distinguished over the teachings of Lee '119. Claim 7 depending from claim 1, therefore is patentably distinguished for at least the same reasons as above. Withdrawal of this rejection is respectfully requested.

- Section 103(a): Hsai '802 over Hong '991

Claims 1-6 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Hsia '802 in view of Hong '991. The rejection states that Hsai '802 in Figure 3b discloses a memory cell with all of the limitations set forth in claim 1, and that Hong '991 suggest the limitations recited in the remaining dependent claims.

It is respectfully submitted that Hsia '802 discloses in Figures 3a and 3b what is known by those skilled in this art as a "split-gate" memory cell. This renders the Hsia '802 memory cell quite different from the claimed memory cell of the present invention in a number of respects. First, according to the split gate Hsia '802 memory cell there are portions of the channel oxide that are covered by the gate poly (18 in Figure 3a) and other portions that are covered by the floating poly (17 in Figure 3a). This is the definition of a split gate cell and is clearly demonstrated in Figures 3, and 3a.

In contrast to the Hsia '802 memory cell, the memory cell of the present invention is not of split gate type. Claim 1 has been amended to highlight this aspect of the present invention. Amended claim 1 recites "a floating polysilicon layer disposed on top of, and substantially covering an area defined by, said channel dielectric layer," This clearly distinguished claim 1 from Hsia, which teaches a memory cell with a control gate (18) that "extends above source region 22 ... in order to achieve split gate operation." [Col. 4, lines 45-53]. Furthermore, similar to the tunnel window in the Lee '119 memory cell, the tunnel window in Hsia '802 is wholly defined by the tunnel window mask (26 in Fig. 3), and is not etched back to the channel-drain junction. Amended claim 1 is thus further distinguished as it recites an edge of the tunnel window being "located substantially at a channel-drain junction."

Claim 1 as amended is thus patentably distinguished over Hsia '802 based at least on these two differentiating features. Claims 2-10 depend from claim 1 and thus derive patentability therefrom. These claims, however, recite additional non-obvious and novel features that further distinguish over the cited art. Claims 3 and 4, for example, define alternative embodiments wherein the window either abuts field oxide or it does not. Field oxide is defined as "substantially surrounding first and second sides of [the] channel." The only thick oxide (19 in Fig. 3b) shown by Hsia '802 extends under the channel abutting the tunnel window. The memory cell of the present invention, in contrast, does not include any filed oxide under the channel (i.e., between the source-drain regions), and instead surrounds the channel as claimed. Furthermore, newly added claims 8 and 9 expressly recite a tunnel window mask that is larger than the actual tunnel window and that the floating poly etch step defines one edge of the tunnel window. No such structure is taught or suggested by any combination of the cited references. Claims 1-6 are therefore clearly distinguished over the combination of Hsia '802 and Hng '991. Withdrawal of this rejection is respectfully requested.

- Section 103(a): Choi '609 over Hsia '802

Claim 7 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Choi '609 in view of Hsia '802. Claim 7 depends from claim 1 and therefore derives

ALI POURKERMATI
Application No.: 08/926,576
Page 8

PATENT

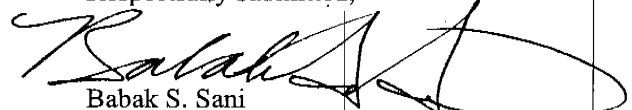
patentability therefrom. As explained above, amended claim 1 is patentably distinguished over the teachings of Hsia '802. Claim 7 depending from claim 1, therefore is patentably distinguished for at least the same reasons as above. Withdrawal of this rejection is respectfully requested.

CONCLUSION

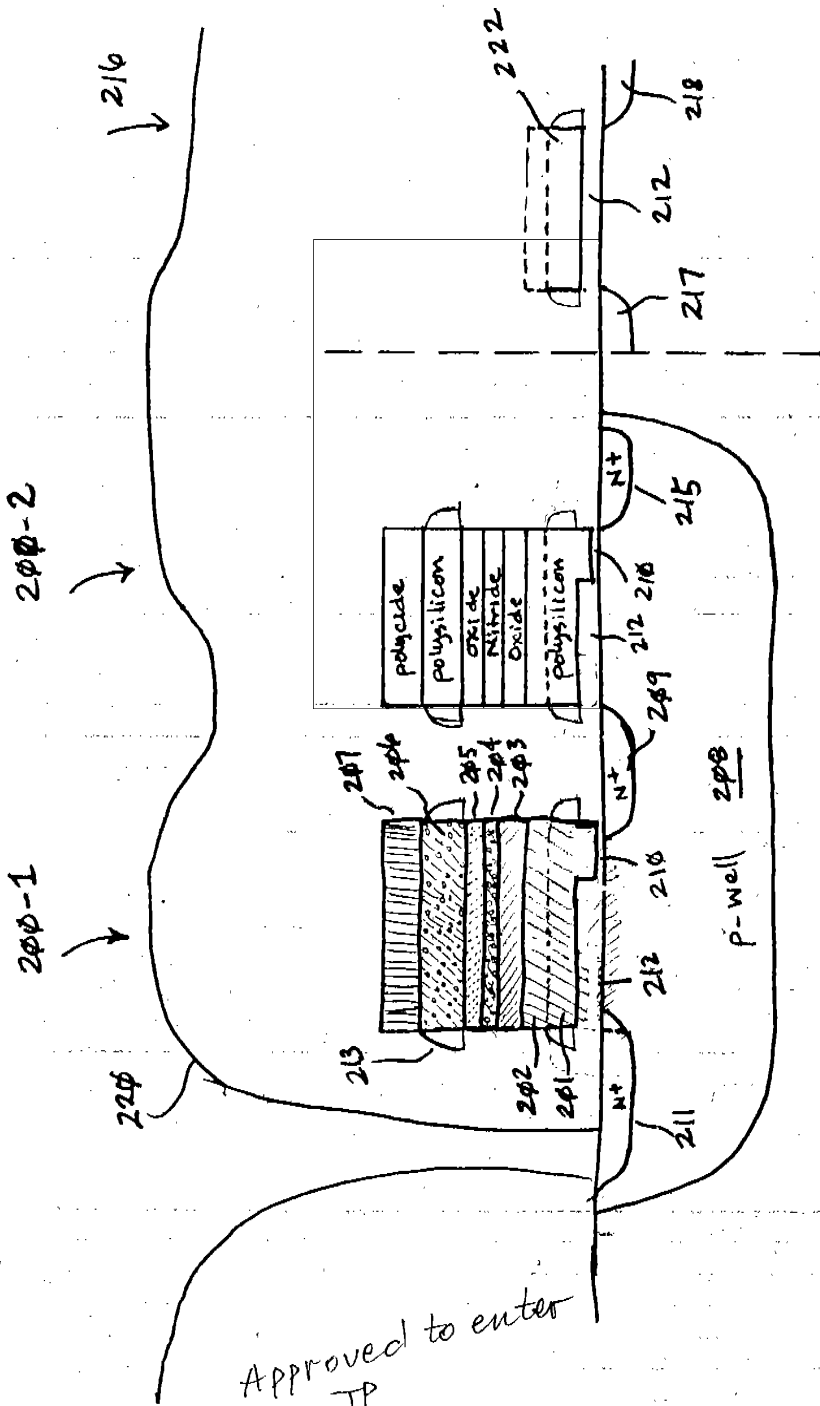
In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,


Babak S. Sani
Reg. No. 37,495

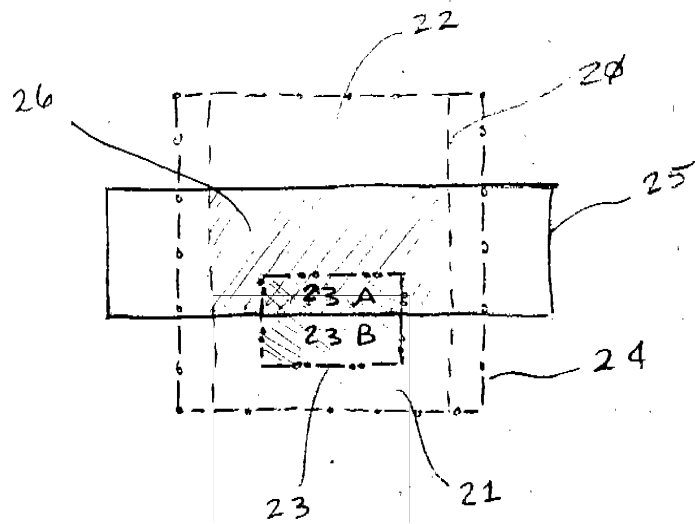
TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: (415) 576-0200
Fax: (415) 576-0300
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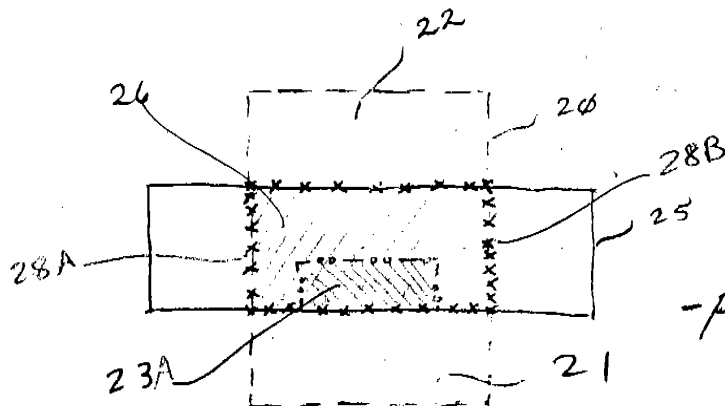
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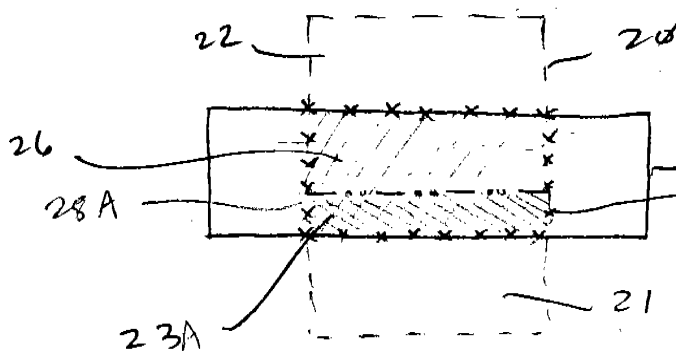
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-FIG. 2-



- FIG. 2A -



- FIG. 2B -



- FIG. 2C -



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY/DOCKET NO.
087326,576	09/04/97	BOURKE, RICHARD A.	

MM11/0315
BABAK S. SANI
TOWNSEND AND TOWNSEND AND CREW
TWO EMBARCADERO CENTER 8TH FLOOR
SAN FRANCISCO CA 94111

PHAN, T. EXAMINER


ART UNIT	PAPER NUMBER
2100	

03/15/99
DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Notice of Allowability	Application No.	Applicant(s)
	08/926,576	ALI POURKERAMATI
	Examiner	Group Art Unit
	TRONG PHAN	2818



All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance and Issue Fee Due or other appropriate communication will be mailed in due course.

☒ This communication is responsive to 2/25/99

☒ The allowed claim(s) is/are 1-7 and 11-13

☐ The drawings filed on _____ are acceptable.

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All. ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

A SHORTENED STATUTORY PERIOD FOR RESPONSE to comply with the requirements noted below is set to EXPIRE **THREE MONTHS** FROM THE "DATE MAILED" of this Office action. Failure to timely comply will result in ABANDONMENT of this application. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.

☒ Applicant MUST submit NEW FORMAL DRAWINGS

☐ because the originally filed drawings were declared by applicant to be informal.

☐ including changes required by the Notice of Draftsperson's Patent Drawing Review, PTO-948, attached hereto or to Paper No. _____

☒ including changes required by the proposed drawing correction filed on 2/25/99, which has been approved by the examiner.

☐ including changes required by the attached Examiner's Amendment/Comment.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the reverse side of the drawings. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

☐ Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Any response to this letter should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included.

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

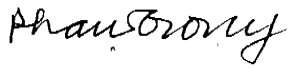
☐ Notice of Informal Patent Application, PTO-152

☐ Interview Summary, PTO-413

☒ Examiner's Amendment/Comment

☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material

☒ Examiner's Statement of Reasons for Allowance



TRONG PHAN
PATENT EXAMINER
ART UNIT 2818

Application/Control Number: 08/926,576

Page 2

Art Unit: 2818

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. The application has been amended as follows:

In the specification, line 1 of page 1, the sentence ~~---This application claims the benefit of U.S. Provisional Application No. 60/025,698, filed September 9, 1996, the disclosure of which is incorporated by reference---~~ has been inserted.

Claim 7, line 14, the word "lien" has been changed to ~~---line---~~.

Non-elected claims 8-10 have been canceled.

Newly added claims 8-10 have been changed to claims 11-13.

All above changes have been made by the examiner in order to place the case in condition for allowance.

3. The following is an examiner's statement of reasons for allowance:

The memory cell having one edge of the tunnel window being defined by an edge of the floating polysilicon layer located substantially at a channel-drain junction as recited in claims 1-7 and 11-13 has not been found in the prior art references.

Application/Control Number: 08/926,576

Page 3

Art Unit: 2818

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trong Phan whose telephone number is (703) 308-4870.

Phan Trong

Trong Phan
Patent Examiner
Art Unit 2818

March 14, 1999

Notice of References Cited				Application No. 08/926,578		Applicant(s) ALI POURKERAMATI	
				Examiner TRONG PHAN		Group Art Unit 2818	
Page 1 of 1							
U.S. PATENT DOCUMENTS							
*		DOCUMENT NO.	DATE	NAME		CLASS	SUBCLASS
x	A	5,838,616	11/98	Randazzo		365	185.20
	B						
	C						
	D						
	E						
	F						
	G						
	H						
	I						
	J						
	K						
	L						
	M						
FOREIGN PATENT DOCUMENTS							
*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUBCLASS
	N						
	O						
	P						
	Q						
	R						
	S						
	T						
NON-PATENT DOCUMENTS							
*		DOCUMENT (Including Author, Title, Source, and Pertinent Pages)					DATE
	U						
	V						
	W						
	X						

Trong Phan 3/14/99

* A copy of this reference is not being furnished with this Office action.
(See Manual of Patent Examining Procedure, Section 707.05(a).)



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

NOTICE OF ALLOWANCE AND ISSUE FEE DUE

PM111/0315

BARAK S. SANI
TOWNSEND AND TOWNSEND AND CREW
TWO EMBARCADERO CENTER 8TH FLOOR
SAN FRANCISCO CA 94111

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
09/926,576	09/04/97	010	PHAN, T 2818	03/15/99
First Named Applicant	POURKERAMATI, 35 USC 154(b) term ext. = 0 Days.			

TITLE OF INVENTION SERIAL FLASH MEMORY

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
2 1782211	365-165,260	030	UTILITY	NO	\$1210.00	06/15/99

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.

HOW TO RESPOND TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.
If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

- If the status is changed, pay twice the amount of the FEE DUE shown above and notify the Patent and Trademark Office of the change in status, or
- If the status is the same, pay the FEE DUE shown above.

If the SMALL ENTITY is shown as NO:

- Pay FEE DUE shown above, or
- File verified statement of Small Entity Status before, or with, payment of 1/2 the FEE DUE shown above.

- Part B-Issue Fee Transmittal should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B Issue Fee Transmittal should be completed and returned. If you are charging the ISSUE FEE to your deposit account, section "4b" of Part B-Issue Fee Transmittal should be completed and an extra copy of the form should be submitted.
- All communications regarding this application must give application number and batch number. Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

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PTOL-85 (REV. 10-96) Approved for use through 06/30/99. (0851-0033)



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Corrected
NOTICE OF ALLOWANCE AND ISSUE FEE DUE

MM11/0323

BABAK S. SANI
TOWNSEND AND TOWNSEND AND CREW
TWO EMBARCADERO CENTER 8TH FLOOR
SAN FRANCISCO CA 94111

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
08/926,576	09/04/97	010	PHAN, T 2818	03/15/99
First Named Applicant: POURKERAMATI, ALI				
TITLE OF INVENTION: SERIAL FLASH MEMORY				

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
2 1782211	365-185.260	030	UTILITY	YES	\$605.00	06/15/99

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.

HOW TO RESPOND TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.
If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

- If the status is changed, pay twice the amount of the FEE DUE shown above and notify the Patent and Trademark Office of the change in status, or
- If the status is the same, pay the FEE DUE shown above.

If the SMALL ENTITY is shown as NO:

- Pay FEE DUE shown above, or
- File verified statement of Small Entity Status before, or with, payment of 1/2 the FEE DUE shown above.

II. Part B-Issue Fee Transmittal should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B Issue Fee Transmittal should be completed and returned. If you are charging the ISSUE FEE to your deposit account, section "4b" of Part B-Issue Fee Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give application number and batch number.
Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

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760 4100
199
019 4-2-42 7310 # 64
26



I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: PATENT
Box Issue Fee Attorney Docket No.: 17822-000110

Assistant Commissioner for Patents,
Washington, D.C. 20231, on May 18, 1999
TOWNSEND and TOWNSEND and CREW LLP
By Sherry Barton

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

ALI POURKERAMATI

Serial No.: 08/926,576

Filed: September 4, 1997

For: SERIAL FLASH MEMORY

Examiner: Trong Phan

Art Unit: 2818

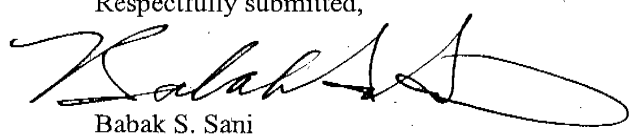
Batch No.: Q30

LETTER TO OFFICIAL DRAFTSPERSON

Box Issue Fee
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Pursuant to the Notice of Allowability dated March 15, 1999, applicant submits four sheets of formal drawings to be made of record in the above-identified case.

Respectfully submitted,

Babak S. Sani
Reg. No. 37,495

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
(415) 576-0200
Fax (415) 576-0300
BSS/sb
SF 220191 v1

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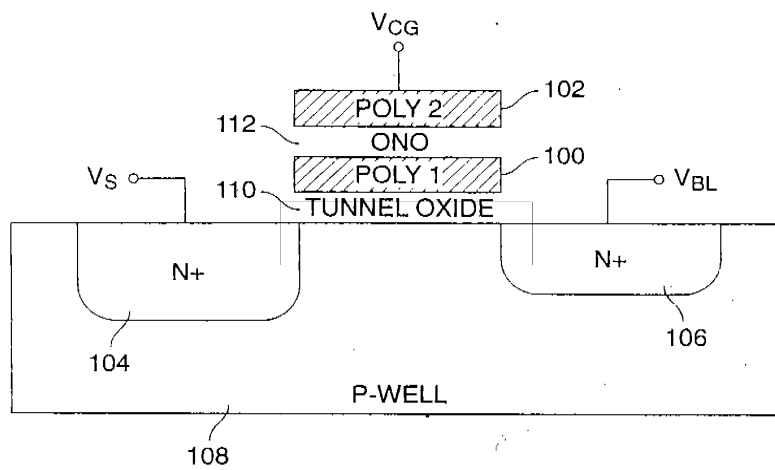


FIG. 1
(PRIOR ART)

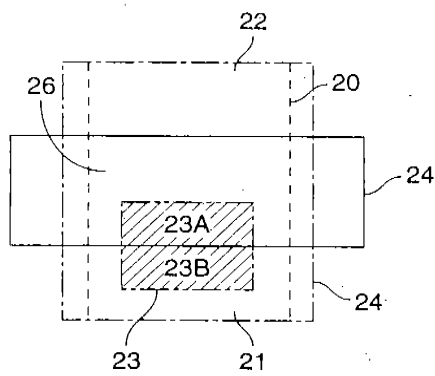


FIG. 2A

2/4

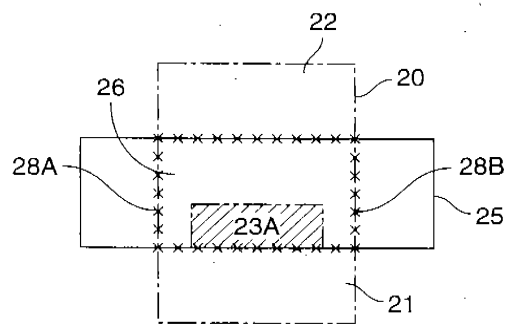


FIG. 2B

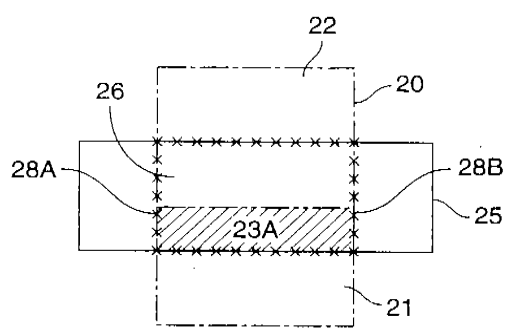


FIG. 2C

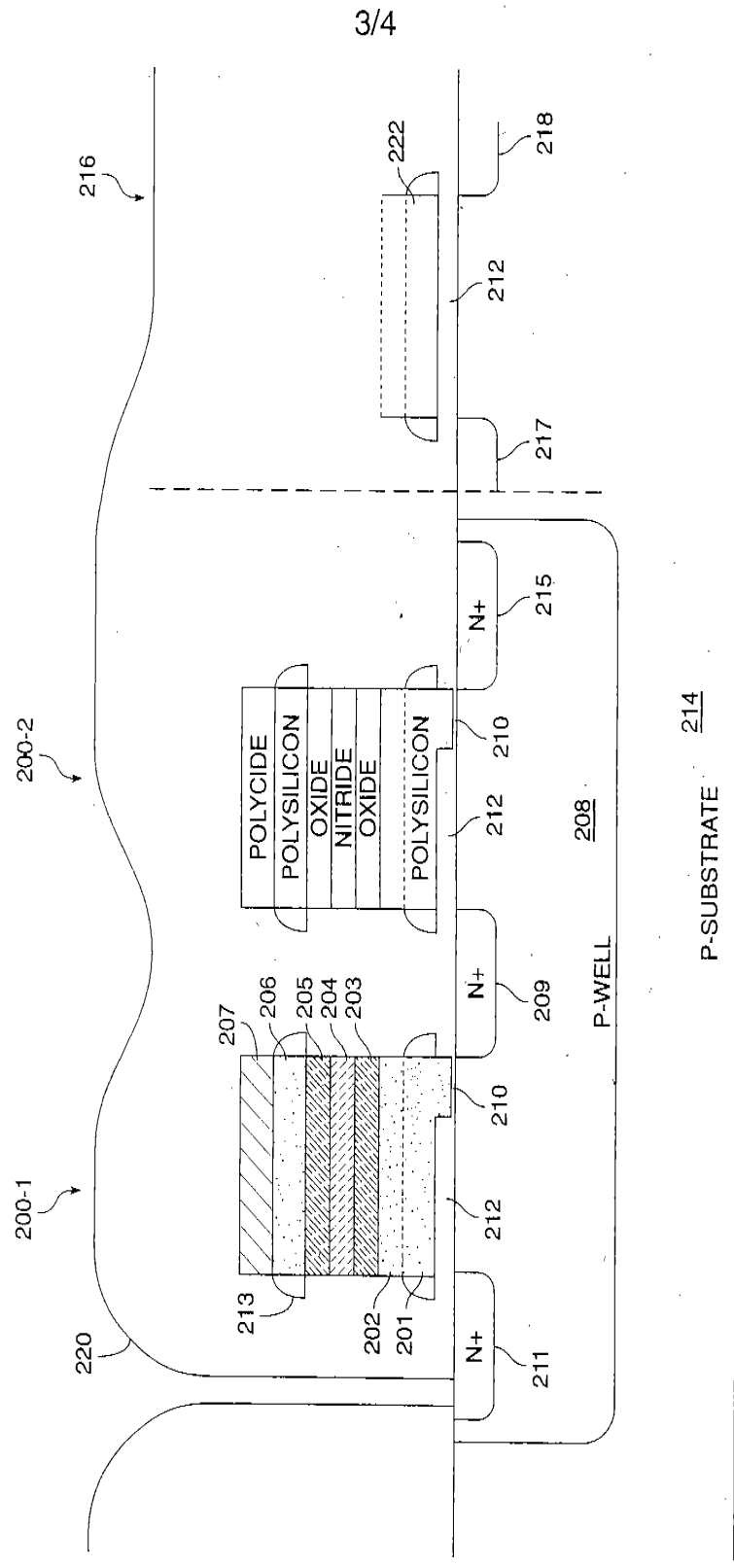


FIG. 3

400

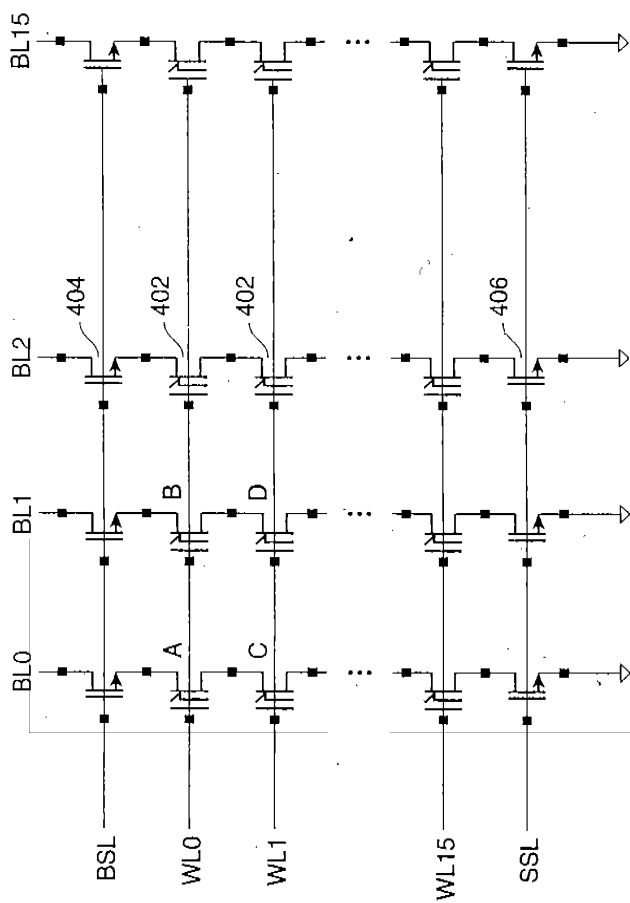


FIG. 4

PART B—ISSUE FEE TRANSMITTAL

te and mail this form, together with applicable fees, to:

Box ISSUE FEE
Assistant Commissioner for Patents
Washington, D.C. 20231

MAY 24 1999

MAILING INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE. Blocks 1 through 4 should be completed when appropriate. All further correspondence including the Issue Fee Receipt, the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

SABAK S. SANI
TOWNSEND AND TOWNSEND AND CREW
TWO EMBARCADERO CENTER 8TH FLOOR
SAN FRANCISCO CA 94111

NM11/0323

Note: The certificate of mailing below can only be used for domestic mailings of the Issue Fee Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing.

Certificate of Mailing

I hereby certify that this Issue Fee Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above on the date indicated below.

Sherry Barton

(Depositor's name)

Sherry Barton

(Signature)

May 18, 1999

(Date)

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
08/926,576	09/04/97	010	PHAN, T	2818 03/15/99
First Named Applicant	FOURKERAMATIC, ALL			

TITLE OF INVENTION
SERIAL FLASH MEMORY

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
2 1782211	365-185.260	030	UTILITY	YES	\$605.00	06/15/99

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363). Use of PTO form(s) and Customer Number are recommended, but not required.

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47) attached.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

Townsend and Townsend
1 and Crew LLP

2

3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)
PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the PTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE Azalea Microelectronics Corp.

(B) RESIDENCE: (CITY & STATE OR COUNTRY) Santa Clara, California

Please check the appropriate assignee category indicated below (will not be printed on the patent)

☐ Individual ☒ corporation or other private group entity ☐ government

4a. The following fees are enclosed (make check payable to Commissioner of Patents and Trademarks):

☐ Issue Fee☐ Advance Order - # of Copies

4b. The following fees or deficiency in these fees should be charged to:

DEPOSIT ACCOUNT NUMBER 20-1430

(ENCLOSE AN EXTRA COPY OF THIS FORM)

☒ Issue Fee☒ Advance Order - # of Copies 10

The COMMISSIONER OF PATENTS AND TRADEMARKS IS requested to apply the Issue Fee to the application identified above.

(Authorized Signatures)

Babak S. Sani, Reg. No. 37,495

(Date)

5-18-99

NOTE: The Issue Fee will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the Patent and Trademark Office.

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending on the needs of the individual case. Any comments on the amount of time required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND FEES AND THIS FORM TO: Box Issue Fee, Assistant Commissioner for Patents, Washington D.C. 20231

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30.00 CH

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Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

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08/926576

Atty Docket No. 022193-120110US

PTO FAX NO.: 703-872-9306

ATTENTION: Examiner T. PHAN

Group Art Unit 2818

**OFFICIAL COMMUNICATION
FOR THE PERSONAL ATTENTION OF
EXAMINER T. PHAN**

CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that the following documents in re Application of Ali POURKERAMATI, Application No. 08/926,576, filed on September 4, 1997 for SERIAL FLASH MEMORY are being facsimile transmitted to the Patent and Trademark Office on the date shown below.

Documents Attached

1. Power of Attorney (1 page)
2. Statement Under 37 CFR 3.73(b) (1 page)

Number of pages being transmitted, including this page: 3

Dated: February 2, 2005


Katherine Parkas

**PLEASE CONFIRM RECEIPT OF THIS PAPER BY
RETURN FACSIMILE AT (415) 576-0300**

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, CA 94111-3834
Telephone: 415-576-0200
Fax: 415-576-0300

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2005 02/02 11:53 FAX 415 576 07

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FEB 02 2005

PTO/SB/81 (11-04)

POWER OF ATTORNEY and CORRESPONDENCE ADDRESS INDICATION FORM	
Application Number	08/926,578
Filing Date	September 4, 1997
First Named Inventor	AI POURKERAMATI
Title	Serial Flash Memory
Art Unit	2818
Examiner Name	T. PHAN
Attorney Docket Number	022183-120110US
I hereby revoke all previous powers of attorney given in the above-identified application.	
I hereby appoint:	
<input checked="" type="checkbox"/> Practitioners associated with the Customer Number:	20350
OR	
<input type="checkbox"/> Practitioner(s) named below:	
Name	Registration Number
as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith.	
Please recognize or change the correspondence address for the above-identified application to:	
<input checked="" type="checkbox"/> The address associated with the above-mentioned Customer Number:	
OR	
<input type="checkbox"/> The address associated with Customer Number:	
OR	
<input type="checkbox"/> Firm or Individual Name	
Address	
City	State Zip
Country	
Telephone	Fax
I am the:	
<input type="checkbox"/> Applicant/Inventor,	
<input checked="" type="checkbox"/> Assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).	
SIGNATURE of Applicant or Assignee of Record	
Signature	Date
Name	Telephone
Title and Company	
NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.	
<input type="checkbox"/> *Total of _____ forms are submitted.	

60411524 v1

2005 02/02 11:55 FAX 415 576 03

003/003

PTO/SB/66 (03-03)

Attorney Docket No. 022193-120110US

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Frontenac Ventures, LLC

Application No./Patent No.: 08/826,576; 5,953,254 Filed/Issue Date: 09/04/1997; September 14, 1999

Entitled: Serial Flash Memory

Frontenac Ventures, LLC a corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. ☒ the assignee of the entire right, title, and interest; or
2. ☐ an assignee of less than the entire right, title and interest.
The extent (by, percentage) of its ownership interest is _____ %

In the patent application/patent identified above by virtue of either:

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

OR

B. ☒ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as shown below:

1. From: Ali POURKERAMATI To: Azalea Microelectronics Corporation

The document was recorded in the United States Patent and Trademark Office at Reel 008039, Frame 0081, or for which a copy thereof is attached.

2. From: Azalea Microelectronics Corporation To: Frontenac Ventures, LLC

The document was recorded in the United States Patent and Trademark Office at Reel 015494, Frame 0256, or for which a copy thereof is attached.

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Copies of assignments or other documents in the chain of title are attached.

(NOTE: A separate copy (i.e., the original assignment document or a true copy of the original document) must be submitted to Assignment Division in accordance with 37 CFR Part 3, if the assignment is to be recorded in the records of the USPTO. See MPEP 302.8)

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

01 FEB 2005

Date

Telephone number

Julia Ceffalo

Typed or printed name

Signature

Authorized Person

Title

44158837.v4

5953254

Page 1 of 1



UNITED STATES PATENT AND TRADEMARK OFFICE

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
08/926,576	09/04/1997	ALI POURKERAMATI	1782211

20350
TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

CONFIRMATION NO. 7207



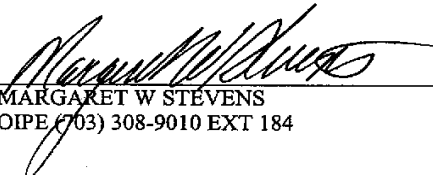
OC000000020342854

Date Mailed: 09/07/2006

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 02/02/2005.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.


MARGARET W STEVENS
OIPE (703) 308-9010 EXT 184

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UNITED STATES PATENT AND TRADEMARK OFFICE

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
08/926,576	09/04/1997	ALI POURKERAMATI	1782211

BABAK S. SANI
TOWNSEND AND TOWNSEND AND CREW
TWO EMBARCADERO CENTER 8TH FLOOR
SAN FRANCISCO, CA 94111

CONFIRMATION NO. 7207




OC000000020342828

Date Mailed: 09/07/2006

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 02/02/2005.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).


MARGARET W STEVENS
OICE (703) 308-9010 EXT 184

OFFICE COPY

201.04(b) Provisional Application [R - 3]

35 U.S.C. 111 APPLICATION.

(b) PROVISIONAL APPLICATION. -

(1) AUTHORIZATION. - A PROVISIONAL APPLICATION FOR PATENT SHALL BE MADE OR AUTHORIZED TO BE MADE BY THE INVENTOR, EXCEPT AS OTHERWISE PROVIDED IN THIS TITLE, IN WRITING TO THE COMMISSIONER. SUCH APPLICATION SHALL INCLUDE -

(A) A SPECIFICATION AS PRESCRIBED BY THE FIRST PARAGRAPH OF SECTION 112 OF THIS TITLE; AND

(B) A DRAWING AS PRESCRIBED BY SECTION 113 OF THIS TITLE.

(2) CLAIM. - A CLAIM, AS REQUIRED BY THE SECOND THROUGH FIFTH PARAGRAPHS OF SECTION 112, SHALL NOT BE REQUIRED IN A PROVISIONAL APPLICATION.

(3) FEE. - (A) THE APPLICATION MUST BE ACCOMPANIED BY THE FEE REQUIRED BY LAW.

(B) THE FEE MAY BE SUBMITTED AFTER THE SPECIFICATION AND ANY REQUIRED DRAWING ARE SUBMITTED, WITHIN SUCH PERIOD AND UNDER SUCH CONDITIONS, INCLUDING THE PAYMENT OF A SURCHARGE, AS MAY BE PRESCRIBED BY THE COMMISSIONER.

(C) UPON FAILURE TO SUBMIT THE FEE WITHIN SUCH PRESCRIBED PERIOD, THE APPLICATION SHALL BE REGARDED AS ABANDONED, UNLESS IT IS SHOWN TO THE SATISFACTION OF THE COMMISSIONER THAT THE DELAY IN SUBMITTING THE FEE WAS UNAVOIDABLE OR UNINTENTIONAL.

(4) FILING DATE. - THE FILING DATE OF A PROVISIONAL APPLICATION SHALL BE THE DATE ON WHICH THE SPECIFICATION AND ANY REQUIRED DRAWING ARE RECEIVED IN THE PATENT AND TRADEMARK OFFICE.

(5) ABANDONMENT. - THE PROVISIONAL APPLICATION SHALL BE REGARDED AS ABANDONED 12 MONTHS AFTER THE FILING DATE OF SUCH APPLICATION AND SHALL NOT BE SUBJECT TO REVIVAL THEREAFTER.

(6) OTHER BASIS FOR PROVISIONAL APPLICATION. - SUBJECT TO ALL THE CONDITIONS IN THIS SUBSECTION AND SECTION 119(e) OF THIS TITLE, AND AS PRESCRIBED BY THE COMMISSIONER, AN APPLICATION FOR PATENT FILED UNDER SUBSECTION (A) MAY BE TREATED AS A PROVISIONAL APPLICATION FOR PATENT.

(7) NO RIGHT OF PRIORITY OR BENEFIT OF EARLIEST FILING DATE. - A PROVISIONAL APPLICATION SHALL NOT BE ENTITLED TO THE RIGHT OF PRIORITY OF ANY OTHER APPLICATION UNDER SECTION 119 OR 365(A) OF THIS TITLE OR TO THE BENEFIT OF AN EARLIER FILING DATE IN THE UNITED STATES UNDER SECTION 120, 121, OR 365(C) OF THIS TITLE.

(8) APPLICABLE PROVISIONS. - THE PROVISIONS OF THIS TITLE RELATING TO APPLICATIONS FOR PATENT SHALL APPLY TO PROVISIONAL APPLICATIONS FOR PATENT, EXCEPT AS OTHERWISE PROVIDED, AND EXCEPT THAT PROVISIONAL APPLICATIONS FOR PATENT SHALL NOT BE SUBJECT TO SECTIONS 115, 131, 135, AND 157 OF THIS TITLE.

37 CFR 1.9 Definitions.

(a)(1) A national application as used in this chapter means a U.S. application for patent which was either filed in the Office under 35 U.S.C. 111, or which entered the national stage from an international application after compliance with 35 U.S.C. 371.

(2) A provisional application as used in this chapter means a U.S. national application for patent filed in the Office under 35 U.S.C. 111(b).

(3) A nonprovisional application as used in this chapter means a U.S. national application for patent which was either filed in the Office under 35 U.S.C. 111(a), or which entered the national stage from an international application after compliance with 35 U.S.C. 371.

37 CFR 1.53 Serial number, filing date, and completion of application.

(b)(2) The filing date of a provisional application is the date on which: a specification as prescribed by 35 U.S.C. 112, first paragraph; and any drawing required by § 1.81(a), are filed in the Patent and Trademark Office in the name of the actual inventor or inventors as required by § 1.41. No amendment, other than to make the provisional application comply with all applicable regulations, may be made to the provisional application after the filing date of the provisional application. If all the names of the actual inventor or inventors are not supplied when the specification and any required drawing are filed, the provisional application will not be given a filing date earlier than the date upon which the names are supplied unless a petition with the fee set forth in § 1.17(q) is filed which sets forth the reasons the delay in supplying the names should be excused.

One of the provisions of the Uruguay Round Agreements Act which is effective as of June 8, 1995, is the establishment of a domestic priority system. The Act provides a mechanism to enable domestic applicants to quickly and inexpensively file provisional applications. Under the provisions of 35 U.S.C. 119(e), applicants are entitled to claim the benefit of priority in a given application in the United States. The domestic priority period will not count in the measurement of the 20 - year patent term. See 35 U.S.C. 154(a)(3). Thus, domestic applicants are placed on equal footing with foreign applicants with respect to the patent term.

The parts of a provisional application that are required are set forth in 37 CFR 1.51(a)(2) and MPEP § 601.01 and § 601.01(b). The filing date of a provisional application is the date on which (1) a specification which complies with 35 U.S.C. 112, first paragraph, and (2) any drawing required by 37 CFR 1.81(a) are filed in the name of the actual inventor or inventors as required by 37 CFR 1.41. A provisional application must also include a cover sheet identifying the application as a provisional application. Otherwise, the application will be treated as an application filed under 37 CFR 1.53(b)(1). The filing fee is set forth in 37 CFR 1.16(k).

Note:

- (1) **No claim is required in a provisional application.**
- (2) **No oath or declaration is required in a provisional application.**
- (3) **Provisional applications will not be examined for patentability,**

placed in an interference, or made the subject of a statutory invention registration.

A provisional application will automatically be abandoned 12 months after its filing date and will not be subject to revival to restore it to pending status thereafter. Since a provisional application can be pending for no more than 12 months, if the last day of pendency is on a Saturday, Sunday, or Federal holiday, copendency would require that the later filed nonprovisional application be filed prior to the Saturday, Sunday, or Federal holiday. See 37 CFR 1.78(a)(3). > For example, if a provisional application was filed on June 28, 1996, the last day of pendency of the provisional application under 35 U.S.C. 111(b)(5) is June 28, 1997. Since June 28, 1997 is a Saturday, a nonprovisional application claiming the benefit of the provisional application must be filed on the Friday, June 27, 1997, prior to the Saturday (See 37 CFR 1.78(a)(3)). However, note that new patent applications filed in accordance with 37 CFR 1.10 will be stamped by the Office with the date of deposit as "Express Mail" with the United States Postal Service. For example, if a new patent application is deposited in "Express Mail" in accordance with 37 CFR 1.10 on a Saturday and the United States Postal Service gives it a date of deposit of Saturday, the Office will accord and stamp the correspondence with the Saturday date. 37 CFR 1.6(a)(2). < A provisional application is not entitled to claim priority benefits based on any other application under 35 U.S.C. 119, 120, 121, or 365.

An application filed under 37 CFR 1.53(b)(1) may be converted to a provisional application provided a petition requesting the conversion is submitted along with the fee as set forth in 37 CFR 1.17(q). The petition and fee must be submitted prior to the earlier of the abandonment of the nonprovisional application, the payment of the issue fee, the expiration of 12 months after the filing date of the nonprovisional application, or the filing of a request for statutory invention registration. The grant of any such petition will not entitle applicant to a refund of the fees which were properly paid in the application filed under 37 CFR 1.53(b)(1).

Design applications may not make a claim for priority of a provisional application under 37 CFR 1.78(a)(3).

PATENT APPLICATION FEE DETERMINATION RECORD Effective October 1, 1996					Application or Docket Number 926576																																				
CLAIMS AS FILED - PART I																																									
		(Column 1)	(Column 2)																																						
FOR		NUMBER FILED		NUMBER EXTRA																																					
BASIC FEE																																									
TOTAL CLAIMS		0	minus 20 =	*																																					
INDEPENDENT CLAIMS		4	minus 3 =	*1																																					
MULTIPLE DEPENDENT CLAIM PRESENT																																									
* If the difference in column 1 is less than zero, enter "0" in column 2																																									
CLAIMS AS AMENDED - PART II																																									
		(Column 1)	(Column 2)	(Column 3)																																					
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<div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"> <p>the entry in column 1 is less than the entry in column 2, write "0" in column 3.</p> <p>the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."</p> <p>the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."</p> <p>the "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.</p> </div> <div style="width: 50%;"> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th colspan="2" style="text-align: center;">SMALL ENTITY</th> <th style="text-align: center;">OR</th> <th colspan="2" style="text-align: center;">OTHER THAN SMALL ENTITY</th> </tr> <tr> <th style="text-align: center;">RATE</th> <th style="text-align: center;">FEE</th> <th></th> <th style="text-align: center;">RATE</th> <th style="text-align: center;">FEE</th> </tr> </thead> <tbody> <tr> <td></td> <td style="text-align: center;">385.00</td> <td style="text-align: center;">OR</td> <td></td> <td style="text-align: center;">770.00</td> </tr> <tr> <td>x\$11=</td> <td></td> <td style="text-align: center;">OR</td> <td>x\$22=</td> <td></td> </tr> <tr> <td>x40=</td> <td></td> <td style="text-align: center;">OR</td> <td>x80=</td> <td style="text-align: center;">80</td> </tr> <tr> <td>+130=</td> <td></td> <td style="text-align: center;">OR</td> <td>+260=</td> <td></td> </tr> <tr> <td>TOTAL</td> <td></td> <td style="text-align: center;">OR</td> <td>TOTAL</td> <td></td> </tr> </tbody> </table> </div> </div>							SMALL ENTITY		OR	OTHER THAN SMALL ENTITY		RATE	FEE		RATE	FEE		385.00	OR		770.00	x\$11=		OR	x\$22=		x40=		OR	x80=	80	+130=		OR	+260=		TOTAL		OR	TOTAL	
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PACE DATA ENTRY CODING SHEET

U.S. DEPARTMENT OF COMMERCE
Patent and Trademark Office

1ST EXAMINER

DATE

2ND EXAMINER

DATE

APPLICATION NUMBER
70204 U.S. PTO
08/926576

TYPE
APPL

FILING DATE
MONTH DAY YEAR

SPECIAL
HANDLING

GROUP
ART UNIT

CLASS

SHEETS OF
DRAWING

INDEPENDENT
CLAIMS

SMALL
ENTITY?

FOREIGN
LICENSE

ATTORNEY DOCKET NUMBER

CONTINUITY DATA

CONT STATUS
CODE

PARENT APPLICATION
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PCT APPLICATION SERIAL NUMBER

PARENT PATENT
NUMBER

PARENT FILING
DATE

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FOREIGN
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PCT/FOREIGN APPLICATION SERIAL NUMBER

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FILING DATE

MONTH DAY YEAR

STAPLE

AREA

U.S. GOVERNMENT PRINTING OFFICE: 1998-440-769

PATENT NUMBER

ORIGINAL CLASSIFICATION

CLASS

365

SUBCLASS

185.26

APPLICATION SERIAL NUMBER

08/926,576

CROSS REFERENCE(S)

CLASS

365

SUBCLASS
(ONE SUBCLASS PER BLOCK)

185.17

185.18

185.33

APPLICANT'S NAME (PLEASE PRINT)

POURKERMATI

257

321

IF REISSUE, ORIGINAL PATENT NUMBER

INTERNATIONAL CLASSIFICATION

G I I C

H O I L

16/04

29/792

GROUP
ART UNIT

2818

ASSISTANT EXAMINER (PLEASE STAMP OR PRINT FULL NAME)

PRIMARY EXAMINER (PLEASE STAMP OR PRINT FULL NAME)

TRONG PHAN

PTO 270
(REV. 5-91)

ISSUE CLASSIFICATION SLIP

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

Claim	Final	Original	2	3	3	Date
			10	19	14	
			13	98	99	
1	1	1	✓	=		
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SYMBOLS

✓ Rejected
- Allowed
(Through numeral) Canceled
+ Restricted
N Non-elected
I Interference
A Appeal
O Objected



SEARCHED			
Class	Sub.	Date	Exmr.
365	185.17 185.18 185.26 185.33	8/18/98	TP
257	321		
438	261		
All above	search updated	3/14/99	TP

INTERFERENCE SEARCHED			
Class	Sub.	Date	Exmr.
All above	search updated	3/14/99	TP

SEARCH NOTES		
APS	Date	Exmr.
	3/14/99	TP

(RIGHT OUTSIDE)