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ALI POURKERAMATI, PALO ALTO, CA.

APPLICANTS

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FOREIGN/PCT APPLICATIONS***
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FOREIGN FILING LICENSE GRANTED 01/08/97

***** SMALL ENTITY *****

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TITLE

SERIAL FLASH MEMORY

U.S. DEPT. OF COMM./ PAT. & TM—PTO-436L (Rev.12-94)

Form PTO-1625
(Rev. 5/95)

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(FACE)

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PATENT APPLICATION



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Date Received or Mailed

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PATENT APPLICATION SERIAL NO. **60/025698**


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ADDRESS	BABAK S SANI TOWNSEND AND TOWNSEND AND CREW 8TH FLOOR TWO EMBARCADERO CENTER SAN FRANCISCO CA 94111-3834				
	TITLE SERIAL FLASH MEMORY				
This is to certify that annexed hereto is a true copy from the records of the United States Patent and Trademark Office of the application which is identified above. By authority of the COMMISSIONER OF PATENTS AND TRADEMARKS Date _____ Certifying Officer _____					

60/025698

PROVISIONAL APPLICATION



Atty. Docket No. 17822-1
"Express Mail" Label No. EM290581412US
Date of Deposit September 9, 1996

I hereby certify that this is being deposited with the U.S. Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above, addressed to the Asst. Commissioner of Patents, Box Provisional Patent Appln., Washington, DC 20231.

By: *[Signature]*

BOX PROVISIONAL PATENT APPLICATION
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Washington, D. C. 20231

Sir:

Transmitted herewith for filing is a provisional patent application under 37 CFR 1.53(b)(2) of:

LAST NAME	FIRST NAME	MIDDLE INITIAL	RESIDENCE (CITY/STATE/COUNTRY)
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Title:

Enclosed are:

☒ 12 pages of the specification (including description and claims).

☒ 5 sheet(s) of drawing(s).

☒ Abstract

☐ A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27.

☐ The invention was made by or under a contract with the following agency of the United States Government: _____

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Attorney Docket No. 017822-0001

PROVISIONAL

PATENT APPLICATION

SERIAL FLASH MEMORY

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PATENT

Attorney Docket No. 017822-0001

SERIAL FLASH MEMORY

5

BACKGROUND OF THE INVENTION

The present invention relates in general to semiconductor memories, and in particular to an improved flash memory circuit and method of manufacture.

10

The flash memory technology developed from the erasable programmable read only memory (EPROM) technology. Similar to the EPROM cell, the flash memory typically uses a single transistor memory cell which makes it relatively lower cost. A flash memory cell, however, is electrically reprogrammable a limited number of times in the system.

15

Figure 1 shows a schematic cross-section of an example of a single-transistor double poly stacked gate flash cell. The cell includes a floating gate 100 made of a first polysilicon layer (poly-1), a control gate 102 made of a second polysilicon layer (poly-2), an N⁺ drain region 104 and an N⁺⁺ source region 106 inside a P-well region 108. A thin layer of silicon dioxide of approximately 70 to 120 Angstroms forms the tunnel oxide 110 between the floating gate poly-1 and the channel, and a 150 to 300 Angstroms thick film made of an oxide-nitride-oxide (ONO) sandwich 112 separates the two poly gates 100 and 102.

25

This cell is programmed by grounding the source terminal ($V_s = \text{gnd}$), applying a 5 to 10 volt signal to the drain terminal or the bit line ($V_{BL} = 5\text{v}$), and applying a high programming voltage V_{pp} of, for example, 18 to 20 volts to control gate 102 ($V_{cg} = V_{pp}$). The high voltage on V_{cg} creates a high electric field across tunnel oxide 110 generating hot electrons in the channel with enough energy to cross the tunnel oxide. These hot electrons are then trapped in the floating gate poly-1 layer 100 resulting in a higher threshold voltage for the transistor. The cell is thus programmed into an OFF (non-conducting) state.

30

Erasing of the cell is performed by grounding the control gate and the drain terminal and applying V_{pp} to the source terminal. The large gate to source voltage causes the trapped electrons on the floating poly 100 to tunnel through the thin oxide layer 110 by a mechanism known as Fowler-Nordhiem. The electrons are
5 collected by the source region 104.

The flash cell shown in Figure 1, however, suffers from a number of drawbacks in terms of its overall performance. Because the source region 104 is subject to very high erase voltages (V_{pp}), this cell requires a carefully engineered high-
10 voltage junction process. As shown in Figure 1, the source region 104 is made deeper than the drain region 106 and has a higher doping concentration. The high-voltage junction requirement results in a more complex and therefore more expensive process. Further, the high-voltage junction requirement results in a cell that is not scalable. That is, the high-voltage diffusion to high-voltage diffusion spacing requirements increases
15 the cell layout pitch. Lower endurance is another drawback of the high-voltage junction, since under high voltage conditions, the source region 104 cannot withstand a large number of erasures.

Furthermore, applying the high V_{pp} voltage to the source region 104
20 generates hot holes that are released into the P-well 108 and then collected and trapped inside the tunnel oxide 110. This phenomenon, sometimes referred to as band bending, not only deteriorates the endurance of the cell, it also results in unpredictable erase threshold voltage over time. Additional erase threshold voltage verification circuitry are thus necessary for proper operation of the cell. Finally, because the tunnel oxide region
25 110 is the same size as the channel, its capacitance is relatively larger, and thus the cell coupling capacitance is lower. Lower cell coupling capacitance requires larger program and erase voltages. Larger program and erase voltages not only lower the endurance of the cell, they also add to the circuitry as they require large pump circuits.

30 An improvement to the flash cell shown in Figure 1 splits the erase voltage between the control gate 102 and the source terminal. That is, instead of applying a high voltage to the source region 104, the control gate 102 is negatively biased with respect to the source terminal. Thus, in this embodiment, programming

voltages remain the same, but during erase, a negative voltage is applied to the control gate ($V_{cg} = -V_{pp}$) while the source terminal connects to the positive power supply voltage (typically 3 to 5 volts). This allows the source junction to be the same size as the drain junction, and eliminates the high-voltage junction process requirements. However, this
5 cell requires an additional negative pump circuit and still suffers from the hot hole injection and the resulting erratic erase threshold voltage.

Various other implementations of a single-transistor flash cell have been proposed each improving on some aspects of the cell performance, but with trade-offs
10 in other aspects. For example, one approach that eliminates performance degradations caused by the hot hole injection, places the P-well 108 inside another N-well. This allows the P-well 108 to be biased to a positive voltage along with the source and drain regions, while the control gate is biased negatively for an erase operation. This type of flash cell, however, requires a triple well technology that is much more complex and
15 costly to manufacture. Further, the cell still requires a negative pump circuit to bias the control gate during erase.

While there have been numerous variations on the double poly stacked gate single-transistor flash cell, there is always room for improvement of the structure
20 and design of the cell in terms of endurance, speed, reliability and cost of manufacture.

SUMMARY OF THE INVENTION

The present invention provides a novel scalable flash memory cell structure and method of manufacture that improves data retention, increases capacitive
25 coupling and speed of operation, and improves reliability among other advantages.

Broadly, the flash cell according to the present invention limits the tunnel oxide to a window having dimensions at the minimum feature size located over the drain side of the transistor. The tunnel oxide window is separated from the field oxide
30 and has no edges abutting field oxide. Thus, leakage due to defects caused by the field edge is eliminated, resulting in higher data retention rates for the cell. The reduced dimensions of the tunnel oxide region significantly increase the gate capacitive coupling ratio of the cell. The higher gate coupling allows the cell to be smaller yet operate at

higher speed (larger read current). The higher coupling ratio also reduces the level of the maximum required voltage resulting in higher endurance.

5 A better understanding of the nature and advantages of the flash memory of the present invention may be had with reference to the drawings and detailed description below.

BRIEF DESCRIPTION OF THE DRAWINGS

10 Figure 1 shows an exemplary prior art double poly stacked gate single transistor flash memory cell;

 Figure 2 illustrates the cross section of two flash memory cells perpendicular to word line and a high voltage transistor switch according to the present
15 invention;

 Figure 3 shows the cross section of the flash memory cell parallel to word line according to the present invention;

20 Figure 4 shows the top view (layout) of the flash cell of the present invention; and

 Figure 5 is a circuit schematic for an array made of flash cells according to the present invention.
25

DESCRIPTION OF THE PREFERRED EMBODIMENT

Cell Structural Design

30 The flash cell according to one embodiment of the present invention is implemented in a double poly, single metal, twin well CMOS process. The tunnel window is fieldless (high endurance) and is preferably of the minimum feature size. The active area surrounding the tunnel window is covered by thick cell gate oxide 38

of, for example, about 100-300 Angs. The tunnel window bottom plate is covered with, for example, 70- 100 Angs thermal dielectric 20. The tunnel window/active area edge has a gradual step of, for example, 30-200 Angs thick. Underneath the cell active area 36 is a plate of charge 30 used to control the threshold voltage of the cell.

5

The non-self aligned tunnel window is located on the drain side of the memory cell. The first polysilicon (poly1) 21 is preferably made of, for example, 500 Angs thick multiple stack with typical grain size at the tunnel oxide boundary of approximately less than 100 Angs. Poly1 21 is used as a floating polysilicon (charge storage layer) whereas the second polysilicon (poly2) of approximately 1000-2000 Angs thickness is silicided 26/27 and used as control gates (connected to word lines). The first polysilicon 21 and second polysilicon 26/27 are separated by, for example, 150-200 Angs thick Oxide-Nitride-Oxide (ONO) 23/24/25 dielectric stack. The self aligned segmented bit lines are strapped in first metal. The memory cell consists of a stack of Poly2-polycide/ONO/Poly1/tunnel oxide/well/substrate and is preferably 0.28-.34 μm .

15

Cell Process Flow

The cell formation begins with a p type resistivity silicon substrate 33. After the typical CMOS N- and P-well formation, the active areas are defined by masking and etching steps. This is followed by a field implant to increase the parasitic field threshold voltage. A thin field oxide of, for example, 3000-5000 Angs. is grown all over the wafer to isolate different active areas followed by nitride strip and kooi oxide growth.

20

A p-well protect mask is then used to block p-well formation from areas where high voltage circuit blocks will be built. This is to avoid high back biased threshold voltages of highly doped p- well. After resist strip and an oxide clean step a high quality thermal oxide (e.g., 150-190 Angs thick) is grown all over the wafer. This is followed by a cell threshold adjust mask and an implant (using e.g., Boron) to adjust the cell threshold to appropriate value between the programmed and the erased V_t distribution target. After implant the resist is stripped.

30

The wafers are then masked to form the tunnel windows in the memory cell. This mask is a critical mask as this term is used in the art. The wafers are then subjected to a short (e.g., 10-25 sec.) wet oxide cleaning step to clean the tunnel windows with non roughening characteristics. The resist is removed from the wafers and the surface is cleaned again to remove organic, metallic and hydrocarbons from the surface. A high quality thermal oxide (e.g., 70-85 Angs) is then thermally grown to cover the whole wafer. This is followed by deposition of the first of several layers of polysilicon layers each engineered with varying grain sizes. This is followed by implanting the top layer of poly with n+ dopant to amorphize the poly and dope it to achieve e.g., 200-500 ohms/square sheet resistivity.

The wafers are then oxidized (e.g., 900-1050 C) to grow thermal oxide of for example 100 Angs. This is followed by deposition of about 75-90 Angs of silicon-nitride grown at exemplary temperatures of 650-700 C. The wafers are then subjected to a wet oxidation to cover the nitride surface with 30-50 Angs of blocking oxide (1000 C wet oxidation to grow 3500-4000 Angs on bare silicon).

The wafers are then masked again to etch ONO/Poly1/gate-tunnel islands in the memory array. The anisotropic etch is designed to endpoint on the tunnel oxide. The polysilicon/ONO/gate oxide stack on the high voltage transistors is also masked in this step to protect the high voltage (HV) transistor gates. After resist strip the wafers are subjected to a light oxidation at 800-900 C in a dry ambient. This oxidation is done to seal off the exposed edges of the floating gate that is freshly exposed after the etch.

The memory array core is then masked to clean the periphery with a wet/dry etch. The memory array core mask is also used to protect the high voltage circuit areas. After the etch, the resist is stripped and the wafers are masked again to form self aligned high voltage graded junctions for the HV enhancement transistors. The high voltage implant could be for example a Phosphorus 31 implant 5E13-5E14 #/cm2 or a double diffused Phos./arsenic implant combination.

After the implant the resist is stripped and the wafers are subjected to a low voltage threshold adjust masked or blanket and implant sequence followed by a

high quality wet gate oxidation to grow about 70-110 Angs oxide in the periphery active areas. The wafers are then covered with 1.5 kA to 2.0 kA polysilicon layer that forms the gate of the periphery transistors and the first layer of the word line for memory array. A 1000-2000 Angs of Wsix is then deposited over the entire wafer.

5 The wafers are then subjected to reoxidation at 900-950 C for 30-50 minutes.

The wafers are then masked to define the memory cell stack and protect the periphery. The stacked array mask etch is then used to etch the polycide/ONO/Poly1/tunnel sandwich. After the etch, wafers are cleaned to remove
10 organics, hydrocarbons and post etch residues. The high voltage transistors are covered with resist during this etch.

The wafers are masked again to define the gate polycide of the periphery low voltage transistors. After the gate poly etch the resist is stripped. The high voltage
15 transistors are exposed during this etch. Both the polycide and the poly is etched away. About 100 Angs ONO is etched away also leaving a 50-100 Angs. dielectric on the HV gates.

The n-tip mask is then used to form the lightly doped drain (LDD) tips of
20 the NMOS transistor followed by p-tip mask and implant. The n-tip mask is blocked from memory array and HV transistors. The spacer deposition is followed by spacer etch and N+ and P+ source drain formation. The first interlayer dielectric is then formed by either BPSG, BPTEOS with 4/4 B/P, or the like. The inter layer dielectric (ILD) is then reflowed at 850-920 C and SOG planarized and the contacts are masked
25 and opened.

This is followed by barrier metal deposition followed by tungsten plug formation and first metal deposition. The metal 1 mask is then used to define the interconnect and memory array bit lines. The metal 1 is then covered with thick ILD
30 and passivation oxynitride is deposited and etched using the pad mask.

Cell Electrical Design

The cell is designed to program (high threshold cell V_t) and erase (low cell V_t) by Fowler Nordhiem tunneling to and from the same tunnel window on the drain side. The read operation is accomplished by grounding the selected word line and applying 1.0 - 1.5 volts on the selected bit line (see Cell bias Table). High cell coupling is accomplished because of reduction in tunnel area in the cell channel. This improves the cell coupling from 0.55 to 0.65. As a result voltage needed on the word line of the cell can be scaled down to 13.5-15.0 volts nominal. The choice of the V_{cg} further depends on the programming speed. At 13.5 volts the field across tunnel oxide is greater than 8 MV/cm and 100-200 uS programming can be achieved to get a target V_{trdp} of 3.0 V. Similarly the erase coupling is adequate to achieve V_{trde} of -2.5 V.

The field across programmed cells on the unselected word line is nominally 5.6 MV/cm and is designed to reduce the stress across tunnel oxide to achieve higher endurance.

Table I
Cell Biasing Scheme

Control Line	Program	Erase	Read	Condition
BSL	Vcc	Vcc	Vcc	Selected
SSL	Vss	Vss	Vcc	Selected
BL0	Vcc	Vss	1.0-1.4 V	Selected
BL1	Vss	Vcc	0.5 V	Unselected
WL0	10 V	10 V	Vcc	Unselected
WL1	-12 to -15 V	15-20 V	Vss	Selected

Cell Programming Constraints

The programming operation is done by applying high voltage on the selected control gate and grounding the selected bit line while the unselected bit lines are at Vcc (program inhibit). The cells are programmed serially such that the pass word lines are pulled up to pass the Vss to the selected cell. The cells that are programmed are subject to limited soft write because the programming is self limiting. The bit line and the select transistors are stressed for the duration of programming times the number of word lines in each block. The bit line select transistor gate oxide is

stressed during program/erase operation and can be designed to avoid both grounded gate and oxide lifetime breakdown. The programming threshold distribution is a strong function of the tunnel oxide thickness. The electrical field across tunnel oxide of a programmed cell during the life of its operation is:

5

$$\begin{aligned} V_{fg} &= K_g (V_{cg} - (V_{trdp} - V_{trdu})) \\ &= 0.6(0 - (-2.5 - (1))) \\ &= 2.1 \text{ V across } 70 \text{ Angs is } \sim 3 \text{ MV/cm} \end{aligned}$$

10 At this field the tunnel oxide stress induced leakage current is not a problem and the cell can last for greater than 25 years based on TDDDB calculations following Berkeley model on oxide breakdown. The typical programming current required is about 100 pA/cell and therefore allows for the pump circuits to be aggressively scaled.

15 Cell Erasability

Cells can be erased by the action of applying negative gate voltage of 12 to 15 volts on the selected word lines and applying $V_{cc} - 2V_{tn}$ to V_{cc} on the bit lines. This action forces electrons to leave the floating gate through the cell tunnel oxide drain interface. The choice of the bit line voltage is primarily limited to suppress
20 band bending and hot hole injection from the cell drain into the tunnel oxide. The erase speed is primarily a function of the field across tunnel oxide which is approximately 8.5 to 10 MV/cm to achieve block erasure in less than 1 msec.

Overerasure of a memory cell in conventional approaches such as single
25 transistor ETOX cells happens when cells are driven into deep depletion. Such overerasure leads to significant performance issues such as program inhibit and/or wide erase threshold variations. The flash cell according to the present invention is less sensitive to both these problems for a number of reasons. First, the engineering of the erase interface (floating poly./tunnel oxide) in the flash cell of the present invention is
30 controlled by limiting the fluctuation of the local barrier height seen by electrons. This allows a tight threshold convergence without relying on algorithm circuits. Secondly, the essentially 1.5-transistor nature of the memory cell limits the threshold variation. The memory cell can be thought of as a tunnel oxide transistor plus a high voltage

thick oxide transistor in series. The threshold voltage of the thick oxide transistor also helps to improve the punchthrough margin of the cell. Typical erase current depends on the block size and is of the order of a few mA.

5 Read Disturb

 This cell has greater margin to counter read disturb seen by memory cells primarily because of the reduced lateral electrical fields in the channel thereby suppressing hot electron generation. Furthermore the selected bit line during read operation is biased such that the erased memory cell is biased close to the velocity
10 saturation point to maximize read current and minimize hot electron generation.

Data Retention

 The cell data retention is a strong function of the two tunnel oxide barriers and the tunnel oxide thickness. Both these barriers are engineered to offer
15 reduced variations by controlling the deposition and processing conditions. Furthermore, the electric field across programmed cell is maintained below 4 MV/cm to allow improved endurance and retention. This is in contrast to ETOX type of cells where the programming is done such that greater than 6 MV/cm are stored on the programmed cell and therefore limit the retention capability.

20

 In conclusion, the present invention offers a single transistor, double-poly flash cell and a method of manufacture for the same that improves data retention, increases capacitive coupling and speed of operation, and improves reliability among other advantages. While the above is a complete description of the preferred
25 embodiment of the present invention, it is possible to use various alternatives, modifications and equivalents. Therefore, the scope of the present invention should be determined not with reference to the above description but should, instead, be determined with reference to the appended claims, along with their full scope of equivalents.

WHAT IS CLAIMED IS:

- 1 1. A memory cell comprising:
2 a source region and a drain region forming a channel therebetween;
3 a channel oxide layer disposed on top of said channel;
4 a floating gate layer disposed on top of said channel oxide layer, said
5 floating gate layer and channel oxide layer defining a window wherein a thickness of
6 said channel oxide is substantially smaller than a remaining portion of said channel
7 oxide; and
8 a control gate layer disposed on top of and separated from said floating
9 gate layer by a dielectric film,
10 wherein said window is located on a drain side of said channel and has
11 dimensions at minimum feature size.

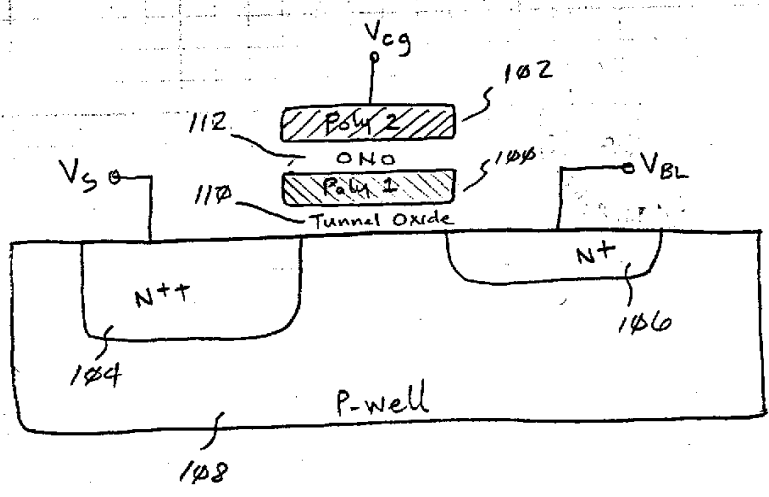
SERIAL FLASH MEMORY**ABSTRACT OF THE DISCLOSURE**

5 A scalable flash memory cell structure and method of manufacture is disclosed that improves data retention, increases capacitive coupling and speed of operation, and improves reliability among other advantages. The flash cell according to the present invention limits the tunnel oxide to a window having dimensions at the minimum feature size located over the drain side of the transistor. The tunnel oxide window is separated from the field oxide and has no edges abutting field oxide.

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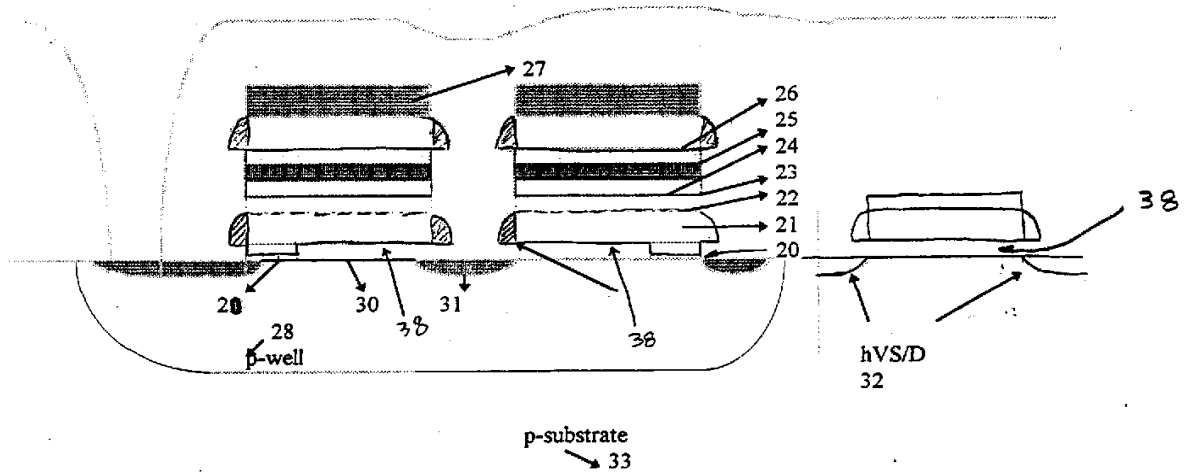
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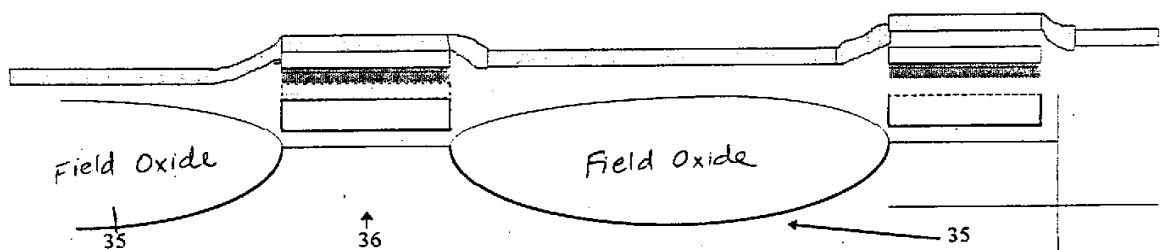


- FIGURE 1 -

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Figure 2 Cell Cross section perpendicular to word lines and cross section of High voltage transistor

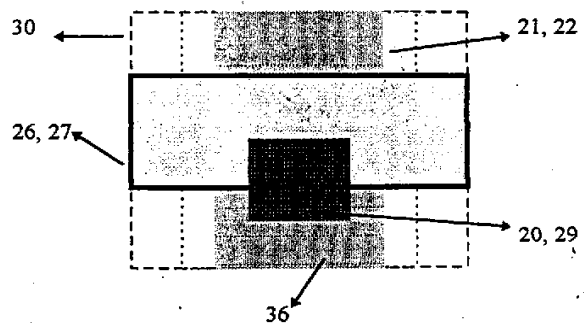


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Figure 3 Cell Cross section parallel to word line

CONFIDENTIAL INFORMATION

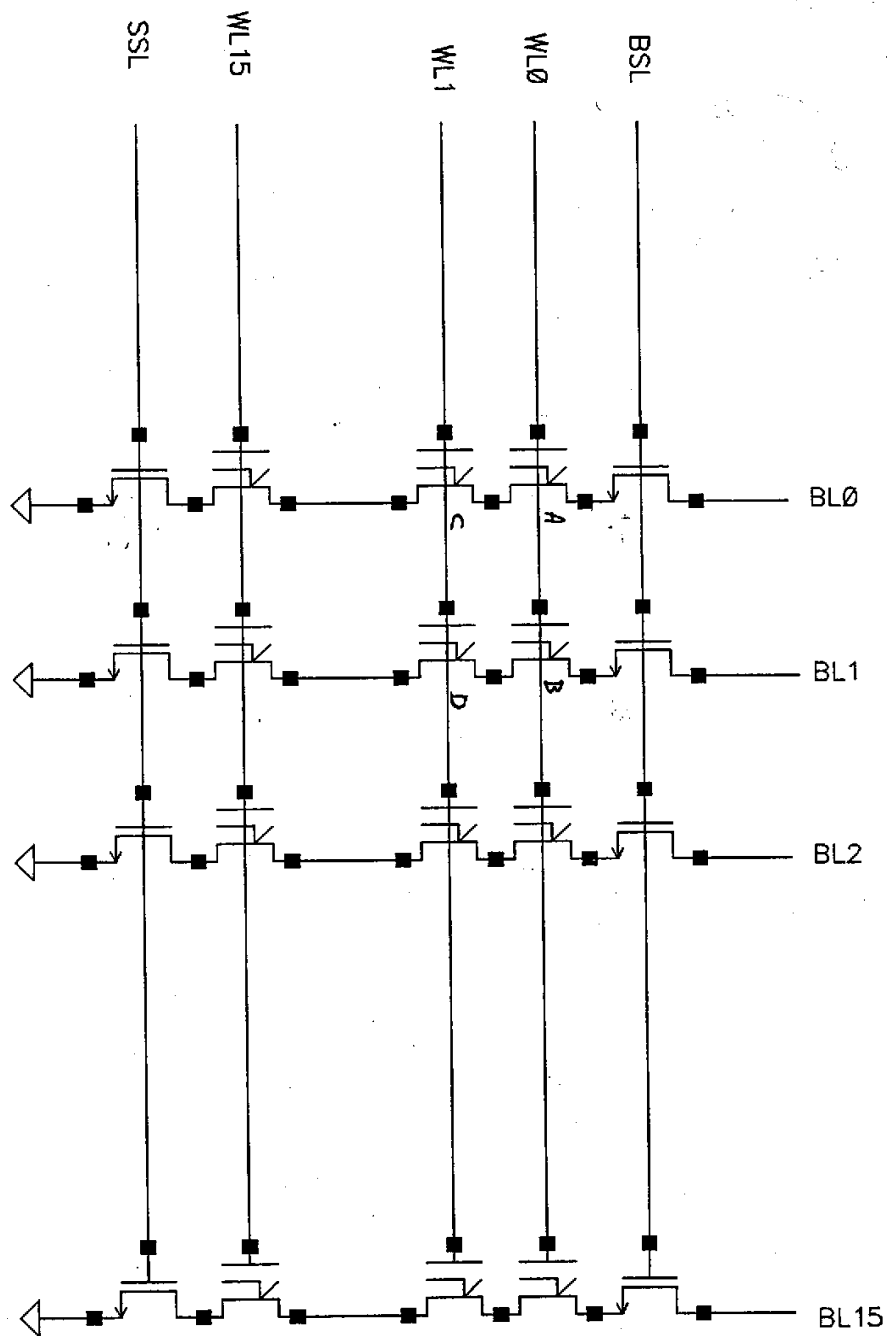
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Figure: ⁴~~X~~ TOP view of cell



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-FIGURE 5-



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Washington, D.C. 20231

APPLICATION NUMBER	RECEIPT DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
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60/025,698 09/09/96 POURKERAMATI A 17822-1

0262/1010

TOWNSEND AND TOWNSEND AND CREW
TWO EMBARCADERO CENTER 8TH FLOOR
SAN FRANCISCO CA 94111-3834

DATE MAILED: 0000

NOTICE TO FILE MISSING PARTS OF PROVISIONAL APPLICATION
FILED UNDER 37 CFR 1.53 (b) (2)

An Application Number and Filing Date have been assigned to this Provisional Application. However, the items indicated below are missing. The required items and fees identified below must be timely submitted **ALONG WITH THE PAYMENT OF THE SURCHARGE (37 CFR 1.16 (1))** for items 1 and 2 only of \$ _____ for large entities or \$ _____ for small entities who have filed a verified statement under 37 CFR 1.27 claiming such status.

If all required items on this form are filed within the period set below, the total amount owed by applicant as a ☒ large entity, ☐ small entity (verified statement filed), is \$ 125.⁰⁰.

Applicant is given **ONE MONTH FROM THE DATE OF THIS LETTER, OR TWO MONTHS FROM THE FILING DATE** of this application, **WHICHEVER IS LATER**, within which to file all required items and pay any fees required above to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136 (a).

- ☒ 1. The statutory provisional application filing fee is: ☐ missing ☒ insufficient. Applicant as a ☒ large entity ☐ small entity, must submit \$ 75.⁰⁰ to complete the filing fee.
- ☐ 2. The provisional application cover sheet identifying:
- ☐ either the city and state or city and foreign country of the residence of each inventor.
 - ☐ the title of the invention is required in compliance with 37 CFR 1.51 (a) (2) (i).
- ☐ 3. The application was filed in a language other than English. Applicant must file a verified English translation of the application and a fee of \$ _____ under 37 CFR 1.17 (k), unless this fee has already been paid.
- ☐ 4. A \$ _____ processing fee is required for returned checks. (37 CFR 1.21 (m)).
- ☐ 5. Your filing receipt was mailed in error because your check was returned without payment.
- ☐ 6. The drawings contained in the application cannot be microfilmed or properly stored because they
- ☐ do not comply with the size requirements (8 1/2 by 11 to 14 in. or 21.0 by 29.7 cm. or 21.6 by 27.9 to 35.6 cm.).
 - ☐ are not clear enough or in permanent ink. New drawings are required.
- ☐ 7. The specification cannot be microfilmed or properly stored. Page (s)
- ☐ _____ do not contain writing on only one side of the page.
 - ☐ _____ do not comply with the size requirements (8 to 8 1/2 by 10 1/2 to 13 in. (20.3 to 21.6 by 26.6 to 33.0 cm.).
 - ☐ _____ are not clear enough or in permanent ink.

Replacement pages, together with a statement that the replacement pages contain the same material as those on deposit, are required. This statement must be verified if made by someone other than an attorney or agent registered to practice before the PTO.

- ☐ 8. Other.

Direct the response and any questions about this notice to "Box Provisional Patent Application,"
ATTN: Office of National Application Review (703) 308-1202.

A copy of this notice MUST be returned with the response.

61889 U.S.



11/05/96

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:
Assistant Commissioner for Patents,
Attn: Box Provisional Patent Appln., Washington, D.C. 20231,

10-28-96

TOWNSEND and TOWNSEND and CREW LLP

By

PATENT

Attorney Docket No. 17822-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:)	BOX PROVISIONAL APPLICATION
)	<u>National Application Review</u>
POURKERAMATI)	
Serial No.: 60/025,698)	TRANSMITTAL LETTER - RESPONSE
Filed: 9/9/96)	<u>TO NOTICE OF MISSING PARTS</u>
For: SERIAL FLASH MEMORY)	

Attn: Box Missing Parts
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Pursuant to the Notice to File Missing Parts dated October 10, 1996, enclosed are the following:

- 1) Verified Statement Claiming Small Entity Status
- 2) Copy of Notice of Missing Parts

Please charge Deposit Account No. 20-1430 for the following fees:

(a) Filing Fee (Small Entity)	\$75.00
(b) Missing Parts Surcharge	\$25.00

TOTAL FEES TO BE CHARGED \$100.00

The Commissioner is hereby authorized to charge any additional fees associated with this paper or during the pendency of this application, or credit any overpayment to Deposit Account No. 20-1430. This Transmittal Letter is submitted in triplicate.

Respectfully submitted,

Babak S. Sani
Reg. No. 37,495

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
(415) 576-0200 Fax (415) 576-0300
BSS:db r:\azalea\1\msgng.Pto

Atty. Docket No. 17822-1

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS
(37 CFR 1.9(f) & 1.27(c)) - SMALL BUSINESS CONCERN

Applicant or Patentee: Ali Pourkeramati
Application or Patent No.: 60/025,698
Filed or Issued: 9/9/96
Title: SERIAL FLASH MEMORY

I hereby declare that I am:

- ☐ the owner of the small business concern identified below:
☒ an official of the small business concern empowered to act on behalf of the concern identified below:

Name of Small Business Concern: Azalea Microelectronics Corp.
Address of Small Business Concern: 2674 N. First St., Suite 208
San Jose, CA 95134

I hereby declare that the above-identified small business concern qualifies as a small business concern as defined in 13 CFR 121.12, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees to the United States Patent and Trademark Office, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention, entitled by inventor(s) Ali Pourkeramati described in:

- ☐ the specification filed herewith.
☒ Application No. 60/025,698, filed 9/9/96.
☐ Patent No. _____, issued _____.

If the rights held by the above identified small business concern are not exclusive, each individual, concern or organization having rights in the invention is listed below* and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person made the invention, or by any concern that would not qualify as a small business concern under 37 CFR 1.9(d), or a nonprofit organization under 37 CFR 1.9(e).

*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

Name Ali Pourkeramati
Address 2674 N. First St. Suite 208
San Jose, CA 95134

☐ Individual ☒ Small Business Concern ☐ Nonprofit Organization

Name _____
Address _____

☐ Individual ☐ Small Business Concern ☐ Nonprofit Organization

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b)).

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

Name of Person Signing: Ali Pourkeramati
Title of Person if Other than Owner: President
Address of Person Signing: 2674 N. First St., Suite 208
San Jose, CA 95134

Signature Ali Pourkeramati

Date 10.24.96

r:\azalea\1\sml.ent

61889 U.S. PTO



11/05/96



UNITED STATES DEPARTMENT OF COMMERCE

Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	RECEIPT DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
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60/025,698 09/09/96 / POURKERAMATI

A 17822-1

0262/1010

TOWNSEND AND TOWNSEND AND CREW
TWO EMBARCADERO CENTER 8TH FLOOR
SAN FRANCISCO CA 94111-3834

DATE MAILED: 0000

NOTICE TO FILE MISSING PARTS OF PROVISIONAL APPLICATION FILED UNDER 37 CFR 1.53 (b) (2)

An Application Number and Filing Date have been assigned to this **Provisional Application**. However, the items indicated below are missing. The required items and fees identified below must be timely submitted **ALONG WITH THE PAYMENT OF THE SURCHARGE** (37 CFR 1.16 (1)) for items 1 and 2 only of \$ _____ for large entities or \$ _____ for small entities who have filed a verified statement under 37 CFR 1.27 claiming such status.

If all required items on this form are filed within the period set below, the total amount owed by applicant as a ☒ large entity, ☐ small entity (verified statement filed), is \$ 125.

Applicant is given **ONE MONTH FROM THE DATE OF THIS LETTER, OR TWO MONTHS FROM THE FILING DATE** of this application, **WHICHEVER IS LATER**, within which to file all required items and pay any fees required above to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136 (a).

- ☒ 1. The statutory provisional application filing fee is: ☐ missing ☒ insufficient. Applicant as a ☒ large entity ☐ small entity, must submit \$ 75 to complete the filing fee.
- ☐ 2. The provisional application cover sheet identifying:
 - ☐ either the city and state or city and foreign country of the residence of each inventor.
 - ☐ the title of the invention is required in compliance with 37 CFR 1.51 (a) (2) (i).
- ☐ 3. The application was filed in a language other than English. Applicant must file a verified English translation of the application and a fee of \$ _____ under 37 CFR 1.17 (k), unless this fee has already been paid.
- ☐ 4. A \$ _____ processing fee is required for returned checks. (37 CFR 1.21 (m)).
- ☐ 5. Your filing receipt was mailed in error because your check was returned without payment.
- ☐ 6. The drawings contained in the application cannot be microfilmed or properly stored because they
 - ☐ do not comply with the size requirements (8 1/2 by 11 to 14 in. or 21.0 by 29.7 cm. or 21.6 by 27.9 to 35.6 cm.).
 - ☐ are not clear enough or in permanent ink. New drawings are required.
- ☐ 7. The specification cannot be microfilmed or properly stored. Page (s)
 - ☐ _____ do not contain writing on only one side of the page.
 - ☐ _____ do not comply with the size requirements (8 to 8 1/2 by 10 1/2 to 13 in. (20.3 to 21.6 by 26.6 to 33.0 cm.).
 - ☐ _____ are not clear enough or in permanent ink.

Replacement pages, together with a statement that the replacement pages contain the same material as those on deposit, are required. This statement must be verified if made by someone other than an attorney or agent registered to practice before the PTO.

☐ 8. Other.

Direct the response and any questions about this notice to "Box Provisional Patent Application,"
ATTN: Office of National Application Review (703) 308-1202.

A copy of this notice MUST be returned with the response.

380 MM 20-1430 11/13/96 60025698
38006 214 75.00CH
38007 227 25.00CH

RP18038 12/12/96 60025698

20-1430 180 214 75.00CR 17822-1

FORM PTO-1627 (REV.4-95)

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In re Application of

Application Number

60/025698

Filed

9/9/96

Paper No.

#4

I hereby request access under 37 CFR 1.14(a)(1)(iv) to the application file record of the above-identified ABANDONED application, which is not within the file jacket of a pending Continued Prosecution Application (CPA) (37 CFR 1.53(d)) and which is identified in, or to which a benefit is claimed, in the following document (as shown in the attachment):

United States Patent Application Publication No. _____, page, _____ line _____

United States Patent Number 5953 254, column _____, line, _____ or

WIPO Pub. No. _____, page _____, line _____

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For published applications that are still pending, a member of the public may obtain a copy of:
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Signature

HENDRICK TRAN

Typed or printed name

Registration Number, if applicable

703-229-7617

Telephone Number

5/4/89
Date

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JUN 30 2009

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In re Application of

Poor Keramati

Application Number

60/025698

Filed

9.9.96

Paper No.

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United States Patent Number *5753254*, column *1*, line *1* or

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Signature

Kenneth Slater

Typed or printed name

Date

6.30.09

Registration Number, if applicable

703 486 1150

Telephone Number

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In re Application of

Application Number

60-025,698

Filed

Sep 9, 1996

Paper No.

#6

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United States Patent Application Publication No. _____, page, _____ line _____

United States Patent Number 6058045 column _____, line, _____ or

WIPO Pub. No. _____, page _____, line _____

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Fahrene Shown

Signature

Fahrene Shown

Typed or printed name

Registration Number, if applicable

(703) 310574

Telephone Number

02/22/10

Date

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(initials)

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Bring completed form to:
File Information Unit, Suite 3A20
2800 South Randolph Street
Arlington, VA 22206

Telephone: (703) 756-1800

In re Application of

Poor Keramati

Application Number

60/025698

Filed

9-9-96

Paper No.

#7

I hereby request access under 37 CFR 1.14(a)(1)(iv) to the application file record of the above-identified ABANDONED application, which is not within the file jacket of a pending Continued Prosecution Application (CPA) (37 CFR 1.53(d)) and which is identified in, or to which a benefit is claimed, in the following document (as shown in the attachment):

United States Patent Application Publication No. _____, page, _____ line _____,

United States Patent Number 6058045, column _____, line, _____,

WIPO Pub. No. _____, page _____, line _____.

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- (1) If the benefit of the pending application is claimed under 35 U.S.C. 119(e), 120, 121, or 365 in another application that has: (a) issued as a U.S. patent, or (b) published as a statutory invention registration, a U.S. patent application publication, or an international patent application publication in accordance with PCT Article 21(2), a member of the public may obtain a copy of the file contents; the pending application as originally filed; or any document in the file of the pending application.
- (2) If the application is incorporated by reference or otherwise identified in a U.S. patent, a statutory invention registration, a U.S. patent application publication, or an international patent application publication in accordance with PCT Article 21(2), a member of the public may obtain a copy of the pending application as originally filed.

Brian G. Willingham

Signature

Brian G. Willingham

Typed of printed name

Registration Number, if applicable

703-379-2676

Telephone Number

3 | 26 | 2013

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If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



United States Patent [19]
Pourkeramati

[11] Patent Number: 6,058,045
[45] Date of Patent: May 2, 2000

[54] SERIAL FLASH MEMORY

- [75] Inventor: Ali Pourkeramati, Redwood City, Calif.
[73] Assignee: Azalea Microelectronics, Santa Clara, Calif.
[21] Appl. No.: 09/318,200
[22] Filed: May 25, 1999

Related U.S. Application Data

- [62] Division of application No. 08/926,576, Sep. 4, 1997, Pat. No. 5,953,254.
[60] Provisional application No. 60/025,698, Sep. 9, 1996.
[51] Int. Cl.⁷ G11C 16/04
[52] U.S. Cl. 365/185.17; 365/185.18;
365/185.29; 365/185.33
[58] Field of Search 365/185.17, 185.18,
365/185.29, 185.33

[56] References Cited

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- | | | | |
|-----------|---------|--------------|------------|
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| 5,216,270 | 6/1993 | Kaya et al. | 257/321 |
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| 5,909,392 | 6/1999 | Chang et al. | 365/185.17 |
| 5,978,267 | 11/1999 | Chen et al. | 365/185.17 |

OTHER PUBLICATIONS

"Semiconductor Memories," Betty Price, Texas Instruments USA, 2nd Ed., 1983, 1991, John Wiley & Sons, Chichester, New York, Brisbane, Toronto, Singapore, pp. 586-604.
"A 3.3 V 32 Mb NAND Flash Memory with Incremental Step Pulse Programming Scheme," Suh et al., *IEEE Journal of Solid-State Circuits*, vol. 30, No. 11, Nov. 1995, pp. 1149-1156.

"A 35 ns Cycle Time 3.3 V Only 32 Mb NAND Flash EEPROM," Iwata et al., *IEEE Journal of Solid-State Circuits*, vol. 30, No. 11, Nov. 1995, pp. 1157-1162.

"Advanced Salicided BECMOS Technology for Complex PLDS," Advanced Micro Devices, USA, The 14th Annual IEEE Nonvolatile Semiconductor Memory Workshop, Monterey, CA Aug. 13-16, 1995.

"Process Technology and Device Built in Reliability in NOR Virtual Ground (NYGTM) Flash Memories," National Semiconductor, U.S.A., The 14th Annual IEEE Nonvolatile Semiconductor Memory Workshop, Monterey, CA Aug. 13-16, 1995.

"High Density 'AND' Cell Technology for 32Mbit Flash Memory," Hitachi, Japan/Mitsubishi, Japan, The 14th Annual IEEE Nonvolatile Semiconductor Memory Workshop, Monterey, CA Aug. 13-16, 1995.

"Effective In-Process Plasma Damage Screening of Tunnel Oxide for Nonvolatile Memory Applications," Motorola, U.S.A., The 14th Annual IEEE Nonvolatile Semiconductor Memory Workshop, Monterey, CA Aug. 13-16, 1995.

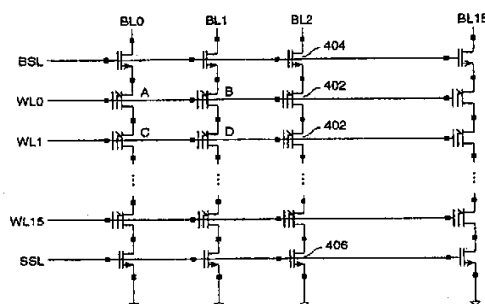
"Sidewall Sealing Effects on Flash EEPROM," SGS-Thomson, Italy, The 14th Annual IEEE Nonvolatile Semiconductor Memory Workshop, Monterey, CA Aug. 13-16, 1995.

Primary Examiner—Trong Phan

[57] ABSTRACT

A scalable flash memory cell structure and method of manufacture is disclosed that improves data retention, increases capacitive coupling and speed of operation, and improves reliability among other advantages. The flash cell according to the present invention limits the tunnel oxide to a window having dimensions at the minimum feature size located over the drain side of the transistor. The tunnel oxide window is separated from the field oxide and has no edges abutting field oxide.

6 Claims, 4 Drawing Sheets



3/26/2013, EAST Version: 3.1.1.2

PACE DATA ENTRY CODING SHEET

U.S. DEPARTMENT OF COMMERCE
Patent and Trademark Office

1ST EXAMINER	DATE
Chal	10-8-96
2ND EXAMINER	DATE
Chal	11-21-96

APPLICATION NUMBER	TYPE APPL	FILING DATE	SPECIAL HANDLING	GROUP ART UNIT	CLASS	SHEETS OF DRAWING
60/025698	9	09/09/96	2			1-1/1

TOTAL CLAIMS	INDEPENDENT CLAIMS	SMALL ENTITY?	FILING FEE	FOREIGN LICENSE	ATTORNEY DOCKET NUMBER
		2	-188	✓	17822-1

CONTINUITY DATA

CONT STATUS CODE	CODE	PARENT APPLICATION SERIAL NUMBER	PCT APPLICATION SERIAL NUMBER	PARENT PATENT NUMBER	PARENT FILING DATE
			P C T /		MONTH DAY YEAR
			P C T /		
			P C T /		
			P C T /		
			P C T /		

PCT/FOREIGN APPLICATION DATA

FOREIGN PRIORITY CLAIMED	COUNTRY CODE	PCT/FOREIGN APPLICATION SERIAL NUMBER	FOREIGN FILING DATE
			MONTH DAY YEAR

UNITED STATES PATENT & TRADEMARK OFFICE
Washington, D.C. 20231

REQUEST FOR PATENT FEE REFUND										
1 Date of Request: <u>11/96</u>		2 Serial/Patent # <u>64/025678</u>								
3 Please refund the following fee(s):		4 PAPER NUMBER	5 DATE FILED							
<input type="checkbox"/>	Filing		\$							
<input type="checkbox"/>	Amendment		\$							
<input type="checkbox"/>	Extension of Time		\$							
<input type="checkbox"/>	Notice of Appeal/Appeal		\$							
<input type="checkbox"/>	Petition		\$							
<input type="checkbox"/>	Issue		\$							
<input type="checkbox"/>	Cert of Correction/Terminal Disc.		\$							
<input type="checkbox"/>	Maintenance		\$							
<input type="checkbox"/>	Assignment		\$							
<input checked="" type="checkbox"/>	Other		\$ <u>75.00</u>							
		7 TOTAL AMOUNT OF REFUND \$ <u>75.00</u>								
10 REASON:		8 TO BE REFUNDED BY:								
<input type="checkbox"/>	Overpayment	<input checked="" type="checkbox"/> Treasury Check								
<input checked="" type="checkbox"/>	Duplicate Payment	<input type="checkbox"/> Credit Deposit A/C #:								
<input type="checkbox"/>	No Fee Due (Explanation):	9 <table border="1" style="display: inline-table; text-align: center;"> <tr> <td>2</td><td>4</td><td>--</td><td>1</td><td>4</td><td>3</td><td>8</td> </tr> </table>		2	4	--	1	4	3	8
2	4	--	1	4	3	8				
11 REFUND REQUESTED BY:										
TYPED/PRINTED NAME: <u>C. Barnes</u>		TITLE: <u>Ex.</u>								
SIGNATURE: <u>C. Barnes</u>		PHONE: <u>308-1202</u>								
OFFICE: <u>Form 6</u>										
***** THIS SPACE RESERVED FOR FINANCE USE ONLY: *****										
APPROVED: <u>Frankie Charles</u>		DATE: <u>12-9-96</u>								

Instructions for completion of this form appear on the back. After completion, attach white and yellow copies to the official file and mail or hand-carry to:

Office of Finance
Refund Branch
Crystal Park One, Room 802B