

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent of Pourkeramati:

U.S. Patent No. 6,058,045

Issued: May 2, 2000

Title: SERIAL FLASH MEMORY

Petition for *Inter Partes* Review

Attorney Docket No.: 351912-
22.045

Customer No.: 26379

Real Parties in Interest: Toshiba
Corporation; Toshiba America,
Inc.; Toshiba America Electronic
Components, Inc.; Toshiba
America Information Systems,
Inc.

DECLARATION OF ROBERT MURPHY

I, Robert Murphy, do hereby declare:

1. I am making this declaration at the request of the above identified Real Parties of Interest (“Toshiba”) in the matter of *Inter Partes* Review of U.S. Patent No. 6,058,045 (the ’045 Patent) to Pourkeramati.

2. I am being compensated for my work in this matter. My compensation in no way depends upon the outcome of this proceeding.

3. In the preparation of this declaration, I have studied:

- a. The ’045 Patent (TOSH-1001);
- b. The prosecution history of the ’045 patent (TOSH-1002);
- c. The prosecution history U.S. Patent No. 5,953,254 (TOSH-1003);

- d. The Provisional Patent Application 60/025,698 (TOSH-1004);
 - e. U.S. Patent No. 5,297,029 to Nakai (TOSH-1005);
 - f. *A 35 ns Cycle Time 3.3 V Only 32 Mb NAND Flash EEPROM*,
Yoshihisa Iwata et al, IEEE Journal of Solid-State Circuits (November
1995) (TOSH-1007);
 - g. Datasheet for *TC584000P/F/FT/TR CMOS NAND E²PROM*
electrically erasable and programmable Nonvolatile Memory,
published in Toshiba 1993 MOS Memory (Non-Volatile) Databook
(**“1993 Databook”**) (TOSH-1009);
 - h. The accompanying Petition for *Inter Partes* Review of U.S. Patent
6,058,045.
4. In forming the opinions expressed below, I have considered:
- a. The documents listed above,
 - b. My knowledge and experience based upon my work in this area as
described below.

Qualifications and Professional Experience

5. My qualifications are set forth in my curriculum vitae, a copy of which is attached as an exhibit to this declaration. As set forth in my curriculum vitae, I have over 39 years of experience with memory devices.

6. I received a Bachelors of Science in Electrical Engineering, from Drexel University (1974), and a Masters of Science in Electrical Engineering from the University of California, Los Angeles (1976).

7. My 39 years of experience in the management, development and design of commercial semiconductor products, including full custom microprocessors, E2CMOS and BiCMOS PALs, CMOS and NMOS SRAMs, CCDS and RAD Hard SOS CMOS, includes:

- a. Hughes Aircraft Co.: 4 years (circuit designer for power supplies and CCD memories);
- b. National Semiconductor: 4 years (design manager for SRAM memory products, design engineer for SRAM and DRAM products);
- c. RCA: 1.5 years (program manager for SRAM memory products);
- d. National Semiconductor: 5.5 years (senior engineering manager for the E2CMOS PAL group);
- e. Weitek Corp.: 3 years (director of engineering for floating point and embedded processor products, output drivers, and electro-static discharge circuits);
- f. Silicon Graphics Inc.: 6 years (director of engineering for microprocessor products); and

g. Firenza, LLC: 15 years (consulting and expert witness services relating to the design and operation of microprocessor and memory devices).

8. I am familiar with the knowledge and capabilities of one of ordinary skill in art for flash memory devices in 1996. Specifically, my experience in the industry and with engineers practicing in the industry allowed me to become personally familiar with the level of skill of individuals and the general state of the art.

9. In my opinion, the level of ordinary skill in the art needed to have the capability of understanding the scientific and engineering principles applicable to the '045 Patent is a Bachelors of Science degree in electrical engineering and 5 years of relevant experience, or a Masters of Science degree in electrical engineering and 3 years of relevant experience, working in the field of non-volatile memory devices.

Background Of The '045 Patent

10. The '045 Patent relates to a "Serial Flash Memory" (TOSH-1001, '045 Patent, Title). In general, the '045 patent describes a scalable flash memory cell structure and a method of manufacture. The '045 patent additionally describes the structural configuration of an array of flash memory cells together with the

application of certain voltages on various memory array lines of the array to implement memory cell program, erase and read. I have been informed that only claims 1 and 4 of the '045 patent are subject to this *inter partes* review, which are directed to the structural configuration of an array of flash memory cells and the application of certain voltages on various memory array lines of the array to implement memory cell program.

11. Claim 1 in relation to Fig. 4 provides the basic overview of the relevant teachings of the '045 patent.

1. An array of flash memory cells comprising:
 - a plurality of columns of serially connected flash memory cells, each memory cell having a gate terminal;
 - a plurality of bit lines respectively coupled to drain side of said plurality of columns of memory cells via a respective plurality of bit line select transistors, said plurality of bit line select transistors having gate terminals coupled to a bit line select control line;
 - a plurality of word lines, each one coupling to a gate terminal of one memory cell in each of said plurality of columns to form rows of memory cells with common gate terminals; and
 - a plurality of source select transistors respectively coupling a source side of said plurality of columns of memory cells to a logic low voltage, and having gate terminals coupled to a source select control line, wherein, during programming:
 - a logic high voltage is applied to said bit line select control line to turn on bit line select transistors,
 - a logic low voltage is applied to source select control line to turn off source select transistors;
 - a logic low voltage is applied to a selected bit line while a logic high voltage is applied to unselected bit lines, and
 - a logic high voltage is applied to unselected word lines, while a boosted positive voltage is applied to a selected word line.

(TOSH-1001, claim 1.)

12. Fig. 4 of the '045 Patent shows the structural configuration of the array of flash memory cells:

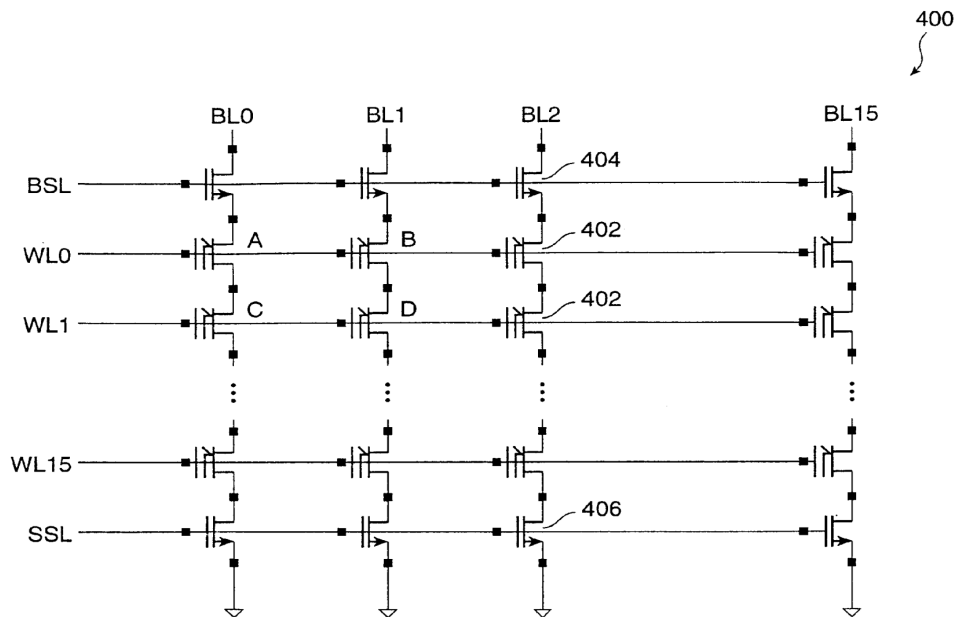


FIG. 4

(TOSH-1001, Fig. 4.)

Claim Construction

13. It is my understanding that in order to properly evaluate the '045 Patent, the terms of the claims must first be interpreted. It is also my understanding that the claims are to be given their broadest reasonable interpretation in light of the specification. It is my further understanding that claim terms are given their ordinary and accustomed meaning as would be understood by

one of ordinary skill in the art, unless the inventor, as a lexicographer, has set forth a special meaning for a term.

14. In order to construe the claims, I have reviewed the entirety of the '045 patent, as well as its prosecution history.

15. In my opinion, the inventor did not act as a lexicographer and did not provide any special meanings for any of the claim terms.

“logic low voltage”

16. It is my opinion that a person of ordinary skill in the art would understand the broadest reasonable interpretation of “logic low voltage” in view of the specification and file history to be: “a low voltage, such as ground or Vss.” This construction is confirmed in the specification of the '045 Patent, which does not include the term “logic low voltage.” Specifically, claims 1 and 4 recite that for programming, a “logic low voltage” is applied to the selected bit line. The specification states that for programming, the selected bit line is grounded and at voltage Vss (TOSH-1001 at 7:29 and 6:37-45). Additionally, claims 1 and 4 recite that for programming, a “logic low voltage” is applied to the source select control line. The specification states for programming, the source select control line is at Vss (TOSH-1001 at 6:37-45; 7:36). Further, the specification states that the source select transistors “couple ground (or Vss) to memory cells 402” (TOSH-1001 at 6:29-30).

“logic high voltage”

17. It is my opinion that a person of ordinary skill in the art would understand the broadest reasonable interpretation of “logic high voltage” in view of the specification and file history to be: “a positive voltage higher than the logic low voltage, such as Vcc.” This construction is confirmed in the specification of the ’045 Patent, which does not include the term “logic high voltage.” Specifically, claims 1 and 4 recite that the “logic high voltage” is applied to the “bit line select control line” (BSL), the unselected bit line and the unselected word line during program. The specification discloses that voltage Vcc is applied to those same lines during program (TOSH-1001 at 6:37-45; 7:26-40).

“boosted positive voltage”

18. It is my opinion that a person of ordinary skill in the art would understand the broadest reasonable interpretation of “boosted positive voltage” in view of the specification and file history to be: “a positive voltage higher than the logic high voltage.” This construction is confirmed in the specification of the ’045 Patent, which does not include the term “boosted positive voltage.” Specifically, claims 1 and 4 recite that a boosted positive voltage is applied to the selected word line during program. The specification discloses that a high voltage (e.g. 15 to 20V) is applied during program (TOSH-1001 at 6:37-45; 7:26-40).

“selected bit line”
“unselected bit lines”

19. It is my opinion that a person of ordinary skill in the art would understand the broadest reasonable interpretation of “selected bit line” in view of the specification and file history to be: “the bit line connected to the column of memory cells containing the memory cell to be operated on.” It is also my opinion that a person of ordinary skill in the art would understand the broadest reasonable interpretation of “unselected bit lines” in view of the specification and file history to be: “the bit lines connected to the columns of memory cells not containing the memory cell to be operated on.” The ’045 Patent supports these constructions where it discloses the relationship between a “selected bit line” and “unselected bit lines” by way of an example involving the programming of memory cell 402-C in Fig. 4 (i.e. the memory cell being operated on during programming). In Fig. 4, memory cell 402-C is depicted in the column of memory cells connected to bit line BL0, while the other bit lines BL1 to BL15 are not connected to the column of memory cells containing memory cell 402-C. In the description, bit line BL0 is referred to as the “selected bit line” and bit lines BL1-BL15 are referred to as the “unselected bit lines.” (TOSH-1001 at 7:27-30 and Fig. 4.)

“selected word line”
“unselected word lines”

20. It is my opinion that a person of ordinary skill in the art would understand the broadest reasonable interpretation of “selected word line” in view of the specification and file history to be: “the word line connected to the row of memory cells containing the memory cell to be operated on.” It is also my opinion that a person of ordinary skill in the art would understand the broadest reasonable interpretation of “unselected word lines” in view of the specification and file history to be: “the word lines connected to the rows of memory cells not containing the memory cell to be operated on.” The ’045 Patent supports these constructions where it discloses that when programming memory cell 402-C (i.e. the memory cell being operated on during programming), which is connected to word line WL1 but not connected to any of the other word lines, word line WL1 is referred to as the “selected word line” and word lines WL0 and WL2-WL15 are referred to as the “unselected word lines.” (TOSH-1001 at 7:27-37 and Fig. 4.)

CHALLENGE #1: Claims 1 and 4 by U.S. Patent 5,297,029 (“Nakai”)

21. The Nakai patent discloses the array configuration and the programming voltages for NAND type EEPROM devices. (TOSH-1005 at col 1, line 10 to col. 2, line 18, and Figs. 22a and 23a.).

22. It was well known to those skilled in the art that NAND type EEPROMs were commonly referred to as “flash memory” for their ability to program and erase multiple memory cells at once. See for example *A 35 ns Cycle Time 3.3 V Only 32 Mb NAND Flash EEPROM*, Yoshihisa Iwata et al, IEEE Journal of Solid-State Circuits (November 1995), which repeatedly refers to “NAND Flash EEPROM’s.” (TOSH-1007.) Therefore, one skilled in the art would understand that Nakai discloses an array of flash memory cells and a method of operating (e.g. programming) a flash memory device.

23. Figs. 22(a) and 23(a) of Nakai show a memory array with 2 columns of memory cells each connected to its own bit line (BL(1) and BL(2)). (TOSH-1005 at Figs. 22a and 23a.) One skilled in the art would understand that these figures show only a portion of the full array, and that additional columns of memory cells each connected to their own bit line are included in the full array. This understanding is supported by the fact that the Nakai patent discloses there are 4096 bit lines laid out in the column direction (TOSH-1005 at 2:25-30), and by Fig. 25(a) of Nakai which shows a multitude of memory cell columns (TOSH-1005 at Fig. 25(a)).

24. One skilled in the art would also have understood as inherent from Nakai that the additional bit lines beyond BL(2) in Figs. 22(a) and 23(a) that were not intended to be programmed would have the same voltage (i.e. VDPI) as that

being applied to BL(2), so that memory cells in those columns (i.e. “non-write cells”) are not programmed. Therefore, one skilled in the art would understand that Nakai discloses applying a logic low voltage to a selected bit line while applying a logic high voltage to unselected bit lines.

CHALLENGE #2: Claims 1 and 4 by Toshiba 1993 MOS Memory (Non-Volatile) Databook (“1993 Databook”)

25. The 1993 Databook includes a datasheet for Toshiba’s TC584000P/F/FT/TR CMOS NAND E²PROM electrically erasable and programmable nonvolatile memory product. (TOSH-1009, pages 367-380.)

26. It was well known to those skilled in the art that NAND E²PROMs were commonly referred to as “flash memory” for their ability to program and erase multiple memory cells at once. See for example *A 35 ns Cycle Time 3.3 V Only 32 Mb NAND Flash EEPROM*, Yoshihisa Iwata et al, IEEE Journal of Solid-State Circuits (November 1995), which repeatedly refers to “NAND Flash EEPROM’s.” (TOSH-1007.) Therefore, one skilled in the art would understand that the 1993 Databook discloses an array of flash memory cells and a method of operating (e.g. programming) a flash memory device.

27. Fig. 2 of the 1993 Databook shows a memory array with 2 columns of memory cells each connected to its own bit line (TOSH-1009 at p. 379). One

skilled in the art would understand that this figure shows only a portion of the full array, and that additional columns of memory cells each connected to their own bit line are included in the full array. This understanding is supported by the fact that the 1993 Databook discloses the organization of the memory cell array as being “512K x 8” (TOSH-1009 at p. 367), and by Fig. 1 which shows a multitude of memory cell columns (TOSH-1009 at p. 376).

28. One skilled in the art would also have understood as inherent from the 1993 Databook that the additional bit lines beyond those shown that were not intended to be programmed (i.e. to be left as data “1”) would have the same voltage (i.e. VDPI) as that being applied to the second bit line (bit line on the right in Fig. 2), so that memory cells in those columns are not programmed with the “0” data. Therefore, one skilled in the art would understand that the 1993 Databook discloses applying a logic low voltage to a selected bit line while applying a logic high voltage to unselected bit lines.

29. I have reviewed, had input into, and adopt the analysis and claim charts in the accompanying Petition for *Inter Partes* Review of U.S. Patent 6,058,045, showing that each element of claims 1 and 4 of the ’045 Patent is disclosed in Nakai. Based on the reasons stated in the petition, as well as my experience and knowledge, it is my opinion that Nakai anticipates claims 1 and 4 of the ’045 Patent.

U.S. Patent No. 6,058,045
Declaration in Support of Petition For Inter Partes Review

30. I have reviewed, had input into, and adopt the analysis and claim charts in the accompanying Petition for *Inter Partes* Review of U.S. Patent 6,058,045, showing that each element of claims 1 and 4 of the '045 Patent is disclosed in the 1993 Databook. Based on the reasons stated in the petition, as well as my experience and knowledge, it is my opinion that the 1993 Databook anticipates claims 1 and 4 of the '045 Patent.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

Executed on this 29th day of October, 2013.

By: Robert L. Murphy
Robert Murphy

Robert J. Murphy
72 Fairview Plaza
Los Gatos, California 95030
(408) 357-4445

Abstract: More than 39 Years of experience in management, and hands-on development and design of: High speed, high complexity, high density and high volume commercial semiconductor products including Full Custom Microprocessors, E2CMOS and BiCMOS PALs, CMOS and NMOS SRAMs, CCDS and RAD Hard SOS CMOS.

Founder & Owner
4/98 - PRESENT

Firenza, LLC.
Los Gatos, CA.

Founded company to respond to the growing needs of the semiconductor industry to license quality high performance building blocks for Semi-Custom and ASIC designs. Developed business plan, cultivated customers and managed the efforts of Design Professionals to deliver world class building blocks in 0.25 0.18 and 0.13 micron processes. Provided circuit design reviews on 65 nM Major Microprocessor. Designed EFUSE circuit for another 65 nM Microprocessor. Debugged and provided layout based solutions for 65 nM process latch-up issue. Designed 28 nM SRAM circuits.

Performed Expert Witness work on the following cases:

NeoMagic Corporation v. Trident Microsystems, Inc.
D. Del., C.A. No. 98-699-RRM

Rambus, Inc. v. Infineon Technologies AG,
Infineon Technologies North America Corp.,
And
Infineon Technologies Holding North America, Inc.
Eastern D. Virginia, C.A. No. 3:00cv524

Micron v, Rambus, Inc.
D. Del., C.A. No. 00-792-(RRM)

Hynix Semiconductor Inc. et al. v. Rambus, Inc.
Northern D. Calif., Case No. CV 00-20905 RMW

Rambus, Inc. v. Hynix Semiconductor Inc. et al.
Northern D. Calif., Case Nos. C-05-00334, C-05-02298,
C-06-00244, C-00-20905 RMW

Toshiba v. Hynix
International Trade Commission, Investigation No. 337-TA-592

UniRAM Technology, Inc. v. MONOLITHIC SYSTEM TECHNOLOGY, TAIWAN
SEMICONDUCTOR MANUFACTURING COMPANY, LTD, & TSMC NORTH AMERICA
Northern D. Calif., Case No. CV-04-01268-VRW

Career History for Robert J. Murphy (Cont'd)

Perego, et al. v. Drehmel, et al.
U.S.P.T.O., Patent Interference No. 105,467 (Bd. Pat, App.& Int.)

Reexamination proceedings involving various U.S. Patents in the
Farmwald / Horowitz Family derived from Application No. 07/510,898

Reexamination proceedings involving U.S. Patents #'s 7,210,016;
7,177,998

Reexamination proceedings involving U.S. Patents #'s 7,287,119;
7,330,952; 7,330,953; 7,360,050

Reexamination proceedings involving U.S. Patents #'s 7,287,109;
6,591,353; 6,470,405

*In The Matter Of: CERTAIN MLC FLASH MEMORY DEVICES AND
PRODUCTS CONTAINING SAME*, International Trade Commission,
Investigation No. 337-TA-683

*In The Matter Of: CERTAIN STATIC RANDOM ACCESS MEMORIES AND
PRODUCTS CONTAINING SAME*, International Trade Commission,
Investigation No. 337-TA-792

*In The Matter Of: CERTAIN WIRELESS COMMUNICATIONS EQUIPMENT AND
ARTICLES THEREIN*, International Trade Commission,
Investigation No. 337-TA-866

Director of Engineering
6/92 - 4/98

Silicon Graphics Inc.
Mountain View, CA.

Beast Program: Hired, managed and directed circuit designers on this 500 MHz design. Responsible for the scheduling and design reviews for all custom circuit design on the chip. Supported CAD tool development with test structures, test cases and debug.

T5 (R10000) Program: Assisted in the final completion of this processor. Took my team of people down to the project in it's late stages and managed 10% of the Units (3) on the chip. Was a key member of the schedule review team.

TFP (R8000) Program: Managed the design and implementation of the Floating Point Chip for SGI's POWER CHALLENGE systems. Directed the re-design of a large Tag Ram done for SGI by Toshiba. Managed a group of Toshiba's engineers in the US and interacted with their counterparts in Japan to debug and repair the design. The repaired design was fully functional with speeds of 110 MHz. The redesign was accomplished while holding 16 lots of silicon in the fab. All of the lots were saved and parts delivered to SGI on time.

Other Accomplishments at SGI:

- * Hired over 20 people.
- * Managed a total team of 30 people.
- * Developed extensive relationships with our Japanese Partners.

Career History for Robert J. Murphy (Cont'd)

- * Hired contractors as needed for specific expertise
- * Directed the development and implementation of world class PLL designs onto the whole SGI campus.
- * Developed internal circuit design resources via training and assignment selection.

Director of Engineering
2/89 - 6/92

Weitek Corp.
Sunnyvale, CA

Initially hired as a Design Manager with responsibility for putting a single chip into production. One year later, was managing the company's most important product along with others. Developed circuitry which gave the company world-class performance in memory, output drivers, and Electro-Static Discharge (ESD). Promoted to Director (1990). Managed the circuit design, architecture and layout groups. This included budgeting, staffing, and resource allocation for multiple programs, the largest of which was over 400K transistors. Responsible for the technical and administrative management of a staff that included 20 engineers and 5 layout people.

Major accomplishments included:

- * Managed the product design and release to production of a 40 MHz SPARC combined IU/FPU product
- * Managed the development and release to production of a Floating Point Coprocessor that works with the Intel i486.
- * Directed the redesign and release to production of two products, completed by other managers, which were not production worthy.
- * Aided Manufacturing in the pre- and post-production release management of our silicon foundries. This included modeling, process issues and production/testing problems.
- * Increased the staff by more than 50% in a one year period.
- * Delivered multiple projects on time.

Senior Engineering Manager
10/83 - 2/89

National Semiconductor Corp.
Santa Clara, CA

As the design manager and chief technical contributor for the E2CMOS PAL group, was a member of a team of three responsible for the introduction of three second-sourced products. Enlarged the design staff, established methodology and set circuit design criteria for new products under development. The group's actions enabled the product line to go from zero revenue to greater than \$1 million/month in just 12 months. Prior to the start up of the E2CMOS PAL group, designed a Bi-CMOS PAL using lateral Ti-W fuses.

Major accomplishments included:

- * Doubled the reliability of the second-sourced devices.
- * Participated fully in all aspects of the second-sourcing licensing agreement.

Career History for Robert J. Murphy (Cont'd)

- * Designed the world's first BiCMOS PAL, which was given as a paper at the ISSCC conference in 1986.
- * Developed the methodology and theory to improve lateral Ti-W fuse blowing circuitry.

Program Manager
4/82 - 10/83

RCA
Sommerville, NJ

Lead an inter-divisional program to develop 2 micron CMOS technology and a 64K SRAM for the commodity market. Responsible for a team of 15 people who: developed the process, did the modeling, designed the circuits, created the layout, and performed the testing.

Major accomplishments included:

- * Created a test chip (4K SRAM) shown to be fully functional, at speed, less than half way thru the program. This test chip was used to flush out the final bugs in the processing.
- * Managed the development of three new process features (Poly fuses, Poly Resistors and a 1 mask twin-tub process) that previously did not exist at RCA. Was technically responsible for Poly Resistors and Poly fuses.
- * Produced fully functional units at speed on first silicon.(64K SRAM)
- * Completed the program within two weeks of an 18 month schedule and under our \$1.2 million budget.

SRAM Design Manager
2/78 - 4/82

National Semiconductor
West Jordan, Utah

Hired as a circuit designer into the Santa Clara, Ca memory group to design a Pseudo-Static DRAM memory. Then designed a 4T cell 4K SRAM product. Promoted to Section Head when my first SRAM design went into production on the first mask set, not at the original design size, but on a 10% shrink die which was placed on the wafer across one of the rows.

Later, promoted to SRAM Design Manager and transferred to National's production facility in West Jordan. Supervised a team of six design engineers developing new products and providing production support for SRAM material in the fab.

Major accomplishments were:

- * Designed National's first SRAM with a 4T cell using poly resistors.
- * Developed a power-on standby circuit for the 2147 (4Kx1 SRAM 55ns) that was eventually copied by Intel.
- * Technical Management of the development of the world's first output short circuit control put into an SRAM.
- * Responsible for SRAM products which had a peak production rate of 30 K 4 inch (100 mm) wafers per month.

Career History for Robert J. Murphy (Cont'd)

- * Lead the team that brought the 2114 (4K SRAM) wafer yield from 50 die/wafer to over 280 die/wafer in 62 days.
- * Re-designed the 2114 to get the yield to 375 die / wafer and increased the production run rate to 4 million units per month.

Circuit Designer
6/74 - 2/78

Hughes Aircraft Co.
El Segundo, CA

Won a Hughes Masters Fellowship and worked part-time at Hughes while getting my Masters degree at UCLA. Initially, a Test Engineer testing space flight sub-assemblies, then my first design work was in power supplies. After receiving my MSEE, moved into IC design. Designed custom LSI's using SOS CMOS and a standard cell approach. Team Member designing Hughes 64K CCD Memories and also solely designed the Analog Buried Channel CCD used for the Liquid Crystal Light Valve.

Major accomplishments include:

- * Helped develop the first Liquid Crystal Light Valve at Hughes.
- * Designed or tested circuits that are still performing somewhere in space.

EDUCATION:	BSEE	Drexel University, Philadelphia, PA	June 1974
	MSEE	UCLA, Los Angeles, CA	June 1976

SIGNIFICANT PUBLICATIONS: "A Bipolar-CMOS Field Programmable Array"
ISSCC Feb 1986

SKILL SET: C, Verilog, Hspice, Dracula, Cadence/Mentor Design Tools