

TOSHIBA
MOS MEMORY (NON-VOLATILE)

DATA BOOK

93

TOSHIBA

DATA BOOK

**MOS MEMORY
(NON-VOLATILE)**

1993

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INTRODUCTION

We continually venture at the leading edge of technology so that we may develop and offer to you a diverse array of semiconductor memory products which may be used in many commercial and industrial applications. At this time, we offer five data books; "MOS-Memory Dynamic RAM", "MOS-Memory Video RAM", "MOS-Memory MODULE • CARD", "MOS-Memory Static RAM" and "MOS-Memory NON-VOLATILE".

Particularly, this data book is "MOS-Memory NON-VOLATILE" edition.

These data books represent our current culminations of electrical characteristics, timing waveforms and package data for our line of semiconductor memory products.

We hope this information will be very useful for you.

Jan. 1993

TOSHIBA CORPORATION
Semiconductor Group

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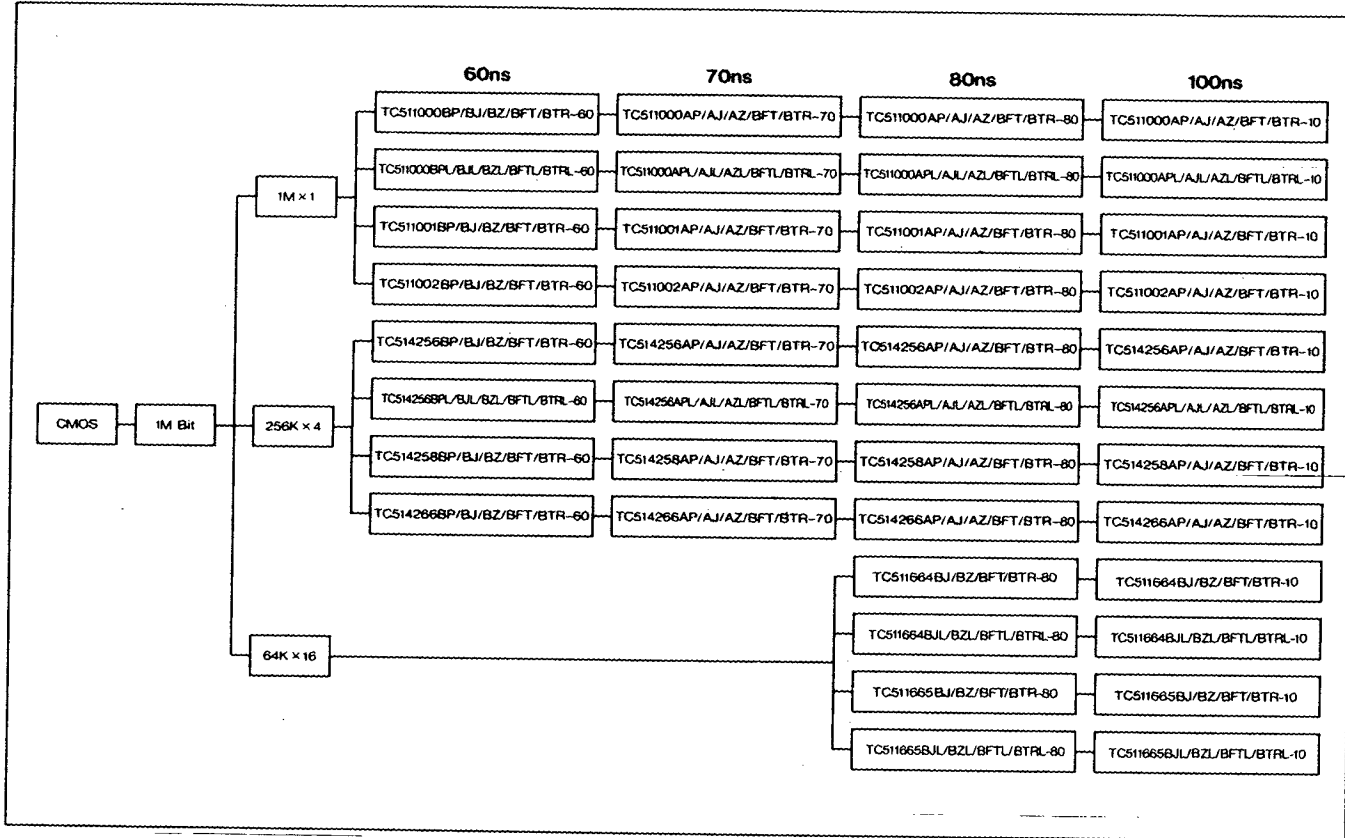
TC54H1000/1001AP/AF-85,-10	1,048,576Bit	(128K×8)	288
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TC544000P/F/FT-12,-150	4,194,304Bit	(512K×8)	308
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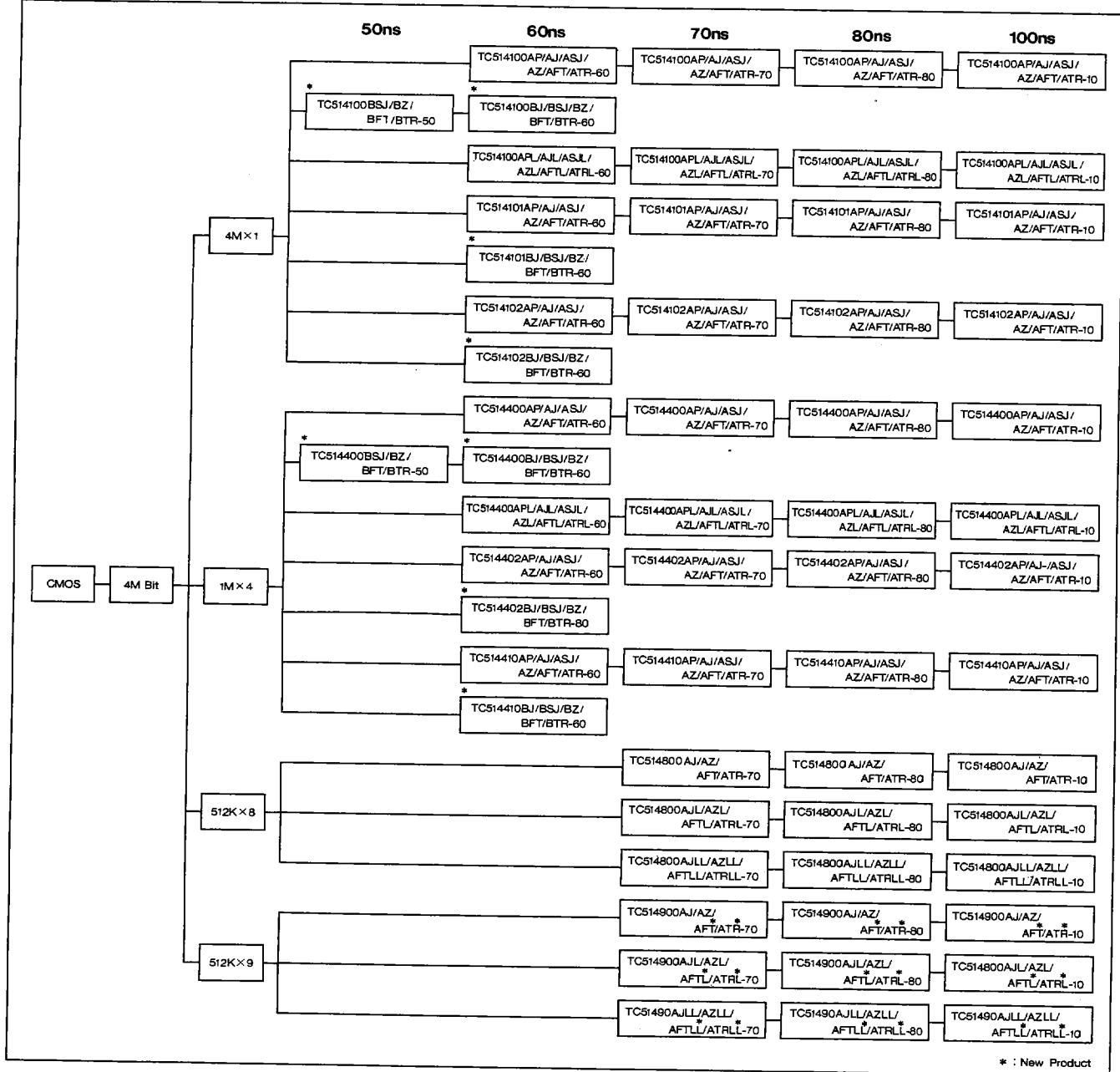
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TC534000AP/AF	4,194,304Bit	(512K×8)	396
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TC534200P/F	4,194,304Bit	(256K×16)	402
TC538000AP/AF	8,388,608Bit	(1M×8)	407
TC538200AP/AF	8,388,608Bit	(1M×8/512K×16)	410
TC5316200AP/AF	16,777,216Bit	(2M×8/1M×16)	415
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TC5316210BP/BF/BFT	16,777,216Bit	(2M×8/1M×16)	430

1. Memory Products Guide

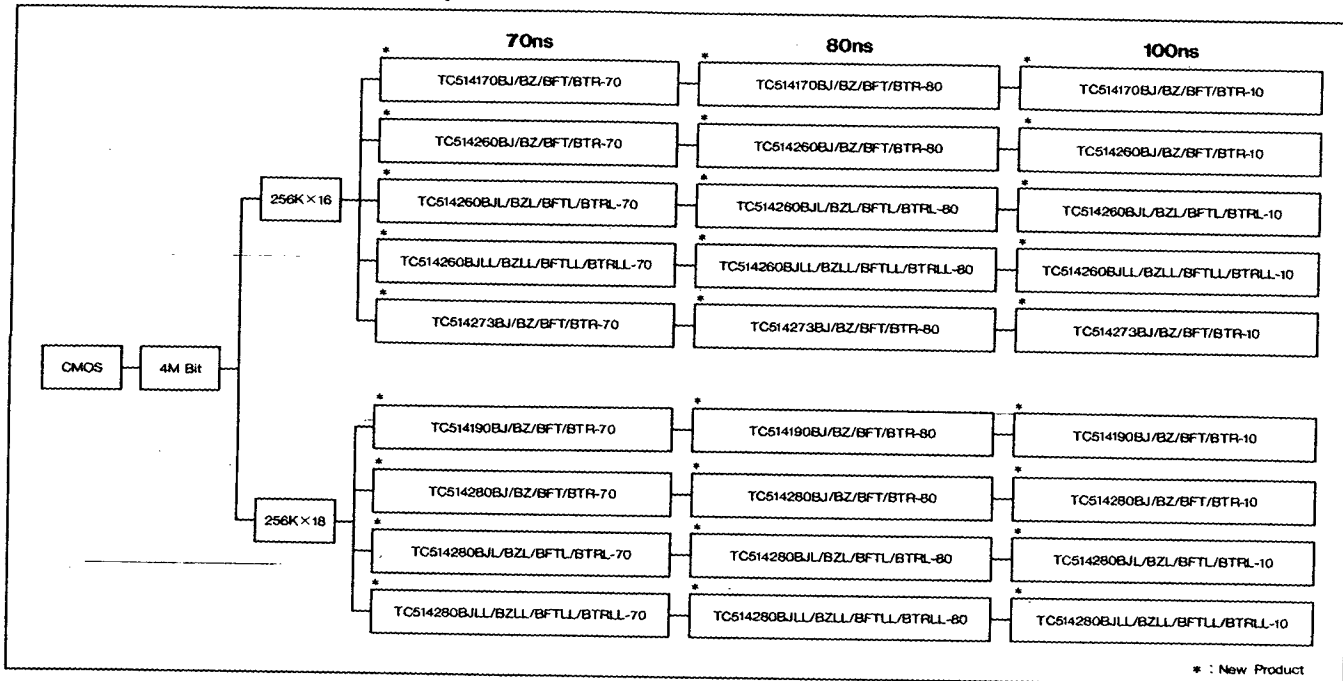
1M Dynamic RAM



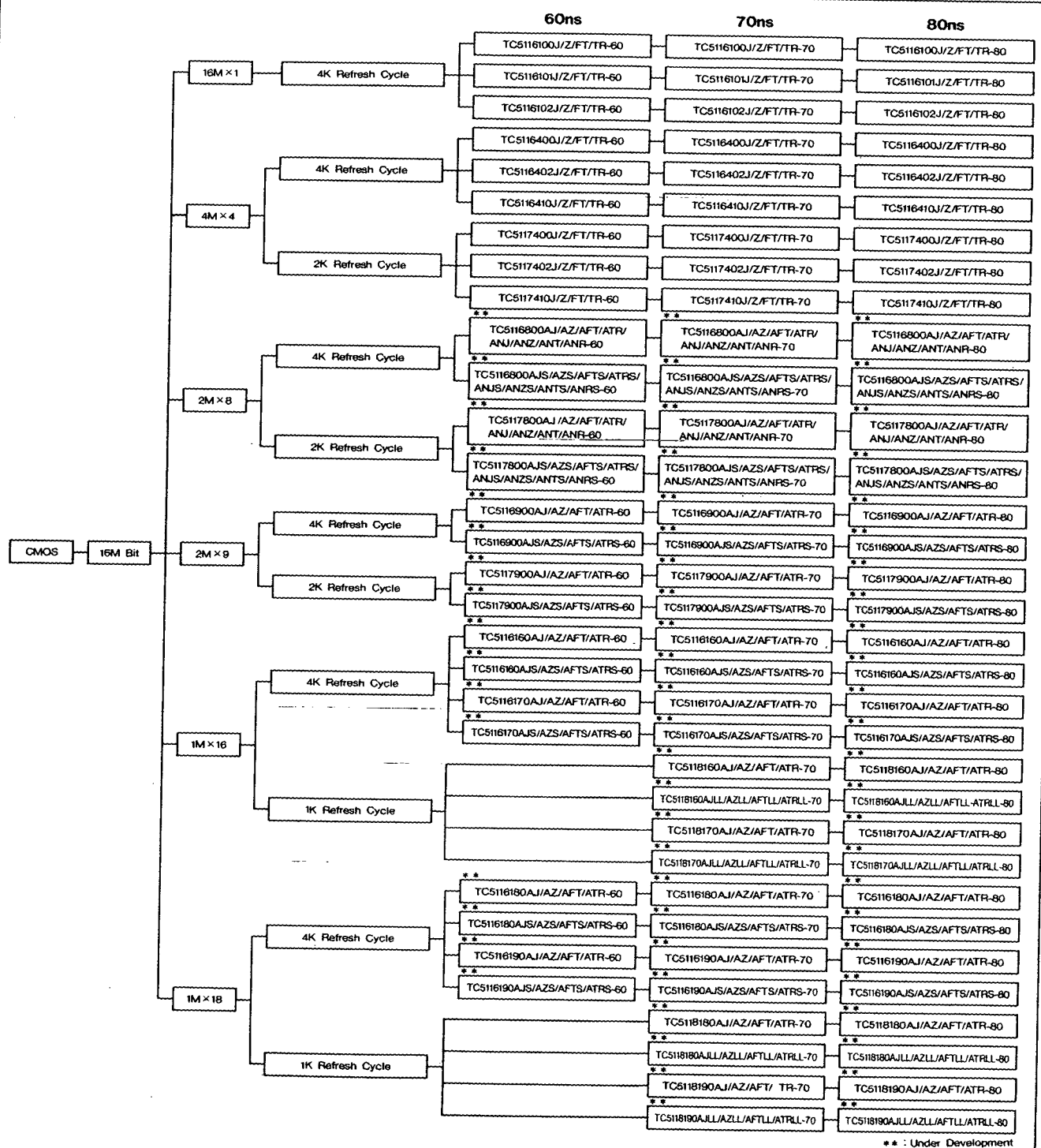
● 4M Dynamic RAM



4M Dynamic RAM (Continued)



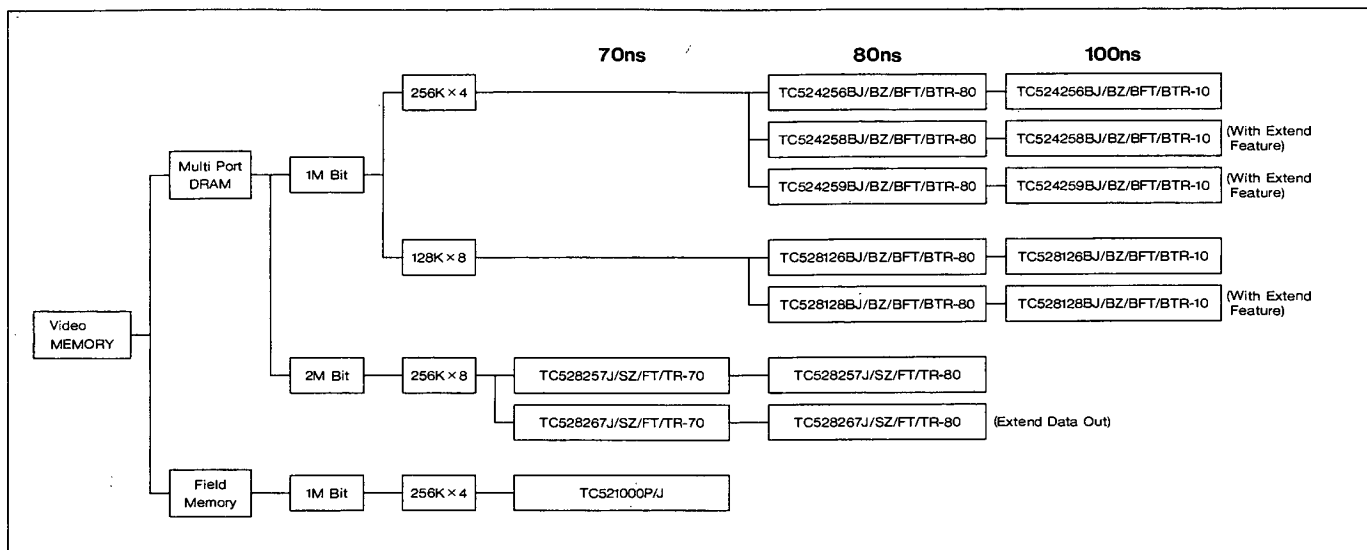
16M Dynamic RAM



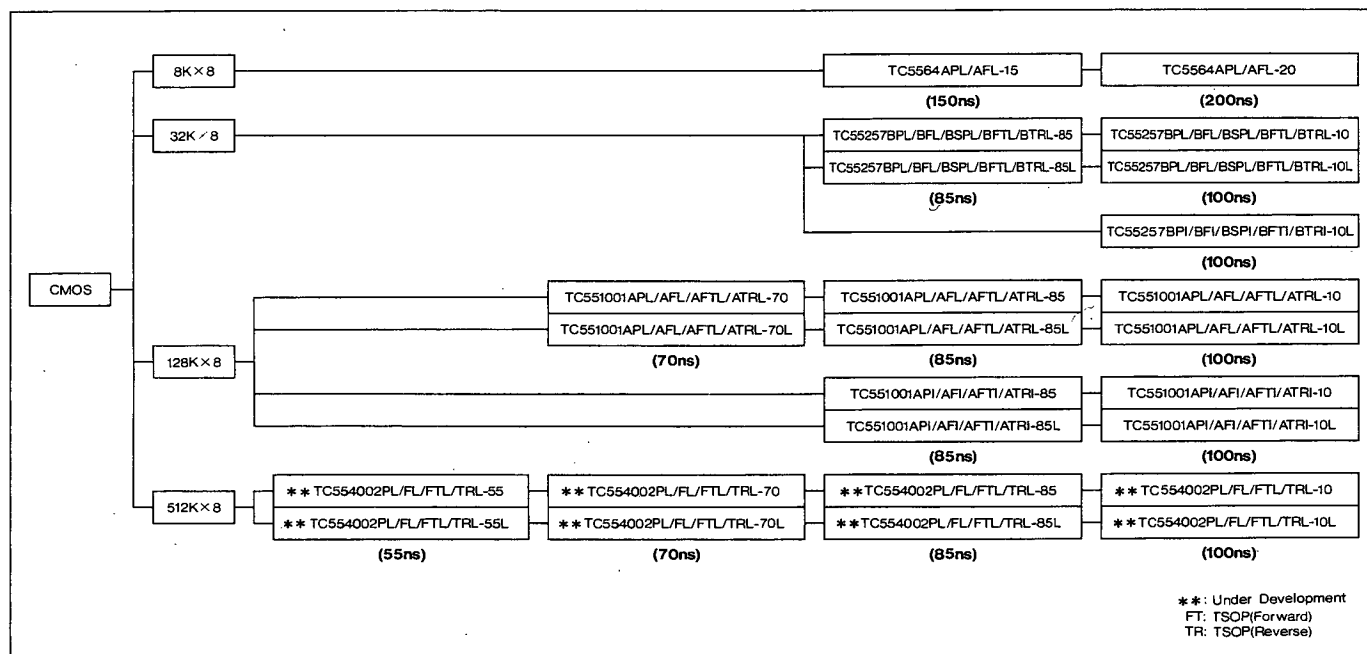
● Dynamic RAM Module

		60ns	70ns	80ns	100ns
1M DRAM Module	2M Bit	256K × 8 THM82500BS/BSG-60	THM82500AS/ASG-70	THM82500AS/ASG-80	THM82500AS/ASG-10
	4M Bit	256K × 9 THM92500BS/BSG-60	THM92500AS/ASG-70	THM92500AS/ASG-80	THM92500AS/ASG-10
		512K × 8 THM85100BS/BL-60	THM85100AS/AL-70	THM85100AS/AL-80	THM85100AS/AL-10
	8M Bit	1M × 8 THM81000BS/BL-60	THM81000AS/AL-70	THM81000AS/AL-80	THM81000AS/AL-10
		256K × 32 THM81020BL-80	THM81020AL-70	THM81020AL-80	THM81020AL-10
			THM322500BS/BSG-60	THM322500AS/ASG-70	THM322500AS/ASG-80
			THM322500BS/BSG-60	THM322500AS/ASG-70	THM322500AS/ASG-80
			THM91000BS/BSG/BL-60	THM91000AS/ASG/AL-70	THM91000AS/ASG/AL-80
			THM91000AS/ASG/AL-70	THM91000AS/ASG/AL-80	THM91000AS/ASG/AL-10
	9M Bit	1M × 9 THM91010BSG-80	THM91010ASG-70	THM91010ASG-80	THM91010ASG-10
			THM91020BL-80	THM91020AL-70	THM91020AL-80
			THM91020AL-70	THM91020AL-80	THM91020AL-10
			THM91050BS-60	THM91050AS-70	THM91050AS-80
			THM91050AS-70	THM91050AS-80	THM91050AS-10
		256K × 36 THM362500BS/BSG-60	THM362500AS/ASG-70	THM362500AS/ASG-80	THM362500AS/ASG-10
			THM362570BS/BSG-60	THM362570AS/ASG-70	THM362570AS/ASG-80
			THM362570AS/ASG-70	THM362570AS/ASG-80	THM362570AS/ASG-10
	10M Bit	256K × 40 THM402500BSG-60	THM402500ASG-70	THM402500ASG-80	THM402500ASG-10
			THM325120BS/BSG-60	THM325120AS/ASG-70	THM325120AS/ASG-80
			THM325120AS/ASG-70	THM325120AS/ASG-80	THM325120AS/ASG-10
	16M Bit	512K × 32 THM325140BSG-60	THM325140ASG-70	THM325140ASG-80	THM325140ASG-10
4M DRAM Module	8M Bit	512K × 36 THM365120BS/BSG-60	THM365120AS/ASG-70	THM365120AS/ASG-80	THM365120AS/ASG-10
			THM365140BSG-80	THM365140ASG-70	THM365140ASG-80
			THM365140ASG-70	THM365140ASG-80	THM365140ASG-10
	18M Bit	512K × 36 THM365160BS/BSG-60	THM365160AS/ASG-70	THM365160AS/ASG-80	THM365160AS/ASG-10
	20M Bit	512K × 40 THM405120BSG-60	THM405120ASG-70	THM405120ASG-80	THM405120ASG-10
	8M Bit	1M × 8 THM81070AS/AL-60	THM81070AS/AL-70	THM81070AS/AL-80	THM81070AS/AL-10
	9M Bit	1M × 9 THM91070AS/AL-60	THM91070AS/AL-70	THM91070AS/AL-80	THM91070AS/AL-10
	16M Bit	1M × 16 THM161000ASG-80	THM161000ASG-70	THM161000ASG-80	THM161000ASG-10
	18M Bit	1M × 18 THM181000ASG-80	THM181000ASG-70	THM181000ASG-80	THM181000ASG-10
	32M Bit	4M × 8 THM84000AS/ASG/AL-60	THM84000AS/ASG/AL-70	THM84000AS/ASG/AL-80	THM84000AS/ASG/AL-10
			THM84020AL-60	THM84020AL-70	THM84020AL-80
			THM84020AL-70	THM84020AL-80	THM84020AL-10
		1M × 32 THM321000AS/ASG-60	THM321000AS/ASG-70	THM321000AS/ASG-80	THM321000AS/ASG-10
			THM321090AS-60	THM321090AS-70	THM321090AS-80
			THM321090AS-70	THM321090AS-80	THM321090AS-10
	33M Bit	1M × 33 THM331000AS-60	THM331000AS-70	THM331000AS-80	THM331000AS-10
		4M × 9 THM94000AS/ASG/AL-80	THM94000AS/ASG/AL-70	THM94000AS/ASG/AL-80	THM94000AS/ASG/AL-10
			THM94020AL-60	THM94020AL-70	THM94020AL-80
			THM94020AL-70	THM94020AL-80	THM94020AL-10
	36M Bit	1M × 36 THM361000AS/ASG-60	THM361000AS/ASG-70	THM361000AS/ASG-80	THM361000AS/ASG-10
16M DRAM Module			THM361020AS/ASG-60	THM361020AS/ASG-70	THM361020AS/ASG-80
			THM361020AS/ASG-70	THM361020AS/ASG-80	THM361020AS/ASG-10
			THM361010AS/ASG-60	THM361010AS/ASG-70	THM361010AS/ASG-80
			THM361010AS/ASG-70	THM361010AS/ASG-80	THM361010AS/ASG-10
	40M Bit	1M × 40 THM401000ASG-60	THM401000ASG-70	THM401000ASG-80	THM401000ASG-10
		4M × 16 THM164020ASG-60	THM164020ASG-70	THM164020ASG-80	THM164020ASG-10
	64M Bit	2M × 32 THM322020AS/ASG-60	THM322020AS/ASG-70	THM322020AS/ASG-80	THM322020AS/ASG-10
			THM322080AS-60	THM322080AS-70	THM322080AS-80
			THM322080AS-70	THM322080AS-80	THM322080AS-10
		8M × 8 THM88020ATS-60	THM88020ATS-70	THM88020ATS-80	THM88020ATS-10
			THM88020ATS-70	THM88020ATS-80	THM88020ATS-10
		8M × 9 THM88020ATS-60	THM88020ATS-70	THM88020ATS-80	THM88020ATS-10
			THM88020ATS-70	THM88020ATS-80	THM88020ATS-10
	72M Bit	4M × 18 THM184020ASG-60	THM184020ASG-70	THM184020ASG-80	THM184020ASG-10
			THM362020AS/ASG-60	THM362020AS/ASG-70	THM362020AS/ASG-80
			THM362020AS/ASG-70	THM362020AS/ASG-80	THM362020AS/ASG-10
		2M × 36 THM362040AS/ASG-60	THM362040AS/ASG-70	THM362040AS/ASG-80	THM362040AS/ASG-10
			THM362060AS/ASG-60	THM362060AS/ASG-70	THM362060AS/ASG-80
			THM362060AS/ASG-70	THM362060AS/ASG-80	THM362060AS/ASG-10
	80M Bit	2M × 40 THM402020ASG-60	THM402020ASG-70	THM402020ASG-80	THM402020ASG-10
16M DRAM Module	128M Bit	4M × 32 THM324080AS/ASG-60	THM324080AS/ASG-70	THM324080AS/ASG-80	THM324080AS/ASG-10
	144M Bit	4M × 36 THM334080AS/ASG-60	THM334080AS/ASG-70	THM334080AS/ASG-80	THM334080AS/ASG-10
	160M Bit	4M × 40 THM334080AS/ASG-60	THM334080AS/ASG-70	THM334080AS/ASG-80	THM334080AS/ASG-10
	320M Bit	8M × 40 THM408020SG-60	THM408020SG-70	THM408020SG-80	THM408020SG-10

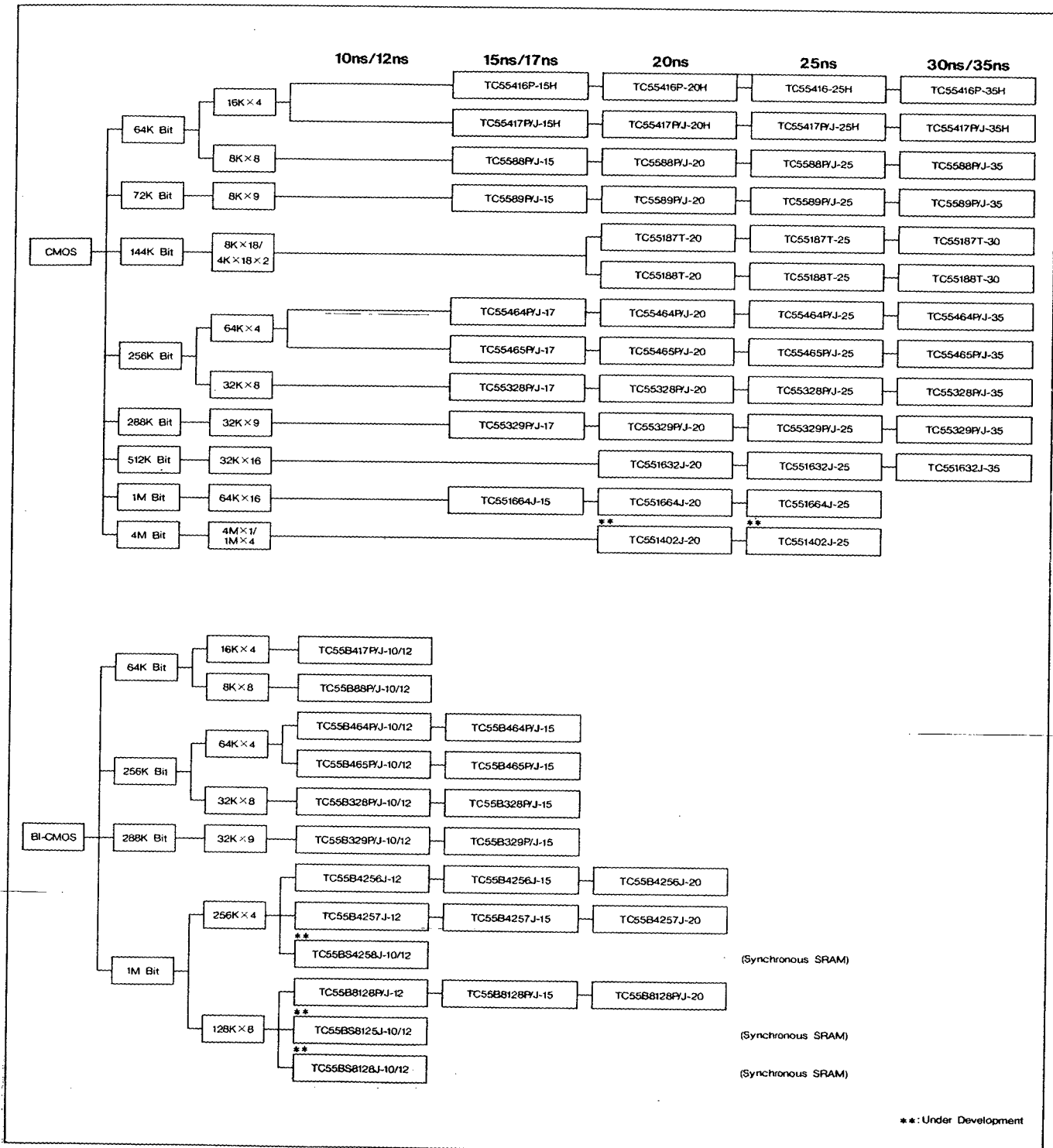
Video MEMORY



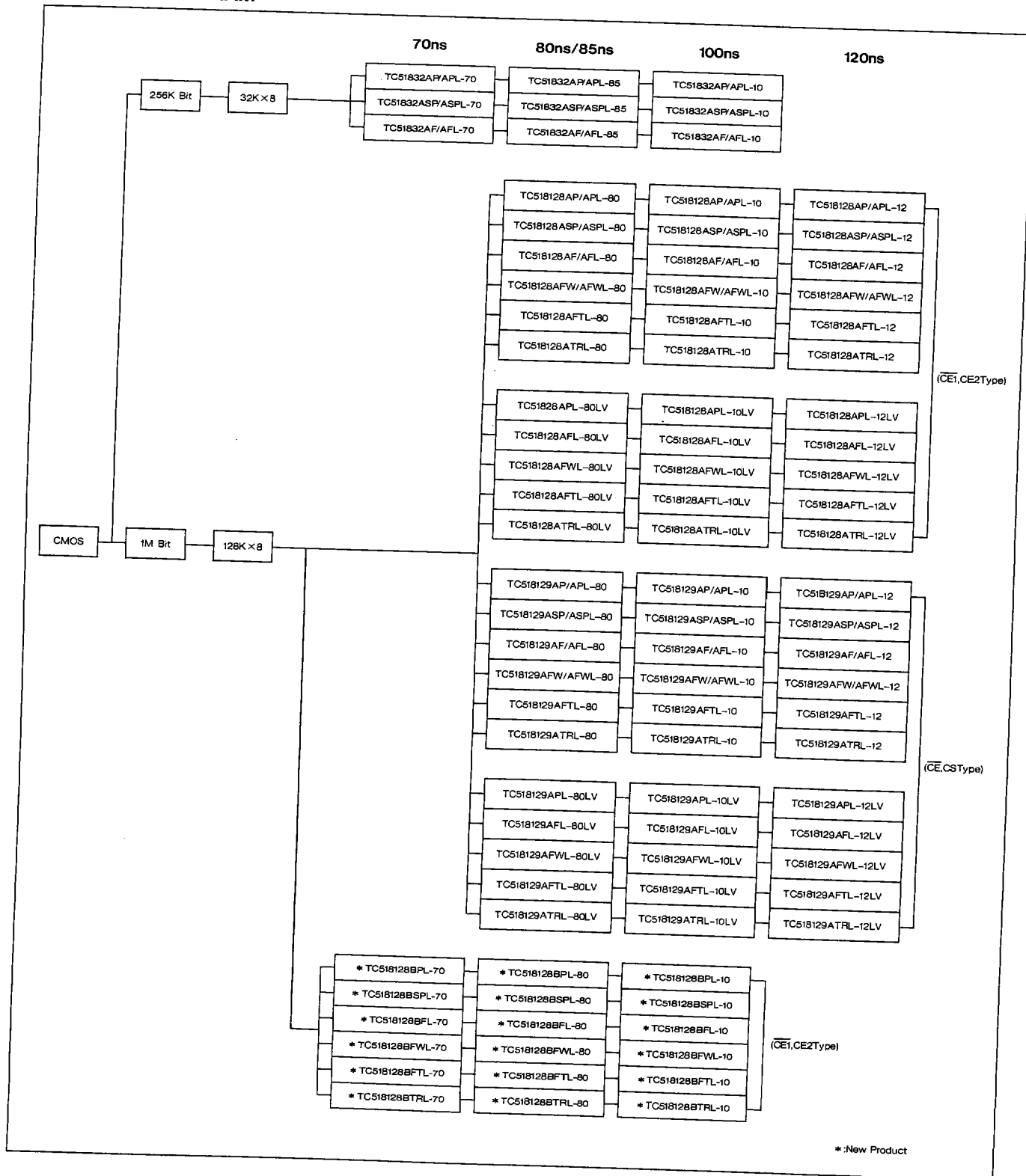
Static RAM

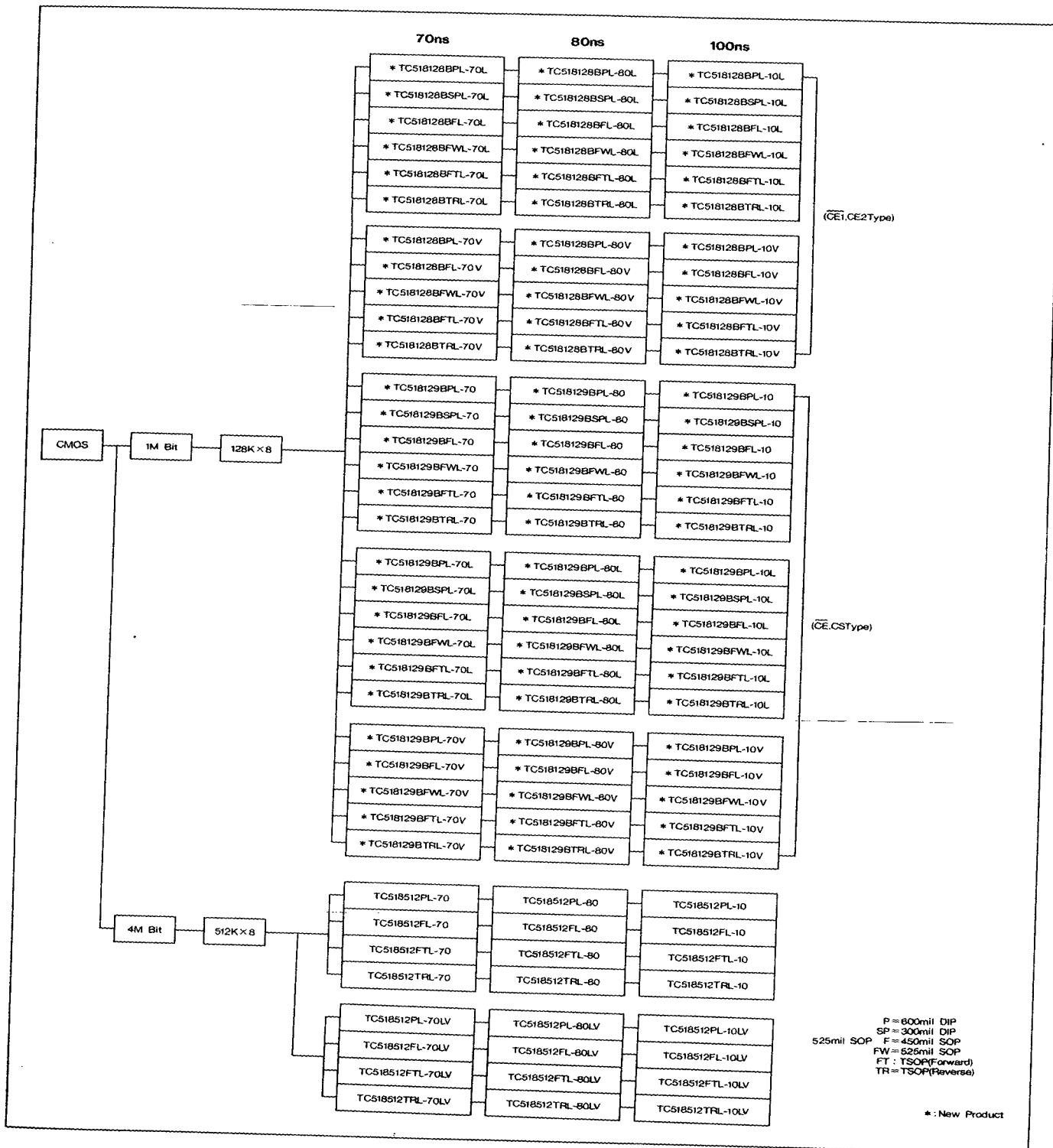


High Speed Static RAM

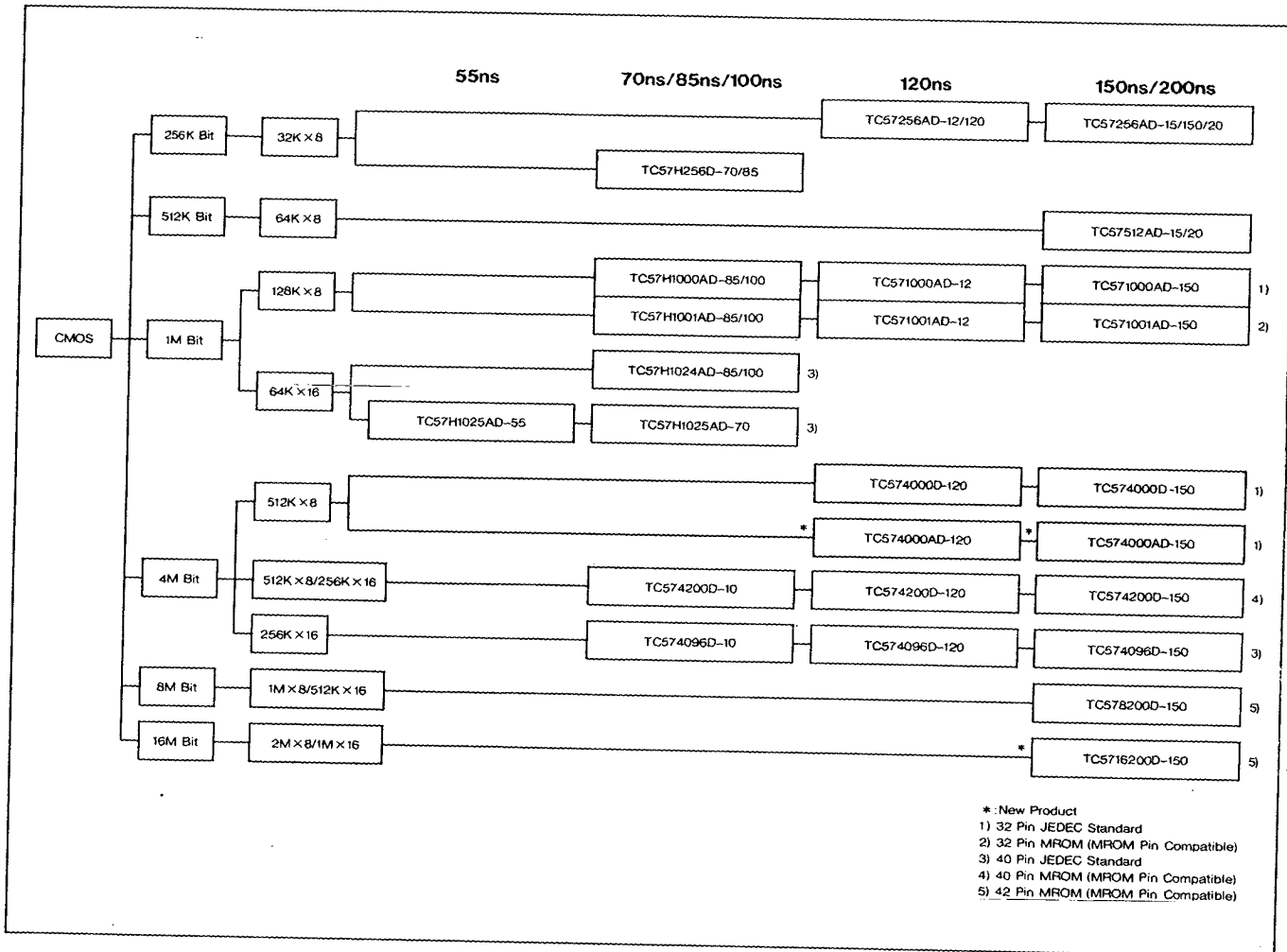


● Pseudo Static RAM

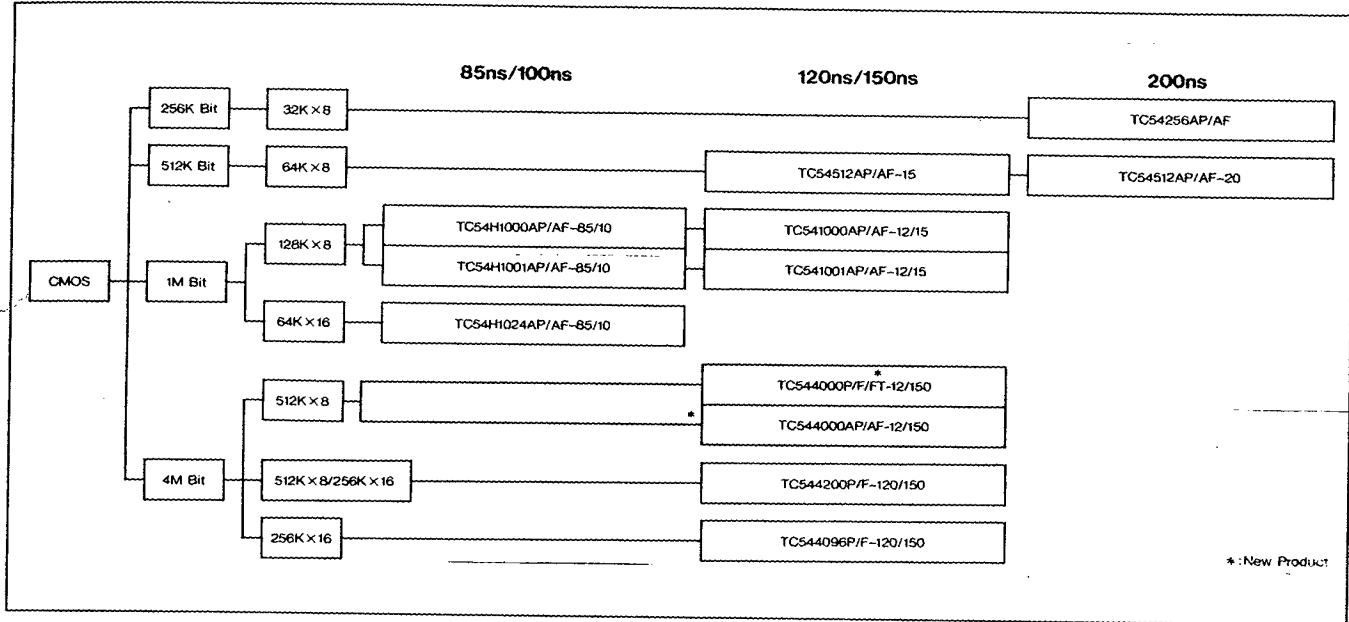




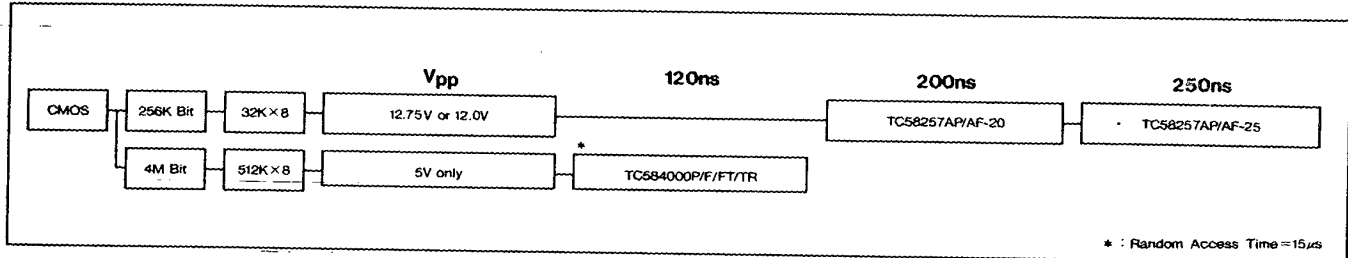
EPROM



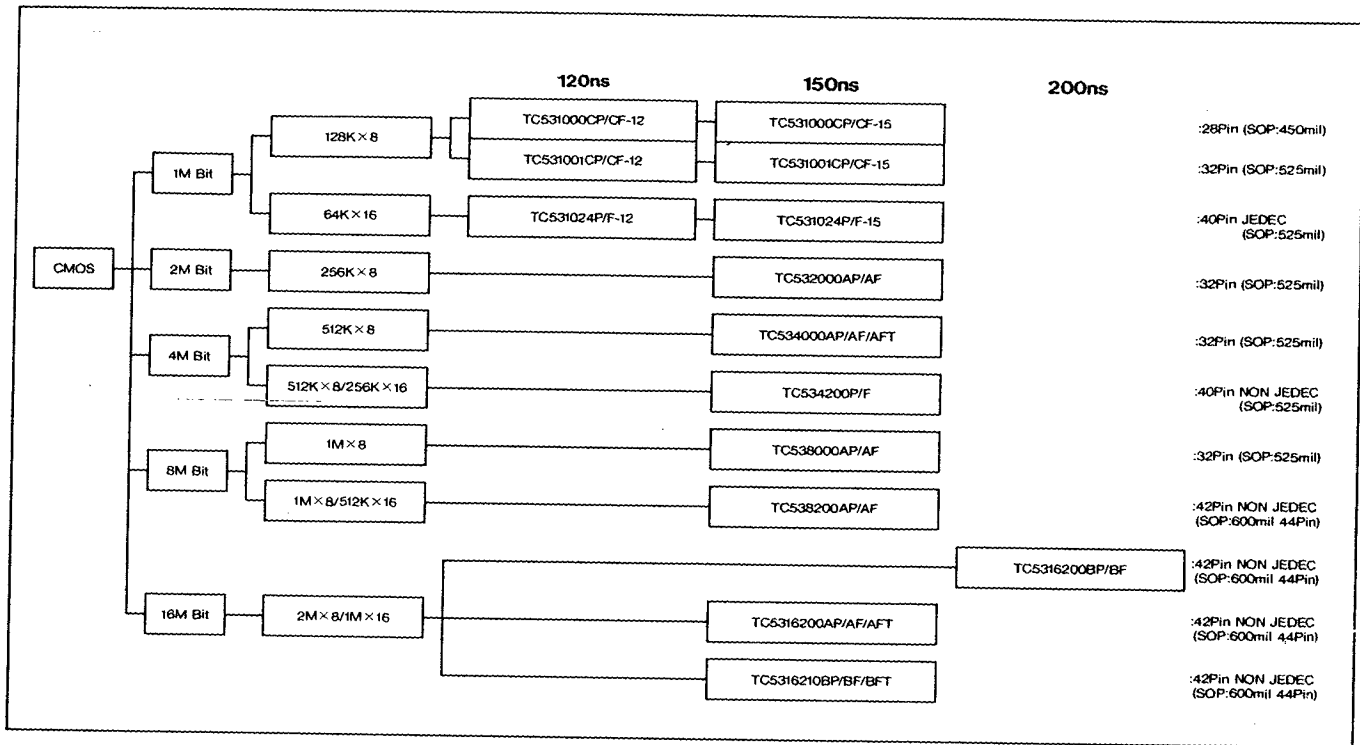
ONE TIME PROM



CMOS FLASH/NAND E²PROM



Mask ROM



CMOS Dynamic RAM

Capacity	Type No.	Organization	Max. Access Time (ns)			Min. Cycle Time (ns)	Power Supply (V)	Max. Power Dissipation (mW)		No. of Pins	Functional Mode
			t _{RAC}	t _{CAC}	t _{AA}			Active	Stand by		
	TC511000AP/AJ/AZ-70	1048576 × 1	70	20	35	130	5V ± 10%	440	5.5	18/26/20	Fast Page Mode
	TC511000AP/AJ/AZ-80		80	20	40	150		385			
	TC511000AP/AJ/AZ-10		100	25	50	180		330			
	TC511000APL/AJL/AZL-70		70	20	35	130		440	1.1 (200μA)		Fast Page Mode Low Power Version
	TC511000APL/AJL/AZL-80		80	20	40	150		385			
	TC511000APL/AJL/AZL-10		100	25	50	180		330			
	TC511001AP/AJ/AZ-70		70	20	35	130		440	5.5		Nibble Mode
	TC511001AP/AJ/AZ-80		80	20	40	150		385			
	TC511001AP/AJ/AZ-10		100	25	50	180		330			
	TC511002AP/AJ/AZ-70		70	20	35	130		440	Static Column Mode		
	TC511002AP/AJ/AZ-80		80	20	40	150		385			
	TC511002AP/AJ/AZ-10		100	25	50	180		330			
	TC511000BP/BJ/BZ/BFT/BTR-60		60	20	30	110		495	5.5	18/26/20/24/24	Fast Page Mode
	TC511000BFT/BTR-70		70	20	35	130		440			
	TC511000BFT/BTR-80		80	20	40	150		385			
	TC511000BFT/BTR-10		100	25	50	180		330	1.1 (200μA)	18/26/20/24/24	Fast Page Mode Low Power Version
	TC511000BPL/BJL/BZL/BFTL/BTRL-60		60	20	30	110		495			
	TC511000BFTL/BTRL-70		70	20	35	130		440			
	TC511000BFTL/BTRL-80		80	20	40	150		385			
	TC511000BFTL/BTRL-10		100	25	50	180		330			
	TC511001BP/BJ/BZ/BFT/BTR-60		60	20	30	110		495	5.5	18/26/20/24/24	Nibble Mode
	TC511001BFT/BTR-70		70	20	35	130		440			
	TC511001BFT/BTR-80		80	20	40	150		385			
	TC511001BFT/BTR-10		100	25	50	180		330	5.5	16/26/20/24/24	Static Column Mode
	TC511002BP/BJ/BZ/BFT/BTR-60		60	20	30	110		495			
	TC511002BFT/BTR-70		70	20	35	130		440	5.5	20/26/20	Fast Page Mode
	TC511002BFT/BTR-80		80	20	40	150		385			
	TC511002BFT/BTR-10		100	25	50	180		330			
TC514256AP/AJ/AZ-70	262144 × 4	70	20	35	130	440	5.5	20/26/20	Fast Page Mode		
TC514256AP/AJ/AZ-80		80	20	40	150	385					
TC514256AP/AJ/AZ-10		100	25	50	180	330					
TC514256APL/AJL/AZL-70		70	20	35	130	440	1.1 (200μA)		Fast Page Mode Low Power Version		
TC514256APL/AJL/AZL-80		80	20	40	150	385					
TC514256APL/AJL/AZL-10		100	25	50	180	330					
TC514258AP/AJ/AZ-70		70	25	35	130	440	5.5		Static Column Mode		
TC514258AP/AJ/AZ-80		80	25	40	150	385					
TC514258AP/AJ/AZ-10		100	30	50	180	330					
TC514266AP/AJ/AZ-70		70	20	35	130	440	Fast Page Mode Write Per Bit				
TC514266AP/AJ/AZ-80		80	20	40	150	385					
TC514266AP/AJ/AZ-10		100	25	50	180	330					
TC514256BP/BJ/BZ/BFT/BTR-60		60	20	30	110	495	5.5	20/26/20/24/24	Fast Page Mode		
TC514256BFT/BTR-70		70	20	35	130	440					
TC514256BFT/BTR-80		80	20	40	150	385					
TC514256BFT/BTR-10		100	25	50	180	330	1.1 (200μA)	20/26/20/24/24	Fast Page Mode Low Power Version		
TC514256BPL/BJL/BZL/BFTL/BTRL-60		60	20	30	110	495					
TC514256BFTL/BTRL-70		70	20	35	130	440					
TC514256BFTL/BTRL-80		80	20	40	150	385					
TC514256BFTL/BTRL-10		100	25	50	180	330					
TC514258BP/BJ/BZ/BFT/BTR/60		60	20	30	110	495	5.5	20/26/20/24/24	Static Column Mode		
TC514258BFT/BTR-70		70	25	35	130	440					
TC514258BFT/BTR-80		80	25	40	150	385					
TC514258BFT/BTR-10		100	30	50	180	330					
TC514266BP/BJ/BZ/BFT/BTR-80		60	20	30	110	495			Fast Page Mode Write Per Bit		
TC514266BFT/BTR-70		70	20	35	130	440					
TC514266BFT/BTR-80		80	20	40	150	385					
TC514266BFT/BTR-10		100	25	50	180	330					

Capacity	Type No.	Organization	Max. Access Time (ns)			Min. Cycle Time (ns)	Power Supply (V)	Max. Power Dissipation (mW)		No. of Pins	Functional Mode
			t _{RAC}	t _{CAC}	t _{AA}			Active	Stand by		
1M Bit	TC511664BJ/BZ/BFT/BTR-80	65536 × 16	80	30	45	135	5V ± 10%	633	5.5	40/40 44/44 TSOP-II 400mil (FT, TR)	Fast Page Mode
	TC511664BJ/BZ/BFT/BTR-10		100	35	55	170		495			
	TC511664BJL/BZL/BFTL/BTRL-80		80	30	45	135		633	1.7 (300 μA)		Fast Page Mode Byte Write Low Power Version
	TC511664BJL/BZL/BFTL/BTRL-10		100	35	55	170		495			
	TC511665BJ/BZ/BFT/BTR-80		80	30	45	135		633	5.5		Fast Page Mode Write Per Bit
	TC511665BJ/BZ/BFT/BTR-10		100	35	55	170		495			
	TC511665BJL/BZL/BFTL/BTRL-80		80	30	45	135		633	1.7 (300 μA)		Fast Page Mode Write Per Bit Low Power Version
	TC511665BJL/BZL/BFTL/BTRL-10		100	35	55	170		495			
4M Bit	TC514100AP/AJ/ASJ/AZ/AFT/ATR-60	4194304 × 1	60	20	30	110	5V ± 10%	660	5.5	18/26 26/20 26/26 TSOP-II 300mil (FT, TR)	Fast Page Mode
	TC514100AP/AJ/ASJ/AZ/AFT/ATR-70		70	20	35	130		550			
	TC514100AP/AJ/ASJ/AZ/AFT/ATR-80		80	20	40	150		468			
	TC514100AP/AJ/ASJ/AZ/AFT/ATR-10		100	25	50	180		413			
	TC514100APL/AJL/ASJL/AZL/AFTL/ATRL-60		60	20	30	110		660	1.1 (200 μA)		Fast Page Mode Low Power Version
	TC514100APL/AJL/ASJL/AZL/AFTL/ATRL-70		70	20	35	130		550			
	TC514100APL/AJL/ASJL/AZL/AFTL/ATRL-80		80	20	40	150		468			
	TC514100APL/AJL/ASJL/AZL/AFTL/ATRL-10		100	25	50	180		413			
	TC514101AP/AJ/ASJ/AZ/AFT/ATR-60		60	20	30	110		660	5.5		Nibble Mode
	TC514101AP/AJ/ASJ/AZ/AFT/ATR-70		70	20	35	130		550			
	TC514101AP/AJ/ASJ/AZ/AFT/ATR-80		80	20	40	150		468			
	TC514101AP/AJ/ASJ/AZ/AFT/ATR-10		100	25	50	180		413			
	TC514102AP/AJ/ASJ/AZ/AFT/ATR-60		60	20	30	110		660	5.5		Static Column Mode
	TC514102AP/AJ/ASJ/AZ/AFT/ATR-70		70	20	35	130		550			
	TC514102AP/AJ/ASJ/AZ/AFT/ATR-80		80	20	40	150		468			
	TC514102AP/AJ/ASJ/AZ/AFT/ATR-10		100	25	50	180		413			
	* TC514100BSJ/BZ/BFT/BTR-50		50	15	25	95		550	5.5		Fast Page Mode
	* TC514100BSJ/BZ/BFT/BTR-60		60	15	30	110		440			Nibble Mode
	* TC514101BSJ/BZ/BFT/BTR-60		60	15	30	110		440			Static Column Mode
	* TC514102BSJ/BZ/BFT/BTR-60		60	15	30	110		440			
	TC514400AP/AJ/ASJ/AZ/AFT/ATR-60		60	20	30	110		660	5.5		Fast Page Mode
	TC514400AP/AJ/ASJ/AZ/AFT/ATR-70		70	20	35	130		550			
	TC514400AP/AJ/ASJ/AZ/AFT/ATR-80		80	20	40	150		468			
	TC514400AP/AJ/ASJ/AZ/AFT/ATR-10		100	25	50	180		413			
	TC514400APL/AJL/ASJL/AZL/AFTL/ATRL-60		60	20	30	110		660	1.1 (200 μA)		Fast Page Mode Low Power Version
	TC514400APL/AJL/ASJL/AZL/AFTL/ATRL-70		70	20	35	130		550			
	TC514400APL/AJL/ASJL/AZL/AFTL/ATRL-80		80	20	40	150		468			
	TC514400APL/AJL/ASJL/AZL/AFTL/ATRL-10		100	25	50	180		413			
	TC514402AP/AJ/ASJ/AZ/AFT/ATR-60		60	20	30	110		660	5.5		Static Column Mode
	TC514402AP/AJ/ASJ/AZ/AFT/ATR-70		70	20	35	130		550			
	TC514402AP/AJ/ASJ/AZ/AFT/ATR-80		80	20	40	150		468			
	TC514402AP/AJ/ASJ/AZ/AFT/ATR-10		100	25	50	180		413			
	TC514410AP/AJ/ASJ/AZ/AFT/ATR-60		60	20	30	110		660	5.5		Fast Page Mode Write Per Bit
	TC514410AP/AJ/ASJ/AZ/AFT/ATR-70		70	20	35	130		550			
	TC514410AP/AJ/ASJ/AZ/AFT/ATR-80		80	20	40	150		468			
	TC514410AP/AJ/ASJ/AZ/AFT/ATR-10		100	25	50	180		413			
	* TC514400BSJ/BZ/BFT/BTR-50		50	15	25	95		550	5.5		Fast Page Mode
	* TC514400BSJ/BZ/BFT/BTR-60		60	15	30	110		440			Static Column Mode
	* TC514402BSJ/BZ/BFT/BTR-60		60	15	30	110		440			Fast Page Mode Write Per Bit
	* TC514410BSJ/BZ/BFT/BTR-60		60	15	30	110		440			

Capacity	Type No.	Organization	Max. Access Time (ns)			Min. Cycle Time (ns)	Power Supply (V)	Max. Power Dissipation (mW)		No. of Pins	Functional Mode
			t _{RAC}	t _{CAC}	t _{AA}			Active	Stand by		
4M Bit	TC514800AJ/AZ/AFT/ATR-70	524288 × 8	70	20	35	130	5V ± 10%	578	5.5	28/28 TSOP-II 400mil (FT, TR)	Fast Page Mode
	TC514800AJ/AZ/AFT/ATR-80		80	20	40	150		495			
	TC514800AJ/AZ/AFT/ATR-10		100	25	50	180		440	1.1 (200μA)	28/28 TSOP-II 400mil (FT, TR)	Fast Page Mode Low Power Version
	TC514800AJL/AZL/AFTL/ATRL-70		70	20	35	130		578			
	TC514800AJL/AZL/AFTL/ATRL-80		80	20	40	150		495	1.1 (200μA)	28/28 TSOP-II 400mil (FT, TR)	Fast Page Mode Low Power Self Refresh
	TC514800AJL/AZL/AFTL/ATRL-10		100	25	50	180		440			
	TC514800AJLL/AZLL/AFTLL/ATRL-70		70	20	35	130		578	1.1 (200μA)	28/28 TSOP-II 400mil (FT, TR)	Fast Page Mode Low Power Self Refresh
	TC514800AJLL/AZLL/AFTLL/ATRL-80		80	20	40	150		495			
	TC514800AJLL/AZLL/AFTLL/ATRL-10		100	25	50	180		440			
	TC514900AJ/AZ/AFT/ATR-70	524288 × 9	70	20	35	130	5V ± 10%	633	5.5	28/28 TSOP-II 400mil (FT, TR)	Fast Page Mode
	TC514900AJ/AZ/AFT/ATR-80		80	20	40	150		550			
	TC514900AJ/AZ/AFT/ATR-10		100	25	50	180		495	1.1 (200μA)	28/28 TSOP-II 400mil (FT, TR)	Fast Page Mode Low Power Version
	TC514900AJL/A/AFTL/ATRL-70		70	20	35	130		633			
	TC514900AJL/A/AFTL/ATRL-80		80	20	40	150		550	1.1 (200μA)	28/28 TSOP-II 400mil (FT, TR)	Fast Page Mode Low Power Self Refresh
	TC514900AJL/A/AFTL/ATRL-10		100	25	50	180		495			
	TC514900AJLL/AZLL/AFTLL/ATRL-70		70	20	35	130		633	1.1 (200μA)	28/28 TSOP-II 400mil (FT, TR)	Fast Page Mode Low Power Self Refresh
	TC514900AJLL/AZLL/AFTLL/ATRL-80		80	20	40	150		550			
	TC514900AJLL/AZLL/AFTLL/ATRL-10		100	25	50	180		495			
	*TC514170BJ/BZ/BFT/BTR-70	262144 × 16	70	20	35	130	5V ± 10%	413	5.5	40/40 44/44 TSOP-II 400mil (FT, TR)	Fast Page Mode 1024 Refresh Cycle
	*TC514170BJ/BZ/BFT/BTR-80		80	20	40	150		358			
	*TC514170BJ/BZ/BFT/BTR-10		100	25	50	180		330	5.5	40/40 44/44 TSOP-II 400mil (FT, TR)	Fast Page Mode 512 Refresh Cycle
	*TC514260BJ/BZ/BFT/BTR-70		70	20	35	130		550			
	*TC514260BJ/BZ/BFT/BTR-80		80	20	40	150		468	1.1 (200μA)	40/40 44/44 TSOP-II 400mil (FT, TR)	Fast Page Mode Low Power Version 512 Refresh Cycle
	*TC514260BJ/BZ/BFT/BTR-10		100	25	50	180		413			
	*TC514260BJL/BZL/BFTL/BTRL-70		70	20	35	130		550	1.1 (200μA)	40/40 44/44 TSOP-II 400mil (FT, TR)	Fast Page Mode Low Power Self Refresh 512 Refresh Cycle
	*TC514260BJL/BZL/BFTL/BTRL-80		80	20	40	150		468			
	*TC514260BJL/BZL/BFTL/BTRL-10		100	25	50	180		413	5.5	40/40 44/44 TSOP-II 400mil (FT, TR)	Fast Page Mode Write Per Bit 512 Refresh Cycle
	*TC514273BJ/BZ/BFT/BTR-70		70	20	35	130		550			
	*TC514273BJ/BZ/BFT/BTR-80		80	20	40	150		468	5.5	40/40 44/44 TSOP-II 400mil (FT, TR)	Fast Page Mode Write Per Bit 512 Refresh Cycle
	*TC514273BJ/BZ/BFT/BTR-10		100	25	50	180		413			
	*TC514190BJ/BZ/BFT/BTR-70	262144 × 18	70	20	35	130	5V ± 10%	468	5.5	40/40 44/44 TSOP-II 400mil (FT, TR)	Fast Page Mode Write Per Bit 512 Refresh Cycle
	*TC514190BJ/BZ/BFT/BTR-80		80	20	40	150		413			
	*TC514190BJ/BZ/BFT/BTR-10		100	25	50	180		385	5.5	40/40 44/44 TSOP-II 400mil (FT, TR)	Fast Page Mode Low Power Self Refresh 1024 Refresh Cycle
	*TC514280BJ/BZ/BFT/BTR-70		70	20	35	130		605			
	*TC514280BJ/BZ/BFT/BTR-80		80	20	40	150		523	1.1 (200μA)	40/40 44/44 TSOP-II 400mil (FT, TR)	Fast Page Mode 512 Refresh Cycle
	*TC514280BJ/BZ/BFT/BTR-10		100	25	50	180		468			
	*TC514280BJL/BZL/BFTL/BTRL-70		70	20	35	130		605	1.1 (200μA)	40/40 44/44 TSOP-II 400mil (FT, TR)	Fast Page Mode Low Power Version 512 Refresh Cycle
	*TC514280BJL/BZL/BFTL/BTRL-80		80	20	40	150		523			
	*TC514280BJL/BZL/BFTL/BTRL-10		100	25	50	180		468	1.1 (200μA)	40/40 44/44 TSOP-II 400mil (FT, TR)	Fast Page Mode Low Power Version 512 Refresh Cycle
	*TC514280BJLL/BZLL/BFTLL/BTRL-70		70	20	35	130		605			
	*TC514280BJLL/BZLL/BFTLL/BTRL-80		80	20	40	150		523			
	*TC514280BJLL/BZLL/BFTLL/BTRL-10		100	25	50	180		468			

Capacity	Type No.	Organization	Max. Access Time (ns)			Min. Cycle Time (ns)	Power Supply (V)	Max. Power Dissipation (mW)		No. of Pins	Functional Mode		
			t _{TRAC}	t _{CAC}	t _{AA}			Active	Stand by				
16M Bit	TC5116100J/Z/FT/TR-60	16777216 × 1	60	15	30	110	5V ± 10%	495	5.5	28/24 28/24 TSOP-II 400mil (FT, TR)	Fast Page Mode 4K Refresh Cycle		
	TC5116100J/Z/FT/TR-70		70	20	35	130		440			Nibble Mode 4K Refresh Cycle		
	TC5116100J/Z/FT/TR-80		80	20	40	150		385					
	TC5116101J/Z/FT/TR-60		60	15	30	110		495			Static Column Mode 4K Refresh Cycle		
	TC5116101J/Z/FT/TR-70		70	20	35	130		440					
	TC5116101J/Z/FT/TR-80		80	20	40	150		385					
	TC5116102J/Z/FT/TR-60		60	15	30	110		495			Fast Page Mode 4K Refresh Cycle		
	TC5116102J/Z/FT/TR-70		70	20	35	130		440					
	TC5116102J/Z/FT/TR-80		80	20	40	150		385			Static Column Mode 4K Refresh Cycle		
	TC5116400J/Z/FT/TR-60		60	15	30	110		495					
	TC5116400J/Z/FT/TR-70		70	20	35	130		440			Fast Page Mode 4K Refresh Cycle		
	TC5116400J/Z/FT/TR-80		80	20	40	150		385					
	TC5116402J/Z/FT/TR-60	4194304 × 4	60	15	30	110	5V ± 10%	495	5.5	28/24 28/24 TSOP-II 400mil (FT, TR)	Static Column Mode 4K Refresh Cycle		
	TC5116402J/Z/FT/TR-70		70	20	35	130		440					
	TC5116402J/Z/FT/TR-80		80	20	40	150		385			Fast Page Mode Write Per Bit 4K Refresh Cycle		
	TC5116410J/Z/FT/TR-60		60	15	30	110		495					
	TC5116410J/Z/FT/TR-70		70	20	35	130		440			Fast Page Mode 2K Refresh Cycle		
	TC5116410J/Z/FT/TR-80		80	20	40	150		385					
	TC5117400J/Z/FT/TR-60		60	15	30	110		715			5.5		Static Column Mode 2K Refresh Cycle
	TC5117400J/Z/FT/TR-70		70	20	35	130		805					
	TC5117400J/Z/FT/TR-80		80	20	40	150		523			5.5		Fast Page Mode Write Per Bit 2K Refresh Cycle
	TC5117402J/Z/FT/TR-60		60	15	30	110		715					
	TC5117402J/Z/FT/TR-70		70	20	35	130		805			5.5		Fast Page Mode Write Per Bit 2K Refresh Cycle
	TC5117402J/Z/FT/TR-80		80	20	40	150		523					
	TC5117410J/Z/FT/TR-60		60	15	30	110		715			5.5		Fast Page Mode Write Per Bit 2K Refresh Cycle
	TC5117410J/Z/FT/TR-70		70	20	35	130		805					
	TC5117410J/Z/FT/TR-80		80	20	40	150		523					
	***TC5116800AJ/AZ/AFT/ATR/ANR-60	2097152 × 8	60	15	30	110	5V ± 10%	495	1.1 (200μA)	32/32/32/32 28/28/28/28 TSOP-II 400mil (FT, TR)	Fast Page Mode 4K Refresh		
	***TC5116800AJ/AZ/AFT/ATR/ANR-70		70	20	35	130		413					
	***TC5116800AJ/AZ/AFT/ATR/ANR-80		80	20	40	150		358			Fast Page Mode Self Refresh 4K Refresh		
	***TC5116900AJ/AZ/AFT/ATR/ANR-60		60	15	30	110		495				1.1 (200μA)	
	***TC5116900AJ/AZ/AFT/ATR/ANR-70		70	20	35	130		413			Fast Page Mode 2K Refresh		
	***TC5116900AJ/AZ/AFT/ATR/ANR-80		80	20	40	150		358				5.5	
	***TC5117800AJ/AZ/AFT/ATR/ANR-60		60	15	30	110		633			Fast Page Mode Self Refresh 2K Refresh		
	***TC5117800AJ/AZ/AFT/ATR/ANR-70		70	20	35	130		523				1.1 (200μA)	
	***TC5117800AJ/AZ/AFT/ATR/ANR-80		80	20	40	150		440			Fast Page Mode 4K Refresh		
	***TC5117900AJ/AZ/AFT/ATR-60		60	15	30	110		633				1.1 (200μA)	
	***TC5117900AJ/AZ/AFT/ATR-70		70	20	35	130		523			Fast Page Mode Self Refresh 2K Refresh		
	***TC5117900AJ/AZ/AFT/ATR-80		80	20	40	150		440				5.5	
	***TC5116900AJ/AZ/AFT/ATR-60	2097152 × 9	60	15	30	110	5V ± 10%	550	1.1 (200μA)	32/32 32/32 TSOP-II 400mil (FT, TR)	Fast Page Mode 4K Refresh		
	***TC5116900AJ/AZ/AFT/ATR-70		70	20	35	130		468					
	***TC5116900AJ/AZ/AFT/ATR-80		80	20	40	150		413			Fast Page Mode Self Refresh 4K Refresh		
	***TC5116900AJ/AZ/AFT/ATR-60		60	15	30	110		550				1.1 (200μA)	
	***TC5116900AJ/AZ/AFT/ATR-70		70	20	35	130		468			Fast Page Mode 2K Refresh		
	***TC5116900AJ/AZ/AFT/ATR-80		80	20	40	150		413				5.5	
	***TC5117900AJ/AZ/AFT/ATR-60		60	15	30	110		688			Fast Page Mode Self Refresh 2K Refresh		
	***TC5117900AJ/AZ/AFT/ATR-70		70	20	35	130		578				1.1 (200μA)	
	***TC5117900AJ/AZ/AFT/ATR-80		80	20	40	150		495			Fast Page Mode Self Refresh 2K Refresh		
	***TC5117900AJ/AZ/AFT/ATR-60		60	15	30	110		688				1.1 (200μA)	
	***TC5117900AJ/AZ/AFT/ATR-70		70	20	35	130		578					
	***TC5117900AJ/AZ/AFT/ATR-80		80	20	40	150		495					

Capacity	Type No.	Organization	Max. Access Time (ns)			Min. Cycle Time (ns)	Power Supply (V)	Max. Power Dissipation (mW)		No. of Pins	Functional Mode	
			t _{RAC}	t _{CAC}	t _{AA}			Active	Stand by			
16M Bit	**TC5116160AJ/AZ/AFT/ATR-60	1048576 × 16	60	15	30	110	5V ± 10%	523	5.5	42/42 50/50 TSOP-II 400mil (FT, TR)	2CAS, 1WE Fast Page Mode 4K Refresh	
	**TC5116160AJ/AZ/AFT/ATR-70		70	20	35	130		440				
	**TC5116160AJ/AZ/AFT/ATR-80		80	20	40	150		385				
	**TC5116160AJ/AZS/AFTS/ATRS-60		60	15	30	110		523	1.1 (200μA)		2CAS, 1WE Fast Page Mode Self Refresh 4K Refresh	
	**TC5116160AJ/AZS/AFTS/ATRS-70		70	20	35	130		440				
	**TC5116160AJ/AZS/AFTS/ATRS-80		80	20	40	150		385				
	**TC5116170AJ/AZ/AFT/ATR-60		60	15	30	110		523	5.5		1CAS, 2WE Fast Page Mode 4K Refresh	
	**TC5116170AJ/AZ/AFT/ATR-70		70	20	35	130		440				
	**TC5116170AJ/AZ/AFT/ATR-80		80	20	40	150		385				
	**TC5116170AJ/AZS/AFTS/ATRS-60		60	15	30	110		523	1.1 (200μA)		1CAS, 2WE Fast Page Mode Self Refresh 4K Refresh	
	**TC5116170AJ/AZS/AFTS/ATRS-70		70	20	35	130		440				
	**TC5116170AJ/AZS/AFTS/ATRS-80		80	20	40	150		385				
	**TC5118160AJ/AZ/AFT/ATR-70		70	20	35	130		770	5.5		1CAS, 1WE Fast Page Mode 1K Refresh	
	**TC5118160AJ/AZ/AFT/ATR-80		80	20	40	150		660				
	**TC5118160AJ/AZLL/AFTLL/ATRL-70		70	20	35	130		770				
	**TC5118160AJ/AZLL/AFTLL/ATRL-80		80	20	40	150		660	1.1 (200μA)		2CAS, 1WE Fast Page Mode Self Refresh 1K Refresh	
	**TC5118170AJ/AZ/AFT/ATR-70		70	20	35	130		770				
	**TC5118170AJ/AZ/AFT/ATR-80		80	20	40	150		660				
	**TC5118170AJ/AZS/AFTS/ATRS-60		60	15	30	110		523	5.5		1CAS, 2WE Fast Page Mode 1K Refresh	
	**TC5118170AJ/AZS/AFTS/ATRS-70		70	20	35	130		440				
	**TC5118170AJ/AZS/AFTS/ATRS-80		80	20	40	150		385				
	**TC5118170AJ/AZLL/AFTLL/ATRL-70		70	20	35	130		770	1.1 (200μA)		1CAS, 2WE Fast Page Mode Self Refresh 1K Refresh	
	**TC5118170AJ/AZLL/AFTLL/ATRL-80		80	20	40	150		660				
	**TC5116180AJ/AZ/AFT/ATR-60		60	15	30	110		578				5.5
	**TC5116180AJ/AZ/AFT/ATR-70	70	20	35	130	495						
	**TC5116180AJ/AZ/AFT/ATR-80	80	20	40	150	440						
	**TC5116180AJ/AZS/AFTS/ATRS-60	60	15	30	110	578	1.1 (200μA)		2CAS, 1WE Fast Page Mode Self Refresh 4K Refresh			
	**TC5116180AJ/AZS/AFTS/ATRS-70	70	20	35	130	495						
	**TC5116180AJ/AZS/AFTS/ATRS-80	80	20	40	150	440						
	**TC5116190AJ/AZ/AFT/ATR-60	60	15	30	110	578	5.5		1CAS, 2WE Fast Page Mode 4K Refresh			
	**TC5116190AJ/AZ/AFT/ATR-70	70	20	35	130	495						
	**TC5116190AJ/AZ/AFT/ATR-80	80	20	40	150	440						
	**TC5116190AJ/AZS/AFTS/ATRS-60	60	15	30	110	578	1.1 (200μA)		1CAS, 2WE Fast Page Mode Self Refresh 4K Refresh			
	**TC5116190AJ/AZS/AFTS/ATRS-70	70	20	35	130	495						
	**TC5116190AJ/AZS/AFTS/ATRS-80	80	20	40	150	440						
	**TC5118180AJ/AZ/AFT/ATR-70	70	20	35	130	825	5.5		2CAS, 1WE Fast Page Mode 1K Refresh			
	**TC5118180AJ/AZ/AFT/ATR-80	80	20	40	150	715						
	**TC5118180AJ/AZLL/AFTLL/ATRL-70	70	20	35	130	825						
	**TC5118180AJ/AZLL/AFTLL/ATRL-80	80	20	40	150	715	1.1 (200μA)		2CAS, 1WE Fast Page Mode Self Refresh 1K Refresh			
	**TC5118190AJ/AZ/AFT/ATR-70	70	20	35	130	825						
	**TC5118190AJ/AZ/AFT/ATR-80	80	20	40	150	715						
	**TC5118190AJ/AZS/AFTS/ATRS-60	60	15	30	110	578	5.5		1CAS, 2WE Fast Page Mode 1K Refresh			
	**TC5118190AJ/AZS/AFTS/ATRS-70	70	20	35	130	495						
	**TC5118190AJ/AZS/AFTS/ATRS-80	80	20	40	150	440						
	**TC5118190AJ/AZLL/AFTLL/ATRL-70	70	20	35	130	825	1.1 (200μA)		1CAS, 2WE Fast Page Mode Self Refresh 1K Refresh			
	**TC5118190AJ/AZLL/AFTLL/ATRL-80	80	20	40	150	715						

P: Plastic DIP, T: PLCC, J: SOJ, Z: ZIP, FT: TSOP (Forward), TR: TSOP (Reverse)

* : New Product
** : Under Development

● Dynamic RAM Module

Capacity	Type No.	Organization	Access Time	No. of Pins	Assembly (mm)			Comment									
					Height	Length	Width										
2M Bit	THM825000BS/BSG-60/AS/ASG-70/80/10	256K×8	T _{RAC} -60: 60ns -70: 70ns -80: 80ns -10: 100ns	30	17.9	88.9	5.08	USE 1MDRAM									
4M Bit	THM925000BS/BSG-60/AS/ASG-70/80/10	256K×9			15.24/17.52	88.9/82.14	With OE										
	THM851000BS/BL-60/AS/AL-70/80/10	512K×8			20.45/22.60	88.9/76.5											
8M Bit	THM81000BS/BL-60/AS/AL-70/80/10	1M×8			12.64	76.5	8.89	Low THM81000AL									
	THM322500BS/BSG-60/AS/ASG-70/80/10	256K×32		72	25.40	107.95	5.08	With OE									
9M Bit	THM322590BS-60/AS-70/80/10			1M×9	30	20.45/20.45/22.60	88.9/88.9/82.14	8.89	Low THM91000AL								
	THM91020BL-60/AL-70/80/10	12.64			88.9	5.08	Common 9I/O With Test Mode ×36 bit ECC Module										
	THM91010BSG-60/ASG-70/80/10	20.45															
	THM91050BS-60/AS-70/80/10	20.45															
	THM362500BS/BSG-60/AS/ASG-70/80/10	256K×36			72	25.40	107.95	8.89	8CAS pins type With OE 8CAS pins type ×36 bit ECC Module								
	THM362570BS/BSG-60/AS/ASG-70/80/10																
10M Bit	THM402500BS/BSG-60/AS/ASG-70/80/10	256K×40															
16M Bit	THM325120BS/BSG-60/AS/ASG-70/80/10	512K×32															
	THM325140BSG-60/ASG-70/80/10																
	THM325180BS-60/AS-70/80/10																
18M Bit	THM365120BS/BSG-60/AS/ASG-70/80/10	512K×36															
	THM365140BSG-60/ASG-70/80/10																
	THM365160BS/BSG-60/AS/ASG-70/80/10																
20M Bit	THM405120BS/BSG-60/AS/ASG-70/80/10	512K×40		T _{RAC} -60: 60ns -70: 70ns -80: 80ns -10: 100ns	30	15.24/17.52	88.9/76.5	5.08	Low THM84000AL								
8M Bit	THM81070AS/AL-60/70/80/10	1M×8															
9M Bit	THM91070AS/AL-60/70/80/10	1M×9															
16M Bit	THM161000ASG-60/70/80/10	1M×16															
18M Bit	THM181000ASG-60/70/80/10	1M×18	72		25.40	107.95	5.08	With OE									
32M Bit	THM84000AS/ASG/AL-60/70/80/10	4M×8	30		20.45/20.45/22.60	88.9/88.9/76.5			8.89								
	THM84020AL-60/70/80/10	1M×32	72		12.64	82.14	5.08										
	THM321000AS/ASG-60/70/80/10				21.59	107.95											
	THM321090AS/ASG-60/70/80/10				25.40												
33M Bit	THM331000AS/ASG-60/70/80/10	1M×33	72		21.59	88.9/88.9/81.2	5.08	Low THM94000AL									
36M Bit	THM94000AS/ASG/AL-60/70/80/10	4M×9	30		20.45/20.45/22.60				88.9	8.89	Single sided type of THM361020						
	THM94020AL-60/70/80/10				12.64		88.9		8.89								
	THM361000AS/ASG-60/70/80/10	1M×36	72		29.68		107.95		5.08	1inch height type of THM361000							
	THM361020AS/ASG-60/70/80/10				21.59	×36 bit ECC Module											
	THM361010AS/ASG-60/70/80/10				25.40	8.89		With OE									
THM361070AS/ASG-60/70/80/10																	
40M Bit	THM401000ASG-60/70/80/10	1M×40	T _{RAC} -60: 60ns -70: 70ns -80: 80ns -10: 100ns		30	20.45	88.9	3.81	TSOP Module								
64M Bit	THM164020ASG-60/70/80/10	4M×16								72	25.40	107.95	8.89	1inch height type of THM362020			
	THM322020AS/ASG-60/70/80/10	2M×32													33.02	116.70	8.89
	THM322080AS-60/70/80/10	8M×8															
THM88020ATS-60/70/80/10	8M×9																
72M Bit	THM184020ASG-60/70/80/10	4M×18		30	25.40	107.95	8.89	2K refresh									
	THM362020AS/ASG-60/70/80/10	2M×36							29.68								
	THM362040AS/ASG-60/70/80/10																
	THM362060AS/ASG-60/70/80/10																
80M Bit	THM402020ASG-60/70/80/10			2M×40	T _{RAC} -60: 60ns -70: 70ns -80: 80ns	30	22.86	88.9		3.81	TSOP Module						
128M Bit	THM324080AS/ASG-60/70/80/10	4M×32		72					17.78			107.95	8.89	2K refresh			
132M Bit	THM334080AS/ASG-60/70/80/10	4M×33													34.00		
144M Bit	THM364080AS/ASG-60/70/80/10	4M×36														34.00	
128M Bit	THM81620TS-60/70/80	16M×8				30	22.86	88.9		3.81	TSOP Module						
144M Bit	THM324000SG-60/70/80	4M×32		72					17.78			107.95	8.89	2K refresh			
	THM91620TS-60/70/80	16M×9													34.00		
	THM364020SG-60/70/80	4M×36														34.00	
160M Bit	THM404020SG-60/70/80	4M×40				72	17.78	107.95		8.89	2K refresh						
256M Bit	THM328020SG-60/70/80	8M×32		34.00													
288M Bit	THM368020SG-60/70/80	8M×36	29.21														
320M Bit	THM408020SG-60/70/80	8M×40															

Video RAM

Capacity	Type No.	Organization	RAM Access Time (ns)			SAM Access Time (ns)		Power Dissipation (mW)		No. of Pins	Package Width (inch)	Comment
			t _{RAC}	t _{CAC}	Cycle Time	Access Time	Cycle Time	Active	Stand by			
1M Bit	TC521000P/J	262,144 × 4				20	30	550	110	40/40	DIP: 0.6, SOJ: 0.4	Field Memory
	TC524256BJ/BZ-80	262,144 × 4	80	25	150	25	30	687.5	55	28/28	SOJ: 0.4 ZIP: 0.4 (H)	Multi-Port DRAM
	TC524256BJ/BZ-10		100	25	180	25	30	605	55			
	TC524258BJ/BZ-80	262,144 × 4	80	25	150	25	30	687.5	55			
	TC524258BJ/BZ-10		100	25	180	25	30	605	55			
	TC524259BJ/BZ-80	262,144 × 4	80	25	150	25	30	687.5	55			
	TC524259BJ/BZ-10		100	25	180	25	30	605	55			
	* TC524256BFT/BTR-80	262,144 × 4	80	25	150	25	30	687.5	55	28	TSOP (II) : 0.4	
	* TC524256BFT/BTR-10		100	25	180	25	30	605	55			
	* TC524258BFT/BTR-80	262,144 × 4	80	25	150	25	30	687.5	55			
	* TC524258BFT/BTR-10		100	25	180	25	30	605	55			
	* TC524259BFT/BTR-80	262,144 × 4	80	25	150	25	30	687.5	55			
	* TC524259BFT/BTR-10		100	25	180	25	30	605	55			
	TC528126BJ/BZ-80	131,072 × 8	80	25	150	25	30	715	55	40/40	SOJ : 0.4 ZIP : 0.475 (H)	
	TC528126BJ/BZ-10		100	25	180	25	30	632.5	55			
	TC528128BJ/BZ-80	131,072 × 8	80	25	150	25	30	715	55			
	TC528128BJ/BZ-10		100	25	180	25	30	632.5	55			
	* TC528126BFT/BTR-80	131,072 × 8	80	25	150	25	30	715	55	44 (40)	TSOP (II) : 0.4 (0.8pitch.)	
	* TC528126BFT/BTR-10		100	25	180	25	30	632.5	55			
	* TC528128BFT/BTR-80	131,072 × 8	80	25	150	25	30	715	55			
	* TC528128BFT/BTR-10		100	25	180	25	30	632.5	55			
2M Bit	* TC528257J/FT/TR-70	262,144 × 8	70	20	130	20	25	825	55	40/ 44 (40)	SOJ: 0.4 TSOP (II) : 0.4 (0.8pitch)	Multi-Port DRAM
	* TC528257J/FT/TR-80		80	20	150	25	30	687.5	55			
	* TC528267J/FT/TR-70	262,144 × 8	70	20	130	20	25	825	55			
	* TC528267J/FT/TR-80		80	20	150	25	30	687.5	55			
	** TC528257SZ-70	262,144 × 8	70	20	130	20	25	825	55	40	SZIP: 0.475 (H) (0.89pitch)	
	** TC528257SZ-80		80	20	150	25	30	687.5	55			
	** TC528267SZ-70	262,144 × 8	70	20	130	20	25	825	55			
	** TC528267SZ-80		80	20	150	25	30	687.5	55			

* New Product
** Under Development

Static RAM

Capacity	Type No.	Organization	Max. Access Time (ns)	Min. Cycle Time (ns)	Power Supply (V)	Max. Power Dissipation (mW)		No. of Pins	Package Width (inch)
						Active	Stand-by		
64K Bit	TC5564APL/AFL-15	8,192 × 8	150	150	5V ± 10%	192.5	0.005	28	0.6/0.45 (P/F)
	TC5564APL/AFL-20		200	200					
256K Bit	TC55257BPL/BFL/BSPL/BFTL/BTRL-85	32,768 × 8	85	85	5V ± 10%	330	0.55	28	0.6/0.45/0.3 (P/F/SP) TSOP-I 8 × 13.4mm (FT, TR)
	TC55257BPL/BFL/BSPL/BFTL/BTRL-10		100	100					
	TC55257BPL/BFL/BSPL/BFTL/BTRL-85L		85	85					
	TC55257BPL/BFL/BSPL/BFTL/BTRL-10L		100	100					
	TC55257BPI/BFI/BSPI/BFTI/BTRI-10L		100	100					
1M Bit	TC551001APL/AFLAFTL/ATRL-70	131,072 × 8	70	70	5V ± 10%	330	0.55	32	0.6/0.525 (P/F) TSOP-I 8 × 20mm (FT, TR)
	TC551001APL/AFLAFTL/ATRL-85		85	85					
	TC551001APL/AFLAFTL/ATRL-10		100	100					
	TC551001APL/AFLAFTL/ATRL-70L		70	70					
	TC551001APL/AFLAFTL/ATRL-85L		85	85					
	TC551001APL/AFLAFTL/ATRL-10L		100	100					
	TC551001API/AFI/AFTI/ATRI-85		85	85					
	TC551001API/AFI/AFTI/ATRI-10		100	100					
	TC551001API/AFI/AFTI/ATRI-85L		85	85					
	TC551001API/AFI/AFTI/ATRI-10L		100	100					
4M Bit	**TC554002PL/FL/FTL/TRL-55	524,288 × 8	55	55	5V ± 10%	385	0.55	32	0.6/0.525 (P/F) TSOP-II 0.4 (FT, TR)
	**TC554002PL/FL/FTL/TRL-70		70	70					
	**TC554002PL/FL/FTL/TRL-85		85	85					
	**TC554002PL/FL/FTL/TRL-10		100	100					
	**TC554002PL/FL/FTL/TRL-55L		55	55					
	**TC554002PL/FL/FTL/TRL-70L		70	70					
	**TC554002PL/FL/FTL/TRL-85L		85	85					
	**TC554002PL/FL/FTL/TRL-10L		100	100					

Package : P:Plastic DIP, F:Flat Package SOP, SP:Simplistic DIP,
FT:TSOP (Forward), TR:TSOP (Reverse)

** : Under Development

High Speed Static RAM

Capacity	Type No.	Organization	Max. Access Time (ns)	Min. Cycle Time (ns)	Power Supply (V)	Max. Power Dissipation (mW)		No. of Pins	Package Width (inch)	Process
						Active	Stand-by			
64K Bit	TC55416P-15H	16,384 × 4	15	15	5V ± 10%	660	5.5	22	0.3	CMOS
	TC55416P-20H		20	20		550				
	TC55416P-25H		25	25		550				
	TC55416P-35H		35	35		440				
	TC55417P/J-15H		15	15	5V ± 10%	660	5.5	24	0.3	CMOS
	TC55417P/J-20H		20	20		550				
	TC55417P/J-25H		25	25		550				
	TC55417P/J-35H		35	35		440				
	TC55B417P/J-10	8,192 × 8	10	10	5V ± 5%	630	55	24	0.3	Bi-CMOS
	TC55B417P/J-12		12	12		660				
	TC5588P/J-15		15	15	5V ± 10%	743	5.5	28	0.3	CMOS
	TC5588P/J-20		20	20						
	TC5588P/J-25		25	25		633				
	TC5588P/J-35		35	35						
	TC55B88P/J-10		10	10	5V ± 5%	814	55	28	0.3	Bi-CMOS
	TC55B88P/J-12		12	12	5V ± 10%	853				
72K Bit	TC5589P/J-15	8,192 × 9	15	15	5V ± 10%	743	5.5	28	0.3	CMOS
	TC5589P/J-20		20	20						
	TC5589P/J-25		25	25		633				
	TC5589P/J-35		35	35						
144K Bit	TC55187T-20	8,192 × 18/ 4,096 × 18 × 2 way	20	20	5V ± 10%	1265	5.5	52	0.75	CMOS
	TC55187T-25		25	25		1210				
	TC55187T-30		30	30		1100				
	TC55188T-20		20	20		1265				
	TC55188T-25		25	25		1210				
	TC55188T-30		30	30		1100				
256K Bit	TC55464P/J-17	65,536 × 4	17	17	5V ± 5%	630	5.5	24	0.3	CMOS
	TC55464P/J-20		20	20	5V ± 10%	660				
	TC55464P/J-25		25	25		550				
	TC55464P/J-35		35	35						
	TC55B464P/J-10		10	10	5V ± 10%	770	82.5	24	0.3	Bi-CMOS
	TC55B464P/J-12		12	12						
	TC55B464P/J-15		15	15						
	TC55465P/J-17		17	17	5V ± 5%	630	5.5	28	0.3	CMOS
	TC55465P/J-20		20	20	5V ± 10%	660				
	TC55465P/J-25		25	25		550				
	TC55465P/J-35		35	35						
	TC55B465P/J-10	32,768 × 8	10	10	5V ± 10%	770	82.5	28	0.3	Bi-CMOS
	TC55B465P/J-12		12	12						
	TC55B465P/J-15		15	15						
	TC55328P/J-17		17	17	5V ± 5%	735	5.5	28	0.3	CMOS
	TC55328P/J-20		20	20	5V ± 10%	770				
	TC55328P/J-25		25	25		660				
	TC55328P/J-35		35	35						
	TC55B328P/J-10		10	10	5V ± 10%	935	82.5	28	0.3	Bi-CMOS
	TC55B328P/J-12		12	12						
	TC55B328P/J-15		15	15						

Capacity	Type No.	Organization	Max. Access Time (ns)	Min. Cycle Time (ns)	Power Supply (V)	Max. Power Dissipation (mW)		No. of Pins	Package Width (inch)	Process				
						Active	Stand-by							
288K Bit	TC55329P/J-17	32,768×9	17	17	5V±5%	735	5.5	32	0.3	CMOS				
	TC55329P/J-20		20	20	5V±10%	770								
	TC55329P/J-25		25	25		660								
	TC55329P/J-35		35	35		935	82.5			Bi-CMOS				
	TC55B329P/J-10		10	10										
	TC55B329P/J-12		12	12										
	TC55B329P/J-15		15	15										
512K Bit	TC551632J-20	32,768×16	20	20	5V±10%	1210	5.5	40	0.4	CMOS				
	TC551632J-25		25	25		1100								
	TC551632J-35		35	35		935								
1M Bit	TC55B4256J-12	262,144×4	12	12	5V±10%	715	66	28	0.4	Bi-CMOS				
	TC55B4256J-15		15	15				32						
	TC55B4256J-20		20	20							825	82.5		
	TC55B4257J-12		12	12									44	
	TC55B4257J-15		15	15										5.5
	TC55B4257J-20		20	20										
	TC55B8128P/J-12	131,072×8	12	12		1155	220	36		0.4	Bi-CMOS			
	TC55B8128P/J-15		15	15										
	TC55B8128P/J-20		20	20										
	TC551664J-15	65,536×16	15	15		1430	5.5	44				CMOS		
	TC551664J-20		20	20		1210								
	TC551664J-25		25	25		1100								
	**TC55BS4256J-10	262,144×4	10+5	10		5V±10%	1045	220	36	0.4	Bi-CMOS			
	**TC55BS4256J-12		12+6	12										
	**TC55BS8125J-10		10+5	10										
	**TC55BS8125J-12	131,072×8	12+6	12	1155		220	40						
	**TC55BS8128J-10		10+5	10										
	**TC55BS8128J-12		12+6	12										
	4M Bit	**TC551402J-20	4,194,304×1/	20	20	5V±10%	825	55	32	0.4	CMOS			
**TC551402J-25		1,048,576×4	25	25										

Package (P:Plastic DIP, J:SOJ, T:Plastic LCC)

** : Under Development

TC55417P/J:Equivalent to TC55416P with OE function

TC55465P/J, TC55B465P:Equivalent to TC55464P/J with OE function

TC55B4257J:Equivalent to TC55B4256P/J with OE function

TC55BS4258J:Synchronous SRAM

TC55BS8125J:Synchronous SRAM

TC55BS8128J:Synchronous SRAM

Pseudo Static RAM

Capacity	Type No.	Organization	Max. Access Time (ns)	Min. Cycle Time (ns)	Power Supply (V)	Max. Power Dissipation (mW)		No. of Pins	Package Width (inch)
						Active	Stand-by		
256K Bit	TC51832AP/ASP/AF-70	32,768 × 8	70	115	5V ± 10%	385	5.5	28	0.6 (P) 0.3 (SP) 0.45 (F)
	TC51832AP/ASP/AF-85		85	135		303			
	TC51832AP/ASP/AF-10		100	160		248			
	TC51832APL/ASPL/AFL-70		70	115		385	0.55		
	TC51832APL/ASPL/AFL-85		85	135		303			
	TC51832APL/ASPL/AFL-10		100	160		248			
1M Bit	TC518128AP/ASP/AF/AFW-80	131,072 × 8 (CE1, CE2 Type)	80	130	5V ± 10%	385	5.5	32	0.6 (P) 0.3 (SP) 0.45 (F) 0.525 (FW) TSOP- I 8 × 20mm (FT, TR)
	TC518128AP/ASP/AF/AFW-10		100	160		330			
	TC518128AP/ASP/AF/AFW-12		120	190		275			
	TC518128APL/ASPL/AFL/AFWL/AFTL/ATRL-80		80	130		385	1.1		
	TC518128APL/ASPL/AFL/AFWL/AFTL/ATRL-10		100	160		330			
	TC518128APL/ASPL/AFL/AFWL/AFTL/ATRL-12		120	190		275			
	TC518128APL/AFL/AFWL/AFTL/ATRL-80LV	80	130	385		1.1 (0.3)			
	TC518128APL/AFL/AFWL/AFTL/ATRL-10LV	100	160	330					
	TC518128APL/AFL/AFWL/AFTL/ATRL-12LV	120	190	275					
	TC518129AP/ASP/AF/AFW-80	131,072 × 8 (CE, CS Type)	80	130		385	5.5		
	TC518129AP/ASP/AF/AFW-10		100	160		330			
	TC518129AP/ASP/AF/AFW-12		120	190		275			
	TC518129APL/ASPL/AFL/AFWL/AFTL/ATRL-80		80	130		385	1.1		
	TC518129APL/ASPL/AFL/AFWL/AFTL/ATRL-10		100	160		330			
	TC518129APL/ASPL/AFL/AFWL/AFTL/ATRL-12		120	190		275			
	TC518129APL/AFL/AFWL/AFTL/ATRL-80LV	80	130	385		1.1 (0.3)			
	TC518129APL/AFL/AFWL/AFTL/ATRL-10LV	100	160	330					
	TC518129APL/AFL/AFWL/AFTL/ATRL-12LV	120	190	275					
	*TC518128BPL/BSPL/BFL/BFWL/BFTL/BTRL-70	131,072 × 8 (CE1, CE2 Type)	70	115		385	1.1		
	*TC518128BPL/BSPL/BFL/BFWL/BFTL/BTRL-80		80	130		330			
	*TC518128BPL/BSPL/BFL/BFWL/BFTL/BTRL-10		100	160		275			
	*TC518128BPL/BSPL/BFL/BFWL/BFTL/BTRL-70L		70	115		385	0.275		
	*TC518128BPL/BSPL/BFL/BFWL/BFTL/BTRL-80L		80	130		330			
	*TC518128BPL/BSPL/BFL/BFWL/BFTL/BTRL-10L		100	160		275			
	*TC518128BPL/BFL/BFWL/BFTL/BTRL-70V	131,072 × 8 (CE, CS Type)	70	115		385	0.275 (0.075)		
	*TC518128BPL/BFL/BFWL/BFTL/BTRL-80V		80	130		330			
	*TC518128BPL/BFL/BFWL/BFTL/BTRL-10V		100	160		275			
	*TC518129BPL/BSPL/BFL/BFWL/BFTL/BTRL-70		70	115		385	1.1		
	*TC518129BPL/BSPL/BFL/BFWL/BFTL/BTRL-80		80	130		330			
	*TC518129BPL/BSPL/BFL/BFWL/BFTL/BTRL-10		100	160		275			
	*TC518129BPL/BSPL/BFL/BFWL/BFTL/BTRL-70L	131,072 × 8 (CE, CS Type)	70	115		385	0.275		
	*TC518129BPL/BSPL/BFL/BFWL/BFTL/BTRL-80L		80	130		330			
	*TC518129BPL/BSPL/BFL/BFWL/BFTL/BTRL-10L		100	160		275			
	*TC518129BPL/BFL/BFWL/BFTL/BTRL-70V		70	115		385	0.275 (0.075)		
	*TC518129BPL/BFL/BFWL/BFTL/BTRL-80V		80	130		330			
	*TC518129BPL/BFL/BFWL/BFTL/BTRL-10V		100	160		275			
4M Bit	TC518512PL/FL/FTL/TRL-70	524,288 × 8	70	115	5V ± 10%	385	1.1	32	0.6 (P) 0.525 (F) TSOP- II 0.4 (FT, TR)
	TC518512PL/FL/FTL/TRL-80		80	130		330			
	TC518512PL/FL/FTL/TRL-10		100	160		275			
	TC518512PL/FL/FTL/TRL-70LV	524,288 × 8	70	115	5V ± 10%	385	1.1 (0.33)	32	
	TC518512PL/FL/FTL/TRL-80LV		80	130		330			
	TC518512PL/FL/FTL/TRL-10LV		100	160		275			

Package : P : Plastic DIP, SP : Slimplastic DIP, F, FW : Flat Package SOP
FT : TSOP (Forward), TR : TSOP (Reverse)

(): 3V * : New Product

EPROM

Capacity	Type No.	Organization	Max. Access Time (ns)	Min. Cycle Time (ns)	Power Supply (V)	Operating Temperature (°C)	Max. Power Dissipation (mW)		No. of Pins	Device Type		
							Active	Stand-by				
256K Bit	TC57256AD-12	32,768 × 8	120	120	5V ± 5%	0 ~ 70	158	0.525	28	CMOS		
	TC57256AD-120		120	120	5V ± 10%		165	0.550				
	TC57256AD-150		160	150			5V ± 5%	158			0.525	
	TC57256AD-15		150	150	- 40 ~ 85	210		0.550				
	TC57256AD-20		200	200		0 ~ 70		220			0.550	
	TC57H256D-70		70	70			158	0.525				
512K Bit	TC57512AD-15	65,536 × 8	85	85	5V ± 10%	- 40 ~ 85	210	0.550	28	CMOS		
	TC57512AD-20		150	150	5V ± 5%		158	0.525				
			200	200	5V ± 10%		165	0.550				
1M Bit	TC571000/1AD-12	131,072 × 8	120	120	5V ± 5%	0 ~ 70	158	0.525	32	CMOS		
	TC571000/1AD-150		150	150	5V ± 10%		165	0.550				
	TC57H1000/1AD-85		85	85	5V ± 5%		210	0.525				
	TC57H1000/1AD-100		100	100	5V ± 10%		220	0.550				
	TC57H1024AD-85	65,536 × 16	85	85	5V ± 5%		315	0.525	40			
	TC57H1024AD-100		100	100	5V ± 10%		330	0.550				
	TC57H1025AD-55		55	55	5V ± 5%		473	105				
	TC57H1025AD-70		70	70								
	4M Bit	TC574000D-120	524,288 × 8	120	120		5V ± 10%	0 ~ 70	330		0.550	32
		TC574000D-150	150	150	275							
* TC574000AD-120		524,288 × 8	120	120	5V ± 10%	330	0.550		32			
* TC574000AD-150		150	150	275								
TC574200D-10		524,288 × 8	100	100	5V ± 5%	368	0.525		40			
TC574200D-120			120	120	5V ± 10%	330	0.550					
TC574200D-150		262,144 × 16	150	150		5V ± 5%	368			0.525		
TC574096D-10		262,144 × 16	100	100	5V ± 10%		330			0.550		
TC574096D-120			120	120		368	0.525					
TC574096D-150			150	150		330	0.550					
8M Bit	TC578200D-150	1,048,576 × 8 524,288 × 16	150	150	5V ± 10%	0 ~ 70	330	0.550	42	CMOS		
16M Bit	* TC5716200D-150	2,097,152 × 8 1,048,576 × 16	150	150	5V ± 10%	0 ~ 70	330	0.550	42	CMOS		

Package D : Cerdip Package

* : New Product

ONE TIME PROM

Capacity	Type No.	Organization	Max. Access Time (ns)	Min. Cycle Time (ns)	Power Supply (V)	Max. Power Dissipation (mW)		No. of Pins	Device Type		
						Active	Stand-by				
256K Bit	TC54256AP/AF	32,768 × 8	200	200	5V ± 5%	158	0.525	28	CMOS		
512K Bit	TC54512AP/AF-15	65,536 × 8	150	150	5V ± 5%	158	0.525	28	CMOS		
	TC54512AP/AF-20		200	200							
1M Bit	TC541000/1AP/AF-12	131,072 × 8	120	120	5V ± 5%	158	0.525	32	CMOS		
	TC541000/1AP/AF-15		150	150							
	TC54H1000/1AP/AF-85		85	85							
	TC54H1000/1AP/AF-10		100	100		210					
	TC54H1024AP/AF-85	65,536 × 16	85	85						40	
	TC54H1024AP/AF-10		100	100		315					
4M Bit	TC544000P/F/FT-12	524,288 × 8	120	120	5V ± 5%	315	0.525	32	CMOS		
	TC544000P/F/FT-150		150	150	5V ± 10%	275	0.550				
	* TC544000AP/AF-12	524,288 × 8	120	120	5V ± 5%	315	0.525	32	CMOS		
	* TC544000AP/AF-150		150	150	5V ± 10%	275					
	TC544200P/F-120	524,288 × 8	120	120	5V ± 10%		0.550	40	CMOS		
	TC544200P/F-150	262,144 × 16	150	150							
	TC544096P/F-120	262,144 × 16	120	120							
	TC544096P/F-150		150	150							
Package	P : Plastic DIP, F : Flat Packages (SO, SSOP, TSOP, etc.)										

Package P : Plastic DIP, F : Flat Package (SOP), FT : TSOP (TYPE II, Normal type)

* : New Product

CMOS Flash/NAND E²PROM

Capacity	Type No.	Organization	Max. Access Time (ns)	Power Supply (V)		Max. Power Dissipation (mW)			Program/Erase Mode	Operating Temperature (°C)	Package	No. of Pins
				V _{CC} (V)	V _{PP} (V)	Read	Program/Erase	Stand-by				
256K Bit Flash	TC58257AP-20, 25	32,768 × 8	200/250	5V ± 10%	12.75 ± 0.25 or 12.0 ± 0.5	165 (V _{CC}) 0.06 (V _{PP})	220 (V _{CC}) 650 (V _{PP})	0.55 (V _{CC}) 0.06 (V _{PP})	EPROM Compatible	-10 ~ 70	600mil DIP	28
	TC58257AF-20, 25										450mil SOP	
4M Bit NAND	* TC584000P	524,288 × 8	120 (Page Access) 15μs (Random Access)	5V ± 10%	—	165	330/275	0.55	Command Control	0 ~ 70	600mil DIP	32
	* TC584000F										525mil SOP	
	* TC584000FT										400mil TSOP TYPE-II (Normal)	44 (40)
	* TC584000TR										400mil TSOP TYPE-II (Reverse)	

Package P : Plastic DIP, F : Flat Package (SOP), FT : TSOP (Normal Bent), TR : TSOP (Reverse Bent)

* : New Product

CMOS Mask ROM

Capacity	Type No.	Organization	Max. Access Time (ns)	Min. Cycle Time (ns)	Power Supply (V)	Max. Power Dissipation (mW)		No. of Pins
						Active	Stand-by	
1M Bit	TC531000CP/CF-15	131,072×8	150	150	5V±10%	193	0.11	28
	TC531000CP/CF-12		120	120		220		
	TC531001CP/CF-15		150	150		193		
	TC531001CP/CF-12		120	120		220		
	TC531024P/F-15	65,536×16	150	150		193		40
	TC531024P/F-12		120	120		220		
2M Bit	TC532000AP/AF	262,144×8	150	150	5V±10%	220	0.11	32
4M Bit	TC534000AP/AF/AFT	524,288×8	150	150	5V±10%	220	0.11	32
	TC534200P/F	524,288×8 262,144×16	150	150		275		40
8M Bit	TC538000AP/AF	1,048,576×8	150	150	5V±10%	303	0.55	32
	TC538200AP/AF	1,048,576×8 524,288×16	150	150		330	0.55	42 (DIP) 44 (SOP)
16M Bit	TC5316200AP/AF/AFT	2,097,152×8 1,048,576×16	150	150	5V±10%	330	0.55	42 (DIP) 44 (SOP)
	TC5316200BP/BF	2,097,152×8 1,048,576×16	200	200		275	0.55	
	TC5316210BP/BF/BFT	2,097,152×8 1,048,576×16	150	150		825	5.5	

Package P : Plastic DIP, F : Flat Package (SOP), FT : TSOP (Normal Bent)

2. Cross Reference

1M Bit Dynamic RAM

Organization	1M × 1 (Fast Page)	1M × 1 (Nibble)	1M × 1 (Static Column)	256K × 4 (Fast Page)	256K × 4 (Static Column)
TOSHIBA	TC511000	TC511001	TC511002	TC514256	TC514258
Fujitsu	MB81C1000	ME81C1001	MB81C1002	MB81C4256	MB81C4258
Hitachi	HM511000	HM511001	HM511002	HM514256	HM514258
Mitsubishi	M5M4C1000	M5M4C1001	M5M4C1002	M5M44C256	M5M44C258
NEC	μPD421000	μPD421001	μPD421002	μPD424256	μPD424258
OKI	MSM511000	MSM511001	MSM511002	MSM514256	MSM514258
TI	TMS4C1024	TMS4C1025	TMS4C1027	TMS44C256	TMS44C257
Motorola	MCM511000	MCM511001	MCM511002	MCM514256	MCM514258
Siemens	HYB511000	—	—	HYB514256	—
SAMSUNG	KM41C1000	KM41C1001	KM41C1002	KM44C256	KM44C258

4M Bit Dynamic RAM

Organization	4M × 1 (Fast Page)	4M × 1 (Nibble)	4M × 1 (Static Column)	1M × 4 (Fast Page)	1M × 4 (Static Column)
TOSHIBA	TC514100	TC514101	TC514102	TC514400	TC514402
Fujitsu	MB814100	MB814101	MB814102	MB814400	MB814402
Hitachi	HM514100	HM514101	HM514102	HM514400	HM514402
Mitsubishi	M5M414000	M5M414001	M5M414002	M5M441000	M5M441002
NEC	μPD424100	μPD424101	μPD424102	μPD424400	μPD424402
OKI	MSM514100	MSM514101	MSM514102	MSM514400	MSM514402
TI	TMS44100	—	—	TMS44400	—
Micron	MT4C1004	MT4C1005	MT4C1006	MT4C4001	MT4C4003
Motorola	MCM514100	MCM514101	MCM514102	MCM514400	MCM514402
Siemens	HYB514100	—	—	HYB514400	—
SAMSUNG	KM41C4000	—	—	KM44C1000	—

16M Bit Dynamic RAM

16M × 1 (4K CYCLE/REFRESH)

Organization	16M × 1 (Fast Page)	16M × 1 (Nibble)	16M × 1 (Static Column)
TOSHIBA	TC5116100	TC5116101	TC5116102
Fujitsu	MB8116100	MB8116101	—
Hitachi	HM5116100	HM5116101	HM5116102
NEC	μPD4216100	—	—
SAMSUNG	—	—	—
Siemens	HYB511610	—	—

4M × 4 (4K CYCLE/REFRESH)

Organization	4M × 4 (Fast Page)	4M × 4 (Static Column)	4M × 4 (Write Per Bit)
TOSHIBA	TC5116400	TC5116402	TC5116410
Fujitsu	MB8116400	—	—
Hitachi	HM5116400	HM5116402	HM5116410
NEC	μPD4216400	—	—
SAMSUNG	KM44C4000	—	—
Siemens	HYB511640	—	—

4M × 4 (2K CYCLE/REFRESH)

Organization	4M × 4 (Fast Page)	4M × 4 (Static Column)	4M × 4 (Write Per Bit)
TOSHIBA	TC5117400	TC5117402	TC5117410
Fujitsu	—	—	—
Hitachi	HM5117400	—	—
NEC	μPD4217400	—	—
SAMSUNG	KM44C4100	—	—
Siemens	—	—	—

Dynamic RAM Module

	1M×8 Socket Type	1M×8 Pin Type	1M×9 Socket Type	1M×9 Pin Type	256K×36 Socket Type	512K×36 Socket Type
TOSHIBA	THM81000AS-70 THM81000AS-80 THM81000AS-10	THM81000AL-70 THM81000AL-80 THM81000AL-10	THM91000AS-70 THM91000AS-80 THM91000AS-10	THM91000AL-70 THM91000AL-80 THM91000AL-10	THM362500ASG-70 THM362500ASG-80 THM362500ASG-10	THM365120ASG-70 THM365120ASG-80 THM365120ASG-10
Fujitsu	MB85230 (100ns/120ns)	MB85230 (100ns/120ns)	MB85235 (100ns/120ns)	MB85235 (100ns/120ns)	MB85236-10 MB85236-12	—
Hitachi	HB56A18B-S (100ns/120ns)	HB56A18A-S (100ns/120ns)	HB56A19B-S (100ns/120ns)	HB56A19A-S (100ns/120ns)	HB56D25636B-85 HB56D25636B-10 HB56D25636B-12	HB56D51236B-85 HB56D51236B-10 HB56D51236B-12
Mitsubishi	MH1M08AQJ-8 MH1M08AQJ-10 MH1M08AQJ-12	MH1M08AQJA-8 MH1M08AQJA-10 MH1M08AQJA-12	MH1M09AQJ-8 MH1M09AQJ-10 MH1M09AQJ-12	MH1M09AQJA-8 MH1M09AQJA-10 MH1M09AQJA-12	MH25636AJ-85 MH25636AJ-10 MH25636AJ-12	MH51236AJ-85 MH51236AJ-10 MH51236AJ-12
NEC	MC-421000A8B-80 MC-421000A8B-10 MC-421000A8B-12	MC-421000A8A-80 MC-421000A8A-10 MC-421000A8A-12	MC-421000A9B-80 MC-421000A9B-10 MC-421000A9B-12	MC-421000A9A-80 MC-421000A9A-10 MC-421000A9A-12	—	—
OKI	MSC2313-10YS MSC2313-12YS	MSC2313-10KS MSC2313-12KS	MSC2312-10YS MSC2312-12YS	MSC2312-10KS MSC2312-12KS	—	—
Toyocom	TH3C10008-70 TH3C10008-80 TH3C10008-10	TH2C10008-70 TH2C10008-80 TH2C10008-10	TH3C10009-70 TH3C10009-80 TH3C10009-10	TH2C10009-70 TH2C10009-80 TH2C10009-10	TH3C1P2536-70 TH3C1P2536-80 TH3C1P2536-10	TH3C1P5136-70 TH3C1P5136-80 TH3C1P5136-10
NMB Semiconductor	MM1M100J8-08 MM1M100J8-10 MM1M100J8-12 (Socket Type)	MM1M100J8-08 MM1M100J8-10 MM1M100J8-12 (Lead Type)	MM1M100J9-08 MM1M100J9-10 MM1M100J9-12 (Socket Type)	MM1M100J9-08 MM1M100J9-10 MM1M100J9-12 (Lead Type)	—	—
Texas Instruments	TM024GAD8-10L TM024GAD8-12L	—	TM024EAD9-10L TM024EAD9-12L	—	—	—
Micron	MT8C8024M-8 MT8C8024M-10 MT8C8024M-12	MT8C8024MN-8 MT8C8024MN-10 MT8C8024MN-12	MT8C9024M-8 MT8C9024M-10 MT8C9024M-12	MT8C9024MN-8 MT8C9024MN-10 MT8C9024MN-12	MT8C36256M-8 MT8C36256M-10 MT8C36256M-12	MT8C36512DM-8 MT8C36512DM-10 MT8C36512DM-12

● 64K Bit Static RAM (8K × 8, 28 pin)

Package Width	0.6 inch DIP	0.45 inch SOP
TOSHIBA	TC5564APL	TC5564AFL
Fujitsu		
Hitachi		
Mitsubishi		
NEC	μPD4464C	μPD4464G
OKI		

● 256K Bit Static RAM (32K × 8, 28 pin)

Package Width	0.3 inch DIP	0.6 inch DIP	0.45 inch SOP	8 × 13.4 mm TYPE I TSOP
TOSHIBA	TC55257BSP	TC55257BP	TC55257BF	TC55257BFT
Fujitsu	M84256A	MB84256	MB84256	MB84256A
Hitachi		MB84256A	MB84256A	
		HM62256P	HM62256FP	
NEC	μPD43256BCX	μPD43256AC	μPD43256AGU	
Mitsubishi	M5M5256BKP	μPD43256BCZ	μPD43256BGU	
		M5M5256BP	M5M5256BFP	M5M5256BVP
SONY	CXK58257SP CXK58257ASP	CXK58257P CXK58257AP	CXK58257M CXK58257AM	CXK58257ATM

● 1M Bit Static RAM (128K × 8, 32 pin)

Package Width	0.6 inch DIP	0.525 inch SOP	8 × 20 mm TYPE I TSOP
TOSHIBA	TC551001AP	TC551001AF	TC551001AFT
Hitachi	HM628128P	HM628128FP	HM628128T
NEC	μPD431000CZ μPD431000ACZ	μPD431000GW μPD431000AGW	μPD431000AGZ
Mitsubishi	M5M51008P	M5M51008FP	M5M51008VP
SONY	CXK581001P	CXK581001M	CXK581001TM

High Speed Static RAM

Organization	16K × 4		8K × 8	8K × 9	8K × 18/4K × 18 × 2	
Package Width	0.3 inch				0.75 inch	
TOSHIBA	TC55416-H	TC55417-H	TC5588	TC5589	TC55187T	TC55188T
Fujitsu	MB81C74	MB81C75	MB81C78A	MB81C79A		
Hitachi	HM6288/6788	HM6789			HM62A188	
Mitsubishi	M5M5188	M5M5189	M5M5178	M5M5179		
NEC	μPD4362	μPD4363				
OKI	MSM5188A					
Sony	CXK5464AP	CXK5465P	CXK5863P	CXK5971P	CXK7701J	
Sharp	LH5262		LH5165/64			
Inmos	IMS1620	IMS1624				
MOTOROLA	MCM6288	MCM6289	MCM6264	MCM6265		
LATTICE	SR64K4	SR64E4	SR64K8			
VITELIC	V61C62		V61C64		V63C330	V63C328
IDT	IDT7188	IDT7198	IDT7164			
AMD	Am99C164	Am99C165	Am99C88H			
CYPRESS	CY7C164	CY7C166	CY7C185		CY7C183	CY7C184
PERFORMANCE	P4C188	P4C198	P4C164	P4C163		
TI					SN74ACT2140	
MICRON	MT5C6404	MT5C6405	MT5C6408		MT56C0416	

Organization	64K × 4		32K × 8	32K × 9	256K × 4		128K × 8	64K × 16
Package Width	0.3 inch				0.4 inch			
TOSHIBA	TC55464	TC55465	TC55328	TC55329	TC55B4256	TC55B4257	TC55B8128	TC551664
Fujitsu	MB81C84A	MB81C85A						
Hitachi	HM6208/6708	HM6709	HM62832					
Mitsubishi	M5M5258AP	M5M5259		M5M5279				
NEC	μPD43254C			μPD43259			μPD431008	μPD431016
OKI	MSM52464							
Sony	CXK54256P		CXK58258	CXK59288				
Sharp	LH52252		LH52258					
Inmos	IMS1820		IMS1830					
MOTOROLA	MCM6208	MCM6209	MCM6206	MCM6205	MCM6728	MCM6729	MCM6726	
LATTICE	SR256K4		SR256K8					
VITELIC								
IDT	IDT71258	IDT61298	IDT71256					
AMD			Am99C328					
CYPRESS	CY7C194	CY7C196	CY7C198					
PERFORMANCE	P4C1258		P4C1256					
TI								
MICRON	MT5C2564	MT5C2565	MT5C2568					

Organization	4M × 1	1M × 4
Package Width	0.4 inch	
TOSHIBA	TC551402	
Hitachi	HM621400	HM624100
NEC	μPD434001	μPD434004

256 K Bit Pseudo Static RAM (32K × 8, 28 pin)

Package Width	0.6 inch DIP	0.3 inch DIP	0.45 inch SOP
TOSHIBA	TC51832AP	TC51832ASP	TC51832AF
Hitachi	HM65256BP	HM65256BSP	HM65256BFP
NEC	μPD42832C	---	μPD42832G
Sharp	LH5P832	LH5P832	LH5P832

1M Bit Pseudo Static RAM (128K × 8, 32 pin)

Package Width	0.6 inch DIP	0.3 inch DIP	0.45 inch SOP	0.525 inch SOP	8 × 20mm TSOP
TOSHIBA	TC518128/9AP TC518128/9BP	TC518128/9ASP TC518128/9BSP	TC518128/9AF TC518128/9BF	TC518128/9AFW TC518128/9BFW	TC518128/9AFT/ATR TC518128/9BFT/BTR
Hitachi	HM658128ALP	---	---	HM658128ALFP	HM658128ALT/ALR
NEC	μPD428128CZ	---	---	μPD428128GW	---
Samsung	KM658128P	---	KM658128SG	KM658128G	---
Sharp	LH5P8128	---	---	LH5P8128N	LH5P8128T/TR

4M Bit Pseudo Static RAM (512K × 8, 32 pin)

Package Width	0.6 inch DIP	0.525 inch SOP	0.4 inch TSOP
TOSHIBA	TC518512P	TC518512F	TC518512FT/TR
Hitachi	HM658512LP	HM658512LFP	HM658512LTT/LRR

256K/512K Bit EPROM/OTP/Mask ROM

Organization	32K × 8			64K × 8		
EPROM/OTP/MROM	EPROM	OTP	MROM	EPROM	OTP	MROM
Pins	28	28	28	28	28	28
TOSHIBA	TC57256AD	TC54256AP	TC53257	TC57512AD	TC54512AP	---
AMD	Am27C256	Am27C256	---	Am27C512	Am27C512	---
Fujitsu	MBM27C256A	MBM27C256AP	MB83256P	MBM27C512	MBM27C512P	MB83512P
Hitachi	HN27C256	HN27C256	HN623257	HN27C512G	HN27512P	---
Intel	27C256	P27C256	---	27C512	P27C512	---
Mitsubishi	M5M27C256AK	M5M27C256AP	---	M5M27C512AK	M5M27C512AP	---
NEC	μPD27C256	μPD27C256	μPD23C256P	μPD27C512D	μPD27C512C	---
OKI	MSM27C256	MSM27256ZB	MSM53256P	MSM27512	MSM27512ZB	---
Sharp	LH57256J	LH57256D	LH53259	---	---	LH53514
TI	---	---	---	---	---	---

1M Bit EPROM/OTP/Mask ROM

Organization	128K × 8			128K × 8			64K × 16		
EPROM/OTP/MROM	EPROM	OTP	MROM	EPROM	OTP	MROM	EPROM	OTP	MROM
Pins	32	32	32	32	32	28	40	40	40
TOSHIBA	TC571000	TC541000	TC531001C	TC571001	TC541001	TC531000C	TC57H1024	TC54H1024	TC531024
AMD	Am27C010	Am27C010	---	Am27C100	Am27C100	---	Am27C1024	Am27C1024	---
Fujitsu	MBM27C1001	MBM27C1001P	---	MBM27C1000	MBM27C1000P	MB831000	MBM27C1024	MBM27C1024P	---
Hitachi	HN27C101AG	HN27C101AP/AFP	HN62321A	HN27C301AG	HN27C301AP/AFP	HN62321	HN27C1024HG	---	---
Intel	27C010	---	---	---	---	---	27C210	---	---
Matsushita	---	---	---	---	---	MN231001	---	---	---
Mitsubishi	M5M27C101K	M5M27C101P/FP	---	M5M27C100K	M5M27C100P/FP	M5M231000	M5M27C102K	M5M27C102P/FP	---
NEC	μPD27C1001AD	μPD27C1001AC	μPD23C100E	μPD27C1000AD	μPD27C1000AC	μPD23C1000	μPD27C1024	---	μPD23C1024
OKI	MSM271000	MSM271000ZB	MSM531001A	---	---	MSM531000	MSM271024	MSM271024ZB	---
Sharp	LH571001J	LH571001	LH530800	LH571000J	LH571000	LH531000A	---	---	---
TI	TMS27C010	---	---	---	---	---	TMS27C210	---	---

2M Bit Mask ROM

Organization	256K × 8
EPROM/OTP/MROM	MROM
Pins	32
TOSHIBA	TC532000A
AMD	
Fujitsu	MB832000A
Hitachi	HN62302B
Intel	
Matsushita	
Mitsubishi	
NEC	
OKI	MSM532001A
Sharp	LH532300
TI	

4M Bit EPROM/OTP/Mask ROM

Organization	512K × 8			512K × 8 / 256K × 16			256K × 16	
EPROM/OTP/MROM	EPROM	OTP	MROM	EPROM	OTP	MROM	EPROM	OTP
Pins	32	32	32	40	40	40	40	40
TOSHIBA	TC574000	TC544000	TC534000	TC574200	TC544200	TC534200	TC574096	TC544096
AMD	Am27C040	Am27C040		Am27C400	Am27C400		Am27C4096	Am27C4096
Fujitsu	MBM27C4001		MB834000			MB834200	MBM27C4096	
Hitachi	HN27C4001G		HN62324			HN62424	HN27C4096G	
Intel	27C040			27C400			27C240	
Matsushita			MN234002			MN234000		
Mitsubishi	M5M27C401K	M5M27C401P	M5M23401			M5M23400	M5M27C402K	M5M27C402P
NEC	μPD27C4001DZ	μPD27C4001CZ	μPD23C4001	μPD27C4000DZ		μPD23C4000	μPD27C4096	
OKI	MSM27C401		MSM534001A			MSM534002A		
Sharp			LH534300			LH534500		
TI	TMS27C040							

8M/16M Bit EPROM/Mask ROM

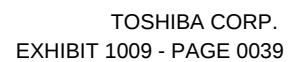
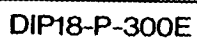
Organization	1M × 8	1M × 8 / 512K × 16		2M × 8 / 1M × 16	
EPROM/OTP/MROM	MROM	EPROM	MROM	EPROM	MROM
Pins	32	42	42/44	42	42/44
TOSHIBA	TC538000A	TC578200	TC538200A	TC5716200	TC5316200A TC5316200B TC5316210B
AMD					
Fujitsu			MB838200		MB831620
Hitachi	HN62308B		HN62408		HN624016
Intel		27C800			
Matsushita	MN238002		MN238000		MN2316000
Mitsubishi	M5M23801		M5M23800		M5M23160
NEC			μPD23C8000		μPD23C16000
OKI	MSM538001A		MSM538002A		
Sharp	LH538100		LH538000		LH5316000
TI					

3. Package

Dual in-Line Package (DIP)

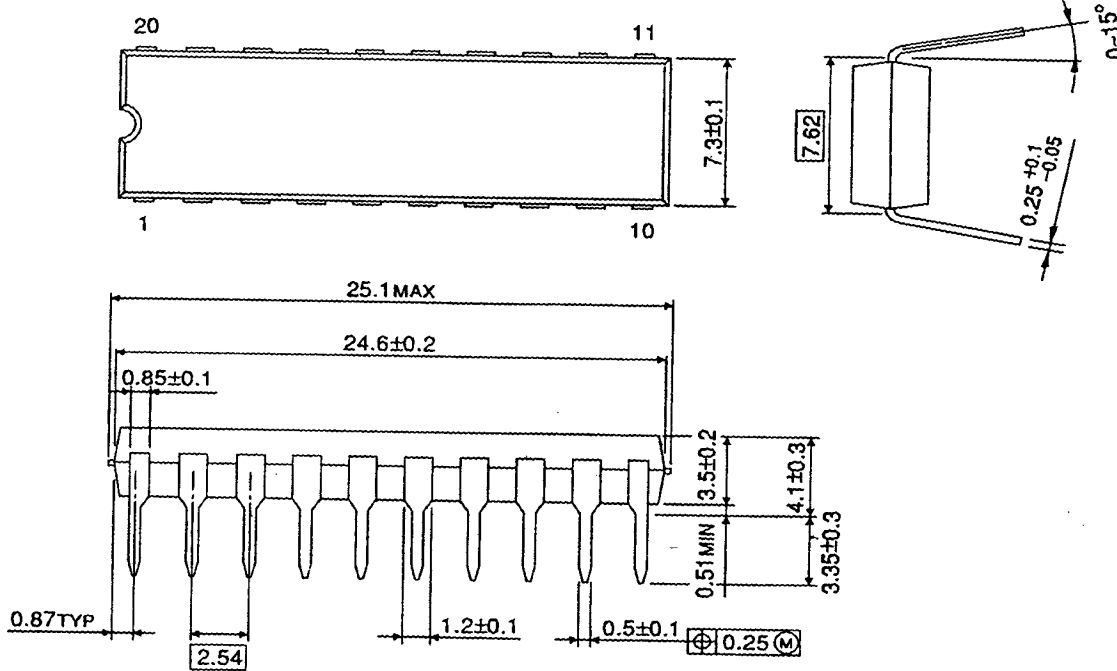
Package Name	Device Group	Device Name
DIP18-P-300C	Dynamic RAM	TC511000AP, TC511001AP, TC511002AP, TC511000BP, TC511001BP, TC511002BP
DIP18-P-300E	Dynamic RAM	TC514100AP, TC514101AP, TC514102AP
DIP20-P-300B	Dynamic RAM	TC514256AP, TC514258AP, TC514266AP, TC514256BP, TC514258BP, TC514266BP
DIP20-P-300C	Dynamic RAM	TC514400AP, TC514402AP, TC514410AP
DIP22-P-300	High speed SRAM	TC55416P-H
DIP24-P-300B	High speed SRAM	TC55417P-H, TC55B417P, TC55464P, TC55B464P
DIP28-P-300B	Static RAM	TC55257BSP
	High Speed SRAM	TC5588P, TC55B88P, TC5589P, TC55465P, TC55B465P, TC55328P, TC55B328P
	Pseudo SRAM	TC51832ASP
DIP28-P-600	Static RAM	TC5564AP, TC55257BP
	Pseudo SRAM	TC51832AP
	One Time PROM	TC54256AP, TC54512AP
	Flash E ² PROM	TC58257AP
	Mask ROM	TC531000CP
DIP32-P-300	High speed SRAM	TC55329P, TC55B329P
	Pseudo SRAM	TC518128ASP, TC518129ASP, TC518128BSP, TC518129BSP
DIP32-P-400	High speed SRAM	TC55B8128P
DIP32-P-600	Static RAM	TC551001AP, TC554002P
	Pseudo SRAM	TC518128AP, TC518129AP, TC518128BP, TC518129BP, TC518512P
	One Time PROM	TC541000/1AP, TC54H1000/1AP, TC544000P, TC544000AP
	Flash/NAND E ² PROM	TC584000P
	Mask ROM	TC531001CP, TC532000AP, TC534000AP, TC538000AP
DIP40-P-600	One Time PROM	TC54H1024AP, TC544200P, TC544096P
	Mask ROM	TC531024P, TC534200P
	Video Memory	TC521000P
DIP42-P-600	Mask ROM	TC538200AP, TC5316200AP, TC5316200BP, TC5316210BP

DIP18-P-300C

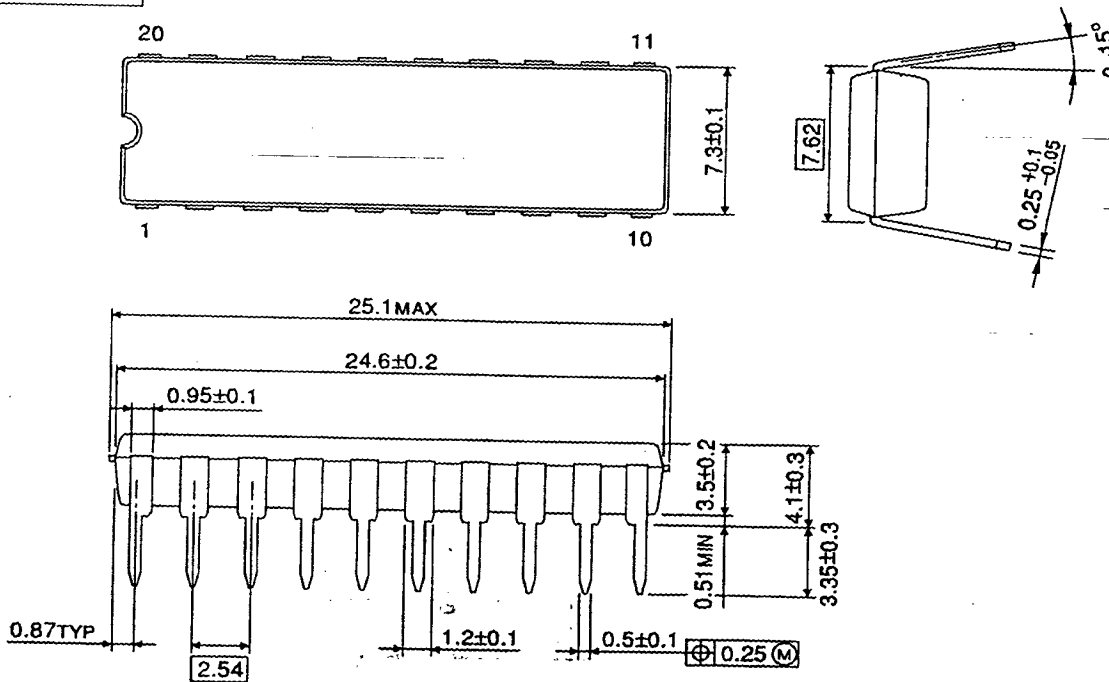


DIP20-P-300B

Unit in mm

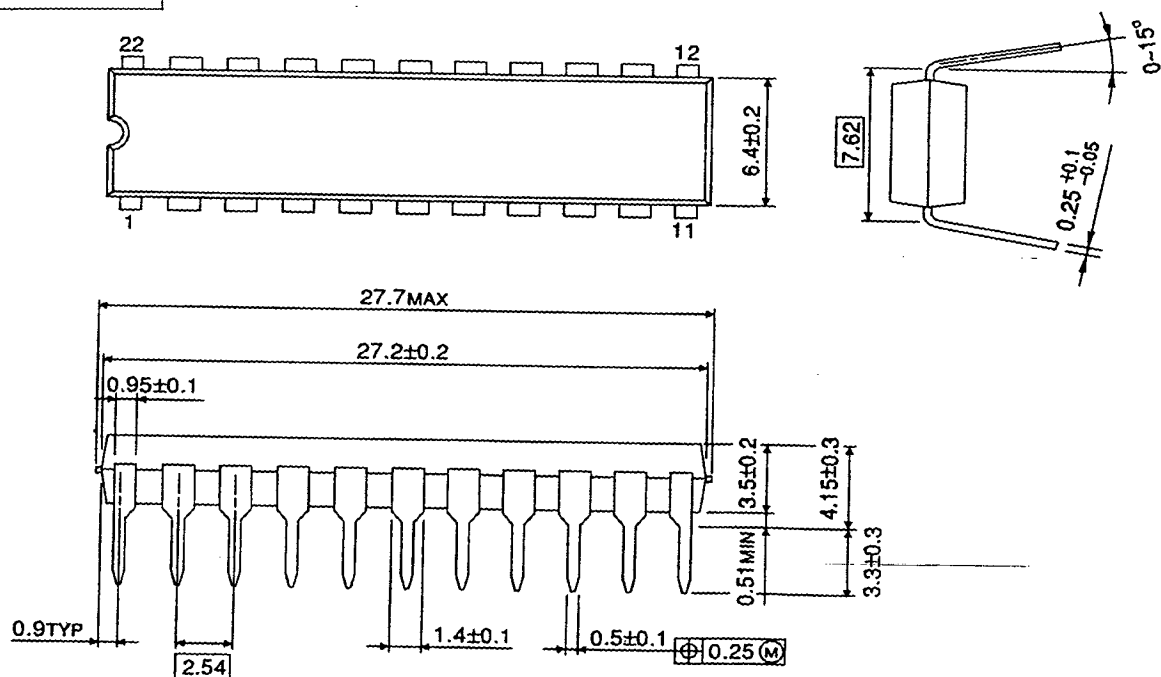


DIP20-P-300C

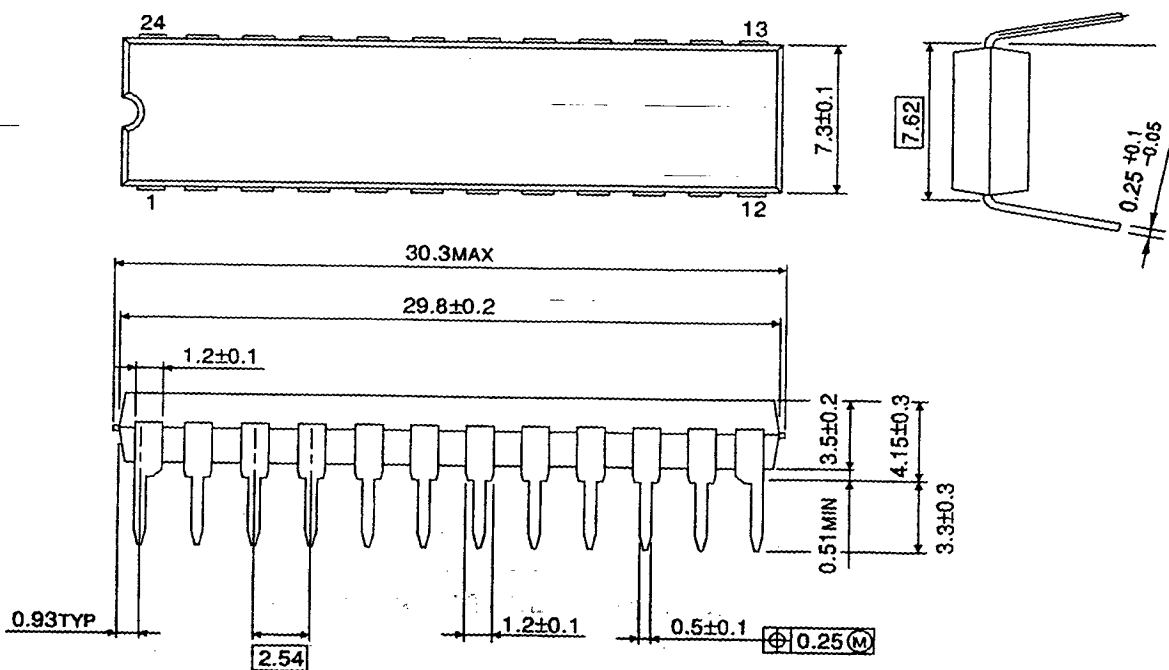


Unit in mm

DIP22-P-300

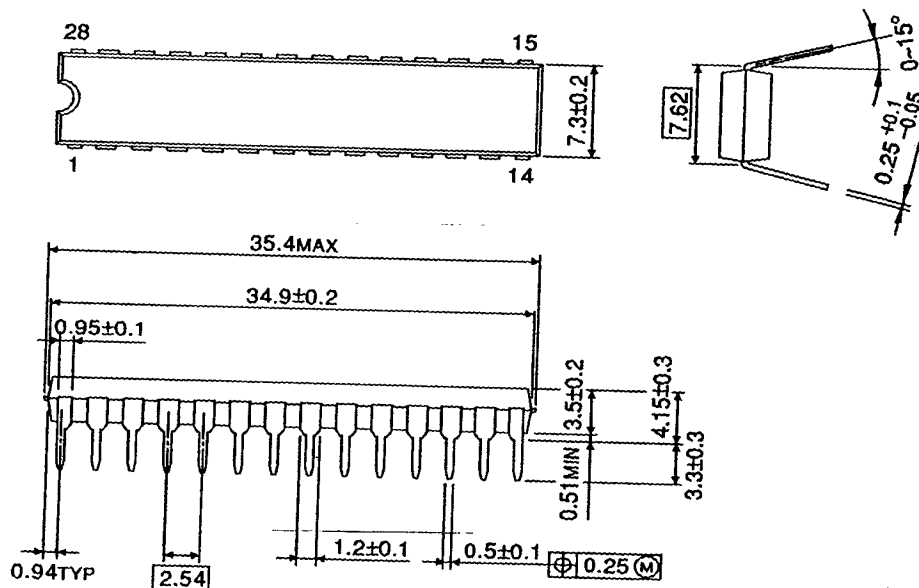


DIP24-P-300B

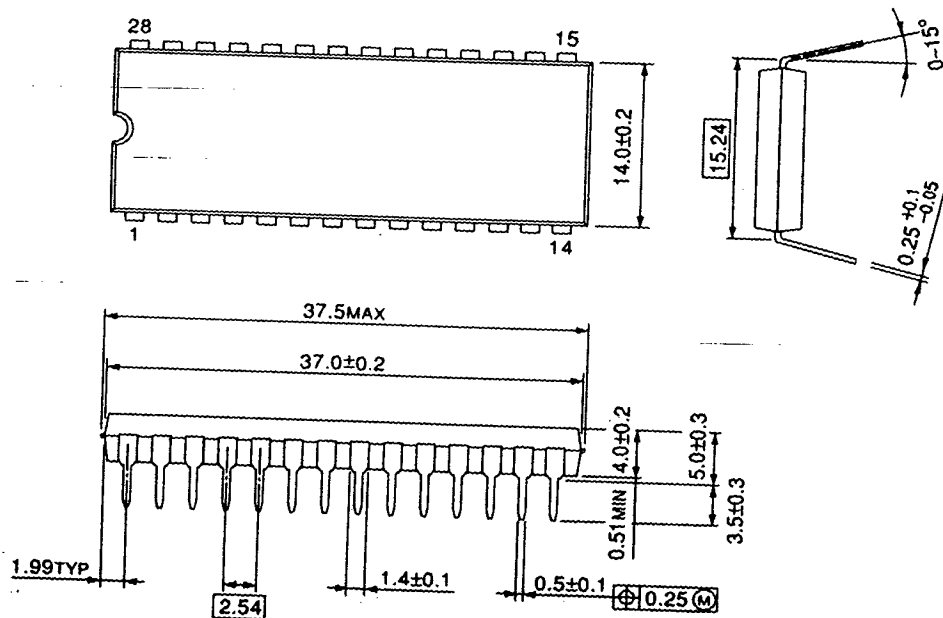


DIP28-P-300B

Unit in mm

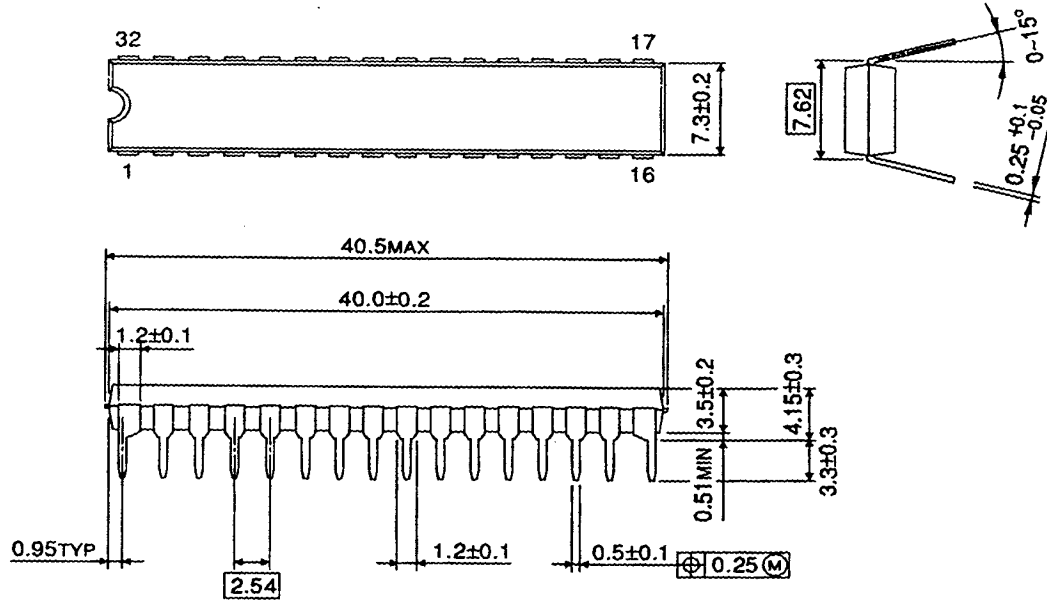


DIP28-P-600

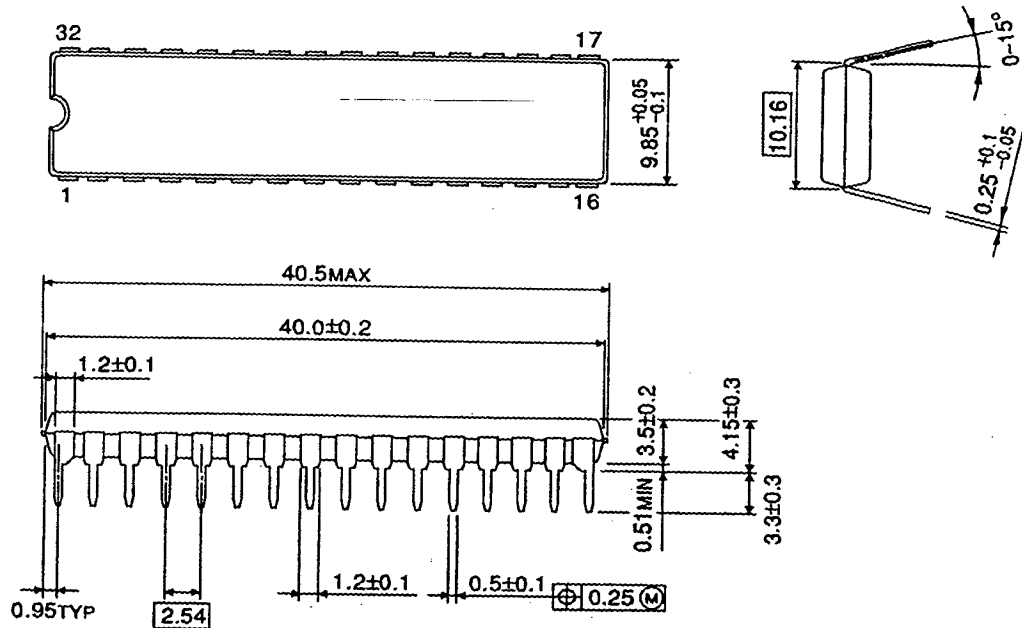


Unit in mm

DIP32-P-300

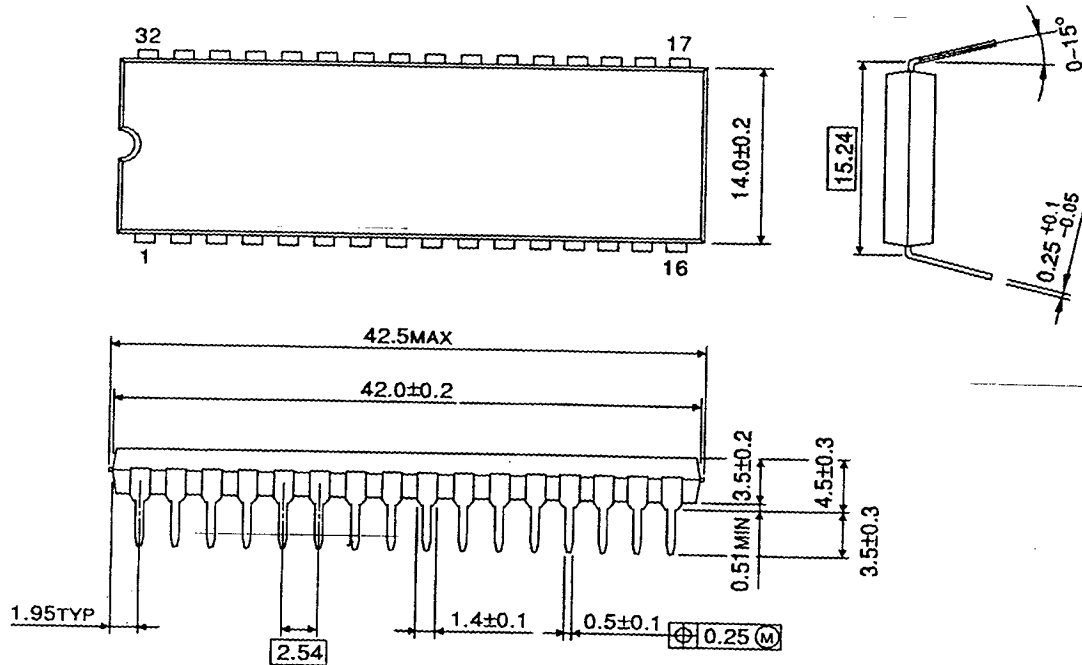


DIP32-P-400

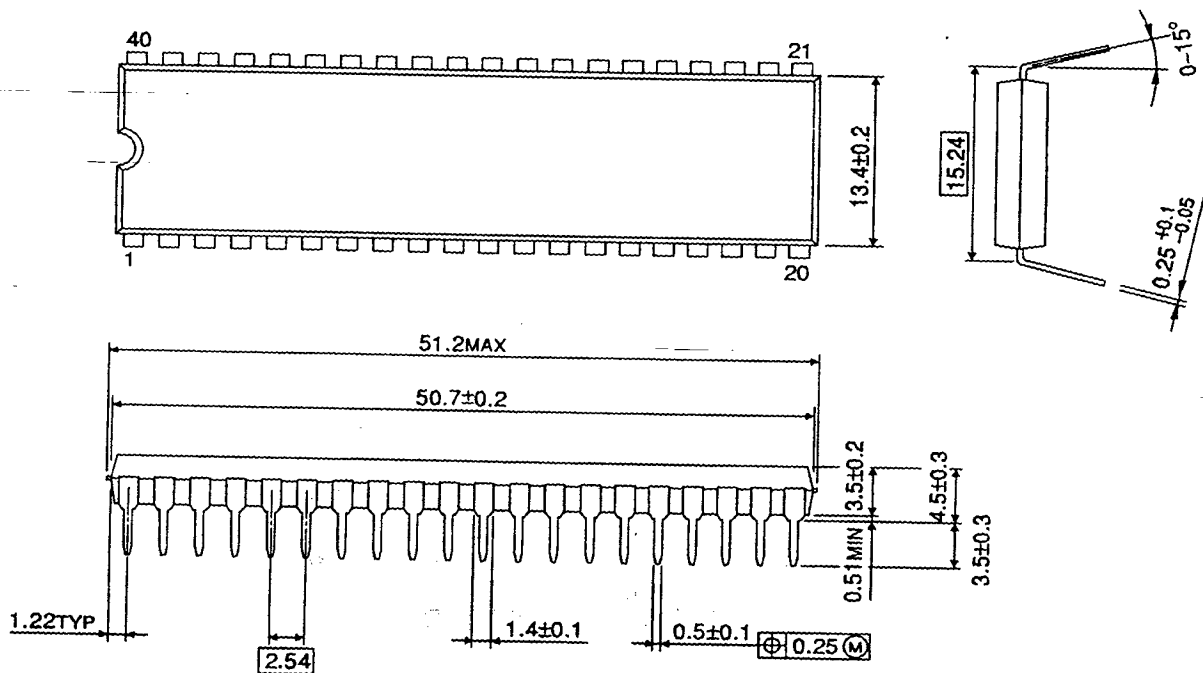


Unit in mm

DIP32-P-600

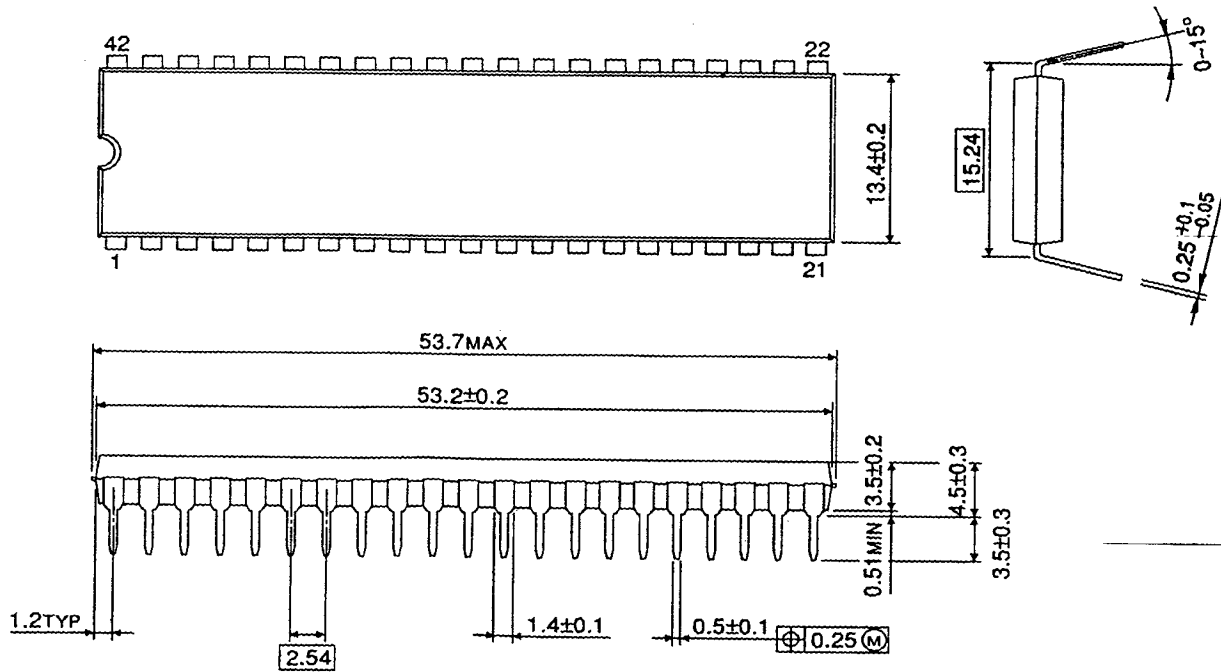


DIP40-P-600



Unit in mm

DIP42-P-600

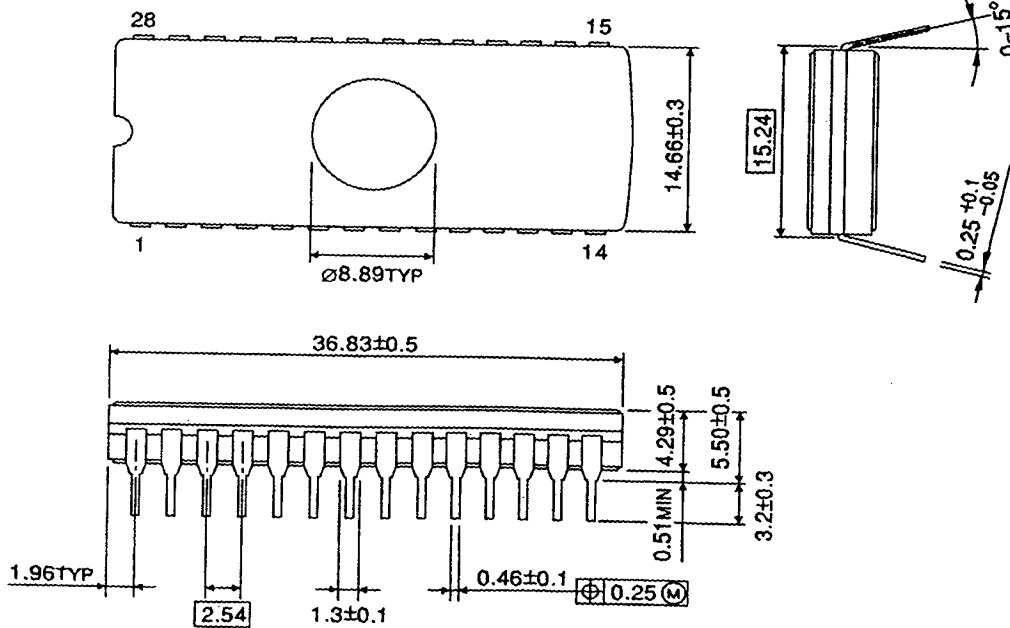


Cerdip DIP

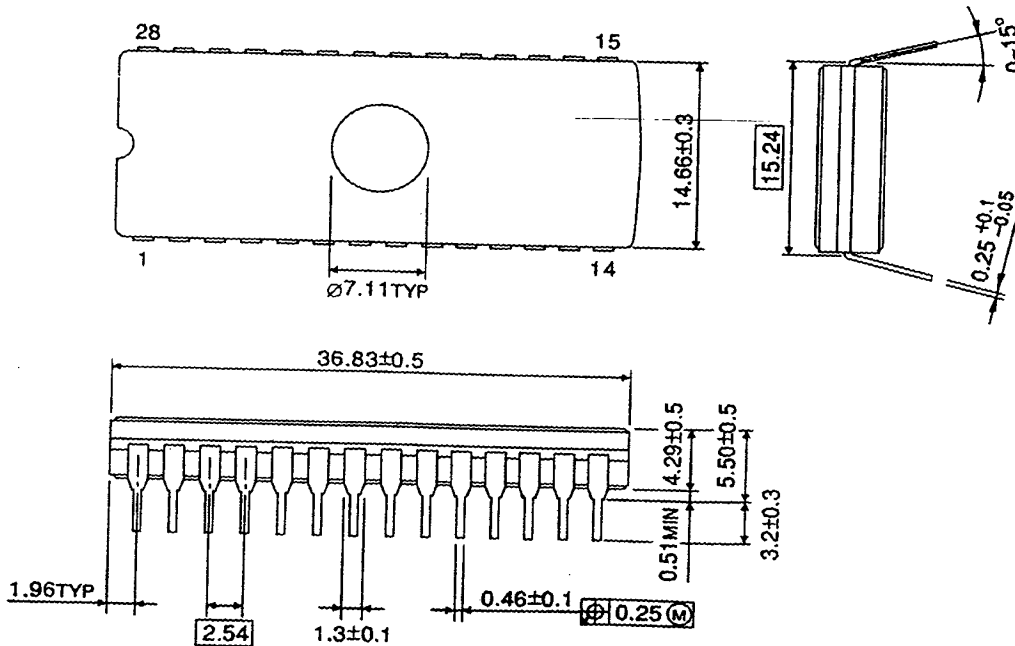
Package Name	Device Group	Device Name
WDIP28-G-600	EPROM	TC57512AD
WDIP28-G-600A	EPROM	TC57256AD, TC57H256D
WDIP32-G-600	EPROM	TC571000/1AD, TC57H1000/1AD
WDIP32-G-600A	EPROM	TC574000D
WDIP32-G-600B	EPROM	TC574000AD
WDIP40-G-600A	EPROM	TC57H1024AD, TC57H1025AD
WDIP40-G-600B	EPROM	TC574200D, TC574096D
WDIP42-G-600A	EPROM	TC578200D
WDIP42-G-600B	EPROM	TC5716200D

Unit in mm

WDIP28-G-600

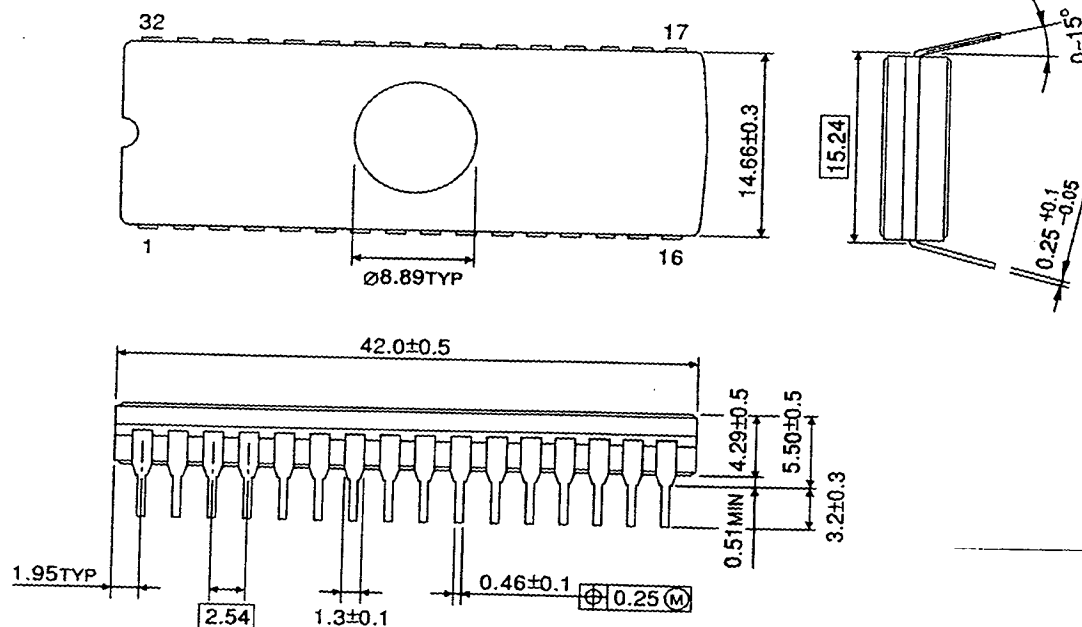


WDIP28-G-600A

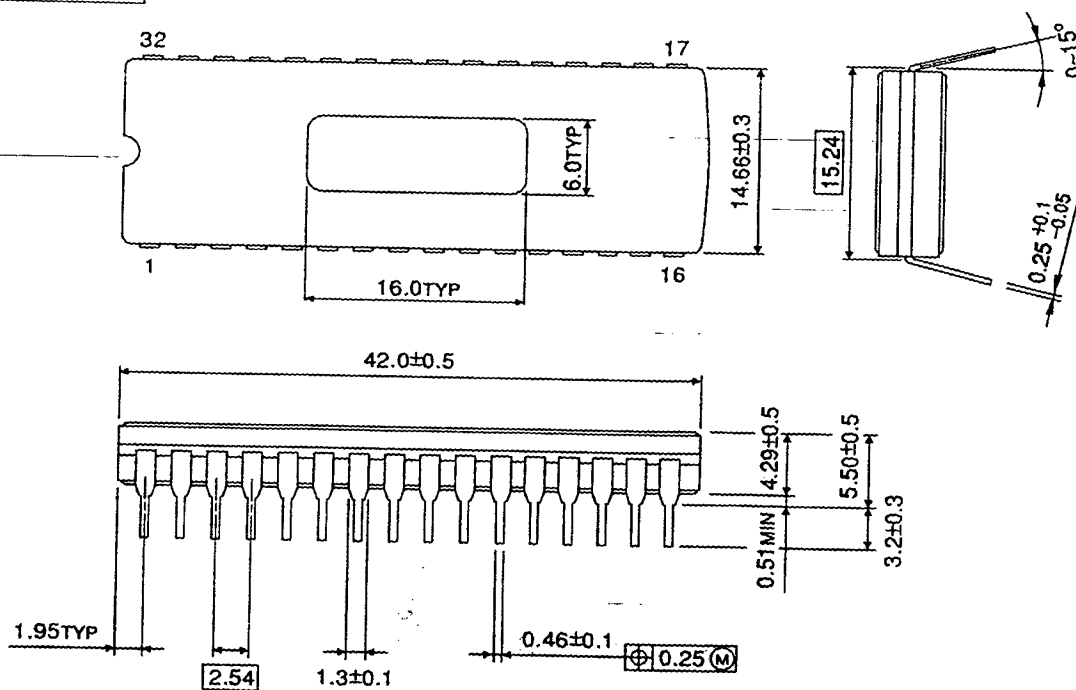


Unit in mm

WDIP32-G-600



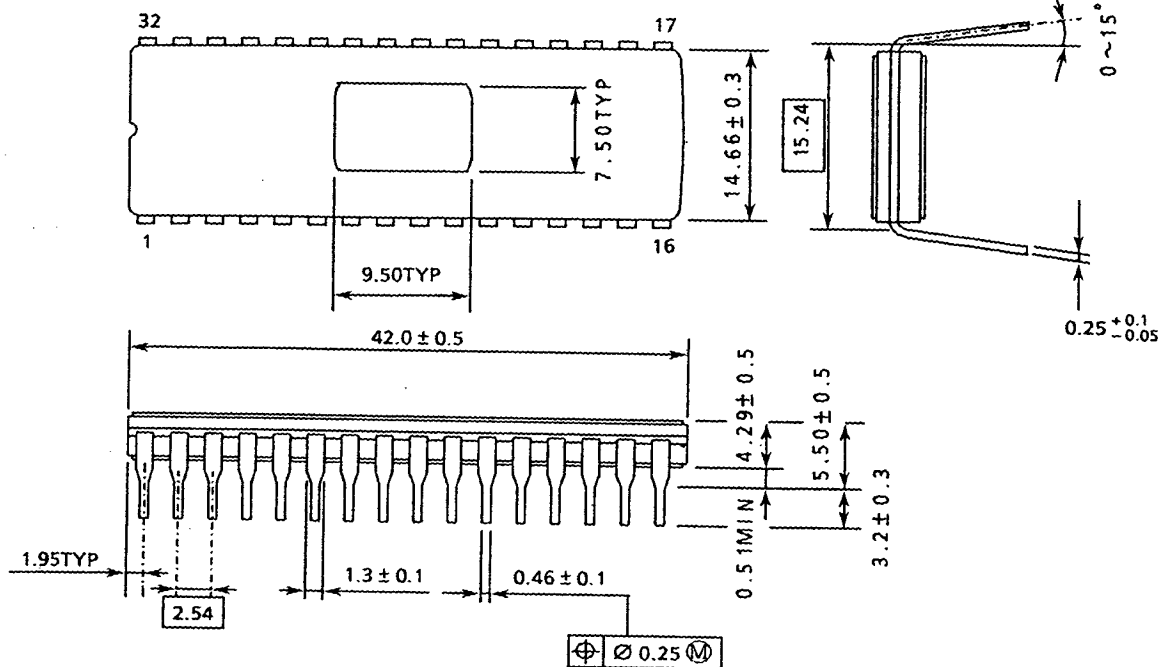
WDIP32-G-600A



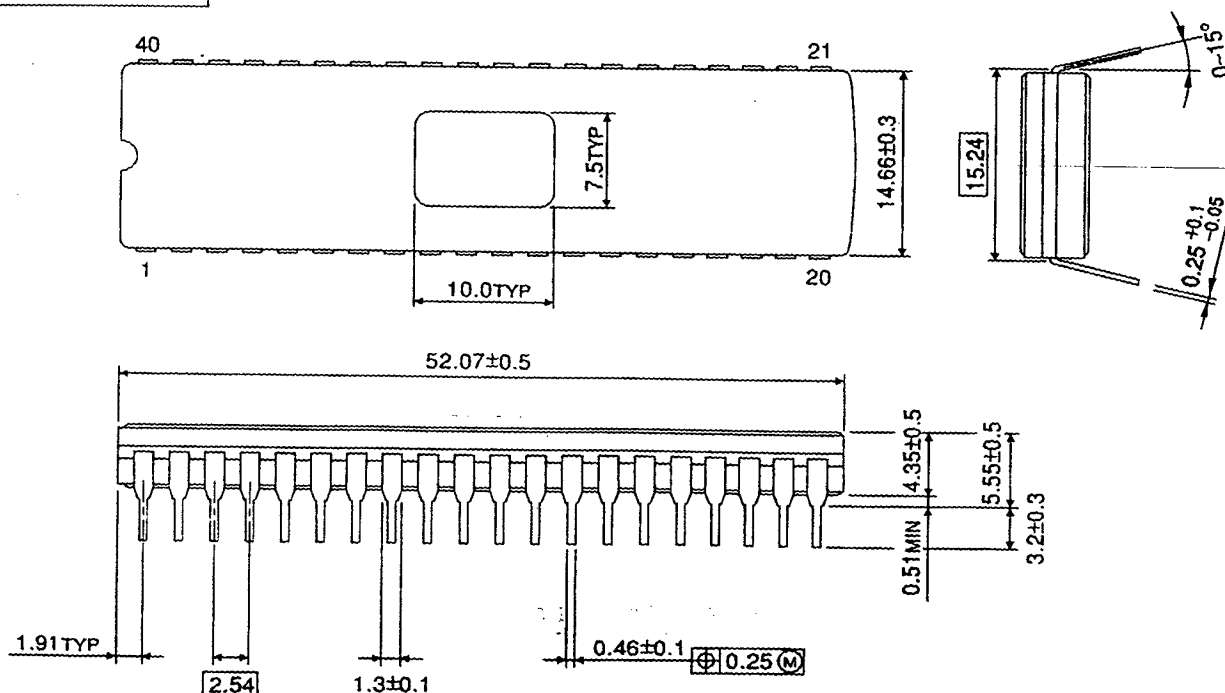
Unit in mm

WDIP32-G-600B

TENTATIVE

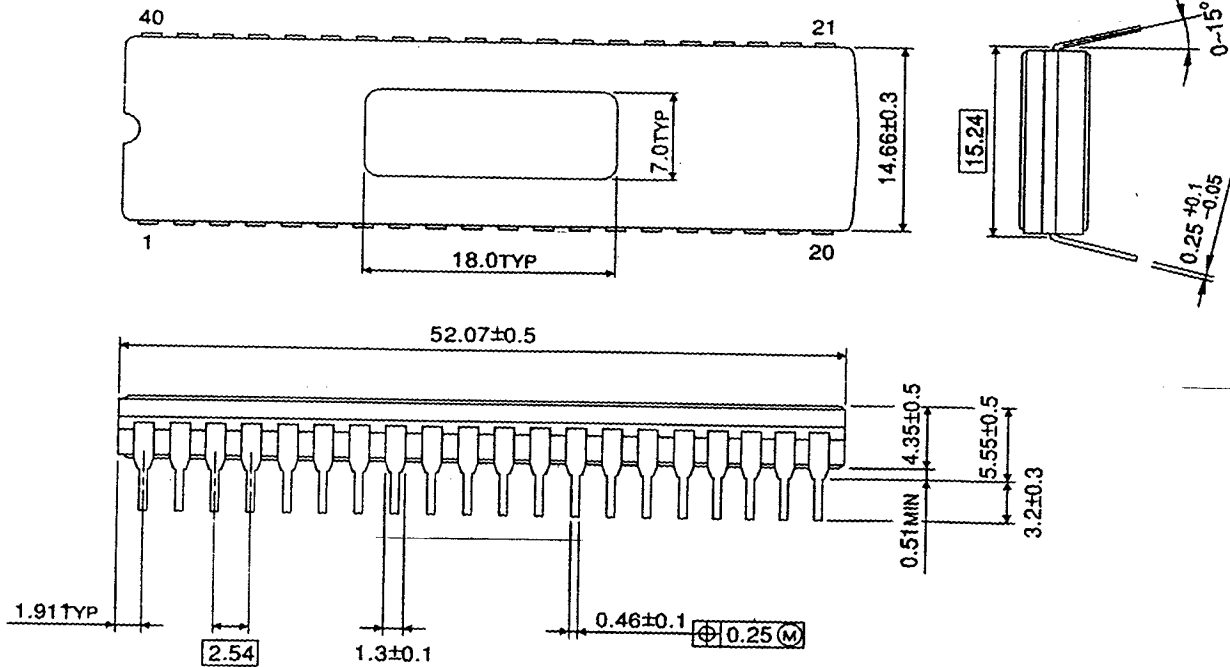


WDIP40-G-600A

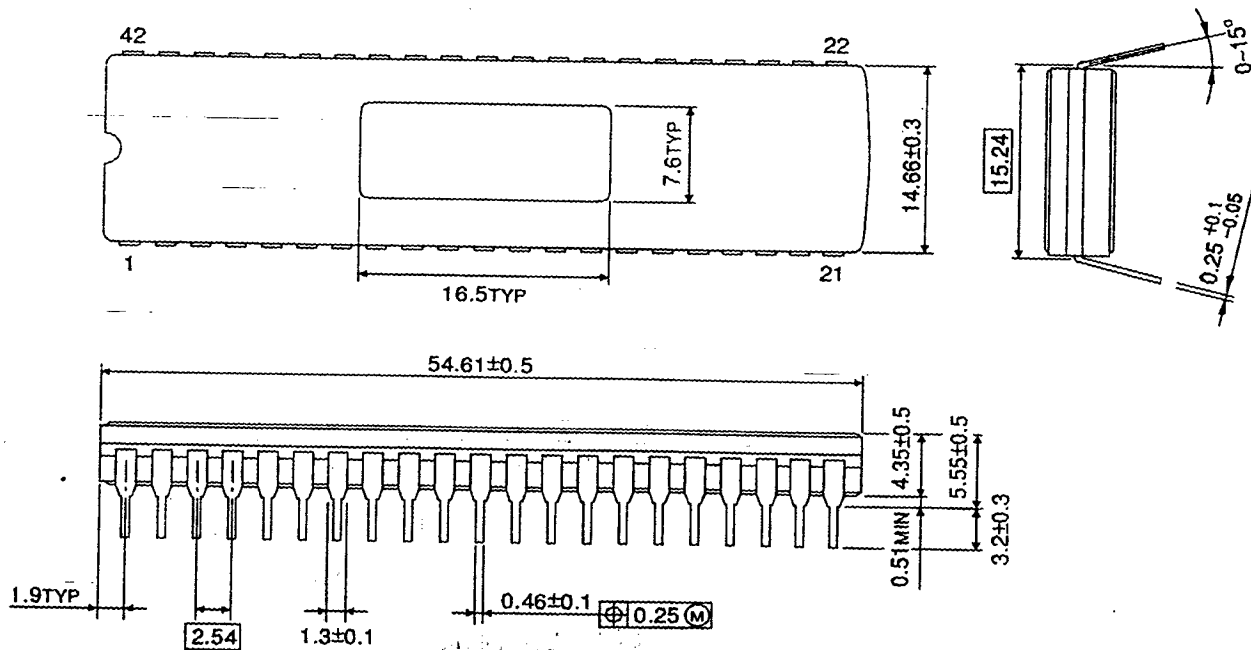


WDIP40-G-600B

Unit in mm



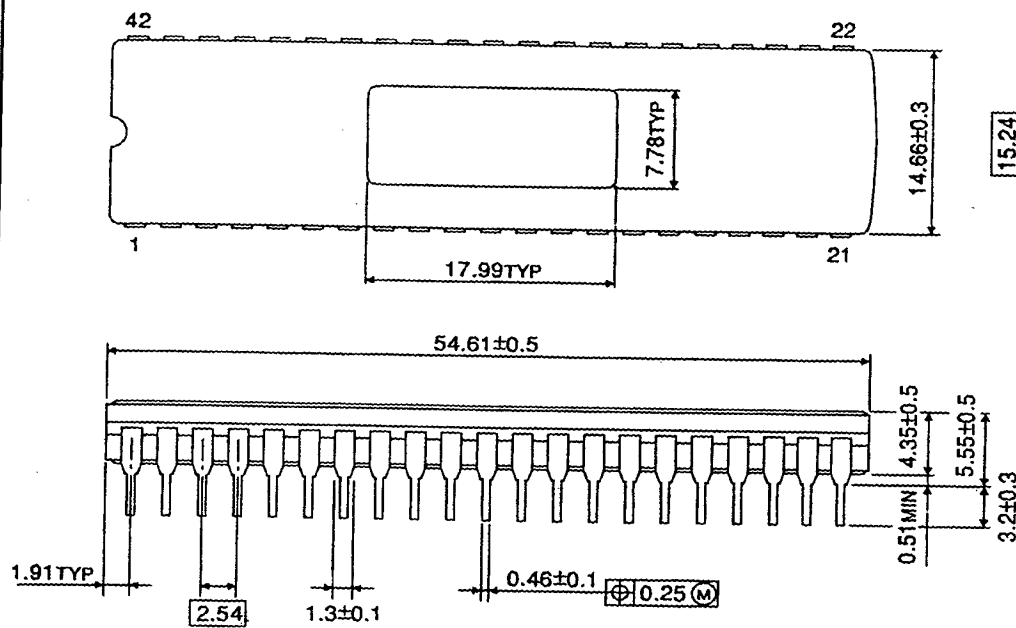
WDIP42-G-600A



WDIP42-G-600B

Unit in mm

TENTATIVE

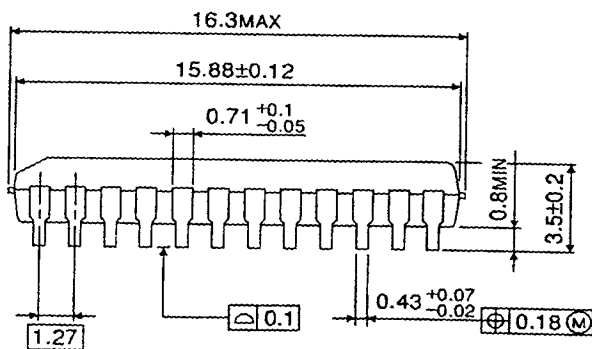
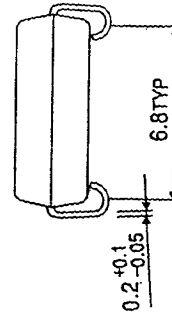
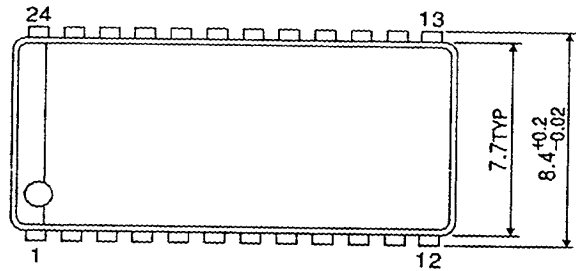


Small Out-line J-lead Package (SOJ)

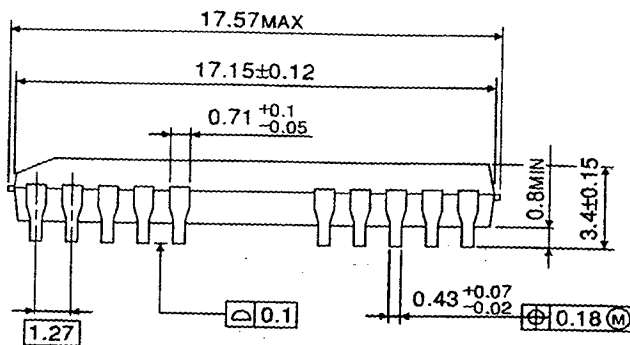
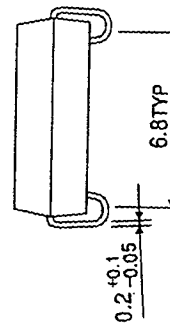
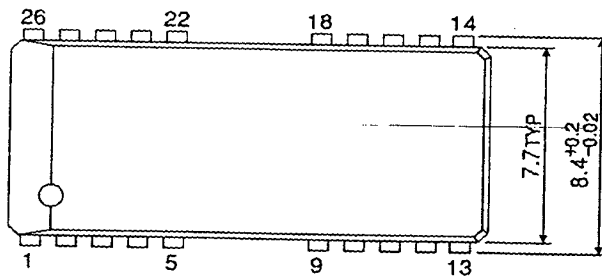
Package Name	Device Group	Device Name
SOJ24-P-300A	High speed SRAM	TC55417J-H, TC55B417J, TC55464J, TC55B464J
SOJ26-P-300	Dynamic RAM	TC511000AJ, TC511001AJ, TC511002AJ, TC511000BJ, TC511001BJ, TC511002BJ
SOJ26-P-300A	Dynamic RAM	TC514256AJ, TC514258AJ, TC514266AJ, TC514256BJ, TC514258BJ, TC514266BJ
SOJ26-P-350	Dynamic RAM	TC514100ASJ, TC514101ASJ, TC514102ASJ, TC514400ASJ, TC514402ASJ, TC514410ASJ
SOJ26-P-350	Dynamic RAM	TC514100BSJ, TC514101BSJ, TC514102BSJ, TC514400BSJ, TC514402BSJ, TC514410BSJ
SOJ28-P-300A	High speed SRAM	TC5588J, TC55B88J, TC5589J, TC55465J, TC55B465J, TC55328J, TC55B328J
SOJ28-P-400	Dynamic RAM	TC514800AJ, TC514900AJ
SOJ28-P-400	Video RAM	TC524256BJ, TC524258BJ, TC524259BJ
SOJ28-P-400A	High Speed SRAM	TC55B4256J
SOJ28-P-400C	Dynamic RAM	TC5116100J, TC5116101J, TC5116102J, TC5116400J, TC5116402J, TC5116410J, TC5117400J, TC5117402J, TC5117410J
SOJ32-P-300	Dynamic RAM	TC5116800ANJ, TC5117800ANJ
SOJ32-P-400A	High speed SRAM	TC55329J, TC55B329J
SOJ32-P-400A	Dynamic RAM	TC5116800AJ, TC5117800AJ, TC5116900AJ, TC5117900AJ
SOJ40-P-400	High speed SRAM	TC55B4257J, TC55B8128J, TC551402J
SOJ40-P-400	Dynamic RAM	TC511664BJ, TC511665BJ, TC514260BJ, TC514170BJ, TC514273BJ, TC514280BJ, TC514190BJ
SOJ40-P-400	Video RAM	TC521000J, TC528126BJ, TC528128BJ, TC528257J, TC528267J
SOJ42-P-400	High speed SRAM	TC551632J
SOJ42-P-400	Dynamic RAM	TC5116160AJ, TC5116170AJ, TC5118160AJ, TC5118170AJ, TC5116180AJ, TC5116190AJ, TC5116180AJ, TC5116190AJ
SOJ44-P-400	High speed SRAM	TC551664J

Unit in mm

SOJ24-P-300A

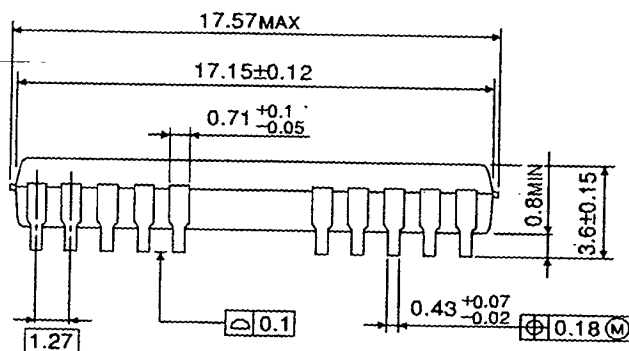
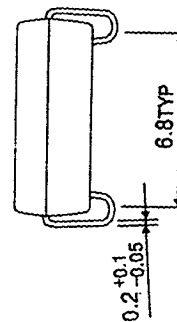
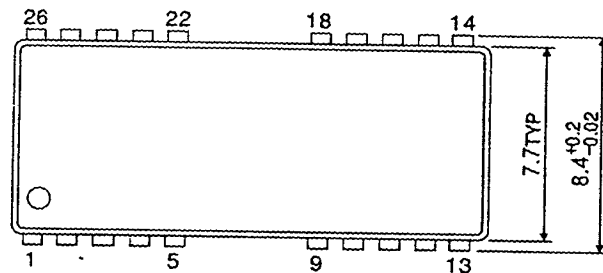


SOJ26-P-300

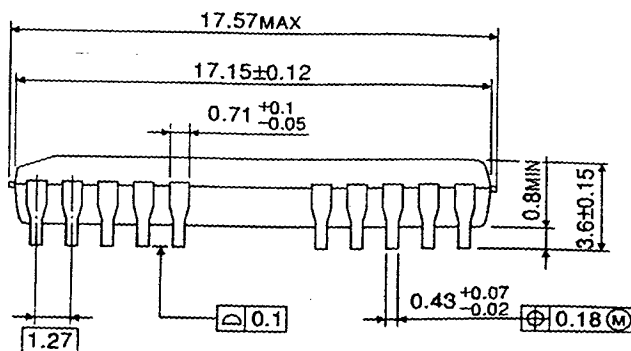
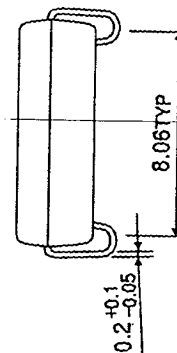
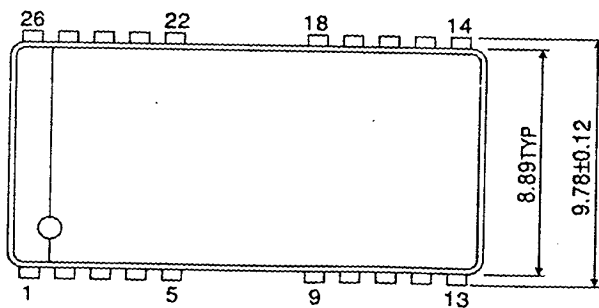


Unit in mm

SOJ26-P-300A

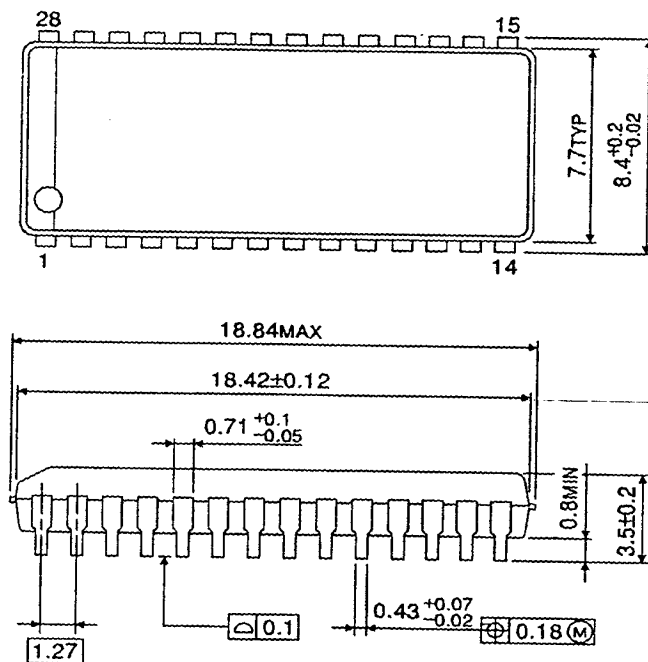


SOJ26-P-350

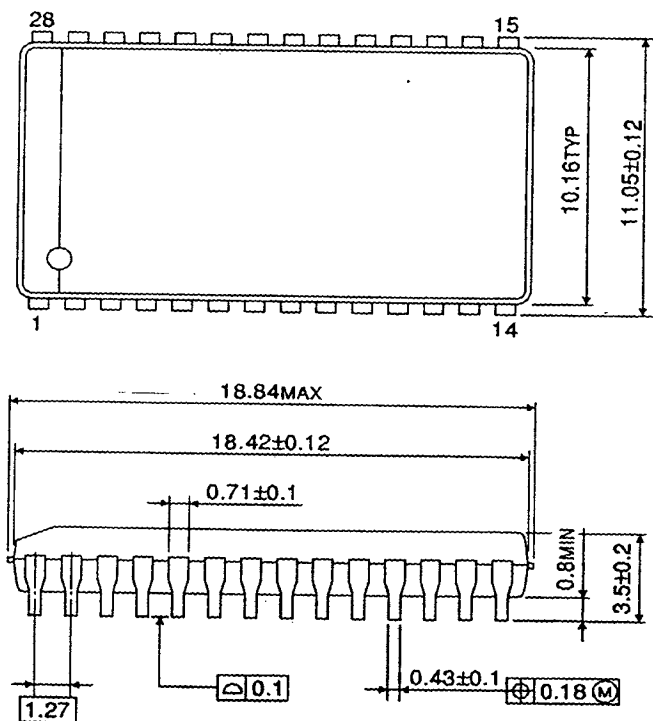


Unit in mm

SOJ28-P-300A



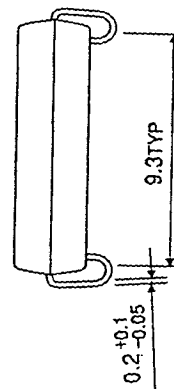
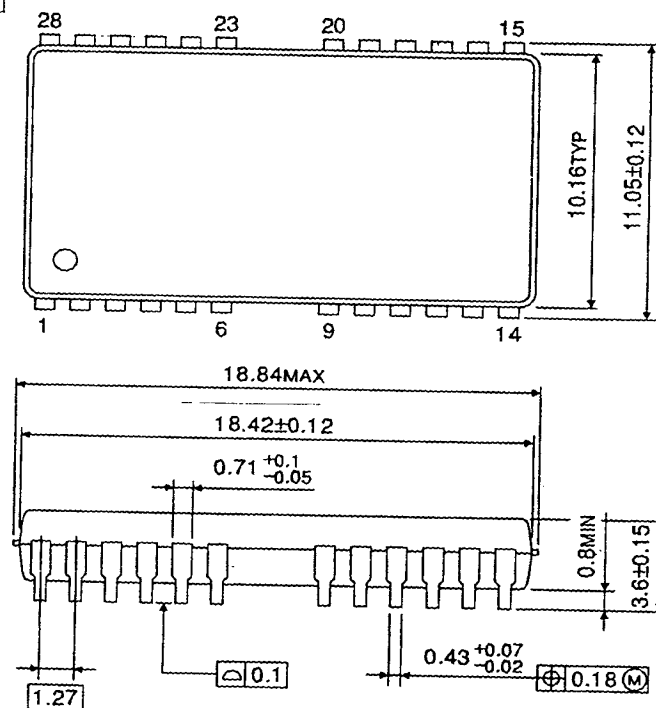
SOJ28-P-400



Unit in mm

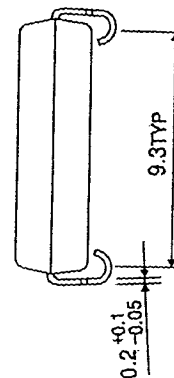
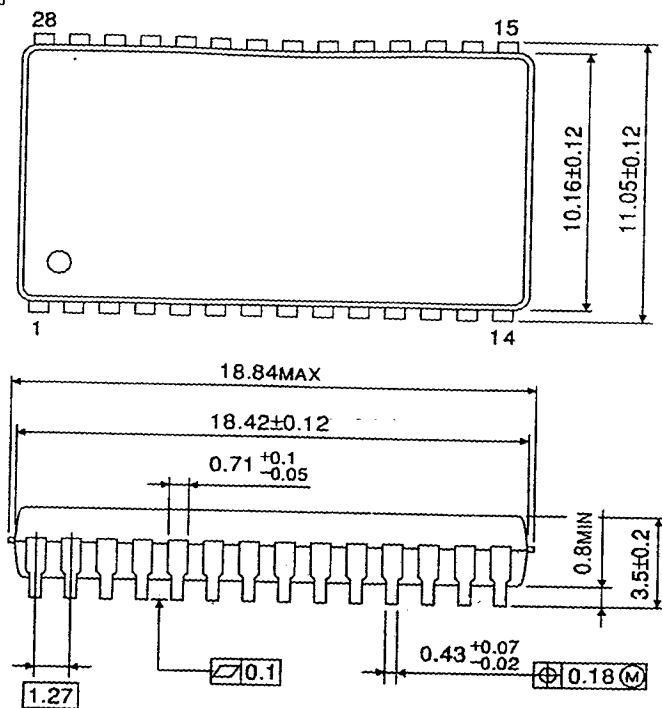
SOJ28-P-400A

TENTATIVE



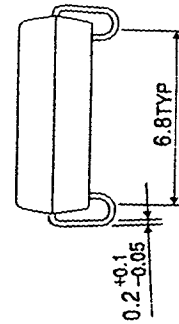
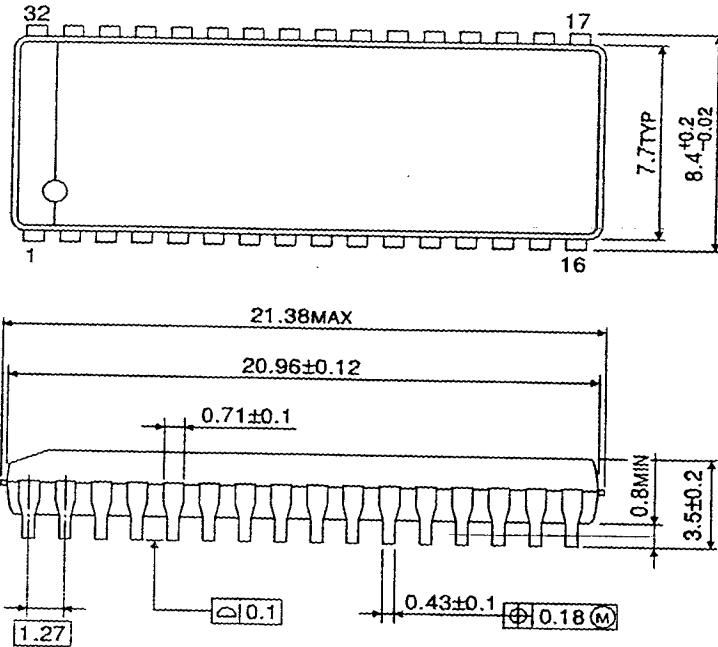
SOJ28-P-400C

TENTATIVE

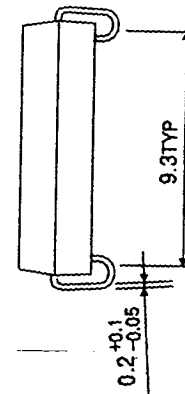
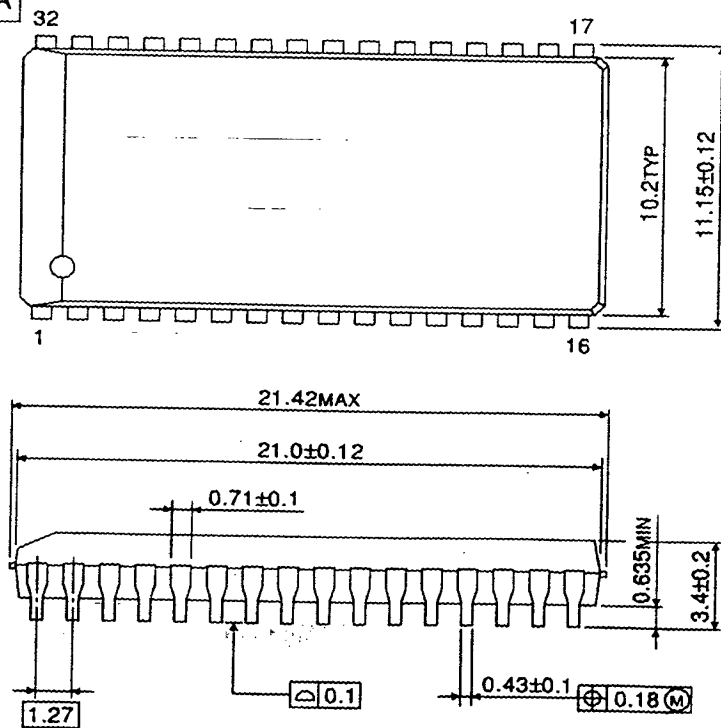


Unit in mm

SOJ32-P-300

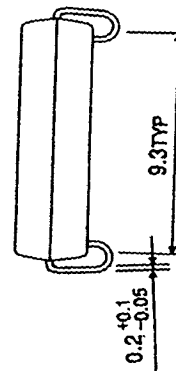
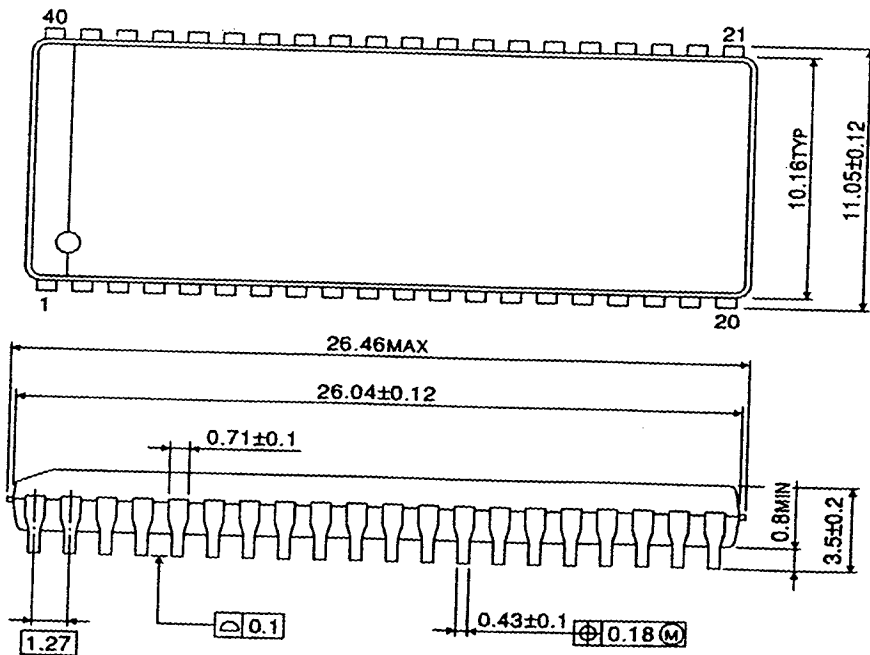


SOJ32-P-400A



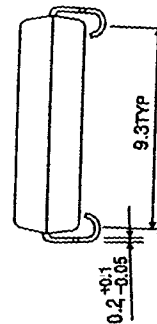
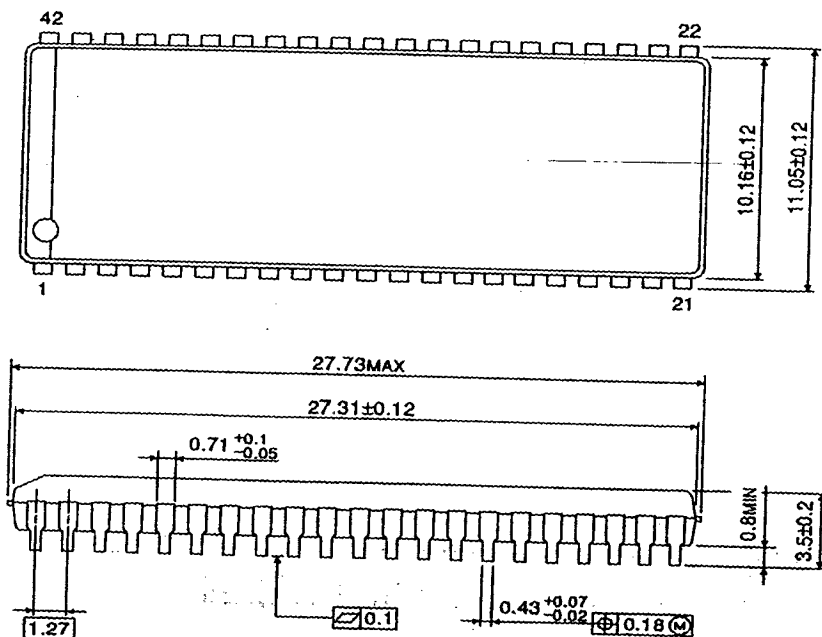
SOJ40-P-400

Unit in mm

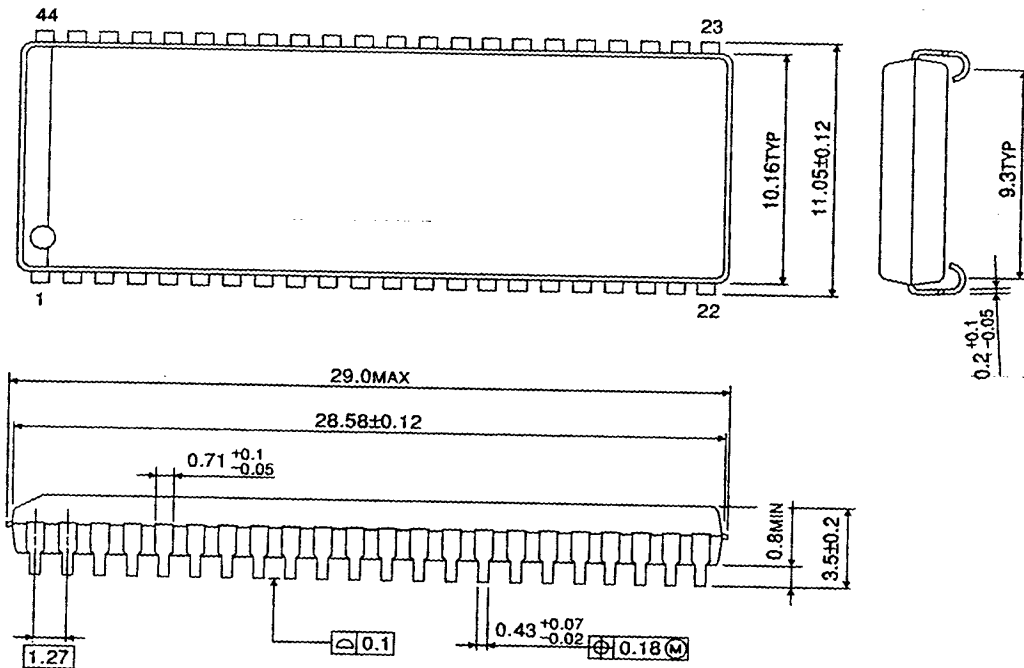


SOJ42-P-400

TENTATIVE



SOJ44-P-400

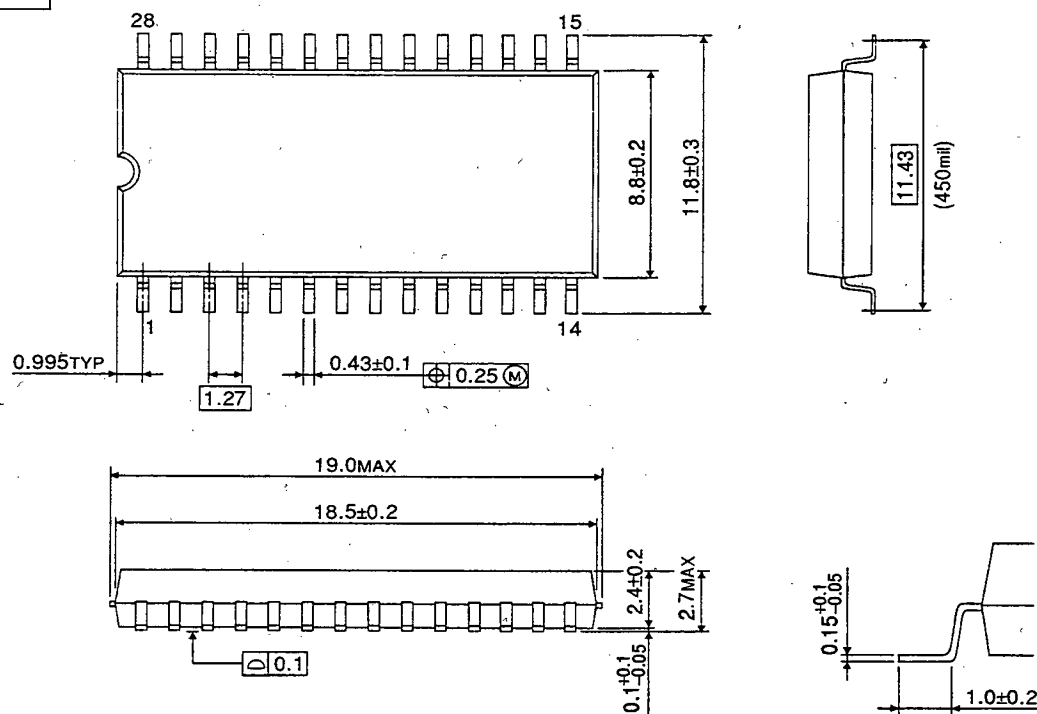


Small Outline L-lead package (SOP)

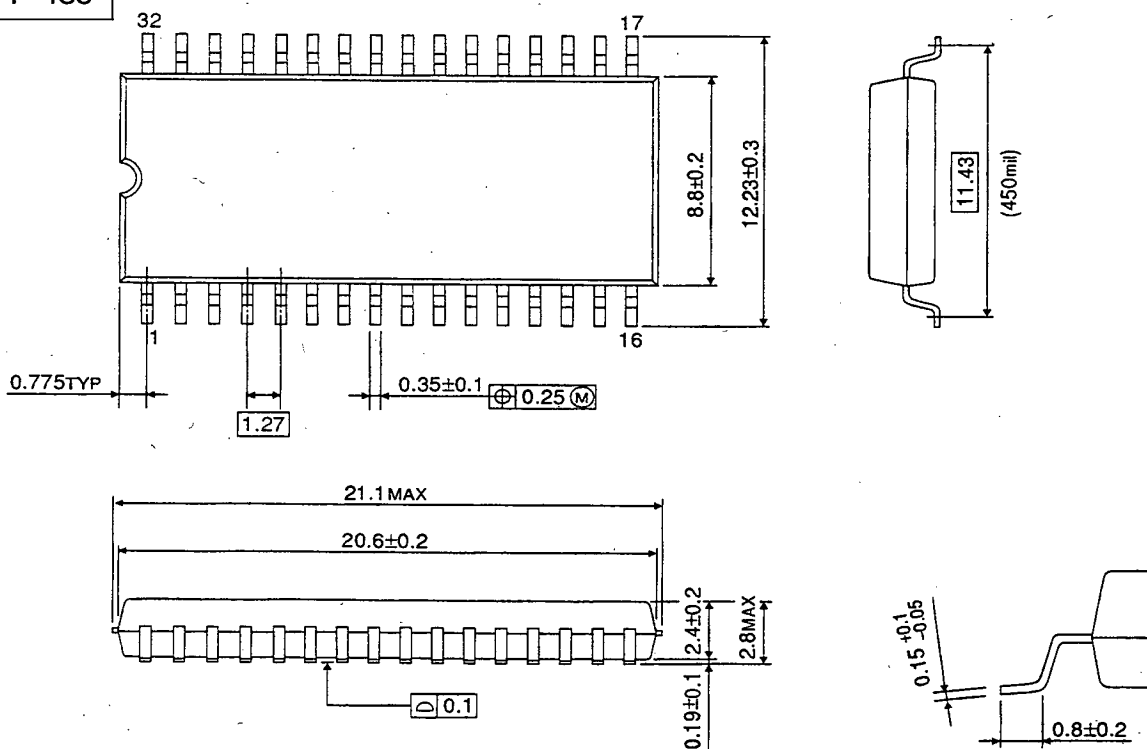
Package Name	Device Group	Device Name
SOP28-P-450	Static RAM	TC5564AF, TC55257BF
	Pseudo SRAM	TC51832AF
	One Time PROM	TC54256AF, TC54512AF
	Flash E ² PROM	TC58257AF
	Mask ROM	TC531000CF
SOP32-P-450	Pseudo SRAM	TC518128AF, TC518129AF, TC518128BF, TC518129BF
SOP32-P-525	Static RAM	TC551001AF, TC554002F
	Pseudo SRAM	TC518128AFW, TC518129AFW, TC518128BFW, TC518129BFW, TC518512F
	One Time PROM	TC541000/1AF, TC54H1000/1AF, TC544000F, TC544000AF
	Flash/NAND E ² PROM	TC584000F
	Mask ROM	TC531001CF, TC532000AF, TC534000AF, TC538000AF
SOP40-P-525	One Time PROM	TC54H1024AF, TC544200F, TC544096F
	Mask ROM	TC531024F, TC534200F
SOP44-P-600	Mask ROM	TC538200AF, TC5316200AF, TC5316200BF, TC5316210BF

Unit in mm

SOP28-P-450

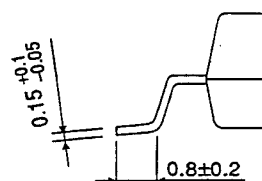
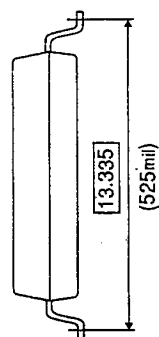
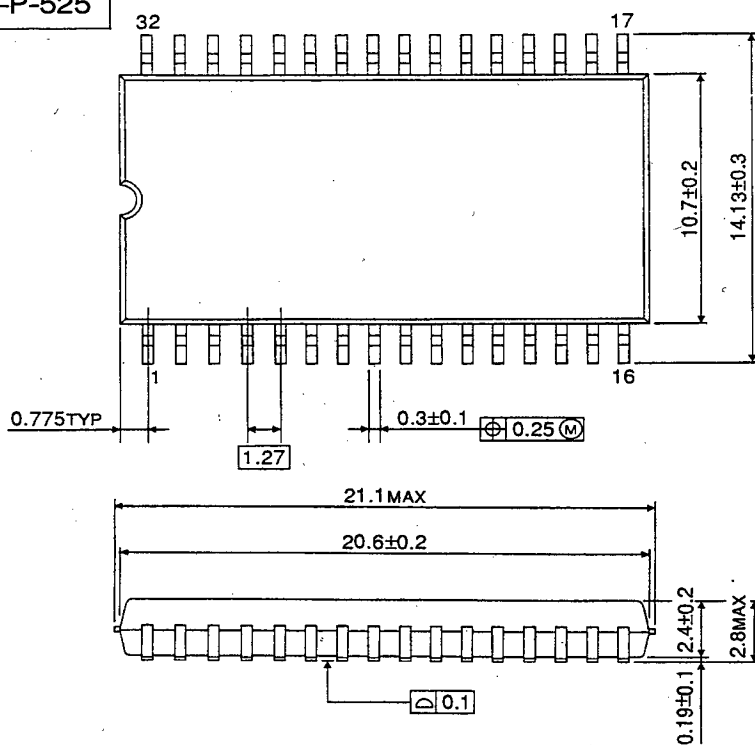


SOP32-P-450

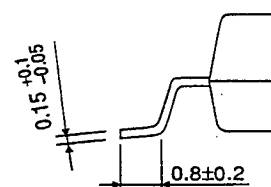
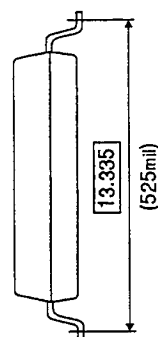
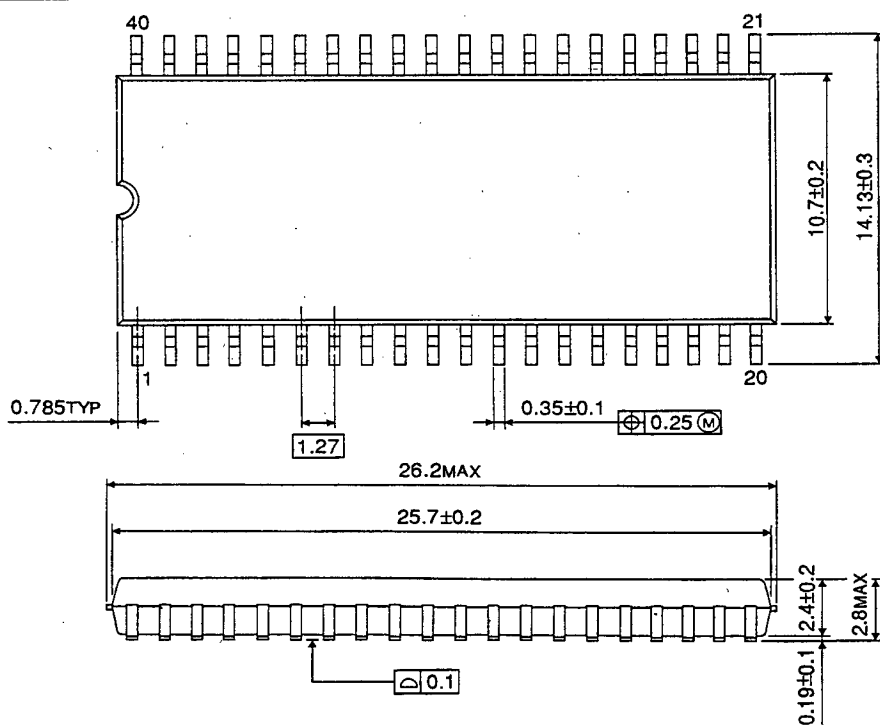


Unit in mm

SOP32-P-525

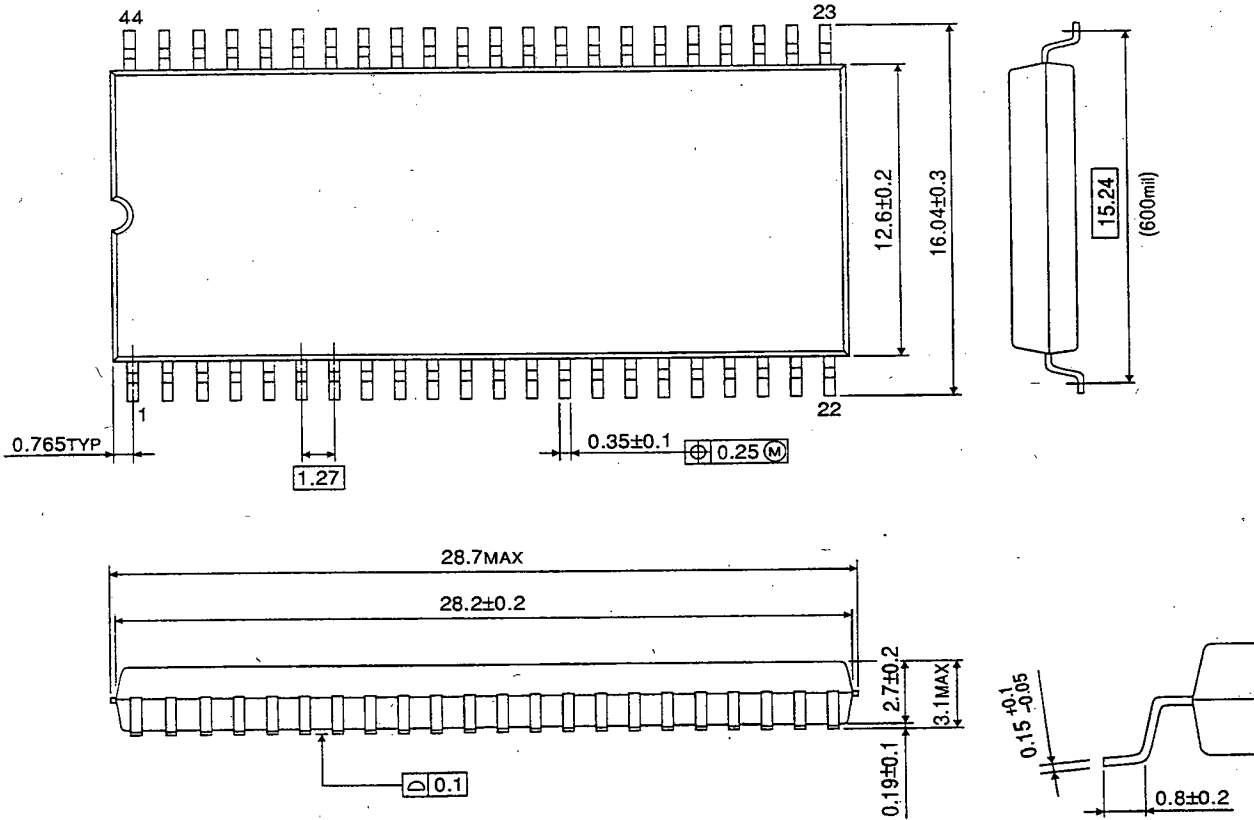


SOP40-P-525



Unit in mm

SOP44-P-600

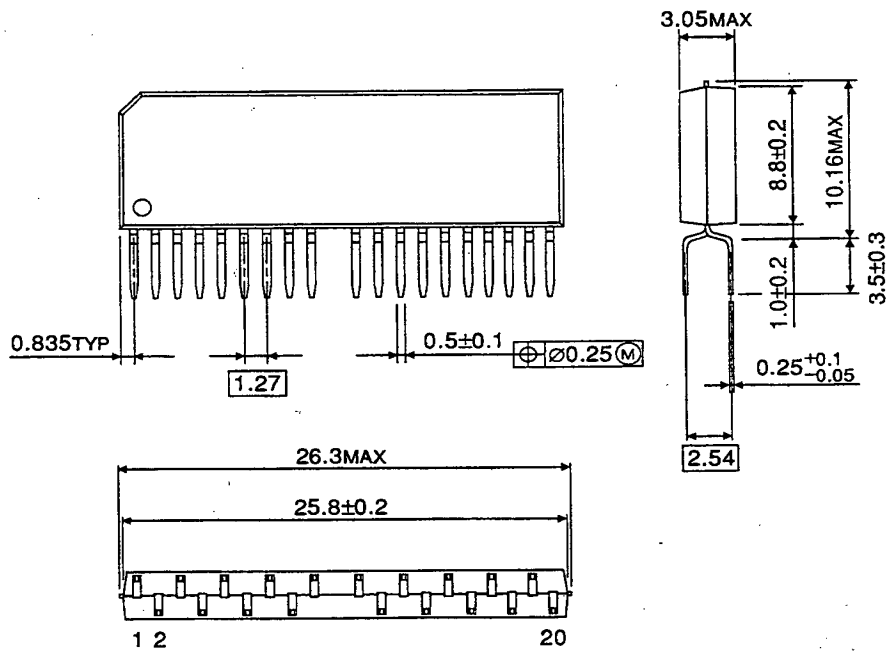


Zig-zag In-line Package (ZIP)

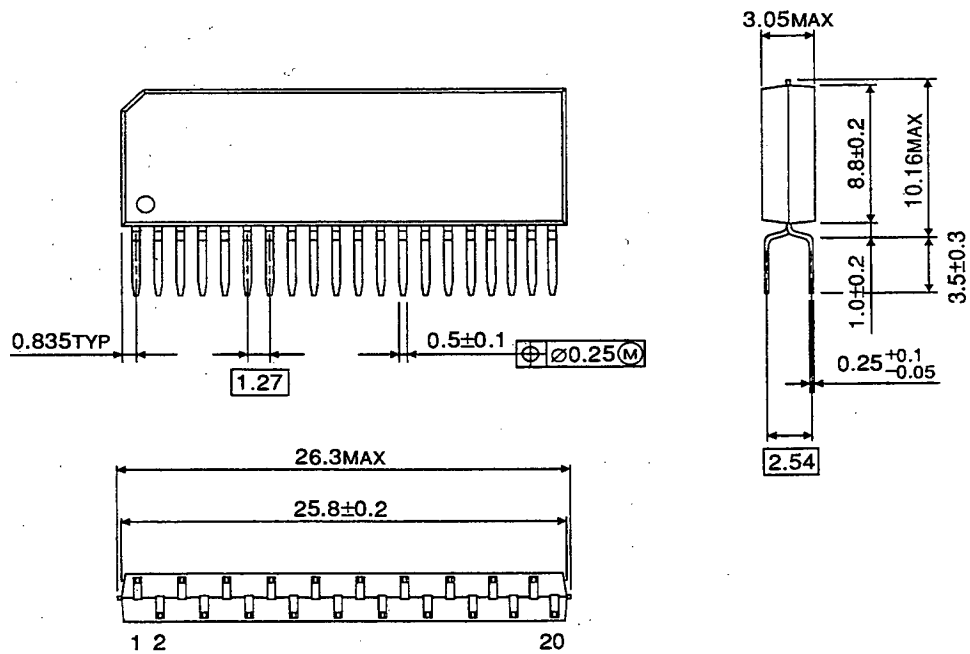
Package Name	Device Group	Device Name
ZIP20-P-400	Dynamic RAM	TC511000AZ, TC511001AZ, TC511002AZ, TC511000BZ, TC511001BZ, TC511002BZ TC514256AZ, TC514258AZ, TC514266AZ, TC514256BZ, TC514258BZ, TC514266BZ
ZIP20-P-400A	Dynamic RAM	TC514100AZ, TC514101AZ, TC514102AZ, TC514400AZ, TC514402AZ, TC514410AZ TC514100BZ, TC514101BZ, TC514102BZ, TC514400BZ, TC514402BZ, TC514410BZ
ZIP24-P-475	Dynamic RAM	TC5116100Z, TC5116101Z, TC5116102Z, TC5116400Z, TC5116402Z, TC5116410Z TC5117400Z, TC5117402Z, TC5117410Z
ZIP28-P-400	Dynamic RAM	TC514800AZ, TC514900AZ
	Video RAM	TC524256BZ, TC524258BZ, TC524259BZ
ZIP28-P-475	Dynamic RAM	TC5116800ANZ, TC5117800ANZ
ZIP32-P-475	Dynamic RAM	TC5116800AZ, TC5117800AZ, TC5116900AZ, TC5117900AZ
ZIP40-P-475	Dynamic RAM	TC511664BZ, TC511665BZ, TC514260BZ, TC514170BZ, TC514273BZ, TC514280BZ, TC514190BZ
	Video RAM	TC528126BZ, TC528128BZ
SZIP40-P-475	Video RAM	TC528257SZ, TC528267SZ
ZIP42-P-475	Dynamic RAM	TC5116160AZ, TC5116170AZ, TC5118160AZ, TC5118170AZ, TC5116180AZ, TC5116190AZ
		TC5118180AZ, TC5118190AZ

Unit in mm

ZIP20-P-400



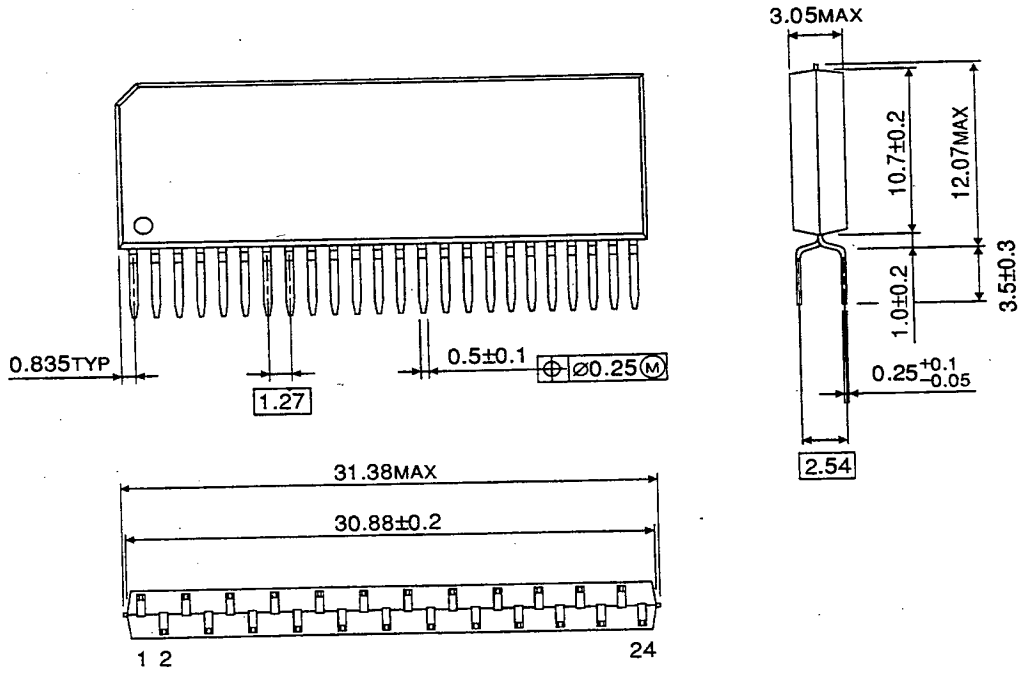
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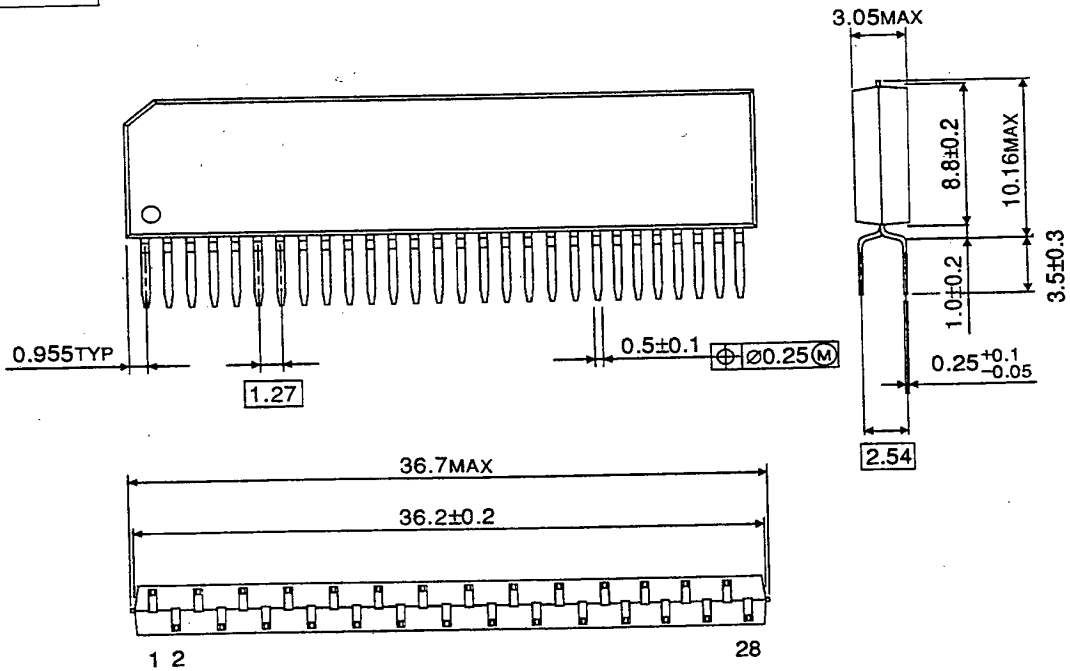
Unit in mm

ZIP24-P-475

TENTATIVE



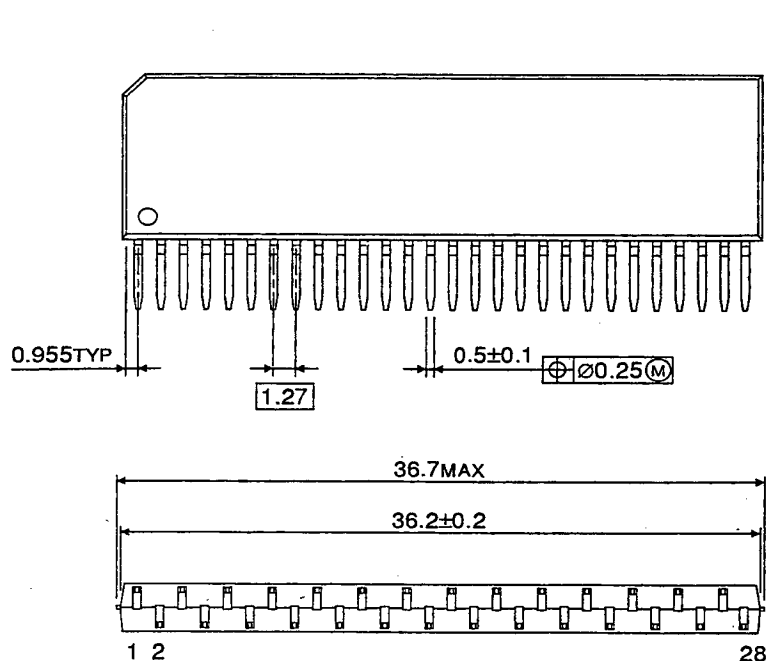
ZIP28-P-400



Unit in mm

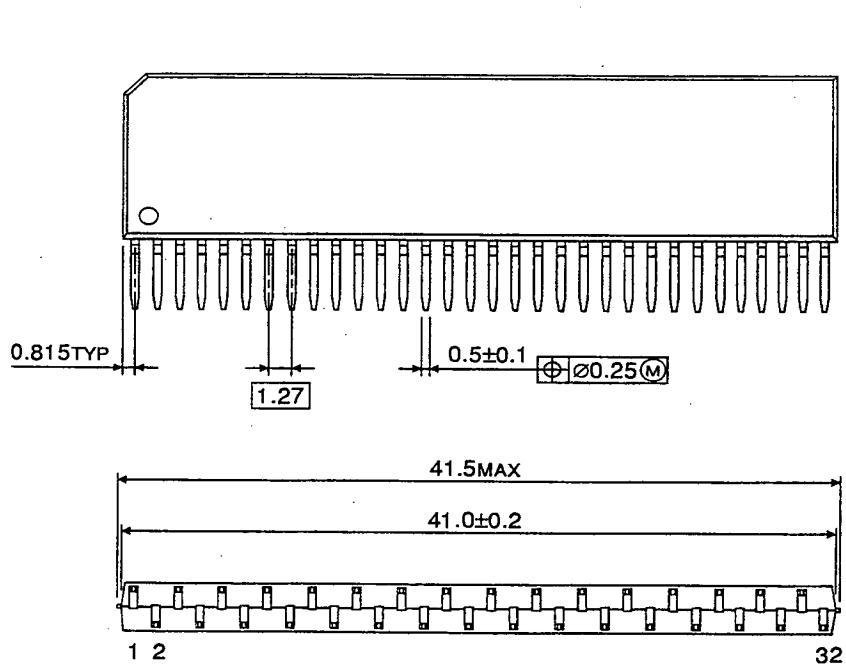
ZIP24-P-475

TENTATIVE



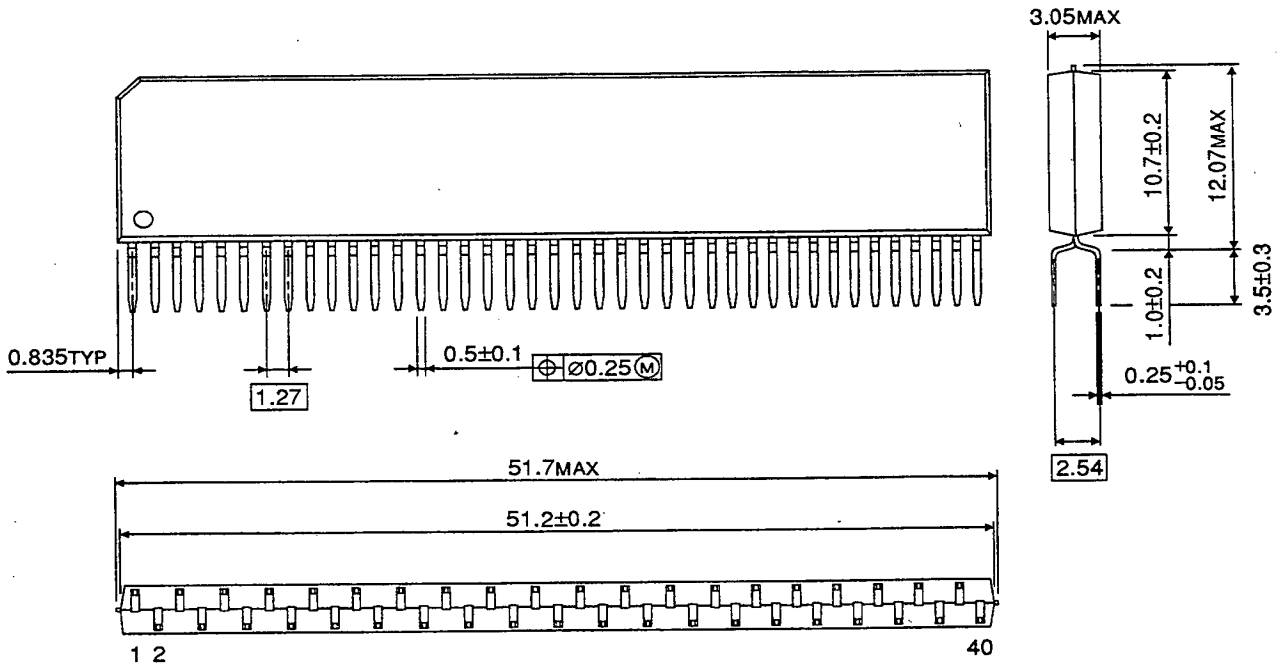
ZIP32-P-475

TENTATIVE



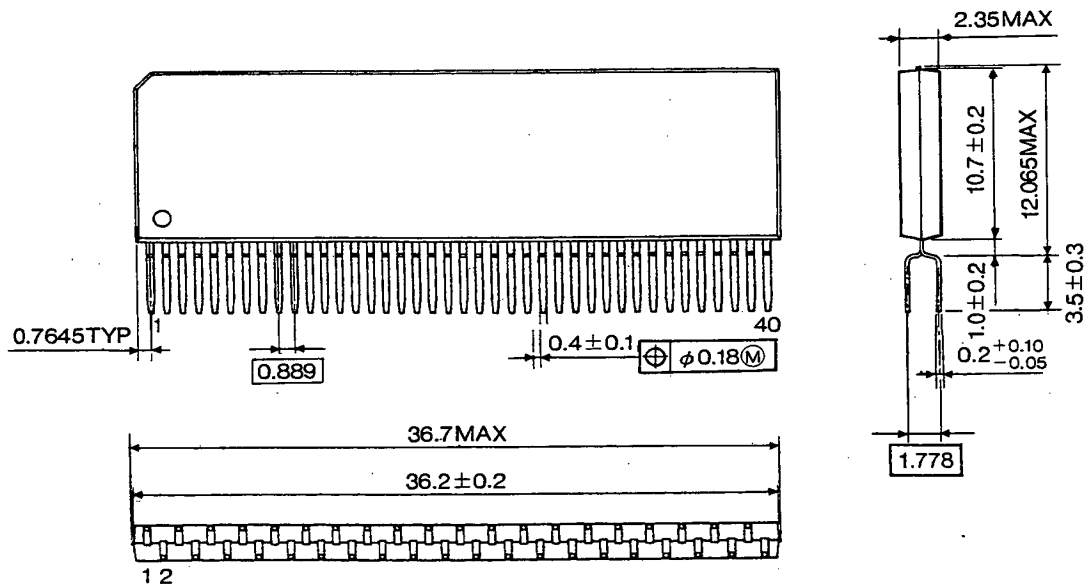
Unit in mm

ZIP40-P-475



SZIP40-P-475

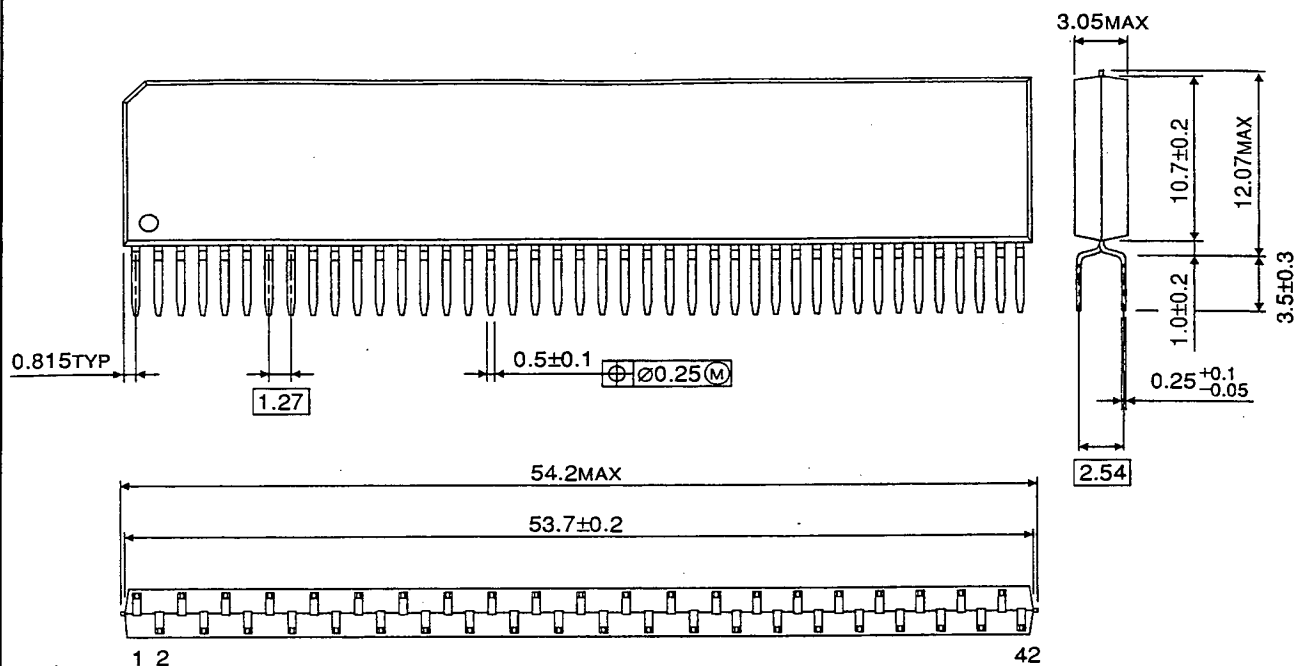
TENTATIVE



Unit in mm

ZIP42-P-475

TENTATIVE

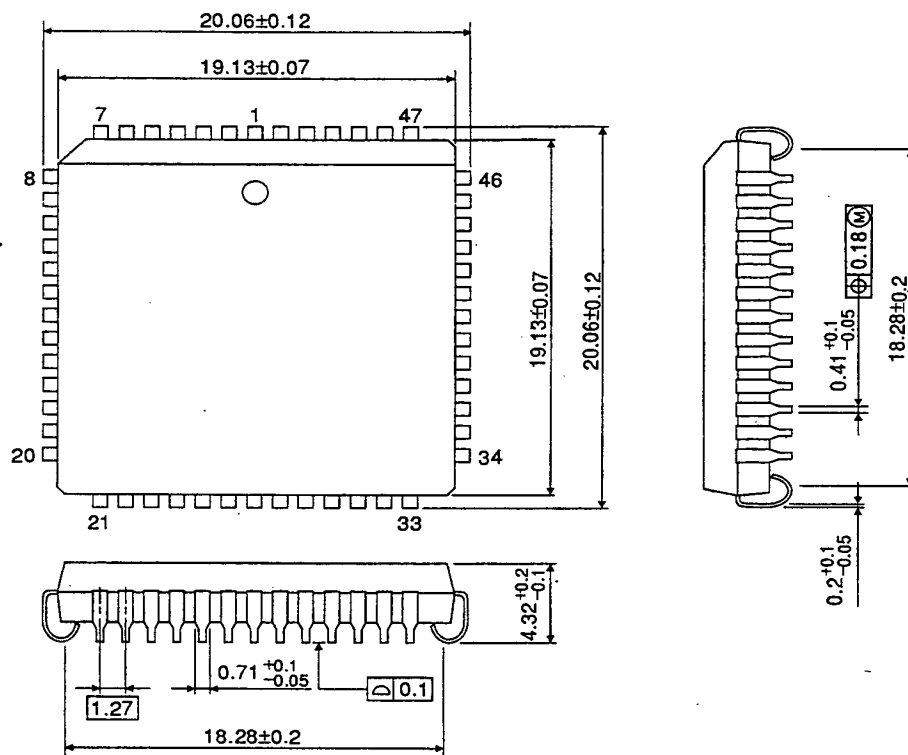


Quad Flat J-lead Package (QFJ)

Package Name	Device Group	Device Name
QFJ52-P-S750	High speed SRAM	TC55187T, TC55188T

Unit in mm

QFJ52-P-S750

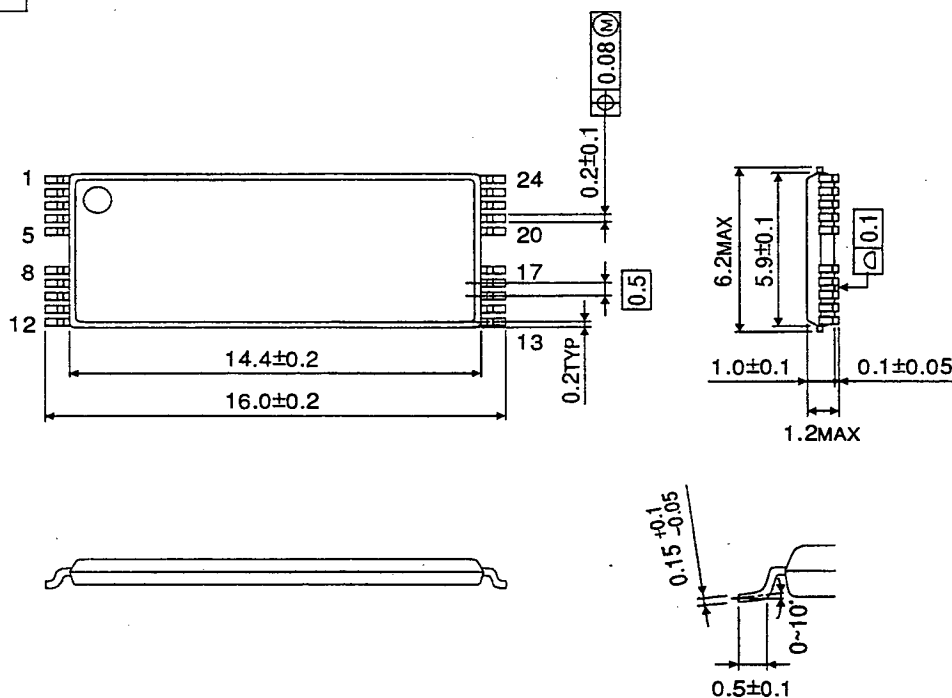


Thin Small Out-line L-lead Package (TSOP I)

Package Name	Device Group	Device Name
TSOP24-P-0616	Dynamic RAM	TC511000BFT, TC511001BFT, TC511002BFT, TC514256BFT, TC514258BFT, TC514266BFT
TSOP24-P-0616A	Dynamic RAM	TC511000BTR, TC511001BTR, TC511002BTR, TC514256BTR, TC514258BTR, TC514266BTR
TSOP28-P	Static RAM	TC55257BFT
TSOP28-P-A	Static RAM	TC55257BTR
TSOP32-P-0820	Static RAM	TC551001AFT
	Pseudo SRAM	TC518128AFT, TC518129AFT, TC518128BFT, TC518129BFT
TSOP32-P-0820A	Static RAM	TC551001ATR
	Pseudo SRAM	TC518128ATR, TC518129ATR, TC518128BTR, TC518129BTR

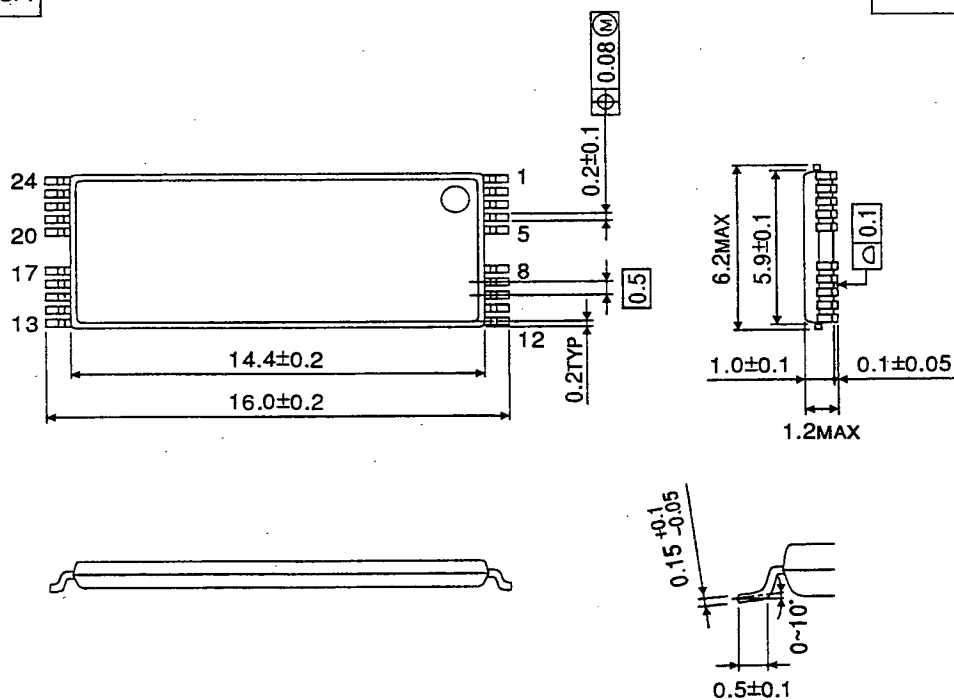
Unit in mm

TSOP24-P-0616



TSOP24-P-0616A

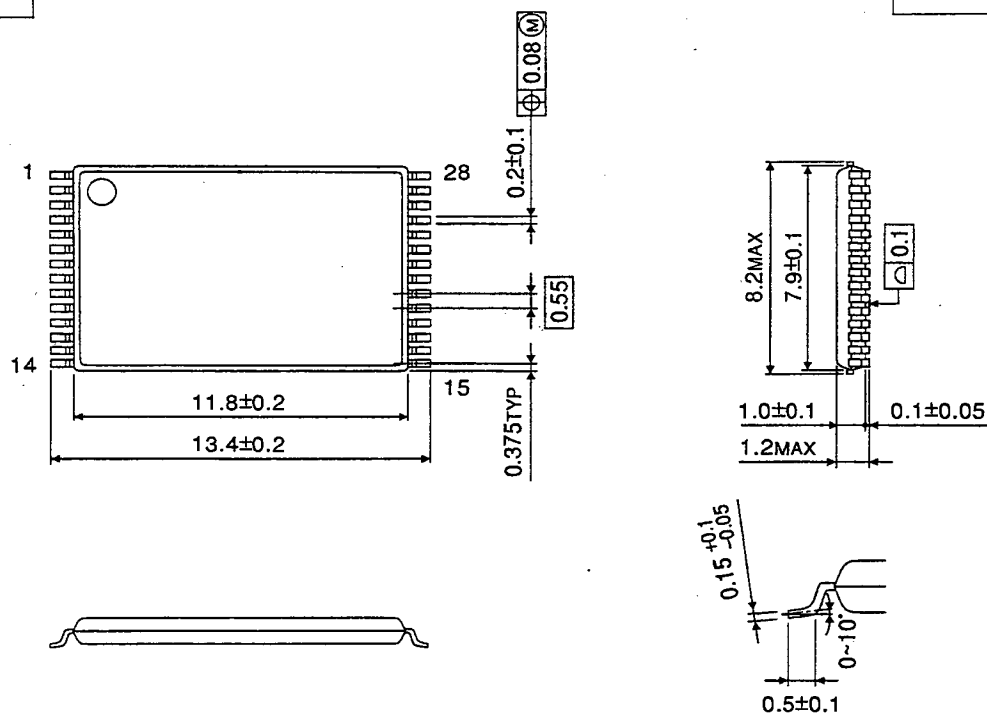
TENTATIVE



Unit in mm

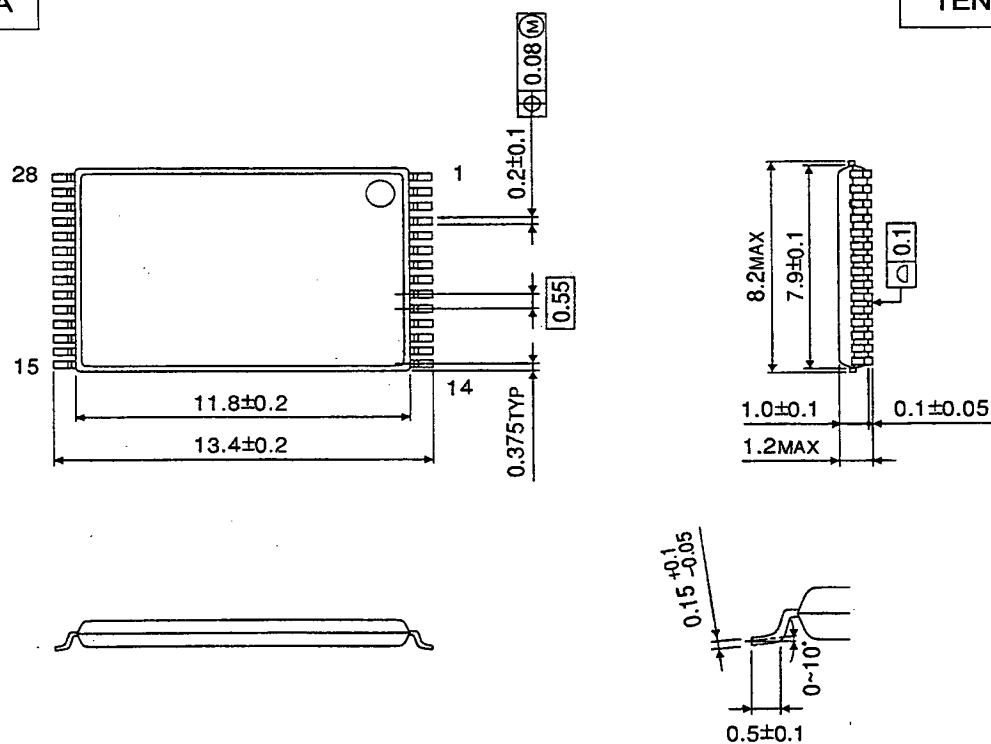
TSOP28-P

TENTATIVE



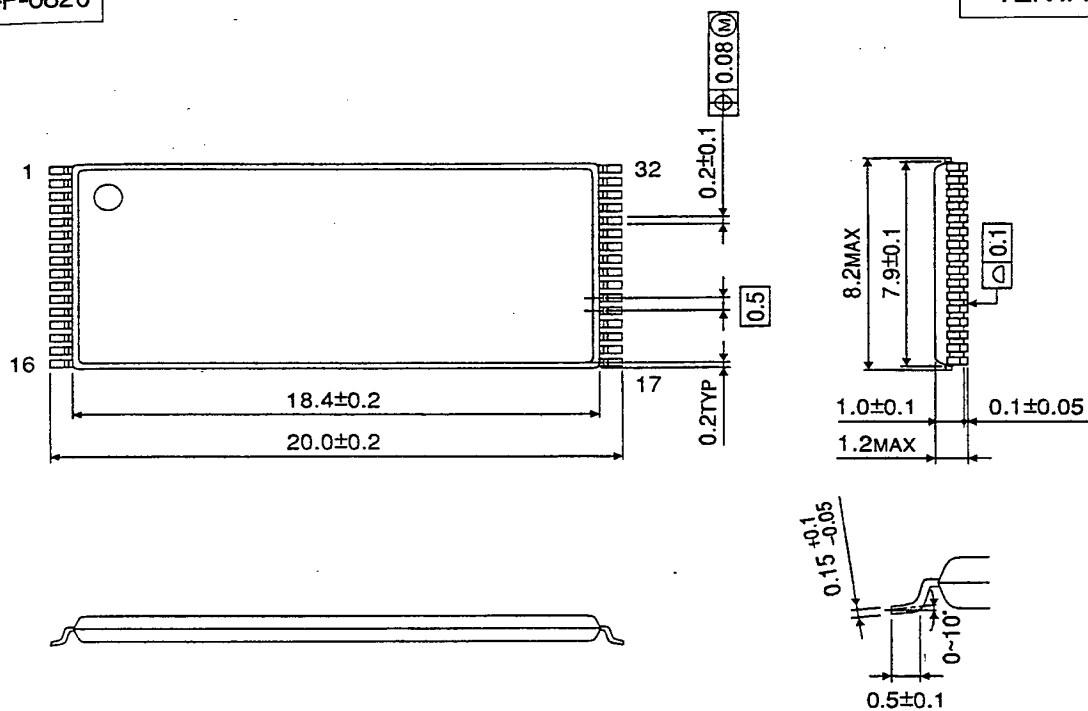
TSOP28-P-A

TENTATIVE



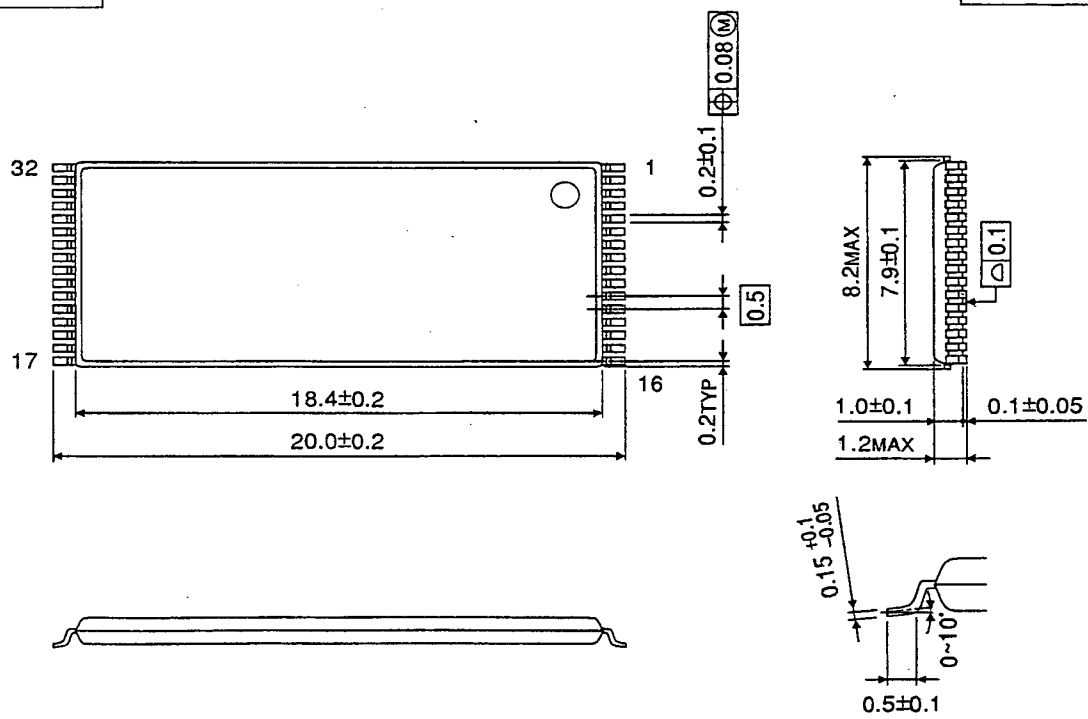
TSOP32-P-0820

TENTATIVE



TSOP32-P-0820A

TENTATIVE



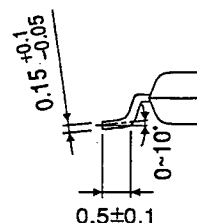
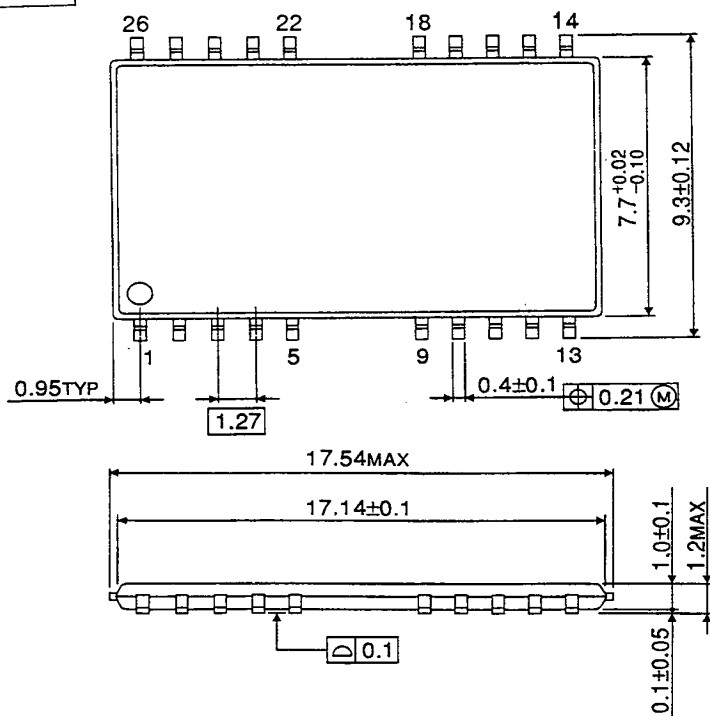
Thin Small Out-line L-lead Package (TSOP II)

Package Name	Device Group	Device Name
TSOP26-P-300	Dynamic RAM	TC514100AFT, TC514101AFT, TC514102AFT, TC514400AFT, TC514402AFT, TC514410AFT TC514100BFT, TC514101BFT, TC514102BFT, TC514400BFT, TC514402BFT, TC514410BFT
TSOP26-P-300A	Dynamic RAM	TC514100ATR, TC514101ATR, TC514102ATR, TC514400ATR, TC514402ATR, TC514410ATR TC514100BTR, TC514101BTR, TC514102BTR, TC514400BTR, TC514402BTR, TC514410BTR
TSOP28-P-400	Video RAM	TC524256BFT, TC524258BFT, TC524259BFT
	Dynamic RAM	TC514800AFT, TC514900AFT, TC5116800ANT, TC5117800ANT
TSOP28-P-400A	Video RAM	TC524256BTR, TC524258BTR, TC524259BTR
	Dynamic RAM	TC514800ATR, TC514900ATR, TC5116800ANR, TC5117800ANR
TSOP28-P-400B	Dynamic RAM	TC5116100FT, TC5116101FT, TC5116102FT, TC5116400FT, TC5116402FT TC5116410FT, TC5117400FT, TC5117402FT, TC5117410FT
TSOP28-P-400C	Dynamic RAM	TC5116100TR, TC5116101TR, TC5116102TR, TC5116400TR, TC5116402TR TC5116410TR, TC5117400TR, TC5117402TR, TC5117410TR
TSOP32-P-400	Static RAM	TC554002FT
	Pseudo SRAM	TC518512FT
	One Time PROM	TC544000FT
	Mask ROM	TC534000AFT
	Dynamic RAM	TC5116800AFT, TC5117800AFT, TC5116900AFT, TC5117900AFT
TSOP32-P-400A	Static RAM	TC554002TR
	Pseudo SRAM	TC518512TR
	Dynamic RAM	TC5116800ATR, TC5117800ATR, TC5116900ATR, TC5117900ATR,
TSOP44-P-400	Mask ROM	TC5316200AFT, TC5316210BFT
TSOP44-P-400B	Video RAM	TC528126BFT, TC528128BFT, TC528257FT, TC528267FT
	Dynamic RAM	TC511664BFT, TC511665BFT, TC514260BFT, TC514170BFT, TC514273BFT TC514280BFT, TC514190BFT
	Flash/NAND E ² PROM	TC584000FT
TSOP44-P-400C	Video RAM	TC528126BTR, TC528128BTR, TC528257TR, TC528267TR
	Dynamic RAM	TC511664BTR, TC511665BTR, TC514260BTR, TC514190BFT, TC514273BTR TC514280BTR, TC514190BTR
	Flash/NAND E ² PROM	TC584000TR
TSOP50-P-400	Dynamic RAM	TC5116160AFT, TC5116170AFT, TC5118160AFT, TC5118170AFT, TC5116180AFT TC5116190AFT, TC5118180AFT, TC5118190AFT
TSOP50-P-400A	Dynamic RAM	TC5116160ATR, TC5116170ATR, TC5118160ATR, TC5118170ATR, TC5116180ATR TC5116190ATR, TC5118180ATR, TC5118190ATR

Unit in mm

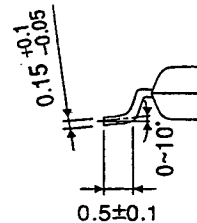
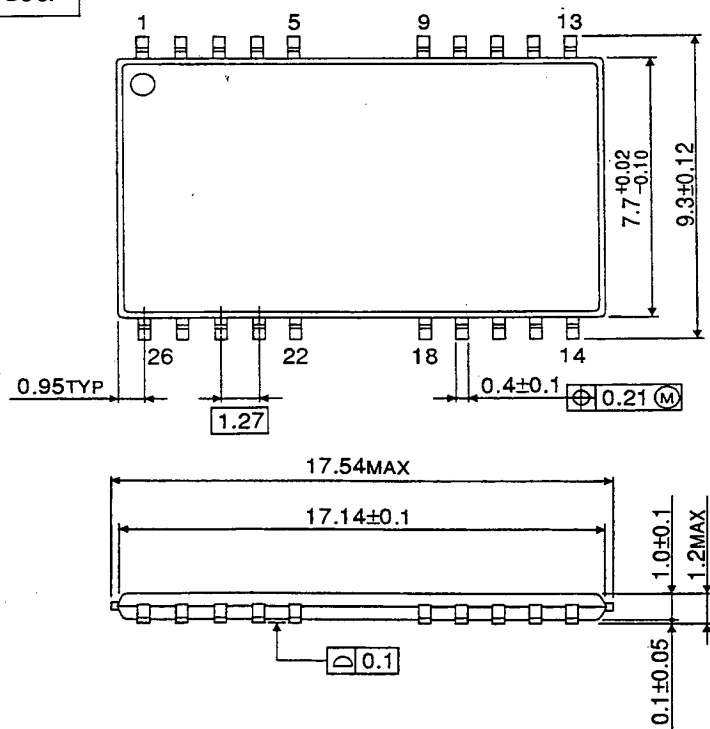
TSOP26-P-300

TENTATIVE



TSOP26-P-300A

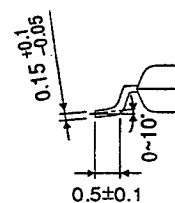
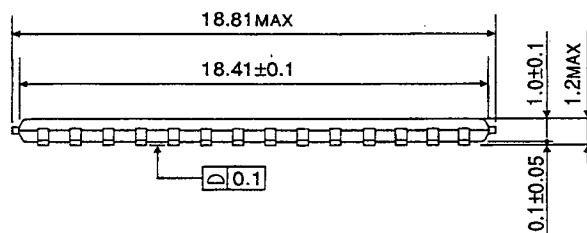
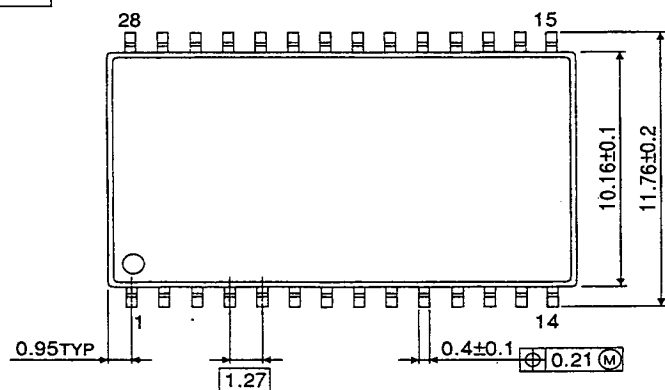
TENTATIVE



Unit in mm

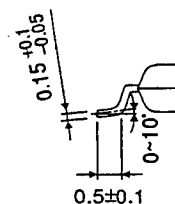
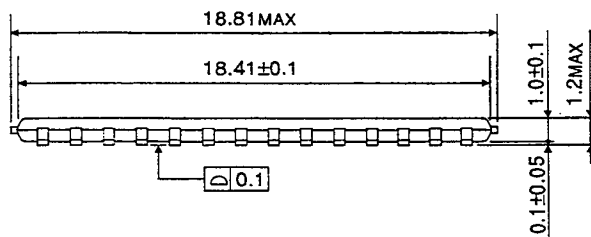
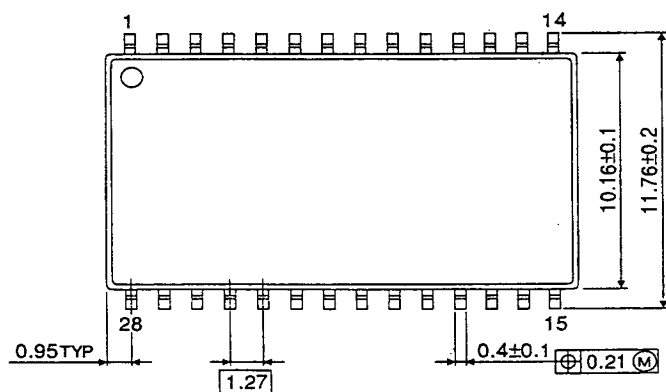
TSOP28-P-400

TENTATIVE



TSOP28-P-400A

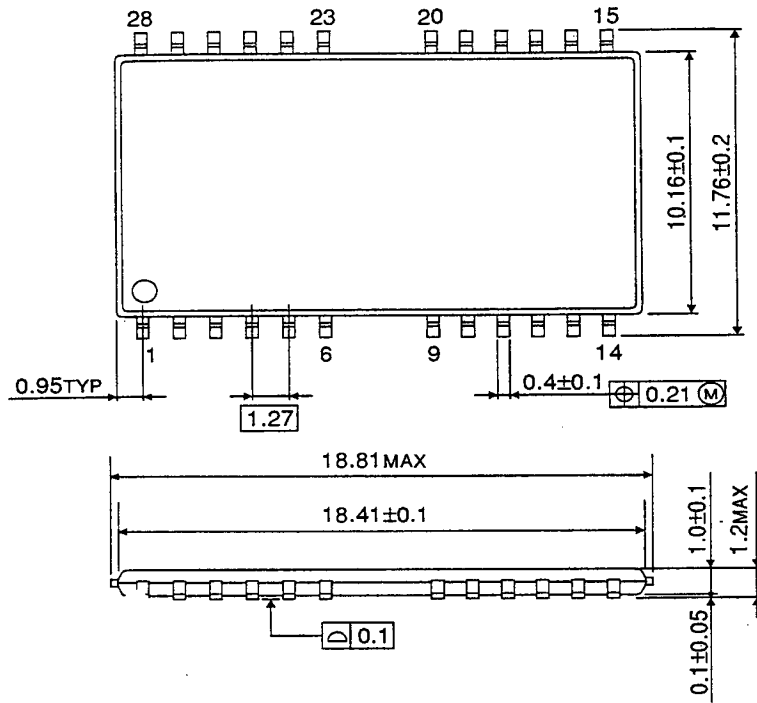
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Unit in mm

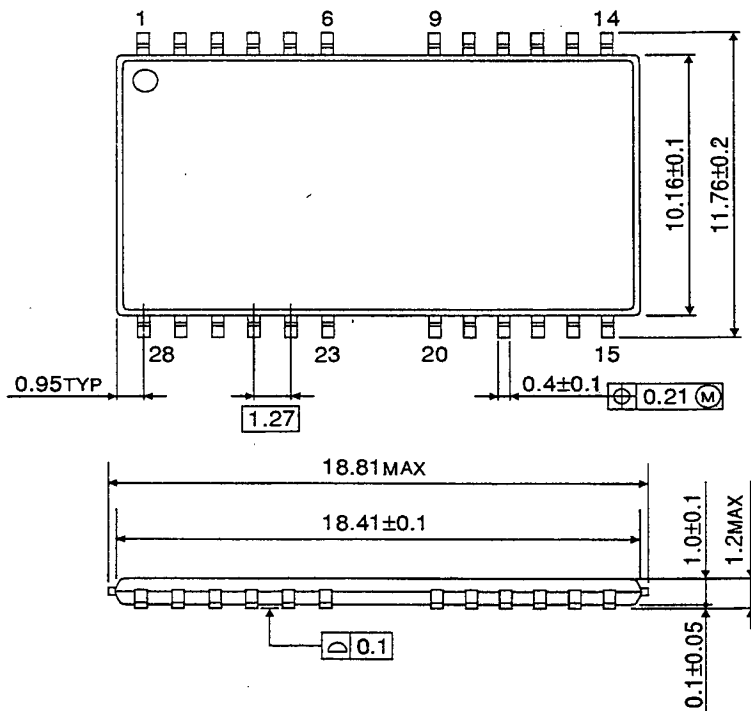
TSOP28-P-400B

TENTATIVE



TSOP28-P-400C

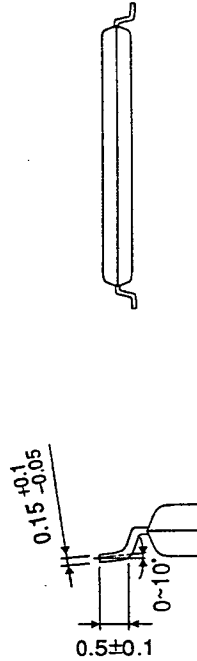
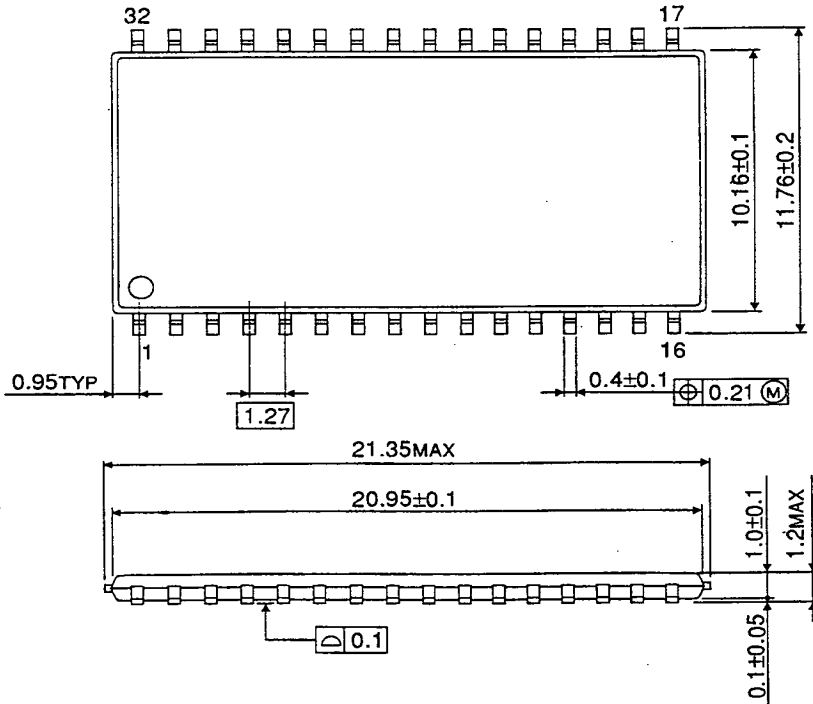
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Unit in mm

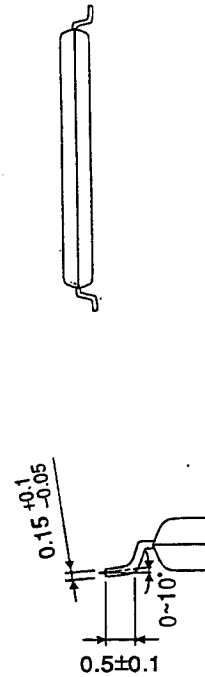
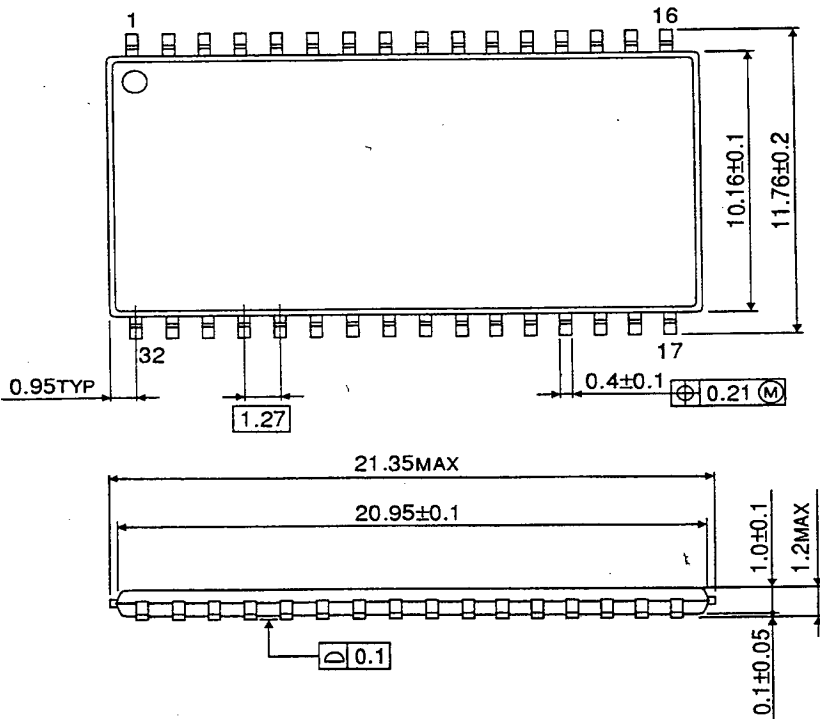
TSOP32-P-400

TENTATIVE



TSOP32-P-400A

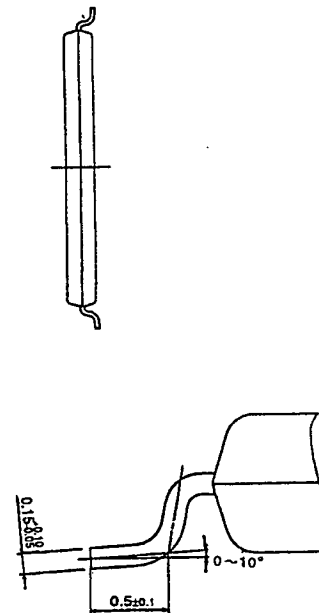
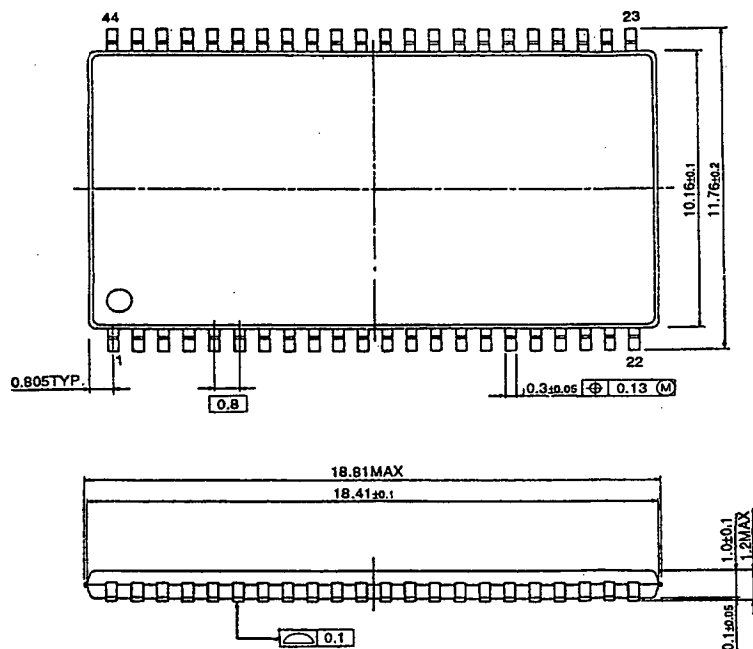
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Unit in mm

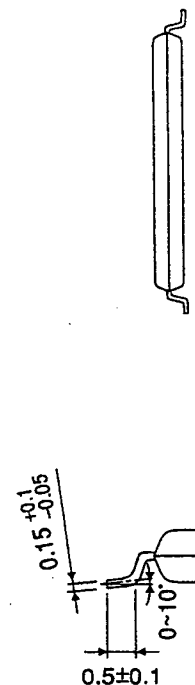
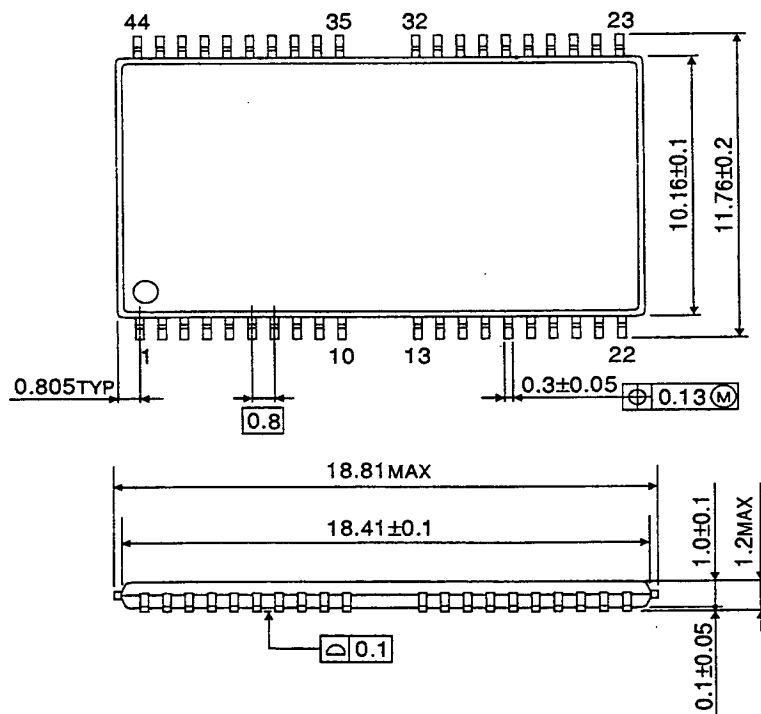
TSOP44-P-400

TENTATIVE



TSOP44-P-400B

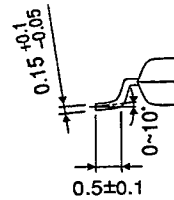
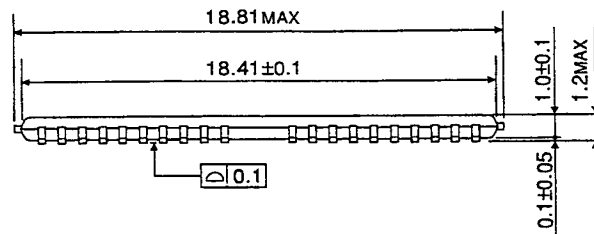
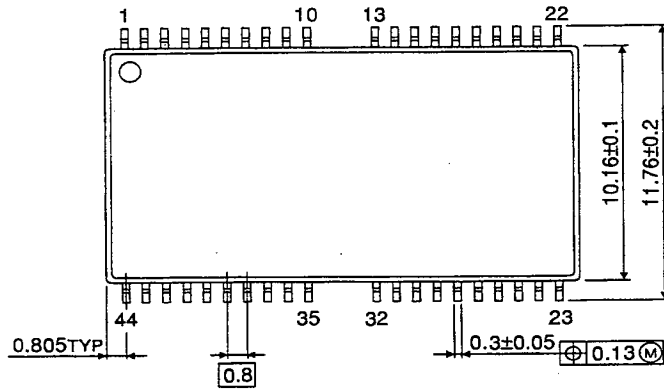
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Unit in mm

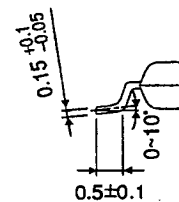
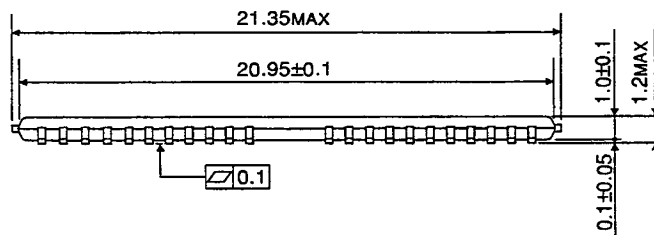
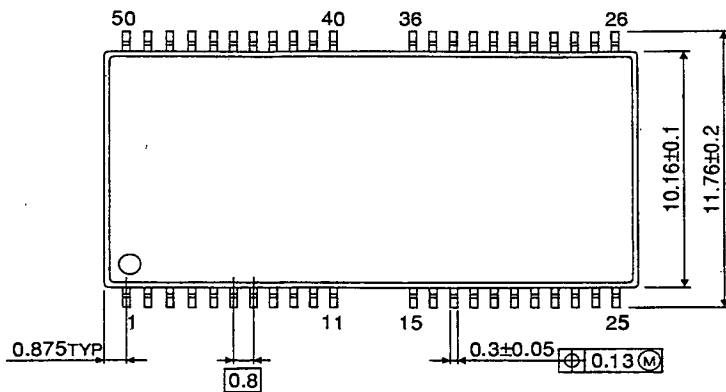
TSOP44-P-400C

TENTATIVE

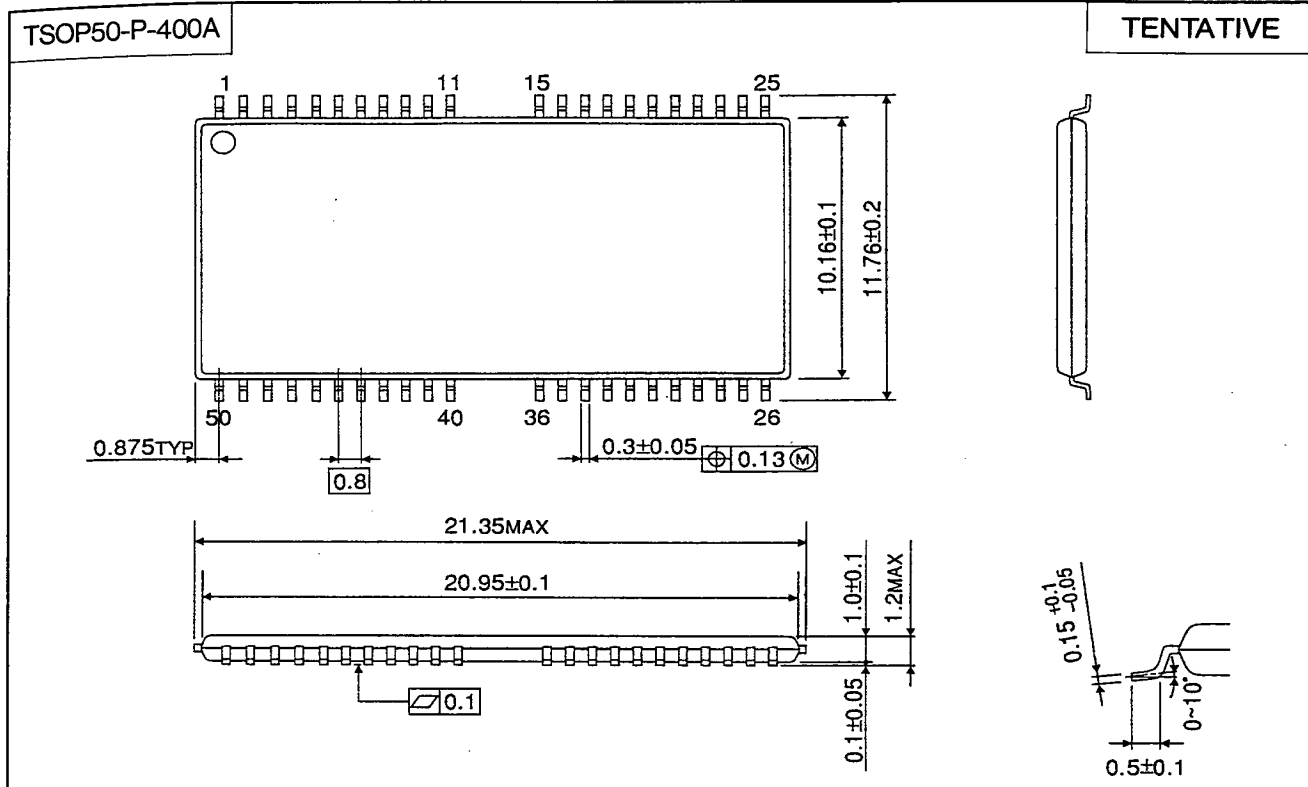


TSOP50-P-400

TENTATIVE



Unit in mm



4. DATA SHEETS

4-1 EPROM

SILICON STACKED GATE MOS INTEGRATED CIRCUIT

TC57256AD-12,-120,-150

32,768 WORD x 8 BIT CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The TC57256AD is a 32,768 word x 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory. For read operation, the TC57256AD's access time is 120ns, and the TC57256AD operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the CE input. Advanced CMOS technology reduces the maximum active current to 30mA/8.3MHz and standby current to 100µA. For program operation, the programming is achieved by using the high speed programming mode. For program operation, the programming is achieved by using high speed programming mode. TC57256AD is fabricated with the CMOS technology and the N-channel silicon double layer gate MOS technology.

FEATURES

- Peripheral circuit: CMOS
- Memory cell : N-MOS

	-12	-120	-150
VCC	5V±5%	5V±10%	
tACC	120ns	120ns	150ns

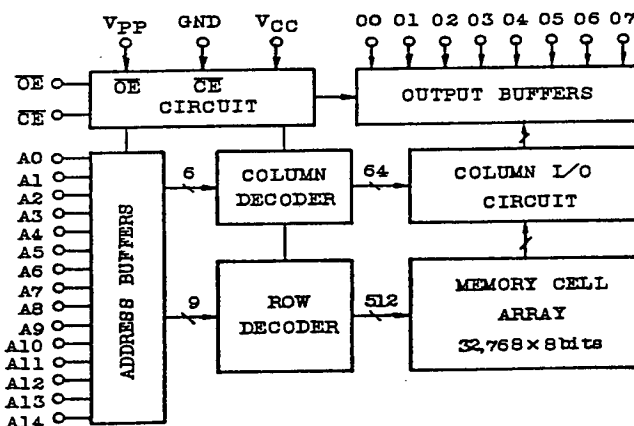
- Single 5V power supply

- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with ROM TC53257P; TMM23256P, TMM27256AD and TC57256D
- Standard 28 pin DIP cerdip package :WDIP28-G-600A

PIN CONNECTION (TOP VIEW)

VPP	1	28	VCC
A12	2	27	A14
A7	3	26	A13
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
A3	7	22	OE
A2	8	21	A10
A1	9	20	CE
A0	10	19	O7
O0	11	18	O6
O1	12	17	O5
O2	13	16	O4
GND	14	15	O3

BLOCK DIAGRAM



PIN NAMES

A0 ~ A14	Address Inputs
O0 ~ O7	Outputs (Inputs)
CE	Chip Enable Input
OE	Output Enable Input
Vpp	Program Supply Voltage
VCC	VCC Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE	PIN	CE (20)	OE (22)	VPP (1)	VCC (28)	O0 ~ O7 (11 ~ 13, 15 ~ 19)	POWER
Read		L	L	5V	5V	Data Out	Active
Output Deselect	*	H	H			High Impedance	
Standby		H	*			High Impedance	
Program		L	H	1) 12.5V 2) 12.75V	1) 6V 2) 6.25V	Data In	Active
Program Inhibit		H	H			High Impedance	
Program Verify	*	L	L			Data Out	

* H or L 1); HIGH SPEED PROGRAM MODE I,
2); HIGH SPEED PROGRAM MODE II

TC57256AD-12,-120,-150

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{CC}	V _{CC} Power Supply Voltage	-0.6 ~ 7.0	V
V _{PP}	Program Supply Voltage	-0.6 ~ 14.0	V
V _{IN}	Input Voltage	-0.6 ~ 7.0	V
V _{I/O}	Input/Output Voltage	-0.6 ~ V _{CC} +0.5	V
P _D	Power Dissipation	1.5	W
T _{SOLDER}	Soldering Temperature . Time	260 . 10	°C . sec
T _{STG}	Storage Temperature	-65 ~ 125	°C
T _{OPR}	Operating Temperature	0 ~ 70	°C

READ OPERATION

D.C. AND A.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC57256AD-12	TC57256AD-120/150
T _a	Operating Temperature	0 ~ 70°C	0 ~ 70°C
V _{CC}	V _{CC} Power Supply Voltage	5V±5%	5V±10%
V _{PP}	V _{PP} Power Supply Voltage	V _{CC} -0.6V ~ V _{CC} +0.6V	V _{CC} -0.6V ~ V _{CC} +0.6V

D.C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Current	V _{IN} =0 ~ V _{CC}	-	-	±10	μA
I _{LO}	Output Leakage Current	V _{OUT} =0.4 ~ V _{CC}	-	-	±10	μA
I _{CCO1}	Operating Current	$\overline{CE}$ =0V f=8.3MHz	-	-	30	mA
I _{CCO2}		I _{OUT} =0mA f=1MHz	-	-	15	
I _{CCS1}	Standby Current	$\overline{CE}$ =V _{IH}	-	-	1	mA
I _{CCS2}		$\overline{CE}$ =V _{CC} -0.2V	-	-	100	
V _{IH}	Input High Voltage	-	2.2	-	V _{CC} +0.3	V
V _{IL}	Output Low Voltage	-	-0.3	-	0.8	V
V _{OH}	Output High Voltage	I _{OH} =-400μA	2.4	-	-	V
V _{OL}	Output Low Voltage	I _{OL} =2.1mA	-	-	0.4	V
I _{PP1}	V _{PP} Current	V _{PP} =V _{CC} -0.6 ~ V _{CC} +0.6	-	-	±10	μA

TC57256AD-12,-120,-150

A.C. CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	TC57256AD-120/12		TC57256AD-150		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE}=\overline{OE}=V_{IL}$	-	120	-	150	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}=V_{IL}$	-	120	-	150	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IL}$	-	60	-	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}=V_{IL}$	0	50	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IL}$	0	50	0	60	ns
t_{OH}	Output Data Hold Time	$\overline{CE}=\overline{OE}=V_{IL}$	0	-	0	-	ns

A.C. TEST CONDITIONS

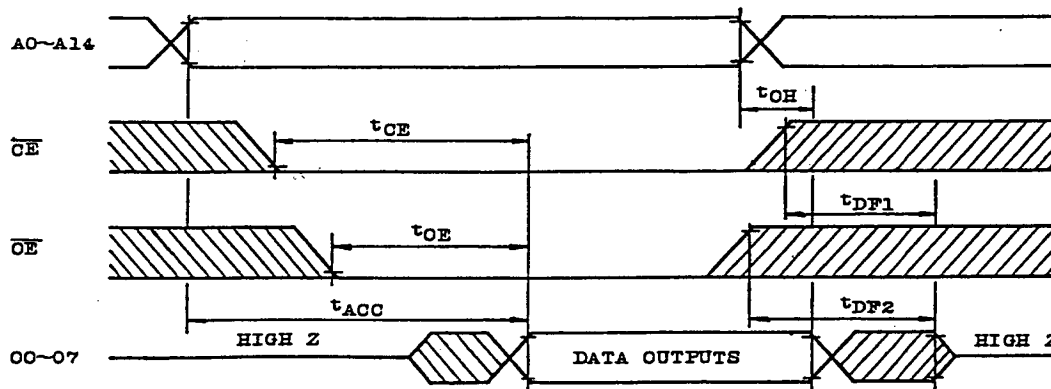
- Output Load : 1 TTL Gate and $C_L=100pF$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ~ 2.4V
- Timing Measurement Reference Level: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE *(Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN}=0V$	-	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT}=0V$	-	8	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS



TC57256AD-12,-120,-150

HIGH SPEED PROGRAM MODE I

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D.C. and OPERATING CHARACTERISTICS ($T_a=25\pm5^\circ\text{C}$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0 \sim V_{CC}$	-	-	± 10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu\text{A}$	2.4	-	-	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1\text{mA}$	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	30	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	-	-	50	mA
V_{ID}	A9 Auto Select Voltage	-	11.5	12.0	12.5	V

A.C. PROGRAMMING CHARACTERISTICS ($T_a=25\pm5^\circ\text{C}$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\overline{CE}$ Setup Time	-	0	-	-	ns
t_{CEH}	$\overline{CE}$ Hold Time	-	0	-	-	ns
t_{OES}	$\overline{OE}$ Setup Time	-	2	-	-	μs
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VPS}	V_{PP} Setup Time	-	2	-	-	μs
t_{VCS}	V_{CC} Setup Time	-	2	-	-	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{IH}$	0.95	1	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IH}$	-	-	100	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IH}$	-	-	90	ns

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and $C_L(100\text{pF})$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V $\sim$ 2.4V
- Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

HIGH SPEED PROGRAM OPERATION II

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{IH}	Input High Voltage	2.2	-	V _{CC} +1.0	V
V _{IL}	Input Low Voltage	-0.3	-	0.8	V
V _{CC}	V _{CC} Power Supply Voltage	6.00	6.25	6.50	V
V _{PP}	V _{PP} Power Supply Voltage	12.50	12.75	13.00	V

D.C. AND OPERATING CHARACTERISTICS (T_a=25±5°C, V_{CC}=6.25±0.25V, V_{PP}=12.75±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Current	V _{IN} =0 ~ V _{CC}	-	-	±10	μA
V _{OH}	Output High Voltage	I _{OH} =-400μA	2.4	-	-	V
V _{OL}	Output Low Voltage	I _{OL} =2.1mA	-	-	0.4	V
I _{CC}	V _{CC} Supply Current	-	-	-	30	mA
I _{PP2}	V _{PP} Supply Current	V _{PP} =13.0V	-	-	50	mA
V _{ID}	A9 Auto Select Voltage	-	11.5	12.0	12.5	V

A.C. PROGRAMMING CHARACTERISTICS (T_a=25±5°C, V_{CC}=6.25±0.25V, V_{PP}=12.75±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t _{AS}	Address Setup Time	-	2	-	-	μs
t _{AH}	Address Hold Time	-	2	-	-	μs
t _{CES}	$\overline{\text{CE}}$ Setup Time	-	0	-	-	ns
t _{CEH}	$\overline{\text{CE}}$ Hold Time	-	0	-	-	ns
t _{DS}	Data Setup Time	-	2	-	-	μs
t _{DH}	Data Hold Time	-	2	-	-	μs
t _{VPS}	V _{PP} Setup Time	-	2	-	-	μs
t _{VCS}	V _{CC} Setup Time	-	2	-	-	μs
t _{PW}	Program Pulse Width	$\overline{\text{CE}}=\text{V}_{\text{IL}}, \overline{\text{OE}}=\text{V}_{\text{IH}}$	0.095	0.1	0.105	ms
t _{OE}	$\overline{\text{OE}}$ to Output Valid	$\overline{\text{CE}}=\text{V}_{\text{IH}}$	-	-	100	ns
t _{DFP}	$\overline{\text{OE}}$ to Output in High-Z	$\overline{\text{CE}}=\text{V}_{\text{IH}}$	-	-	90	ns

A.C. TEST CONDITIONS

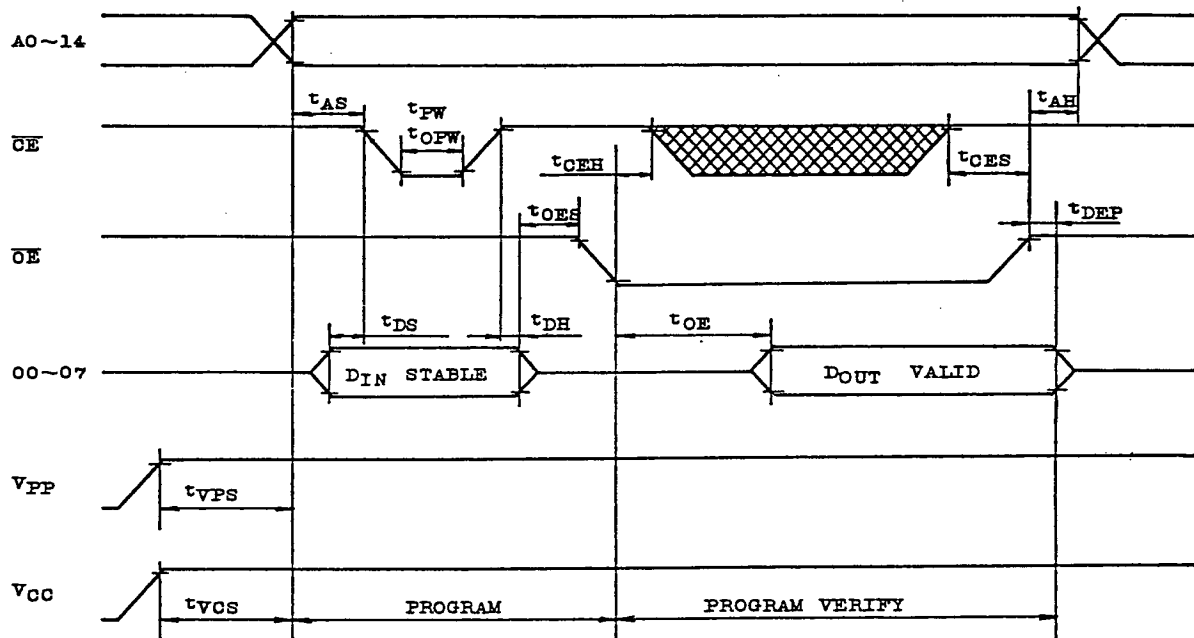
- Output Load : 1 TTL Gate and C_L(100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

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TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAM MODE I ($V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

HIGH SPEED PROGRAM MODE II ($V_{CC}=6.25V\pm0.25V$, $V_{PP}=12.75V\pm0.25V$)



Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP} .

2. Removing the device from socket and setting the device in socket with $V_{PP}=12.5V$ (12.75V) may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC57256AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. Then intergrated does (ultraviolet light intensity [w/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [w·sec/cm²].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [μw/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated does is 12000 [μw/cm²] × (20 × 60) [sec] ≈ 15 [w·sec/cm²].)

The TC57256AD's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the flourescent lamps will include 3000~4000Å wave-length components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TC57256AD's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

PIN NAMES (NUMBER)		CE (20)	OE (22)	VPP (1)	VCC (28)	00 ~ 07 (11 ~ 13, 15 ~ 19)	POWER
Read Operation (Ta=0 ~ 70°C)	Read	L	L	5V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	
	Standby	H	*			High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	H	1) 12.5V	1) 6V	Data In	Active
	Program Inhibit	H	H	2) 12.75V	2) 6.25V	High Impedance	
	Program Verify	*	L			Data Out	

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}. 1); HIGH SPEED PROGRAM MODE I
2); HIGH SPEED PROGRAM MODE II

READ MODE

The TC57256AD has two control functions. The chip enable (CE) controls the operation power and should be used for device selection.

The output enable (OE) control the output buffers, independent of device selection. Assuming that CE=OE=V_{IL}, the output data is valid at the outputs after address access time from stabilizing of all addresses.

The CE to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that CE=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of OE.

OUTPUT DESELECT MODE

Assuming that CE=V_{IH} or OE=V_{IH}, the outputs will be in a high impedance state.

So two or more TC57256AD's can be connected together on a common bus line.

When CE is decoded for device selection, all deselected devices are in low power standby mode.

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STANDBY MODE

The TC57256AD has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC57256AD is placed in the standby mode which reduce the operating current to 100 μ A by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC57256AD are in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming. The TC57256AD is in the programming mode when the V_{pp} input is at 12.5V and $\overline{CE}$ is at TTL-Low under $\overline{OE}=V_{IH}$. The TC57256AD can be programmed any location at any time either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with $\overline{OE}$ at V_{IL} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V or +12.75V) is applied to V_{pp} terminal, a high level $\overline{CE}$ input inhibits the TC57256AD from being programmed. Programming of two or more TC57256AD's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM MODE I

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{pp} terminal with $V_{CC}=6V$. The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times). After correctly programming the selected address, the additional program pulse with width of 3 times more than that needed for initial programming is applied. When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{pp}=5V$.

HIGH SPEED PROGRAM MODE II

The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the V_{PP} terminal with $V_{CC}=6.25V$.

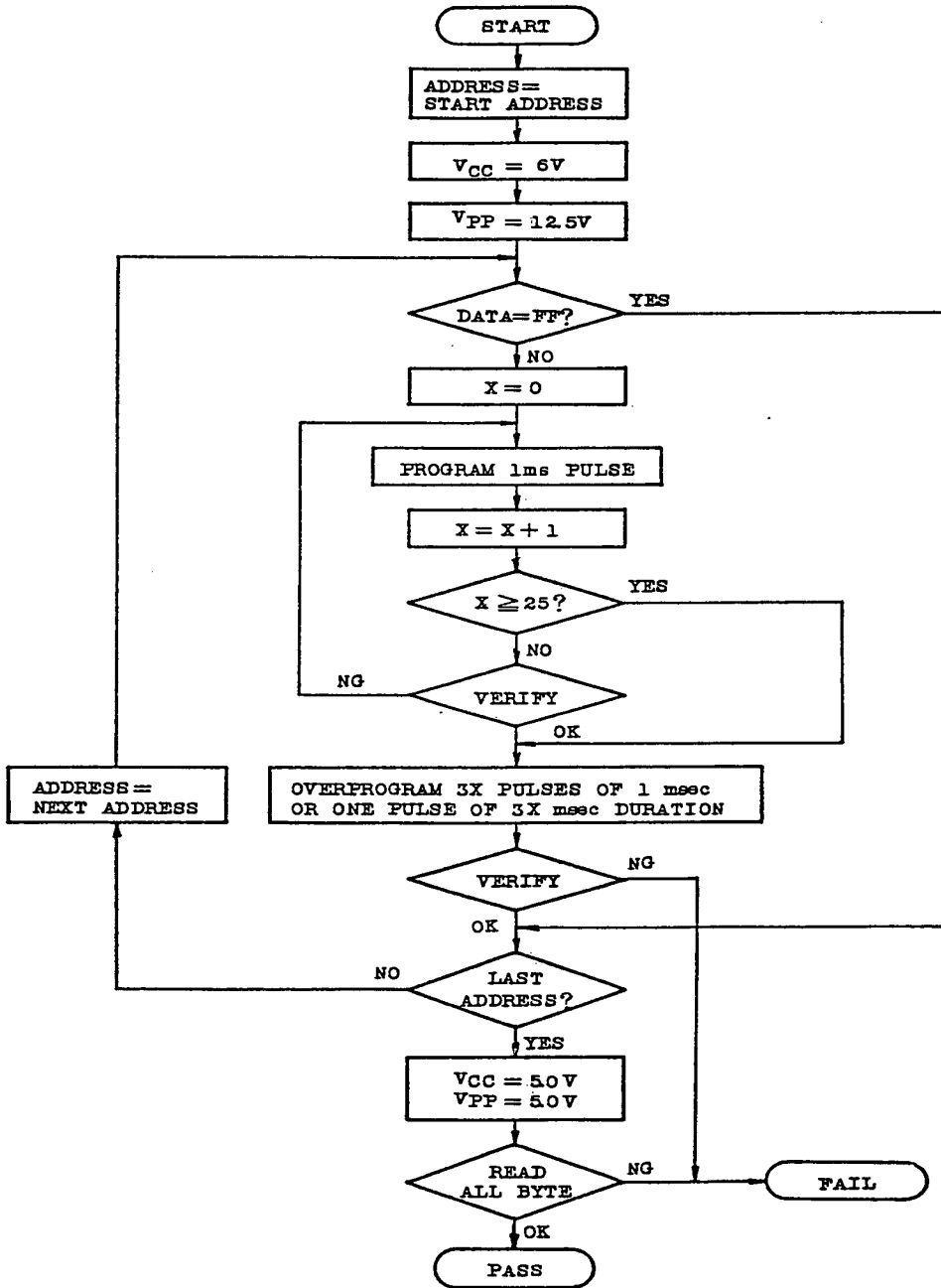
The programming is achieved by applying a single TTL low level 0.1ms pulse the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

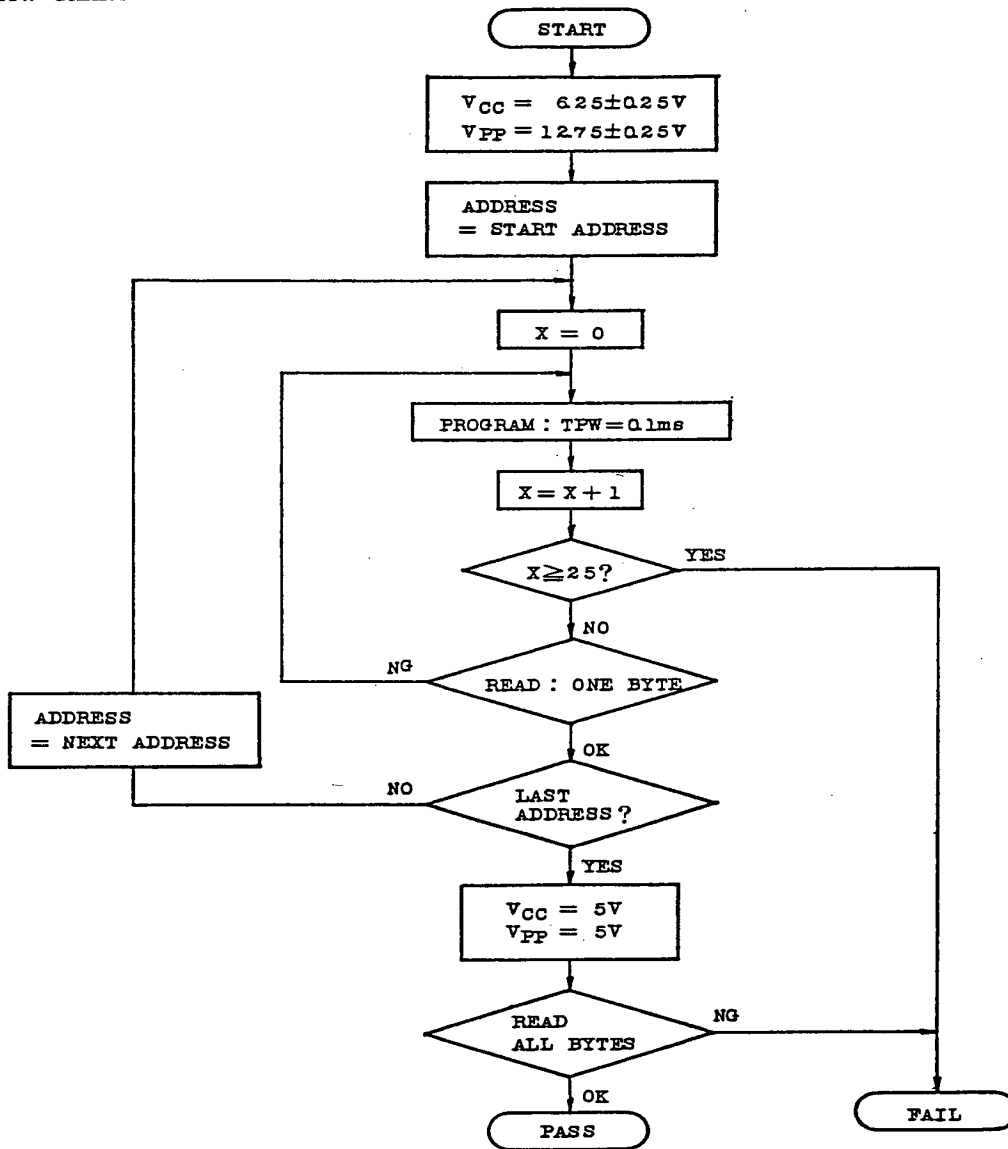
HIGH SPEED PROGRAM MODE I

FLOW CHART



HIGH SPEED PROGRAM MODE II

FLOW CHART



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ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC57256AD which identifies its manufacturer and device type.

The programming equipment may reads out manufacturer code and device code from TC57256AD by using this mode before program operation and automatically set program voltage (Vpp) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to VIL in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to VIH. These two codes possess an odd parity with the parity bit of MSB (07).

The following table shows electric signature of TC57256AD.

SIGNATURE PINS	A0 (10)	07 (19)	06 (18)	05 (17)	04 (16)	03 (15)	02 (13)	01 (12)	00 (11)	HEX. DATA
Manufacture Code	VIL	1	0	0	1	1	0	0	0	98
Device Code	VIH	1	1	0	0	0	1	0	0	C4

Notes: A9=12V±0.5V
A1 ~A8, A10 ~A14, CE, OE=VIL

SILICON STACKED GATE MOS INTEGRATED CIRCUIT

TC57256AD-15, -20

32,768 WORD x 8 BIT CMOS UV ERASABLE AND ELECTRICALLY
PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

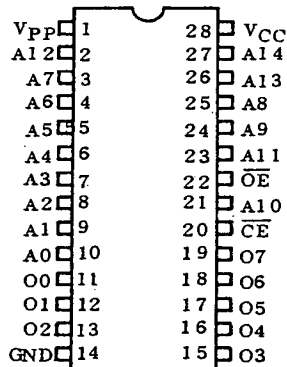
The TC57256AD is a 32,768 word x 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory. For read operation, the TC57256AD's access time is 150ns, and the TC57256AD operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input. Advanced CMOS technology reduces the maximum active current to 30mA/6.7MHz and standby current to 100 μ A. For program operation, the programming is achieved by using the high speed programming mode. TC57256AD is fabricated with the CMOS technology and the N-channel silicon double layer gate MOS technology.

FEATURES

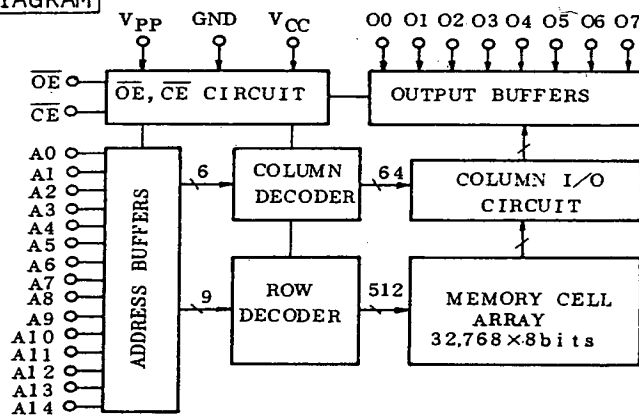
- Peripheral circuit: CMOS
- Memory cell : N-MOS
- Low power dissipation
 - Active : 30mA/6.7MHz
 - Standby: 100 μ A
- Fast access time: TC57256AD-15 150ns
TC57256AD-20 200ns
- Single 5V power supply
- Fully static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with ROM TC53257P, TMM23256P, TMM27256AD and TC57256D
- Standard 28 pin DIP cerdip package

:WDIP28-G-600A

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

AO ~ A14	Address Inputs
O0 ~ O7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
OE	Output Enable Input
Vpp	Program Supply Voltage
VCC	Power Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE	PIN	$\overline{CE}$ (20)	OE (22)	VPP (1)	VCC (28)	O0 ~ O7 (11 ~ 13, 15 ~ 19)	POWER
Read		L	L	5V	5V	Data Out	Active
Output Deselect		*	H			High Impedance	
Standby		H	*			High Impedance	
Program		L	H			Data In	Active
Program Inhibit		H	H	12.5V	6V	High Impedance	
Program Verify		*	L			Data Out	

* H or L

TC57256AD-15, -20

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	$-0.6 \sim 7.0$	V
V_{PP}	Program Supply Voltage	$-0.6 \sim 14.0$	V
V_{IN}	Input Voltage	$-0.6 \sim 7.0$	V
$V_{I/O}$	Input/Output Voltage	$-0.6 \sim V_{CC}+0.5$	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature . Time	260 . 10	$^{\circ}\text{C} \cdot \text{sec}$
T_{STRG}	Storage Temperature	$-65 \sim 125$	$^{\circ}\text{C}$
T_{OPR}	Operating Temperature	$-40 \sim 85$	$^{\circ}\text{C}$

READ OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	$V_{CC}+0.3$	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	
V_{PP}	V_{PP} Power Supply Voltage	$V_{CC}-0.6$	V_{CC}	$V_{CC}+0.6$	

DC and OPERATING CHARACTERISTICS (Ta=-40~85°C, VCC=5V±5%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0V \sim V_{CC}$	-	-	±10	μA
I_{CC01}	Operating Current	$\overline{CE}=0V$ f=6.7MHz	-	-	30	mA
I_{CC02}		$I_{OUT}=0mA$ f=1MHz	-	-	10	
I_{CCS1}	Standby Current	$\overline{CE}=V_{IH}$	-	-	1	mA
I_{CCS2}		$\overline{CE}=V_{CC}-0.2V$	-	-	100	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	-	-	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	-	-	0.4	V
I_{PP1}	V_{CC} Current	$V_{PP}=V_{CC} \pm 0.6V$	-	-	±10	μA
I_{LO}	Output Leakage Current	$V_{OUT}=0.4V \sim V_{CC}$	-	-	±10	μA

AC CHARACTERISTICS (Ta=-40~85°C, V_{CC}=5V±5%, V_{PP}=V_{CC}±0.6V)

SYMBOL	PARAMETER	TEST CONDITION	TC57256AD-15		TC57256AD-20		UNIT
			MIN.	MAX.	MIN.	MAX.	
t _{ACC}	Address Access Time	$\overline{CE}=\overline{OE}=V_{IL}$	-	150	-	200	ns
t _{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}=V_{IL}$	-	150	-	200	
t _{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IL}$	-	70	-	70	
t _{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}=V_{IL}$	0	60	0	60	
t _{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IL}$	0	60	0	60	
t _{OH}	Output Data Hold Time	$\overline{CE}=\overline{OE}=V_{IL}$	0	-	0	-	

AC TEST CONDITIONS

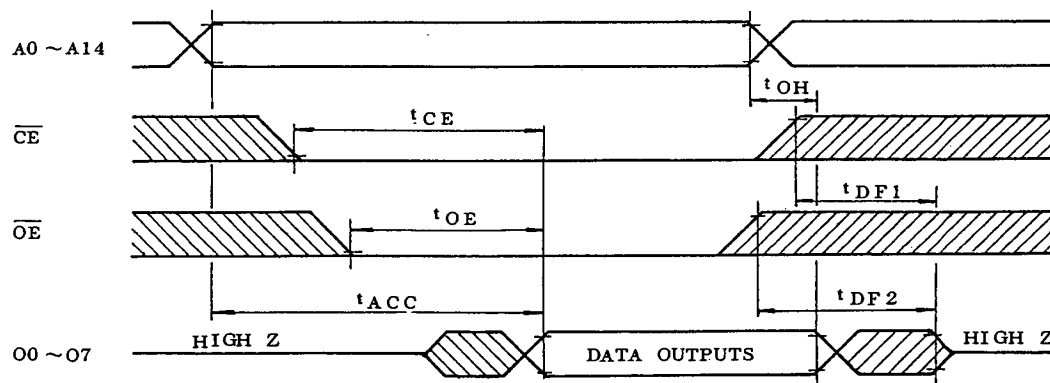
- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V~2.4V
- Timing Measurement Reference Level: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE *(Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} =0V	-	4	6	pF
C _{OUT}	Output Capacitance	V _{OUT} =0V	-	8	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



TC57256AD-15, -20

PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{IH}	Input High Voltage	2.2	-	V _{CC} +1.0	V
V _{IL}	Input Low Voltage	-0.3	-	0.8	
V _{CC}	V _{CC} Power Supply Voltage	5.75	6.0	6.25	
V _{PP}	V _{PP} Power Supply Voltage	12.0	12.5	13.0	

DC and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Current	V _{IN} =0 ~ V _{CC}	-	-	±10	μA
V _{OH}	Output High Voltage	I _{OH} =-400μA	2.4	-	-	V
V _{OL}	Output Low Voltage	I _{OL} =2.1mA	-	-	0.4	V
I _{CC}	V _{CC} Supply Current	-	-	-	30	mA
I _{PP2}	V _{PP} Supply Current	V _{PP} =13.0V	-	-	50	mA
V _{ID}	A9 Auto Select Voltage	-	11.5	12.0	12.5	V

AC PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t _{AS}	Address Setup Time	-	2	-	-	μs
t _{AH}	Address Hold Time	-	2	-	-	μs
t _{CES}	$\overline{CE}$ Setup Time	-	0	-	-	ns
t _{CEH}	$\overline{CE}$ Hold Time	-	0	-	-	ns
t _{OES}	$\overline{OE}$ Setup Time	-	2	-	-	μs
t _{DS}	Data Setup Time	-	2	-	-	μs
t _{DH}	Data Hold Time	-	2	-	-	μs
t _{VPS}	V _{PP} Setup Time	-	2	-	-	μs
t _{VCS}	V _{CC} Setup Time	-	2	-	-	μs
t _{PW}	Initial Program Pulse Width	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{IH}$	0.95	1	1.05	ms
t _{OPW}	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t _{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IH}$	-	-	150	ns
t _{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IH}$	-	-	130	ns

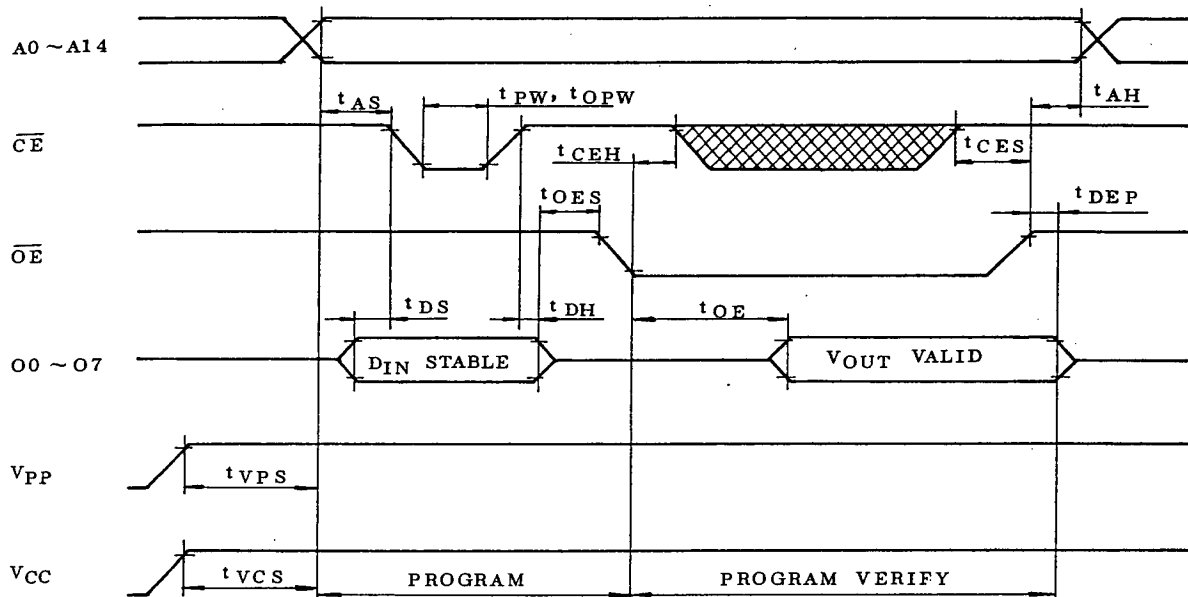
AC TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ~ 2.4V
- Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

($V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)



- Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP} .
2. Removing the device from socket and setting the device in socket with $V_{PP}=12.5V$ may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

TC57256AD-15, -20

ERASURE CHARACTERISTICS

The TC57256AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. Then intergrated does (ultraviolet light intensity [w/cm^2] $\times$ exposure time [sec.]) for erasure should be a minimum of 15 [$\text{w} \cdot \text{sec}/\text{cm}^2$].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is a 12000 [$\mu\text{w}/\text{cm}^2$] will reduce the exposure time to about 20 minutes. (In this case, the integrated does is 12000 [$\mu\text{w}/\text{cm}^2$] $\times$ (20 $\times$ 60) [sec] $\approx$ 15 [$\text{w} \cdot \text{sec}/\text{cm}^2$].)

The TC57256AD's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the flourescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available.

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The TC57256AD's six operation modes are listed in the following table.
Mode selection can be achieved by applying TTL level signal to all inputs.

PIN NAMES (NUMBER)		CE (20)	OE (22)	V _{PP} (1)	V _{CC} (28)	00~07 (11~13, 15~19)	POWER
MODE							
Read Operation (Ta=-40~85°C)	Read	L	L	5V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	
	Standby	H	*			High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	H	12.5V	6V	Data In	Active
	Program Inhibit	H	H			High Impedance	
	Program Verify	*	L			Data Out	

Note: H; V_{IH}, L; V_{IL}, *: V_{IH} or V_{IL}

READ MODE

The TC57256AD has two control functions. The chip enable ($\overline{\text{CE}}$) controls the operation power and should be used for device selection.

The output enable ($\overline{\text{OE}}$) control the output buffers, independent of device selection.

Assuming that $\overline{\text{CE}}=\overline{\text{OE}}=\text{V}_{\text{IL}}$, the output data is valid at the outputs after address access time from stabilizing of all addresses.

The $\overline{\text{CE}}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{\text{CE}}=\text{V}_{\text{IL}}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{\text{OE}}$.

OUTPUT DESELECT MODE

Assuming that $\overline{\text{CE}}=\text{V}_{\text{IH}}$ or $\overline{\text{OE}}=\text{V}_{\text{IH}}$, the outputs will be in a high impedance state.

So two or more TC57256AD's can be connected together on a common bus line.

When $\overline{\text{CE}}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC57256AD has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC57256AD is placed in the standby mode which reduce the operating current to 100 μ A by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC57256AD are in the "1" state which is erased state.

Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.

The TC57256AD is in the programming mode when the V_{pp} input is at 12.5V and $\overline{CE}$ is at TTL-Low under $\overline{OE}=V_{IH}$.

The TC57256AD can be programmed any location at any time either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ at V_{IL} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{pp} terminal, a high level $\overline{CE}$ input inhibits the TC57256AD from being programmed.

Programming of two or more TC57256AD's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{pp} terminal with $V_{CC}=6V$.

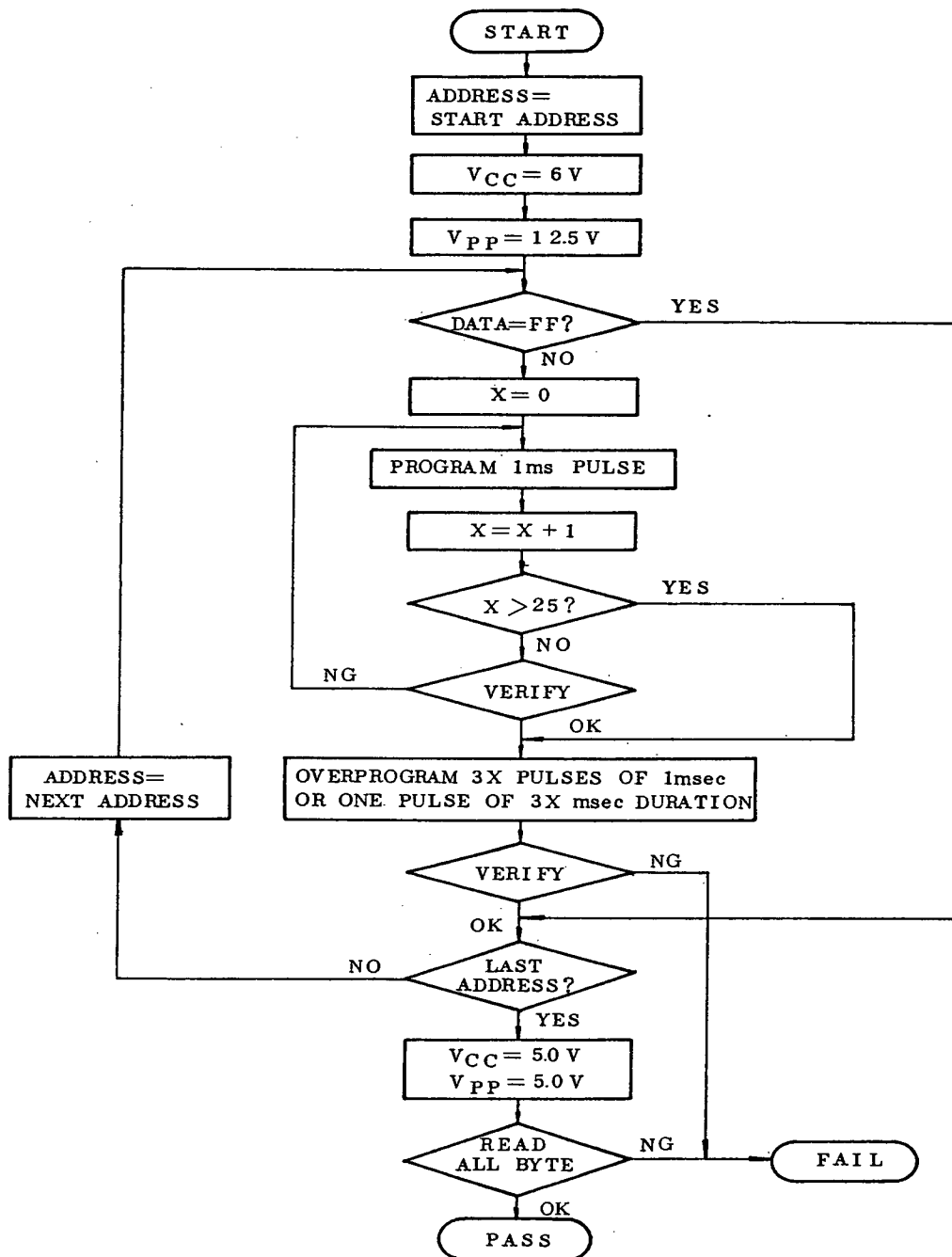
The programming is achieved by applying a single TTL low level lms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of lms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times)

After correctly programming the selected address, the additional program pulse with width of 3 times more than that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{pp}=5V$.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC57256AD which identifies its manufacturer and device type.

The programming equipment may reads out manufacturer code and device code from TC57256AD by using this mode before program operation and automatically set program voltage (V_{pp}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH} .

These two codes possess an odd parity with the parity bit of MSB (07).

The following table shows electric signature of TC57256AD.

SIGNATURE \ PINS	A0 (10)	07 (19)	06 (18)	05 (17)	04 (16)	03 (15)	02 (13)	01 (12)	00 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	1	0	0	0	1	0	0	C4

Notes: A9=12V $\pm$ 0.5V

A1 ~ A8, A10 ~ A14, $\overline{CE}$, $\overline{OE}$ = V_{IL}

SILICON STACKED GATE MOS INTEGRATED CIRCUIT

TC57H256D-70,-85

32,768 WORD x 8 BIT CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The TC57H256D is a 32,768 word x 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory. For read operation, the TC57H256D's access time is 70ns, and the TC57H256D operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the CE input. Advanced CMOS technology reduces the maximum active current to 50mA/14.2MHz and standby current to 100µA. For program operation, the programming is achieved by using the high speed programming mode. For program operation, the programming is achieved by using high speed programming mode. TC57H256D is fabricated with the CMOS technology and the N-channel silicon double layer gate MOS technology.

FEATURES

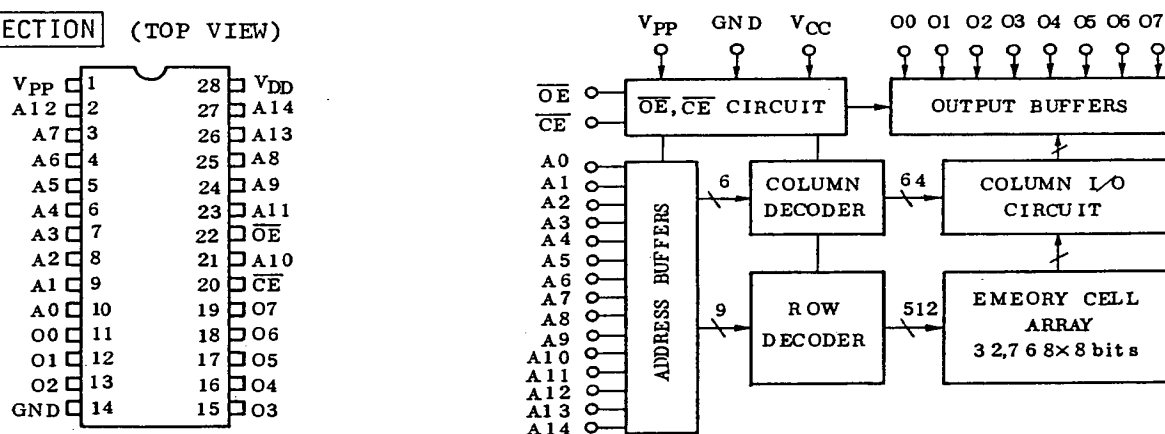
- Peripheral circuit: CMOS
- Memory cell : N-MOS

	-70	-85
V _{CC}	5V±5%	5V±10%
t _{ACC}	70ns	85ns

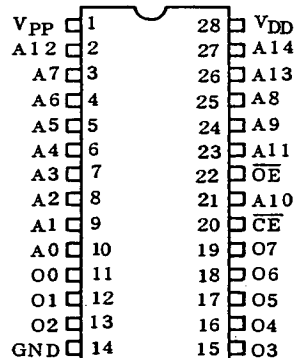
- Single 5V power supply

- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with ROM TC53257P, TMM23256P, TMM27256AD and TC57256AD
- Standard 28 pin DIP cerdip package :WDIP28-G-600A

BLOCK DIAGRAM



PIN CONNECTION (TOP VIEW)



PIN NAMES

A0 ~ A14	Address Inputs
00 ~ 07	Outputs (Inputs)
CE	Chip Enable Input
OE	Output Enable Input
Vpp	Program Supply Voltage
VCC	V _{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE	PIN	CE (20)	OE (22)	VPP (1)	VCC (28)	00 ~ 07 (11~13, 15~19)	POWER
Read		L	L	5V	5V	Data Out	Active
Output Deselect	*	H	*			High Impedance	
Standby	H	*				High Impedance	
Program	L	H		12.5V ¹⁾	6V ¹⁾	Data In	Active
Program Inhibit	H	H				High Impedance	
Program Verify	*	L		12.75V ²⁾	6.25V ²⁾	Data Out	

* H or L 1): HIGH SPEED PROGRAM MODE I
2): HIGH SPEED PROGRAM MODE II

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{CC}	V _{CC} Power Supply Voltage	-0.6 ~ 7.0	V
V _{PP}	Program Supply Voltage	-0.6 ~ 14.0	V
V _{IN}	Input Voltage	-0.6 ~ 7.0	V
V _{I/O}	Input/Output Voltage	-0.6 ~ V _{CC} +0.5	V
P _D	Power Dissipation	1.5	W
T _{SOLDER}	Soldering Temperature Time	260 ± 10	°C · sec
t _{STG}	Storage Temperature	-65 ~ 125	°C
t _{OPR}	Operating Temperature	0 ~ 70	°C

READ OPERATION

D.C. AND A.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC57H256D-70	TC57H256D-85
T _a	Operating Temperature	0 ~ 70°C	0 ~ 70°C
V _{CC}	V _{CC} Power Supply Voltage	5V±5%	5V±10%
V _{PP}	V _{PP} Power Supply Voltage	V _{CC} -0.6V ~ V _{CC} +0.6V	V _{CC} -0.6V ~ V _{CC} +0.6V

D.C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION		NIN.	TYP.	MAX.	UNIT
I _{LI}	Input Current	V _{IN} =0 ~ V _{CC}		-	-	±10	μA
I _{LO}	Output Leakage Current	V _{OUT} =0.4 ~ V _{CC}		-	-	±10	μA
I _{CC01}	Operating Current	$\overline{CE}$ =0V	f=14.2MHz	-	-	50	mA
I _{CC02}		I _{OUT} =0mA	f=1MHz	-	-	20	
I _{CCS1}	Standby Current	$\overline{CE}$ =V _{IH}		-	-	1	mA
I _{CCS2}		$\overline{CE}$ =V _{CC} -0.2V		-	-	100	
V _{IH}	Input High Voltage	-		2.2	-	V _{CC} +0.3	V
V _{IL}	Output Low Voltage	-		0.3	-	0.8	V
V _{OH}	Output High Voltage	I _{OH} =0400μA		2.4	-	-	V
V _{OL}	Output Low Voltage	I _{OL} =2.1mA		-	-	0.4	V
I _{PP1}	V _{PP} Current	V _{PP} =V _{CC} -0.6 ~ V _{CC} +0.6		-	-	±10	μA

TC57H256D-70, -85

A.C. CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	TC57H256D-70		TC57H256D-85		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE}=\overline{OE}=V_{IL}$	-	70	-	85	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}=V_{IL}$	-	70	-	85	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IL}$	-	40	-	45	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}=V_{IL}$	0	30	0	30	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IL}$	0	30	0	30	ns
t_{OH}	Output Data Hold Time	$\overline{CE}=\overline{OE}=V_{IL}$	5	-	5	-	ns

A.C. TEST CONDITIONS

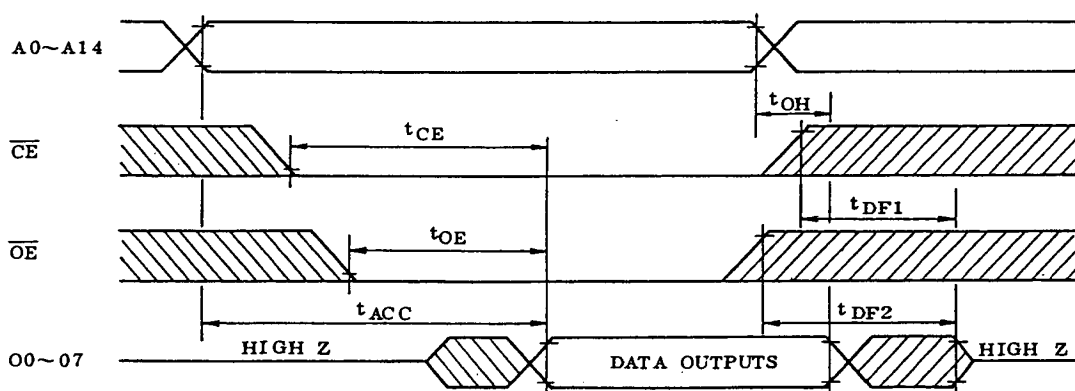
- Output Load : 1 TTL Gate and $C_L=100\text{pF}$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ~ 2.4V
- Timing Measurement Reference Level: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE *(Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN}=0V$	-	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT}=0V$	-	8	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS



HIGH SPEED PROGRAM MODE I

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D.C. and OPERATING CHARACTERISTICS ($T_a=25\pm5^\circ\text{C}$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0 \sim V_{CC}$	-	-	± 10	μA
V_{OH}	Output High Voltage	$I_{OH}=400\mu\text{A}$	2.4	-	-	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1\text{mA}$	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	40	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	-	-	50	mA

A.C. PROGRAMMING CHARACTERISTICS ($T_a=25\pm5^\circ\text{C}$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\overline{CE}$ Setup Time	-	0	-	-	μs
t_{CEH}	$\overline{CE}$ Hold Time	-	0	-	-	μs
t_{OES}	$\overline{OE}$ Setup Time	-	2	-	-	μs
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VPS}	V_{PP} Setup Time	-	2	-	-	μs
t_{VCS}	V_{CC} Setup Time	-	2	-	-	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{IH}$	0.95	1	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IH}$	-	-	100	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IH}$	-	-	90	ns

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and $C_L(100\text{pF})$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V $\sim$ 2.4V
- Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

TC57H256D-70, -85

HIGH SPEED PROGRAM OPERATION II

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{IH}	Input High Voltage	2.2	—	V _{CC} +1.0	V
V _{IL}	Input Low Voltage	-0.3	—	0.8	V
V _{CC}	V _{CC} Power Supply Voltage	6.00	6.25	6.50	V
V _{PP}	V _{PP} Power Supply Voltage	12.50	12.75	13.00	V

D.C. AND OPERATING CHARACTERISTICS (T_a=25±5°C, V_{CC}=6.25±0.25V, V_{PP}=12.75±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Current	V _{IN} =0 ~ V _{CC}	—	—	±10	μA
V _{OH}	Output High Voltage	I _{OH} =-400μA	2.4	—	—	V
V _{OL}	Output Low Voltage	I _{OL} =2.1mA	—	—	0.4	V
I _{CC}	V _{CC} Supply Current	—	—	—	40	mA
I _{PP2}	V _{PP} Supply Current	V _{PP} =13.0V	—	—	50	mA

A.C. PROGRAMMING CHARACTERISTICS (T_a=25±5°C, V_{CC}=6.25±0.25V, V_{PP}=12.75±0.25V)

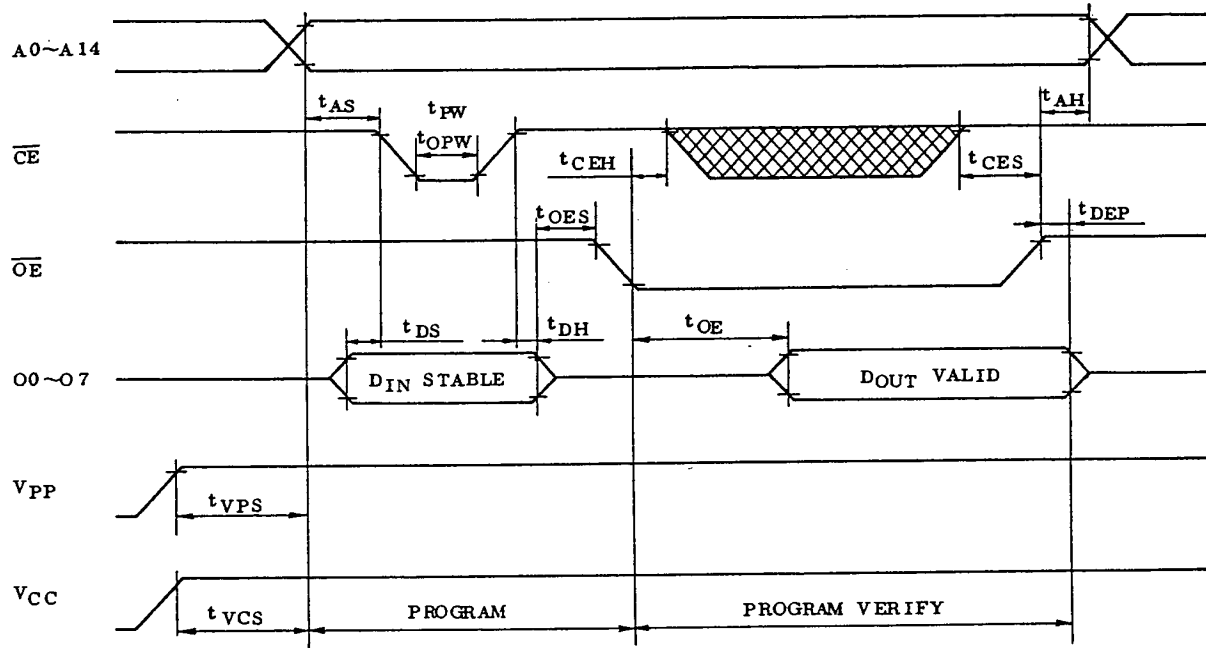
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t _{AS}	Address Setup Time	—	2	—	—	μs
t _{AH}	Address Hold Time	—	2	—	—	μs
t _{CES}	$\overline{CE}$ Setup Time	—	0	—	—	ns
t _{CEH}	$\overline{CE}$ Hold Time	—	0	—	—	ns
t _{DS}	Data Setup Time	—	2	—	—	μs
t _{DH}	Data Hold Time	—	2	—	—	μs
t _{VPS}	V _{PP} Setup Time	—	2	—	—	μs
t _{VCS}	V _{CC} Setup Time	—	2	—	—	μs
t _{PW}	Program Pulse Width	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{IH}$	0.095	0.1	0.105	ms
t _{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IH}$	—	—	100	ns
t _{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IH}$	—	—	90	ns

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L(100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAM MODE I ($V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)
 HIGH SPEED PROGRAM MODE II ($V_{CC}=6.25V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)



- Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP} .
2. Removing the device from socket and setting the device in socket with $V_{PP}=12.5V(12.75V)$ may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

TC57H256D-70, -85

ERASURE CHARACTERISTICS

The TC57H256D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. Then integrated does (ultraviolet light intensity [w/cm^2] $\times$ exposure time [sec.]) for erasure should be a minimum of 15 [$\text{w}\cdot\text{sec}/\text{cm}^2$].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [$\mu\text{w}/\text{cm}^2$] will reduce the exposure time to about 20 minutes. (In this case, the integrated does is 12000 [$\mu\text{w}/\text{cm}^2$] $\times$ (20 $\times$ 60) [sec] $\approx$ 15 [$\text{w}\cdot\text{sec}/\text{cm}^2$].)

The TC57H256D's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000 $\sim$ 4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TC57H256D's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE		PIN NAMES (NUMBER)	$\overline{\text{CE}}$ (20)	$\overline{\text{OE}}$ (22)	V_{PP} (1)	V_{CC} (28)	00 $\sim$ 07 (11 $\sim$ 13, 15 $\sim$ 19)	POWER
Read Operation ($T_a = 0 \sim 70^\circ\text{C}$)	Read		L	L	5V	5V	Data Out	Active
	Output Deselect		*	H			High Impedance	
	Standby		H	*			High Impedance	Standby
Program Operation ($T_a = 25 \pm 5^\circ\text{C}$)	Program		L	H	1) 12.5V	1) 6V	Data In	Active
	Program Inhibit		H	H	2) 12.75V	2) 6.25V	High Impedance	
	Program Verify		*	L			Data Out	

Note: H; V_{IH} ; L; V_{IL} ; *: V_{IH} or V_{IL} .

1): HIGH SPEED PROGRAM MODE I,
2): HIGH SPEED PROGRAM MODE II

READ MODE

The TC57H256D has two control functions. The chip enable ($\overline{\text{CE}}$) controls the operation power and should be used for device selection.

The output enable ($\overline{\text{OE}}$) control the output buffers, independent of device selection. Assuming that $\overline{\text{CE}} = \overline{\text{OE}} = V_{\text{IL}}$, the output data is valid at the outputs after address access time from stabilizing of all addresses.

The $\overline{\text{CE}}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{\text{CE}} = V_{\text{IL}}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{\text{OE}}$.

OUTPUT DESELECT MODE

Assuming that $\overline{\text{CE}} = V_{\text{IH}}$ or $\overline{\text{OE}} = V_{\text{IH}}$, the outputs will be in a high impedance state.

So two or more TC57H256D's can be connected together on a common bus line.

When $\overline{\text{CE}}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC57H256D has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC57H256D is placed in the standby mode which reduce the operating current to 100 μ A by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the OE inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC57H256D are in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming. The TC57H256D is in the programming mode when the V_{pp} input is at 12.5V and $\overline{CE}$ is at TTL-Low under $\overline{OE}=V_{IH}$. The TC57H256D can be programmed any location at any time either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with $\overline{OE}$ at V_{IL} .

PROGRAM INHIBIT MODE

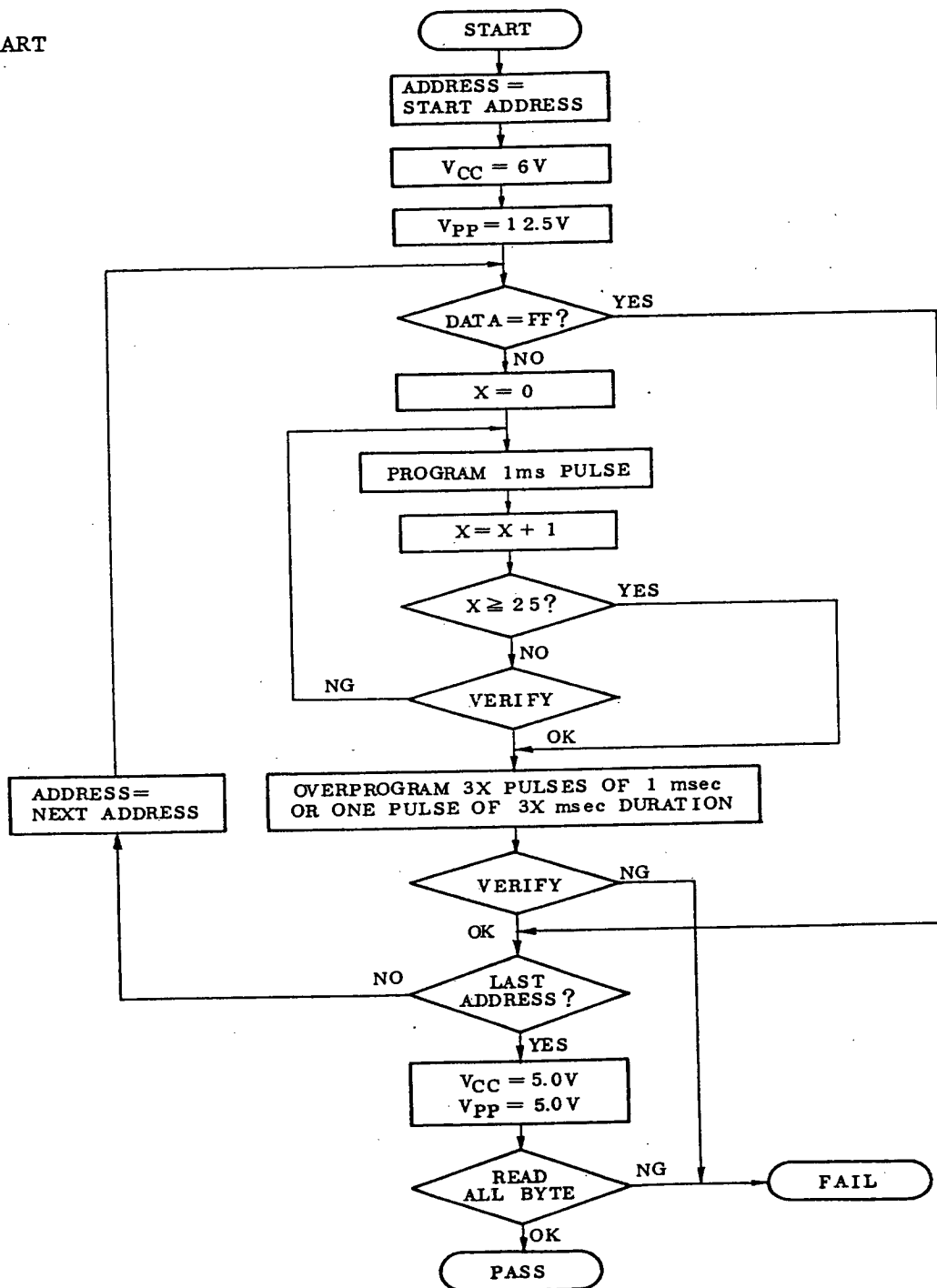
Under the condition that the program voltage (+12.5V or 12.75V) is applied to V_{pp} terminal, a high level $\overline{CE}$ input inhibits the TC57H256D from being programmed. Programming of two or more TC57H256D's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM MODE I

The program time can be greatly decreased by using this high speed programming mode. The device is set up is the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{pp} terminal with $V_{CC}=6V$. The programming is achieved by applying a single TTL low level lms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of lms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times). After correctly programming the selected address, the additional program pulse with width of 3 times more than that needed for initial programming is applied. When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{pp}=5V$.

HIGH SPEED PROGRAM MODE I

FLOW CHART



HIGH SPEED PROGRAM MODE II

The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the V_{pp} terminal with $V_{CC}=6.25V$.

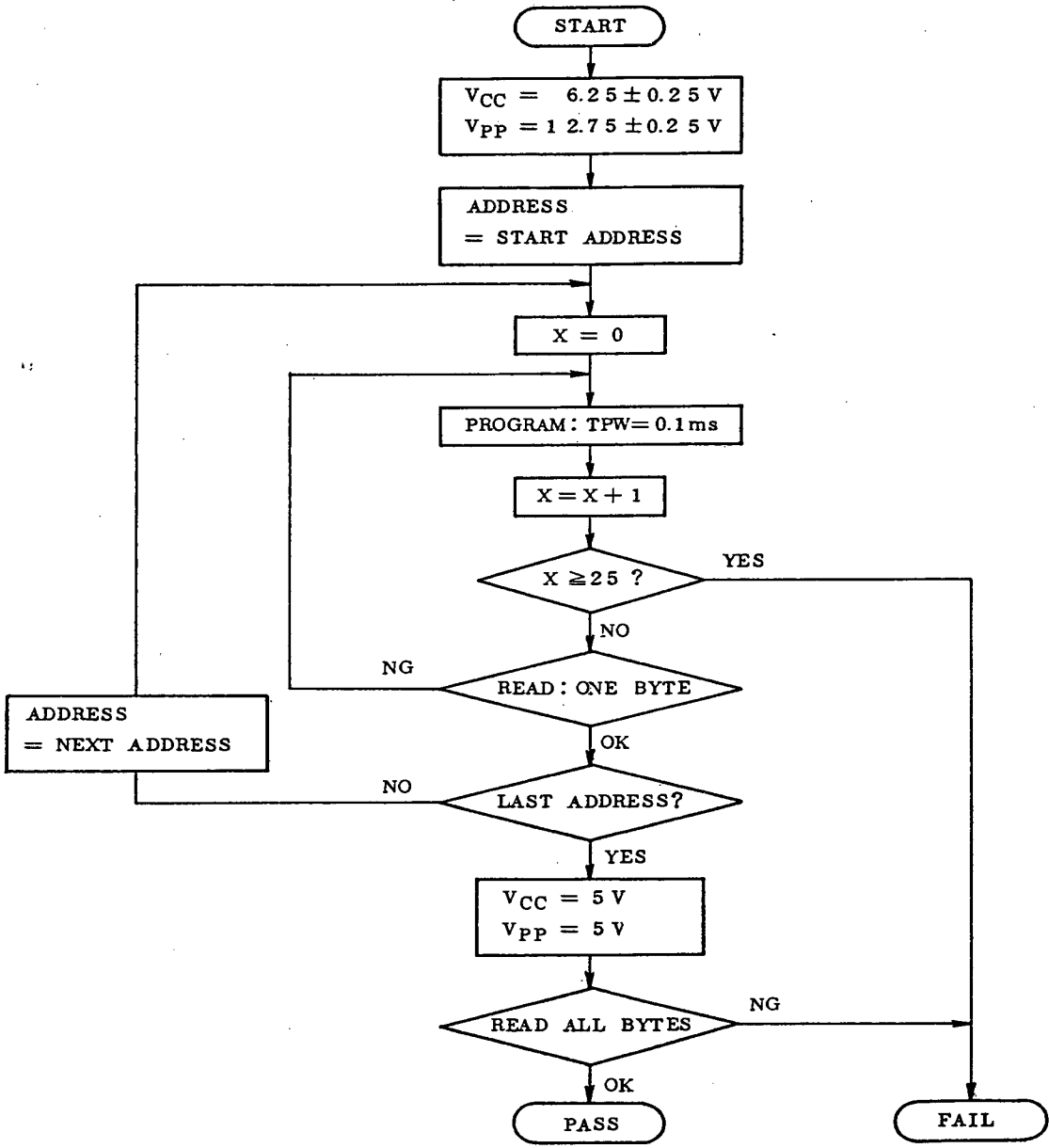
The programming is achieved by applying a single TTL low level 0.1ms pulse the CE input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{pp}=5V$.

HIGH SPEED PROGRAM MODE II

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC57H256D which identifies its manufacturer and device type.

The programming equipment may reads out manufacturer coce and device code from TC57H256D by using this mode before program operation and automatically set program voltage (V_{pp}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH} . These two codes possess an odd parity with the parity bit of MSB (07). The following table shows electric signature of TC57H256D.

SIGNATURE \ PINS	A0 (10)	07 (19)	06 (18)	05 (17)	04 (16)	03 (15)	02 (13)	01 (12)	00 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	0	1	0	0	0	1	0	1	45

Notes: A9=12V±0.5V

A1 ~ A8, A10 ~ A14, $\overline{CE}$, $\overline{OE}=V_{IL}$

SILICON STACKED GATE MOS INTEGRATED CIRCUIT

TC57512AD-15, -20

65,536 WORDS x 8 BITS CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

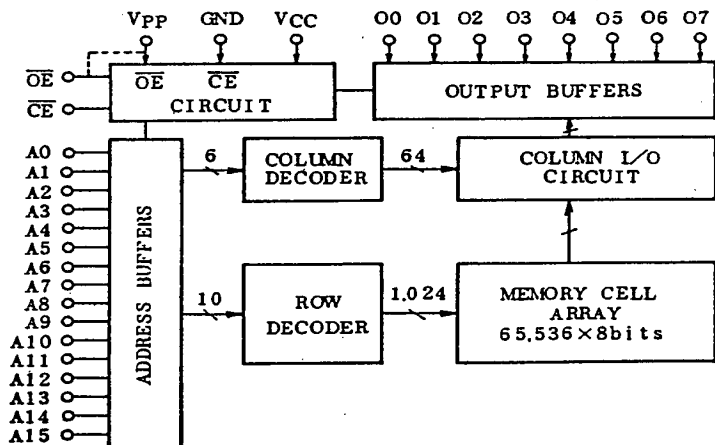
DESCRIPTION

The TC57512AD is a 65,536 word x 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory. For read operation, the TC57512AD's access time is 150ns/200ns, and the TC57512AD operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input. Advanced CMOS technology reduces the maximum active current to 30mA/6.7MHz and standby current to 100 μ A. For program operation, the programming is achieved by using the high speed programming mode. TC57512AD is fabricated with the CMOS technology and the N-channel silicon double layer gate MOS technology.

FEATURES

- Peripheral circuit: CMOS
Memory cell : N-MOS
- Fast access time:
TC57512AD-15 150ns
TC57512AD-20 200ns
- Low power dissipation
Active : 30mA/6.7MHz
Standby: 100 μ A
- Full static operation
- High speed programming mode I, II
- Inputs and outputs TTL compatible
- Standard 28 pin DIP cerdip package :WDIP28-G-600

BLOCK DIAGRAM



PIN CONNECTION (TOP VIEW)

A15	1	28	VCC
A12	2	27	A14
A7	3	26	A13
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
A3	7	22	$\overline{OE}/V_{PP}$
A2	8	21	A10
A1	9	20	$\overline{CE}$
A0	10	19	O7
O0	11	18	O6
O1	12	17	O5
O2	13	16	O4
GND	14	15	O3

MODE SELECTION

MODE	PIN	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	VCC (28)	00 ~ 07 (11 ~ 13, 15 ~ 19)	POWER
Read		L	L	5V	Data Out	Active
Output Deselect		*	H		High Impedance	
Standby		H	*		High Impedance	
Program		L	V _{PP}	6V ¹⁾ 2) 6.25V	Data In	Active
Program Inhibit		H	V _{PP}		High Impedance	
Program Verify		L	L		Data Out	

*: H or L

- 1): HIGH SPEED PROGRAMMING MODE I
2): HIGH SPEED PROGRAMMING MODE II

PIN NAMES

A0 ~ A15	Address Inputs
O0 ~ O7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}/V_{PP}$	Output Enable Input / Program Supply Voltage
VCC	Power Supply Voltage (+5V)
GND	Ground

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{CC}	V _{CC} Power Supply Voltage	-0.6 ~ 7.0	V
V _{PP}	Program Supply Voltage	-0.6 ~ 14.0	V
V _{IN}	Input Voltage	-0.6 ~ 7.0	V
V _{I/O}	Input/Output Voltage	-0.6 ~ V _{CC} +0.5	V
P _D	Power Dissipation	1.5	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STG}	Storage Temperature	-65 ~ 125	°C
T _{OPR}	Operating Temperature	-40 ~ 85	°C

READ OPERATION

D.C. AND A.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC57512AD-15/TC57512AD-20
T _a	Operating Temperature	-40 ~ 85°C
V _{CC}	V _{CC} Power Supply Voltage	5V±5%

D.C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Current	V _{IN} =0 ~ V _{CC}		-	-	±10	μA
I _{LO}	Output Leakage Current	V _{OUT} =0.4 ~ V _{CC}		-	-	±10	μA
I _{CC01}	Operating Current	$\overline{CE}$ =0V	f=6.7MHz	-	-	30	mA
I _{CC02}		I _{OUT} =0mA	f=1MHz	-	-	15	
I _{CCS1}	Standby Current	$\overline{CE}$ =V _{IH}		-	-	1	mA
I _{CCS2}		$\overline{CE}$ =V _{CC} -0.2V		-	-	100	μA
V _{IH}	Input High Voltage	-		2.2	-	V _{CC} +0.3	V
V _{IL}	Output Low Voltage	-		-0.3	-	0.8	V
V _{OH}	Output High Voltage	I _{OH} =-400μA		2.4	-	-	V
V _{OL}	Output Low Voltage	I _{OL} =2.1mA		-	-	0.4	V
I _{PP1}	V _{PP} Current	V _{PP} =0 ~ V _{CC} +0.6		-	-	±10	μA

TC57512AD-15, -20

A.C. CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	TC57512AD-15		TC57512AD-20		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE}=\overline{OE}=V_{IL}$	-	150	-	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}=V_{IL}$	-	150	-	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IL}$	-	70	-	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}=V_{IL}$	0	60	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IL}$	0	60	0	60	ns
t_{OH}	Output Data Hold Time	$\overline{CE}=\overline{OE}=V_{IL}$	0	-	0	-	ns

A.C. TEST CONDITIONS

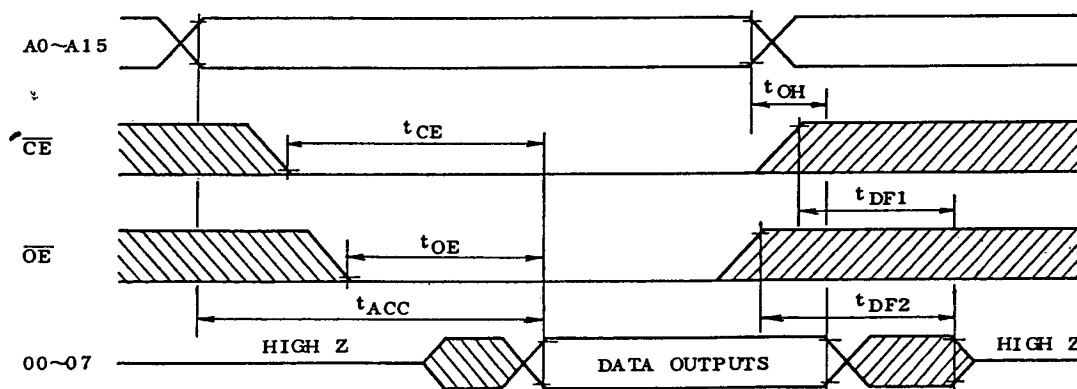
- Output Load : 1 TTL Gate and $C_L=100pF$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ~ 2.4V
- Timing Measurement Reference Level: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE *($T_a=25^\circ C$, $f=1MHz$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance	$V_{IN}=0V$	-	4	6	pF
C_{IN2}	$\overline{OE}/V_{pp}$ Input Capacitance	$V_{IN}=0V$	-	50	60	pF
C_{OUT}	Output Capacitance	$V_{OUT}=0V$	-	8	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS



HIGH SPEED PROGRAM MODE I

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{IH}	Input High Voltage	2.2	-	V _{CC} +1.0	V
V _{IL}	Input Low Voltage	-0.3	-	0.8	V
V _{CC}	V _{CC} Power Supply Voltage	5.75	6.0	6.25	V
V _{PP}	V _{PP} Power Supply Voltage	12.0	12.5	13.0	V

DC and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Current	V _{IN} =0 ~ V _{CC}	-	-	±10	μA
V _{OH}	Output High Voltage	I _{OH} =-400μA	2.4	-	-	V
V _{OL}	Output Low Voltage	I _{OL} =2.1mA	-	-	0.4	V
I _{CC}	V _{CC} Supply Current	-	-	-	30	mA
I _{PP2}	V _{PP} Supply Current	V _{PP} =13.0V	-	-	50	mA

AC PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t _{AS}	Address Setup Time	-	2	-	-	μs
t _{AH}	Address Hold Time	-	2	-	-	μs
t _{OES}	$\overline{\text{OE}}$ /V _{PP} Setup Time	-	2	-	-	μs
t _{OEH}	$\overline{\text{OE}}$ /V _{PP} Hold Time	-	2	-	-	μs
t _{PRT}	$\overline{\text{OE}}$ /V _{PP} Pulse Rise Time	-	50	-	-	ns
t _{DS}	Data Setup Time	-	2	-	-	μs
t _{DH}	Data Hold Time	-	2	-	-	μs
t _{VR}	$\overline{\text{OE}}$ /V _{PP} Recovery Time	-	2	-	-	μs
t _{VCS}	V _{CC} Setup Time	-	2	-	-	μs
t _{PW}	Initial Program Pulse Width	$\overline{\text{CE}}=V_{IL}$, $\overline{\text{OE}}/V_{PP}=V_{PP}$	0.95	1.0	1.05	ms
t _{OPW}	Overprogram Pulse Width	Note 1	2.85	3.0	78.75	ms
t _{DV}	Data Valid from $\overline{\text{CE}}$	$\overline{\text{OE}}/V_{PP}=V_{IL}$	-	-	1	μs
t _{DF}	$\overline{\text{CE}}$ to Output in High-Z	$\overline{\text{OE}}/V_{PP}=V_{IL}$	-	-	130	ns

AC TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ~ 2.4V
- Timing Measurement Reference Level: Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

TC57512AD-15, -20

HIGH SPEED PROGRAM MODE II

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{IH}	Input High Voltage	2.2	-	V _{CC} +1.0	V
V _{IL}	Input Low Voltage	-0.3	-	0.8	V
V _{CC}	V _{CC} Power Supply Voltage	6.0	6.25	6.5	V
V _{PP}	V _{PP} Power Supply Voltage	12.5	12.75	13.0	V

DC and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6.25V±0.25V, V_{PP}=12.75V±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Current	V _{IN} =0 ~ V _{CC}	-	-	±10	μA
V _{OH}	Output High Voltage	I _{OH} =-400μA	2.4	-	-	V
V _{OL}	Output Low Voltage	I _{OL} =2.1mA	-	-	0.4	V
I _{CC}	V _{CC} Supply Current	-	-	-	30	mA
I _{PP2}	V _{PP} Supply Current	V _{PP} =13.0V	-	-	50	mA

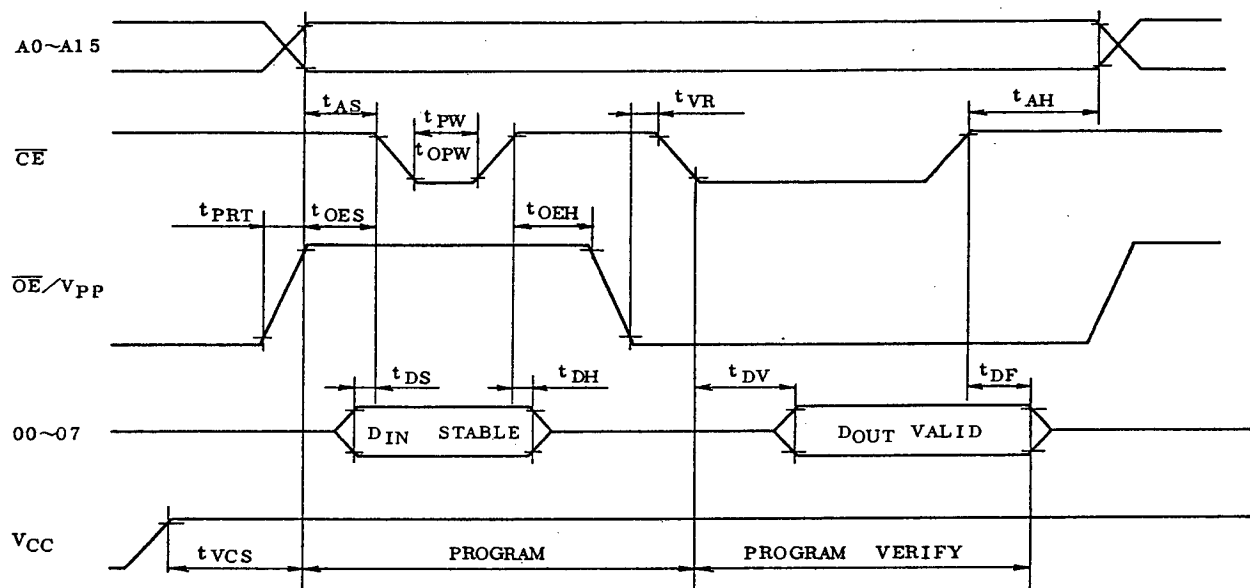
AC PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6.25V±0.25V, V_{PP}=12.75V±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t _{AS}	Address Setup Time	-	2	-	-	μs
t _{AH}	Address Hold Time	-	2	-	-	μs
t _{OES}	$\overline{OE}/V_{PP}$ Setup Time	-	2	-	-	μs
t _{OEH}	$\overline{OE}/V_{PP}$ Hold Time	-	2	-	-	μs
t _{PRI}	$\overline{OE}/V_{PP}$ Pulse Rise Time	-	50	-	-	ns
t _{DS}	Data Setup Time	-	2	-	-	μs
t _{DH}	Data Hold Time	-	2	-	-	μs
t _{VR}	$\overline{OE}/V_{PP}$ Recovery Time	-	2	-	-	μs
t _{VCS}	V _{CC} Setup Time	-	2	-	-	μs
t _{PW}	Program Pulse Width	$\overline{CE}=V_{IL}$, $\overline{OE}/V_{PP}=V_{PP}$	0.095	0.1	0.105	ms
t _{DV}	Data Valid from $\overline{CE}$	$\overline{OE}/V_{PP}=V_{IL}$	-	-	1	μs
t _{DF}	$\overline{CE}$ to Output in High-Z	$\overline{OE}/V_{PP}=V_{IL}$	-	-	130	ns

AC TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ~ 2.4V
- Timing Measurement Reference Level: Input 0.8V and 2.0V, Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAMMING MODE I ($V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)HIGH SPEED PROGRAMMING MODE II ($V_{CC}=6.25V\pm0.25V$, $V_{PP}=12.75V\pm0.25V$)

- Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP} .
2. Removing the device from socket and setting the device in socket with $V_{PP}=12.5\pm0.5V$ or $V_{PP}=12.75\pm0.25V$ may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

TC57512AD-15, -20

ERASURE CHARACTERISTICS

The TC57512AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. Then intergrated does (ultraviolet light intensity [w/cm^2] $\times$ exposure time [sec.]) for erasure should be a minimum of 15 [$\text{w}\cdot\text{sec}/\text{cm}^2$]. When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [$\mu\text{w}/\text{cm}^2$] will reduce the exposure time to about 20 minutes. (In this case, the integrated does is 12000 [$\mu\text{w}/\text{cm}^2$] $\times$ (20 $\times$ 60) [sec] $\approx$ 15 [$\text{w}\cdot\text{sec}/\text{cm}^2$].) The TC57512AD's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the flourescent lamps will include 3000 $\sim$ 4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TC57512AD's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

PIN NAMES (NUMBER)		$\overline{\text{CE}}$ (20)	$\overline{\text{OE}}/\text{V}_{\text{PP}}$ (22)	V_{CC} (28)	00 $\sim$ 07 (11 $\sim$ 13, 15 $\sim$ 19)	POWER
MODE						
Read Operation ($T_a = -40 \sim 85^\circ\text{C}$)	Read	L	L	5V	Data Out	Active
	Output Deselect	*	H		High Impedance	
	Standby	H	*		High Impedance	Standby
Program Operation ($T_a = 25 \pm 5^\circ\text{C}$)	Program	L	V_{PP}	6V1)	Data In	Active
	Program Inhibit	H	V_{PP}	2)	High Impedance	
	Program Verify	L	L	6.25V	Data Out	

Note: H; V_{IH} , L; V_{IL} , *; V_{IH} or V_{IL}

1); HIGH SPEED PROGRAMMING MODE I

2); HIGH SPEED PROGRAMMING MODE II

READ MODE

The TC57512AD has two control functions. The chip enable ($\overline{\text{CE}}$) controls the operation power and should be used for device selection. The output enable ($\overline{\text{OE}}$) control the output buffers, independent of device selection. Assuming that $\overline{\text{CE}} = \overline{\text{OE}} = \text{V}_{\text{IL}}$, the output data is valid at the outputs after address access time from stabilizing of all addresses. The $\overline{\text{CE}}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}). Assuming that $\overline{\text{CE}} = \text{V}_{\text{IL}}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{\text{OE}}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state. So two or more TC57512AD's can be connected together on a common bus line. When $\overline{CE}$ is decode for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC57512AD has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC57512AD is placed in the standby mode which reduce the operating current to 100 μ A by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC57512AD are in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming. The TC57512AD is in the programming mode when the $\overline{OE}/V_{pp}$ input is at 12.5V or 12.75V and $\overline{CE}$ is at TTL-Low level. The TC57512AD can be programmed any location at any time either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with $\overline{OE}/V_{pp}$ at V_{IL} and $\overline{CE}$ at V_{IL} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V or +12.75V) is applied to V_{pp} terminal, a high level $\overline{CE}$ input inhibits the TC57512AD from being programmed. Programming of two or more TC57512AD's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM MODE I

This high speed programming mode I is performed at $V_{CC}=6.0V$ and $\overline{OE}/V_{pp}=12.5V$.

The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with pulse width 3 times that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC}=5V$.

HIGH SPEED PROGRAM MODE II

The program time can be greatly decreased by using this high speed programming mode II. This high speed programming mode II is performed at $V_{CC}=6.25V$ and $\overline{OE}/V_{pp}=12.75V$.

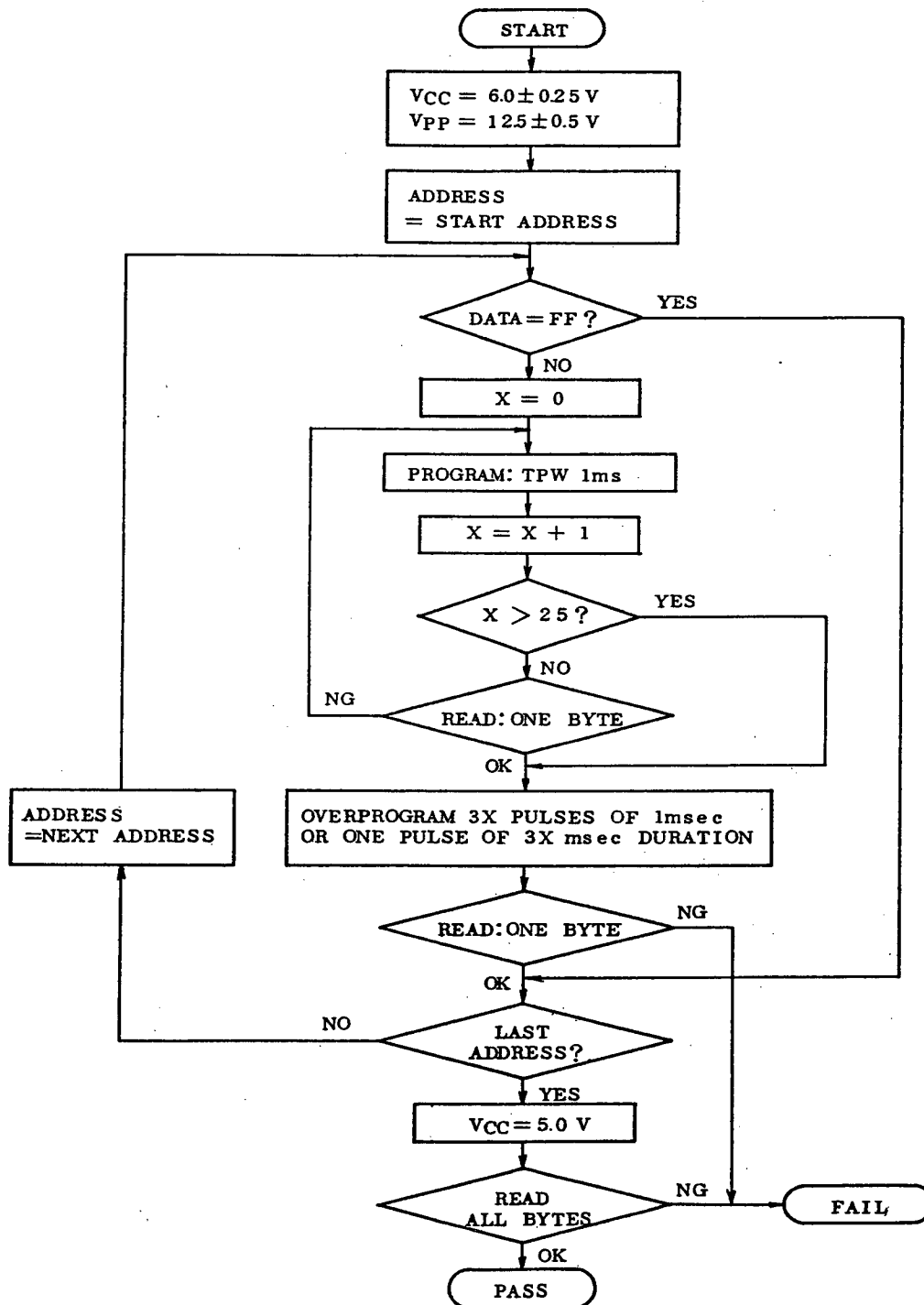
The programming is achieved by applying a single TTL low level 0.1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 0.1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{CC}=5V$.

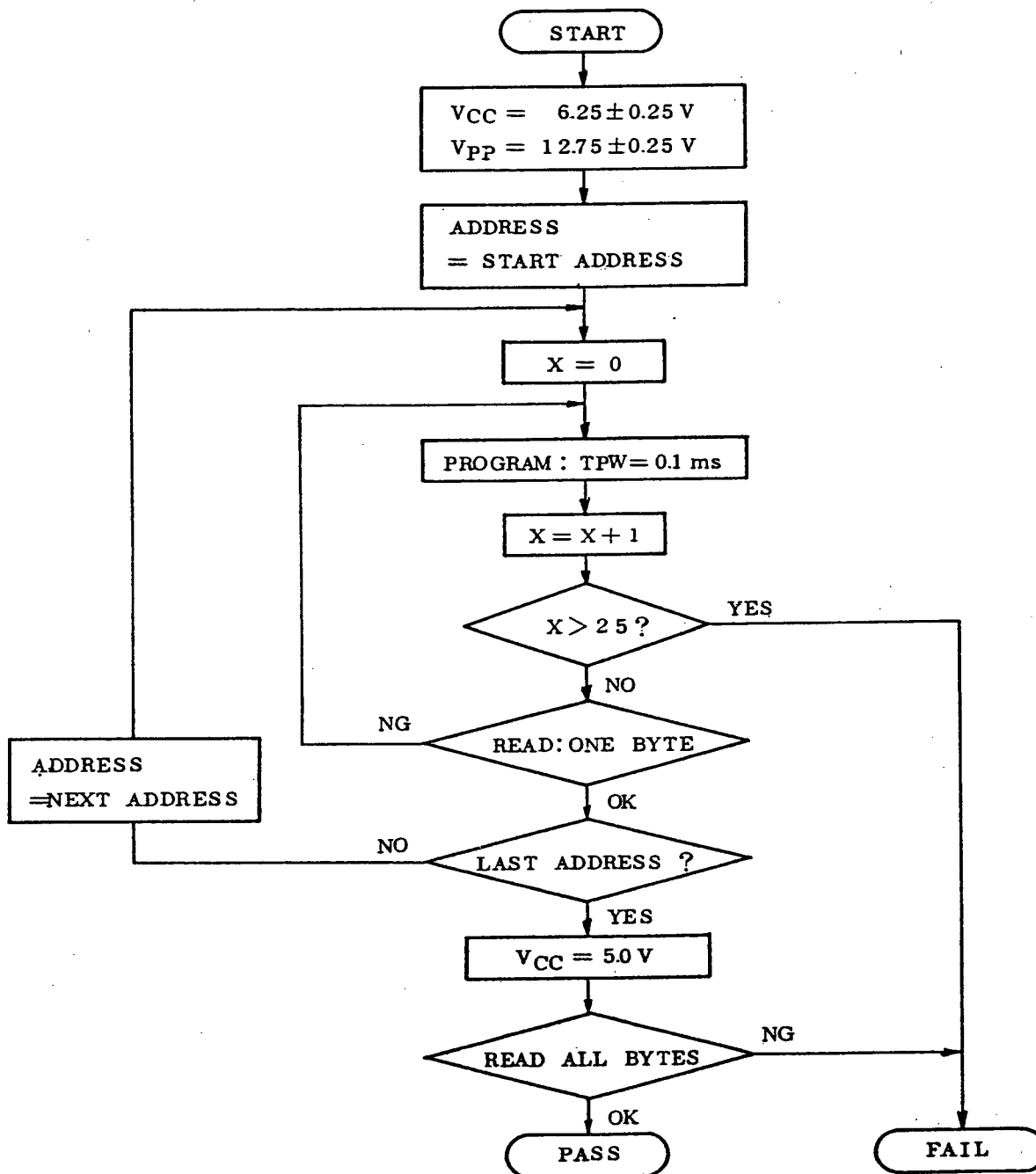
HIGH SPEED PROGRAM MODE I

FLOW CHART



HIGH SPEED PROGRAM MODE II

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC57512AD which identifies its manufacturer and device type.

The programming equipment may reads out manufacturer code and device code from TC57512AD by using this mode before program operation and automatically set program voltage (V_{pp}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH} . These two codes possess an odd parity with the parity bit of MSB (07).

The following table shows electric signature of TC57512AD.

SIGNATURE	PINS	A0	07	06	05	04	03	02	01	00	HEX.
		(10)	(19)	(18)	(17)	(16)	(15)	(13)	(12)	(11)	DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	0	98
Device Code	V_{IH}	1	0	0	0	0	1	0	1	1	85

Notes: A9=12V±0.5V

A1 ~ A8, A10 ~ A15, $\overline{CE}$, $\overline{OE}$ = V_{IL}

TC571000AD-12,-150

TC571001AD-12,-150

SILICON STACKED GATE MOS
INTEGRATED CIRCUIT

131,072 WORD×8 BIT CMOS UV ERASABLE AND ELECTRICALLY
PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The TC571000AD/TC571001AD is a 131,072 word × 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory.

The TC571000AD is JEDEC standard pin configuration and the TC571001AD is compatible with 28 pin 1M bit Mask ROM. Both products are packed in 32 pin standard cerdip package.

The TC571000AD/TC571001AD is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 30mA/8.3MHz and access time of 120ns/150ns.

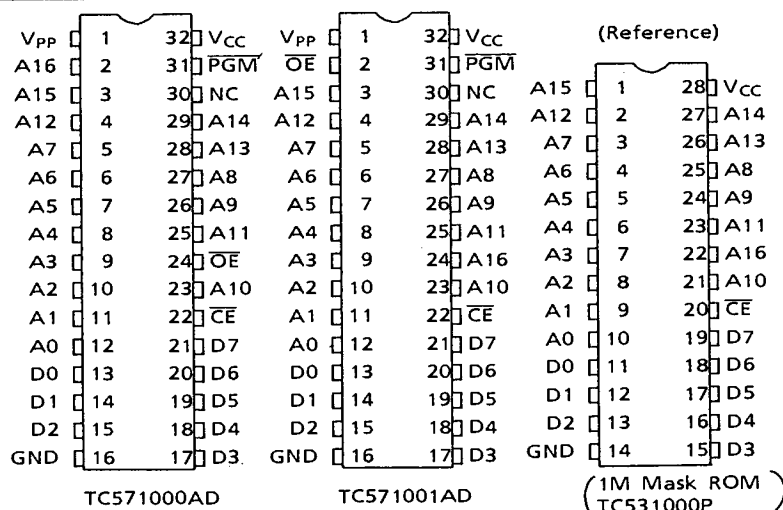
The programming times of the TC571000AD/TC571001AD except overhead times of EPROM programmer is only 14 seconds by using the high speed programming algorithm.

FEATURES

- Peripheral circuit : CMOS
- Memory cell : N-MOS
- Access time

	- 12	- 12 / - 150
V _{CC}	5V ± 5%	5V ± 10%
t _{ACC}	120ns	150ns
- Low power dissipation
 - Active : 30mA/8.3MHz
 - Standby: 100μA
- Wide operating temperature range : 0~70°C
- Single 5V power supply
- Full static operation
- High speed programming operation : tpw 0.1ms
- Input and output TTL compatible
- JEDEC standard 32 pin : TC571000AD
- 1M MROM compatible : TC571001AD
- Standard 32 pin DIP cerdip package : WDIP32-G-600

PIN CONNECTION (TOP VIEW)

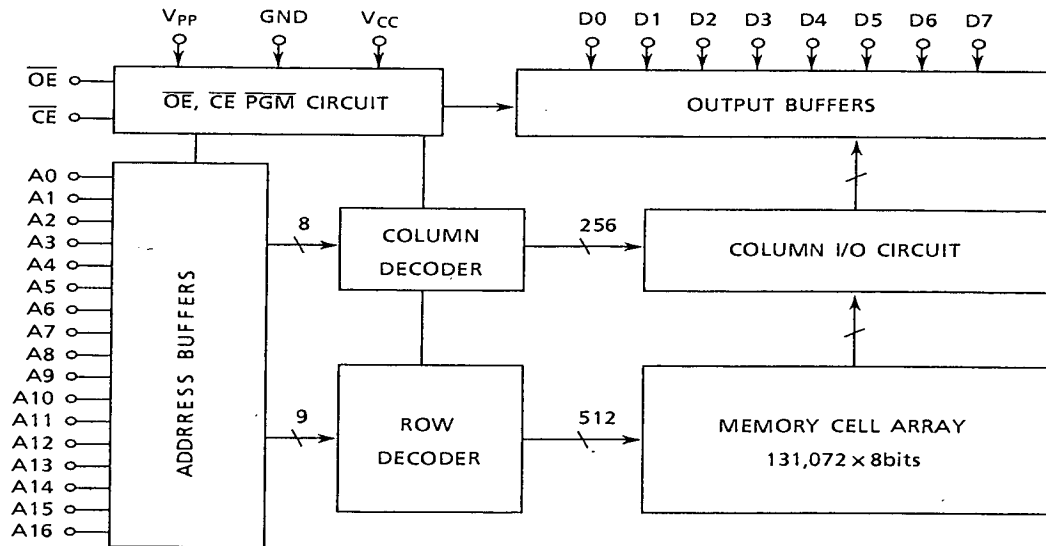


PIN NAMES

A0~A16	Address Inputs
D0~D7	Outputs (Inputs)
CE	Chip Enable Input
OE	Output Enable Input
PGM	Program Control Input
V _{CC}	V _{CC} Supply Voltage
V _{PP}	Program Supply Voltage
GND	Ground
NC	No Connection

TC571000AD-12, -150 TC571001AD-12, -150

BLOCK DIAGRAM



MODE SELECTION

MODE \ PIN	PGM	CE	OE	V _{PP}	V _{CC}	D0~D7	Power
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	H	12.75V	6.25V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

* : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{CC}	V _{CC} Power Supply Voltage	- 0.6~7.0	V
V _{PP}	Program Supply Voltage	- 0.6~14.0	V
V _{IN}	Input Voltage	- 0.6~7.0	V
V _{IO}	Input/ Output Voltage	- 0.6~V _{CC} + 0.5	V
P _D	Power Dissipation	1.5	W
T _{SOLDER}	Soldering Temperature Time	260 · 10	°C · sec
T _{STRG}	Storage Temperature	- 65~125	°C
T _{OPR}	Operating Temperature	0~70	°C

TC571000AD-12, -150 TC571001AD-12, -150

READ OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC571000AD / 1001AD - 12		TC571000AD / 1001AD - 12 / - 150		UNIT
		MIN.	MAX.	MIN.	MAX.	
V_{IH}	Input High Voltage	2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage	- 0.3	0.8	- 0.3	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.25	4.50	5.50	V
V_{PP}	V_{PP} Power Supply Voltage	$V_{CC} - 0.6$	$V_{CC} + 0.6$	$V_{CC} - 0.6$	$V_{CC} + 0.6$	V

DC AND OPERATING CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	—	—	± 10	μA
I_{CCO1}	Operating Current	$\overline{CE} = 0V$	—	—	30	mA
I_{CCO2}		$I_{OUT} = 0mA$	—	—	15	
I_{CCS1}	Standby Current	$\overline{CE} = V_{IH}$	—	—	1	mA
I_{CCS2}		$\overline{CE} = V_{CC} - 0.2V$	—	—	100	
V_{OH}	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1mA$	—	—	0.4	V
I_{PP1}	V_{PP} Current	$V_{PP} = V_{CC} \pm 0.6V$	—	—	± 10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 0.4V \sim V_{CC}$	—	—	10	μA

AC CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{PP} = V_{CC} \pm 0.6V$)

SIMBOL	PARAMETER	TC571000AD / 1001AD - 12		TC571000AD / 1001AD - 12 / - 150		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	—	120	—	150	ns
t_{CE}	$\overline{CE}$ to Output Valid	—	120	—	150	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	60	—	70	ns
t_{PGM}	$\overline{PGM}$ to Output Valid	—	60	—	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	50	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	50	0	60	ns
t_{DF3}	$\overline{PGM}$ to Output in High-Z	0	50	0	60	ns
t_{OH}	Output Data Hold Time	0	—	0	—	ns

TC571000AD/TC571001AD-12 are satisfied with the specification of TC571000AD/TC571001AD-150.

AC TEST CONDITIONS

- Output Load : 1 TTL Gate and $C_L = 100pF$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V~2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

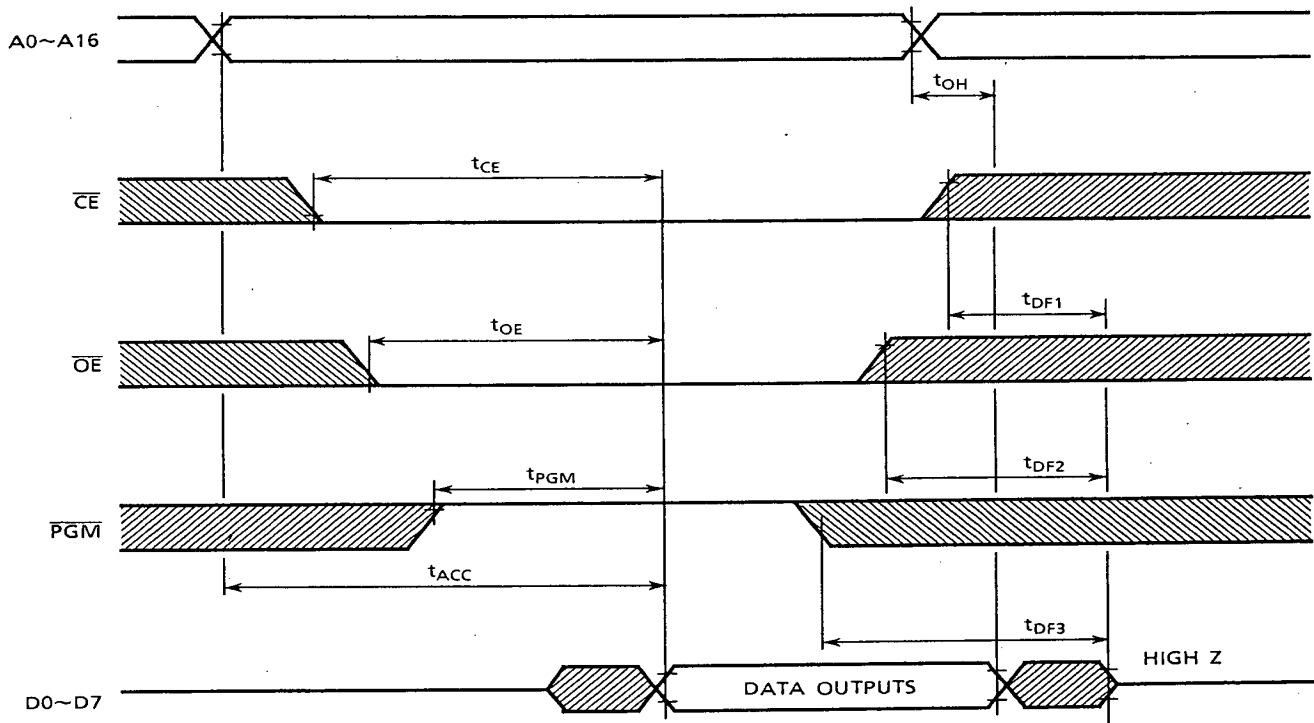
TC571000AD-12,-150 TC571001AD-12,-150

CAPACITANCE* ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$	—	16	P_F
C_{OUT}	Output Capacitance	$V_{OUT} = 0\text{V}$	—	16	

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



TC571000AD-12, -150 TC571001AD-12, -150

HIGH SPEED PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	$V_{CC} + 1.0$	V
V_{IL}	Input Low Voltage	- 0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.50	12.75	13.00	V

DC AND OPERATING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.75\text{V} \pm 0.25\text{V}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	—	—	± 10	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{mA}$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	30	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP} = 13.0\text{V}$	—	—	50	mA

AC PROGRAMMING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.75\text{V} \pm 0.25\text{V}$)

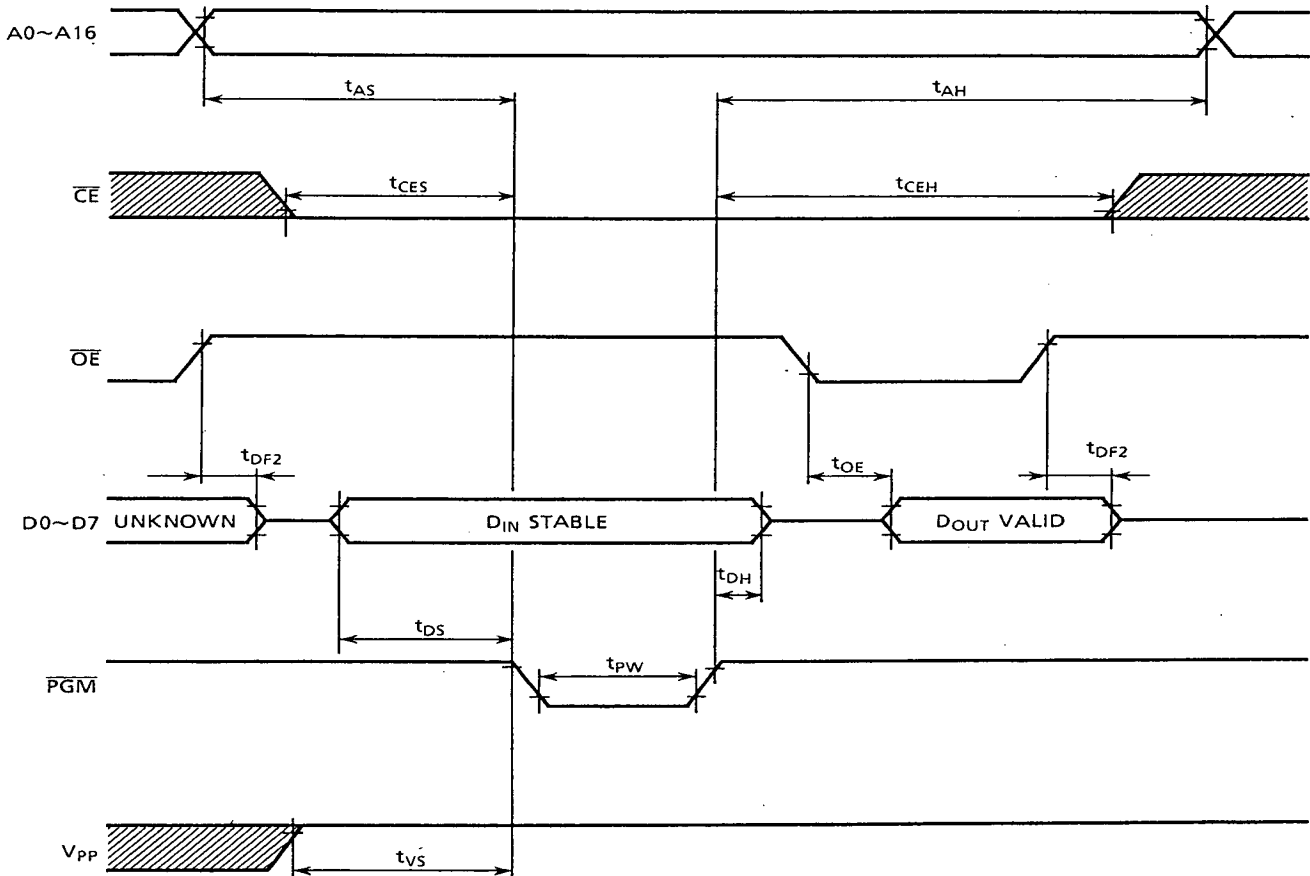
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	2	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	2	—	—	μs
t_{DS}	Data Set up Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VS}	V_{PP} Set up Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	—	0.095	0.1	0.105	ms
t_{OE}	$\overline{OE}$ to Output Valid	—	—	—	100	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE} = V_{IL}$	—	—	90	ns

AC TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V~2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAM OPERATION



- Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.
2. Removing the device from socket and setting the device in socket with V_{PP}=12.75V may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

TC571000AD-12, -150 TC571001AD-12, -150

ERASURE CHARACTERISTICS

The TC571000AD / TC571001AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window.

Then integrated dose (ultraviolet light intensity [w/cm²]×exposure time [sec.]) for erasure should be a minimum of 15 [w·sec/cm²].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is a 12000 [μw/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000[μw/cm²]×(20×60) [sec.] ≈15 [w·sec/cm²].)

The TC571000AD / TC571001AD's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TC571000AD / TC571001AD's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN		PGM	CE	OE	V _{PP}	V _{CC}	D0~D7	POWER
Read Operation (Ta = 0~70°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselet	*	*	H			High Impedance	
	Standby	*	H	*			High Impedance	Standby
Program Operation (Ta = 25 ± 5°C)	Program	L	L	H	12.75V	6.25V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	
		H	L	H			High Impedance	
	Program Verify	H	L	L			Data Out	

Note : H ; V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TC571000AD / TC571001AD has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection. The output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers independent of device selection.

Assuming in that $\overline{CE} = \overline{OE} = V_{IL}$ and $\overline{PGM} = V_{IH}$, the output data is valid at the output after address access time from stabilizing of all addresses. The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$. And assuming that $\overline{CE} = \overline{OE} = V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$, the outputs will be in a high impedance state. So two or more ROMs can be connected together on a common bus line. When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC571000AD / TC571001AD has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC571000AD / TC571001AD is placed in the standby mode which reduce the operating current to $100\mu A$ by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC571000AD / TC571001AD is in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming. The levels required for all inputs are TTL.

The TC571000AD / TC571001AD can be programmed any location at anytime either individually, sequentially, or at random.

TC571000AD-12, -150 TC571001AD-12, -150

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.75V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TC571000AD/TC571001AD from being programmed.

Programming of two or more EPROM's in inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM MODE

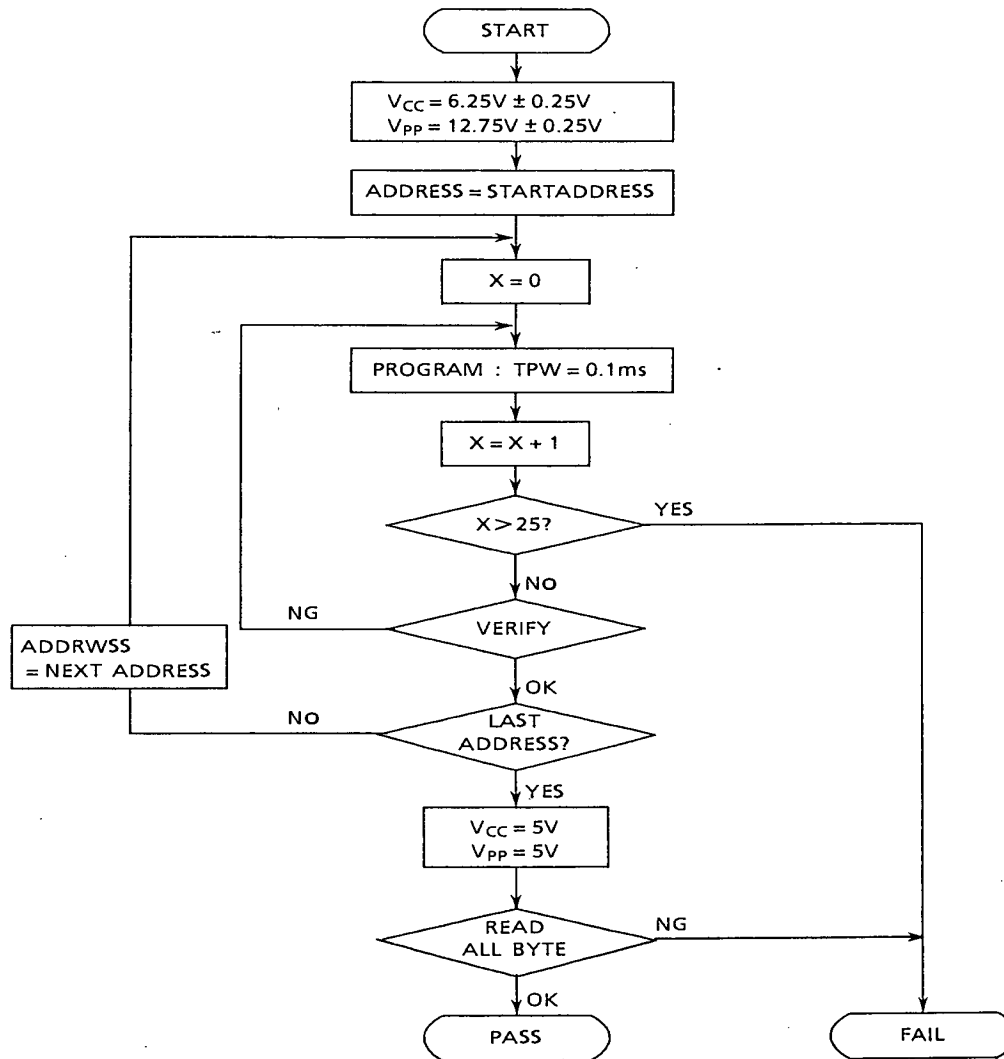
The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the V_{PP} terminal with $V_{CC}=6.25V$ and $\overline{PGM}=V_{IH}$.

The programming is achieved by applying a single TTL low level 0.1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM MODE

FLOW CHART



TC571000AD-12, -150

TC571001AD-12, -150

ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC571000AD / TC571001AD which identifies its manufacturer and device type.

The programming equipment may reads out manufacturer code and device code from TC571000AD / TC571001AD by using this mode before program operation and automatically set program voltage (Vpp) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}.

These two codes possess an odd parity with the parity bit of MSB (D7).

The following table shows electric signature of TC571000AD / TC571001AD.

SIGNATURE \ PINS		A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX Data
Manufacture Code		V _{IL}	1	0	0	1	1	0	0	0	98
Device Code	TC571000AD	V _{IH}	1	0	0	0	0	1	1	0	86
	TC571001AD		0	0	0	0	0	1	1	1	07

Notes : A9=12V±0.5V

A1~A8, A0~A16, $\overline{CE}$, $\overline{OE}$ =V_{IL}

$\overline{PGM}$ =V_{IH}

SILICON STACKED GATE MOS INTEGRATED CIRCUIT

TC57H1000AD-85, -100 TC57H1001AD-85, -100

131,072 WORD × 8 BIT CMOS UV ERASABLE AND ELECTRICALLY
PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The TC57H1000AD/TC57H1001AD is a 131,072 word × 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory.

The TC57H1000AD is JEDEC standard pin configuration and the TC57H1001AD is compatible with 28 pin 1M bit Mask ROM. Both products are packed in 32 pin standard cerdip package.

The TC57H1000AD/TC57H1001AD is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 40mA/11.8MHz and access time of 85ns/100ns.

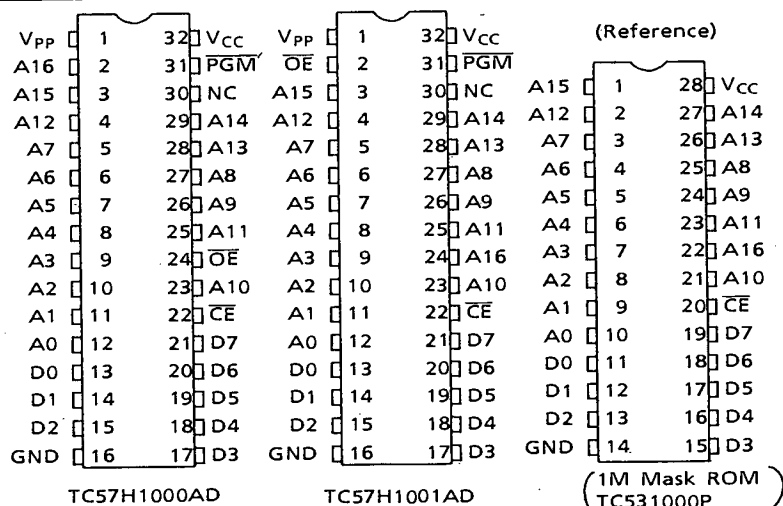
The programming times of the TC57H1000AD / TC57H1001AD except overhead times of EPROM programmer is only 14 seconds by using the high speed programming algorithm.

FEATURES

- Peripheral circuit : CMOS
- Memory cell : N-MOS
- Access time

	- 85	- 85 / - 100
t _{ACC}	85ns	100ns
V _{CC}	5V ± 5%	5V ± 10%
- Low power dissipation
 - Active : 40mA / 11.8MHz
 - Standby: 100μA (T_a = 70°C)
- Wide operating temperature range : 0~70°C
- Single 5V power supply
- Full static operation
- High speed programming operation : tpw 0.1ms
- Input and output TTL compatible
- JEDEC standard 32 pin : TC57H1000AD
- 1M MROM compatible : TC57H1001AD
- Standard 32 pin DIP cerdip package : WDIP32-G-600

PIN CONNECTION (TOP VIEW)

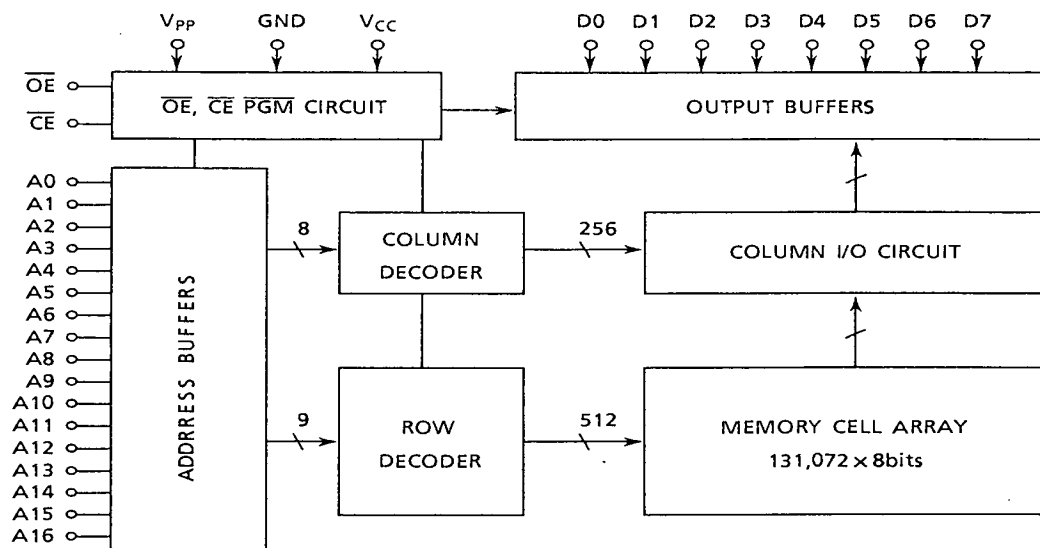


PIN NAMES

A0~A16	Address Inputs
D0~D7	Outputs (Inputs)
CE	Chip Enable Input
OE	Output Enable Input
PGM	Program Control Input
V _{CC}	V _{CC} Supply Voltage
V _{PP}	Program Supply Voltage
GND	Ground
NC	No Connection

TC57H1000AD-85, -100 TC57H1001AD-85, -100

BLOCK DIAGRAM



MODE SELECTION

MODE \ PIN	PGM	CE	OE	V _{PP}	V _{CC}	D0~D7	Power
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	H	12.75V	6.25V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

* : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{CC}	V _{CC} Power Supply Voltage	-0.6~7.0	V
V _{PP}	Program Supply Voltage	-0.6~14.0	V
V _{IN}	Input Voltage	-0.6~7.0	V
V _{I/O}	Input / Output Voltage	-0.6~V _{CC} +0.5	V
P _D	Power Dissipation	1.5	W
T _{SOLDER}	Soldering Temperature Time	260 · 10	°C · sec
T _{STRG}	Storage Temperature	-65~125	°C
T _{OPR}	Operating Temperature	0~70	°C

TC57H1000AD-85, -100 TC57H1001AD-85, -100

READ OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC57H1000AD / 1001AD - 85			TC57H1000AD / 1001AD - 100			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{IH}	Input High Voltage	2.2	—	$V_{CC} + 0.3$	2.2	—	$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage	- 0.3	—	0.8	- 0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	4.50	5.00	5.50	V
V_{PP}	V_{PP} Power Supply Voltage	$V_{CC} - 0.6$	V_{CC}	$V_{CC} + 0.6$	$V_{CC} - 0.6$	V_{CC}	$V_{CC} + 0.6$	V

DC AND OPERATING CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	—	—	± 10	μA
I_{CCO1}	Operating Current	$\overline{CE} = 0V$ $I_{OUT} = 0\text{mA}$	—	—	40	mA
I_{CCO2}		$f = 11.8\text{MHz}$ $f = 1\text{MHz}$	—	—	15	
I_{CCS1}	Standby Current	$\overline{CE} = V_{IH}$	—	—	1	mA
I_{CCS2}		$\overline{CE} = V_{CC} - 0.2V$	—	—	100	
V_{OH}	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{mA}$	—	—	0.4	V
I_{PP1}	V_{PP} Current	$V_{PP} = V_{CC} \pm 0.6V$	—	—	± 10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 0.4V \sim V_{CC}$	—	—	10	μA

AC CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{PP} = V_{CC} \pm 0.6V$)

SIMBOL	PARAMETER	TC57H1000AD / 1001AD - 85		TC57H1000AD / 1001AD - 100		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	—	85	—	100	ns
t_{CE}	$\overline{CE}$ to Output Valid	—	85	—	100	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	45	—	50	ns
t_{PGM}	$\overline{PGM}$ to Output Valid	—	45	—	50	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	30	0	40	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	30	0	40	ns
t_{DF3}	$\overline{PGM}$ to Output in High-Z	0	30	0	40	ns
t_{OH}	Output Data Hold Time	0	—	0	—	ns

TC57H1000AD/TC57H1001AD-85 are satisfied with the specification of TC57H1000AD/TC57H1001AD-100

AC TEST CONDITIONS

- Output Load : 1 TTL Gate and $C_L = 100\text{pF}$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V~2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

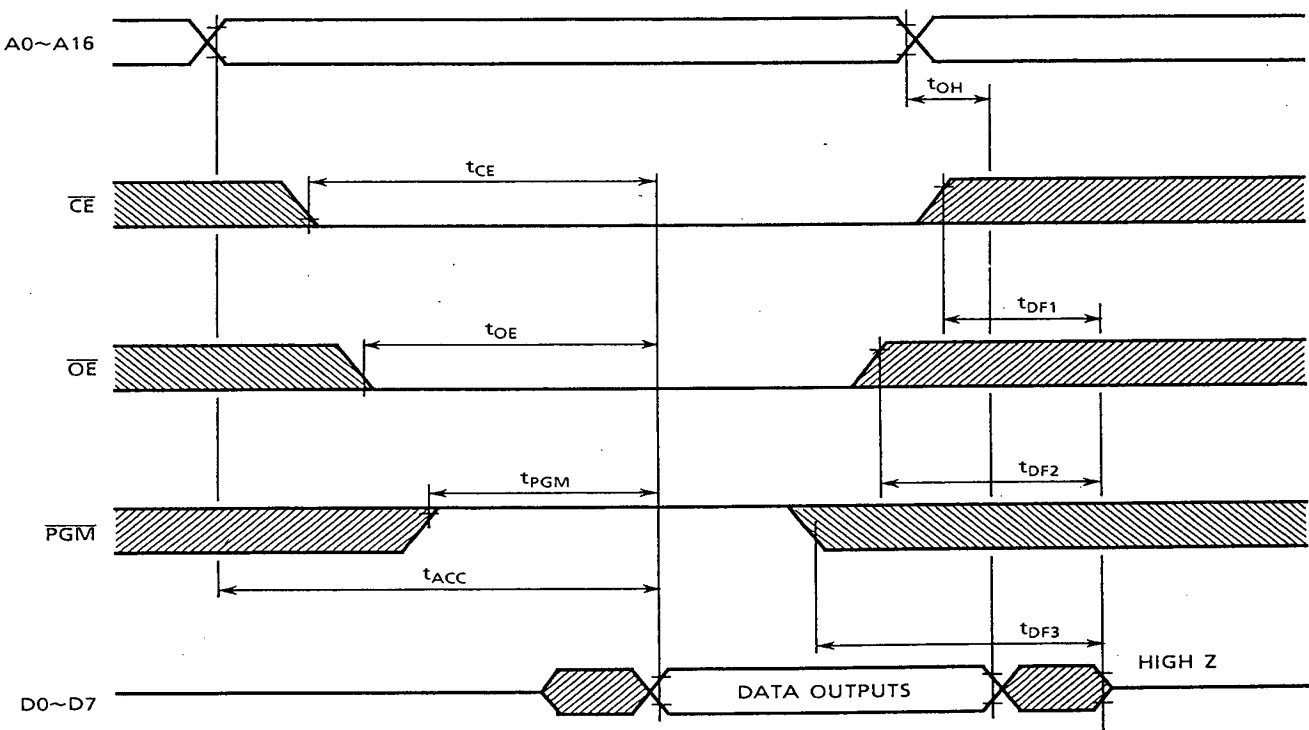
TC57H1000AD-85,-100
TC57H1001AD-85,-100

CAPACITANCE* (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = 0V	—	16	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	—	16	

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



TC57H1000AD-85,-100 TC57H1001AD-85,-100

HIGH SPEED PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	$V_{CC} + 1.0$	V
V_{IL}	Input Low Voltage	-0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.50	12.75	13.00	V

DC AND OPERATING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.75\text{V} \pm 0.25\text{V}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	—	—	± 10	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{mA}$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	30	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP} = 13.0\text{V}$	—	—	50	mA

AC PROGRAMMING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.75\text{V} \pm 0.25\text{V}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	2	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	2	—	—	μs
t_{DS}	Data Set up Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VS}	V_{PP} Set up Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	—	0.095	0.1	0.105	ms
t_{OE}	$\overline{OE}$ to Output Valid	—	—	—	100	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE} = V_{IL}$	—	—	90	ns

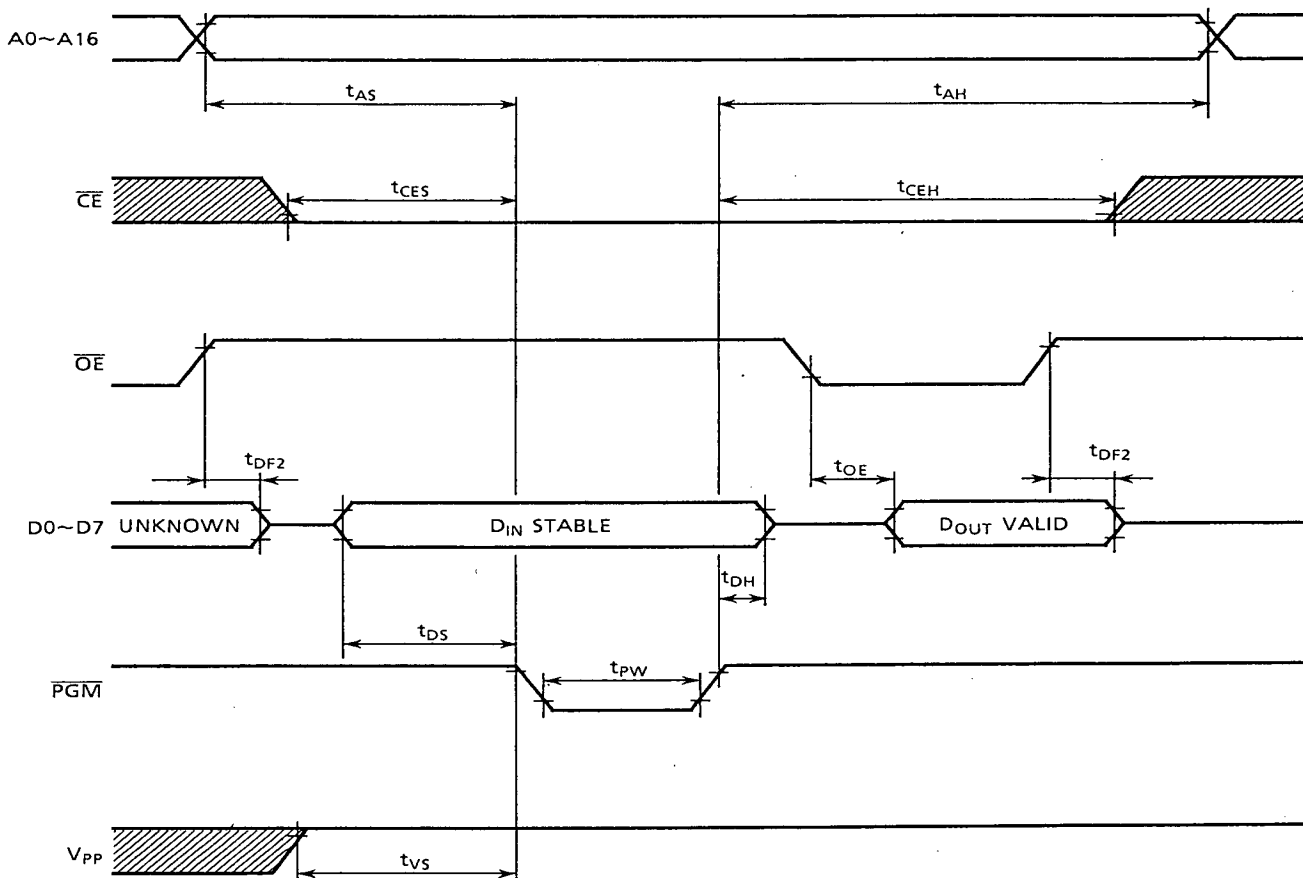
AC TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V~2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

TC57H1000AD-85, -100 TC57H1001AD-85, -100

TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAM OPERATION



- Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.
2. Removing the device from socket and setting the device in socket with V_{PP}=12.75V may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC57H1000AD / TC57H1001AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window.

Then integrated dose (ultraviolet light intensity [w/cm²]×exposure time [sec.]) for erasure should be a minimum of 15 [w·sec/cm²].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is a 12000 [μw/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000[μw/cm²]×(20×60) [sec.] ≈15 [w·sec/cm²].)

The TC57H1000AD / TC57H1001AD's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TC57H1000AD / TC57H1001AD's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

MODE		PIN	PGM	CE	OE	V _{PP}	V _{CC}	D0~D7	POWER
Read Operation (Ta = 0~70°C)	Read		H	L	L	5V	5V	Data Out	Active
	Output Deselet		*	*	H			High Impedance	
	Standby		*	H	*			High Impedance	Standby
Program Operation (Ta = 25 ± 5°C)	Program		L	L	H	12.75V	6.25V	Data In	Active
	Program Inhibit		*	H	*			High Impedance	
			H	L	H			High Impedance	
	Program Verify		H	L	L			Data Out	

Note : H ; V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

TC57H1000AD-85,-100

TC57H1001AD-85,-100

READ MODE

The TC57H1000AD/TC57H1001AD has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection. The output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers independent of device selection.

Assuming in that $\overline{CE} = \overline{OE} = V_{IL}$ and $\overline{PGM} = V_{IH}$, the output data is valid at the output after address access time from stabilizing of all addresses. The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$. And assuming that $\overline{CE} = \overline{OE} = V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$, the outputs will be in a high impedance state. So two or more ROMs can be connected together on a common bus line. When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC57H1000AD/TC57H1001AD has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC57H1000AD/TC57H1001AD is placed in the standby mode which reduce the operating current to $100\mu A$ by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC57H1000AD/TC57H1001AD is in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming. The levels required for all inputs are TTL.

The TC57H1000AD/TC57H1001AD can be programmed any location at anytime either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.75V) is applied to V_{pp} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TC57H1000AD/TC57H1001AD from being programmed.

Programming of two or more EPROM's in inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM MODE

The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the V_{pp} terminal with $V_{CC}=6.25V$ and $\overline{PGM}=V_{IH}$.

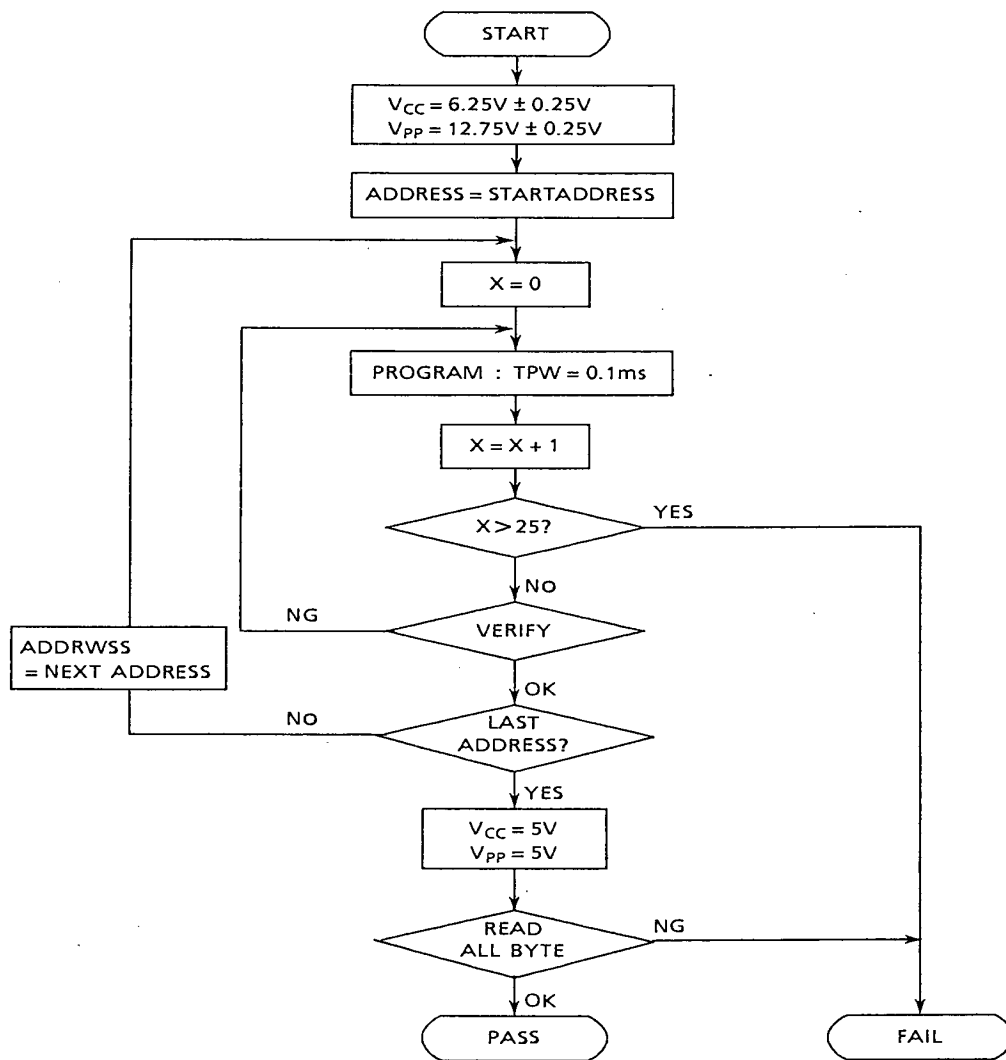
The programming is achieved by applying a single TTL low level 0.1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{pp}=5V$.

TC57H1000AD-85,-100 TC57H1001AD-85,-100

HIGH SPEED PROGRAM MODE

FLOW CHART



TC57H1000AD-85, -100 TC57H1001AD-85, -100

ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC57H1000AD / TC57H1001AD which identifies its manufacturer and device type.

The programming equipment may reads out manufacturer code and device code from TC57H1000AD / TC57H1001AD by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH} .

These two codes possess an odd parity with the parity bit of MSB (D7).

The following table shows electric signature of TC57H1000AD / TC57H1001AD.

PINS		A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX Data
SIGNATURE											
Manufacture Code		V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	TC57H1000AD	V_{IH}	1	0	0	0	0	1	1	0	86
	TC57H1001AD		0	0	0	0	0	1	1	1	07

Notes : A9 = 12V $\pm$ 0.5V

A1~A8, A0~A16, $\overline{CE}$, $\overline{OE}$ = V_{IL}

$\overline{PGM}$ = V_{IH}

TC57H1024AD-85, -100

1 MEGA BIT (65,536 WORD $\times$ 16 BIT)

CMOS U.V. ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The TC57H1024AD is a 65,536 word $\times$ 16 bit CMOS ultraviolet light erasable and electrically programmable read only memory. The TC57H1024AD is JEDEC standard pin configuration. This product is packed in 40 pin standard cerdip package.

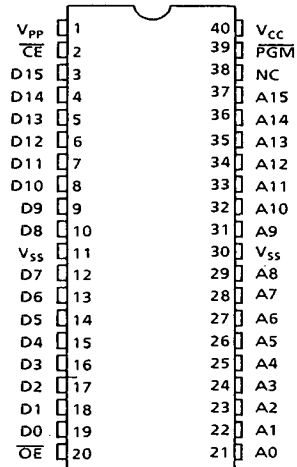
TC57H1024AD is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 40mA/1MHz and access time of 85ns/100ns.

The programming times of the TC57H1024AD except overhead times of EPROM programmer is only 7 seconds by using the high speed programming algorithm.

FEATURES

- Peripheral circuit : CMOS
- Memory cell : NMOS
- Fast access time
 - TC57H1024AD-85 : 85ns
 - TC57H1024AD-100 : 100ns
- 85 is satisfied with the specification of -100
- Low power dissipation
 - Active : 40mA/1MHz
 - Standby : 100 μ A
- Single 5V power supply
- Full static operation
- High speed programming operation : tpw 0.1ms
- Input and output TTL compatible
- JEDEC standard 40 pin
- Standard 40 pin DIP cerdip package : WDIP40-G-600A

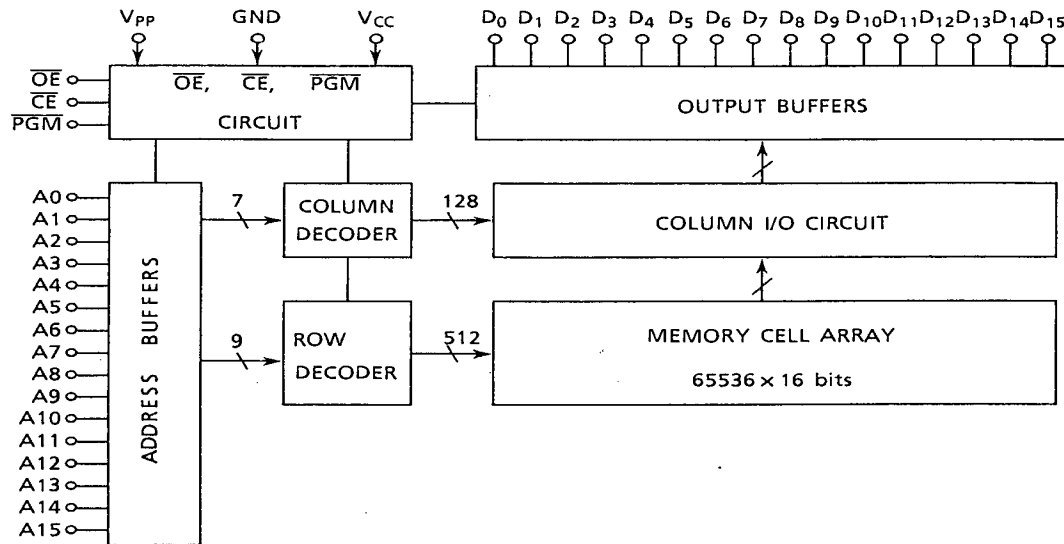
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A15	Address Inputs
D0~D15	Outputs (Inputs)
CE	Chip Enable Input
OE	Output Enable Input
PGM	Program Control Input
Vcc	Vcc Supply Voltage
Vpp	Program Supply Voltage
Vss	Ground
NC	No Connection

BLOCK DIAGRAM



MODE SELECTION

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	D0~D15	Power
Read	L	L	H	5V	5V	Data Out	Active
Output Deselect	*	H	*			High Impedance	
Standby	H	*	*				Standby
Program	L	H	L	12.75V	6.25V	Data In	Active
Program Inhibit	H	*	*			High Impedance	
	L	H	H				
Program Verify	L	L	H			Data Out	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	-0.6~7.0	V
V_{PP}	Program Supply Voltage	-0.6~14.0	V
V_{IN}	Input Voltage	-0.6~7.0	V
$V_{IN}(A9)$	Input Voltage (A9)	-0.6~13.5	V
V_{IO}	Input/Output Voltage	-0.6~ $V_{CC} + 0.5$	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature Time	260 · 10	°C · sec
T_{strg}	Storage Temperature	-65~125	°C
T_{opr}	Operating Temperature	0~70	°C

TC57H1024AD-85, -100

READ OPERATION

AC/DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC57H1024AD-85	TC57H1024AD-100
Ta	Ambient Temperature	0~70°C	
V _{CC}	V _{CC} Power Supply Voltage	5V ± 5%	5V ± 10%
V _{PP}	V _{PP} Power Supply Voltage	0V~V _{CC} + 0.6V	

DC AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Current	V _{IN} = 0~V _{CC}	—	—	± 10	μA
I _{CCO}	Operating Current	CE = 0V I _{OUT} = 0mA	—	—	60	mA
		tcycle = 85ns tcycle = 1μs	—	—	40	mA
I _{CCS1}	Standby Current	CE = V _{IH}	—	—	1	mA
I _{CCS2}		CE = V _{CC} - 0.2V	—	—	100	μA
V _{IH}	Input High Voltage	—	2.2	—	V _{CC} + 0.3	V
V _{IL}	Input Low Voltage	—	- 0.3	—	0.8	V
V _{OH}	Output High Voltage	I _{OH} = - 400μA	2.4	—	—	V
V _{OL}	Output Low Voltage	I _{OL} = 2.1mA	—	—	0.4	V
I _{PP1}	V _{PP} Current	V _{PP} = 0V~V _{CC} + 0.6V	—	—	± 10	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0.4V~V _{CC}	—	—	± 10	μA

AC CHARACTERISTICS (V_{PP}=0V~V_{CC}+0.6V)

SYMBOL	PARAMETER	TC57H1024AD-85		TC57H1024AD-100		UNIT
		MIN.	MAX.	MIN.	MAX.	
t _{ACC}	Address Access Time	—	85	—	100	ns
t _{CE}	CE to Output Valid	—	85	—	100	
t _{OE}	OE to Output Valid	—	45	—	50	
t _{DF1}	CE to Output in High-Z	—	30	—	50	
t _{DF2}	OE to Output in High-Z	—	30	—	50	
t _{OH}	Output Data Hold Time	5	—	10	—	

TC57H1024AD-85 is satisfied with the specification of TC57H1024AD-100

AC TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V and 2.4V
- Timing Measurement Reference Levels: Inputs 0.8V and 2.2V Outputs 0.8V and 2.0V

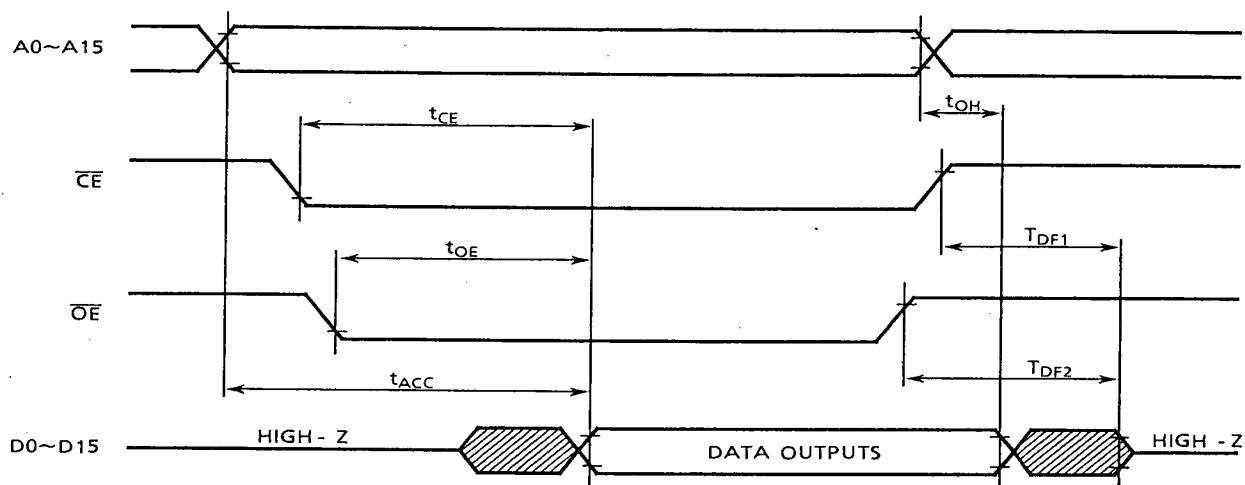
TC57H1024AD-85,-100

CAPACITANCE *(Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = 0V	—	16	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	—	16	

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



TC57H1024AD-85, -100

HIGH SPEED PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage	-0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.50	12.75	13.00	V

DC AND OPERATING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.75\text{V} \pm 0.25\text{V}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	—	—	± 10	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{mA}$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	50	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP} = 13.0\text{V}$	—	—	100	mA

AC PROGRAMMING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.75\text{V} \pm 0.25\text{V}$)

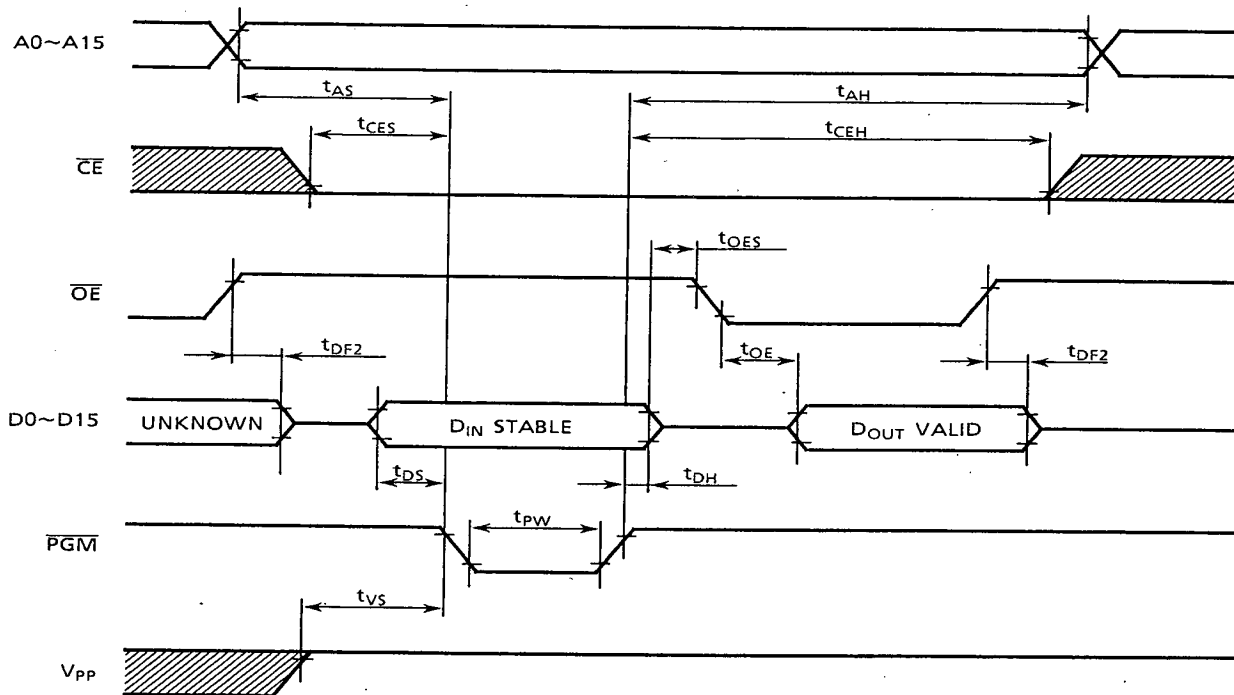
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	2	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VS}	V_{PP} Setup Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	—	0.095	0.1	0.105	ms
t_{OE}	$\overline{OE}$ to Output Valid	—	—	—	500	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE} = V_{IL}$	—	—	150	ns
t_{OES}	$\overline{OE}$ Setup Time	—	2	—	—	μs

AC TEST CONDITIONS

- Output Load : 1 TTL Gate and $CL = 100\text{pF}$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V and 2.4V
- Timing Measurement Reference Levels: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

HIGH SPEED PROGRAM OPERATION

TIMING CHART



- Note :
1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP} .
 2. Removing the device from socket and setting the device in socket with $V_{PP}=12.75V$ may cause permanent damage to the device.
 3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal.
When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

TC57H1024AD-85, -100

ERASURE CHARACTERISTICS

The TC57H1024AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. Then integrated dose (Ultraviolet light intensity [W/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [W·sec./cm²].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [μW/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μW/cm²] × (20 × 60) [sec.] ≈ 15 [W sec./cm²].)

The TC57H1024AD's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the flourescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opeque seals - Toshiba EPROM Protect Seal AC901 - are available.

OPERATION INFORMATION

The TC57H1024AD's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

MODE		PIN	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V _{PP}	V _{CC}	D0~D15	Power
READ OPERATION	Read		L	L	H	5V	5V	Data Out	Active
	Output Deselect		*	H	*			High Impedance	
	Standby		H	*	*				Standby
PROGRAM OPERATION (Ta = 25 ± 5°C)	Program		L	H	L	12.75V	6.25V	Data In	Active
	Program Inhibit		H	*	*			High Impedance	
			L	H	H				
	Program Verify		L	L	H			Data Out	

Note : H ; V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TC57H1024AD has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) controls the output buffers, independent of device selection. Assuming that $\overline{CE} = \overline{OE} = V_{IL}$ and $\overline{PGM} = V_{IH}$, the output data is valid at the output after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$, the outputs will be in a high impedance state. So two or more ROMs can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC57H1024AD has a low power standby mode controlled by the $\overline{CE}$ signal.

By applying a high level to the $\overline{CE}$ input, the TC57H1024AD is placed in the standby mode which reduce the operating current to $100\mu A$ by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC57H1024AD are in the "1" state which is erased state.

Therefore the program operation is to introduce "0s" data into the desired bit locations by electrically programming.

The levels required for all inputs are TTL. The TC57H1024AD can be programmed any location at anytime -- either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.75V) is applied to V_{pp} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TC57H1024AD from being programmed.

Programming of two or more EPROMs in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM OPERATION

The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the V_{pp} terminal with V_{CC}=6.25V and $\overline{PGM}=V_{IH}$.

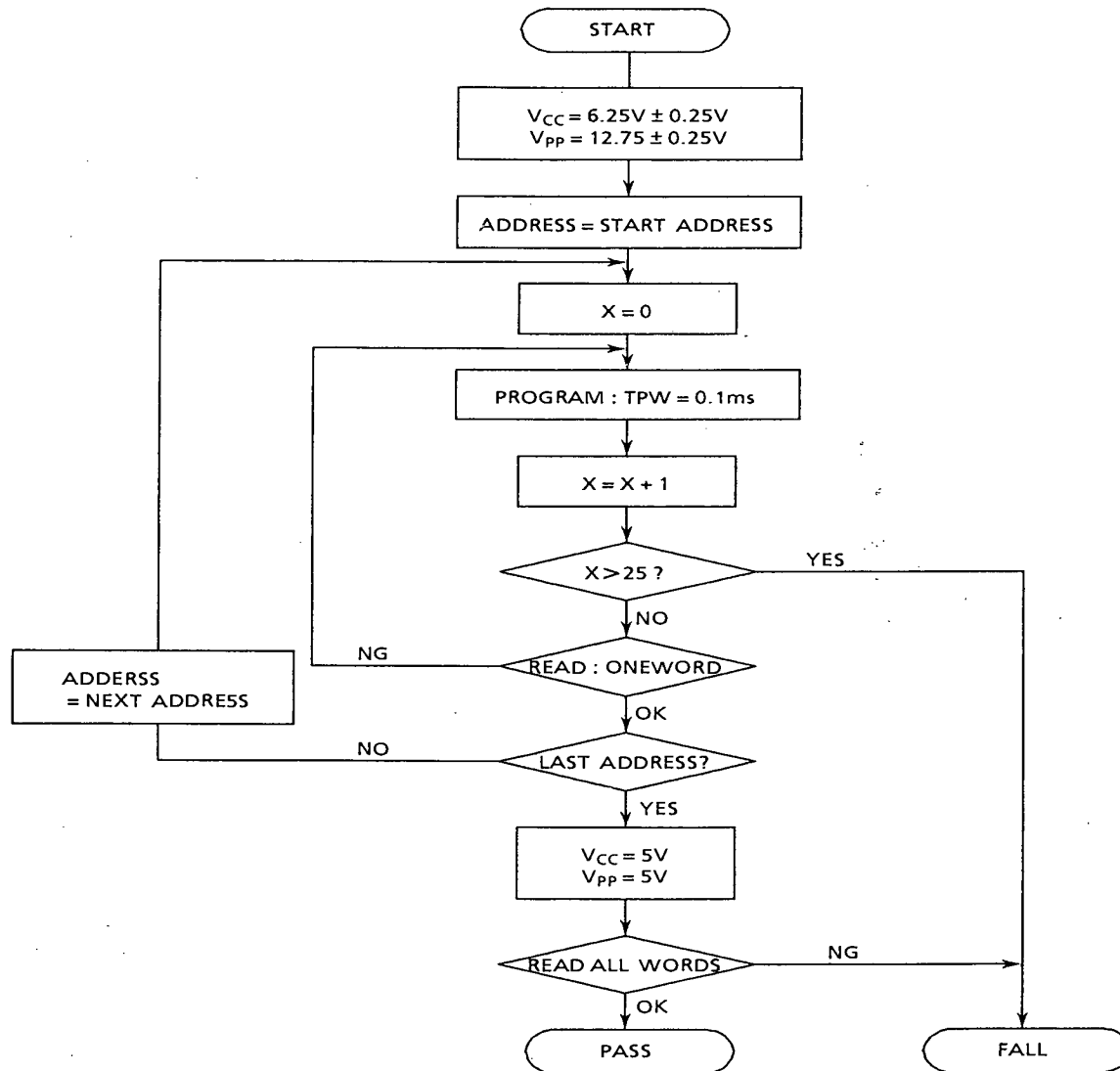
The programming is achieved by applying a single TTL low level 0.1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with V_{CC}=V_{PP}=5V.

HIGH SPEED PROGRAM OPERATION

FLOW CHART



TC57H1024AD-85, -100

ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC57H1024AD which identifies its manufacture and device type.

The programming equipment may read out manufacturer code and device code from TC57H1024AD by using this mode before program operation and automatically set program voltage (V_{pp}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH} .

These two codes possess an odd parity with the parity bit of (D7).

The following table shows electric signature of TC57H1024AD.

SIGNATURE	PINS	A ₀	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	HEX DATA
Manufacturer Code		V_{IL}	*	*	*	*	*	*	*	*	1	0	0	1	1	0	0	0	**98
Device Code		V_{IH}	*	*	*	*	*	*	*	*	1	0	0	0	1	0	0	1	**89

Notes : A9=12V $\pm$ 0.5V, A₁–A₈, A₁₀–A₁₅, $\overline{CE}$, $\overline{OE}$ = V_{IL} , $\overline{PGM}$ = V_{IH}

* : Don't care

SILICON STACKED GATE MOS INTEGRATED CIRCUIT

TC57H1025AD-55

1 MEGA BIT (65,536 WORD×16 BIT) HIGH SPEED CMOS U.V. ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The TC57H1025AD is a 65,536 word × 16 bit high speed CMOS ultraviolet light erasable and electrically programmable read only memory. The TC57H1025AD is JEDEC standard pin configuration. This product is packed in 40 pin standard cerdip package.

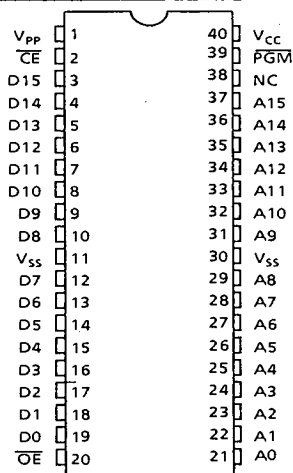
TC57H1025AD is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 60mA/1MHz and access time of 55ns.

The programming times of the TC57H1025AD except overhead times of EPROM programmer is only 7 seconds by using the high speed programming algorithm.

FEATURES

- Peripheral circuit : CMOS
- Memory cell : NMOS
- Fast access time
TC57H1025AD-55 : 55ns
- Low power dissipation
Active : 60mA/1MHz
Standby : 20mA
- Single 5V power supply
- Full static operation
- High speed programming operation : tpw 0.1ms
- Input and output TTL compatible
- JEDEC standard 40 pin
- Standard 40pin DIP cerdip package
: WDIP40-G-600A

PIN CONNECTION (TOP VIEW)

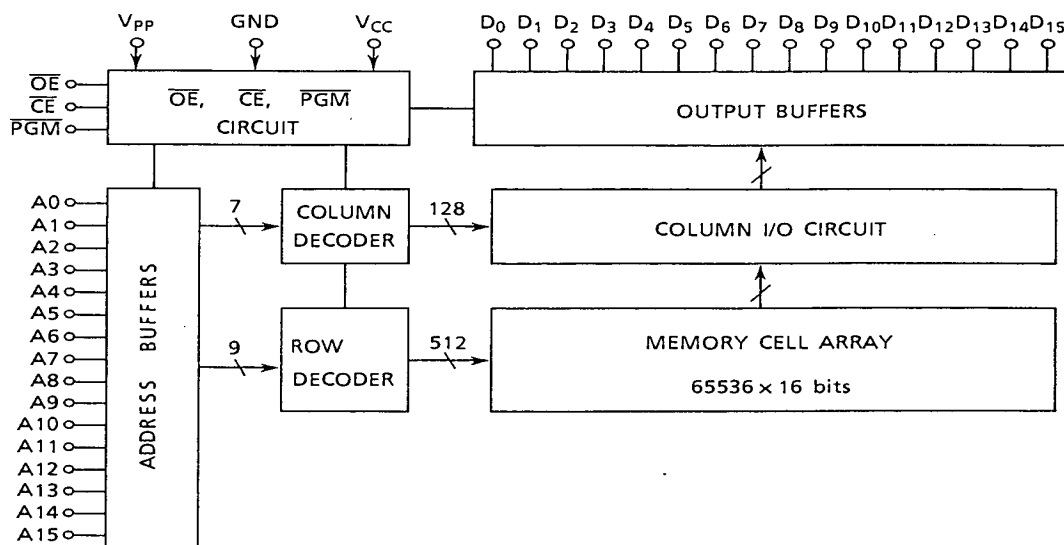


PIN NAMES

A0~A15	Address Inputs
D0~D15	Outputs (Inputs)
CE	Chip Enable Input
OE	Output Enable Input
PGM	Program Control Input
Vcc	Vcc Supply Voltage
Vpp	Program Supply Voltage
Vss	Ground
NC	No Connection

TC57H1025AD-55

BLOCK DIAGRAM



MODE SELECTION

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	D0~D15	Power
Read	L	L	H	5V	5V	Data Out	Active
Output Deselect	*	H	*			High Impedance	
Standby	H	*	*				Standby
Program	L	H	L	12.75V	6.25V	Data In	Active
Program Inhibit	H	*	*			High Impedance	
	L	H	H				
Program Verify	L	L	H			Data Out	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	-0.6~7.0	V
V_{PP}	Program Supply Voltage	-0.6~14.0	V
V_{IN}	Input Voltage	-0.6~7.0	V
$V_{IN}(A_9)$	Input Voltage (A9)	-0.6~13.5	V
$V_{I/O}$	Input/Output Voltage	-0.6~ $V_{CC} + 0.5$	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
T_{strg}	Storage Temperature	-65~125	°C
T_{opr}	Operating Temperature	0~70	°C

READ OPERATION

AC/DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC57H1025AD-55
Ta	Ambient Temperature	0~70°C
V _{CC}	V _{CC} Power Supply Voltage	5V ± 5%
V _{PP}	V _{PP} Power Supply Voltage	0V~V _{CC} + 0.6V

DC AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Current	V _{IN} = 0~V _{CC}	—	—	± 10	μA
I _{CCO}	Operating Current	$\overline{CE} = 0V$ I _{OUT} = 0mA	—	—	90	mA
		tcycle = 55ns	—	—	60	mA
		tcycle = 1μs	—	—	60	mA
I _{CCS1}	Standby Current	$\overline{CE} = V_{IH}$	—	—	20	mA
I _{CCS2}		$\overline{CE} = V_{CC} - 0.2V$	—	—	20	mA
V _{IH}	Input High Voltage	—	2.2	—	V _{CC} + 0.3	V
V _{IL}	Input Low Voltage	—	- 0.3	—	0.8	V
V _{OH}	Output High Voltage	I _{OH} = - 4.0mA	2.4	—	—	V
V _{OL}	Output Low Voltage	I _{OL} = 8.0mA	—	—	0.4	V
I _{PP1}	V _{PP} Current	V _{PP} = 0V~V _{CC} + 0.6V	—	—	± 10	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0.4V~V _{CC}	—	—	± 10	μA

AC CHARACTERISTICS (V_{PP} = 0V~V_{CC} + 0.6V)

SYMBOL	PARAMETER	TC57H1025AD-55		UNIT
		MIN.	MAX.	
t _{ACC}	Address Access Time	—	55	ns
t _{CE}	$\overline{CE}$ to Output Valid	—	55	
t _{OE}	$\overline{OE}$ to Output Valid	—	25	
t _{DF1}	$\overline{CE}$ to Output in High-Z	—	25	
t _{DF2}	$\overline{OE}$ to Output in High-Z	—	25	
t _{OH}	Output Data Hold Time	0	—	

AC TEST CONDITIONS

- Output Load : See Fig.1
- Input Pulse Rise and Fall Times : 5ns Max.
- Input Pulse Levels : 0V to 3V
- Timing Measurement Reference Levels : Inputs 1.5V Outputs 1.5V

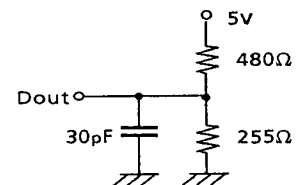


Fig.1 OUTPUT LOAD

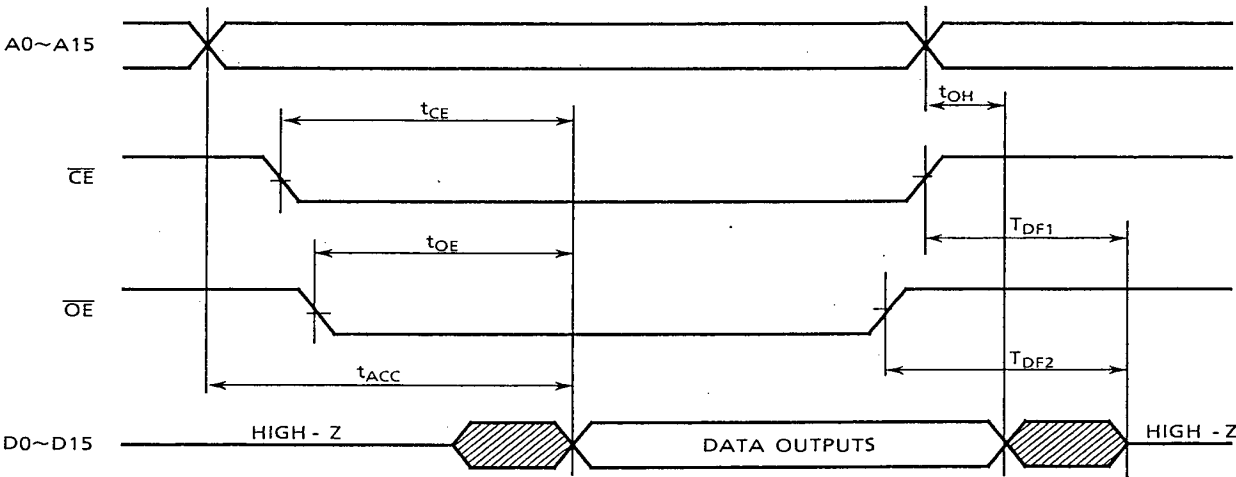
TC57H1025AD-55

CAPACITANCE *(Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = 0V	—	16	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	—	16	

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage	-0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.50	12.75	13.00	V

DC AND OPERATING CHARACTERISTICS($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.75\text{V} \pm 0.25\text{V}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	—	—	± 10	μA
V_{OH}	Output High Voltage	$I_{OH} = -4.0\text{mA}$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 8.0\text{mA}$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	50	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP} = 13.0\text{V}$	—	—	100	mA

AC PROGRAMMING CHARACTERISTICS($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.75\text{V} \pm 0.25\text{V}$)

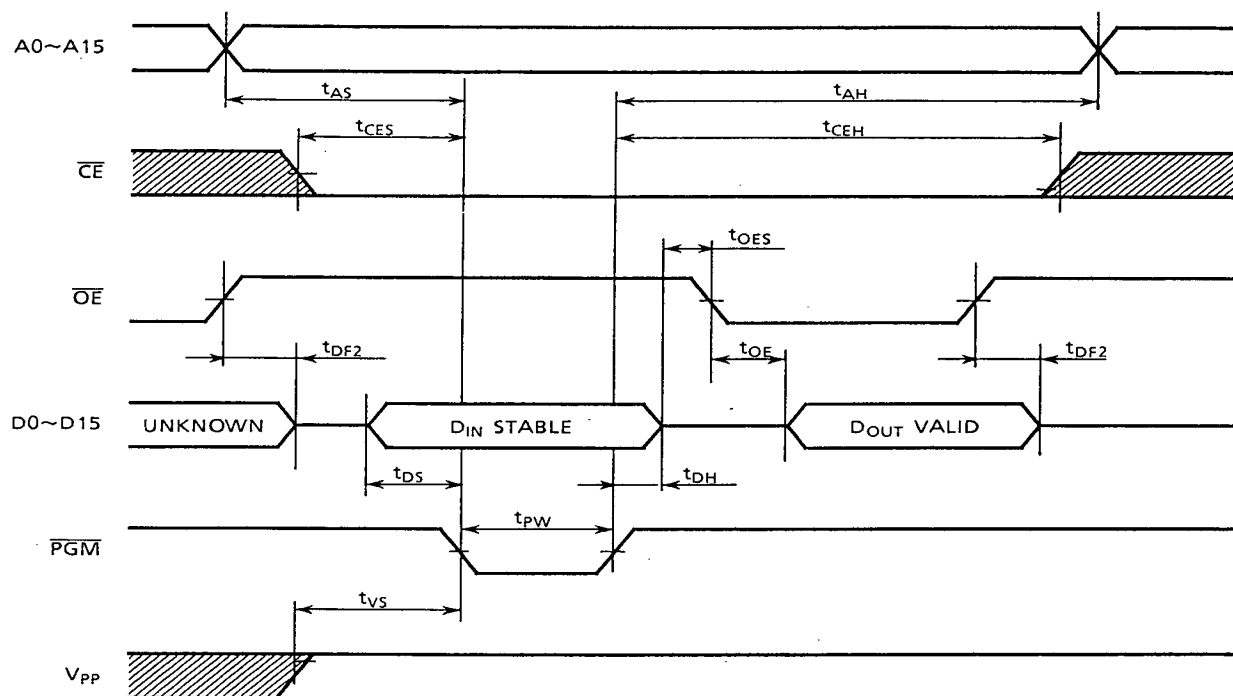
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	2	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VS}	V_{PP} Setup Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	—	0.095	0.1	0.105	ms
t_{OE}	$\overline{OE}$ to Output Valid	—	—	—	500	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE} = V_{IL}$	—	—	150	ns
t_{OES}	$\overline{OE}$ Setup Time	—	2	—	—	μs

AC TEST CONDITION

- Output Load : See Fig.1
- Input Pulse Rise and Fall Times : 5ns Max.
- Input Pulse Levels : 0V to 3V
- Timing Measurement Reference Levels : Inputs 1.5V Outputs 1.5V

HIGH SPEED PROGRAM OPERATION

TIMING CHART



- Note :
1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP} .
 2. Removing the device from socket and setting the device in socket with $V_{PP}=12.75V$ may cause permanent damage to the device.
 3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal.
When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC57H1025AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. Then integrated dose (Ultraviolet light intensity [W/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [W·sec./cm²].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [μW/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μW/cm²] × (20 × 60) [sec.] ≈ 15 [W·sec./cm²].)

The TC57H1025AD's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opeque seals - Toshiba EPROM Protect Seal AC901 - are available.

OPERATION INFORMATION

The TC57H1025AD's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

MODE		PIN	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	D0~D15	Power
READ OPERATION (Ta = 0~70°C)	Read		L	L	H	5V	5V	Data Out	Active
	Output Deselect		*	H	*			High Impedance	
	Standby		H	*	*				Standby
PROGRAM OPERATION (Ta = 25 ± 5°C)	Program		L	H	L	12.75V	6.25V	Data In	Active
	Program Inhibit		H	*	*			High Impedance	
			L	H	H				
	Program Verify		L	L	H			Data Out	

Note : H ; V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

TC57H1025AD-55

READ MODE

The TC57H1025AD has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) controls the output buffers, independent of device selection. Assuming that $\overline{CE} = \overline{OE} = V_{IL}$ and $\overline{PGM} = V_{IH}$, the output data is valid at the output after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$, the outputs will be in a high impedance state. So two or more ROMs can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC57H1025AD has a low power standby mode controlled by the $\overline{CE}$ signal.

By applying a high level to the $\overline{CE}$ input, the TC57H1025AD is placed in the standby mode which reduce the operating current to 10mA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC57H1025AD are in the "1" state which is erased state.

Therefore the program operation is to introduce "0s" data into the desired bit locations by electrically programming.

The levels required for all inputs are TTL. The TC57H1025AD can be programmed any location at anytime -- either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.75V) is applied to V_{pp} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TC57H1025AD from being programmed.

Programming of two or more EPROMs in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM OPERATION

The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the V_{pp} terminal with V_{CC}=6.25V and $\overline{PGM}=V_{IH}$.

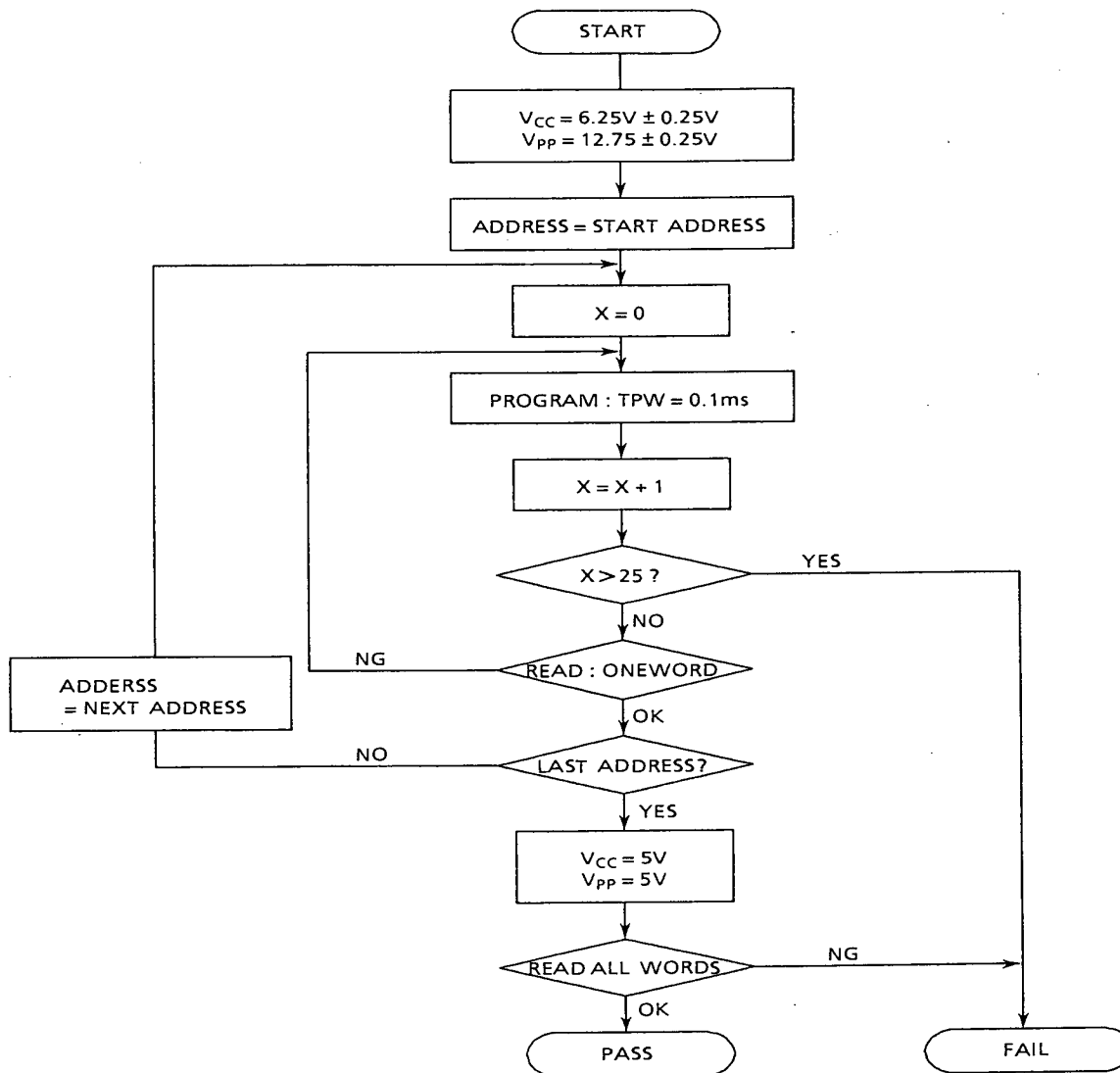
The programming is achieved by applying a single TTL low level 0.1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with V_{CC}=V_{pp}=5V.

HIGH SPEED PROGRAM OPERATION

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC57H1025AD which identifies it's manufacture and device type.

The programming equipment may read out manufacturer code and device code from TC57H1025AD by using this mode before program operation and automatically set program voltage (Vpp) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}.

These two codes possess an odd parity with the parity bit of (D7).

The following table shows electric signature of TC57H1025AD.

SIGNATURE	PINS	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX DATA
Manufacturer Code	V _{IL}	*	*	*	*	*	*	*	*	*	1	0	0	1	1	0	0	0	**98
Device Code	V _{IH}	*	*	*	*	*	*	*	*	*	1	0	0	0	1	0	0	1	**89

Note: A9=12V±0.5V, A1-A8, A10-A15, $\overline{CE}$, $\overline{OE}$ =V_{IL}, $\overline{PGM}$ =V_{IH}

*: Don't care

TC57H1025AD-70

1 MEGA BIT (65,536 WORD $\times$ 16 BIT) HIGH SPEED CMOS U.V. ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The TC57H1025AD is a 65,536 word $\times$ 16 bit high speed CMOS ultraviolet light erasable and electrically programmable read only memory. The TC57H1025AD is JEDEC standard pin configuration. This product is packed in 40 pin standard cerdip package.

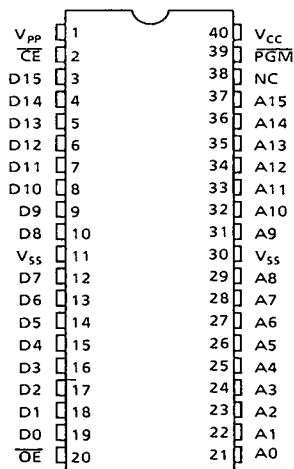
TC57H1025AD is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 60mA/1MHz and access time of 55ns.

The programming times of the TC57H1025AD except overhead times of EPROM programmer is only 7 seconds by using the high speed programming algorithm.

FEATURES

- Peripheral circuit : CMOS
- Memory cell : NMOS
- Fast access time
TC57H1025AD-70 : 70ns
- Low power dissipation
Active : 60mA/1MHz
Standby : 20mA
- Single 5V power supply
- Full static operation
- High speed programming operation : tpw 0.1ms
- Input and output TTL compatible
- JEDEC standard 40 pin
- Standard 40pin DIP cerdip package
: WDIP40-G-600A

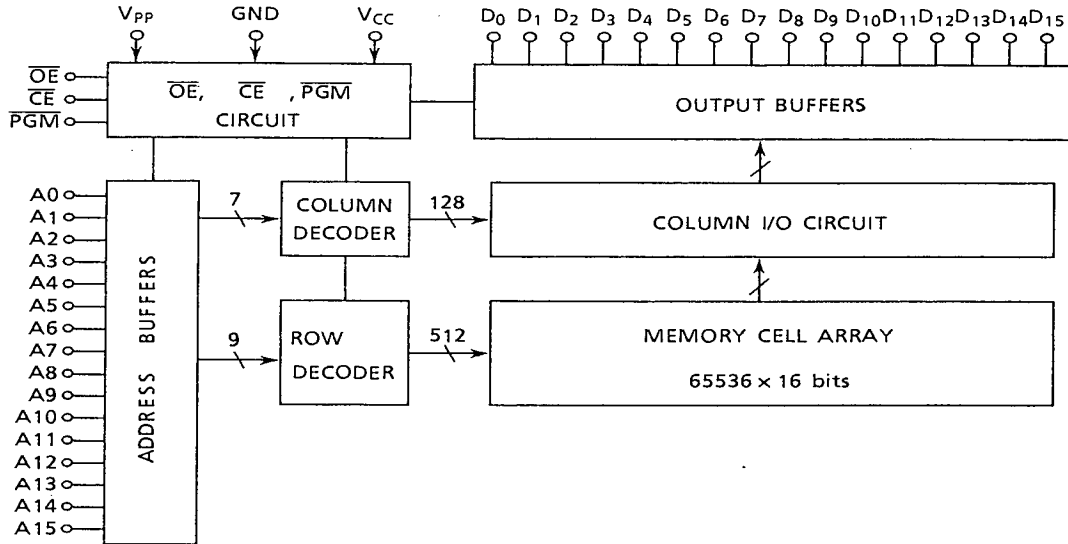
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A15	Address Inputs
D0~D15	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
PGM	Program Control Input
Vcc	Vcc Supply Voltage
Vpp	Program Supply Voltage
Vss	Ground
NC	No Connection

BLOCK DIAGRAM



MODE SELECTION

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	D0~D15	Power
Read	L	L	H	5V	5V	Data Out	Active
Output Deselect	*	H	*			High Impedance	
Standby	H	*	*				Standby
Program	L	H	L	12.75V	6.25V	Data In	Active
Program Inhibit	H	*	*			High Impedance	
	L	H	H				
Program Verify	L	L	H			Data Out	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	-0.6~7.0	V
V_{PP}	Program Supply Voltage	-0.6~14.0	V
V_{IN}	Input Voltage	-0.6~7.0	V
$V_{IN}(A9)$	Input Voltage (A9)	-0.6~13.5	V
V_{IO}	Input/Output Voltage	-0.6~ $V_{CC} + 0.5$	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
T_{strg}	Storage Temperature	-65~125	°C
T_{opr}	Operating Temperature	0~70	°C

TC57H1025AD-70

READ OPERATION

AC/DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC57H1025AD-70
Ta	Ambient Temperature	0~70°C
V _{CC}	V _{CC} Power Supply Voltage	5V ± 5%
V _{PP}	V _{PP} Power Supply Voltage	0V~V _{CC} + 0.6V

DC AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Current	V _{IN} = 0~V _{CC}	—	—	± 10	μA
I _{CCO}	Operating Current	$\overline{CE} = 0V$ I _{OUT} = 0mA	—	—	90	mA
		tcycle = 70ns	—	—	60	mA
		tcycle = 1μs	—	—	60	mA
I _{CCS1}	Standby Current	$\overline{CE} = V_{IH}$	—	—	20	mA
I _{CCS2}		$\overline{CE} = V_{CC} - 0.2V$	—	—	20	mA
V _{IH}	Input High Voltage	—	2.2	—	V _{CC} + 0.3	V
V _{IL}	Input Low Voltage	—	- 0.3	—	0.8	V
V _{OH}	Output High Voltage	I _{OH} = - 4.0mA	2.4	—	—	V
V _{OL}	Output Low Voltage	I _{OL} = 8.0mA	—	—	0.4	V
I _{PP1}	V _{PP} Current	V _{PP} = 0V~V _{CC} + 0.6V	—	—	± 10	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0.4V~V _{CC}	—	—	± 10	μA

AC CHARACTERISTICS (V_{PP} = 0V~V_{CC} + 0.6V)

SYMBOL	PARAMETER	TC57H1025AD-70		UNIT
		MIN.	MAX.	
t _{ACC}	Address Access Time	—	70	ns
t _{CE}	$\overline{CE}$ to Output Valid	—	70	
t _{OE}	$\overline{OE}$ to Output Valid	—	40	
t _{DF1}	$\overline{CE}$ to Output in High-Z	—	30	
t _{DF2}	$\overline{OE}$ to Output in High-Z	—	30	
t _{OH}	Output Data Hold Time	5	—	

AC TEST CONDITIONS

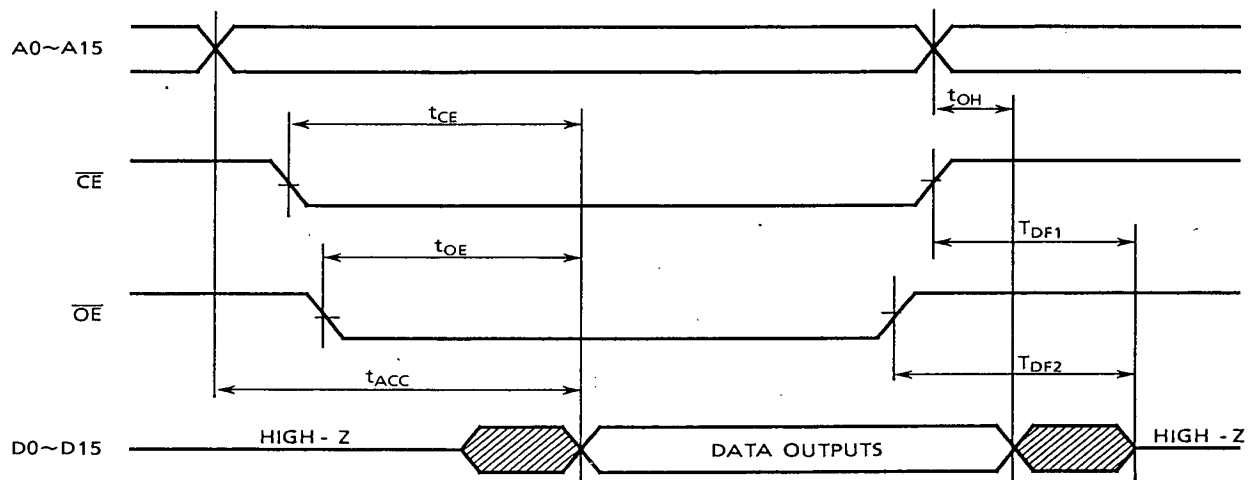
- Output Load : 1 TTL Gate and CL = 100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Levels : Inputs 0.8V Outputs 2.2V
: Outputs 0.8V Outputs 2.0V

CAPACITANCE *(Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = 0V	—	16	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	—	16	

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



TC57H1025AD-70

HIGH SPEED PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage	-0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.50	12.75	13.00	V

DC AND OPERATING CHARACTERISTICS($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.75\text{V} \pm 0.25\text{V}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	—	—	± 10	μA
V_{OH}	Output High Voltage	$I_{OH} = -4.0\text{mA}$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 8.0\text{mA}$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	50	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP} = 13.0\text{V}$	—	—	100	mA

AC PROGRAMMING CHARACTERISTICS($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.75\text{V} \pm 0.25\text{V}$)

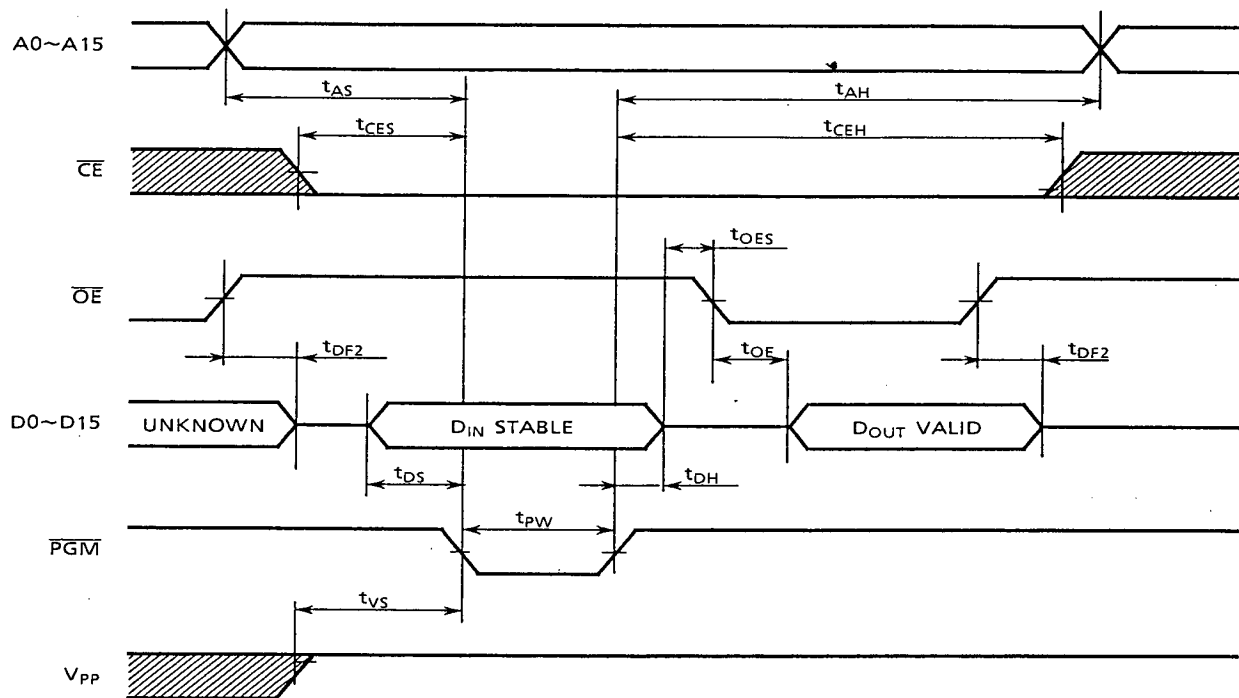
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	2	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VS}	V_{PP} Setup Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	—	0.095	0.1	0.105	ms
t_{OE}	$\overline{OE}$ to Output Valid	—	—	—	500	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE} = V_{IL}$	—	—	150	ns
t_{OES}	$\overline{OE}$ Setup Time	—	2	—	—	μs

AC TEST CONDITION

- Output Load : 1 TTL Gate and $C_L = 100\text{pF}$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V and 2.4V
- Timing Measurement Reference Levels : Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

HIGH SPEED PROGRAM OPERATION

TIMING CHART



- Note :
1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP} .
 2. Removing the device from socket and setting the device in socket with $V_{PP}=12.75V$ may cause permanent damage to the device.
 3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal.
When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

TC57H1025AD-70

ERASURE CHARACTERISTICS

The TC57H1025AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. Then integrated dose (Ultraviolet light intensity [W/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [W·sec./cm²].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [μW/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μW/cm²] × (20 × 60) [sec] ≈ 15 [W·sec./cm²].)

The TC57H1025AD's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the flourescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opeque seals - Toshiba EPROM Protect Seal AC901 - are available.

OPERATION INFORMATION

The TC57H1025AD's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

MODE		PIN	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	D0~D15	Power
READ OPERATION (Ta = 0~70°C)	Read		L	L	H	5V	5V	Data Out	Active
	Output Deselect		*	H	*			High Impedance	
	Standby		H	*	*				Standby
PROGRAM OPERATION (Ta = 25 ± 5°C)	Program		L	H	L	12.75V	6.25V	Data In	Active
	Program Inhibit		H	*	*			High Impedance	
			L	H	H				
	Program Verify		L	L	H			Data Out	

Note : H : V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TC57H1025AD has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) controls the output buffers, independent of device selection. Assuming that $\overline{CE} = \overline{OE} = V_{IL}$ and $\overline{PGM} = V_{IH}$, the output data is valid at the output after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$, the outputs will be in a high impedance state. So two or more ROMs can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC57H1025AD has a low power standby mode controlled by the $\overline{CE}$ signal.

By applying a high level to the $\overline{CE}$ input, the TC57H1025AD is placed in the standby mode which reduce the operating current to 10mA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC57H1025AD are in the "1" state which is erased state.

Therefore the program operation is to introduce "0s" data into the desired bit locations by electrically programming.

The levels required for all inputs are TTL. The TC57H1025AD can be programmed any location at anytime -- either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.75V) is applied to Vpp terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TC57H1025AD from being programmed.

Programming of two or more EPROMs in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM OPERATION

The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the Vpp terminal with $V_{CC}=6.25V$ and $\overline{PGM}=V_{IH}$.

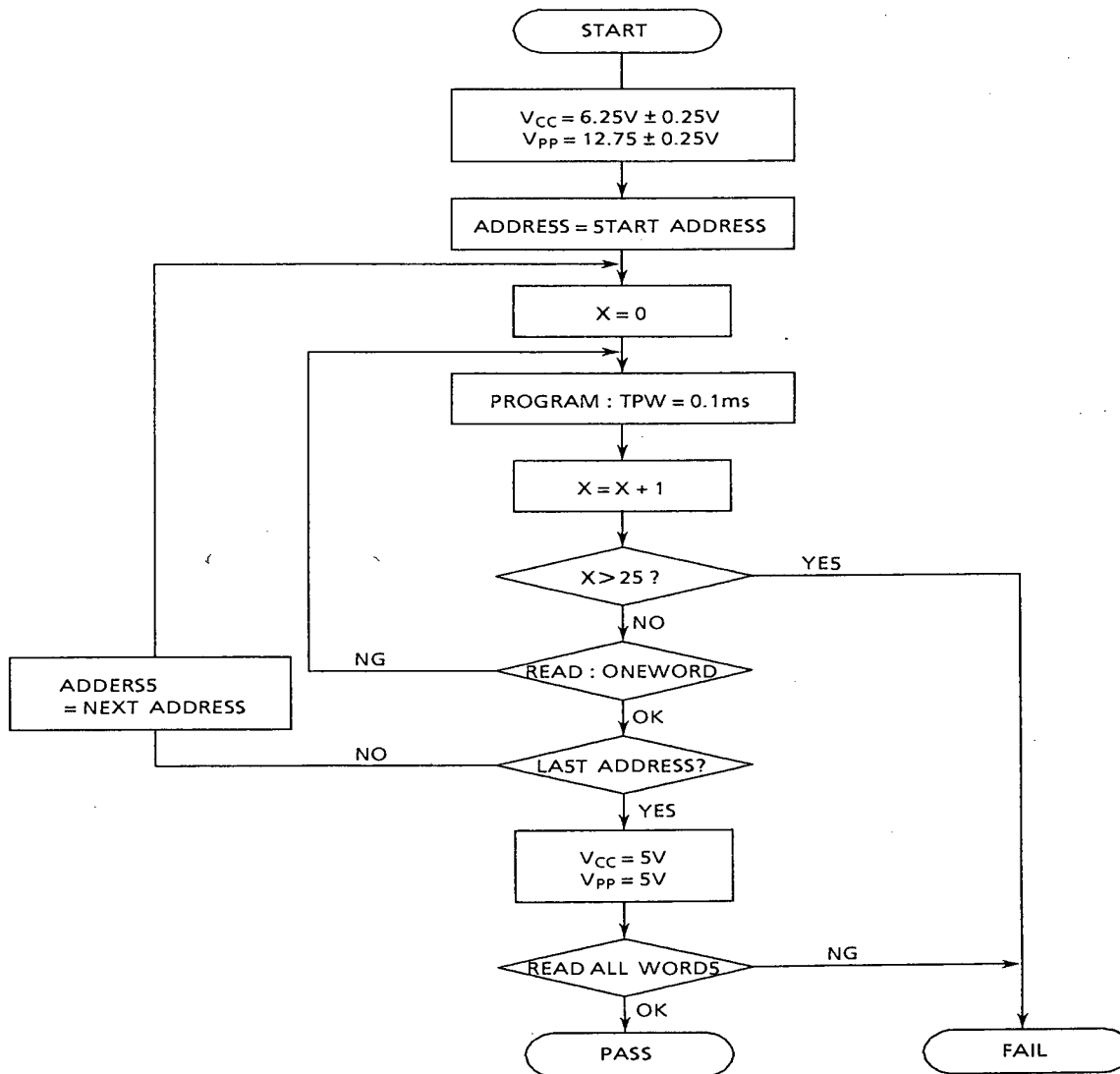
The programming is achieved by applying a single TTL low level 0.1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM OPERATION

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC57H1025AD which identifies it's manufacture and device type.

The programming equipment may read out manufacturer code and device code from TC57H1025AD by using this mode before program operation and automatically set program voltage (Vpp) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to VIL in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to VIH.

These two codes possess an odd parity with the parity bit of (D7).

The following table shows electric signature of TC57H1025AD.

SIGNATURE	PINS	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX DATA
Manufacturer Code		VIL	*	*	*	*	*	*	*	*	1	0	0	1	1	0	0	0	**98
Device Code		VIH	*	*	*	*	*	*	*	*	1	0	0	0	1	0	0	1	**89

Note: A9=12V±0.5V, A1-A8, A10-A15, CE, OE=VIL, PGM=VIH

*: Don't care

SILICON STACKED GATE MOS INTEGRATED CIRCUIT

TC574000D-120,-150

524,288 WORD $\times$ 8 BIT CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The TC574000D is a 524,288 word $\times$ 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory. For read operation, the TC574000D's access time is 120ns, and the TC574000D operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time.

The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input.

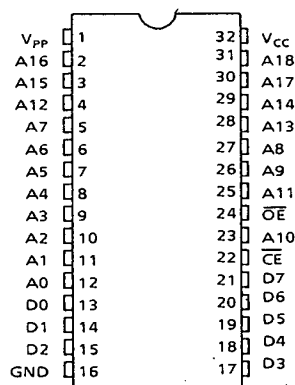
Advanced CMOS technology reduces the maximum active current to 60mA / 8.3MHz and standby current to 100 μ A. For program operation, the programming is achieved by using the high speed programming mode. TC574000D is fabricated with the CMOS technology and the N-channel silicon double layer gate MOS technology.

FEATURES

- Peripheral circuit : CMOS
- Memory cell : N-MOS
- Access time
- Low power dissipation
 - Active : 60mA / 8.3MHz
 - Standby: 100 μ A ($T_a = 70^\circ\text{C}$)
- High speed programming operation
- Single 5V power supply
- Full static operation
- Input and output TTL compatible
- JEDEC standard 32 pin
- Standard 32 pin DIP cerdip package : WDIP32-G-600A

	- 120	- 150
V_{CC}	$5V \pm 10\%$	
Temp	$0 \sim 70^\circ\text{C}$	
t_{ACC}	120ns	150ns

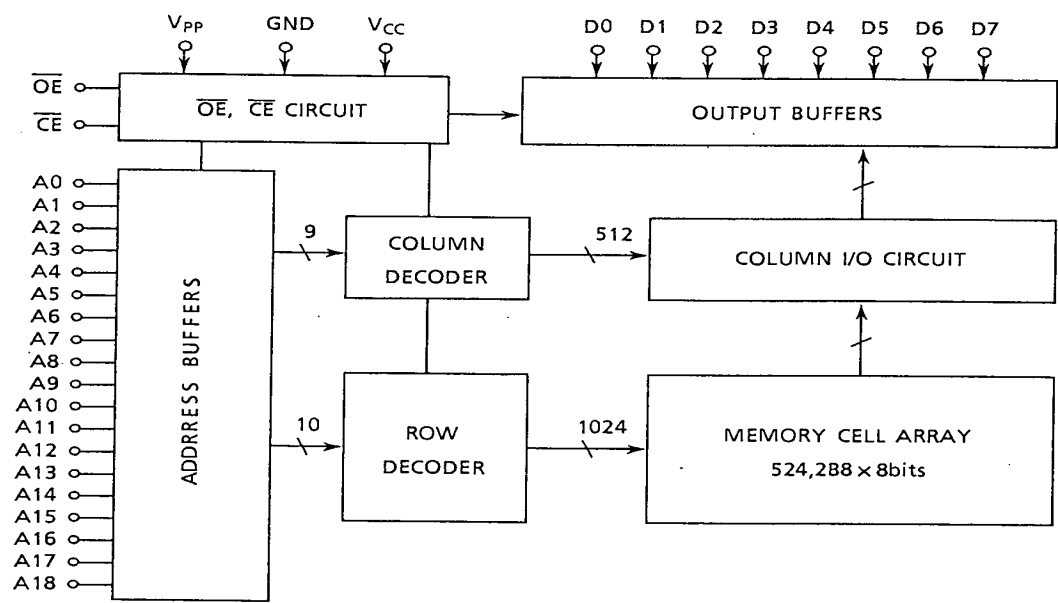
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A18	Address Inputs
D0~D7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{CC}	V_{CC} Supply Voltage
V_{PP}	Program Supply Voltage
GND	Ground

BLOCK DIAGRAM



MODE SELECTION

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	D0~D7	Power
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*			High Impedance	Standby
Program	L	H	12.50V	6.25V	Data In	Active
Program Inhibit	H	H			High Impedance	
Program Verify	*	L			Data Out	

* : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	- 0.6~7.0	V
V_{PP}	Program Supply Voltage	- 0.6~14.0	V
V_{IN}	Input Voltage	- 0.6~7.0	V
$V_{IN}(A9)$	Input Voltage (A9)	- 0.6~13.5	V
V_{IO}	Input/Output Voltage	- 0.6~ $V_{CC} + 0.5$	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
T_{strg}	Storage Temperature	- 65~125	°C
T_{opr}	Operating Temperature	0~70	°C

READ OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage	-0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.50	5.00	5.50	V
V_{PP}	V_{PP} Power Supply Voltage	$V_{CC} - 0.6$	V_{CC}	$V_{CC} + 0.6$	V

DC AND OPERATING CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$)

SIMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	—	—	± 10	μA
I_{CCO1}	Operating Current	$\overline{CE} = V_{IL}$ $I_{OUT} = 0\text{mA}$	—	—	60	mA
					50	
I_{CCO2}					15	
I_{CCS1}	Standby Current	$\overline{CE} = V_{IH}$	—	—	1	mA
I_{CCS2}		$\overline{CE} = V_{CC} - 0.2\text{V}$	—	—	100	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{mA}$	—	—	0.4	V
I_{PP1}	V_{PP} Current	$V_{PP} = V_{CC} \pm 0.6\text{V}$	—	—	± 10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 0.4\text{V} \sim V_{CC}$	—	—	± 10	μA

AC CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{PP} = V_{CC} \pm 0.6\text{V}$)

SIMBOL	PARAMETER	TEST CONDITION	TC574000D - 120		TC574000D - 150		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE} = \overline{OE} = V_{IL}$	—	120	—	150	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE} = V_{IL}$	—	120	—	150	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE} = V_{IL}$	—	60	—	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE} = V_{IL}$	0	50	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE} = V_{IL}$	0	50	0	60	ns
t_{OH}	Output Data Hold Time	$\overline{CE} = \overline{OE} = V_{IL}$	0	—	0	—	ns

AC TEST CONDITIONS

- Output Load : 1 TTL Gate and $C_L = 100\text{pF}$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V~2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

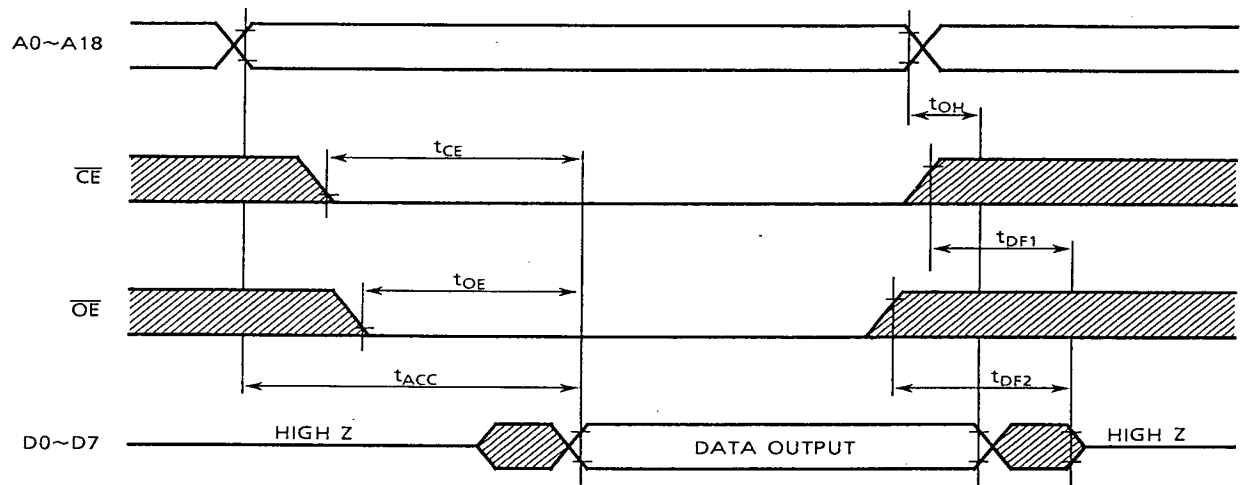
TC574000D-120, -150

CAPACITANCE* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = 0V	—	9	PF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	—	13	

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	$V_{CC} + 1.0$	V
V_{IL}	Input Low Voltage	-0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.20	12.50	12.80	V

DC AND OPREATING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.50\text{V} \pm 0.30\text{V}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	—	—	± 10	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{mA}$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	30	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP} = 12.8\text{V}$	—	—	50	mA

AC PROGRAMMING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.50\text{V} \pm 0.30\text{V}$)

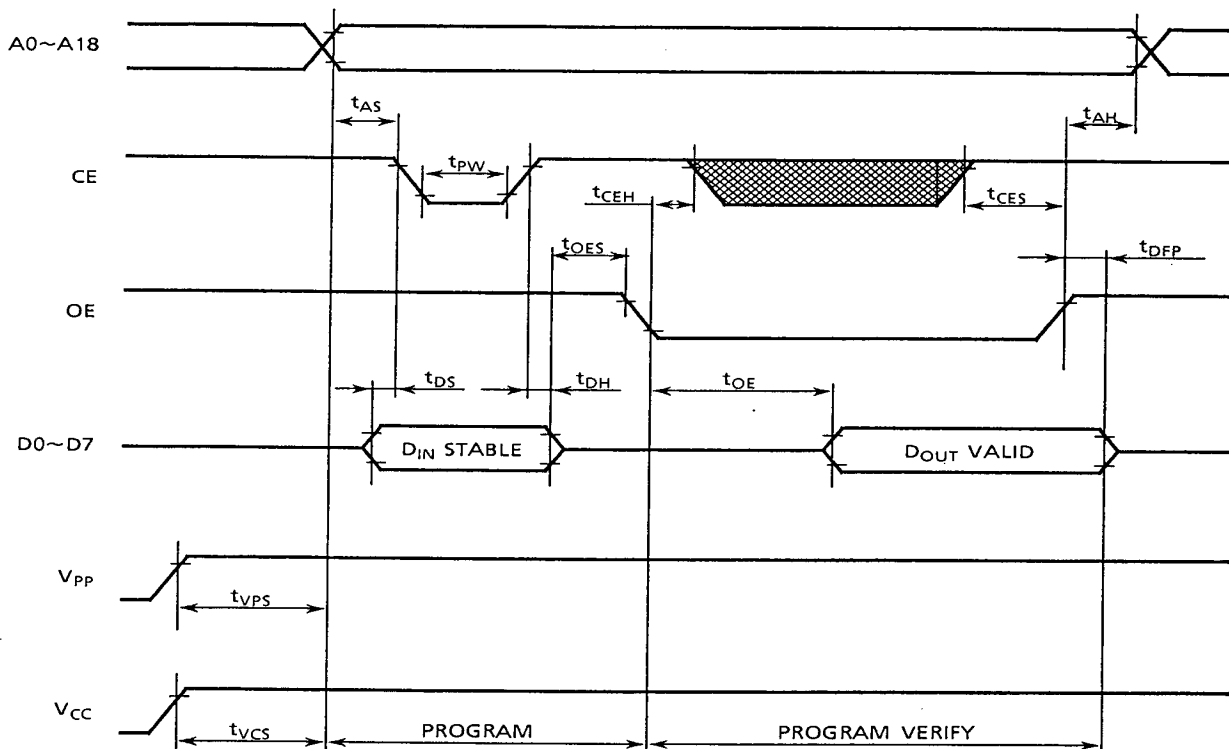
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	0	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	0	—	—	μs
t_{OES}	$\overline{OE}$ Set up Time	—	2	—	—	μs
t_{DS}	Data Set up Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VPS}	V_{PP} Set up Time	—	2	—	—	μs
t_{VCS}	V_{CC} Set up Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	45	50	55	μs
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE} = V_{IH}$	—	—	100	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE} = V_{IH}$	—	—	90	ns

AC TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V~2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAM OPERATION



- Note 1. V_{CC} must be applied simultaneously or before V_{pp} and cut off simultaneously or after V_{pp}.
2. Removing the device from socket and setting the device in socket with V_{PP}=12.50V may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC574000D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window.

Then integrated dose (ultraviolet light intensity [w/cm²]×exposure time [sec.]) for erasure should be a minimum of 15 [w·sec/cm²].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is a 12000 [μw/cm²] will reduce the exposure time to about 20 minutes. (In this case, the intergrated dose is 12000[μw/cm²]×(20×60) [sec.] ≈15 [w·sec/cm²].)

The TC574000D's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC902-are available.

OPERATION INFORMATION

The TC574000D's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

MODE		PIN NAMES (NUMBER)	$\overline{CE}$ (22)	$\overline{OE}$ (24)	V_{PP} (1)	V_{CC} (32)	D0~D7 (13~15, 17~21)	POWER
Read Operation (Ta=0~70°C)	Read		L	L	5V	5V	Data Out	Active
	Output Deselet		*	H			High Impedance	
	Standby		H	*			High Impedance	Standby
Program Operation (Ta=25±5°C)	Program		L	H	12.50V	6.25V	Data In	Active
	Program Inhibit		H	H			High Impedance	
	Program Verify		*	L			Data Out	

Note : H ; V_{IH} , L : V_{IL} , * : V_{IH} or V_{IL}

READ MODE

The TC574000D has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection. The output enable ($\overline{OE}$) controls the output buffers, independent of device selection. Assuming that $\overline{CE}=\overline{OE}=V_{IL}$, the output data is valid at the outputs after address access time from stabilizing of all addresses. The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

TC574000D-120, -150

OUTPUT DESELECT MODE

Assuming that $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$, the outputs will be in a high impedance state. So two or more TC574000D's can be connected together on a common bus line. When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC574000D has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC574000D is placed in the standby mode which reduce the operating current to $100\mu A$ by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC574000D are in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming. The TC574000D is in the programming mode when the V_{pp} input is at 12.50V and $\overline{CE}$ is at Low under $\overline{OE} = V_{IH}$.

The TC574000D can be programmed any location at any time either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with $\overline{OE}$ at V_{IL} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.50V) is applied to V_{pp} terminal, a high level $\overline{CE}$ and $\overline{OE}$ input inhibits the TC574000D from being programmed.

Programming of two or more TC574000D's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a low level program pulse is applied to the $\overline{CE}$ of the desired device only and high level signal is applied to the other devices.

HIGH SPEED PROGRAM MODE

The device is set up in the high speed programming mode when the programming voltage (+12.50V) is applied to the V_{PP} terminal with $V_{CC}=6.25V$.

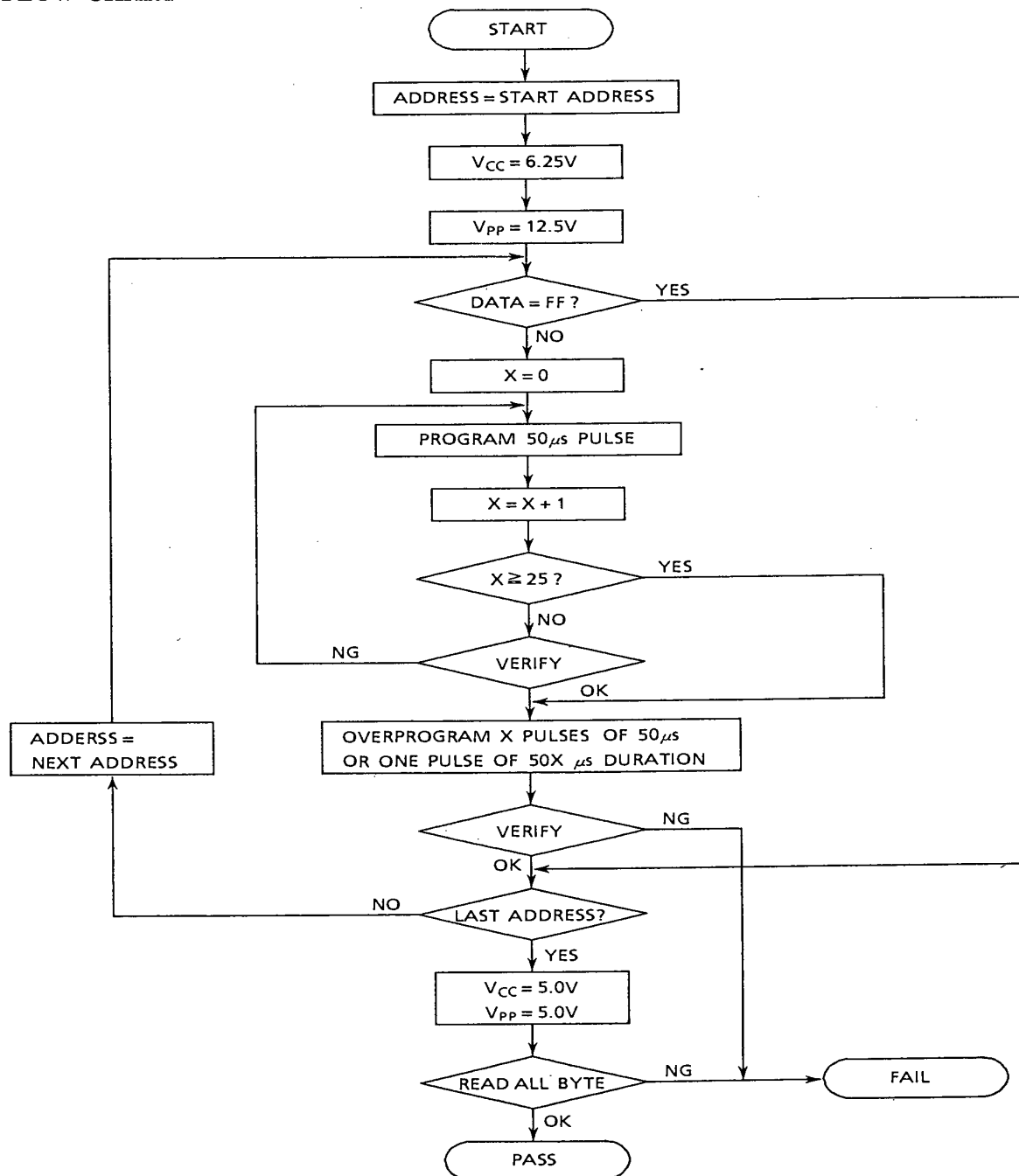
The programming is achieved by applying a single low level $50\mu s$ pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of $50\mu s$ is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with width of 1 time more than that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM MODE

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC574000D which identifies its manufacturer and device type.

The programming equipment may reads out manufacturer code and device code from TC574000D by using this mode before program operation and automatically set program voltage (V_{pp}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH} .

These two codes possess an odd parity with the parity bit of MSB (D7).

The following table shows electric signature of TC574000D.

SIGNATURE \ PINS	A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	0	0	0	1	1	0	0	8C

Notes : A9=12V±0.5V

A1~A8, A0~A18, $\overline{CE}$, $\overline{OE}$ = V_{IL}

TC574000AD-120, -150

524,288 WORD $\times$ 8 BIT CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The TC574000AD is a 524,288 word $\times$ 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory. For read operation, the TC574000AD's access time is 120ns, and the TC574000AD operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time.

The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input.

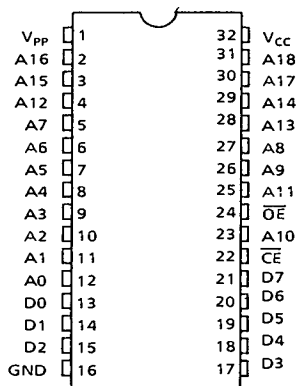
Advanced CMOS technology reduces the maximum active current to 60mA / 8.3MHz and standby current to 100 μ A. For program operation, the programming is achieved by using the high speed programming mode. TC574000AD is fabricated with the CMOS technology and the N-channel silicon double layer gate MOS technology.

FEATURES

- Peripheral circuit : CMOS
- Memory cell : N-MOS
- Access time
- Low power dissipation
 - Active : 60mA / 8.3MHz
 - Standby: 100 μ A ($T_a = 70^\circ\text{C}$)
- High speed programming operation
- Single 5V power supply
- Full static operation
- Input and output TTL compatible
- JEDEC standard 32 pin
- Standard 32 pin DIP cerdip package : WDIP32-G-600B

	- 120	- 150
V_{CC}	5V $\pm$ 10%	
Temp	0~70°C	
t_{ACC}	120ns	150ns

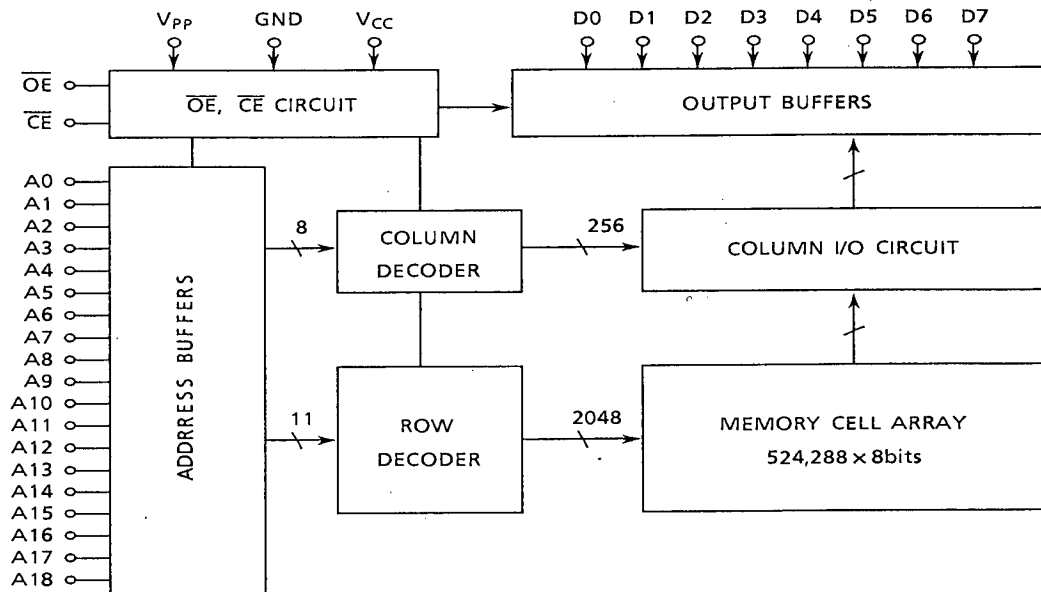
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A18	Address Inputs
D0~D7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{CC}	V_{CC} Supply Voltage
V_{PP}	Program Supply Voltage
GND	Ground

BLOCK DIAGRAM



MODE SELECTION

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	D0~D7	Power
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*			High Impedance	Standby
Program	L	H	12.50V	6.25V	Data In	Active
Program Inhibit	H	H			High Impedance	
Program Verify	*	L			Data Out	

* : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	-0.6~7.0	V
V_{PP}	Program Supply Voltage	-0.6~14.0	V
V_{IN}	Input Voltage	-0.6~7.0	V
$V_{IN}(A9)$	Input Voltage (A9)	-0.6~13.5	V
$V_{I/O}$	Input/Output Voltage	-0.6~ $V_{CC} + 0.5$	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
T_{strg}	Storage Temperature	-65~125	°C
T_{opr}	Operating Temperature	0~70	°C

TC574000AD-120, -150

READ OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage	-0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.50	5.00	5.50	V
V_{PP}	V_{PP} Power Supply Voltage	$V_{CC} - 0.6$	V_{CC}	$V_{CC} + 0.6$	V

DC AND OPERATING CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$)

SIMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	—	—	± 10	μA
I_{CCO1}	Operating Current	$\overline{CE} = V_{IL}$ $I_{OUT} = 0\text{mA}$	—	—	60	mA
					50	
I_{CCO2}					30	
I_{CCS1}	Standby Current	$\overline{CE} = V_{IH}$	—	—	1	mA
I_{CCS2}		$\overline{CE} = V_{CC} - 0.2\text{V}$	—	—	100	
V_{OH}	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{mA}$	—	—	0.4	V
I_{PP1}	V_{PP} Current	$V_{PP} = V_{CC} \pm 0.6\text{V}$	—	—	± 10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 0.4\text{V} \sim V_{CC}$	—	—	± 10	μA

AC CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{PP} = V_{CC} \pm 0.6\text{V}$)

SIMBOL	PARAMETER	TEST CONDITION	TC574000AD - 120		TC574000AD - 150		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE} = \overline{OE} = V_{IL}$	—	120	—	150	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE} = V_{IL}$	—	120	—	150	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE} = V_{IL}$	—	60	—	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE} = V_{IL}$	0	50	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE} = V_{IL}$	0	50	0	60	ns
t_{OH}	Output Data Hold Time	$\overline{CE} = \overline{OE} = V_{IL}$	0	—	0	—	ns

AC TEST CONDITIONS

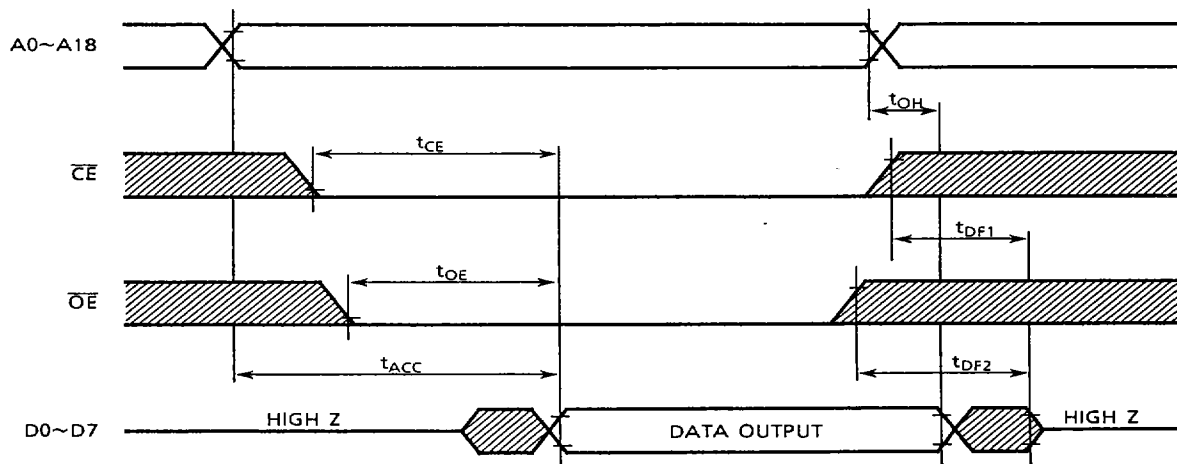
- Output Load : 1 TTL Gate and $C_L = 100\text{pF}$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ~ 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE* ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$	—	12	PF
C_{OUT}	Output Capacitance	$V_{OUT} = 0\text{V}$	—	15	

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



TC574000AD-120, -150

HIGH SPEED PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	$V_{CC} + 1.0$	V
V_{IL}	Input Low Voltage	-0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.20	12.50	12.80	V

DC AND OPERATING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.50\text{V} \pm 0.30\text{V}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	—	—	± 10	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{mA}$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	30	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP} = 12.8\text{V}$	—	—	50	mA

AC PROGRAMMING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.50\text{V} \pm 0.30\text{V}$)

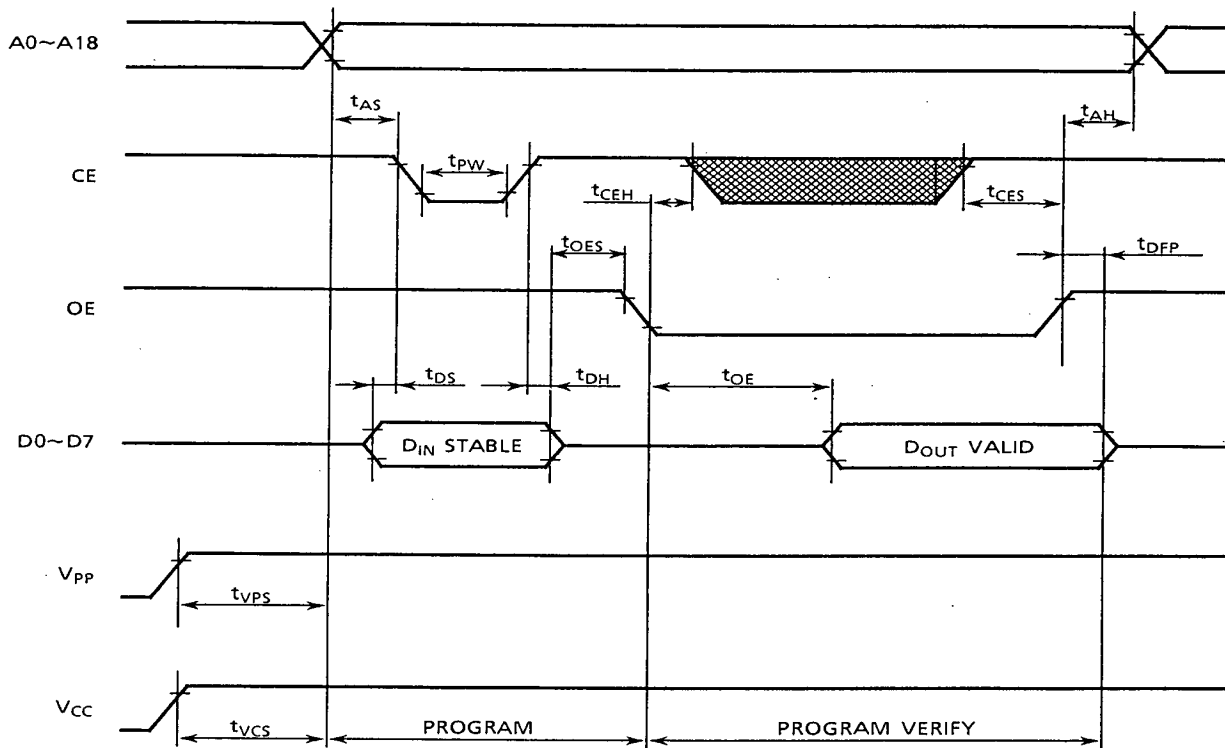
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	0	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	0	—	—	μs
t_{OES}	$\overline{OE}$ Set up Time	—	2	—	—	μs
t_{DS}	Data Set up Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VPS}	V_{PP} Set up Time	—	2	—	—	μs
t_{VCS}	V_{CC} Set up Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	—	2	—	—	μs
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	45	50	55	μs
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE} = V_{IH}$	—	—	100	ns
		$\overline{CE} = V_{IH}$	—	—	90	ns

AC TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V~2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAM OPERATION



- Note 1. V_{CC} must be applied simultaneously or before V_{pp} and cut off simultaneously or after V_{pp}.
2. Removing the device from socket and setting the device in socket with V_{PP}=12.50V may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

TC574000AD-120,-150

ERASURE CHARACTERISTICS

The TC574000AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window.

Then integrated dose (ultraviolet light intensity [w/cm^2] $\times$ exposure time [sec.]) for erasure should be a minimum of 15 [$\text{w} \cdot \text{sec/cm}^2$].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is a 12000 [$\mu\text{w/cm}^2$] will reduce the exposure time to about 20 minutes. (In this case, the intergrated dose is 12000[$\mu\text{w/cm}^2$] $\times$ (20 $\times$ 60) [sec.] $\approx$ 15 [$\text{w} \cdot \text{sec/cm}^2$].)

The TC574000AD's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TC574000AD's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

MODE		PIN NAMES (NUMBER)	$\overline{\text{CE}}$ (22)	$\overline{\text{OE}}$ (24)	V_{PP} (1)	V_{CC} (32)	D0~D7 (13~15, 17~21)	POWER
Read Operation ($T_a = 0 \sim 70^\circ\text{C}$)	Read		L	L	5V	5V	Data Out	Active
	Output Deselet		*	H			High Impedance	
	Standby		H	*			High Impedance	Standby
Program Operation ($T_a = 25 \pm 5^\circ\text{C}$)	Program		L	H	12.50V	6.25V	Data In	Active
	Program Inhibit		H	H			High Impedance	
	Program Verify		*	L			Data Out	

Note : H : V_{IH} , L : V_{IL} , * : V_{IH} or V_{IL}

READ MODE

The TC574000AD has two control functions. The chip enable ($\overline{\text{CE}}$) controls the operation power and should be used for device selection. The output enable ($\overline{\text{OE}}$) controls the output buffers, independent of device selection. Assuming that $\overline{\text{CE}} = \overline{\text{OE}} = V_{\text{IL}}$, the output data is valid at the outputs after address access time from stabilizing of all addresses. The $\overline{\text{CE}}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{\text{CE}} = V_{\text{IL}}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{\text{OE}}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$, the outputs will be in a high impedance state. So two or more TC574000AD's can be connected together on a common bus line. When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC574000AD has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC574000AD is placed in the standby mode which reduce the operating current to $100\mu A$ by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC574000AD are in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming. The TC574000AD is in the programming mode when the V_{PP} input is at 12.50V and $\overline{CE}$ is at Low under $\overline{OE} = V_{IH}$.

The TC574000AD can be programmed any location at any time either indivicually, sequentially, or at random.

PROGRAM VERIFY MODE

The verigy mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with $\overline{OE}$ at V_{IL} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.50V) is applied to V_{PP} terminal, a high level $\overline{CE}$ and $\overline{OE}$ input inhibits the TC574000AD from being programmed.

Programming of two or more TC574000AD's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a low level program pulse is applied to the $\overline{CE}$ of the desired device only and high level signal is applied to the other devices.

HIGH SPEED PROGRAM MODE

The device is set up in the high speed programming mode when the programming voltage (+12.50V) is applied to the V_{PP} terminal with $V_{CC}=6.25V$.

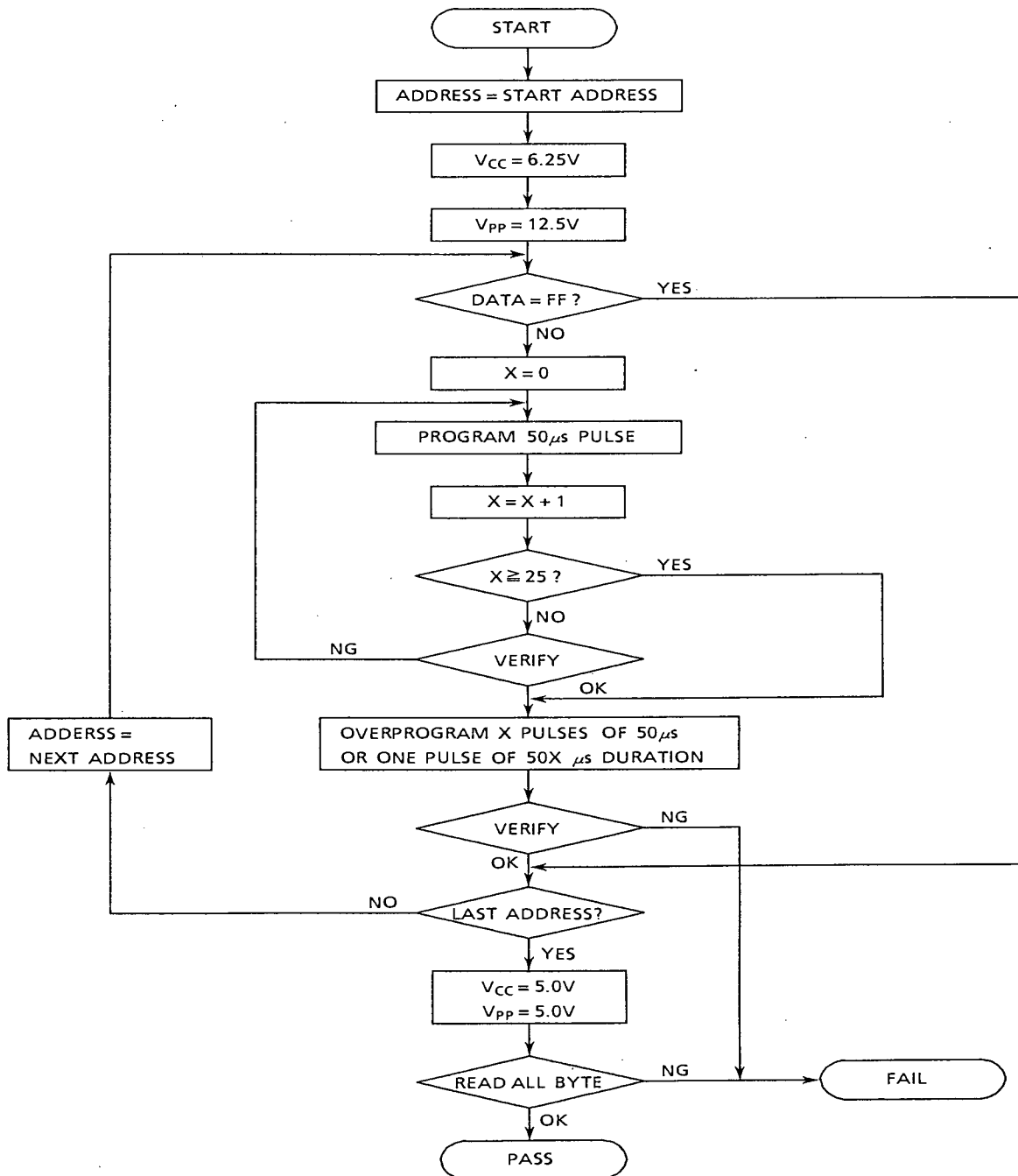
The programming is achieved by applying a single low level $50\mu s$ pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of $50\mu s$ is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with width of 1 time more than that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM MODE

FLOW CHART



TC574000AD-120, -150

ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC574000AD which identifies its manufacturer and device type.

The programming equipment may reads out manufacturer code and device code from TC574000AD by using this mode before program operation and automatically set program voltage (V_{pp}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH} .

These two codes possess an odd parity with the parity bit of MSB (D7).

The following table shows electric signature of TC574000AD.

SIGNATURE	PINS	A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	0	98
Device Code	V_{IH}	1	0	0	0	1	1	0	0	0	8C

Notes: A9=12V $\pm$ 0.5V

A1~A8, A0~A18, $\overline{CE}$, $\overline{OE}$ = V_{IL}

SILICON STACKED GATE MOS INTEGRATED CIRCUIT

TC574200D-10,-120,-150

4MEGA BIT (262,144 WORD × 16BIT / 524,288 WORD × 8BIT)
CMOS U.V. ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The TC574200D is a 4,194,304 bit CMOS ultraviolet light erasable and electrically programmable read only memory. It is organized as 256K words of 16 bit or 512K words of 8 bit.

The TC574200D is compatible with 40 pin 4M bit Mask ROM. This product is packed in 40 pin standard cerdip package. The TC574200D is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and low power features with access time of 100ns/120ns / 150ns and a maximum operating current of 70mA / 10MHz. The programming time of the TC574200D except overhead times of EPROM programmer is only 28 seconds by using the high speed programming algorithm.

FEATURES

- Peripheral circuit : CMOS
- Memory cell : NMOS
- Fast access time
- Low power
- Standby dissipation : 100 μ A
- Full static operation
- Input and output TTL compatible
- Three state output
- High speed programming operation : tpw 50 μ s
- 4M MROM compatible pinout : TC534200P
- Standard 40 pin DIP cerdip package : WDIP40 - P - 600B

	- 10	- 120	- 150
V _{CC}	5V $\pm$ 5%	5V $\pm$ 10%	
Temp	0°C ~ 70°C		
T _{acc}	100ns	120ns	150ns

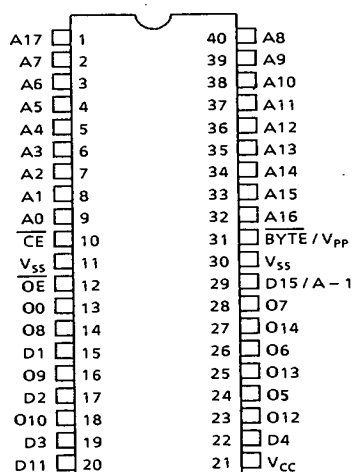
-10 satisfies characteristics of -120.

- Single 5V power supply

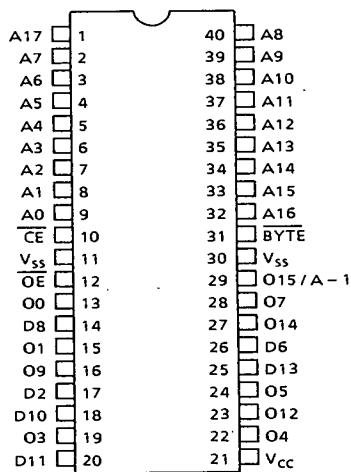
PIN CONNECTION

(TOP VIEW)

(Reference)



TC574200D



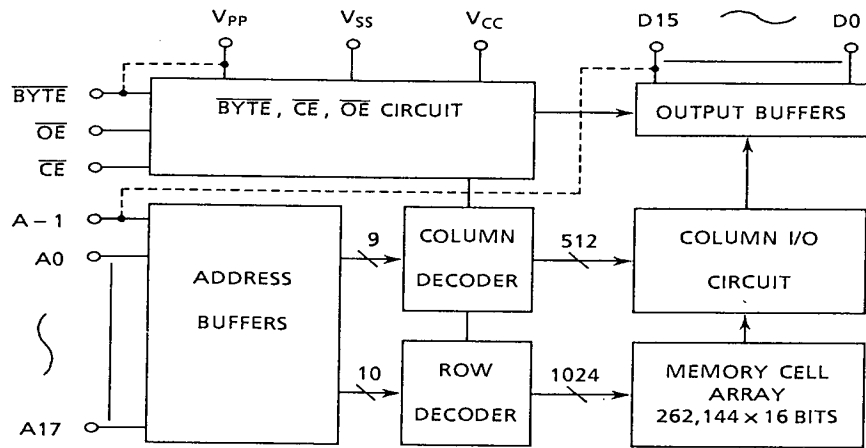
4M Mask ROM
TC534200P

PIN NAMES

A0~A17	Address Input
D0~D14	Output (Input)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
D15 / A - 1	Output (Input) / Address Input
BYTE / V _{pp}	Word, Byte select Input / Program Supply Voltage
V _{CC}	V _{CC} Supply Voltage
V _{SS}	Ground

TC574200D-10,-120,-150

BLOCK DIAGRAM



MODE SELECTION

MODE \ PINS	$\overline{CE}$	$\overline{OE}$	BYTE / V_{PP}	V_{CC}	D0~D7	D8~D14	D15 / A-1	Power
Read (16 Bit)	L	L	H	5V	Data Out			Active
Read (Lower 8 Bit)	L	L	L		Data Out (Lower 8 Bit)	High Impedance	L	
Read (Upper 8 Bit)	L	L	L		Data Out (Upper 8 Bit)	High Impedance	H	
Output Deselect	L	H	H		High Impedance			
			L		High Impedance		*	
Standby	H	*	H	High Impedance			Standby	
			L	High Impedance		*		
Program	L	H	12.5V	6.25V	Data In			Active
Program Inhibit	H	H			High Impedance			
Program Verify	*	L			Data Out			

Note: H = V_{IH} , L = V_{IL} , * = V_{IH} or V_{IL}

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	- 0.6~7.0	V
V_{PP}	Program Supply Voltage	- 0.6~14.0	V
V_{IN}	Input Voltage	- 0.6~7.0	V
$V_{IN(A9)}$	Input Voltage (A9)	- 0.6~13.5	V
$V_{I/O}$	Input / Output Voltage	- 0.6~ $V_{CC} + 0.5$	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260·10	°C · sec
T_{STRG}	Storage Temperature	- 65~150	°C
T_{OPR}	Operating Temperature	0~70	°C

TC574200D-10,-120,-150

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC574200D - 10	TC574200D - 120 / 150
V_{IH}	Input High Voltage	$2.2V \sim V_{CC} + 0.3$	$2.2V \sim V_{CC} + 0.3$
V_{IL}	Input Low Voltage	$-0.3V \sim 0.8V$	$-0.3V \sim 0.8V$
V_{CC}	V_{CC} Power Supply Voltage	$5V \pm 5\%$	$5V \pm 10\%$

D.C. AND OPERATING CHARACTERISTICS (Ta = 0~70°C)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0V \sim V_{CC}$	-	-	± 10	μA
I_{CCO1}	Operating Current	$\overline{CE} = 0V$ $I_{OUT} = 0mA$ $f = 10MHz$	-	-	70	mA
		$\overline{CE} = 0V$ $I_{OUT} = 0mA$ $f = 8.3MHz$	-	-	60	mA
I_{CCO2}		$\overline{CE} = 0V$ $I_{OUT} = 0mA$ $f = 1MHz$	-	-	30	mA
I_{CCS1}	Standby Current	$\overline{CE} = V_{IH}$	-	-	1	mA
I_{CCS2}		$\overline{CE} = V_{CC} - 0.2V$	-	-	100	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu A$	2.4	-	-	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1mA$	-	-	0.4	V
I_{PP1}	V_{PP} Current	$V_{PP} = 0V \sim V_{CC} + 0.6V$	-	-	± 10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 0.4V \sim V_{CC}$	-	-	± 10	μA

A.C. CHARACTERISTICS (Ta = 0~70°C)

SYMBOL	PARAMETER	- 10		- 120		- 150		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	-	100	-	120	-	150	ns
t_{CE}	$\overline{CE}$ to Output Valid	-	100	-	120	-	150	ns
t_{OE}	$\overline{OE}$ to Output Valid	-	50	-	60	-	70	ns
t_{DF1}	$\overline{CE}$ to Output in High Impedance	0	50	0	50	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High Impedance	0	50	0	50	0	60	ns
t_{OH}	Output Data Hold Time	0	-	0	-	0	-	ns
t_{BT}	BYTE to Output Valid	-	100	-	120	-	150	ns
t_{BD}	BYTE to Output in High Impedance	-	60	-	60	-	70	ns

TC574200D - 10 satisfies characteristics of TC574200D - 120.

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and $CL = 100PF$
- Input Pulse Rise and Fall Time : 10ns Max
- Input Pulse Levels : 0.45V and 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

TC574200D-10,-120,-150

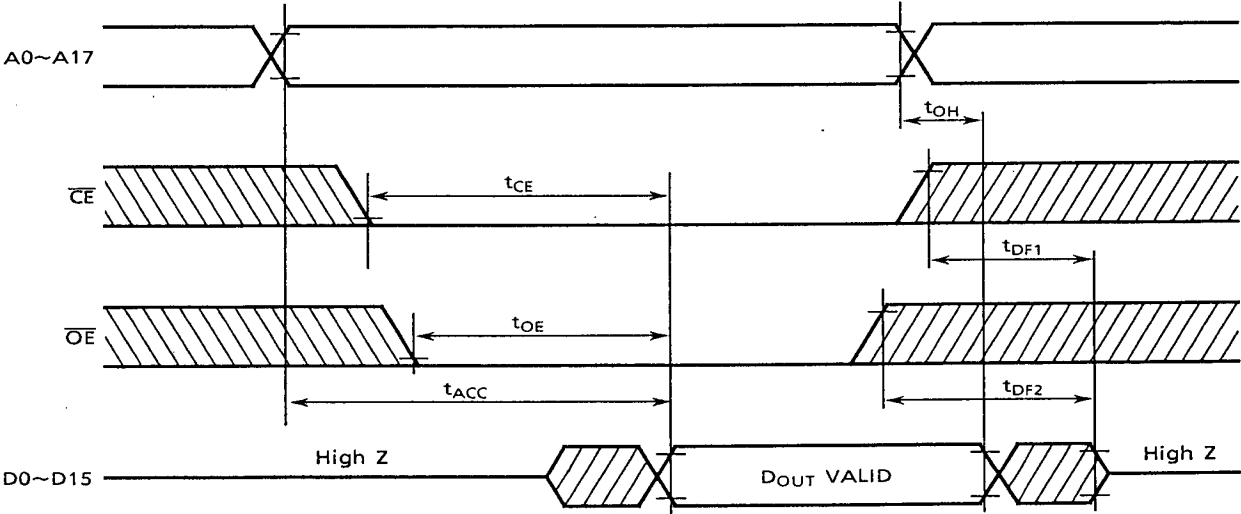
CAPACITANCE * (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
CIN1	Input Capacitance	VIN = 0V	—	6	10	pF
CIN2	Input Capacitance (BYTE / Vpp)	VIN = 0V	—	110	120	pF
COUT	Output Capacitance	VOU = 0V	—	10	12	pF

* This parameter is periodically sampled and is not 100% tested.

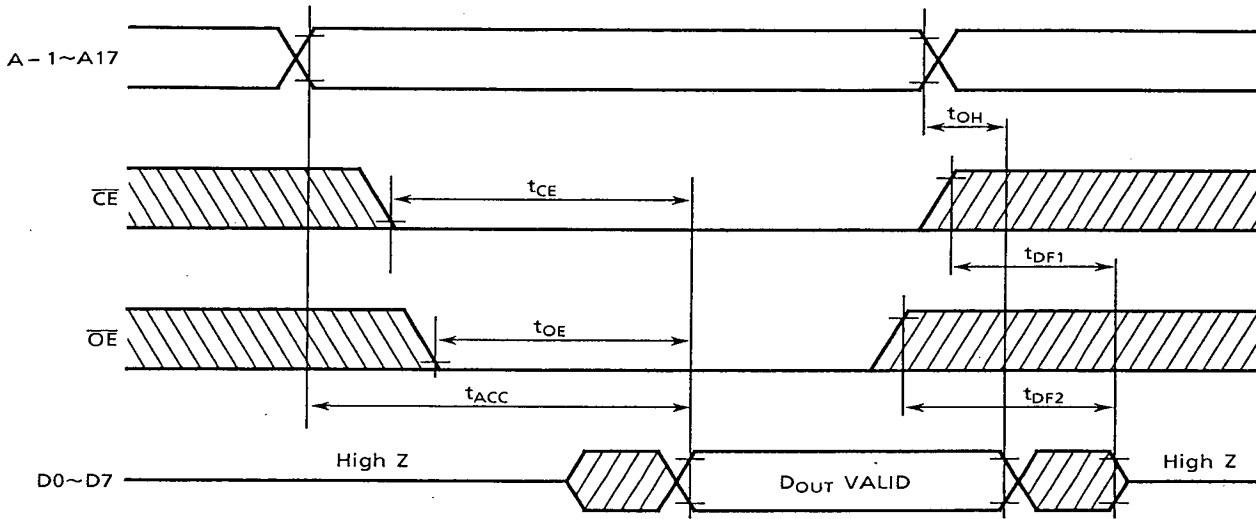
TIMING WAVEFORMS

WORD – WIDE READ MODE



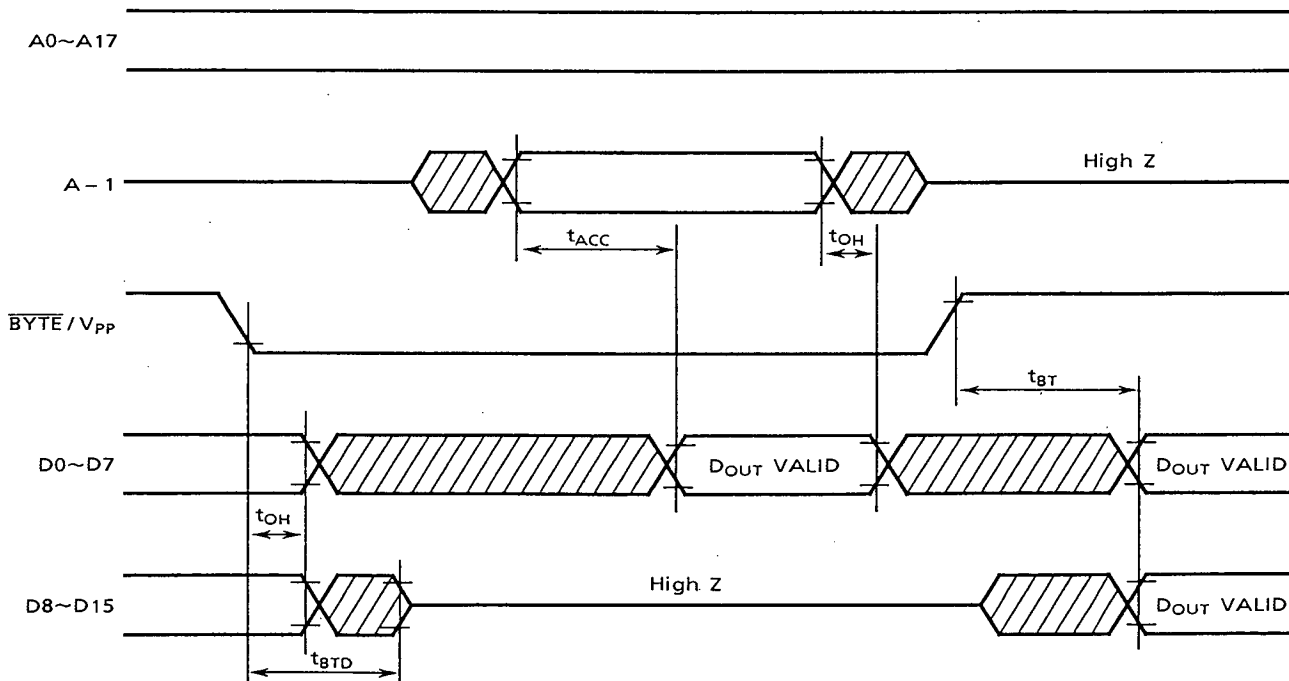
Note: $\overline{\text{BYTE}} / V_{pp} = V_{IH}$

BYTE - WIDE READ MODE



Note: $\overline{BYTE} / V_{PP} = V_{IL}$

BYTE TRANSITION



Note: $\overline{CE}, \overline{OE} = V_{IL}$

TC574200D-10,-120,-150

HIGH SPEED PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	$V_{CC} + 1.0$	V
V_{IL}	Input Low Voltage	-0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.20	12.50	12.80	V

D.C. AND OPERATING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25 \pm 0.25\text{V}$, $V_{PP} = 12.50 \pm 0.30\text{V}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0\text{V} \sim V_{CC}$	—	—	± 10	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{mA}$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	40	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP} = 12.8\text{V}$	—	—	50	mA

A.C. PROGRAMMING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25 \pm 0.25\text{V}$, $V_{PP} = 12.50 \pm 0.30\text{V}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	0	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	0	—	—	μs
t_{OES}	$\overline{OE}$ Setup Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VPS}	V_{PP} Setup Time	—	2	—	—	μs
t_{VCS}	V_{CC} Setup Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	—	45	50	55	μs
t_{OPW}	Overprogram Pulse Width	Note 1	45	50	55	μs
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE} = V_{IH}$	—	—	100	ns
t_{DFP}	$\overline{OE}$ to Output in High Impedance	$\overline{CE} = V_{IH}$	—	—	90	ns

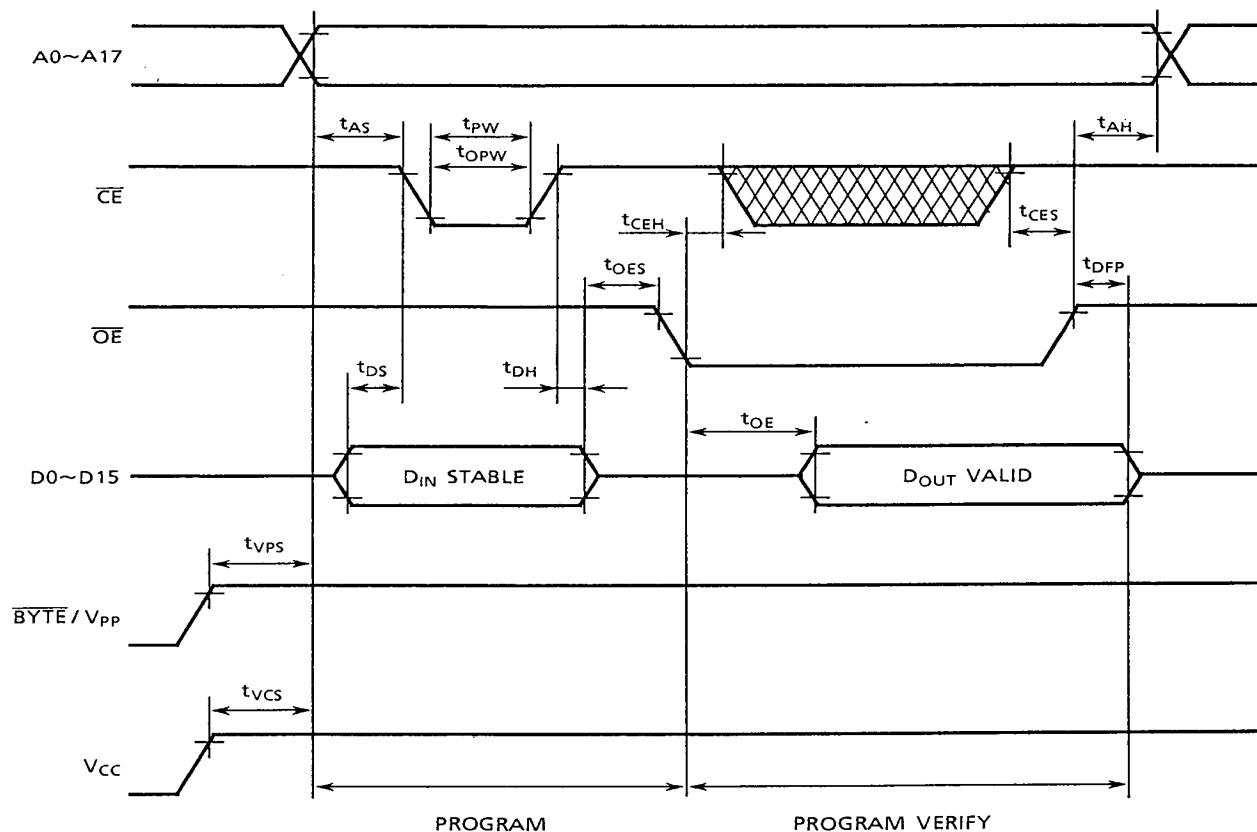
A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and $CL = 100\text{PF}$
- Input Pulse Rise and Fall Time : 10ns Max
- Input Pulse Levels : 0.45V and 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

Note 1: t_{OPW} depends on the program pulse width which is required in the initial program.

TIMING WAVEFORMS

HIGH SPEED PROGRAM OPERATION



- Note: 1. V_{CC} must be applied simultaneously or before V_{pp} and cut off simultaneously or after V_{pp} .
2. Removing the device from socket and setting the device in socket with $V_{pp}=12.50V$ may cause permanent damage to the device.
3. The V_{pp} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{pp} terminal. When the switching pulse voltage is applied to the V_{pp} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

TC574200D-10,-120,-150

ERASURE CHARACTERISTICS

The TC574200D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. Then integrated dose (ultraviolet light intensity [W/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [W · sec/cm²].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [μW/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μW/cm²] × (20×60) [sec]=15 [W · sec/cm²].)

The TC574200D's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals - Toshiba EPROM Protect Seal AC907 - are available.

OPERATION INFORMATION

The TC574200D's eight operation mode are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PINS	CE	OE	BYTE / V _{PP}	V _{CC}	D0~D7	D8~D14	D15 / A-1	Power
Read (16 Bit)	L	L	H	5V	Data Out			Active
Read (Lower 8 Bit)	L	L	L		Data Out (Lower 8 Bit)	High Impedance	L	
Read (Upper 8 Bit)	L	L	L		Data Out (Upper 8 Bit)	High Impedance	H	
Output Deselect	L	H	H		High Impedance			
			L		High Impedance		*	
Standby	H	*	H		High Impedance			
			L	High Impedance		*		
Program	L	H	12.5V	6.25V	Data In			Active
Program Inhibit	H	H			High Impedance			
Program Verify	*	L			Data Out			

Note: H = V_{IH}, L = V_{IL}, * = V_{IH} or V_{IL}

READ MODE

The TC574200D has the $\overline{\text{BYTE}}/\text{V}_{\text{PP}}$ terminal that selects word-wide output and byte-wide output. When $\overline{\text{BYTE}}/\text{V}_{\text{PP}}$ is set to V_{IH} , the word-wide output is selected, and D15/A-1 pin is used for D15 data output.

When $\overline{\text{BYTE}}/\text{V}_{\text{PP}}$ is set to V_{IL} , the byte-wide output is selected, and D15/A-1 pin is used for A-1 address input. When A-1 is set to V_{IL} in this condition, the data output is selected lower 8 bits of the 16 bit data which has been programmed. When A-1 is set to V_{IH} , the data output is selected upper 8 bits.

The TC574200D has two control function. The chip enable ($\overline{\text{CE}}$) controls the operation power and should be used for device selection. The output enable ($\overline{\text{OE}}$) controls the output buffers, independent of device selection. Assuming that $\overline{\text{CE}} = \overline{\text{OE}} = \text{V}_{\text{IL}}$, the output data is valid at the outputs after address access time from stabilizing of all addresses. The $\overline{\text{CE}}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}). Assuming that $\overline{\text{CE}} = \text{V}_{\text{IL}}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{\text{OE}}$.

OUTPUT DESELECT MODE

Assuming that $\overline{\text{CE}} = \text{V}_{\text{IH}}$ or $\overline{\text{OE}} = \text{V}_{\text{IH}}$, the outputs will be in a high impedance state. So two or more TC574200D's can be connected together on a common bus line. When $\overline{\text{CE}}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC574200D has a low power standby mode controlled by the $\overline{\text{CE}}$ signal. By applying a high level to the $\overline{\text{CE}}$ input, the TC574200D is placed in the standby mode which reduces the operating current to $100\mu\text{A}$ by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$ input.

TC574200D-10,-120,-150

PROGRAM MODE

Initially, when recieved by customers, all bits of the TC574200D are in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit location by electrically programming. The TC574200D is in the programming mode when the V_{PP} input is at 12.50V and $\overline{CE}$ is at TTL-Low under $\overline{OE}=V_{IH}$. Data to be programmed must be applied 16 bits in parallel to the data pins.

The TC574200D can be programmed any location at anytime either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with $\overline{OE}$ at V_{IL} . The programmed data should be compared with the original word-wide (16 bit) data.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (12.50V) is applied to V_{PP} terminal, a high level $\overline{CE}$ input inhibits the TC574200D from being programmed. Programming of two or more EPROMs in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

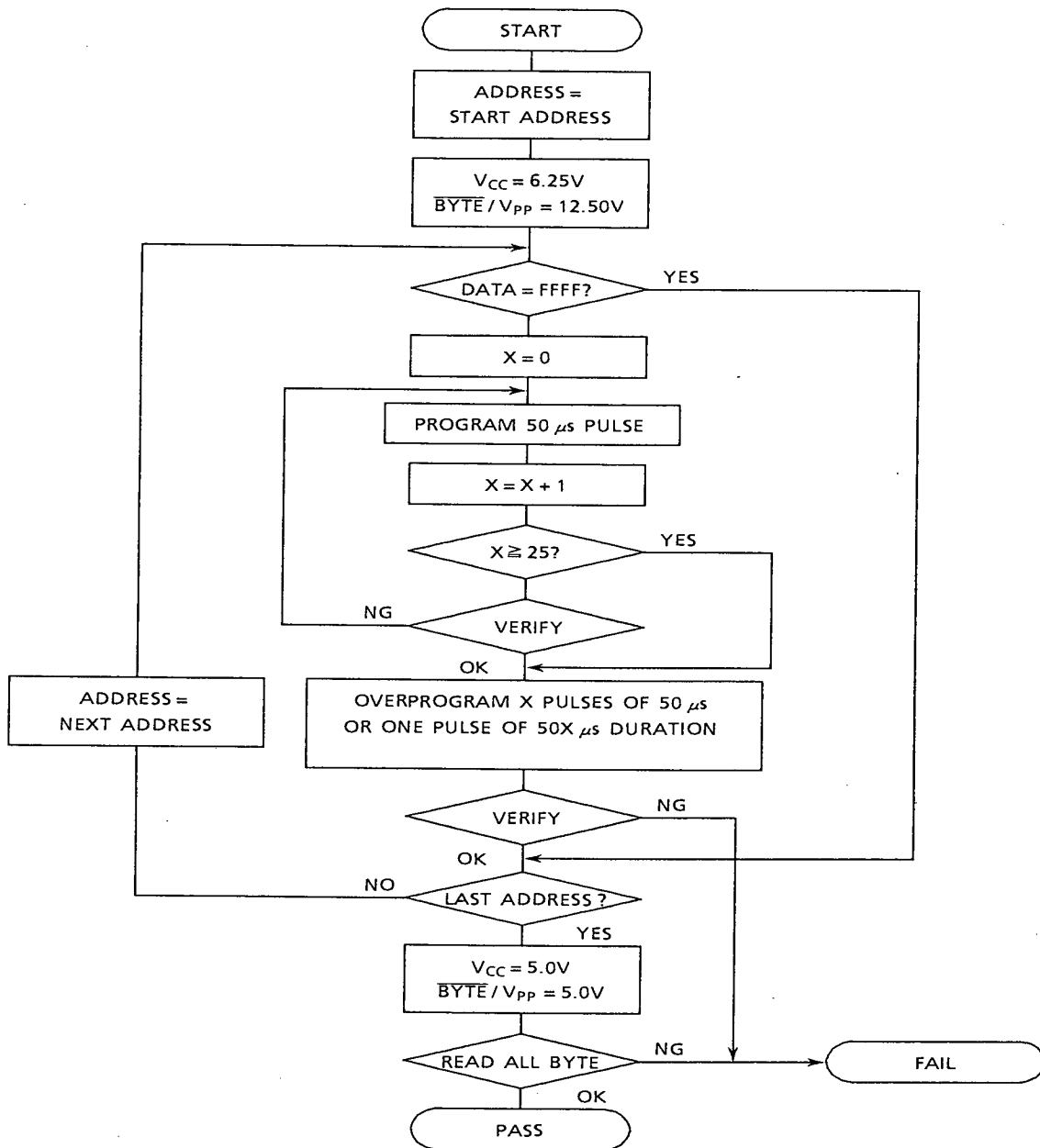
HIGH SPEED PROGRAM MODE

The device is set up the high speed programming mode when the programming voltage (12.50V) is applied to the V_{PP} terminal with $V_{CC}=6.25V$. The programming is achieved by applying a single TTL low level $50\mu s$ pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of $50\mu s$ is applied and then the programmed data is verified. This should be repeated until the program operates correctly(max. 25 times).

After correctly programming the selected address, the overprogram pulse of same length that needed for initial programming should be applied. When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM MODE

FLOW CHART



TC574200D-10,-120,-150

ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC574200D which identifies its manufacturer and device type. The programming equipment may read out manufacturer code and device code from TC574200D by using this mode before program operation and automatically set program voltage(V_{pp}) and algorithm.

Electric signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of (D7).

The following table shows electric signature of TC574200D.

SIGNATURE \ PINS	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX DATA
Manufacturer Code	V _{IL}	*	*	*	*	*	*	*	*	1	0	0	1	1	0	0	0	**98
Device Code	V _{IH}	*	*	*	*	*	*	*	*	1	0	0	0	1	1	1	1	**8F

Note: A9 = 12.0V ± 0.5V
 * A1 – A8, A10 – A17, $\overline{CE}$, $\overline{OE}$ = V_{IL}
 BYTE / VPP = V_{IH}

*Don't care

SILICON STACKED GATE MOS INTEGRATED CIRCUIT

TC574096D-10,-120,-150

4 MEGA BIT (262,144 WORD $\times$ 16 BIT)

CMOS U.V. ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The TC574096D is a 262,144 word $\times$ 16 bit CMOS ultraviolet light erasable and electrically programmable read only memory. The TC574096D is JEDEC standard pin configuration. This product is packed in 40 pin standard cerdip package.

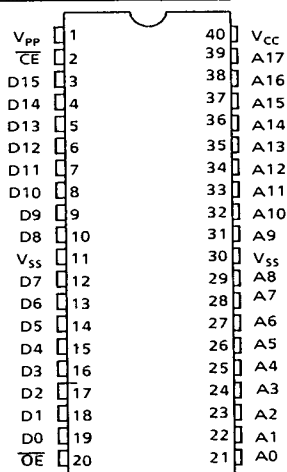
TC574096D is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 70mA/10MHz and access time of 100ns/120ns/150ns.

For program operation, the programming is achieved by using the high speed programming mode.

FEATURES

- Peripheral circuit : CMOS
- Memory cell : N-MOS
- Fast access time
 - TC574096D - 10 : 100ns ($V_{CC}=5.0V \pm 5\%$)
 - TC574096D - 120 : 120ns ($V_{CC}=5.0V \pm 10\%$)
 - TC574096D - 150 : 150ns ($V_{CC}=5.0V \pm 10\%$)
- Low power dissipation
 - Active : 60mA/10MHz
 - Standby : 100 μ A
- Single 5V power supply
- Full static operation
- High speed programming operation : tpw 50 μ s
- Input and output TTL compatible
- JEDEC standard 40 pin
- Standard 40 pin DIP cerdip package

PIN CONNECTION (TOP VIEW)

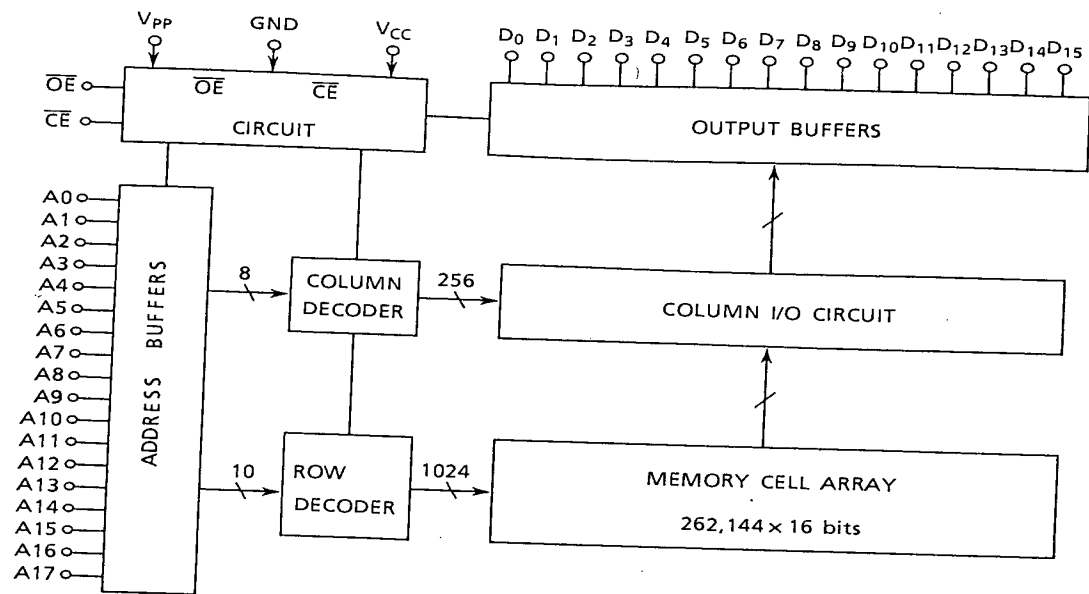


PIN NAMES

A0~A17	Address Inputs
D0~D15	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{CC}	V_{CC} Supply Voltage
V_{PP}	Program Supply Voltage
V_{SS}	Ground

TC574096D-10,-120,-150

BLOCK DIAGRAM



MODE SELECTION

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	D0~D15	Power
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*				Standby
Program	L	H	12.50V	6.25V	Data In	Active
Program Inhibit	H	H			High Impedance	
Program Verify	*	L			Data Out	

* : H or L

MAXIMUM RATINGS

SYMBOL	CHARACTERISTIC	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	- 0.6~7.0	V
V_{PP}	Program Supply Voltage	- 0.6~14.0	V
V_{IN}	Input Voltage	- 0.6~7.0	V
$V_{IN}(A9)$	Input Voltage (A9)	- 0.6~13.5	V
$V_{I/O}$	Input/Output Voltage	- 0.6~ $V_{CC} + 0.5$	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature Time	260 · 10	°C · sec
T_{strg}	Storage Temperature	- 65~125	°C
T_{opr}	Operating Temperature	0~70	°C

TC574096D-10,-120,-150

READ OPERATION

AC/DC RECOMMENDED OPERATING CONDITIONS

AC/DC RECOMMENDED OPERATING CONDITIONS				
SYMBOL	CHARACTERISTIC	TC574096D - 10	TC574096D - 120	TC574096D - 150
Ta	Ambient Temperature	0~70°C		
VCC	VCC Power Supply Voltage	5V ± 5%	5V ± 10%	
VPP	VPP Power Supply Voltage	0V~VCC + 0.6V		

DC CHARACTERISTICS

記 号	項 目	条 件	MIN.	TYP.	MAX.	単 位
I _{LI}	Input Current	V _{IN} = 0~V _{CC}	—	—	± 10	μA
I _{CCO1}	Operating Current	$\overline{CE} = 0V$ I _{OUT} = 0mA	f = 8.3MHz	—	60	mA
			f = 10MHz	—	70	
I _{CCO2}			f = 1MHz	—	30	
I _{CCS1}	Standby Current	$\overline{CE} = V_{IH}$	—	—	1	mA
I _{CCS2}		$\overline{CE} = V_{CC} - 0.2V$	—	—	100	
V _{IH}	Input High Voltage	—	2.2	—	V _{CC} + 0	V
V _{IL}	Input Low Voltage	—	- 0.3	—	0.8	V
V _{OH}	Output High Voltage	I _{OH} = - 400μA	2.4	—	—	V
V _{OL}	Output Low Voltage	I _{OL} = 2.1mA	—	—	0.4	V
I _{PP1}	V _{PP} Current	V _{PP} = 0V~V _{CC} + 0.6V	—	—	± 10	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0.4V~V _{CC}	—	—	± 10	μA

SYMBOL	CHARACTERISTIC	TC574096D - 10		TC574096D - 120		TC574096D - 150		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{ACC}	Address Access Time	—	100	—	120	—	150	ns
t _{CE}	$\overline{CE}$ to Output Valid	—	100	—	120	—	150	
t _{OE}	$\overline{OE}$ to Output Valid	—	50	—	60	—	70	
t _{DF1}	$\overline{CE}$ to Output in High-Z	—	50	—	50	—	60	
t _{DF2}	$\overline{OE}$ to Output in High-Z	—	50	—	50	—	60	
t _{OH}	Output Data Hold Time	0	—	0	—	0	—	

TC574096D - 10 satisfies characteristics of TC574096D - 120 / 150

AC TEST CONDITIONS

Output Load : 1 TTL Gate and C_L = 100pF
Input Pulse Rise and Fall Times : 10ns Max.
Input Pulse Levels : 0.45V to 2.4V
Timing Measurement Reference Levels: Inputs 0.8V and 2.2V Outputs 0.8V and 2.0V

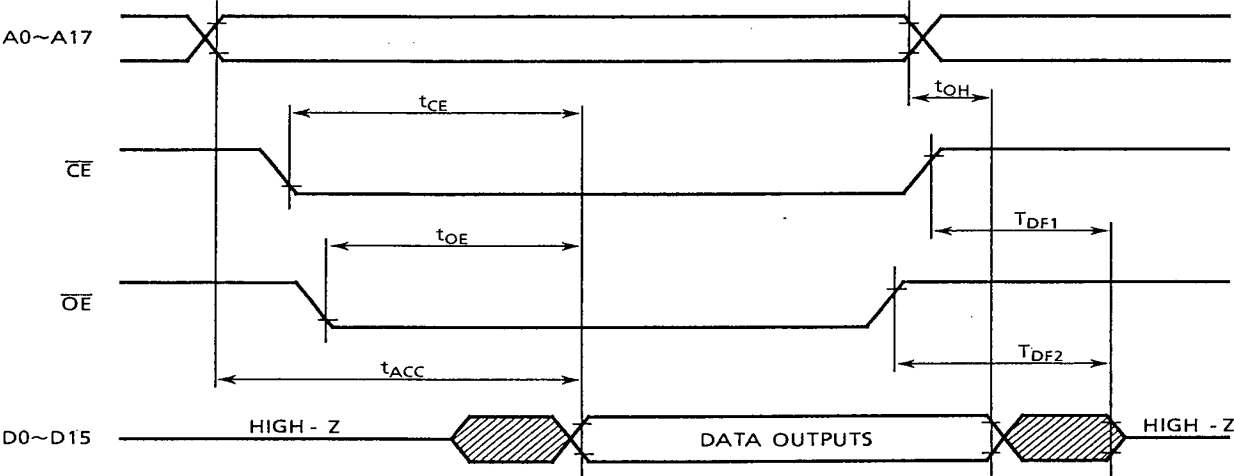
TC574096D-10,-120,-150

CAPACITANCE *(Ta=25°C, f=1MHz)

SYMBOL	CHARACTERISTIC	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = 0V	—	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	—	10	12	

* This characteristic is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



TC574096D-10,-120,-150

HIGH SPEED PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	$V_{CC} + 1.0$	V
V_{IL}	Input Low Voltage	-0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.20	12.50	12.80	V

DC AND OPERATING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.50\text{V} \pm 0.30\text{V}$)

SYMBOL	CHARACTERISTIC	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	—	—	± 10	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{mA}$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	30	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP} = 12.8\text{V}$	—	—	50	mA

AC PROGRAMMING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.50\text{V} \pm 0.30\text{V}$)

SYMBOL	CHARACTERISTIC	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	0	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	0	—	—	μs
t_{OES}	$\overline{OE}$ Set up Time	—	2	—	—	μs
t_{DS}	Data Set up Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VPS}	V_{PP} Set up Time	—	2	—	—	μs
t_{VCS}	V_{CC} Set up Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	—	45	50	55	μs
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE} = V_{IH}$	—	—	100	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE} = V_{IH}$	—	—	90	ns

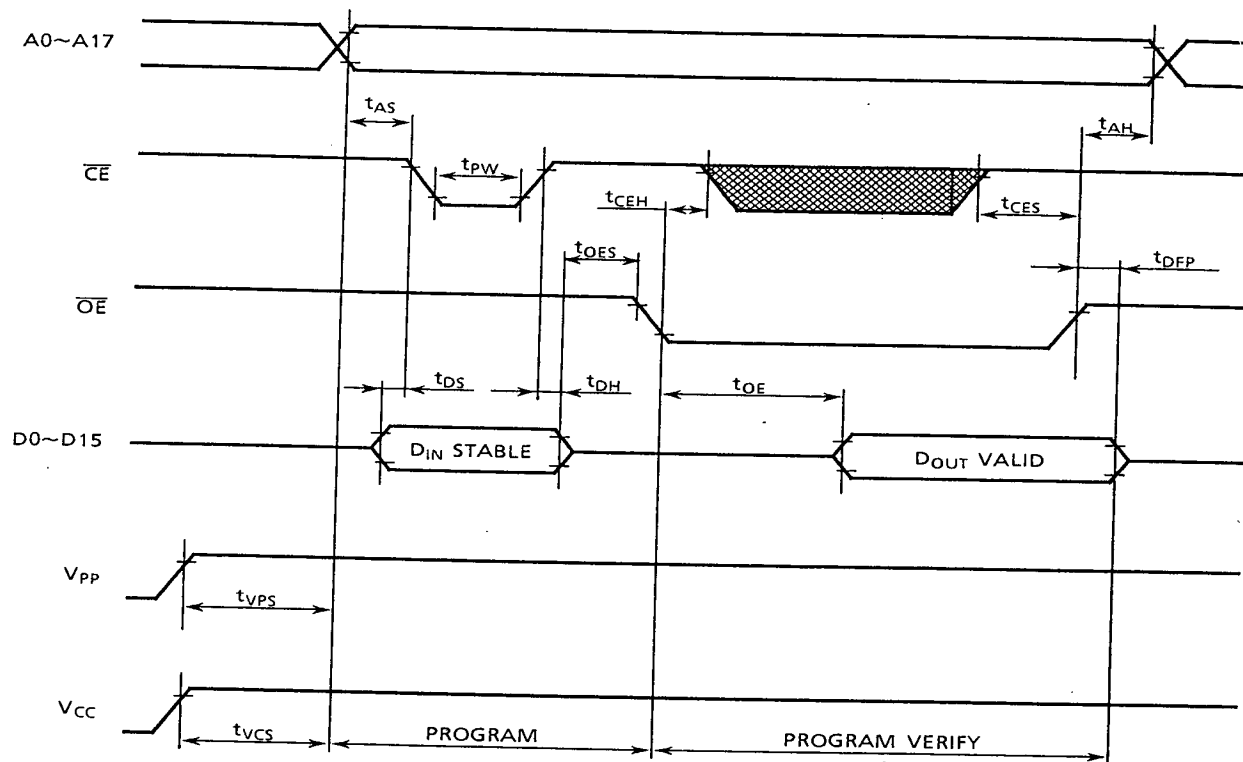
AC TEST CONDITIONS

- Output Load : 1 TTL Gate and $C_L = 100\text{pF}$
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

TC574096D-10,-120,-150

TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAM OPERATION



- Note 1. Vcc must be applied simultaneously or before Vpp and cut off simultaneously or after Vpp.
2. Removing the device from socket and setting the device in socket with Vpp=12.50V may cause permanent damage to the device.
3. The Vpp supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the Vpp terminal. When the switching pulse voltage is applied to the Vpp terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC574096D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. Then integrated dose (Ultraviolet light intensity [W/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [W·sec./cm²].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [μW/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μW/cm²] × (20 × 60) [sec.] ≈ 15 [W·sec./cm²].)

The TC574096D's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals - Toshiba EPROM Protect Seal AC906 - are available.

OPERATION INFORMATION

The TC574096D's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

MODE		PIN NAMES		$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	D0~D15	POWER
Read Operation	Read	L	L	5V	5V	Data Out	Active		
	Output Deselect	*	H			High Impedance			
	Standby	H	*			Standby			
Program Operation (Ta = 25 ± 5°C)	Program	L	H	12.50V	6.25V	Data In	Active		
	Program Inhibit	H	H			High Impedance			
	Program Verify	*	L			Data Out			

Note : H ; V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TC574096D has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection. The output enable ($\overline{OE}$) controls the output buffers, independent of device selection. Assuming that $\overline{CE} = \overline{OE} = V_{IL}$, the output data is valid at the outputs after address access time from stabilizing of all addresses. The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE} = V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

TC574096D-10,-120,-150

OUTPUT DESELECT MODE

Assuming that $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$, the outputs will be in a high impedance state. So two or more TC574096D's can be connected together on a common bus line. When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC574096D has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC574096D is placed in the standby mode which reduce the operating current to $100\mu A$ by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC574096D are in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming. The TC574096D is in the programming mode when the V_{pp} input is at 12.50V and $\overline{CE}$ is at Low under $\overline{OE} = V_{IH}$.

The TC574096D can be programmed any location at any time either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with $\overline{OE}$ at V_{IL} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.50V) is applied to V_{pp} terminal, a high level $\overline{CE}$ and $\overline{OE}$ input inhibits the TC574096D from being programmed.

Programming of two or more TC574096D's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a low level program pulse is applied to the $\overline{CE}$ of the desired device only and high level signal is applied to the other devices.

HIGH SPEED PROGRAM MODE

The device is set up in the high speed programming mode when the programming voltage (+12.50V) is applied to the V_{PP} terminal with V_{CC}=6.25V.

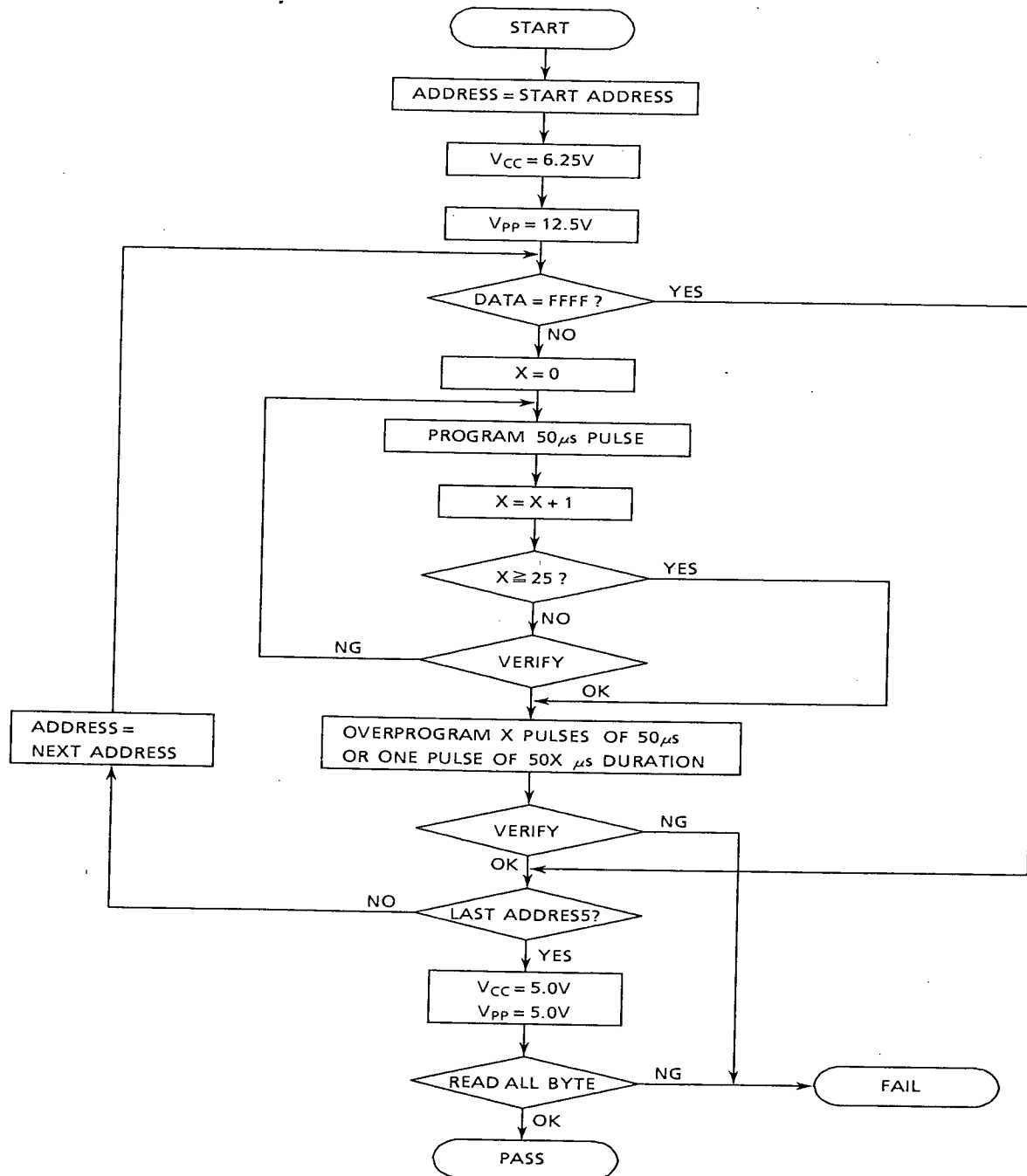
The programming is achieved by applying a single low level 50μs pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of 50μs is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with width of 1 time more than that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with V_{CC}=V_{PP}=5V.

HIGH SPEED PROGRAM MODE

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC574096D which identifies it's manufacture and device type.

The programming equipment may read out manufacturer code and device code from TC574096D by using this mode before program operation and automatically set program voltage (V_{pp}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A₉ and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A₀ is set to V_{IH}.

These two codes possess an odd parity with the parity bit of (D₇).

The following table shows electric signature of TC574096D.

SIGNATURE \ PINS	A ₀	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	HEX DATA
Manufacturer Code	V _{IL}	*	*	*	*	*	*	*	*	1	0	0	1	1	0	0	0	**98
Device Code	V _{IH}	*	*	*	*	*	*	*	*	0	0	0	0	1	1	1	0	**0E

Notes : A₉=12V±0.5V,

A₁—A₈, A₁₀—A₁₇, $\overline{CE}$, $\overline{OE}$ =V_{IL}

*: Don't care

SILICON STACKED GATE MOS INTEGRATED CIRCUIT

TC578200D-150, -200

8MEGA BIT (524,288 WORD × 16BIT / 1,048,576 WORD × 8BIT)

CMOS U.V. ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

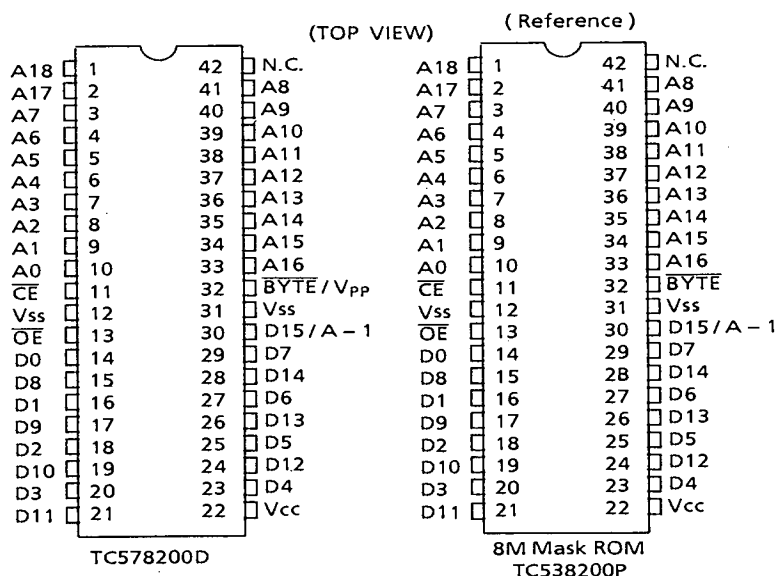
DESCRIPTION

The TC578200D is a 8,388,608 bit CMOS ultraviolet light erasable and electrically programmable read only memory. It is organized as 512K words of 16 bit or 1M words of 8 bit. The TC578200D is compatible with 42 pin 8M bit Mask ROM. This product is packed in 42 pin standard cerdip package. The TC578200D is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and low power features with access time of 150ns/200ns and a maximum operating current of 60mA/6.7MHz. The programming time of the TC578200D except overhead times of EPROM programmer is only 53 seconds by using the high speed programming algorithm.

FEATURES

- Peripheral circuit : CMOS
- Memory cell : NMOS
- Fast access time
($V_{CC}=5V \pm 10\%$, $T_a=0 \sim 70^\circ C$)
TC578200D - 150 : 150ns
TC578200D - 200 : 200ns
- Single 5V power supply
- Low power dissipation
Standby : $100\mu A$
- Full static operation
- Input and output TTL compatible
- Three state output
- High speed programming operation : tpw $50\mu s$
- 8M MROM compatible pinout : TC538200P
- Standard 42 pin DIP cerdip package : WDIP42-G-600B

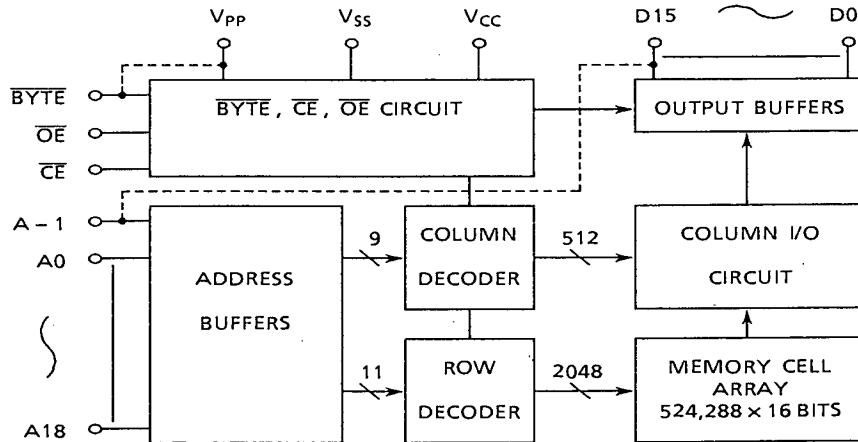
PIN CONNECTION



PIN NAMES

A0~A18	Address Input
D0~D14	Output (Input)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
D15/A-1	Output (Input) / Address Input
BYTE/ V_{PP}	Word, Byte select Input / Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



MODE SELECTION

MODE \ PINS	$\overline{CE}$	$\overline{OE}$	BYTE / V_{pp}	V_{CC}	D0~D7	D8~D14	D15 / A-1	Power
Read (16 Bit)	L	L	H	5V	Data Out			Active
Read (Lower 8 Bit)	L	L	L		Data Out (Lower 8 Bit)	High Impedance	L	
Read (Upper 8 Bit)	L	L	L		Data Out (Upper 8 Bit)	High Impedance	H	
Output Deselect	L	H	H		High Impedance			
			L		High Impedance		*	
Standby	H	*	H		High Impedance			
			L	High Impedance		*		
Program	L	H	12.5V	6.25V	Data In			Active
Program Inhibit	H	H			High Impedance			
Program Verify	*	L			Data Out			

Note: H ... V_{IH} , L ... V_{IL} , * ... V_{IH} or V_{IL}

MAXIMUM RATINGS

SYMBOL	CHARACTERISTIC	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	- 0.6~7.0	V
V_{PP}	Program Supply Voltage	- 0.6~14.0	V
V_{IN}	Input Voltage	- 0.6~7.0	V
$V_{IN} (A9)$	Input Voltage (A9)	- 0.6~13.5	V
$V_{I/O}$	Input / Output Voltage	- 0.6~ $V_{CC} + 0.5$	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260·10	°C · sec
T_{STRG}	Storage Temperature	- 65~150	°C
T_{OPR}	Operating Temperature	0~70	°C

TC578200D-150, -200

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage	- 0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.50	5.00	5.50	V

D.C. AND OPERATING CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	CHARACTERISTIC	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0V \sim V_{CC}$	—	—	± 10	μA
I_{CCO1}	Operating Current	$\overline{CE} = 0V$ $I_{OUT} = 0\text{mA}$ $f = 6.7\text{MHz}$	—	—	60	mA
I_{CCO2}		$\overline{CE} = 0V$ $I_{OUT} = 0\text{mA}$ $f = 1\text{MHz}$	—	—	40	mA
I_{CCS1}	Standby Current	$\overline{CE} = V_{IH}$	—	—	1	mA
I_{CCS2}		$\overline{CE} = V_{CC} - 0.2V$	—	—	100	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{mA}$	—	—	0.4	V
I_{PP1}	V_{PP} Current	$V_{PP} = 0V \sim V_{CC} + 0.6V$	—	—	± 10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 0.4V \sim V_{CC}$	—	—	± 10	μA

A.C. CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	CHARACTERISTIC	- 150		- 200		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	—	150	—	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	—	150	—	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	70	—	70	ns
t_{DF1}	$\overline{CE}$ to Output in High Impedance	0	60	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High Impedance	0	60	0	60	ns
t_{OH}	Output Data Hold Time	0	—	0	—	ns
t_{BT}	$\overline{BYTE}$ to Output Valid	—	150	—	200	ns
t_{BD}	$\overline{BYTE}$ to Output in High Impedance	—	70	—	70	ns

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and $C_L = 100\text{PF}$
- Input Pulse Rise and Fall Time : 10ns Max
- Input Pulse Levels : 0.45V and 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

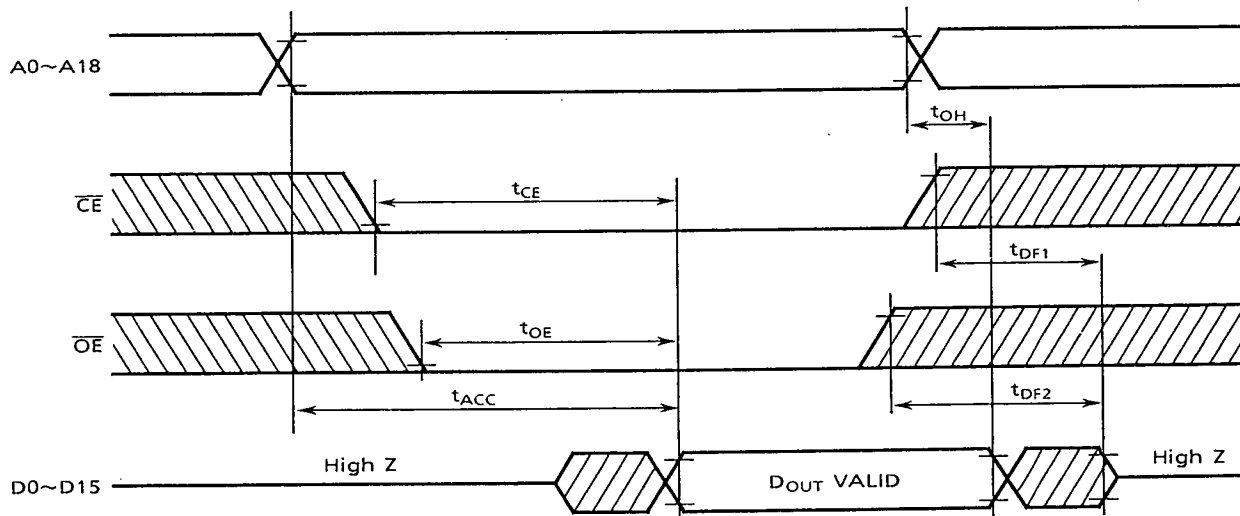
CAPACITANCE * ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	CHARACTERISTIC	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance	$V_{IN} = 0\text{V}$	—	6	10	pF
C_{IN2}	Input Capacitance ($\overline{\text{BYTE}} / V_{PP}$)	$V_{IN} = 0\text{V}$	—	110	120	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0\text{V}$	—	10	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS

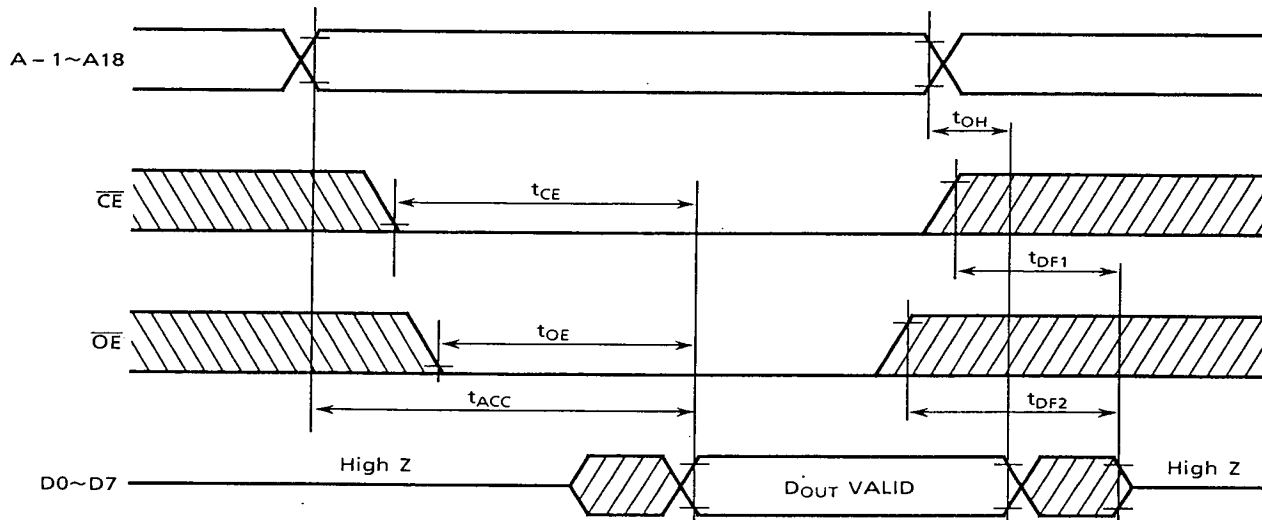
WORD - WIDE READ MODE



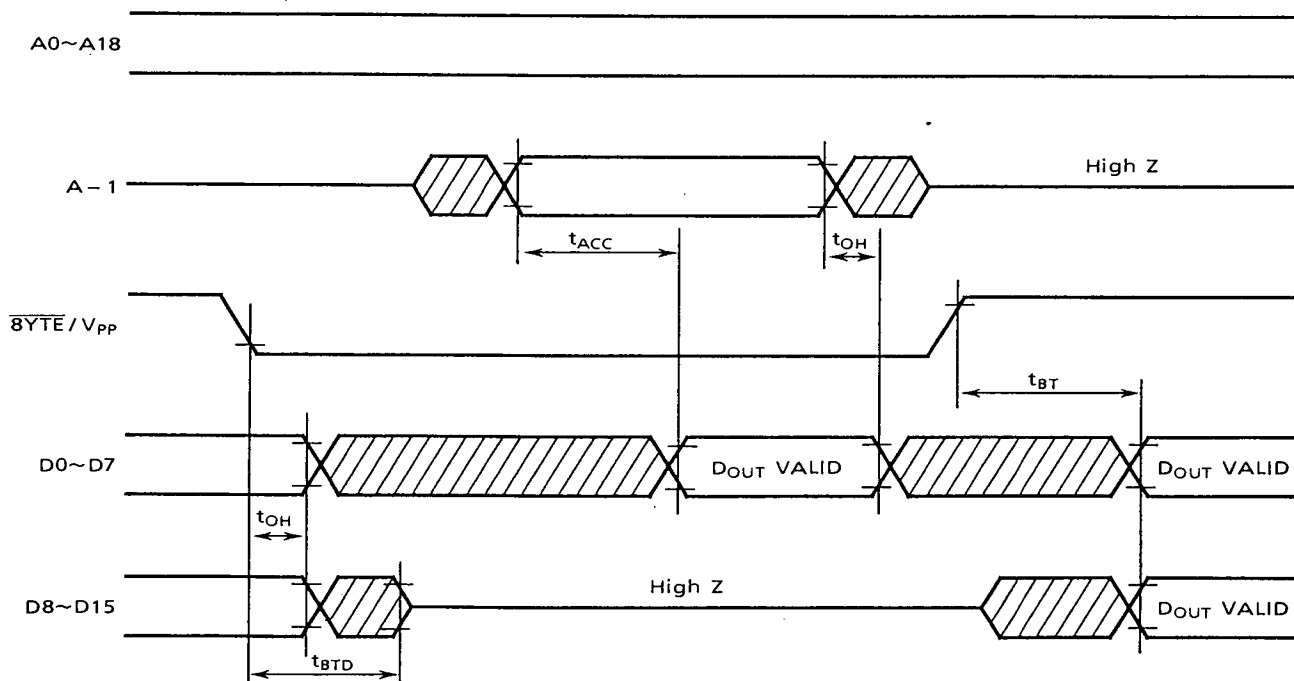
Note: $\overline{\text{BYTE}} / V_{PP} = V_{IH}$

TC578200D-150, -200

BYTE - WIDE READ MODE



BYTE TRANSITION



HIGH SPEED PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	$V_{CC} + 1.0$	V
V_{IL}	Input Low Voltage	-0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.20	12.50	12.80	V

D.C. AND OPERATING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25 \pm 0.25\text{V}$, $V_{PP} = 12.50 \pm 0.30\text{V}$)

SYMBOL	CHARACTERISTIC	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0\text{V} \sim V_{CC}$	—	—	± 10	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{mA}$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	40	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP} = 12.8\text{V}$	—	—	50	mA

A.C. PROGRAMMING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25 \pm 0.25\text{V}$, $V_{PP} = 12.50 \pm 0.30\text{V}$)

SYMBOL	CHARACTERISTIC	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	0	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	0	—	—	μs
t_{OES}	$\overline{OE}$ Setup Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VPS}	V_{PP} Setup Time	—	2	—	—	μs
t_{VCS}	V_{CC} Setup Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	—	45	50	55	μs
t_{OPW}	Overprogram Pulse Width	Note 1	45	50	55	μs
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE} = V_{IH}$	—	—	150	ns
t_{DFP}	$\overline{OE}$ to Output in High Impedance	$\overline{CE} = V_{IH}$	—	—	90	ns

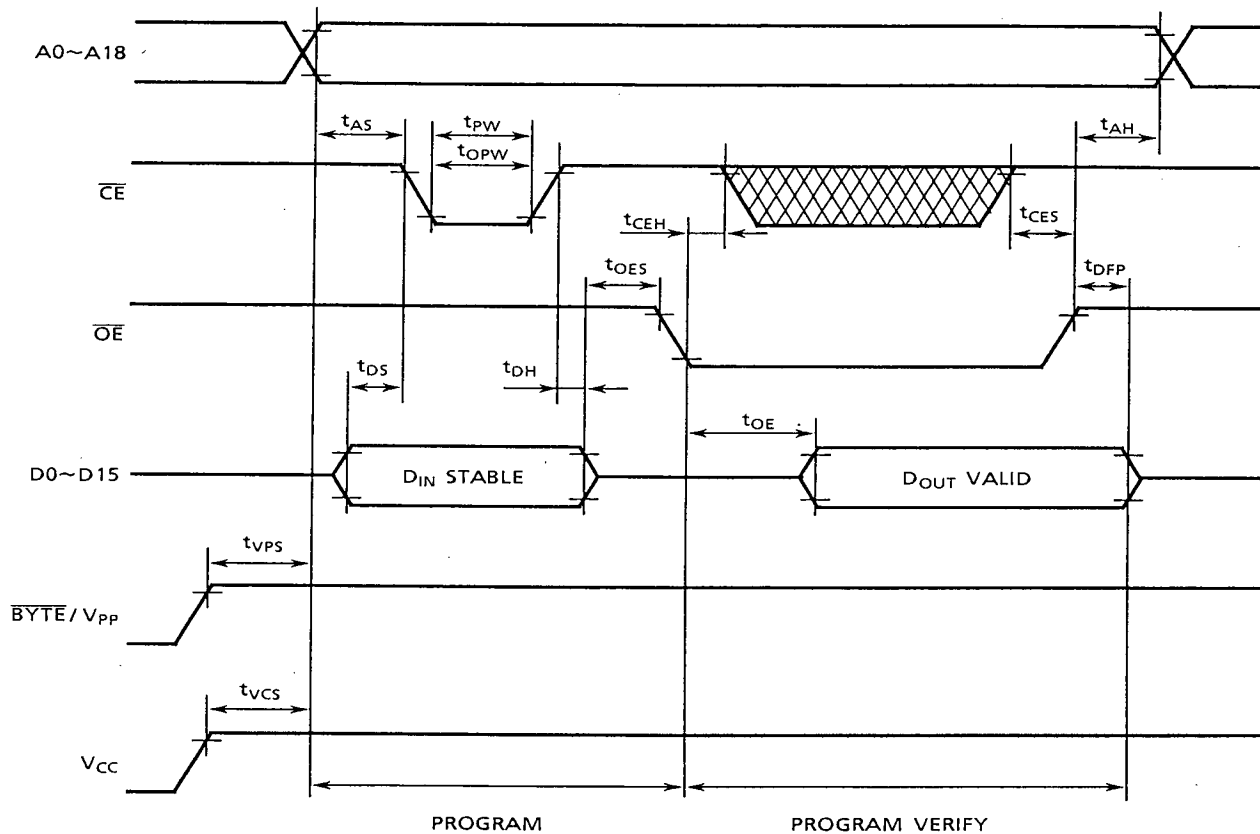
A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and $CL = 100\text{PF}$
- Input Pulse Rise and Fall Time : 10ns Max
- Input Pulse Levels : 0.45V and 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

Note 1: t_{OPW} depends on the program pulse width which is required in the initial program.

TIMING WAVEFORMS

HIGH SPEED PROGRAM OPERATION



- Note: 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP} .
2. Removing the device from socket and setting the device in socket with $V_{PP}=12.50V$ may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC578200D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. Then integrated dose (ultraviolet light intensity [W/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [W · sec/cm²].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [μW/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μW/cm²] × (20×60) [sec] ≈ 15 [W · sec/cm²].)

The TC578200D's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components.

Therefore when used under such lighting for extended periods of time, the opaque seals - Toshiba EPROM Protect Seal AC907 - are available.

OPERATION INFORMATION

The TC578200D's eight operation mode are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PINS	$\overline{CE}$	$\overline{OE}$	BYTE / V _{PP}	V _{CC}	D0~D7	D8~D14	D15 / A-1	Power
Read (16 Bit)	L	L	H	5V	Data Out			Active
Read (Lower 8 Bit)	L	L	L		Data Out (Lower 8 Bit)	High Impedance	L	
Read (Upper 8 Bit)	L	L	L		Data Out (Upper 8 Bit)	High Impedance	H	
Output Deselect	L	H	H		High Impedance			
			L		High Impedance		*	
Standby	H	*	H		High Impedance			
			L	High Impedance		*		
Program	L	H	12.5V	6.25V	Data In			Active
Program Inhibit	H	H			High Impedance			
Program Verify	*	L			Data Out			

Note: H ... V_{IH}, L ... V_{IL}, * ... V_{IH} or V_{IL}

TC578200D-150, -200

READ MODE

The TC578200D has the $\overline{\text{BYTE}}/\text{V}_{\text{PP}}$ terminal that selects word-wide output and byte-wide output. When $\overline{\text{BYTE}}/\text{V}_{\text{PP}}$ is set to V_{IH} , the word-wide output is selected, and D15/A-1 pin is used for D15 data output.

When $\overline{\text{BYTE}}/\text{V}_{\text{PP}}$ is set to V_{IL} , the byte-wide output is selected, and D15/A-1 pin is used for A-1 address input. When A-1 is set to V_{IL} in this condition, the data output is selected lower 8 bits of the 16 bit data which has been programmed. When A-1 is set to V_{IH} , the data output is selected upper 8 bits.

The TC578200D has two control function. The chip enable ($\overline{\text{CE}}$) controls the operation power and should be used for device selection. The output enable ($\overline{\text{OE}}$) controls the output buffers, independent of device selection. Assuming that $\overline{\text{CE}}=\overline{\text{OE}}=V_{\text{IL}}$, the output data is valid at the outputs after address access time from stabilizing of all addresses. The $\overline{\text{CE}}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}). Assuming that $\overline{\text{CE}}=V_{\text{IL}}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{\text{OE}}$.

OUTPUT DESELECT MODE

Assuming that $\overline{\text{CE}}=V_{\text{IH}}$ or $\overline{\text{OE}}=V_{\text{IH}}$, the outputs will be in a high impedance state. So two or more TC578200D's can be connected together on a common bus line. When $\overline{\text{CE}}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC578200D has a low power standby mode controlled by the $\overline{\text{CE}}$ signal. By applying a high level to the $\overline{\text{CE}}$ input, the TC578200D is placed in the standby mode which reduces the operating current to $100\mu\text{A}$ by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$ input.

PROGRAM MODE

Initially, when recieved by customers, all bits of the TC578200D are in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit location by electrically programming. The TC578200D is in the programming mode when the V_{pp} input is at 12.50V and $\overline{CE}$ is at TTL-Low under $\overline{OE}=V_{IH}$. Data to be programmed must be applied 16 bits in parallel to the data pins.

The TC578200D can be programmed any location at anytime either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ at V_{IL} . The programmed data should be compared with the original word-wide (16 bit) data.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (12.50V) is applied to V_{pp} terminal, a high level $\overline{CE}$ input inhibits the TC578200D from being programmed. Programming of two or more EPROMs in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

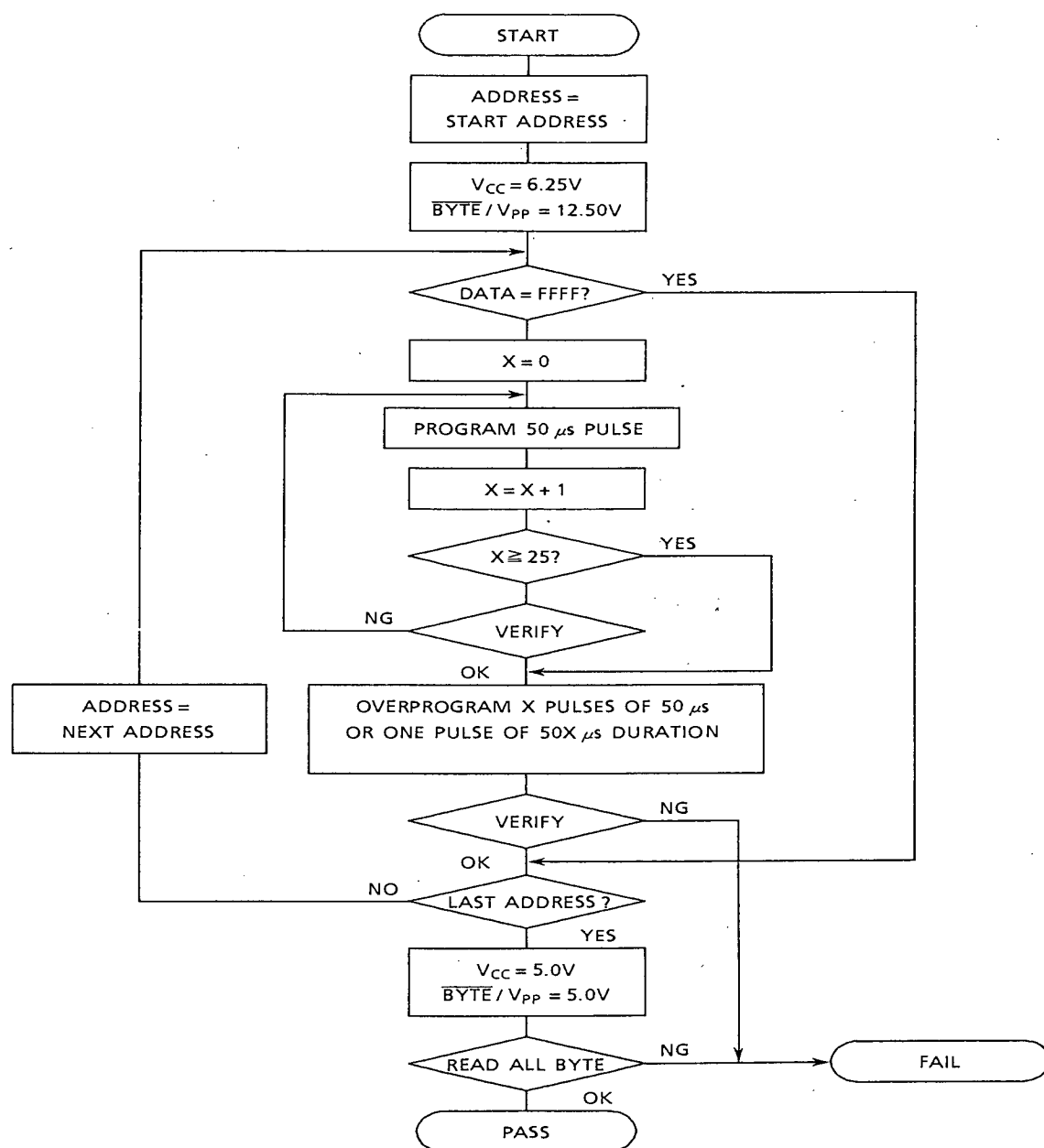
HIGH SPEED PROGRAM MODE

The device is set up the high speed programming mode when the programming voltage (12.50V) is applied to the V_{pp} terminal with $V_{CC}=6.25V$. The programming is achieved by applying a single TTL low level $50\mu s$ pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of $50\mu s$ is applied and then the programmed data is verified. This should be repeated until the program operates correctly(max. 25 times).

After correctly programming the selected address, the overprogram pulse of same length that needed for initial programming should be applied. When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM MODE

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC578200D which identifies its manufacturer and device type. The programming equipment may read out manufacturer code and device code from TC578200D by using this mode before program operation and automatically set program voltage (V_{pp}) and algorithm.

Electric signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to V_{IH} . These two codes possess an odd parity with the parity bit of (D7).

The following table shows electric signature of TC578200D.

SIGNATURE \ PINS	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX DATA
Manufacturer Code	V_{IL}	*	*	*	*	*	*	*	*	1	0	0	1	1	0	0	0	**98
Device Code	V_{IH}	*	*	*	*	*	*	*	*	0	0	0	1	1	1	0	0	**1C

Note: A9 = 12.0V $\pm$ 0.5V

* Don't care

A1 - A8, A10 - A18, $\overline{CE}$, $\overline{OE}$ = V_{IL}

$\overline{BYTE} / V_{PP}$ = V_{IH}

SILICON STACKED GATE MOS INTEGRATED CIRCUIT

TC5716200D-150, -200

16MEGA BIT (1,048,576 WORD $\times$ 16BIT / 2,097,152 WORD $\times$ 8BIT)
CMOS U.V. ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

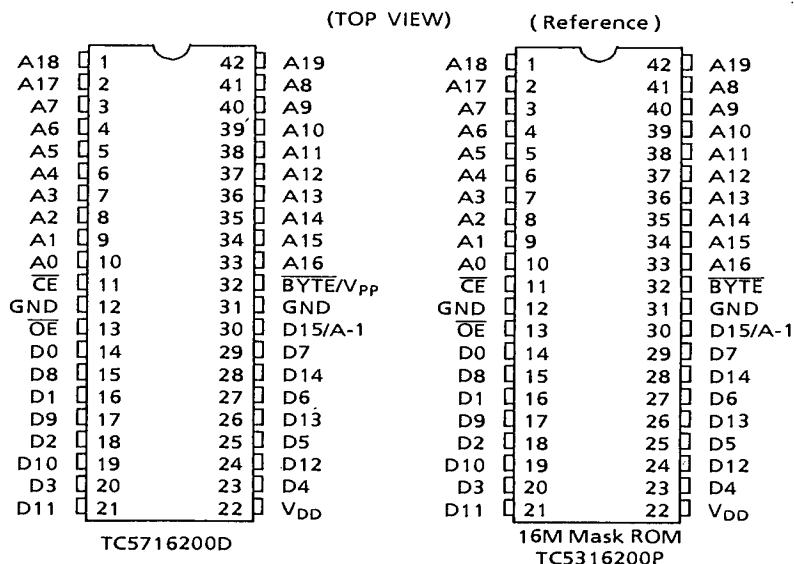
DESCRIPTION

The TC5716200D is a 16,777,216 bit CMOS ultraviolet light erasable and electrically programmable read only memory. It is organized as 1M words by 16 bits or 2M words by 8 bits. The TC5716200D is compatible with 42 pin 16M bit Mask ROM. This product is packed in 42 pin standard cerdip package. The TC5716200D is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and low power features with access time of 150ns/200ns and a maximum operating current of 60mA/6.7MHz. The programming time of the TC5716200D except overhead times of EPROM programmer is only 52 seconds by using the high speed programming algorithm.

FEATURES

- Peripheral circuit : CMOS
- Memory cell : NMOS
- Fast access time
($V_{CC}=5V \pm 10\%$, $T_a=0 \sim 70^\circ C$)
TC5716200D - 150 : 150ns
TC5716200D - 200 : 200ns
- Single 5V power supply
- Low power dissipation
- Standby : $100\mu A$
- Full static operation
- Input and output TTL compatible
- Three state output
- High speed programming operation : tpw 25 μs
- 16M MROM compatible pinout : TC5316200P
- Standard 42 pin DIP cerdip package : WDIP42-G-600B

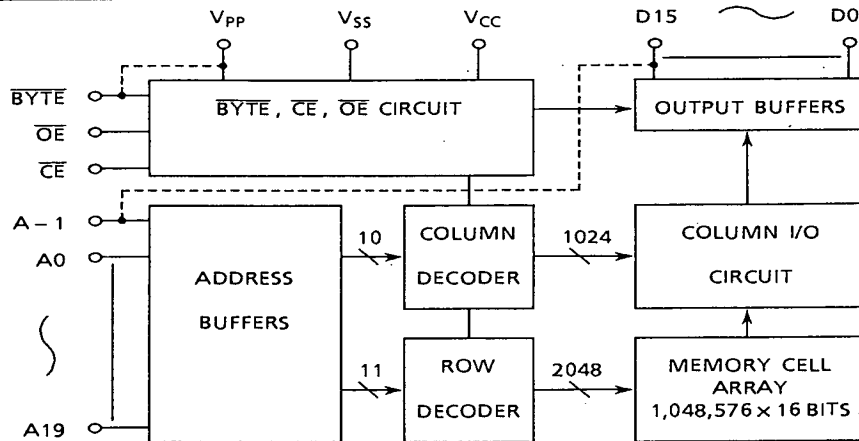
PIN CONNECTION



PIN NAMES

A0~A19	Address Input
D0~D14	Output (Input)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
D15/A-1	Output (Input) / Address Input
$\overline{BYTE}/V_{PP}$	Word, Byte select Input / Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage
V_{SS}	Ground

BLOCK DIAGRAM



MODE SELECTION

MODE \ PINS	$\overline{CE}$	$\overline{OE}$	BYTE / V_{PP}	V_{CC}	D0~D7	D8~D14	D15 / A-1	Power
Read (16 Bit)	L	L	H	5V	Data Out			Active
Read (Lower 8 Bit)	L	L	L		Data Out (Lower 8 Bit)	High Impedance	L	
Read (Upper 8 Bit)	L	L	L		Data Out (Upper 8 Bit)	High Impedance	H	
Output Deselect	L	H	H		High Impedance			
			L		High Impedance	*		
Standby	H	*	H	High Impedance			Standby	
			L	High Impedance	*			
Program	L	H	12.5V	6.25V	Data In			Active
Program Inhibit	H	H			High Impedance			
Program Verify	*	L			Data Out			

Note: H = V_{IH} , L = V_{IL} , * = V_{IH} or V_{IL}

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	- 0.6~7.0	V
V_{PP}	Program Supply Voltage	- 0.6~14.0	V
V_{IN}	Input Voltage	- 0.6~7.0	V
$V_{IN}(A9)$	Input Voltage (A9)	- 0.6~13.5	V
$V_{I/O}$	Input/Output Voltage	- 0.6~ $V_{CC} + 0.5$	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260·10	°C · sec
T_{STRG}	Storage Temperature	- 65~150	°C
T_{OPR}	Operating Temperature	0~70	°C

TC5716200D-150,-200

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage	- 0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.50	5.00	5.50	V

D.C. AND OPERATING CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0V \sim V_{CC}$	—	—	± 10	μA
I_{CCO1}	Operating Current	$\overline{CE} = 0V$ $I_{OUT} = 0\text{mA}$ $f = 6.7\text{MHz}$	—	—	60	mA
I_{CCO2}		$\overline{CE} = 0V$ $I_{OUT} = 0\text{mA}$ $f = 1\text{MHz}$	—	—	30	mA
I_{CCS1}	Standby Current	$\overline{CE} = V_{IH}$	—	—	1	mA
I_{CCS2}		$\overline{CE} = V_{CC} - 0.2V$	—	—	100	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{mA}$	—	—	0.4	V
I_{PP1}	V_{PP} Current	$V_{PP} = 0V \sim V_{CC} + 0.6V$	—	—	± 10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 0.4V \sim V_{CC}$	—	—	± 10	μA

A.C. CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	- 150		- 200		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	—	150	—	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	—	150	—	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	70	—	70	ns
t_{DF1}	$\overline{CE}$ to Output in High Impedance	0	60	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High Impedance	0	60	0	60	ns
t_{OH}	Output Data Hold Time	0	—	0	—	ns
t_{BT}	BYTE to Output Valid	—	150	—	200	ns
t_{BTD}	BYTE to Output in High Impedance	—	70	—	70	ns

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and $CL = 100\text{PF}$
- Input Pulse Rise and Fall Time : 10ns Max
- Input Pulse Levels : 0.45V and 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

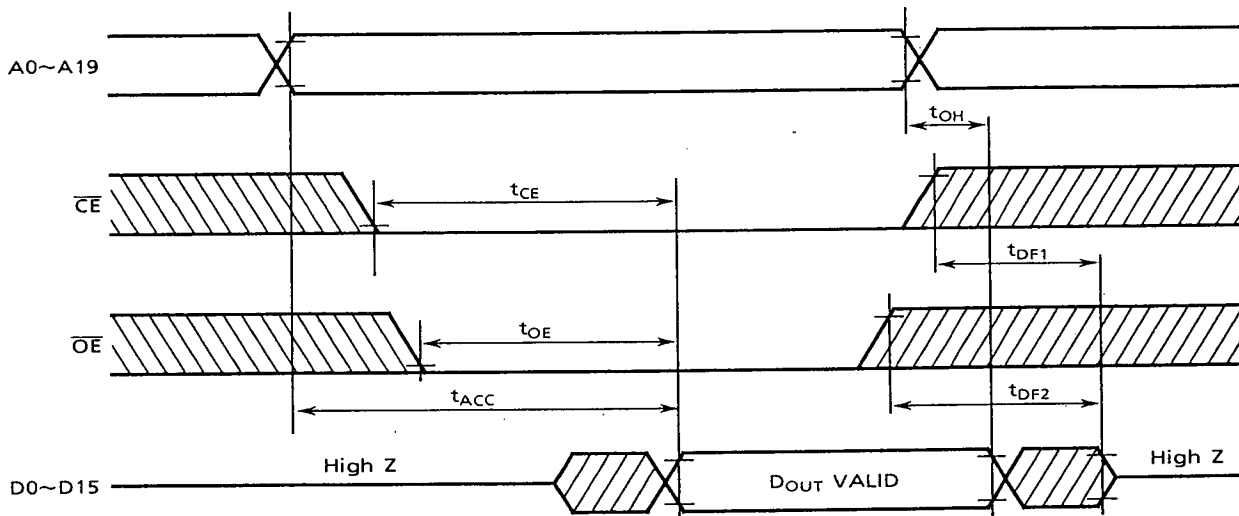
CAPACITANCE * ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance	$V_{IN} = 0\text{V}$	—	6	10	pF
C_{IN2}	Input Capacitance ($\overline{\text{BYTE}} / V_{PP}$)	$V_{IN} = 0\text{V}$	—	110	120	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0\text{V}$	—	10	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS

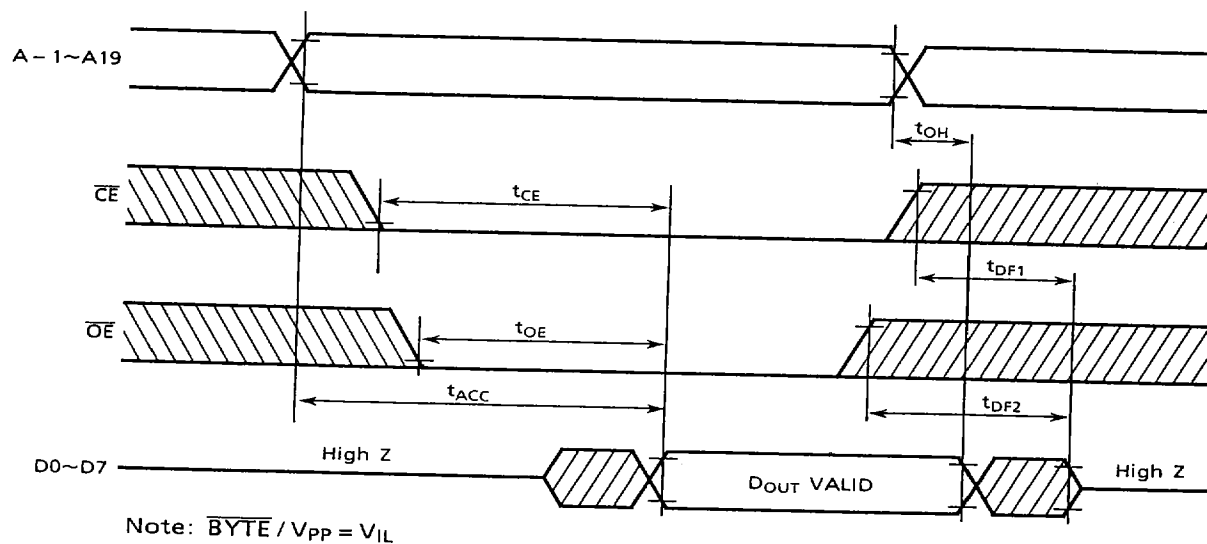
WORD - WIDE READ MODE



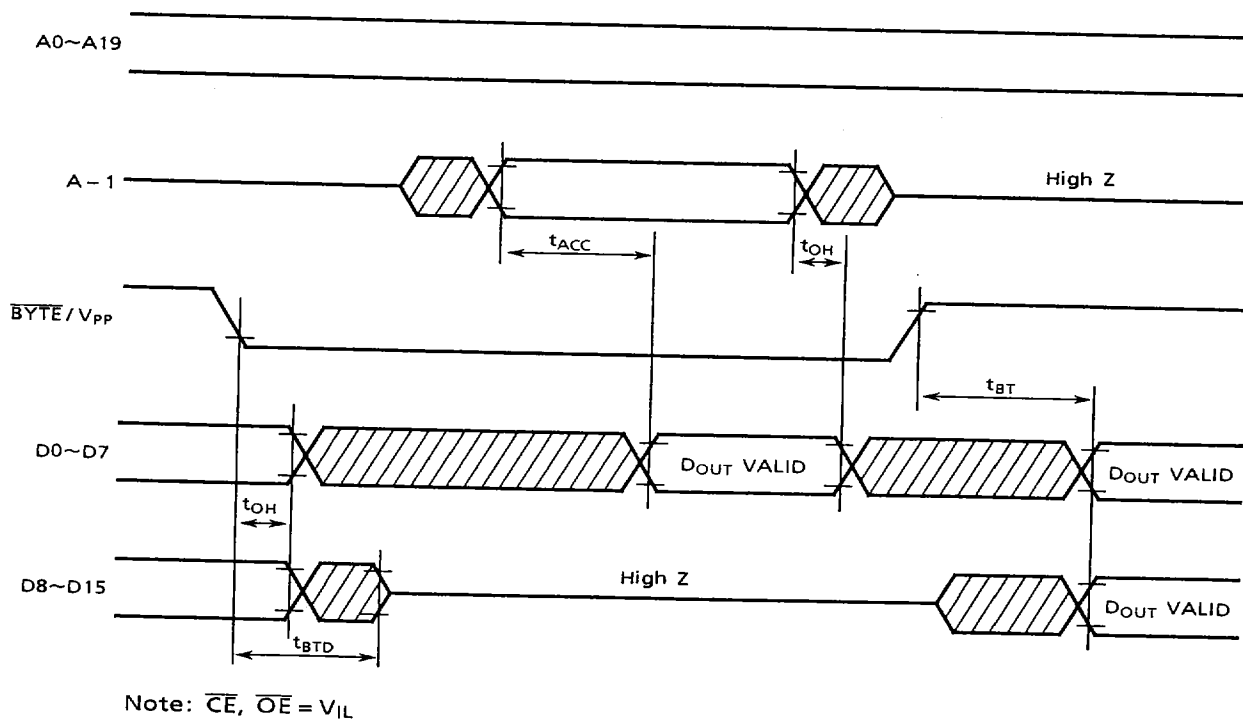
Note: $\overline{\text{BYTE}} / V_{PP} = V_{IH}$

TC5716200D-150, -200

BYTE-WIDE READ MODE



BYTE TRANSITION



HIGH SPEED PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	$V_{CC} + 1.0$	V
V_{IL}	Input Low Voltage	-0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.20	12.50	12.80	V

D.C. AND OPERATING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25 \pm 0.25\text{V}$, $V_{PP} = 12.50 \pm 0.30\text{V}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0\text{V} \sim V_{CC}$	—	—	± 10	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{mA}$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	40	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP} = 12.8\text{V}$	—	—	50	mA

A.C. PROGRAMMING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25 \pm 0.25\text{V}$, $V_{PP} = 12.50 \pm 0.30\text{V}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	0	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	0	—	—	μs
t_{OES}	$\overline{OE}$ Setup Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VPS}	V_{PP} Setup Time	—	2	—	—	μs
t_{VCS}	V_{CC} Setup Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	—	22.5	25	27.5	μs
t_{OPW}	Overprogram Pulse Width	Note 1	22.5	25	27.5	μs
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE} = V_{IH}$	—	—	150	ns
t_{DFP}	$\overline{OE}$ to Output in High Impedance	$\overline{CE} = V_{IH}$	—	—	90	ns

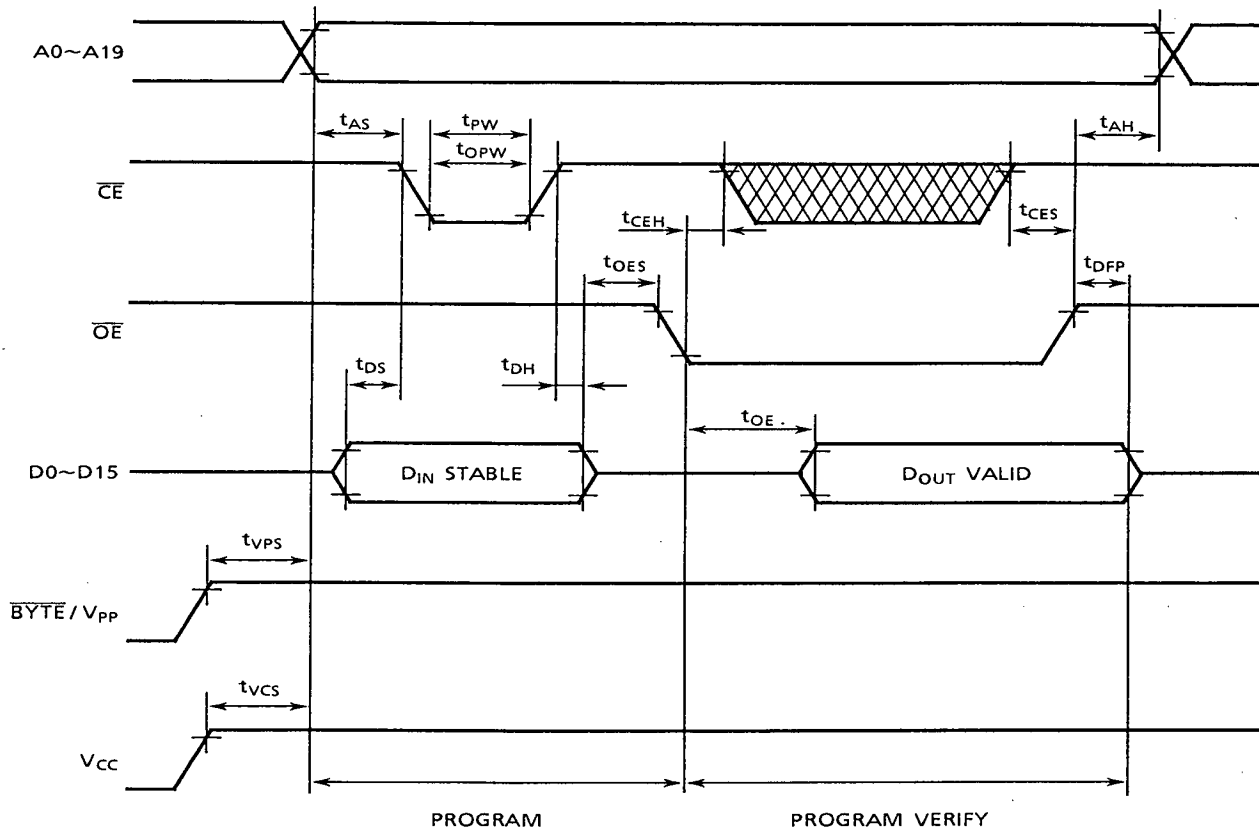
A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and $C_L = 100\text{PF}$
- Input Pulse Rise and Fall Time : 10ns Max
- Input Pulse Levels : 0.45V and 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

Note 1: t_{OPW} depends on the program pulse width which is required in the initial program.

TIMING WAVEFORMS

HIGH SPEED PROGRAM OPERATION



- Note: 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP} .
2. Removing the device from socket and setting the device in socket with $V_{PP}=12.50V$ may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not exceed 14V.

ERASURE CHARACTERISTICS

The TC5716200D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. Then integrated dose (ultraviolet light intensity $[W/cm^2] \times$ exposure time $[sec.]$) for erasure should be a minimum of 15 $[W \cdot sec/cm^2]$.

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps of which ultraviolet light intensity is a 12000 $[\mu W/cm^2]$ will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is $12000 [\mu W/cm^2] \times (20 \times 60) [sec] \approx 15 [W \cdot sec/cm^2]$.)

The TC5716200D's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components.

Therefore when used under such lighting for extended periods of time, the opaque seals - Toshiba EPROM Protect Seal AC907 - are available.

OPERATION INFORMATION

The TC5716200D's eight operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PINS	$\overline{CE}$	$\overline{OE}$	BYTE / V_{PP}	V_{CC}	D0~D7	D8~D14	D15 / A-1	Power
Read (16 Bit)	L	L	H	5V	Data Out			Active
Read (Lower 8 Bit)	L	L	L		Data Out (Lower 8 Bit)	High Impedance	L	
Read (Upper 8 Bit)	L	L	L		Data Out (Upper 8 Bit)	High Impedance	H	
Output Deselect	L	H	H		High Impedance			
			L		High Impedance		*	
Standby	H	*	H		High Impedance		Standby	
			L	High Impedance		*		
Program	L	H	12.5V	6.25V	Data In			Active
Program Inhibit	H	H			High Impedance			
Program Verify	*	L			Data Out			

Note: H = V_{IH} , L = V_{IL} , * = V_{IH} or V_{IL}

TC5716200D-150, -200

READ MODE

The TC5716200D has the $\overline{\text{BYTE}}/\text{V}_{\text{PP}}$ terminal that selects word-wide output or byte-wide output. When $\overline{\text{BYTE}}/\text{V}_{\text{PP}}$ is set to V_{IH} , the word-wide output is selected, and D15/A-1 pin is used for D15 data output.

When $\overline{\text{BYTE}}/\text{V}_{\text{PP}}$ is set to V_{IL} , the byte-wide output is selected, and D15/A-1 pin is used for A-1 address input. When A-1 is set to V_{IL} in this condition, lower 8 bits of the 16 bit data which has been programmed are selected. When A-1 is set to V_{IH} , upper 8 bits are selected.

The TC5716200D has two control functions. The chip enable ($\overline{\text{CE}}$) controls the operation power and should be used for device selection. The output enable ($\overline{\text{OE}}$) controls the output buffers, independent of device selection. Assuming that $\overline{\text{CE}} = \overline{\text{OE}} = V_{\text{IL}}$, the output data is valid at the outputs after address access time from stabilizing of all addresses. The $\overline{\text{CE}}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}). Assuming that $\overline{\text{CE}} = V_{\text{IL}}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{\text{OE}}$.

OUTPUT DESELECT MODE

Assuming that $\overline{\text{CE}} = V_{\text{IH}}$ or $\overline{\text{OE}} = V_{\text{IH}}$, the outputs will be in a high impedance state. So two or more TC5716200D's can be connected together on a common bus line. When $\overline{\text{CE}}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC5716200D has a low power standby mode controlled by the $\overline{\text{CE}}$ signal. By applying a high level to the $\overline{\text{CE}}$ input, the TC5716200D is placed in the standby mode which reduces the operating current to $100\mu\text{A}$ by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$ input.

PROGRAM MODE

Initially, when recieved by customers, all bits of the TC5716200D are in the "1" state which is erased state. Therefore the program operation is to introduce "0" data into the desired bit location by electrically programming. The TC5716200D is in the programming mode when the V_{pp} input is at 12.50V and $\overline{CE}$ is at TTL-Low under $\overline{OE}=V_{IH}$. Data to be programmed must be applied 16 bits in parallel to the data pins.

Data can be programmed in any locations at anytime either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ at V_{IL} . The programmed data should be compared with the original word-wide (16 bit) data.

PROGRAM INHIBIT MODE

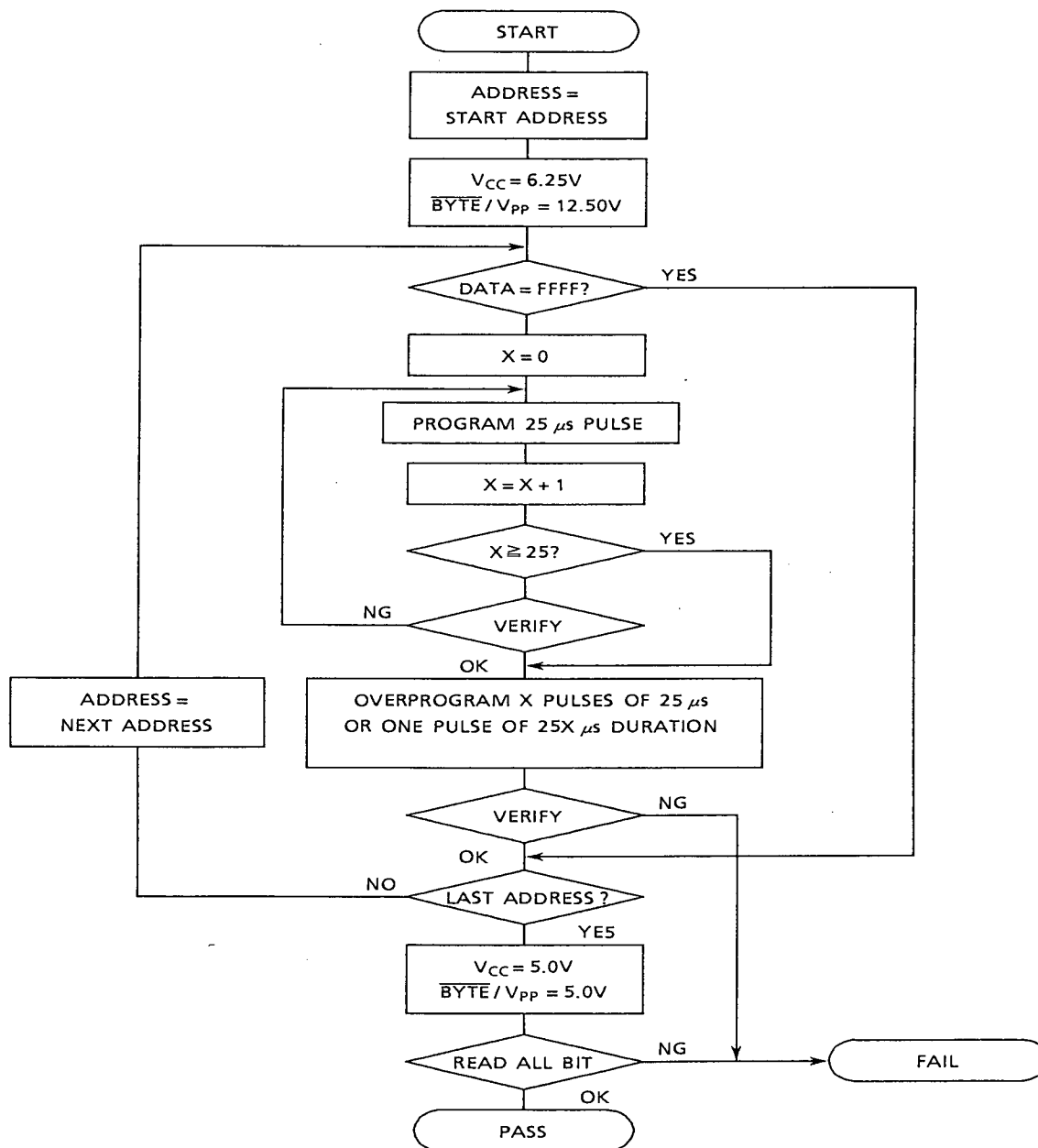
Under the condition that the program voltage (12.50V) is applied to V_{pp} terminal, a high level $\overline{CE}$ input inhibits the TC5716200D from being programmed. Programming of two or more EPROMs in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM MODE

The device is subjected to the high speed programming mode when the programming voltage (12.50V) is applied to the V_{pp} terminal with $V_{CC}=6.25V$. The programming is achieved by applying a single TTL low level $25\mu s$ pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, one more program pulse of $25\mu s$ is applied and then the programmed data is verified. This should be repeated until the program operates correctly(max. 25 times).

After correctly programming the selected address, the overprogram pulse of same length that needed for initial programming should be applied. When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM MODE
FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC5716200D which identifies its manufacturer and device type. The programming equipment may read out manufacturer code and device code from TC5716200D by using this mode before program operation and automatically set program voltage (V_{pp}) and algorithm.

Electric signature mode is set up when 12V is applied to address line A9 and the rest of address lines are set to V_{IL} in read operation. Data output in this condition is manufacturer code.

Device code is identified when address A0 is set to V_{IH} . These two codes possess an odd parity with the parity bit of (D7).

The following table shows electric signature of TC5716200D.

SIGNATURE	PINS																	HEX DATA
	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
Manufacturer Code	V_{IL}	*	*	*	*	*	*	*	*	1	0	0	1	1	0	0	0	**98
Device Code	V_{IH}	*	*	*	*	*	*	*	*	0	0	0	1	1	0	1	0	**1A

Note: A1 – A8, A10 – A19, $\overline{CE}$, $\overline{OE} = V_{IL}$, A9 = 12V $\pm$ 0.5V
 $\overline{BYTE}/V_{PP} = V_{IH}$
 * Don't care

4-2 ONE TIME PROM

TC54256AP/AF

32,768 WORD x 8 BIT COMS ONE TIME PROGRAMMABLE READ ONLY MEMORY

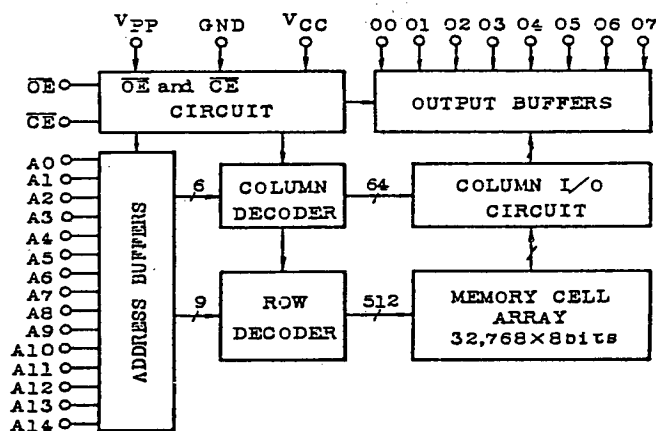
DESCRIPTION

The TC54256AP/AF is a 32,768 word x 8 bit one time programmable read only memory, and molded in a 28 pin plastic package. The TC54256AP/AF's access time is 200ns and has low power standby mode which reduces the power dissipation without increasing access time. The electrical characteristics and programming method are the same as U.V. EPROM TC57256AD's. Once programmed, the TC54256AP/AF can not be erased because of using plastic DIP without transparent window.

FEATURES

- Peripheral circuit: CMOS
- Memory cell : N-MOS
- Low power dissipation
 - Active : 30mA/6.7MHz
 - Standby: 100µA
- Fast access time: 200ns
- Single 5V power supply
- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with ROM TC53257P, TMM23256P, EPROM TMM27256D/AD, TC57256D/AD, One time PROM TMM24256P/AP and TC54256P
- TC54256AP: DIP28-P-600
- TC54256AF: SOP28-P-450

BLOCK DIAGRAM



PIN CONNECTION (TOP VIEW)

VPP	1	28	VCC
A12	2	27	A14
A7	3	26	A13
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
A3	7	22	OE
A2	8	21	A10
A1	9	20	CE
A0	10	19	07
00	11	18	06
01	12	17	05
02	13	16	04
GND	14	15	03

PIN NAMES

A0 ~ A14	Address Inputs
00 ~ 07	Outputs (Inputs)
CE	Chip Enable Input
OE	Output Enable Input
VPP	Program Supply Voltage
VCC	VCC Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE	PIN	CE (20)	OE (22)	VPP (1)	VCC (28)	00 ~ 07 (11 ~ 13, 15 ~ 19)	POWER
Read		L	L	5V	5V	Data Out	Active
Output Deselect		*	H			High Impedance	
Standby		H	*			High Impedance	
Program		L	H	12.5V	6V	Data In	Active
Program Inhibit		H	H			High Impedance	
Program Verify		*	L			Data Out	

*: H or L

TC54256AP/AF

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{CC}	V _{CC} Power Supply Voltage	-0.6 ~ 7.0	V
V _{PP}	Program Supply Voltage	-0.6 ~ 14.0	V
V _{IN}	Input Voltage	-0.6 ~ 7.0	V
V _{I/O}	Input/Output Voltage	-0.6 ~ V _{CC} +0.5	V
P _D	Power Dissipation	1.5	W
T _{SOLDER}	Soldering Temperature Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-65 ~ 125	°C
TOPR	Operating Temperature	-40 ~ 85	°C

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{IH}	Input High Voltage	2.2	-	V _{CC} +0.3	V
V _{IL}	Input Low Voltage	-0.3	-	0.8	
V _{CC}	V _{CC} Power Supply Voltage	4.75	5.00	5.25	
V _{PP}	V _{PP} Power Supply Voltage	V _{CC} -0.6	V _{CC}	V _{CC} +0.6	

D.C. and OPERATING CHARACTERISTICS (T_a=-40 ~ 85°C, V_{CC}=5V±5%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Current	V _{IN} =0V ~ V _{CC}	-	-	±10	μA
I _{CC01}	Operating Current	$\overline{CE}$ =0V f=6.7MHz	-	-	30	mA
I _{CC02}			-	-	10	
I _{CCS1}	Standby Current	$\overline{CE}$ =V _{IH}	-	-	1	mA
I _{CCS2}		$\overline{CE}$ =V _{CC} -0.2V	-	-	100	μA
V _{OH}	Output High Voltage	I _{OH} =-400μA	2.4	-	-	V
V _{OL}	Output Low Voltage	I _{OL} =2.1mA	-	-	0.4	V
I _{PP1}	V _{PP} Current	V _{PP} =V _{CC} ±0.6V	-	-	±10	μA
I _{LO}	Output Leakage Current	V _{OUT} =0.4V ~ V _{CC}	-	-	±10	μA

A.C. CHARACTERISTICS ($T_a = -40 \sim 85^\circ\text{C}$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = V_{CC} \pm 0.6V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
t_{ACC}	Address Access Time	$\overline{CE} = \overline{OE} = V_{IL}$	-	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE} = V_{IL}$	-	200	
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE} = V_{IL}$	-	70	
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE} = V_{IL}$	0	60	
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE} = V_{IL}$	0	60	
t_{OH}	Output Data in Hold Time	$\overline{CE} = \overline{OE} = V_{IL}$	0	-	

A.C. TEST CONDITIONS

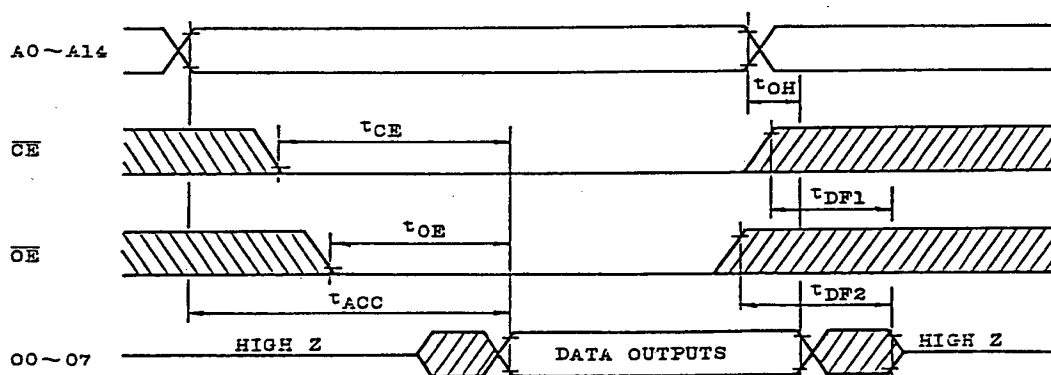
- Output Load : 1 TTL Gate and $C_L = 100\text{pF}$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ~ 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE * ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0V$	-	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	-	8	12	

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



TC54256AP/AF

PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{IH}	Input High Voltage	2.2	-	V _{CC} +1.0	V
V _{IL}	Input Low Voltage	-0.3	-	0.8	
V _{CC}	V _{CC} Power Supply Voltage	5.75	6.0	6.25	
V _{PP}	V _{PP} Power Supply Voltage	12.0	12.5	13.0	

D.C. and OPERATING CHARACTERISTICS (T_a=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Current	V _{IN} =0 ~ V _{CC}	-	-	±10	μA
V _{OH}	Output High Voltage	I _{OH} =-400μA	2.4	-	-	V
V _{OL}	Output Low Voltage	I _{OL} =2.1mA	-	-	0.4	V
I _{CC}	V _{CC} Supply Current	-	-	-	40	mA
I _{PP2}	V _{PP} Supply Current	V _{PP} =13.0V	-	-	50	mA
V _{ID}	A9 Auto Select Voltage	-	11.5	12.0	12.5	V

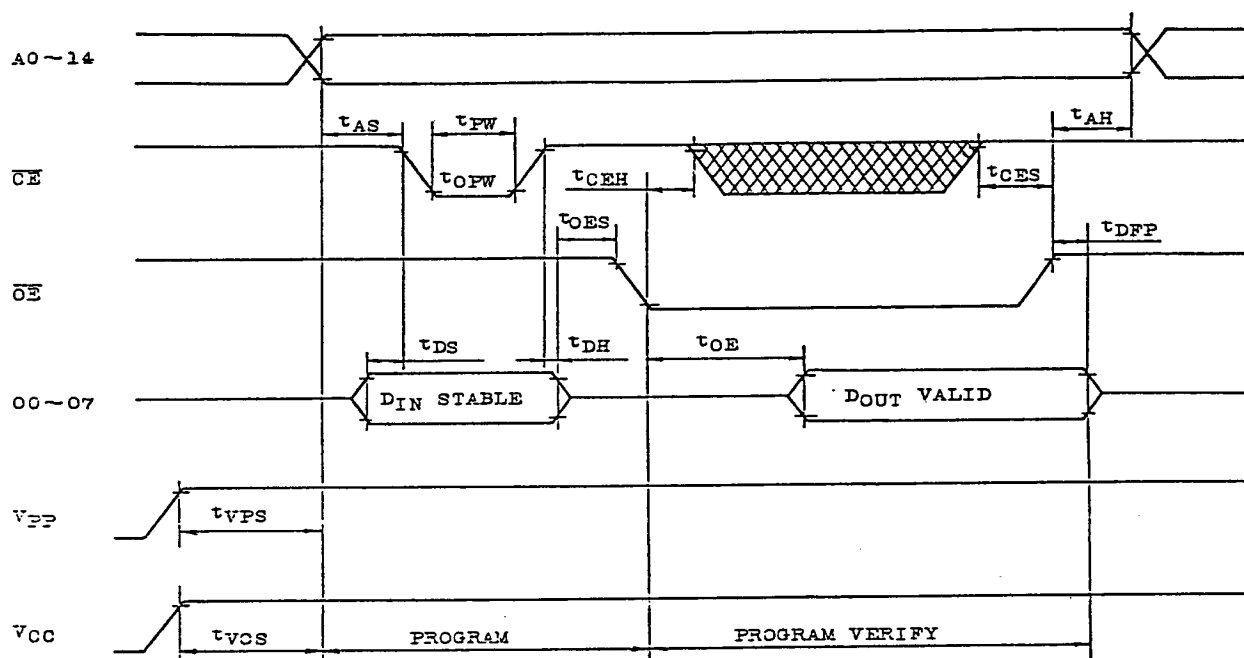
A.C. PROGRAMMING CHARACTERISTICS (T_a=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t _{AS}	Address Setup Time	-	2	-	-	μs
t _{AH}	Address Hold Time	-	2	-	-	μs
t _{CES}	$\overline{CE}$ Setup Time	-	0	-	-	ns
t _{CEH}	$\overline{CE}$ Hold Time	-	0	-	-	ns
t _{OES}	$\overline{OE}$ Setup Time	-	2	-	-	μs
t _{DS}	Data Setup Time	-	2	-	-	μs
t _{DH}	Data Hold Time	-	2	-	-	μs
t _{VPS}	V _{PP} Setup Time	-	2	-	-	μs
t _{VCS}	V _{CC} Setup Time	-	2	-	-	μs
t _{PW}	Initial Program Pulse Width	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{IH}$	0.95	1	1.05	ms
t _{OPW}	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t _{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IH}$	-	-	150	ns
t _{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IH}$	-	-	130	ns

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ~ 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.



2. Removing the device from socket and setting the device in socket with $V_{pp}=12.5V$ may cause permanent damage to the device.
3. The V_{pp} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{pp} terminal. When the switching pulse voltage is applied to the V_{pp} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

TC54256AP/AF

OPERATION INFORMATION

The TC54256AP/AF's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE	PIN NAMES (NUMBER)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	00 ~ 07 (11 ~ 13, 15 ~ 19)	POWER
Read Operation ($T_a = -40 \sim 85^\circ\text{C}$)	Read	L	L	5V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	
	Standby	H	*			High Impedance	Standby
Program Operation ($T_a = 25 \pm 5^\circ\text{C}$)	Program	L	H	12.5V	6V	Data In	Active
	Program Inhibit	H	H			High Impedance	
	Program Verify	*	L			Data Out	

Note: H; V_{IH} , L; V_{IL} , *; V_{IH} or V_{IL}

READ MODE

The TC54256AP/AF has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection. The output enable ($\overline{OE}$) controls the output buffers, independent of device selection. Assuming that $\overline{CE} = \overline{OE} = V_{IL}$, the output data is valid at the outputs after address access time from stabilizing of all addresses. The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}). Assuming that $\overline{CE} = V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$, the outputs will be in a high impedance state. So two or more TC54256AP/AF's can be connected together on a common bus line. When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC54256AP/AF has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC54256AP/AF is placed in the standby mode which reduce the operating current to 100 μ A by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC54256AP/AF are in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming. The TC54256AP/AF is in the programming mode when the V_{pp} input is at 12.5V and $\overline{CE}$ is at TTL-Low level under $\overline{OE}=V_{IH}$. The TC54256AP/AF can be programmed any location at anytime either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with $\overline{OE}$ at V_{IL} and $\overline{CE}$ at V_{IH} or V_{IL} .

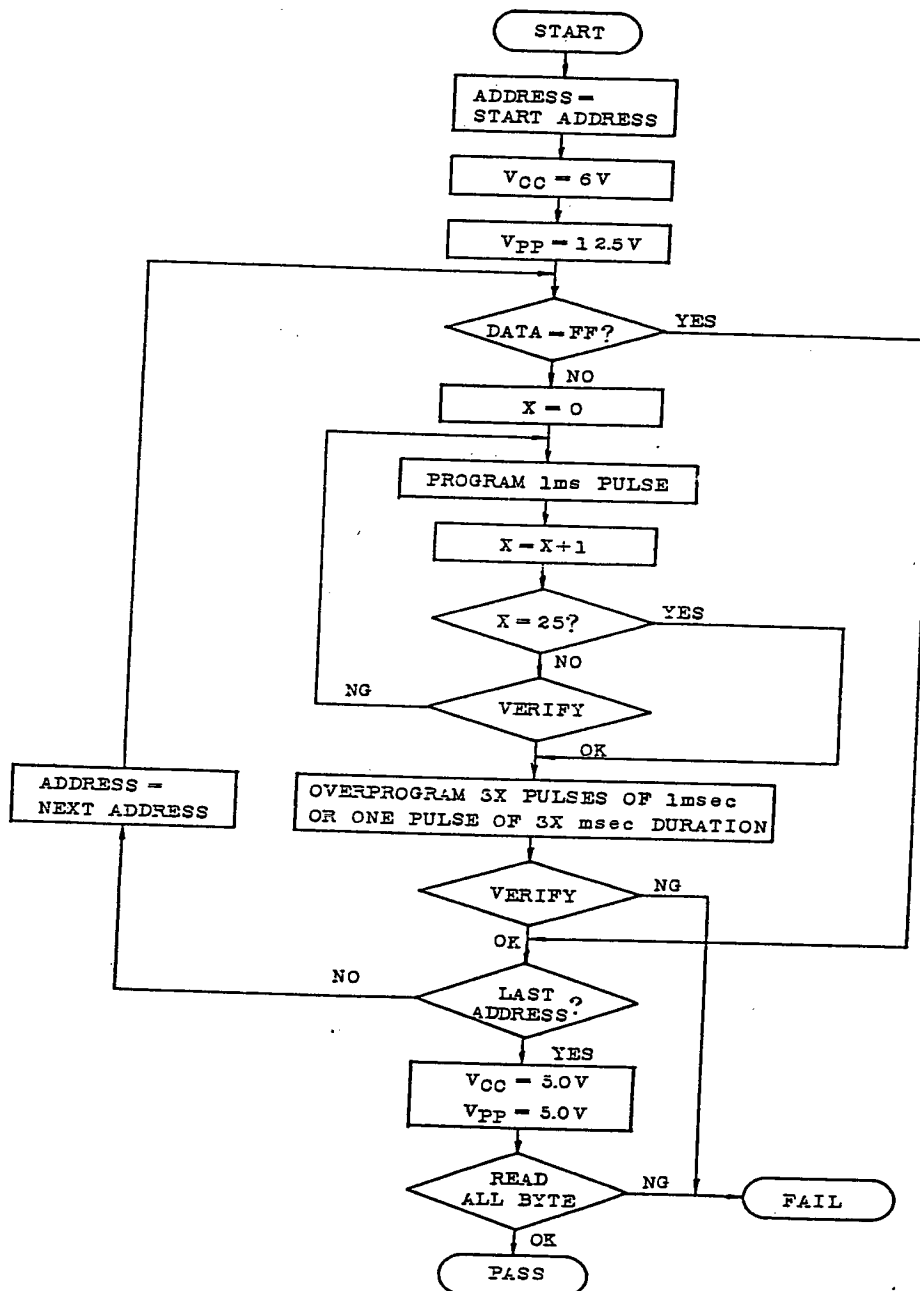
PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{pp} terminal, a TTL high level $\overline{CE}$ input inhibits the TC54256AP/AF from being programmed. Programming of two or more TC54256AP/AF's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a TTL Low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{pp} terminal with $V_{CC}=6V$. The programming is achieved by applying a single TTL low level lms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of lms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times). After correctly programming the selected address, the additional program pulse with width of 3 times more than that needed for initial programming is applied. When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{pp}=5V$.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC54256AP/AF which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TC54256AP/AF by using this mode before program operation and automatically set program voltage (V_{pp}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH} . These two codes possess an odd parity with the parity bit of MSB (07). The following table shows electric signature of TC54256AP/AF.

PINS SIGNATURE	A0 (10)	07 (19)	06 (18)	05 (17)	04 (16)	03 (15)	02 (13)	01 (12)	00 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	1	0	0	0	1	0	0	C4

Notes: A9=12V±0.5V

A1 ~ A8, A10 ~ A14, $\overline{CE}$, $\overline{OE}=V_{IL}$

TC54512AP/AF-15, -20

65,536 WORDS x 8 BITS CMOS ONE TIME PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The TC54512AP/AF is a 65,536 word x 8 bit CMOS one time programmable read only memory, and molded in a 28 pin plastic package. For read operation, the TC54512AP/AF's access time is 150ns/200ns, and the TC54512AP/AF operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input. Advanced CMOS technology reduces the maximum active current to 30mA/5.9MHz and standby current to 100 μ A. The electrical characteristics and programming method are the same as U.V. EPROM TC57512AD's. Once programmed, the TC54512AP/AF can not be erased because of using plastic DIP without transparent window.

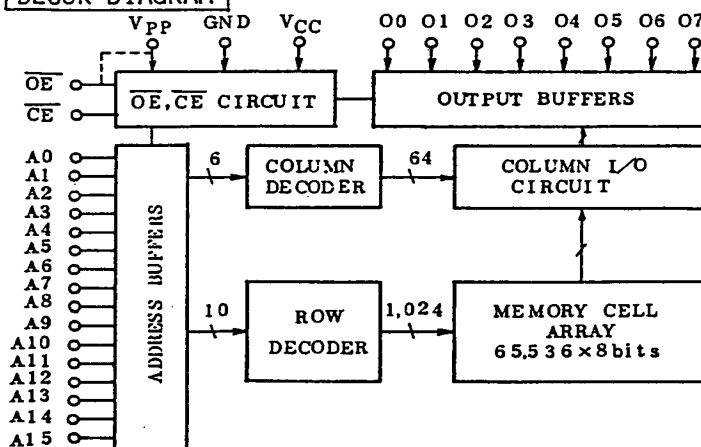
FEATURES

- Peripheral circuit: CMOS
- Memory cell : N-MOS
- Fast access time:
 - TC54512AP/AF-15 150ns
 - TC54512AP/AF-20 200ns
- Low power dissipation
 - Active : 30mA/5.9MHz
 - Standby: 100 μ A
- Full static operation
- High speed programming mode I, II
- Inputs and outputs TTL compatible
- TC54512AP :DIP28-P-600
- TC54512AF :SOP28-P-450

PIN CONNECTION (TOP VIEW)

A15	1	28	V _{CC}
A12	2	27	A14
A7	3	26	A13
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
A3	7	22	OE/V _{PP}
A2	8	21	A10
A1	9	20	CE
A0	10	19	O7
O0	11	18	O6
O1	12	17	O5
O2	13	16	O4
GND	14	15	O3

BLOCK DIAGRAM



PIN NAMES

A0 ~ A15	Address Inputs
O0 ~ O7	Outputs (Inputs)
CE	Chip Enable Input
OE/V _{PP}	Output Enable / Program Supply Voltage Input
V _{CC}	Power Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE	PIN	CE (20)	OE/V _{PP} (22)	V _{CC} (28)	O0 ~ O7 (11 ~ 13, 15 ~ 19)	POWER
Read		L	L	5V	Data Out	Active
Output Deselect		*	H		High Impedance	
Standby		H	*		High Impedance	Standby
Program		L	V _{PP}	6V ¹⁾	Data In	
Program Inhibit		H	V _{PP}	2)	High Impedance	Active
Program Verify		L	L	6.25V	Data Out	

*: H or L 1): HIGH SPEED PROGRAMMING MODE I
2): HIGH SPEED PROGRAMMING MODE II

TC54512AP/AF-15, -20

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{CC}	V _{CC} Power Supply Voltage	-0.6 ~ 7.0	V
V _{PP}	Program Supply Voltage	-0.6 ~ 14.0	V
V _{IN}	Input Voltage	-0.6 ~ 7.0	V
V _{I/O}	Input/Output Voltage	-0.6 ~ V _{CC} +0.5	V
P _D	Power Dissipation	1.5	W
T _{SOLDER}	Soldering Temperature·Time	260 · 10	°C·sec
T _{STG}	Storage Temperature	-65 ~ 125	°C
T _{OPR}	Operating Temperature	-40 ~ 85	°C

READ OPERATION

D.C. AND A.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC54512AP/AF-15/TC54512AP/AF-20
T _a	Operating Temperature	-40 ~ 85°C
V _{CC}	V _{CC} Power Supply Voltage	5V±5%

D.C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Current	V _{IN} =0 ~ V _{CC}	-	-	±10	μA
I _{LO}	Output Leakage Current	V _{OUT} =0.4 ~ V _{CC}	-	-	±10	μA
I _{CCO1}	Operating Current	$\overline{CE}=0V$ f=5.9MHz	-	-	30	mA
I _{CCO2}		I _{OUT} =0mA f=1MHz	-	-	15	
I _{CCS1}	Standby Current	$\overline{CE}=V_{IH}$	-	-	1	mA
I _{CCS2}		$\overline{CE}=V_{CC}-0.2V$	-	-	100	
V _{IH}	Input High Voltage	-	2.2	-	V _{CC} +0.3	V
V _{IL}	Input Low Voltage	-	-0.3	-	0.8	V
V _{OH}	Output High Voltage	I _{OH} =-400μA	2.4	-	-	V
V _{OL}	Output Low Voltage	I _{OL} =2.1mA	-	-	0.4	V
I _{PPI}	V _{PP} Current	V _{PP} =0 ~ V _{CC} +0.6	-	-	±10	μA

TC54512AP/AF-15, -20

A.C. CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	TC54512AP/AF-15		TC54512AP/AF-20		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE}=\overline{OE}=V_{IL}$	-	150	-	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}=V_{IL}$	-	150	-	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IL}$	-	70	-	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}=V_{IL}$	0	60	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IL}$	0	60	0	60	ns
t_{OH}	Output Data Hold Time	$\overline{CE}=\overline{OE}=V_{IL}$	0	-	0	-	ns

A.C. TEST CONDITIONS

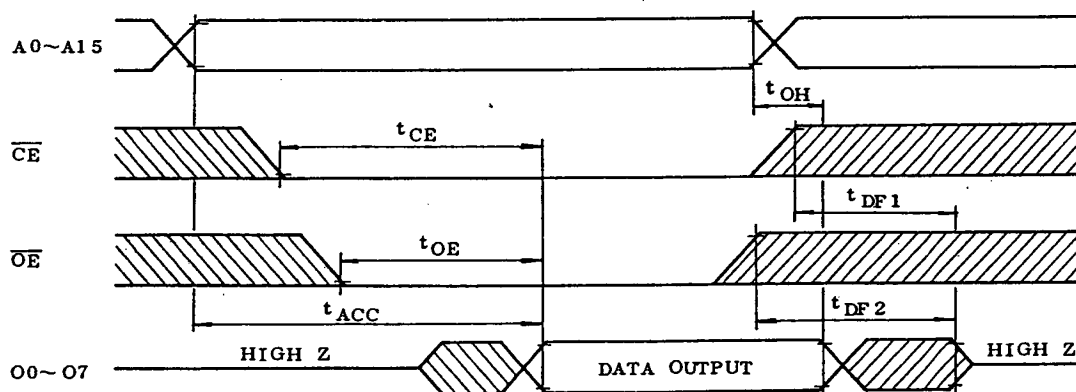
Output Load : 1 TTL Gate and $C_L=100pF$
Input Pulse Rise and Fall Times : 10ns Max.
Input Pulse Levels : 0.45V ~ 2.4V
Timing Measurement Reference Level: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE *($T_a=25^\circ C$, $f=1MHz$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance	$V_{IN}=0V$	-	4	6	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	$V_{IN}=0V$	-	50	60	pF
C_{OUT}	Output Capacitance	$V_{OUT}=V$	-	8	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS



TC54512AP/AF-15,-20

HIGH SPEED PROGRAM MODE I

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{CC}	VCC Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	Vpp Power Supply Voltage	12.0	12.5	13.0	V

DC and OPERATING CHARACTERISTICS ($T_a=25\pm5^\circ\text{C}$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0 \sim V_{CC}$	-	-	± 10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu\text{A}$	2.4	-	-	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1\text{mA}$	-	-	0.4	V
I_{CC}	VCC Supply Current	-	-	-	30	mA
I_{PP2}	Vpp Supply Current	$V_{PP}=13.0V$	-	-	50	mA

AC PROGRAMMING CHARACTERISTICS ($T_a=25\pm5^\circ\text{C}$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time	-	2	-	-	μs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time	-	2	-	-	μs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time	-	50	-	-	ns
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time	-	2	-	-	μs
t_{VCS}	VCC Setup Time	-	2	-	-	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}=V_{IL}$, $\overline{OE}/V_{PP}=V_{PP}$	0.95	1.0	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3.0	78.75	ms
t_{DV}	Data Valid from $\overline{CE}$	$\overline{OE}/V_{PP}=V_{IL}$	-	-	1	μs
t_{DF}	$\overline{CE}$ to Output in High-Z	$\overline{OE}/V_{PP}=V_{IL}$	-	-	130	ns

AC TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V $\sim$ 2.4V
- Timing Measurement Reference Level: Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

TC54512AP/AF-15, -20

HIGH SPEED PROGRAM MODE II

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{IH}	Input High Voltage	2.2	-	V _{CC} +1.0	V
V _{IL}	Input Low Voltage	-0.3	-	0.8	V
V _{CC}	V _{CC} Power Supply Voltage	6.0	6.25	6.5	V
V _{PP}	V _{PP} Power Supply Voltage	12.5	12.75	13.0	V

DC and OPERATING CHARACTERISTICS (T_a=25±5°C, V_{CC}=6.25V±0.25V, V_{PP}=12.75V±0.25V)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Current V _{IN} =0 ~ V _{CC}	-	-	±10	μA
V _{OH}	Output High Voltage V _{OH} =-400μA	2.4	-	-	V
V _{OL}	Output Low Voltage I _{OL} =2.1mA	-	-	0.4	V
I _{CC}	V _{CC} Supply Current	-	-	30	mA
I _{PP2}	V _{PP} Supply Current V _{PP} =13.0V	-	-	50	mA

AC PROGRAMMING CHARACTERISTICS (T_a=25±5°C, V_{CC}=6.25V±0.25V, V_{PP}=12.75V±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t _{AS}	Address Setup Time	-	2	-	-	μs
t _{AH}	Address Hold Time	-	2	-	-	μs
t _{OES}	$\overline{OE}/V_{PP}$ Setup Time	-	2	-	-	μs
t _{OEh}	$\overline{OE}/V_{PP}$ Hold Time	-	2	-	-	μs
t _{PRI}	$\overline{OE}/V_{PP}$ Pulse Rise Time	-	50	-	-	ns
t _{DS}	Data Setup Time	-	2	-	-	μs
t _{DH}	Data Hold Time	-	2	-	-	μs
t _{VR}	$\overline{OE}/V_{PP}$ Recovery Time	-	2	-	-	μs
t _{VCS}	V _{CC} Setup Time	-	2	-	-	μs
t _{PW}	Program Pulse Width	$\overline{CE}=V_{IL}$, $\overline{OE}/V_{PP}=V_{PP}$	0.095	0.1	0.105	ms
t _{DV}	Data Valid from $\overline{CE}$	$\overline{OE}/V_{PP}=V_{IL}$	-	-	1	μs
t _{DF}	$\overline{CE}$ to Output in High-Z	$\overline{OE}/V_{PP}=V_{IL}$	-	-	130	ns

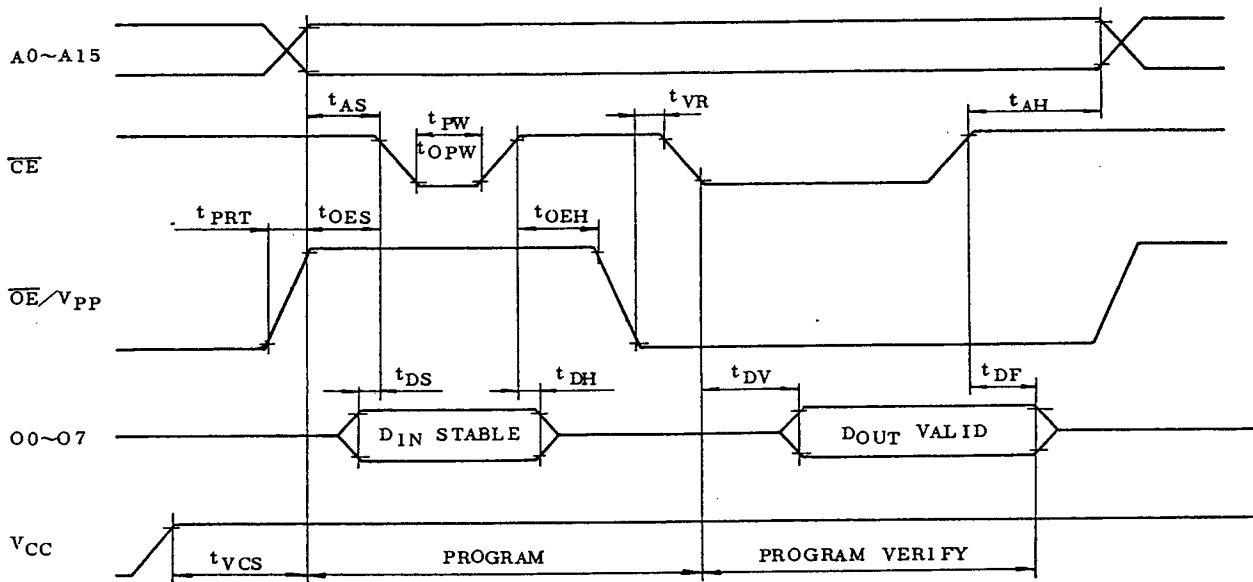
AC TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ~ 2.4V
- Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAMMING MODE I ($V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

HIGH SPEED PROGRAMMING MODE II ($V_{CC}=6.25V\pm0.25V$, $V_{PP}=12.75V\pm0.25V$)



Note 1. V_{CC} must be applied simultaneously or before V_{pp} and cut off simultaneously or after V_{pp} .

2. Removing the device from socket and setting the device in socket with $V_{pp}=12.5\pm0.5V$ or $V_{pp}=12.75\pm0.25V$ may cause permanent damage to the device.
3. The V_{pp} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{pp} terminal. When the switching pulse voltage is applied to the V_{pp} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

TC54512AP/AF-15, -20

OPERATION INFORMATION

The TC54512AP/AF's six operation modes are listed in the following table.
Mode selection can be achieved by applying TTL level signal to all inputs.

PIN NAMES (NUMBER)		$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	V_{CC} (28)	00 ~ 07 (11 ~ 13, 15 ~ 19)	POWER
Read Operation ($T_a = -40 \sim 85^\circ\text{C}$)	Read	L	L	5V	Data Out	Active
	Output Deselect	*	H		High Impedance	
	Standby	H	*		High Impedance	Standby
Program Operation ($T_a = 25 \pm 5^\circ\text{C}$)	Program	L	V_{PP}	6V ¹⁾	Data In	Active
	Program Inhibit	H	V_{PP}	2)	High Impedance	
	Program Verify	L	L	6.25V	Data Out	

Note: H; V_{IH} , L; V_{IL} , *: V_{IH} or V_{IL}

1); HIGH SPEED PROGRAMMING MODE I
2); HIGH SPEED PROGRAMMING MODE II

READ MODE

The TC54512AP/AF has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection. The output enable ($\overline{OE}$) control the output buffers, independent of device selection. Assuming that $\overline{CE} = \overline{OE} = V_{IL}$, the output data is valid at the outputs after address access time from stabilizing of all addresses. The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}). Assuming that $\overline{CE} = V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state. So two or more TC54512AP/AF's can be connected together on a common bus line. When $\overline{CE}$ is decode for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC54512AP/AF has a low power standby mode controlled by the CE signal. By applying a high level to the $\overline{CE}$ input, the TC54512AP/AF is placed in the standby mode which reduce the operating current to 100 μ A by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC54512AP/AF are in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming. The TC54512AP/AF is in the programming mode when the $\overline{OE}/V_{pp}$ input is at 12.5V or 12.75V and $\overline{CE}$ is at TTL-Low level. The TC54512AP/AF can be programmed any location at any time either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with $\overline{OE}/V_{pp}$ at V_{IL} and $\overline{CE}$ at V_{IL} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V or +12.75V) is applied to V_{pp} terminal, a high level $\overline{CE}$ input inhibits the TC54512AP/AF from being programmed. Programming of two or more TC54512AP/AF's in parallel with different data is easily accomplished. That is, all inputs except for CE may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM MODE I

This high speed programming mode I is performed at $V_{CC}=6.0V$ and $\overline{OE}/V_{PP}=12.5V$.

The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with 3 times that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC}=5V$.

HIGH SPEED PROGRAM MODE II

The program time can be greatly decreased by using this high speed programming mode II. This high speed programming mode II is performed at $V_{CC}=6.25V$ and $\overline{OE}/V_{PP}=12.75V$.

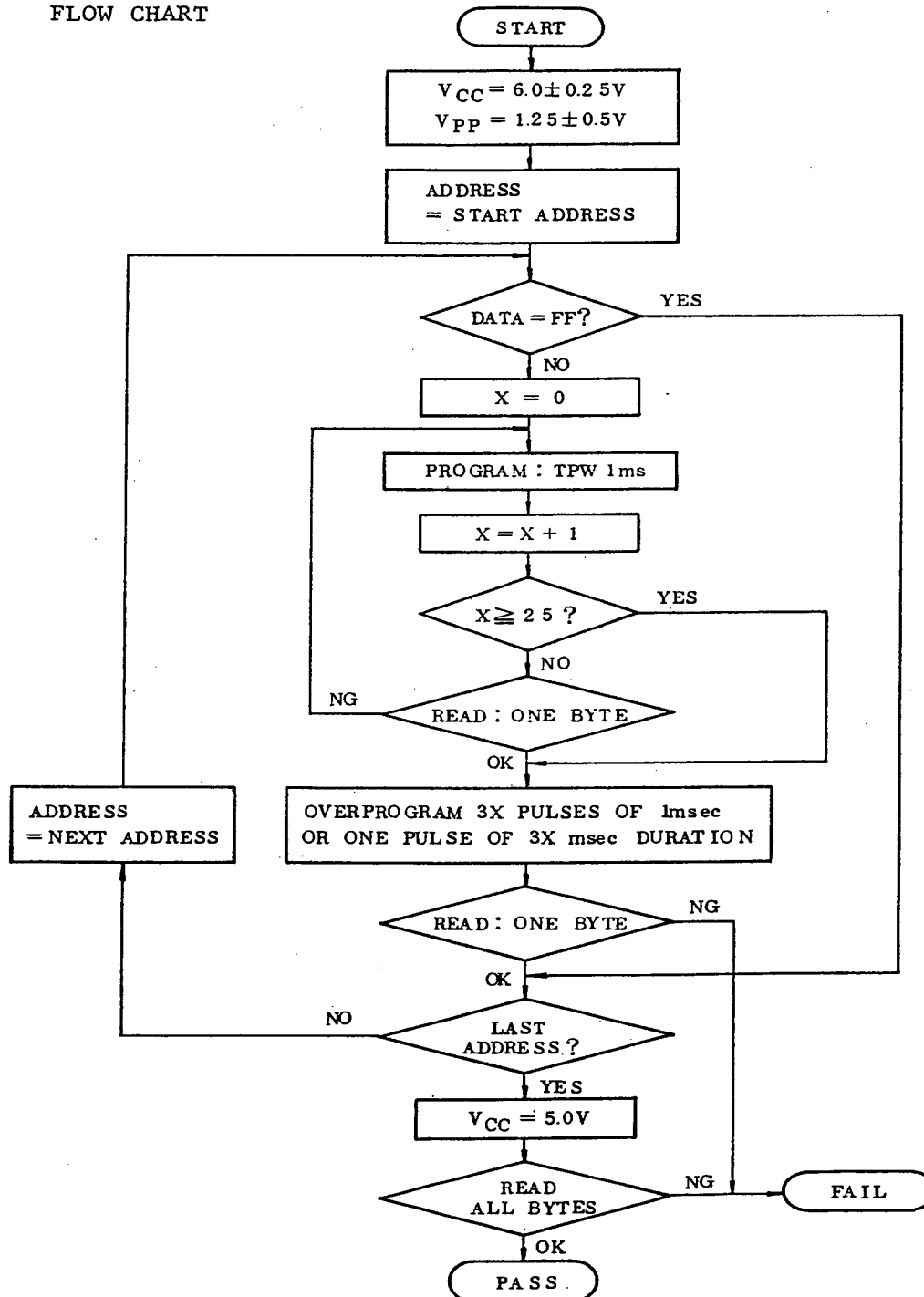
The programming is achieved by applying a single TTL low level 0.1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 0.1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{CC}=5V$.

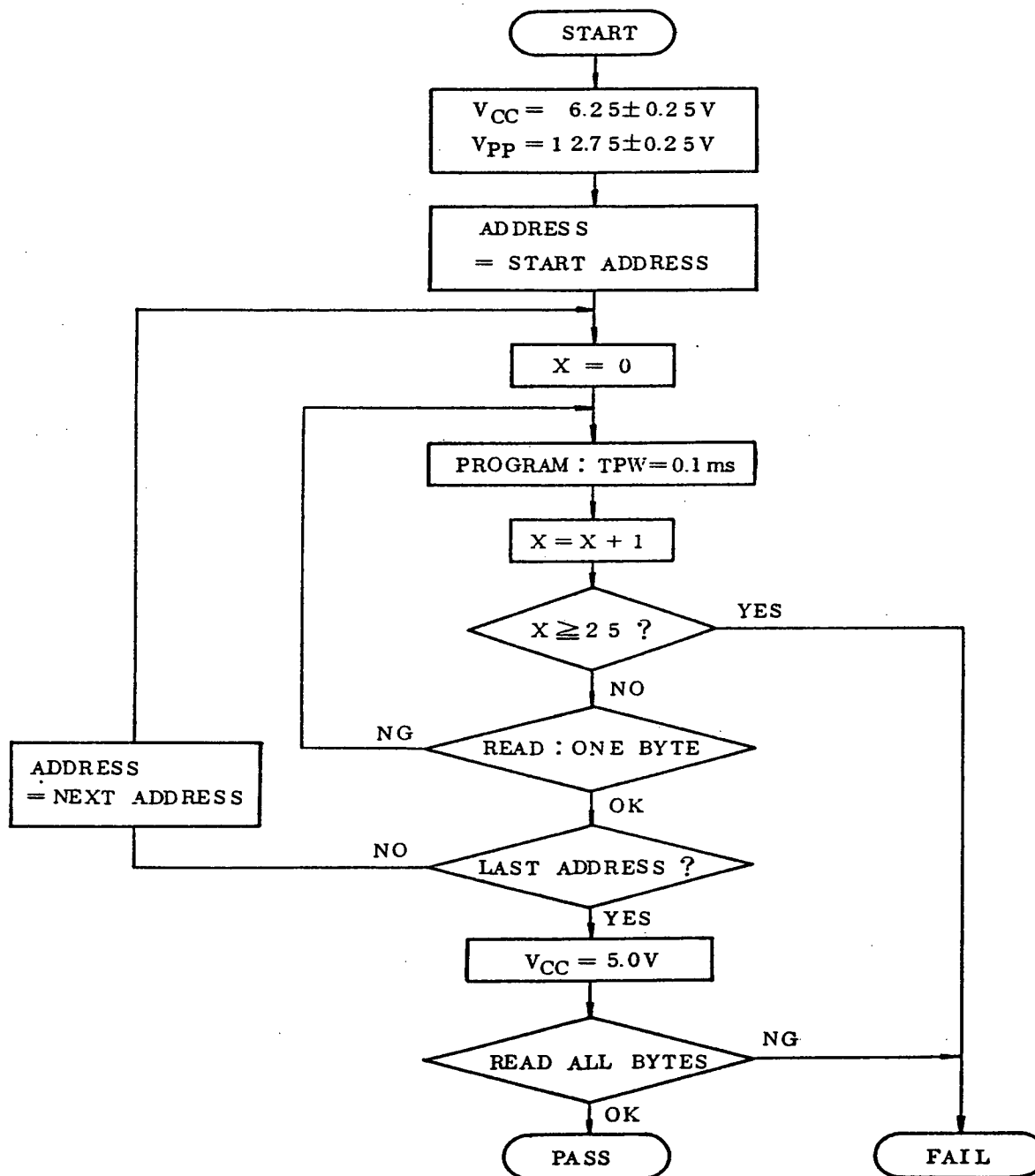
HIGH SPEED PROGRAM MODE I

FLOW CHART



HIGH SPEED PROGRAM MODE II

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC54512AP/AF which identifies its manufacturer and device type.

The programming equipment may reads out manufacturer code and device code from TC54512AP/AF by using this mode before program operation and automatically set program voltage (V_{pp}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH} . These two codes possess an odd parity with the parity bit of MSB (07).

The following table shows electric signature of TC54512AP/AF.

PINS SIGNATURE	A0 (10)	07 (19)	06 (18)	05 (17)	04 (16)	03 (15)	02 (13)	01 (12)	00 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	0	0	0	0	1	0	1	85

Notes: A9=12V±0.5V

A1 ~ A8, A10 ~ A15, $\overline{CE}$, $\overline{OE}=V_{IL}$

TC541000AP/AF-12, -15

TC541001AP/AF-12, -15

SILICON STACKED GATE MOS
INTEGRATED CIRCUIT

131,072 WORD x 8 BIT CMOS ONE TIME PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The TC541000AP/AF and TC541001AP/AF are a 131,072 word $\times$ 8 bit one time programmable read only memory and molded in a 32 pin plastic package.

The TC541000AP/AF and TC541001AP/AF's access time are 120ns/150ns and has low power standby mode which reduces the power dissipation without increasing access time. The electrical characteristic and programming method are the same as U.V. EPROM TC571000AD/TC571001AD's. Once programmed, the TC541000AP/AF and TC541001AP/AF can not be erased because of using plastic package without transparent window.

FEATURES

- Peripheral circuit : CMOS
- Memory cell : N-MOS
- Access Time

	- 12	- 15
t _{ACC}	120ns	150ns
Temp	0~70°C	

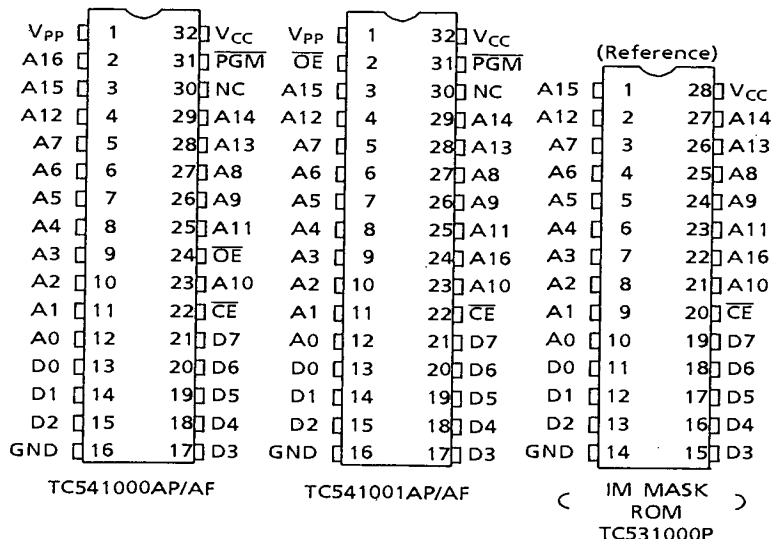
- Low power dissipation

Active : 30mA / 8.3MHz

Standby : 100 μ A

- Single 5V power supply
- Full static operation
- High speed programming operation : tpw 0.1ms
- Input and output TTL compatible
- JEDEC standard 32 pin : TC541000AP/AF
- 1M MROM compatible : TC541001AP/AF
- TC541000AP/TC541001AP : DIP32-P-600
- TC541000AF/TC541001AF : SOP32-P-525

PIN CONNECTION (TOP VIEW)

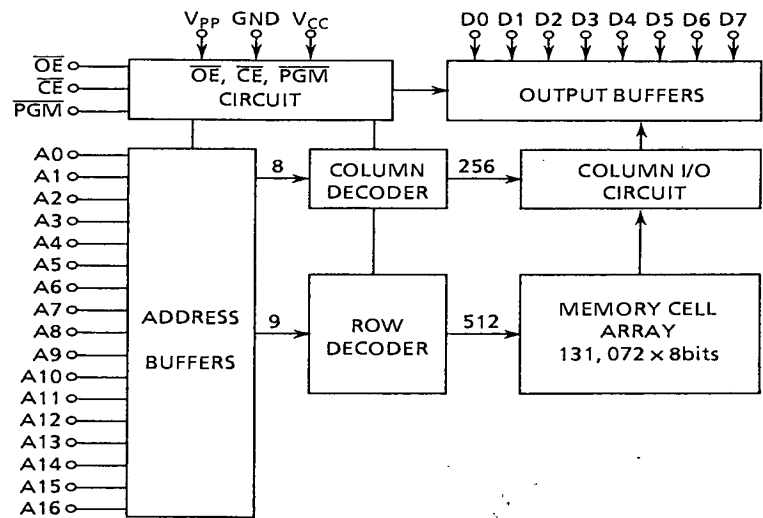


PIN NAMES

A0~A16	Address Inputs
D0~D7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
PGM	Program Control Input
V _{CC}	V _{CC} Supply Voltage
V _{PP}	Program Supply Voltage
GND	Ground
NC	No Connection

TC541000AP/AF-12,-15 TC541001AP/AF-12,-15

BLOCK DIAGRAM



MODE SELECTION

MODE	PIN	PGM	CE	OE	V _{PP}	V _{CC}	D0~D7	Power
Read		H	L	L	5V	5V	Data Out	Active
Output Deselect		*	*	H			High Impedance	
Standby		*	H	*			High Impedance	Standby
Program		L	L	H	12.75V	6.25V	Data In	Active
Program Inhibit		*	H	*			High Impedance	
		H	L	H			High Impedance	
Program Verify		H	L	L			Data Out	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{CC}	V _{CC} Power Supply Voltage	- 0.6~7.0	V
V _{PP}	Program Supply Voltage	- 0.6~14.0	V
V _{IN}	Input Voltage	- 0.6~7.0	V
V _{I/O}	Input/Output Voltage	- 0.6~V _{CC} + 0.5	V
P _D	Power Dissipation	1.0	W
T _{SOLDER}	Soldering Temperature Time	260 · 10	°C · sec
T _{STRG}	Storage Temperature	- 65~125	°C
T _{OPR}	Operating Temperature	0~70	°C

TC541000AP/AF-12, -15 TC541001AP/AF-12, -15

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage	– 0.3	–	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	$V_{CC} - 0.6$	V_{CC}	$V_{CC} - 0.6$	V

D.C. AND OPERATING CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	–	–	± 10	μA
I_{CCO1}	Operating Current	$\overline{CE} = 0\text{V}$	–	–	30	mA
I_{CCO2}		$I_{OUT} = 0\text{mA}$	–	–	15	mA
I_{CCS1}	Standby Current	$\overline{CE} = V_{IH}$	–	–	1	mA
I_{CCS2}		$\overline{CE} = V_{CC} - 0.2\text{V}$	–	–	100	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4	–	–	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{mA}$	–	–	0.4	V
I_{PP1}	V_{PP} Current	$V_{PP} = V_{CC} \pm 0.6\text{V}$	–	–	± 10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 0.4\text{V} \sim V_{CC}$	–	–	± 10	μA

A.C. CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$, $V_{PP} = V_{CC} \pm 0.6\text{V}$)

SYMBOL	PARAMETER	TC541000AP – 12 / TC541001AP – 12 TC541000AF – 12 / TC541001AF – 12		TC541000AP – 15 / TC541001AP – 15 TC541000AF – 15 / TC541001AF – 15		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	–	120	–	150	ns
t_{CE}	$\overline{CE}$ to Output Valid	–	120	–	150	ns
t_{OE}	$\overline{OE}$ to Output Valid	–	60	–	70	ns
t_{PGM}	$\overline{PGM}$ to Output Valid	–	60	–	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	50	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	50	0	60	ns
t_{DF3}	$\overline{PGM}$ to Output in High-Z	0	50	0	60	ns
t_{OH}	Output Data Hold Time	0	–	0	–	ns

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and $C_L = 100\text{pF}$
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

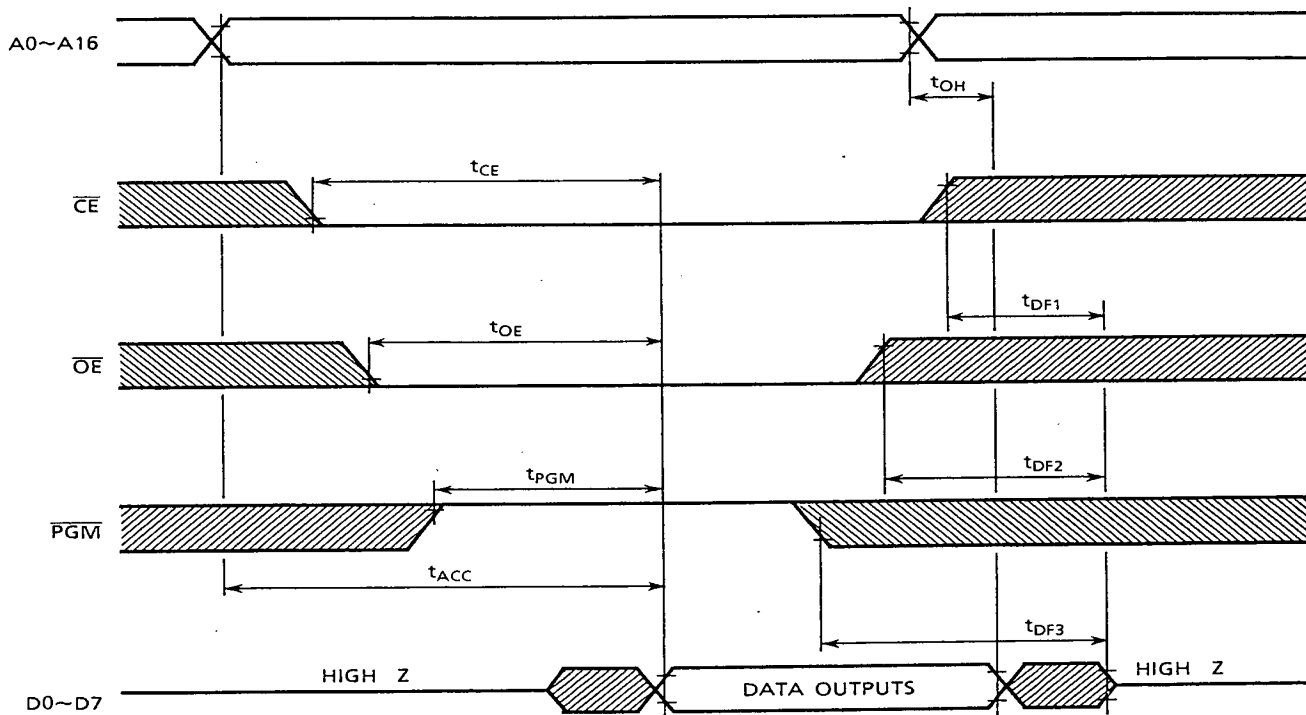
TC541000AP/AF-12, -15 **TC541001AP/AF-12, -15**

CAPACITANCE* ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$	—	16	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0\text{V}$	—	16	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



TC541000AP/AF-12,-15

TC541001AP/AF-12,-15

HIGH SPEED PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	$V_{CC} + 1.0$	V
V_{IL}	Input Low Voltage	— 0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.50	12.75	13.00	V

D.C. AND OPERATING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25 \pm 0.25\text{V}$, $V_{PP} = 12.75 \pm 0.25\text{V}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	—	—	± 10	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{mA}$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	30	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP} = 13.0\text{V}$	—	—	50	mA

A.C. PROGRAMMING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25 \pm 0.25\text{V}$, $V_{PP} = 12.75 \pm 0.25\text{V}$)

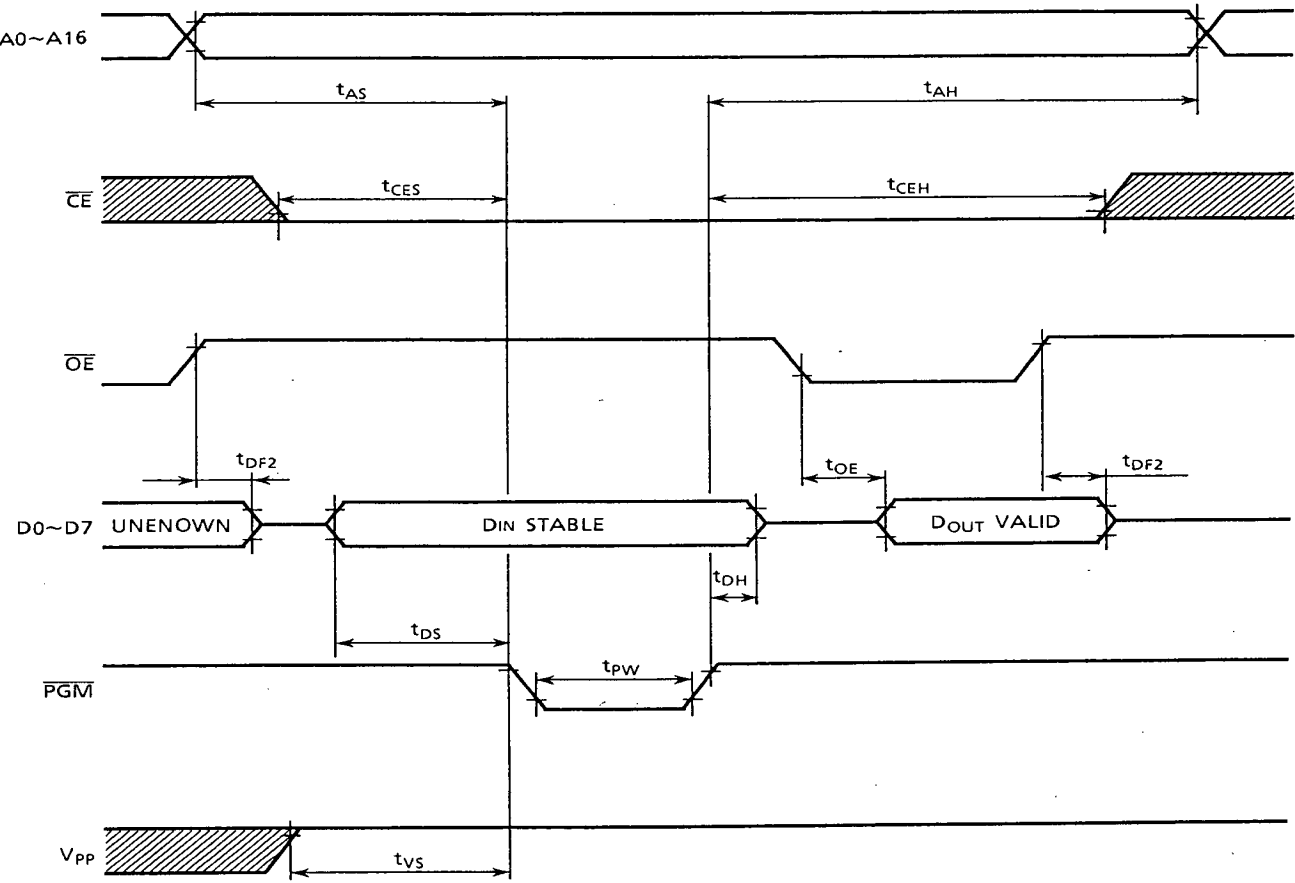
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	2	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VS}	V_{PP} Setup Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	—	0.095	0.1	0.105	ms
t_{OE}	$\overline{OE}$ to Output Valid	—	—	—	100	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE} = V_{IL}$	—	—	90	ns

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V and 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

TC541000AP/AF-12,-15 TC541001AP/AF-12,-15

HIGH SPEED PROGRAM OPERATION TIMING CHART



- Note :
1. VCC must be applied simultaneously or before Vpp and cut off simultaneously or after Vpp.
 2. Removing the device from socket and setting the device in socket with Vpp=12.75V may cause permanent damage to the device.
 3. The VPP supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the Vpp terminal. When the switching pulse voltage is applied to the Vpp terminal, the overshoot voltage of its pulse should not be exceeded 14V.

TC541000AP/AF-12, -15 TC541001AP/AF-12, -15

OPERATION INFORMATION

The TC541000AP/AF/TC541001AP/AF's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

		$\overline{\text{PGM}}$	$\overline{\text{CE}}$	$\overline{\text{OE}}$	V_{PP}	V_{CC}	D0~D7	Power
READ OPERATION	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	
	Standby	*	H	*			High Impedance	Standby
PROGRAM OPERATION ($T_a = 25 \pm 5^\circ\text{C}$)	Program	L	L	H	12.75V	6.25V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	
		H	L	H			High Impedance	
	Program Verify	H	L	L			Data Out	

Note : H; V_{IH} , L; V_{IL} , *; V_{IH} or V_{IL}

READ MODE

The TC541000AP/AF/TC541001AP/AF has three control functions. The chip enable ($\overline{\text{CE}}$) controls the operation power and should be used for device selection.

The output enable ($\overline{\text{OE}}$) and the program control ($\overline{\text{PGM}}$) control the output buffers. Independent of device selection.

Assuming in that $\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$ and $\overline{\text{PGM}} = V_{IH}$, the output data is valid at the output after address access time from stabilizing of all addresses.

The $\overline{\text{CE}}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{\text{CE}} = V_{IL}$, $\overline{\text{PGM}} = V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{\text{OE}}$.

And assuming that $\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{\text{PGM}}$.

OUTPUT DESELECT MODE

Assuming that $\overline{\text{CE}} = V_{IH}$ or $\overline{\text{OE}} = V_{IH}$, the outputs will be in a high impedance state.

So two or more ROMs can be connected together on a common bus line.

When $\overline{\text{CE}}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC541000AP / AF / TC541001AP / AF has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC541000AP / AF / TC541001AP / AF is placed in the standby mode which reduce the operating current to $100\mu A$ by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC541000AP / AF / TC541001AP / AF are in the "1" state which is erased state.

Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.

The levels required for all inputs are TTL. The TC541000AP / AF / TC541001AP / AF can be programmed any location at anytime - either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.75V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TC541000AP / AF / TC541001AP / AF from being programmed.

Programming of two or more EPROMs in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM OPERATION

The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the V_{PP} terminal with $V_{CC}=6.25V$ and $\overline{PGM}=V_{IH}$.

The programming is achieved by applying a single TTL low level 0.1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

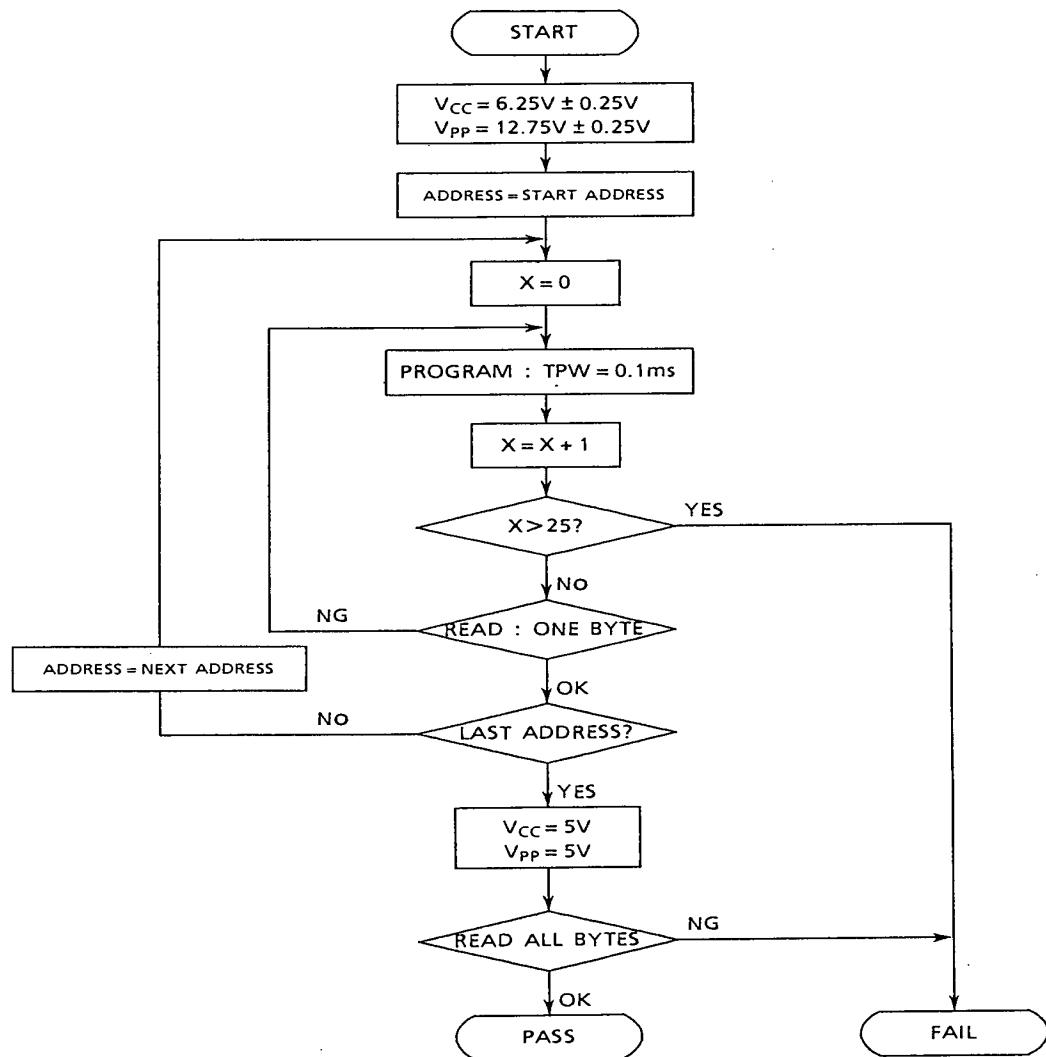
If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

TC541000AP/AF-12, -15 TC541001AP/AF-12, -15

HIGH SPEED PROGRAM OPERATION

FLOW CHART



TC541000AP/AF-12,-15 TC541001AP/AF-12,-15

ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC541000AP / AF / TC541001AP / AF which identifies it's manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TC541000AP / AF / TC541001AP / AF by using this mode before program operation and automatically set program voltage (V_{pp}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH} . These two codes possess an odd parity with the parity bit of MSB (D7).

The following table shows electric signature of TC541000AP / AF / TC541001AP / AF.

SIGNATURE		PINS	A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX. DATA
Manufacture Code			V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	TC541000AP / AF		V_{IH}	1	0	0	0	0	1	1	0	86
	TC541001AP / AF			0	0	0	0	0	1	1	1	07

Notes : A9=12V $\pm$ 0.5V
A1~A8, A10~A16, $\overline{CE}$, $\overline{OE}$ = V_{IL}
 $\overline{PGM}$ = V_{IH}

TC54H1000AP/AF-85,-10

TC54H1001AP/AF-85,-10

SILICON STACKED GATE MOS
INTEGRATED CIRCUIT

131,072 WORD x 8 BIT CMOS ONE TIME PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The TC54H1000AP / AF and TC54H1001AP / AF are a 131,072 word × 8 bit one time programmable read only memory and molded in a 32 pin plastic package.

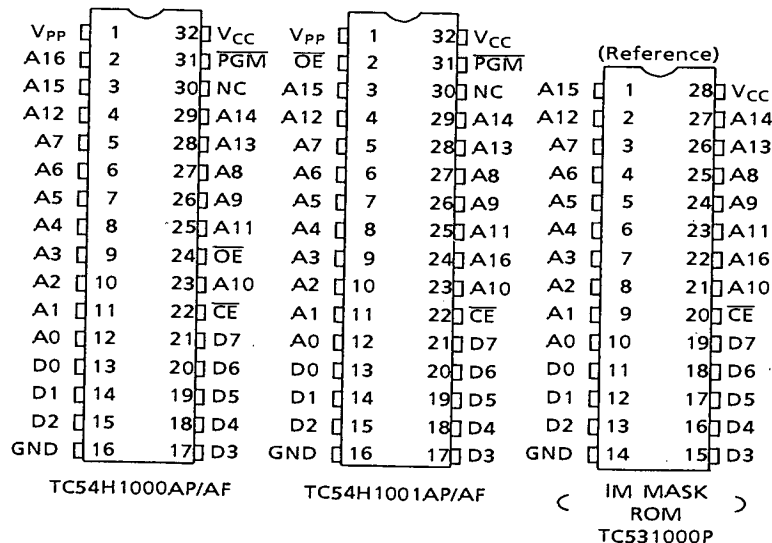
The TC54H1000AP / AF and TC54H1001AP / AF's access time are 85ns/100ns and has low power standby mode which reduces the power dissipation without increasing access time. The electrical characteristic and programming method are the same as U.V. EPROM TC57H1000AD / TC57H1001AD's. Once programmed, the TC54H1000AP / AF and TC54H1001AP / AF can not be erased because of using plastic package without transparent window.

FEATURES

- Peripheral circuit : CMOS
- Memory cell : N-MOS
- Access Time
- Low power dissipation
- Active : 40mA / 11.8MHz
- Standby : 100μA
- Single 5V power supply
- Full static operation
- High speed programming operation : tpw 0.1ms
- Input and output TTL compatible
- JEDEC standard 32 pin : TC54H1000AP / AF
- 1M MROM compatible : TC54H1001AP / AF
- TC54H1000AP / TC54H1001AP : DIP32-P-600
- TC54H1000AF / TC54H1001AF : SOP32-P-525

	- 85	- 10
t _{ACC}	85ns	100ns
Temp	0~70°C	

PIN CONNECTION (TOP VIEW)

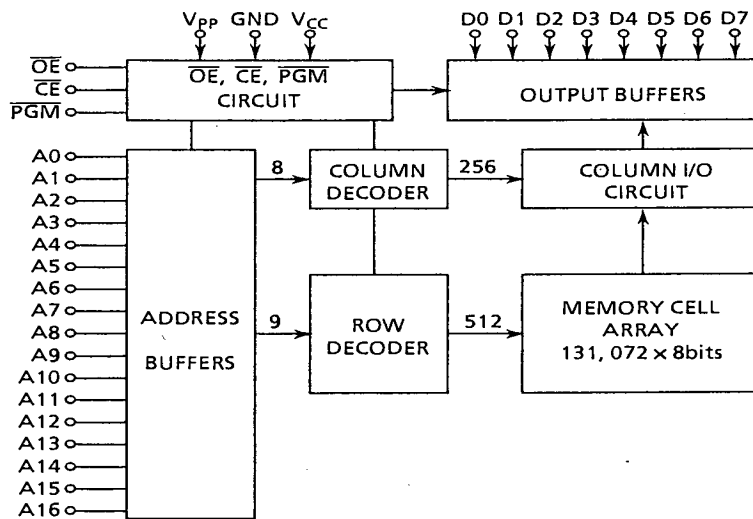


PIN NAMES

A0~A16	Address Inputs
D0~D7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
PGM	Program Control Input
V _{CC}	V _{CC} Supply Voltage
V _{PP}	Program Supply Voltage
GND	Ground
NC	No Connection

TC54H1000AP/AF-85,-10 TC54H1001AP/AF-85,-10

BLOCK DIAGRAM



MODE SELECTION

MODE \ PIN	PGM	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	D0~D7	Power
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	H	12.75V	6.25V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	- 0.6~7.0	V
V_{PP}	Program Supply Voltage	- 0.6~14.0	V
V_{IN}	Input Voltage	- 0.6~7.0	V
$V_{I/O}$	Input/Output Voltage	- 0.6~ $V_{CC} + 0.5$	V
P_D	Power Dissipation	1.0	W
T_{SOLDER}	Soldering Temperature Time	260 · 10	°C · sec
T_{STRG}	Storage Temperature	- 65~125	°C
T_{OPR}	Operating Temperature	0~70	°C

TC54H1000AP/AF-85,-10 TC54H1001AP/AF-85,-10

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage	– 0.3	–	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	$V_{CC} - 0.6$	V_{CC}	$V_{CC} - 0.6$	V

D.C. AND OPERATING CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5V \pm 5\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	–	–	± 10	μA
I_{CCO1}	Operating Current	$\overline{CE} = 0V$	–	–	40	mA
I_{CCO2}		$I_{OUT} = 0mA$	–	–	15	mA
I_{CCS1}	Standby Current	$\overline{CE} = V_{IH}$	–	–	1	mA
I_{CCS2}		$\overline{CE} = V_{CC} - 0.2V$	–	–	100	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4	–	–	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1mA$	–	–	0.4	V
I_{PP1}	V_{PP} Current	$V_{PP} = V_{CC} \pm 0.6V$	–	–	± 10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 0.4V \sim V_{CC}$	–	–	± 10	μA

A.C. CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = V_{CC} \pm 0.6V$)

SYMBOL	PARAMETER	TC54H1000AP – 85 / TC54H1001AP – 85 TC54H1000AF – 85 / TC54H1001AF – 85		TC54H1000AP – 10 / TC54H1001AP – 10 TC54H1000AF – 10 / TC54H1001AF – 10		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	–	85	–	100	ns
t_{CE}	$\overline{CE}$ to Output Valid	–	85	–	100	ns
t_{OE}	$\overline{OE}$ to Output Valid	–	45	–	50	ns
t_{PGM}	PGM to Output Valid	–	45	–	50	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	30	0	40	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	30	0	40	ns
t_{DF3}	PGM to Output in High-Z	0	30	0	40	ns
t_{OH}	Output Data Hold Time	0	–	0	–	ns

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and $C_L = 100\text{pF}$
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

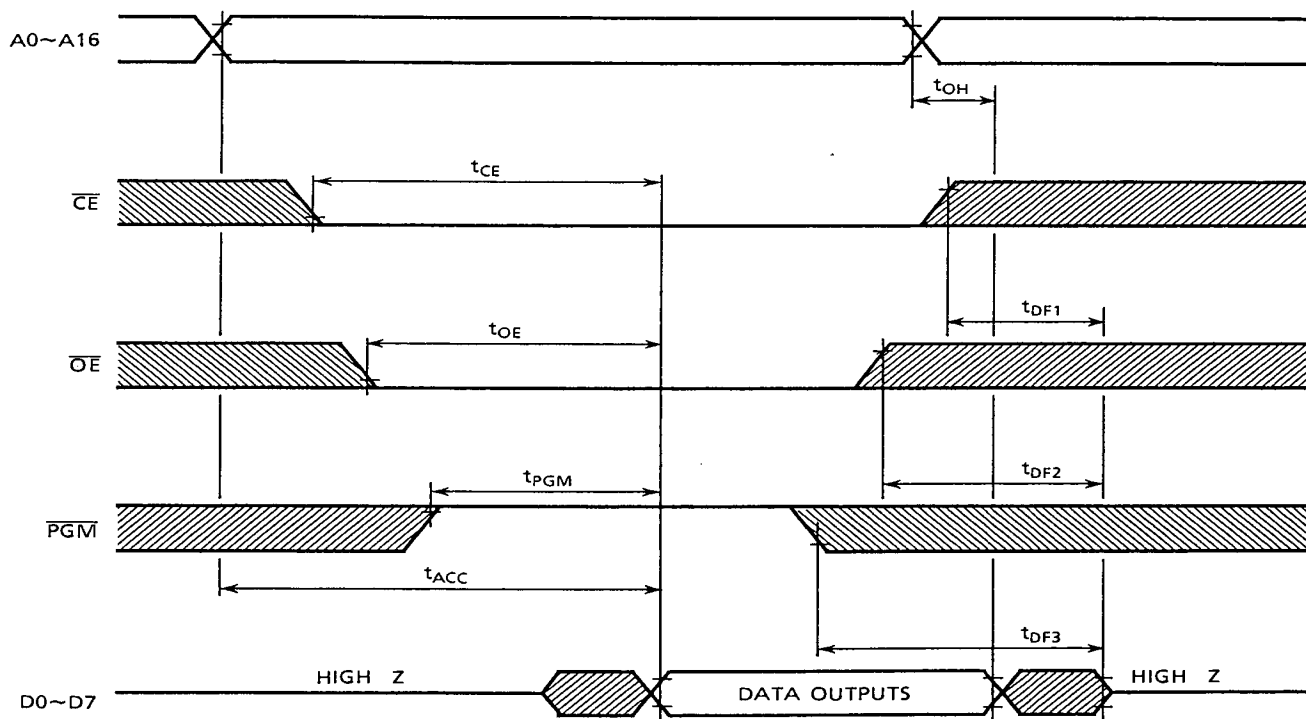
TC54H1000AP/AF-85,-10 TC54H1001AP/AF-85,-10

CAPACITANCE* ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$	—	16	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0\text{V}$	—	16	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



TC54H1000AP/AF-85,-10 **TC54H1001AP/AF-85,-10**

HIGH SPEED PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	$V_{CC} + 1.0$	V
V_{IL}	Input Low Voltage	-0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.50	12.75	13.00	V

D.C. AND OPERATING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25 \pm 0.25\text{V}$, $V_{PP} = 12.75 \pm 0.25\text{V}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	—	—	± 10	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{mA}$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	30	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP} = 13.0\text{V}$	—	—	50	mA

A.C. PROGRAMMING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25 \pm 0.25\text{V}$, $V_{PP} = 12.75 \pm 0.25\text{V}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	2	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VS}	V_{PP} Setup Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	—	0.095	0.1	0.105	ms
t_{OE}	$\overline{OE}$ to Output Valid	—	—	—	100	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE} = V_{IL}$	—	—	90	ns

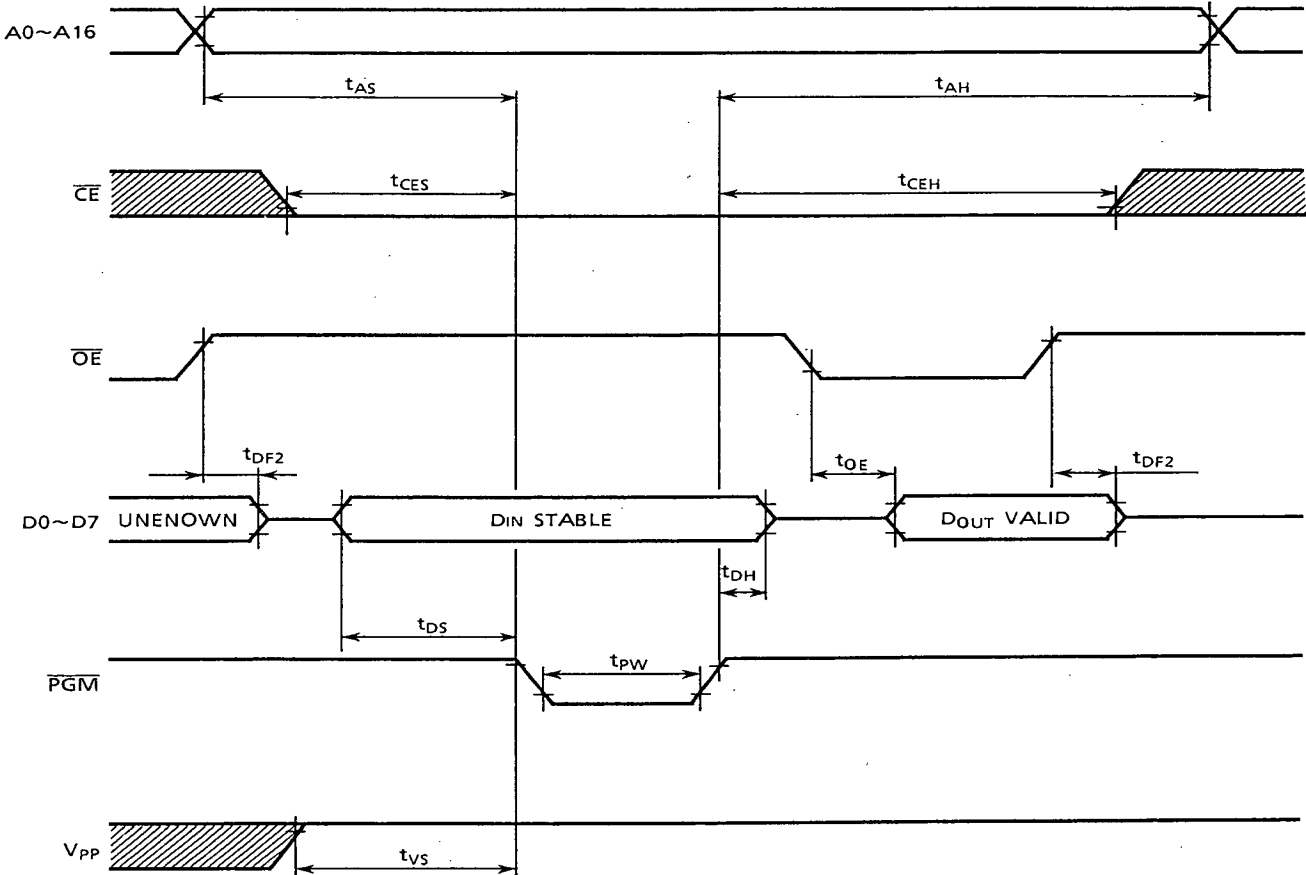
A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V and 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

TC54H1000AP/AF-85,-10
TC54H1001AP/AF-85,-10

HIGH SPEED PROGRAM OPERATION

TIMING CHART



- Note :
1. VCC must be applied simultaneously or before Vpp and cut off simultaneously or after Vpp.
 2. Removing the device from socket and setting the device in socket with Vpp=12.75V may cause permanent damage to the device.
 3. The Vpp supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the Vpp terminal. When the switching pulse voltage is applied to the Vpp terminal, the overshoot voltage of its pulse should not be exceeded 14V.

TC54H1000AP/AF-85,-10 TC54H1001AP/AF-85,-10

OPERATION INFORMATION

The TC54H1000AP / AF / TC54H1001AP / AF's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

		$\overline{\text{PGM}}$	$\overline{\text{CE}}$	$\overline{\text{OE}}$	V_{PP}	V_{CC}	D0~D7	Power
READ OPERATION	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	
	Standby	*	H	*			High Impedance	Standby
PROGRAM OPERATION ($T_a = 25 \pm 5^\circ\text{C}$)	Program	L	L	H	12.75V	6.25V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	
		H	L	H			High Impedance	
	Program Verify	H	L	L			Data Out	

Note : H; V_{IH} , L; V_{IL} , *; V_{IH} or V_{IL}

READ MODE

The TC54H1000AP / AF / TC54H1001AP / AF has three control functions. The chip enable ($\overline{\text{CE}}$) controls the operation power and should be used for device selection.

The output enable ($\overline{\text{OE}}$) and the program control ($\overline{\text{PGM}}$) control the output buffers. Independent of device selection.

Assuming in that $\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$ and $\overline{\text{PGM}} = V_{IH}$, the output data is valid at the output after address access time from stabilizing of all addresses.

The $\overline{\text{CE}}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{\text{CE}} = V_{IL}$, $\overline{\text{PGM}} = V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{\text{OE}}$.

And assuming that $\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{\text{PGM}}$.

OUTPUT DESELECT MODE

Assuming that $\overline{\text{CE}} = V_{IH}$ or $\overline{\text{OE}} = V_{IH}$, the outputs will be in a high impedance state.

So two or more ROMs can be connected together on a common bus line.

When $\overline{\text{CE}}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC54H1000AP/AF/TC54H1001AP/AF has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC54H1000AP/AF/TC54H1001AP/AF is placed in the standby mode which reduce the operating current to $100\mu A$ by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC54H1000AP/AF/TC54H1001AP/AF are in the "1" state which is erased state.

Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.

The levels required for all inputs are TTL. The TC54H1000AP/AF/TC54H1001AP/AF can be programmed any location at anytime - either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.75V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TC54H1000AP/AF/TC54H1001AP/AF from being programmed.

Programming of two or more EPROMs in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM OPERATION

The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the V_{PP} terminal with $V_{CC}=6.25V$ and $\overline{PGM}=V_{IH}$.

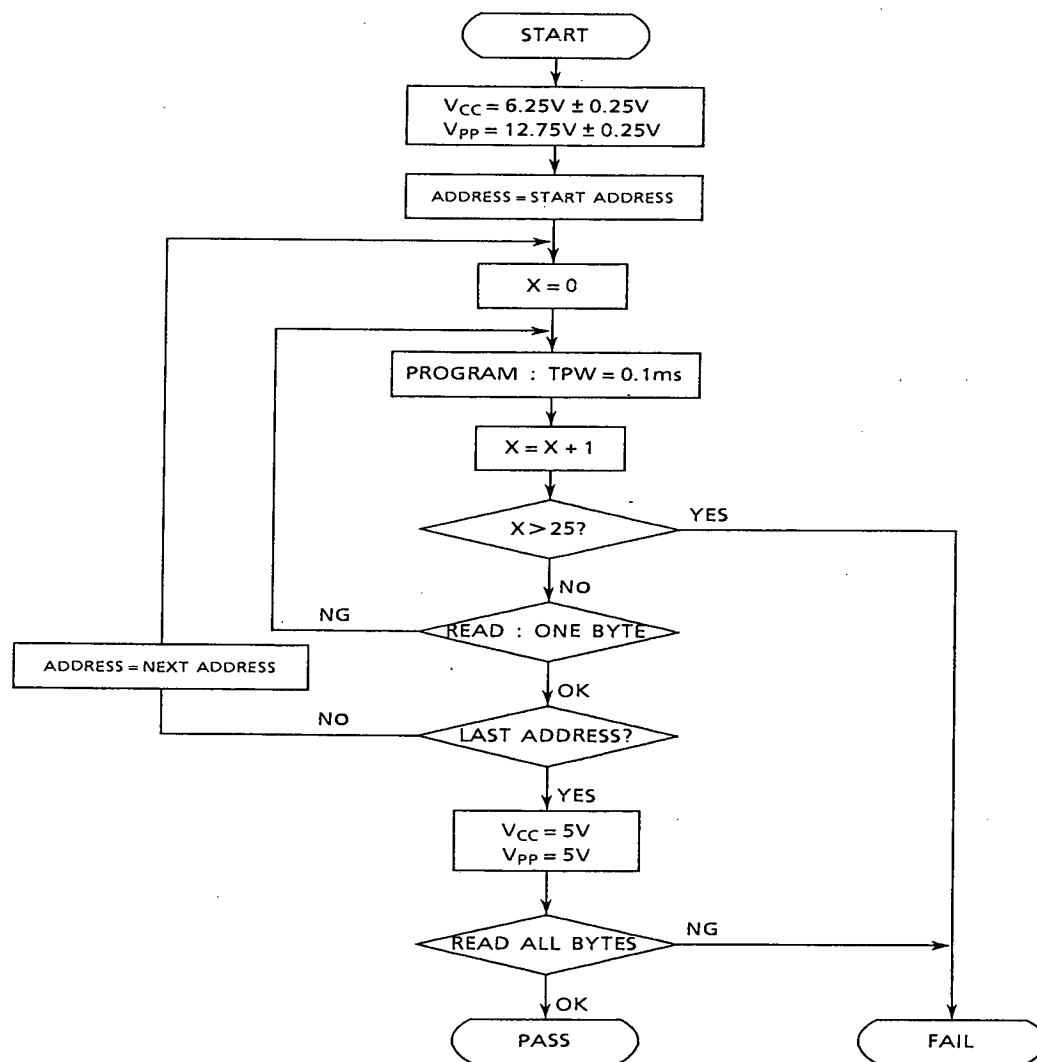
The programming is achieved by applying a single TTL low level 0.1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

TC54H1000AP/AF-85,-10
TC54H1001AP/AF-85,-10

HIGH SPEED PROGRAM OPERATION
FLOW CHART



TC54H1000AP/AF-85,-10 TC54H1001AP/AF-85,-10

ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC54H1000AP / AF / TC54H1001AP / AF which identifies it's manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TC54H1000AP / AF / TC54H1001AP / AF by using this mode before program operation and automatically set program voltage (V_{pp}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH} . These two codes possess an odd parity with the parity bit of MSB (D7).

The following table shows electric signature of TC54H1000AP / AF / TC54H1001AP / AF.

SIGNATURE		PINS	A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX. DATA
Manufacture Code			V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	TC54H1000AP / AF		V_{IH}	1	0	0	0	0	1	1	0	86
	TC54H1001AP / AF			0	0	0	0	0	1	1	1	07

Notes : A9 = 12V $\pm$ 0.5V

A1~A8, A10~A16, $\overline{CE}$, $\overline{OE}$ = V_{IL}

$\overline{PGM}$ = V_{IH}

TC54H1024AP/AF-85, -10

1 MEGA BIT (65,536 WORD $\times$ 16 BIT)

CMOS ONE TIME PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The TC54H1024AP/AF is a 65,536 word $\times$ 16 bit one time programmable read only memory, and molded in a 40 pin plastic package.

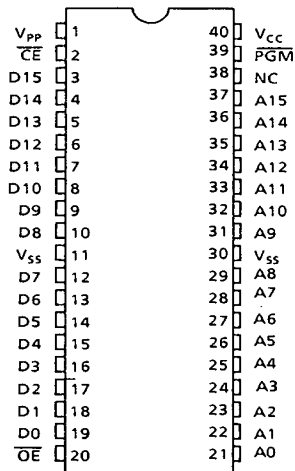
TC54H1024AP/AF is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 40mA/1MHz.

The electrical characteristics and programming method are the same as U.V.EPROM TC57H1024AD. Once programmed, the TC54H1024AP/AF can not be erased because of using plastic package without transparent window.

FEATURES

- Peripheral circuit : CMOS
- Memory cell : N-MOS
- Fast access time
 - TC54H1024AP/AF-85 : 85ns
 - TC54H1024AP/AF-10 : 100ns
- Low power dissipation
 - Active : 40mA/1MHz
 - Standby : 100 μ A
- Single 5V power supply
- Full static operation
- High speed programming operation : tpw 0.1ms
- Input and output TTL compatible
- JEDEC standard 40 pin
- TC54H1024AP : DIP40 - P - 600
- TC54H1024AF : SOP40 - P - 525

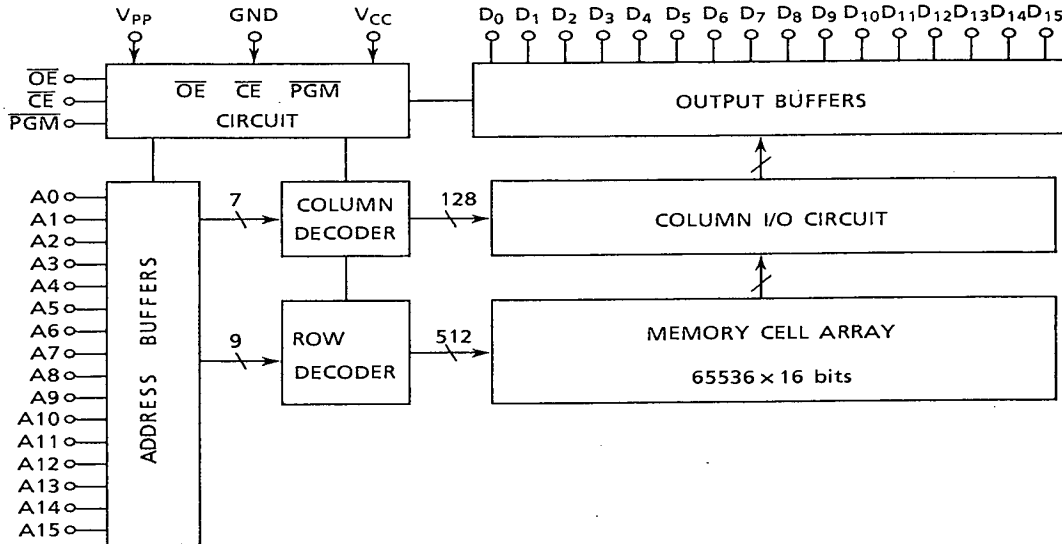
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A15	Address Inputs
D0~D15	Outputs (Inputs)
CE	Chip Enable Input
OE	Output Enable Input
PGM	Program Control Input
Vcc	Vcc Supply Voltage
Vpp	Program Supply Voltage
Vss	Ground
NC	No Connection

BLOCK DIAGRAM



MODE SELECTION

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	D0~D15	Power
Read	L	L	H	5V	5V	Data Out	Active
Output Deselect	*	H	*			High Impedance	
Standby	H	*	*				Standby
Program	L	H	L	12.75V	6.25V	Data In	Active
Program Inhibit	H	*	*			High Impedance	
	L	H	H				
Program Verify	L	L	H			Data Out	

*...H or L

MAXIMUM RATINGS

SYMBOL	CHARACTERISTIC	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	-0.6~7.0	V
V_{PP}	Program Supply Voltage	-0.6~14.0	V
V_{IN}	Input Voltage	-0.6~7.0	V
$V_{IN}(A9)$	Input Voltage (A9)	-0.6~13.5	V
V_{IO}	Input/Output Voltage	-0.6~ $V_{CC} + 0.5$	V
P_D	Power Dissipation	1.0	W
T_{SOLDER}	Soldering Temperature Time	260 · 10	°C · sec
T_{strg}	Storage Temperature	-65~125	°C
T_{opr}	Operating Temperature	0~70	°C

TC54H1024AP/AF-85, -10

READ OPERATION

AC/DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	CHARACTERISTIC	TC54H1024AP / AF-85/10
Ta	Ambient Temperature	0~70°C
V _{CC}	V _{CC} Power Supply Voltage	5V ± 5%
V _{PP}	V _{PP} Power Supply Voltage	0V~V _{CC} + 0.6V

DC AND OPERATING CHARACTERISTICS

SYMBOL	CHARACTERISTIC	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Current	V _{IN} = 0~V _{CC}	—	—	± 10	μA
I _{CCO}	Operating Current	$\overline{CE}$ = 0V I _{OUT} = 0mA	t _{cycle} 85ns t _{cycle} 1μs	— —	60 40	mA
I _{CCS1}	Standby Current	$\overline{CE}$ = V _{IH}	—	—	1	mA
I _{CCS2}		$\overline{CE}$ = V _{CC} - 0.2V	—	—	100	μA
V _{IH}	Input High Voltage	—	2.2	—	V _{CC} + 0.3	V
V _{IL}	Input Low Voltage	—	- 0.3	—	0.8	V
V _{OH}	Output High Voltage	I _{OH} = - 400μA	2.4	—	—	V
V _{OL}	Output Low Voltage	I _{OL} = 2.1mA	—	—	0.4	V
I _{PP1}	V _{PP} Current	V _{PP} = 0V~V _{CC} + 0.6V	—	—	± 10	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0.4V~V _{CC}	—	—	± 10	μA

AC CHARACTERISTICS

SYMBOL	CHARACTERISTIC	TC54H1024AP/AF-85		TC54H1024AP/AF-10		UNIT
		MIN.	MAX.	MIN.	MAX.	
t _{ACC}	Address Access Time	—	85	—	100	ns
t _{CE}	$\overline{CE}$ to Output Valid	—	85	—	100	
t _{OE}	$\overline{OE}$ to Output Valid	—	45	—	50	
t _{DF1}	$\overline{CE}$ to Output in High-Z	—	30	—	50	
t _{DF2}	$\overline{OE}$ to Output in High-Z	—	30	—	50	
t _{OH}	Output Data Hold Time	5	—	10	—	

AC TEST CONDITIONS

Output Load : 1 TTL Gate and C_L = 100pF
 Input Pulse Rise and Fall Times : 10ns Max.
 Input Pulse Levels : 0.45V to 2.4V
 Timing Measurement Reference Levels: Inputs 0.8V and 2.2V Outputs 0.8V and 2.0V

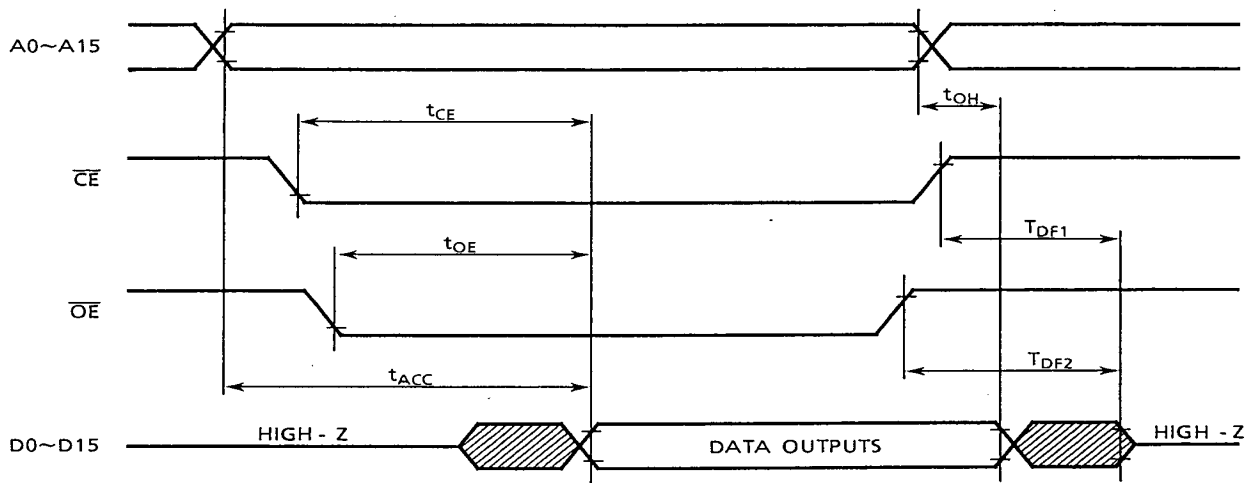
TC54H1024AP/AF-85, -10

CAPACITANCE *(Ta = 25°C, f = 1MHz)

SYMBOL	CHARACTERISTIC	TEST CONDITION	MIN.	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = 0V	—	16	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	—	16	

* This characteristic is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



TC54H1024AP/AF-85, -10

HIGH SPEED PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage	- 0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.50	12.75	13.00	V

DC AND OPERATING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.75\text{V} \pm 0.25\text{V}$)

SYMBOL	CHARACTERISTIC	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	—	—	± 10	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{mA}$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	50	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP} = 13.0\text{V}$	—	—	100	mA

AC PROGRAMMING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.75\text{V} \pm 0.25\text{V}$)

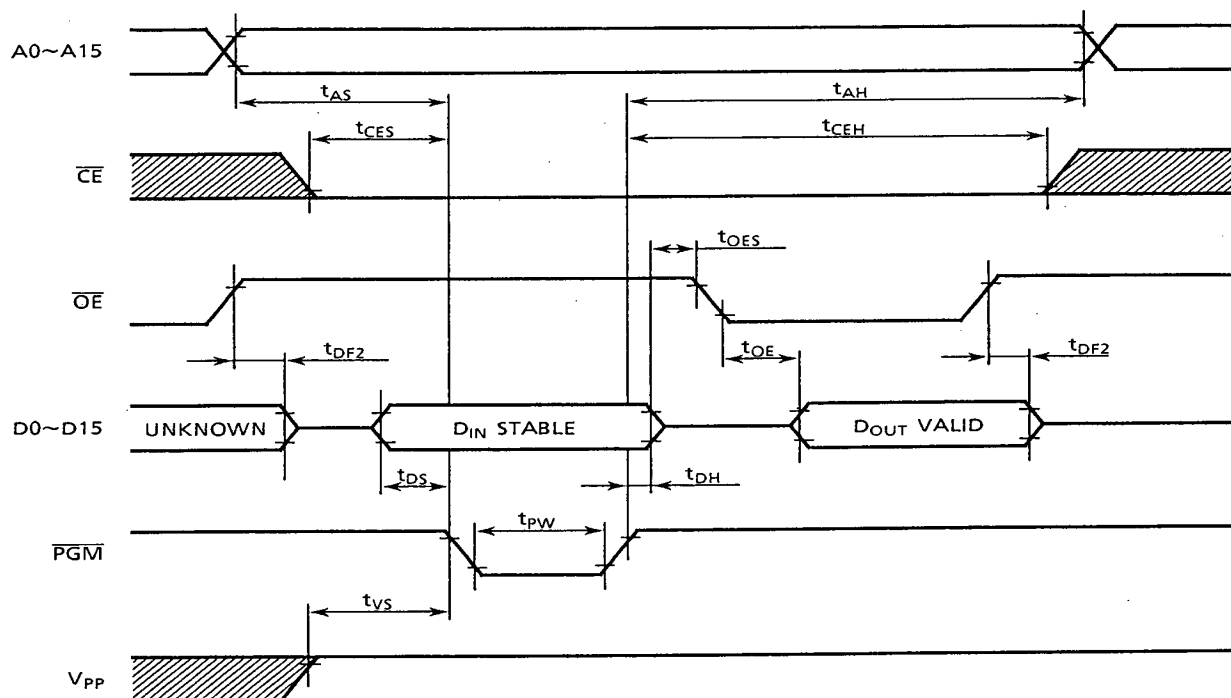
SYMBOL	CHARACTERISTIC	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	2	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VS}	V_{PP} Setup Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	—	0.095	0.1	0.105	ms
t_{OE}	$\overline{OE}$ to Output Valid	—	—	—	500	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE} = V_{IL}$	—	—	150	ns
t_{OES}	$\overline{OE}$ Setup Time	—	2	—	—	μs

AC TEST CONDITIONS

- Output Load : 1 TTL Gate and $C_L = 100\text{pF}$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V and 2.4V
- Timing Measurement Reference Levels: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

HIGH SPEED PROGRAM OPERATION

TIMING CHART



- Note :
1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP} .
 2. Removing the device from socket and setting the device in socket with $V_{PP}=12.75V$ may cause permanent damage to the device.
 3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal.
When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

TC54H1024AP/AF-85,-10

OPERATION INFORMATION

The TC54H1024AP / AF's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

MODE		PIN	$\overline{CE}$	$\overline{OE}$	PGM	V_{PP}	V_{CC}	D0~D15	Power
READ OPERATION	Read		L	L	H	5V	5V	Data Out	Active
	Output Deselect		*	H	*			High Impedance	
	Standby		H	*	*				Standby
PROGRAM OPERATION	Program		L	H	L	12.75V	6.25V	Data In	Active
	Program Inhibit		H	*	*			High Impedance	
			L	H	H				
	Program Verify		L	L	H			Data Out	

Note : H... V_{IH} , L... V_{IL} , *... V_{IH} or V_{IL}

READ MODE

The TC54H1024AP / AF has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) controls the output buffers, independent of device selection. Assuming that $\overline{CE} = \overline{OE} = V_{IL}$ and $\overline{PGM} = V_{IH}$, the output data is valid at the output after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$, the outputs will be in a high impedance state. So two or more ROMs can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC54H1024AP / AF has a low power standby mode controlled by the $\overline{CE}$ signal.

By applying a high level to the $\overline{CE}$ input, the TC54H1024AP / AF is placed in the standby mode which reduce the operating current to $100\mu A$ by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC54H1024AP / AF are in the "1" state which is erased state.

Therefore the program operation is to introduce O'S data into the desired bit locations by electrically programming.

The levels required for all inputs are TTL. The TC54H1024AP / AF can be programmed any location at anytime -- either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.75V) is applied to V_{pp} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TC54H1024AP / AF from being programmed.

Programming of two or more EPROMs in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM OPERATION

The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the V_{pp} terminal with $V_{CC}=6.25V$ and $\overline{PGM}=V_{IH}$.

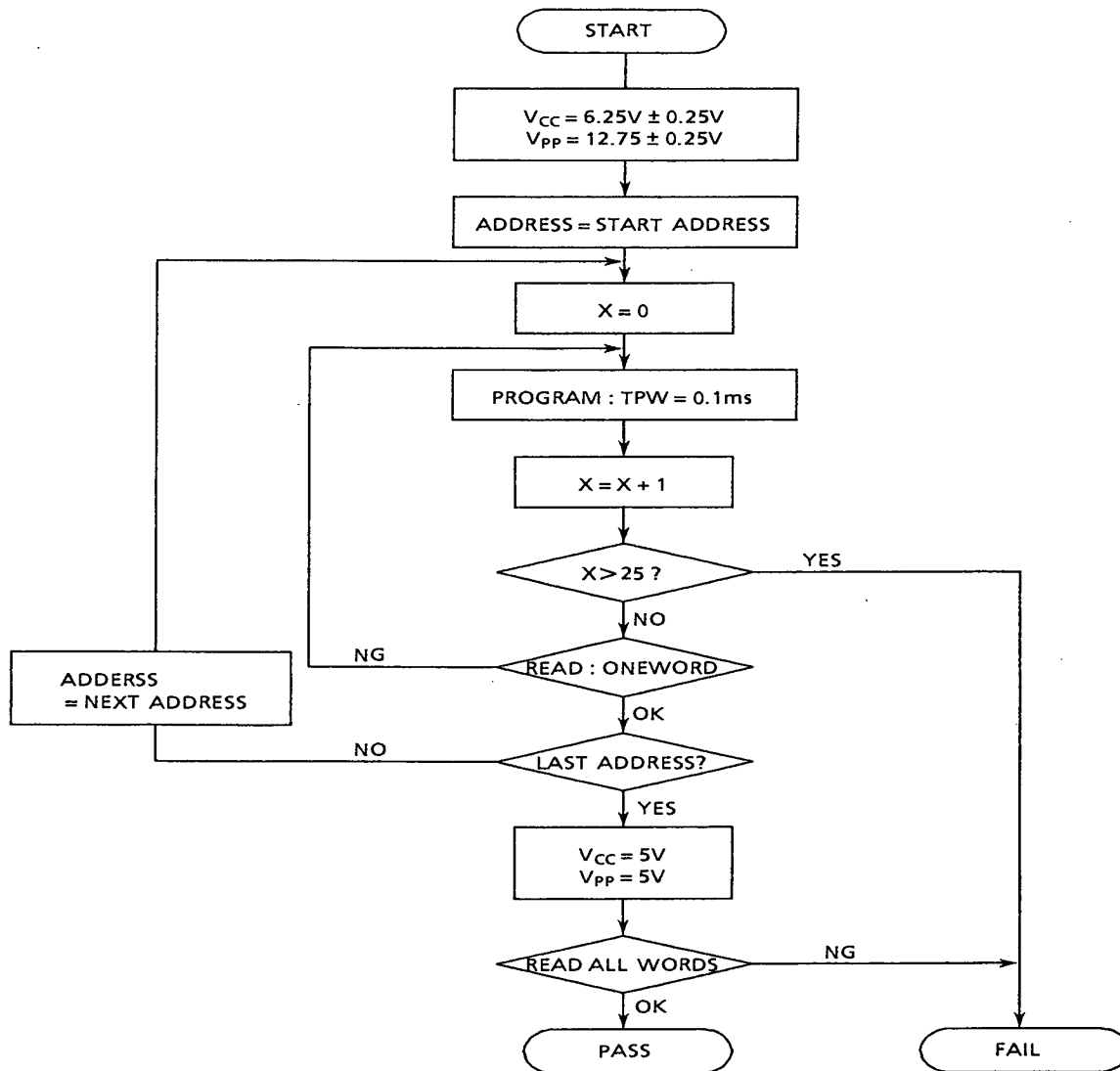
The programming is achieved by applying a single TTL low level 0.1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM OPERATION

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC54H1024AP/AF which identifies it's manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TC54H1024AP/AF by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH} .

These two codes possess an odd parity with the parity bit of (D7).

The following table shows electric signature of TC54H1024AP/AF.

SIGNATURE \ PINS	A ₀	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	HEX DATA
Manufacturer Code	V_{IL}	*	*	*	*	*	*	*	*	1	0	0	1	1	0	0	0	**98
Device Code	V_{IH}	*	*	*	*	*	*	*	*	1	0	0	0	1	0	0	1	**89

Notes : A9=12V±0.5V, A₁–A₈, A₁₀–A₁₅, $\overline{CE}$, $\overline{OE}$ = V_{IL} , $\overline{PGM}$ = V_{IH}

* : Don't care

SILICON STACKED GATE MOS INTEGRATED CIRCUIT

TC544000P/F/FT-12,-150

524,288 WORD $\times$ 8 BIT CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The TC544000P/F/FT is a 524,288 word $\times$ 8 bit one time programmable read only memory, and molded in a 32 pin plastic package. The access time of TC544000P/F/FT is 120ns/150ns and has low power standby mode which reduces the power dissipation without increasing access time.

The electrical characteristics and programming method are the same as U.V. EPROM TC574000D'S once programmed, the TC544000P/F/FT can not be erased because of using plastic DIP without transparent window.

FEATURES

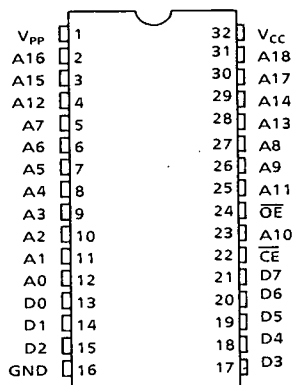
- Peripheral circuit : CMOS
- Memory cell : N-MOS
- Access time

	- 12	- 150
V _{CC}	5V $\pm$ 5%	5V $\pm$ 10%
Temp	0°C~70°C	
t _{ACC}	120ns	150ns

- 12 are satisfied with the specification of - 150

- Low power dissipation
 - Active : 60mA/8.3MHz
 - Standby: 100 μ A (T_a=70°C)
- High speed programming operation
- Single 5V power supply
- Full static operation
- Input and output TTL compatible
- JEDEC standard 32 pin
- TC544000P : DIP32-P-600
- TC544000F : SOP32-P-525
- TC544000FT : TSOP32-P-400

PIN CONNECTION (TOP VIEW)

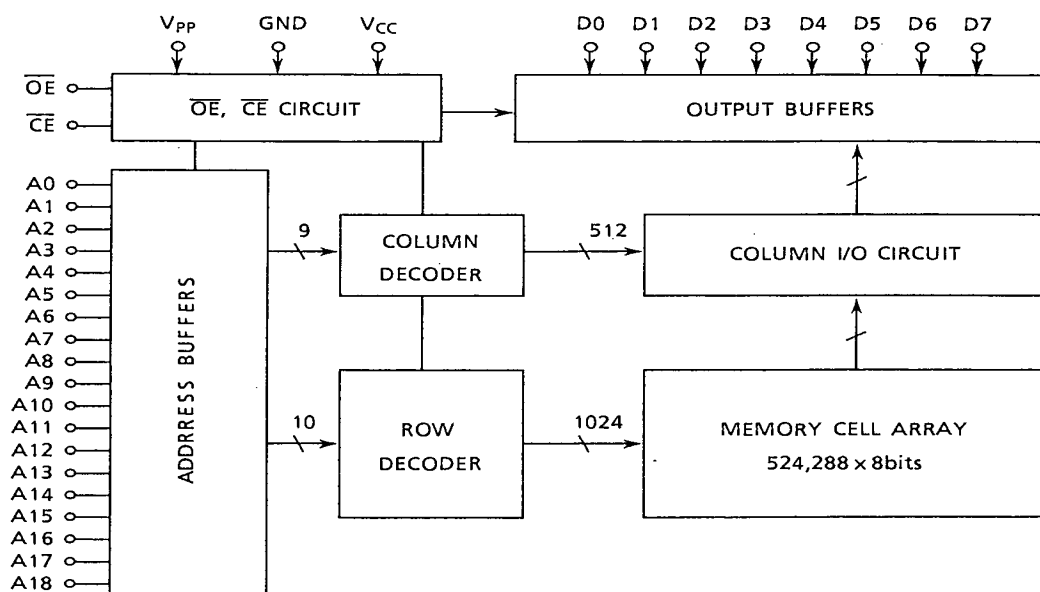


TC544000P/F/FT

PIN NAMES

A0~A18	Address Inputs
D0~D7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V _{CC}	V _{CC} Supply Voltage
V _{PP}	Program Supply Voltage
GND	Ground

BLOCK DIAGRAM



MODE SELECTION

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	D0~D7	Power
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*			High Impedance	Standby
Program	L	H	12.50V	6.25V	Data In	Active
Program Inhibit	H	H			High Impedance	
Program Verify	*	L			Data Out	

* : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	-0.6~7.0	V
V_{PP}	Program Supply Voltage	-0.6~14.0	V
V_{IN}	Input Voltage	-0.6~7.0	V
$V_{IN}(A9)$	Input Voltage (A9)	-0.6~13.5	V
$V_{I/O}$	Input/Output Voltage	-0.6~ $V_{CC} + 0.5$	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
T_{strg}	Storage Temperature	-65~125	°C
T_{opr}	Operating Temperature	0~70	°C

* : SOP Package

TC544000P/F/FT-12,-150

READ OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC544000P / F / FT - 12	TC544000P / F / FT - 150
V_{IH}	Input High Voltage	$2.2V \sim V_{CC} + 0.3V$	$2.2V \sim V_{CC} + 0.3V$
V_{IL}	Input Low Voltage	$-0.3V \sim 0.8V$	$0.3V \sim 0.8V$
V_{CC}	V_{CC} Power Supply Voltage	$5V \pm 5\%$	$5V \pm 10\%$
V_{PP}	V_{PP} Power Supply Voltage	$V_{CC} - 0.6V \sim V_{CC} + 0.6V$	$V_{CC} - 0.6V \sim V_{CC} + 0.6V$

DC AND OPERATING CHARACTERISTICS ($T_a = 0 \sim 70^\circ C$)

SIMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	—	—	± 10	μA
I_{CCO1}	Operating Current	$\overline{CE} = V_{IL}$ $I_{OUT} = 0mA$	$f = 8.3MHz$	—	60	mA
			$f = 6.7MHz$	—	50	
I_{CCO2}			$f = 1MHz$	—	15	
I_{CCS1}	Standby Current	$\overline{CE} = V_{IH}$	—	—	1	mA
I_{CCS2}		$\overline{CE} = V_{CC} - 0.2V$	—	—	100	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu A$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1mA$	—	—	0.4	V
I_{PP1}	V_{PP} Current	$V_{PP} = V_{CC} \pm 0.6V$	—	—	± 10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 0.4V \sim V_{CC}$	—	—	± 10	μA

AC CHARACTERISTICS ($T_a = 0 \sim 70^\circ C$, $V_{PP} = V_{CC} \pm 0.6V$)

SIMBOL	PARAMETER	TEST CONDITION	TC544000P / F / FT - 12		TC544000P / F / FT - 150		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE} = \overline{OE} = V_{IL}$	—	120	—	150	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE} = V_{IL}$	—	120	—	150	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE} = V_{IL}$	—	60	—	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE} = V_{IL}$	0	50	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE} = V_{IL}$	0	50	0	60	ns
t_{OH}	Output Data Hold Time	$\overline{CE} = \overline{OE} = V_{IL}$	0	—	0	—	ns

TC544000P/F/FT-12 are satisfied with the specification of TC544000P/F/FT/FT-150

AC TEST CONDITIONS

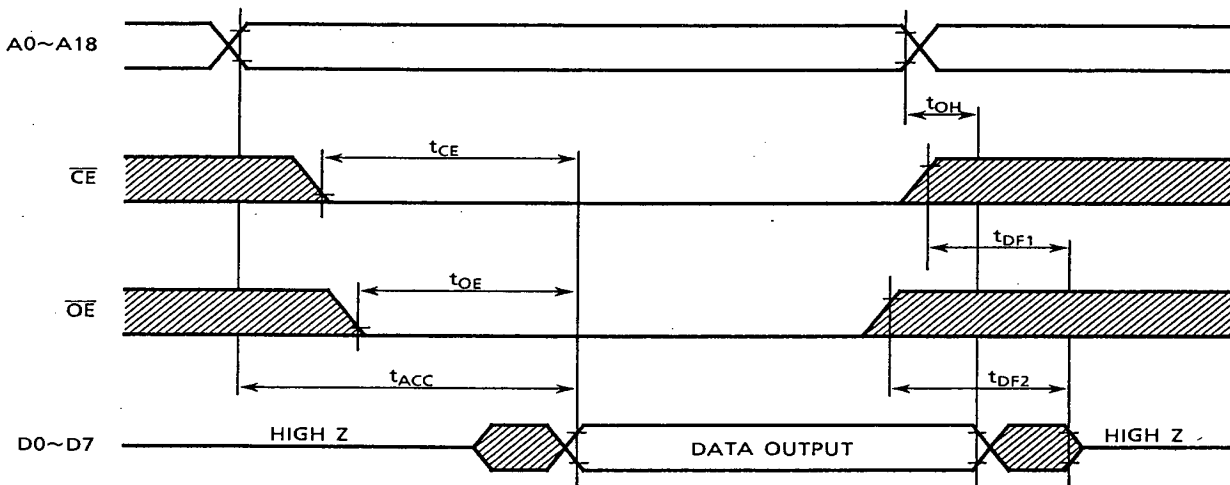
- Output Load : 1 TTL Gate and $C_L = 100pF$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V~2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = 0V	—	9	PF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	—	13	

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



TC544000P/F/FT-12,-150

HIGH SPEED PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	$V_{CC} + 1.0$	V
V_{IL}	Input Low Voltage	-0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.20	12.50	12.80	V

DC AND OPERATING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.50\text{V} \pm 0.30\text{V}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	—	—	± 10	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{mA}$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	30	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP} = 12.8\text{V}$	—	—	50	mA

AC PROGRAMMING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.50\text{V} \pm 0.30\text{V}$)

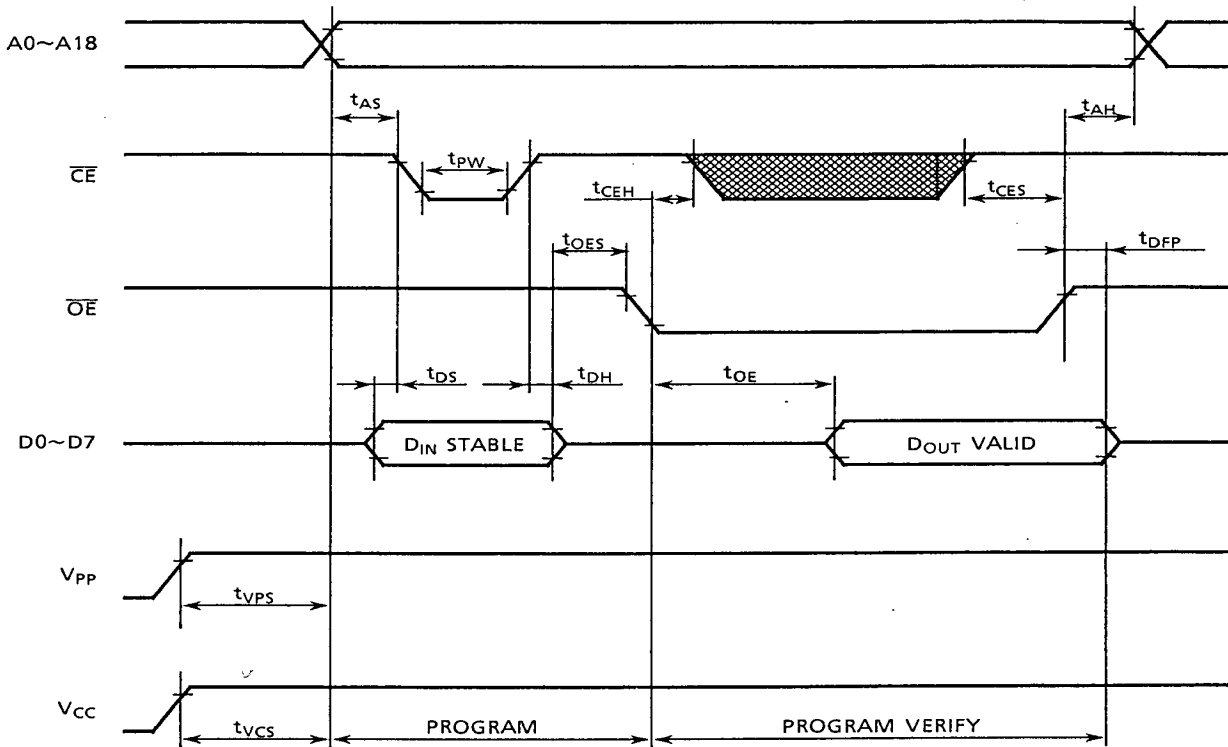
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	0	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	0	—	—	μs
t_{OES}	$\overline{OE}$ Set up Time	—	2	—	—	μs
t_{DS}	Data Set up Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VPS}	V_{PP} Set up Time	—	2	—	—	μs
t_{VCS}	V_{CC} Set up Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	45	50	55	μs
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE} = V_{IH}$	—	—	100	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE} = V_{IH}$	—	—	90	ns

AC TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V~2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAM OPERATION



- Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP} .
2. Removing the device from socket and setting the device in socket with $V_{PP}=12.50V$ may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

TC544000P/F/FT-12,-150

OPERATION INFORMATION

The TC544000P/F/FT's six operation modes are listed in the following table.
Mode selection can be achieved by applying TTL level signal to all inputs.

MODE		PIN NAMES (NUMBER)	$\overline{CE}$ (22)	$\overline{OE}$ (24)	V_{PP} (1)	V_{CC} (32)	D0~D7 (13~15, 17~21)	POWER
Read Operation ($T_a = 0 \sim 70^\circ\text{C}$)	Read		L	L	5V	5V	Data Out	Active
	Output Deselet		*	H			High Impedance	
	Standby		H	*			High Impedance	Standby
Program Operation ($T_a = 25 \pm 5^\circ\text{C}$)	Program		L	H	12.50V	6.25V	Data In	Active
	Program Inhibit		H	H			High Impedance	
	Program Verify		*	L			Data Out	

Note : H ; V_{IH} , L : V_{IL} , * : V_{IH} or V_{IL}

READ MODE

The TC544000P/F/FT has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection. The output enable ($\overline{OE}$) controls the output buffers, independent of device selection. Assuming that $\overline{CE} = \overline{OE} = V_{IL}$, the output data is valid at the outputs after address access time from stabilizing of all addresses. The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE} = V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$, the outputs will be in a high impedance state. So two or more TC544000P/F/FT's can be connected together on a common bus line. When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC544000P/F/FT has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC544000P/F/FT is placed in the standby mode which reduce the operating current to $100\mu\text{A}$ by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC544000P/F/FT are in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming. The TC544000P/F/FT is in the programming mode when the V_{PP} input is at 12.50V and $\overline{CE}$ is at Low under $\overline{OE}=V_{IH}$.

The TC544000P/F/FT can be programmed any location at any time either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with $\overline{OE}$ at V_{IL} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.50V) is applied to V_{PP} terminal, a high level $\overline{CE}$ and $\overline{OE}$ input inhibits the TC544000P/F/FT from being programmed.

Programming of two or more TC544000P/F/FT's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a low level program pulse is applied to the $\overline{CE}$ of the desired device only and high level signal is applied to the other devices.

HIGH SPEED PROGRAM MODE

The device is set up in the high speed programming mode when the programming voltage (+12.50V) is applied to the V_{PP} terminal with $V_{CC}=6.25V$.

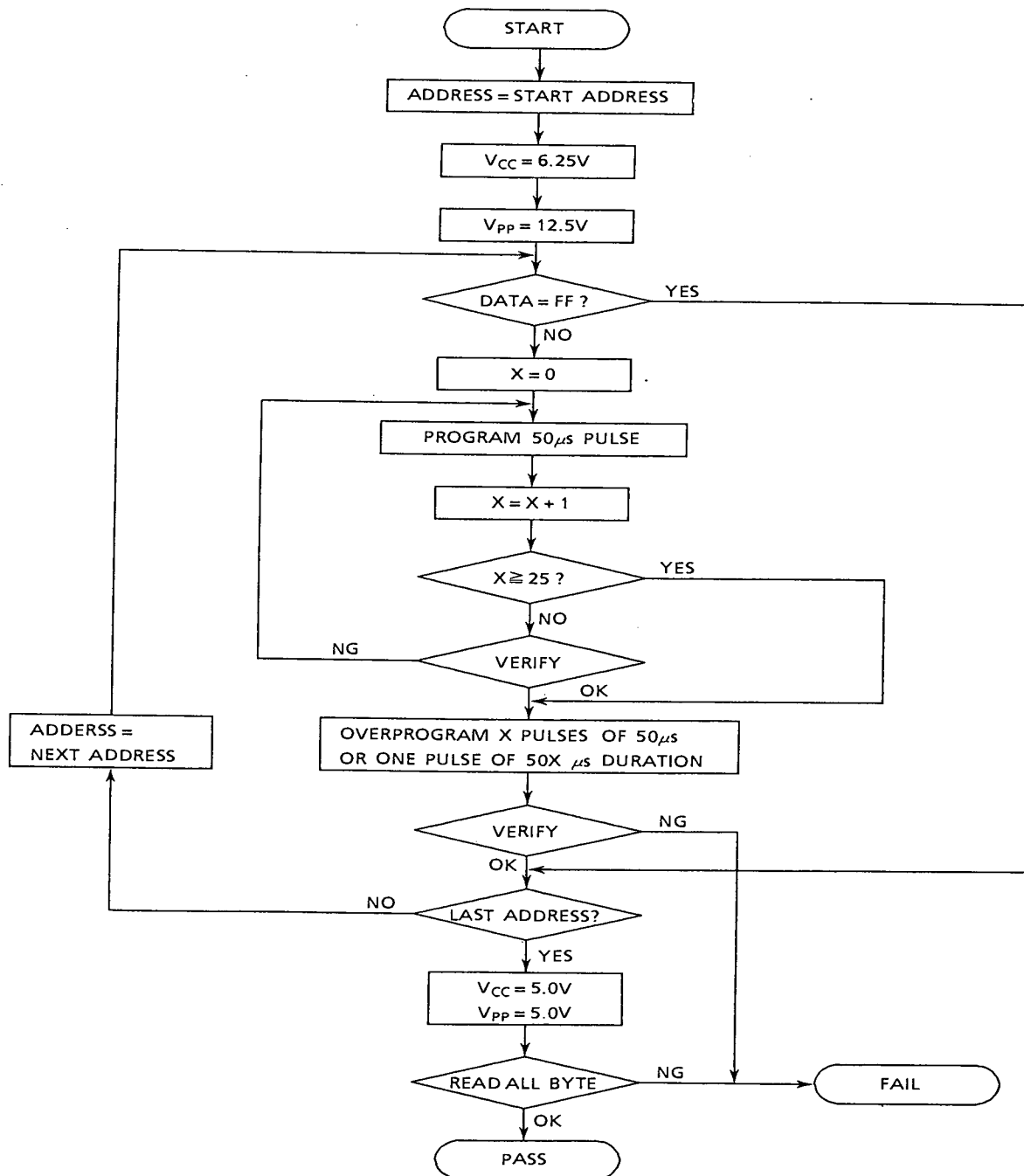
The programming is achieved by applying a single low level $50\mu s$ pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of $50\mu s$ is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with width of 1 time more than that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM MODE

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC544000P / F which identifies its manufacturer and device type.

The programming equipment may reads out manufacturer code and device code from TC544000P / F by using this mode before program operation and automatically set program voltage (V_{pp}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH} .

These two codes possess an odd parity with the parity bit of MSB (D7).

The following table shows electric signature of TC544000P / F.

SIGNATURE \ PINS	A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	0	0	0	1	1	0	0	8C

Notes : A9=12V±0.5V

A1~A8, A10~A18, $\overline{CE}$, $\overline{OE}$ = V_{IL}

TC544000AP/AF-12, -150

524,288 WORD $\times$ 8 BIT CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The TC544000AP/AF is a 524,288 word $\times$ 8 bit one time programmable read only memory, and molded in a 32 pin plastic package. The access time of TC544000AP/AF is 120ns/150ns and has low power standby mode which reduces the power dissipation without increasing access time.

The electrical characteristics and programming method are the same as U.V. EPROM TC574000AD'S once programmed, the TC544000AP/AF can not be erased because of using plastic DIP without transparent window.

FEATURES

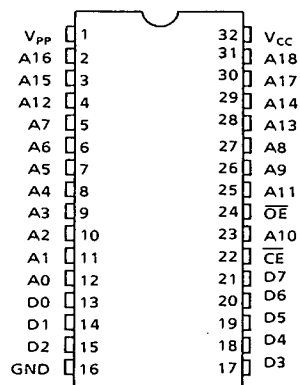
- Peripheral circuit : CMOS
- Memory cell : N-MOS
- Access time

	- 12	- 150
V _{CC}	5V $\pm$ 5%	5V $\pm$ 10%
Temp	0°C~70°C	
t _{ACC}	120ns	150ns

- 12 are satisfied with the specification of - 150

- Low power dissipation
 - Active : 60mA/8.3MHz
 - Standby: 100 μ A (T_a = 70°C)
- High speed programming operation
- Single 5V power supply
- Full static operation
- Input and output TTL compatible
- JEDEC standard 32 pin
- TC544000AP : DIP32-P-600
- TC544000AF : SOP32-P-525

PIN CONNECTION (TOP VIEW)

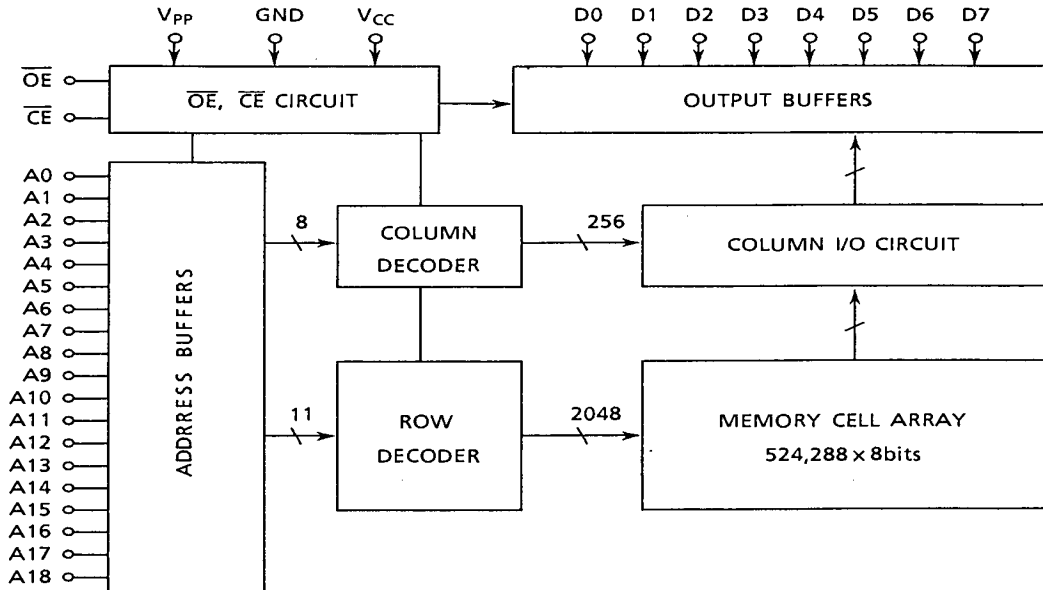


TC544000AP/AF

PIN NAMES

A0~A18	Address Inputs
D0~D7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V _{CC}	V _{CC} Supply Voltage
V _{PP}	Program Supply Voltage
GND	Ground

BLOCK DIAGRAM



MODE SELECTION

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	D0~D7	Power
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*			High Impedance	Standby
Program	L	H	12.50V	6.25V	Data In	Active
Program Inhibit	H	H			High Impedance	
Program Verify	*	L			Data Out	

* : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	-0.6~7.0	V
V_{PP}	Program Supply Voltage	-0.6~14.0	V
V_{IN}	Input Voltage	-0.6~7.0	V
$V_{IN}(A9)$	Input Voltage (A9)	-0.6~13.5	V
$V_{I/O}$	Input/Output Voltage	-0.6~ $V_{CC} + 0.5$	V
P_D	Power Dissipation	1.0/0.6*	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
T_{strg}	Storage Temperature	-65~125	°C
T_{opr}	Operating Temperature	0~70	°C

* : SOP Package

TC544000AP/AF-12, -150

READ OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC544000AP / AF - 12	TC544000AP / AF - 150
V_{IH}	Input High Voltage	$2.2V \sim V_{CC} + 0.3V$	$2.2V \sim V_{CC} + 0.3V$
V_{IL}	Input Low Voltage	$-0.3V \sim 0.8V$	$0.3V \sim 0.8V$
V_{CC}	V_{CC} Power Supply Voltage	$5V \pm 5\%$	$5V \pm 10\%$
V_{PP}	V_{PP} Power Supply Voltage	$V_{CC} - 0.6V \sim V_{CC} + 0.6V$	$V_{CC} - 0.6V \sim V_{CC} + 0.6V$

DC AND OPERATING CHARACTERISTICS ($T_a = 0 \sim 70^\circ C$)

SIMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	—	—	± 10	μA
I_{CCO1}	Operating Current	$\overline{CE} = V_{IL}$ $I_{OUT} = 0mA$	$f = 8.3MHz$	—	60	mA
			$f = 6.7MHz$	—	50	
I_{CCO2}			$f = 1MHz$	—	30	
I_{CCS1}	Standby Current	$\overline{CE} = V_{IH}$	—	—	1	mA
I_{CCS2}		$\overline{CE} = V_{CC} - 0.2V$	—	—	100	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu A$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1mA$	—	—	0.4	V
I_{PP1}	V_{PP} Current	$V_{PP} = V_{CC} \pm 0.6V$	—	—	± 10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 0.4V \sim V_{CC}$	—	—	± 10	μA

AC CHARACTERISTICS ($T_a = 0 \sim 70^\circ C$, $V_{PP} = V_{CC} \pm 0.6V$)

SIMBOL	PARAMETER	TEST CONDITION	TC544000AP / AF - 12		TC544000AP / AF - 150		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE} = \overline{OE} = V_{IL}$	—	120	—	150	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE} = V_{IL}$	—	120	—	150	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE} = V_{IL}$	—	60	—	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE} = V_{IL}$	0	50	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE} = V_{IL}$	0	50	0	60	ns
t_{OH}	Output Data Hold Time	$\overline{CE} = \overline{OE} = V_{IL}$	0	—	0	—	ns

TC544000AP/AF-12 are satisfied with the specification of TC544000AP/AF-150

AC TEST CONDITIONS

- Output Load : 1 TTL Gate and $C_L = 100pF$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V~2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

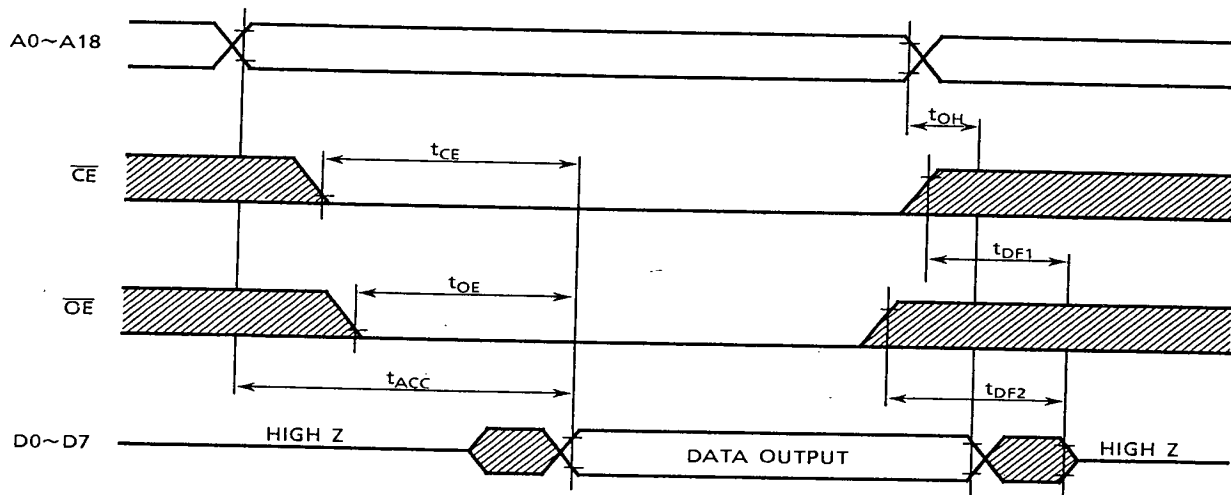
TC544000AP/AF-12, -150

CAPACITANCE* ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$	—	12	PF
C_{OUT}	Output Capacitance	$V_{OUT} = 0\text{V}$	—	15	

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	$V_{CC} + 1.0$	V
V_{IL}	Input Low Voltage	- 0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.20	12.50	12.80	V

DC AND OPREATING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.50\text{V} \pm 0.30\text{V}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	—	—	± 10	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{mA}$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	30	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP} = 12.8\text{V}$	—	—	50	mA

AC PROGRAMMING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.50\text{V} \pm 0.30\text{V}$)

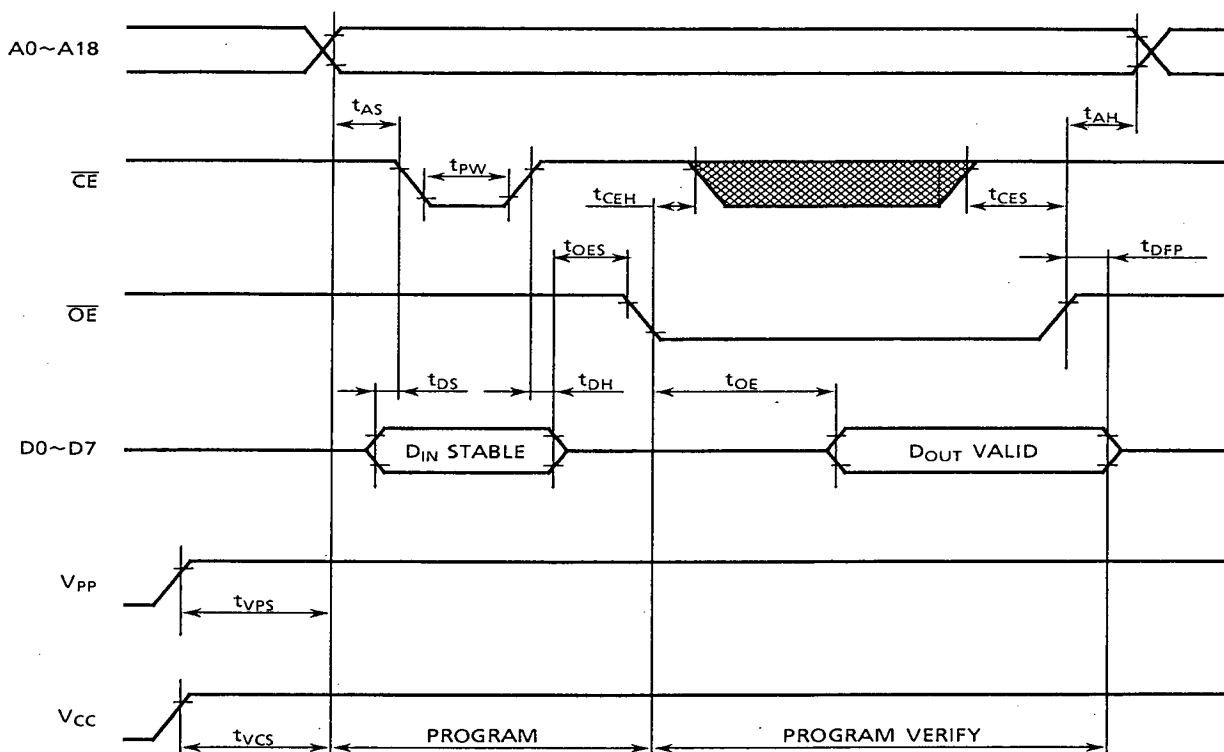
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	0	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	0	—	—	μs
t_{OES}	$\overline{OE}$ Set up Time	—	2	—	—	μs
t_{DS}	Data Set up Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VPS}	V_{PP} Set up Time	—	2	—	—	μs
t_{VCS}	V_{CC} Set up Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	45	50	55	μs
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE} = V_{IH}$	—	—	100	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE} = V_{IH}$	—	—	90	ns

AC TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V~2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAM OPERATION



- Note 1. VCC must be applied simultaneously or before Vpp and cut off simultaneously or after Vpp.
2. Removing the device from socket and setting the device in socket with VPP=12.50V may cause permanent damage to the device.
3. The VPP supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the VPP terminal. When the switching pulse voltage is applied to the VPP terminal, the overshoot voltage of its pulse should not be exceeded 14V.

TC544000AP/AF-12, -150

OPERATION INFORMATION

The TC544000AP/AF's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

MODE		PIN NAMES (NUMBER)	$\overline{CE}$ (22)	$\overline{OE}$ (24)	V_{PP} (1)	V_{CC} (32)	D0~D7 (13~15, 17~21)	POWER
Read Operation ($T_a = 0 \sim 70^\circ\text{C}$)	Read		L	L	5V	5V	Data Out	Active
	Output Deselet		*	H			High Impedance	
	Standby		H	*			High Impedance	Standby
Program Operation ($T_a = 25 \pm 5^\circ\text{C}$)	Program		L	H	12.50V	6.25V	Data In	Active
	Program Inhibit		H	H			High Impedance	
	Program Verify		*	L			Data Out	

Note : H ; V_{IH} , L : V_{IL} , * : V_{IH} or V_{IL}

READ MODE

The TC544000AP/AF has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection. The output enable ($\overline{OE}$) controls the output buffers, independent of device selection. Assuming that $\overline{CE} = \overline{OE} = V_{IL}$, the output data is valid at the outputs after address access time from stabilizing of all addresses. The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE} = V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$, the outputs will be in a high impedance state. So two or more TC544000AP/AF's can be connected together on a common bus line. When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC544000AP/AF has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC544000AP/AF is placed in the standby mode which reduce the operating current to $100\mu\text{A}$ by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC544000AP / AF are in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming. The TC544000AP / AF is in the programming mode when the V_{PP} input is at 12.50V and $\overline{CE}$ is at Low under $\overline{OE} = V_{IH}$.

The TC544000AP / AF can be programmed any location at any time either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with $\overline{OE}$ at V_{IL} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.50V) is applied to V_{PP} terminal, a high level $\overline{CE}$ and $\overline{OE}$ input inhibits the TC544000AP / AF from being programmed.

Programming of two or more TC544000AP / AF's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a low level program pulse is applied to the $\overline{CE}$ of the desired device only and high level signal is applied to the other devices.

HIGH SPEED PROGRAM MODE

The device is set up in the high speed programming mode when the programming voltage (+12.50V) is applied to the V_{PP} terminal with $V_{CC} = 6.25V$.

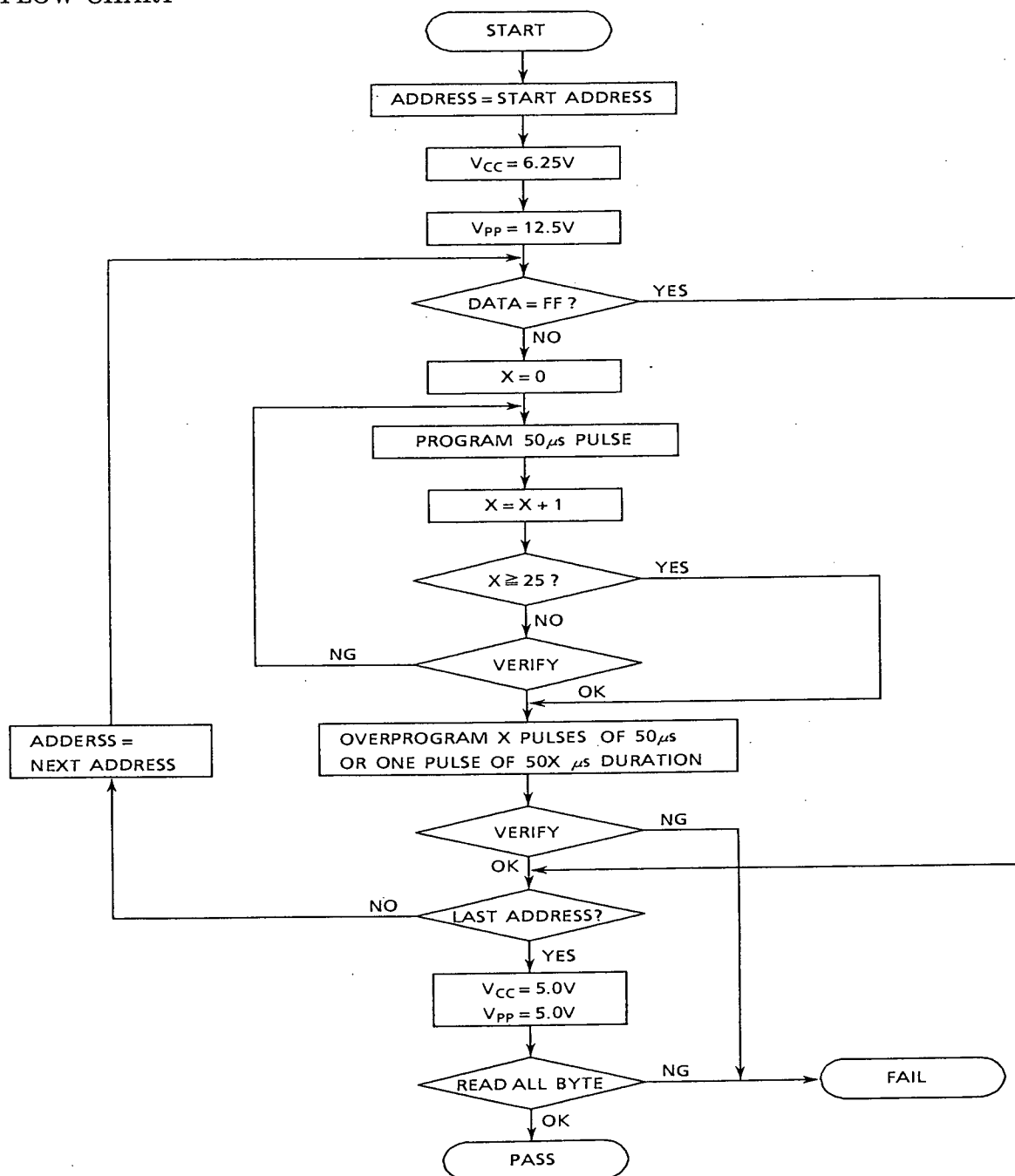
The programming is achieved by applying a single low level $50\mu s$ pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of $50\mu s$ is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with width of 1 time more than that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC} = V_{PP} = 5V$.

HIGH SPEED PROGRAM MODE

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC544000P / F which identifies its manufacturer and device type.

The programming equipment may reads out manufacturer code and device code from TC544000AP / AF by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH} .

These two codes possess an odd parity with the parity bit of MSB (D7).

The following table shows electric signature of TC544000AP / AF.

SIGNATURE \ PINS	A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	0	0	0	1	1	0	0	8C

Notes : A9=12V $\pm$ 0.5V

A1~A8, A10~A18, $\overline{CE}$, $\overline{OE}$ = V_{IL}

TC544200P/F-120,-150

4MEGA BIT (262,144 WORD $\times$ 16BIT / 524,288 WORD $\times$ 8BIT)
CMOS ONE TIME PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The TC544200P/F is a 4,194,304 bit CMOS One time programmable read only memory. It is organized as 256K words of 16 bit or 512K words of 8 bit.

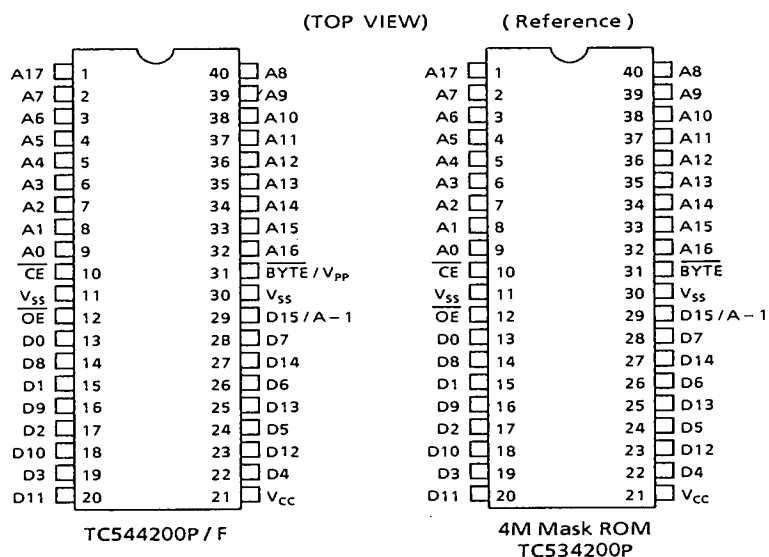
The TC544200P/F is compatible with 40 pin 4M bit Mask ROM. This product is packed in 40 pin standard plastic package. The TC544200P/F is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and low power features with access time of 120ns/150ns and a maximum operating current of 60mA/8.3MHz.

The electrical characteristics and programming method are the same as U. V. EPROM TC574200D's once programmed, the TC544200P/F can not be erased because of using plastic DIP without transparent window.

FEATURES

- Peripheral circuit : CMOS
- Memory cell : NMOS
- Fast access time
($V_{CC}=5V \pm 10\%$, $T_a=0 \sim 70^\circ C$)
 - TC544200P/F-120 : 120ns
 - TC544200P/F-150 : 150ns
- Single 5V power supply
- Low power dissipation
Standby : 100 μA
- Full static operation
- Input and output TTL compatible
- Three state output
- High speed programming operation : tpw 50 μs
- 4M MROM compatible pinout : TC534200P
- TC544200P : DIP40-P-600
- TC544200F : SOP40-P-525

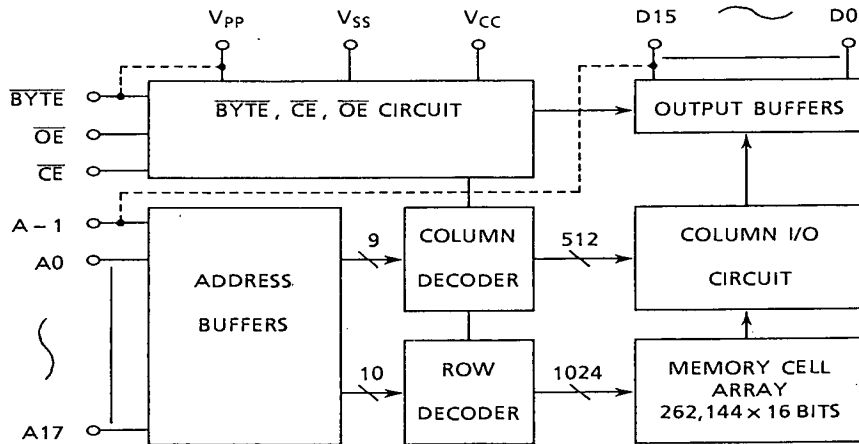
PIN CONNECTION



PIN NAMES

A0~A17	Address Input
D0~D14	Output (Input)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
D15 / A - 1	Output (Input) / Address Input
$\overline{BYTE} / V_{PP}$	Word, Byte select Input / Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage
V_{SS}	Ground

BLOCK DIAGRAM



MODE SELECTION

MODE \ PINS	$\overline{\text{CE}}$	$\overline{\text{OE}}$	BYTE / V_{pp}	V_{CC}	D0~D7	D8~D14	D15 / A-1	Power
Read (16 Bit)	L	L	H	5V	Data Out			Active
Read (Lower 8 Bit)	L	L	L		Data Out (Lower 8 Bit)	High Impedance	L	
Read (Upper 8 Bit)	L	L	L		Data Out (Upper 8 Bit)	High Impedance	H	
Output Deselect	L	H	H		High Impedance			
			L		High Impedance	*		
Standby	H	*	H		High Impedance			
			L	High Impedance	*			
Program	L	H	12.5V	6.25V	Data In			Active
Program Inhibit	H	H			High Impedance			
Program Verify	*	L			Data Out			

Note: H = V_{IH}, L = V_{IL}, * = V_{IH} or V_{IL}

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{CC}	V _{CC} Power Supply Voltage	-0.6~7.0	V
V _{PP}	Program Supply Voltage	-0.6~14.0	V
V _{IN}	Input Voltage	-0.6~7.0	V
V _{IN} (A9)	Input Voltage (A9)	-0.6~13.5	V
V _{I/O}	Input/Output Voltage	-0.6~V _{CC} + 0.5	V
P _D	Power Dissipation	1.5	W
T _{SOLDER}	Soldering Temperature · Time	260·10	°C · sec
T _{STRG}	Storage Temperature	-65~150	°C
T _{OPR}	Operating Temperature	0~70	°C

TC544200P/F-120, -150

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage	-0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.50	5.00	5.50	V

D.C. AND OPERATING CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0V \sim V_{CC}$	—	—	± 10	μA
I_{CCO1}	Operating Current	$\overline{CE} = 0V$ $I_{OUT} = 0\text{mA}$ $f = 8.3\text{MHz}$	—	—	60	mA
I_{CCO2}		$\overline{CE} = 0V$ $I_{OUT} = 0\text{mA}$ $f = 1\text{MHz}$	—	—	30	mA
I_{CCS1}	Standby Current	$\overline{CE} = V_{IH}$	—	—	1	mA
I_{CCS2}		$\overline{CE} = V_{CC} - 0.2V$	—	—	100	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{mA}$	—	—	0.4	V
I_{PP1}	V_{PP} Current	$V_{PP} = 0V \sim V_{CC} + 0.6V$	—	—	± 10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 0.4V \sim V_{CC}$	—	—	± 10	μA

A.C. CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	- 120		- 150		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	—	120	—	150	ns
t_{CE}	$\overline{CE}$ to Output Valid	—	120	—	150	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	60	—	70	ns
t_{DF1}	$\overline{CE}$ to Output in High Impedance	0	50	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High Impedance	0	50	0	60	ns
t_{OH}	Output Data Hold Time	0	—	0	—	ns
t_{BT}	BYTE to Output Valid	—	120	—	150	ns
t_{BTD}	BYTE to Output in High Impedance	—	60	—	70	ns

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and $CL = 100\text{PF}$
- Input Pulse Rise and Fall Time : 10ns Max
- Input Pulse Levels : 0.45V and 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

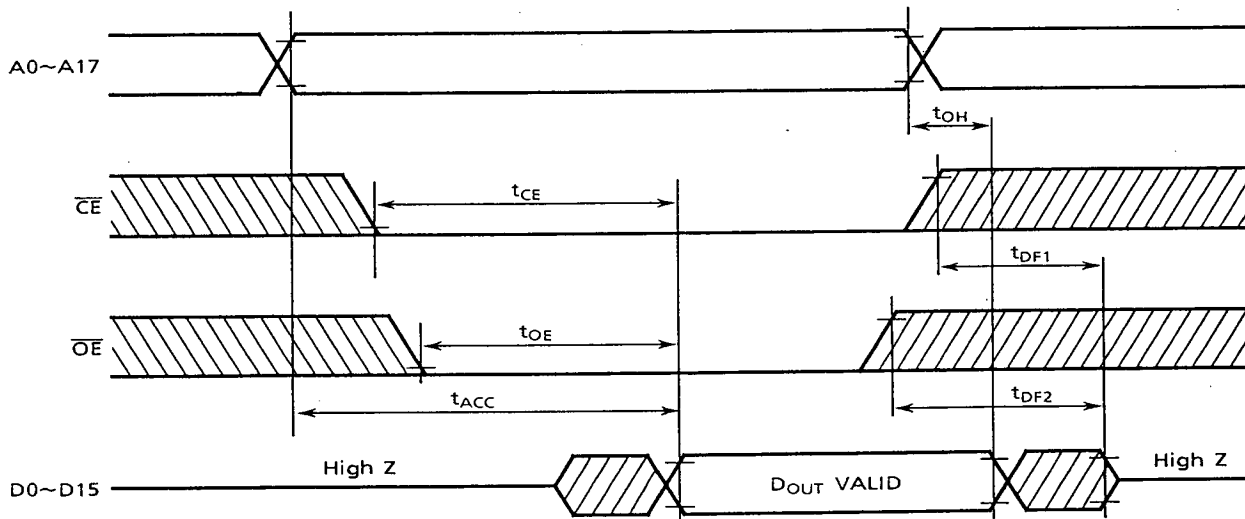
CAPACITANCE * ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance	$V_{IN} = 0\text{V}$	—	6	10	μF
C_{IN2}	Input Capacitance ($\overline{\text{BYTE}}/V_{PP}$)	$V_{IN} = 0\text{V}$	—	110	120	μF
C_{OUT}	Output Capacitance	$V_{OUT} = 0\text{V}$	—	10	12	μF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS

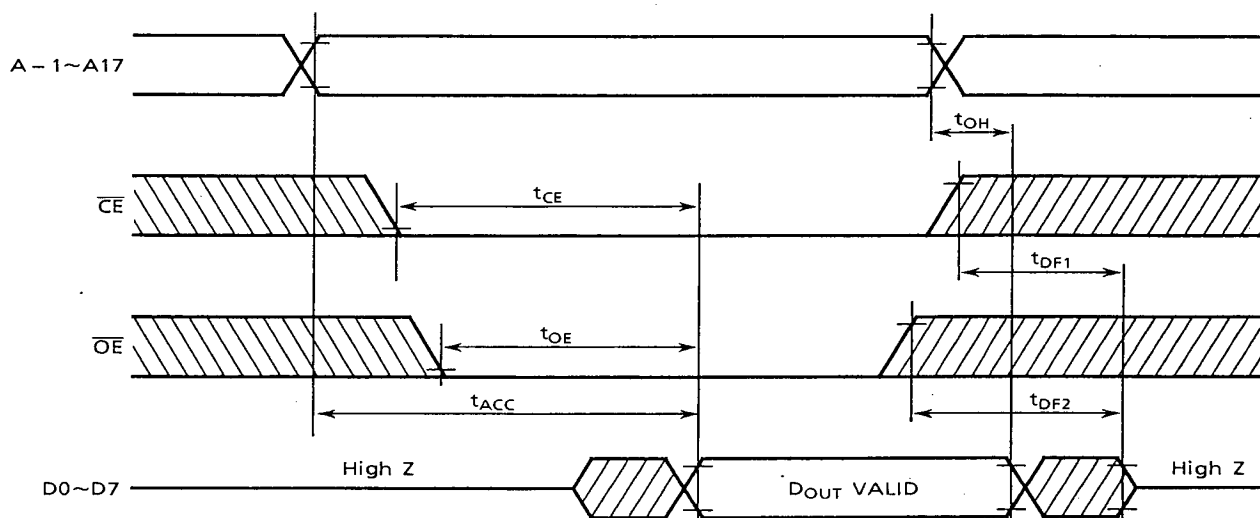
WORD - WIDE READ MODE



Note: $\overline{\text{BYTE}}/V_{PP} = V_{IH}$

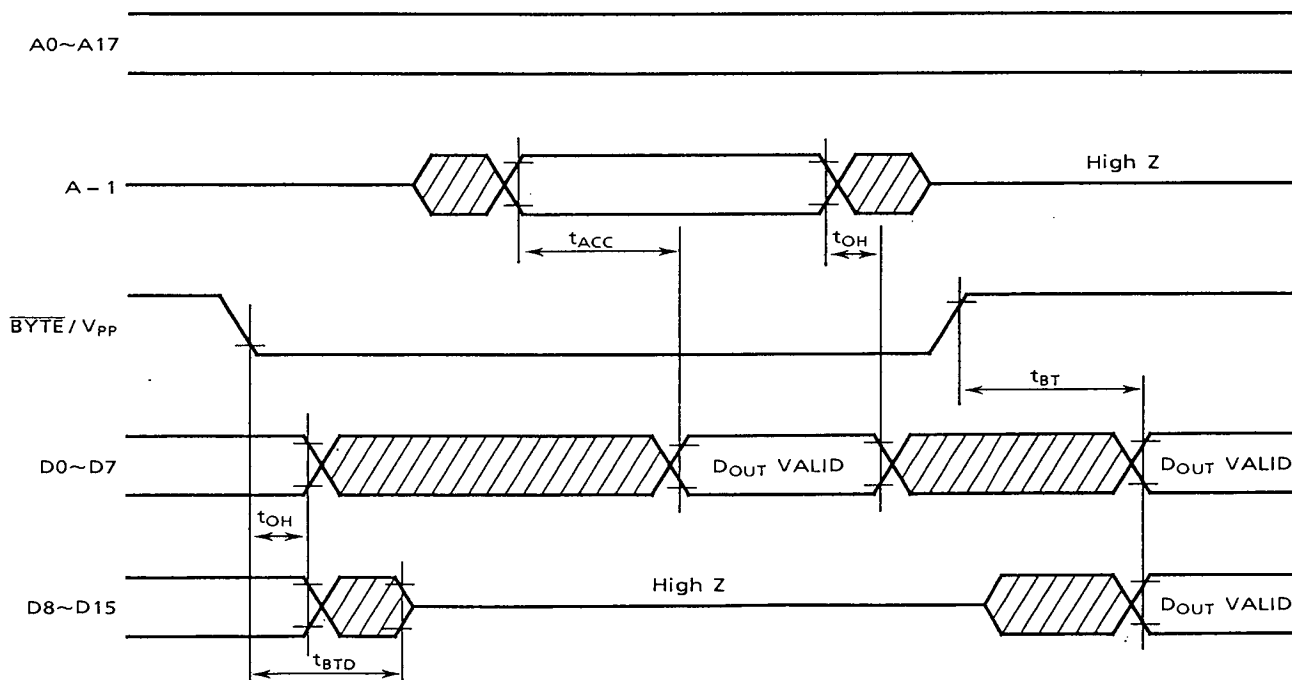
TC544200P/F-120,-150

BYTE-WIDE READ MODE



Note: $\overline{BYTE} / V_{pp} = V_{IL}$

BYTE TRANSITION



Note: $\overline{CE}, \overline{OE} = V_{IL}$

HIGH SPEED PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	$V_{CC} + 1.0$	V
V_{IL}	Input Low Voltage	-0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.20	12.50	12.80	V

D.C. AND OPERATING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25 \pm 0.25\text{V}$, $V_{PP} = 12.50 \pm 0.30\text{V}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0\text{V} \sim V_{CC}$	—	—	± 10	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{mA}$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	40	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP} = 12.8\text{V}$	—	—	50	mA

A.C. PROGRAMMING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25 \pm 0.25\text{V}$, $V_{PP} = 12.50 \pm 0.30\text{V}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	0	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	0	—	—	μs
t_{OES}	$\overline{OE}$ Setup Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VPS}	V_{PP} Setup Time	—	2	—	—	μs
t_{VCS}	V_{CC} Setup Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	—	45	50	55	μs
t_{OPW}	Overprogram Pulse Width	Note 1	45	50	55	μs
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE} = V_{IH}$	—	—	100	ns
t_{DFP}	$\overline{OE}$ to Output in High Impedance	$\overline{CE} = V_{IH}$	—	—	90	ns

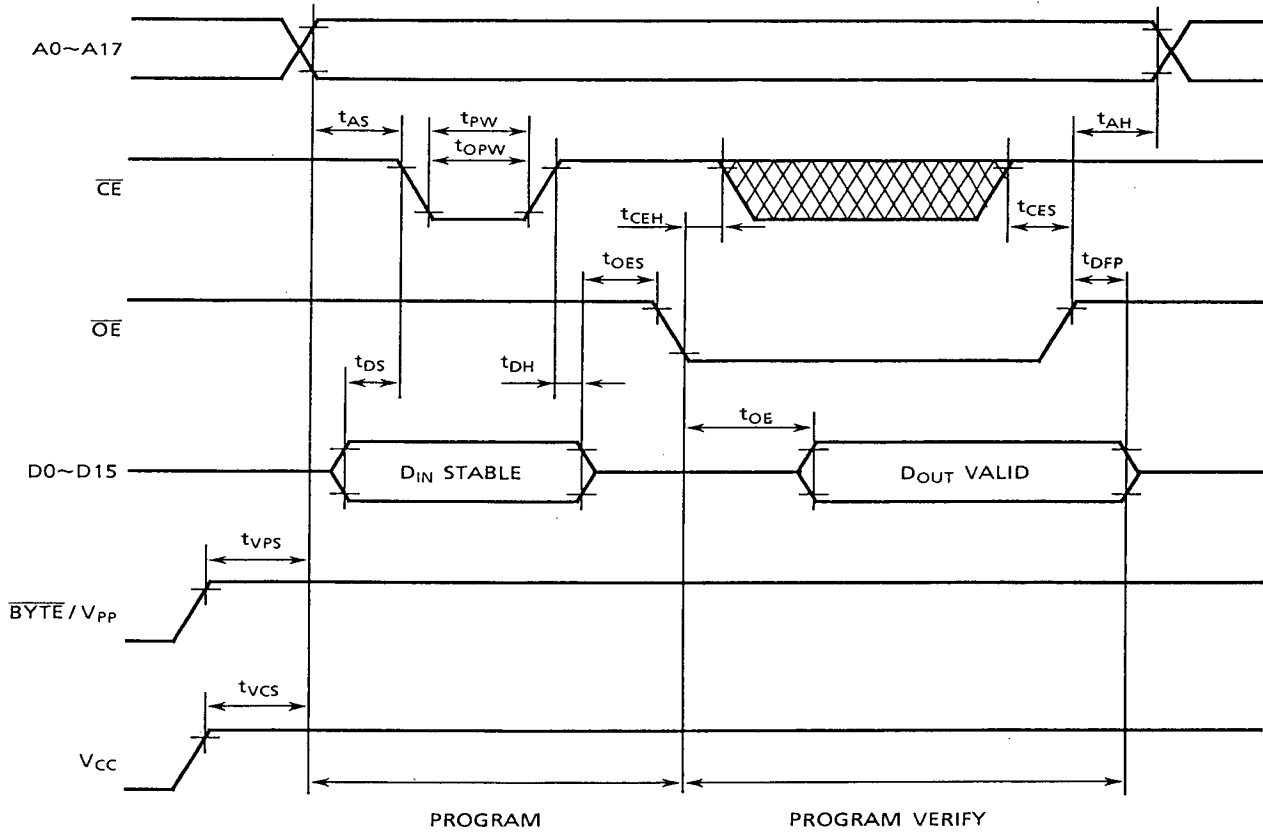
A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and $CL = 100\text{PF}$
- Input Pulse Rise and Fall Time : 10ns Max
- Input Pulse Levels : 0.45V and 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

Note 1 : t_{OPW} depends on the program pulse width which is required in the initial program.

TIMING WAVEFORMS

HIGH SPEED PROGRAM OPERATION



- Note: 1. V_{CC} must be applied simultaneously or before V_{pp} and cut off simultaneously or after V_{pp} .
2. Removing the device from socket and setting the device in socket with $V_{pp}=12.50V$ may cause permanent damage to the device.
3. The V_{pp} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{pp} terminal. When the switching pulse voltage is applied to the V_{pp} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

OPERATION INFORMATION

The TC544200P/F's eight operation mode are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PINS	$\overline{CE}$	$\overline{OE}$	BYTE / V _{PP}	V _{CC}	D0~D7	D8~D14	D15 / A - 1	Power
Read (16 Bit)	L	L	H	5V	Data Out			Active
Read (Lower 8 Bit)	L	L	L		Data Out (Lower 8 Bit)	High Impedance	L	
Read (Upper 8 Bit)	L	L	L		Data Out (Upper 8 Bit)	High Impedance	H	
Output Deselect	L	H	H		High Impedance			
			L		High Impedance		*	
Standby	H	*	H		High Impedance			
			L	High Impedance		*		
Program	L	H	12.5V	6.25V	Data In			Active
Program Inhibit	H	H			High Impedance			
Program Verify	*	L			Data Out			

Note: H = V_{IH}, L = V_{IL}, * = V_{IH} or V_{IL}

READ MODE

The TC544200P/F has the $\overline{BYTE}/V_{PP}$ terminal that selects word-wide output and byte-wide output. When $\overline{BYTE}/V_{PP}$ is set to V_{IH}, the word-wide output is selected, and D15/A-1 pin is used for D15 data output.

When $\overline{BYTE}/V_{PP}$ is set to V_{IL}, the byte-wide output is selected, and D15/A-1 pin is used for A-1 address input. When A-1 is set to V_{IL} in this condition, the data output is selected lower 8 bits of the 16 bit data which has been programmed. When A-1 is set to V_{IH}, the data output is selected upper 8 bits.

The TC544200P/F has two control function. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection. The output enable ($\overline{OE}$) controls the output buffers, independent of device selection. Assuming that $\overline{CE} = \overline{OE} = V_{IL}$, the output data is valid at the outputs after address access time from stabilizing of all addresses. The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}). Assuming that $\overline{CE} = V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$, the outputs will be in a high impedance state. So two or more TC544200P/F's can be connected together on a common bus line. When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC544200P/F has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC544200P/F is placed in the standby mode which reduces the operating current to 100 μ A by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

TC544200P/F-120,-150

PROGRAM MODE

Initially, when received by customers, all bits of the TC544200P/F are in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit location by electrically programming. The TC544200P/F is in the programming mode when the V_{PP} input is at 12.50V and $\overline{CE}$ is at TTL-Low under $\overline{OE}=V_{IH}$. Data to be programmed must be applied 16 bits in parallel to the data pins.

The TC544200P/F can be programmed any location at anytime either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ at V_{IL} . The programmed data should be compared with the original word-wide (16 bit) data.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (12.50V) is applied to V_{PP} terminal, a high level $\overline{CE}$ input inhibits the TC544200P/F from being programmed. Programming of two or more EPROMs in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

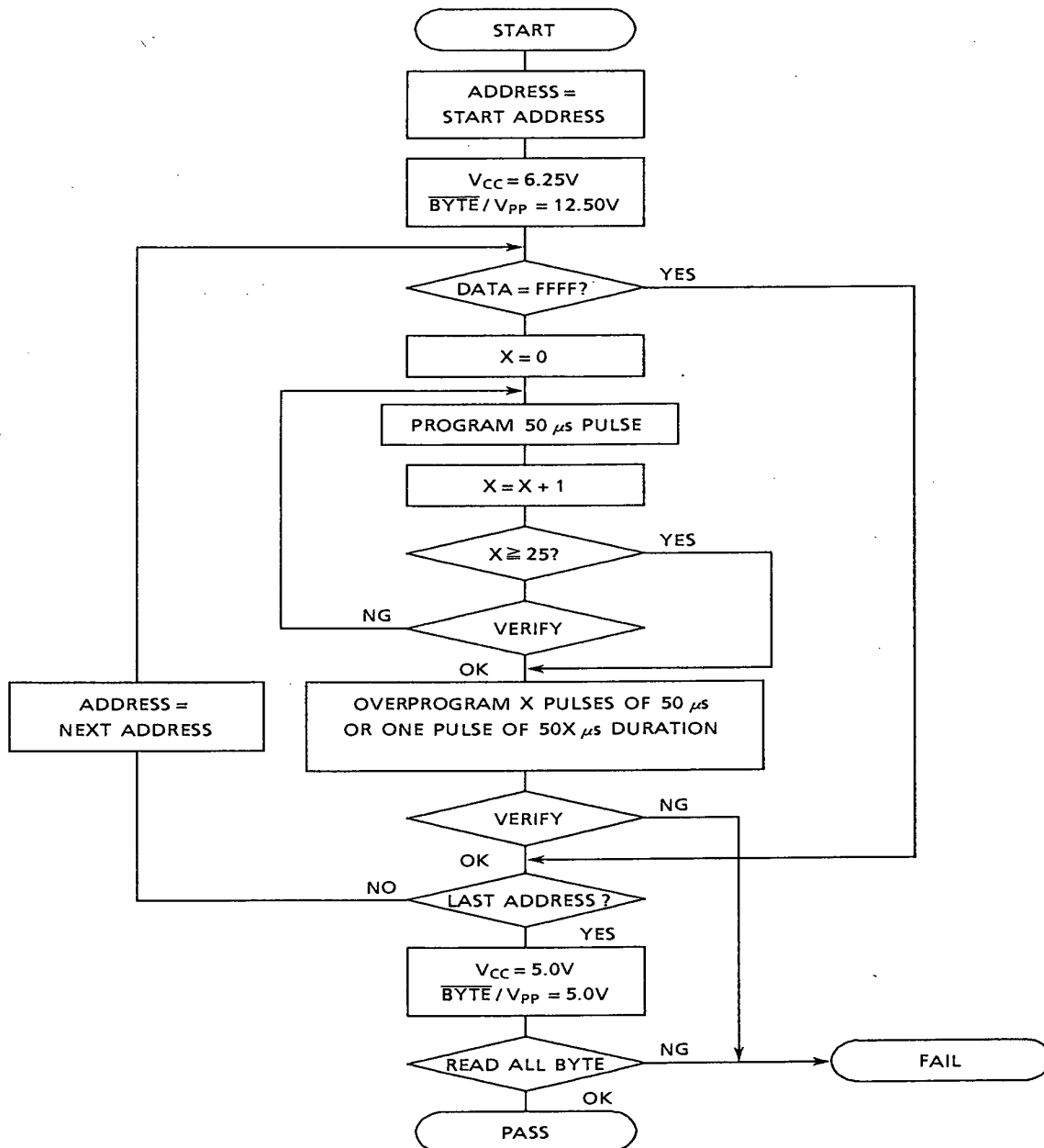
HIGH SPEED PROGRAM MODE

The device is set up the high speed programming mode when the programming voltage (12.50V) is applied to the V_{PP} terminal with $V_{CC}=6.25V$. The programming is achieved by applying a single TTL low level $50\mu s$ pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of $50\mu s$ is applied and then the programmed data is verified. This should be repeated until the program operates correctly(max. 25 times).

After correctly programming the selected address, the overprogram pulse of same length that needed for initial programming should be applied. When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM MODE

FLOW CHART



TC544200P/F-120, -150

ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC544200P / F which identifies its manufacturer and device type. The programming equipment may read out manufacturer code and device code from TC544200P / F by using this mode before program operation and automatically set program voltage (Vpp) and algorithm.

Electric signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of (D7).

The following table shows electric signature of TC544200P / F.

SIGNATURE \ PINS	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX DATA
Manufacturer Code	V _{IL}	*	*	*	*	*	*	*	*	1	0	0	1	1	0	0	0	**98
Device Code	V _{IH}	*	*	*	*	*	*	*	*	1	0	0	0	1	1	1	1	**8F

Note: A9 = 12.0V ± 0.5V
A1 – A8, A10 – A17, $\overline{CE}$, $\overline{OE}$ = V_{IL}
 $\overline{BYTE} / VPP$ = V_{IH}

* Don't care

SILICON STACKED GATE MOS INTEGRATED CIRCUIT

TC544096P/F-120, -150

4 MEGA BIT (262,144 WORD $\times$ 16 BIT)

CMOS ONE TIME PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The TC544096P/F is a 262,144 word $\times$ 16 bit CMOS one time programmable read only memory. The TC544096P/F is JEDEC standard pin configuration.

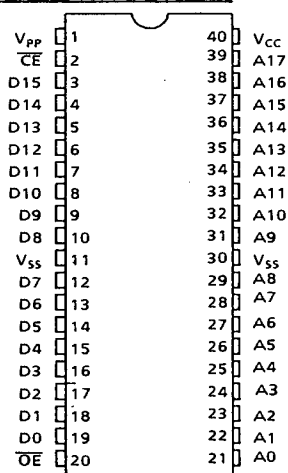
TC544096P/F is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 60mA/8.3MHz and access time of 120ns/150ns.

The electrical characteristics and programming method and the same as U.V. EPROM TC574096D's once programmed, the TC544096P/F can not be erased because of using plastic package without transparent window.

FEATURES

- Peripheral circuit : CMOS
- Memory cell : N-MOS
- Fast access time
 - TC544096P/F-120 : 120ns ($V_{CC}=5.0V \pm 10\%$)
 - TC544096P/F-150 : 150ns ($V_{CC}=5.0V \pm 10\%$)
- Low power dissipation
 - Active : 60mA/8.3MHz
 - Standby : 100 μ A
- Single 5V power supply
- Full static operation
- High speed programming operation : tpw 50 μ s
- Input and output TTL compatible
- JEDEC standard 40 pin
- TC544096P : DIP40 - P - 600
- TC544096F : SOP40 - P - 525

PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A17	Address Inputs
D0~D15	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{CC}	V_{CC} Supply Voltage
V_{PP}	Program Supply Voltage
V_{SS}	Ground

READ OPERATION

AC/DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	CHARACTERISTIC	TC544096P / F - 120, 150
T _a	Ambient Temperature	0~70°C
V _{CC}	V _{CC} Power Supply Voltage	5V ± 10%
V _{PP}	V _{PP} Power Supply Voltage	0V~V _{CC} + 0.6V

DC AND OPERATING CHARACTERISTICS

SYMBOL	CHARACTERISTIC	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Current	V _{IN} = 0~V _{CC}	—	—	± 10	μA
I _{CCO1}	Operating Current	$\overline{CE} = 0V$ f = 8.3MHz	—	—	60	mA
I _{CCO2}		I _{OUT} = 0mA f = 1MHz	—	—	30	mA
I _{CCS1}	Standby Current	$\overline{CE} = V_{IH}$	—	—	1	mA
I _{CCS2}		$\overline{CE} = V_{CC} - 0.2V$	—	—	100	μA
V _{IH}	Input High Voltage	—	2.2	—	V _{CC} + 0.3	V
V _{IL}	Input Low Voltage	—	- 0.3	—	0.8	V
V _{OH}	Output High Voltage	I _{OH} = - 400μA	2.4	—	—	V
V _{OL}	Output Low Voltage	I _{OL} = 2.1mA	—	—	0.4	V
I _{PP1}	V _{PP} Current	V _{PP} = 0V~V _{CC} + 0.6V	—	—	± 10	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0.4V~V _{CC}	—	—	± 10	μA

AC CHARACTERISTICS

SYMBOL	CHARACTERISTIC	TC544096P / F - 120		TC544096P / F - 150		UNIT
		MIN.	MAX.	MIN.	MAX.	
t _{ACC}	Address Access Time	—	120	—	150	ns
t _{CE}	$\overline{CE}$ to Output Valid	—	120	—	150	
t _{OE}	$\overline{OE}$ to Output Valid	—	60	—	70	
t _{DF1}	$\overline{CE}$ to Output in High-Z	—	50	—	60	
t _{DF2}	$\overline{OE}$ to Output in High-Z	—	50	—	60	
t _{OH}	Output Data Hold Time	0	—	0	—	

AC TEST CONDITIONS

Output Load : 1 TTL Gate and C_L = 100pF
 Input Pulse Rise and Fall Times : 10ns Max.
 Input Pulse Levels : 0.45V to 2.4V
 Timing Measurement Reference Levels: Inputs 0.8V and 2.2V Outputs 0.8V and 2.0V

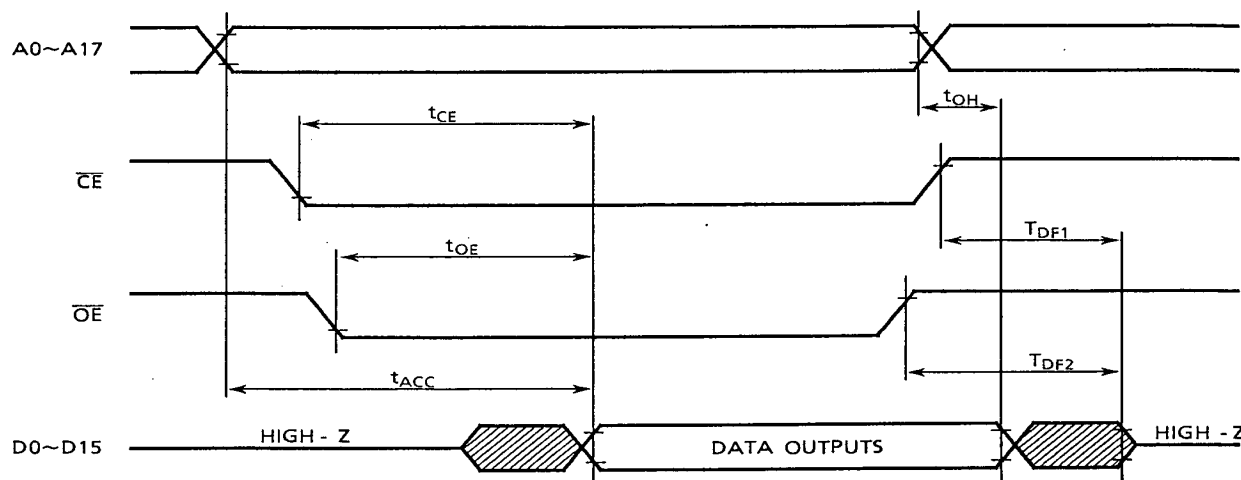
TC544096P/F-120, -150

CAPACITANCE *(Ta = 25°C, f = 1MHz)

SYMBOL	CHARACTERISTIC	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = 0V	—	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	—	10	12	

* This characteristic is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	$V_{CC} + 1.0$	V
V_{IL}	Input Low Voltage	-0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.20	12.50	12.80	V

DC AND OPERATING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.50\text{V} \pm 0.30\text{V}$)

SYMBOL	CHARACTERISTIC	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	—	—	± 10	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{mA}$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	30	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP} = 12.8\text{V}$	—	—	50	mA

AC PROGRAMMING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.50\text{V} \pm 0.30\text{V}$)

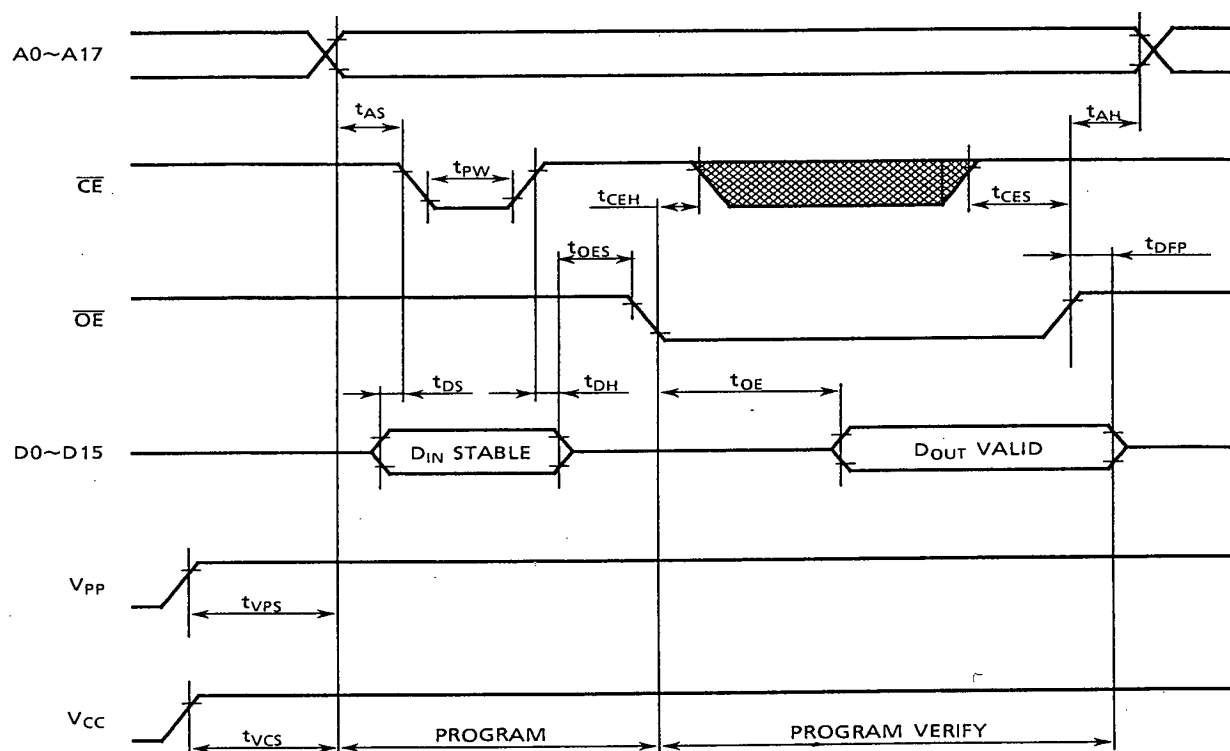
SYMBOL	CHARACTERISTIC	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	0	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	0	—	—	μs
t_{OES}	$\overline{OE}$ Set up Time	—	2	—	—	μs
t_{DS}	Data Set up Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VPS}	V_{PP} Set up Time	—	2	—	—	μs
t_{VCS}	V_{CC} Set up Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	—	45	50	55	μs
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE} = V_{IH}$	—	—	100	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE} = V_{IH}$	—	—	90	ns

AC TEST CONDITIONS

- Output Load : 1 TTL Gate and $C_L = 100\text{pF}$
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAM OPERATION



- Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP} .
2. Removing the device from socket and setting the device in socket with $V_{PP}=12.50V$ may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

OPERATION INFORMATION

The TC544096P/F's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

MODE		PIN NAMES	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	D0~D15	POWER
Read Operation	Read		L	L	5V	5V	Data Out	Active
	Output Deselect		*	H			High Impedance	Standby
	Standby		H	*				
Program Operation ($T_a = 25 \pm 5^\circ\text{C}$)	Program		L	H	12.50V	6.25V	Data In	Active
	Program Inhibit		H	H			High Impedance	
	Program Verify		*	L			Data Out	

Note : H ; V_{IH} , L : V_{IL} , * : V_{IH} or V_{IL}

READ MODE

The TC544096P/F has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection. The output enable ($\overline{OE}$) controls the output buffers, independent of device selection. Assuming that $\overline{CE} = \overline{OE} = V_{IL}$, the output data is valid at the outputs after address access time from stabilizing of all addresses. The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE} = V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$, the outputs will be in a high impedance state. So two or more TC544096P/F's can be connected together on a common bus line. When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC544096P/F has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC544096P/F is placed in the standby mode which reduce the operating current to $100\mu\text{A}$ by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

TC544096P/F-120,-150

PROGRAM MODE

Initially, when received by customers, all bits of the TC544096P/F are in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming. The TC544096P/F is in the programming mode when the V_{PP} input is at 12.50V and $\overline{CE}$ is at Low under $\overline{OE}=V_{IH}$.

The TC544096P/F can be programmed any location at any time either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with $\overline{OE}$ at V_{IL} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.50V) is applied to V_{PP} terminal, a high level $\overline{CE}$ and $\overline{OE}$ input inhibits the TC544096P/F from being programmed.

Programming of two or more TC544096P/F's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a low level program pulse is applied to the $\overline{CE}$ of the desired device only and high level signal is applied to the other devices.

HIGH SPEED PROGRAM MODE

The device is set up in the high speed programming mode when the programming voltage (+12.50V) is applied to the V_{PP} terminal with $V_{CC}=6.25V$.

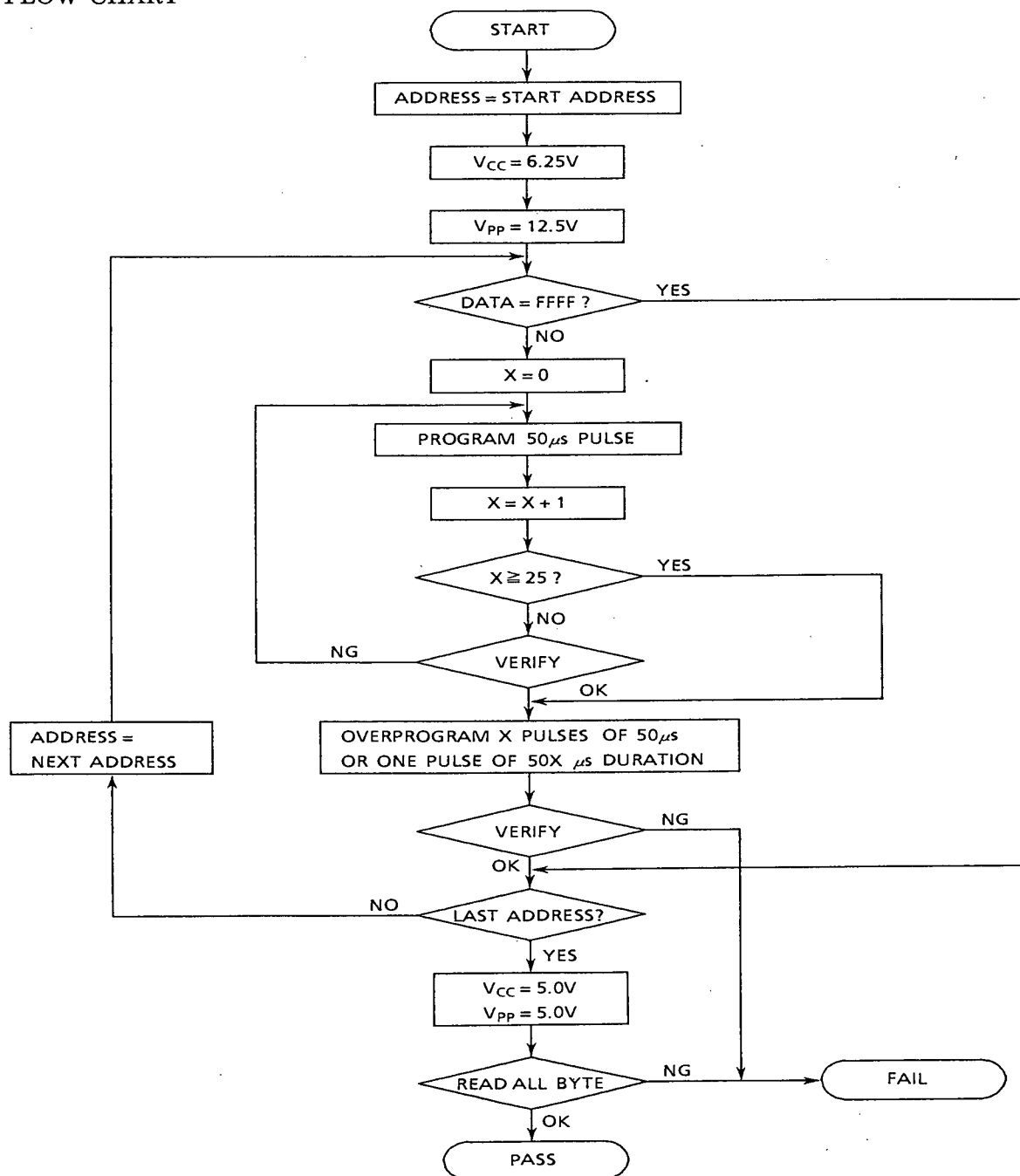
The programming is achieved by applying a single low level $50\mu s$ pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of $50\mu s$ is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with width of 1 time more than that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM MODE

FLOW CHART



TC544096P/F-120,-150

ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC544096P / F which identifies it's manufacture and device type.

The programming equipment may read out manufacturer code and device code from TC544096P / F by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH} .

These two codes possess an odd parity with the parity bit of (D7).

The following table shows electric signature of TC544096P / F.

SIGNATURE	PINS	A ₀	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	HEX DATA
Manufacturer Code		V_{IL}	*	*	*	*	*	*	*	*	1	0	0	1	1	0	0	0	**98
Device Code		V_{IH}	*	*	*	*	*	*	*	*	0	0	0	0	1	1	1	0	**0E

Notes : A9=12V±0.5V,

A₁ - A₈, A₁₀ - A₁₇, $\overline{CE}$, $\overline{OE}$ = V_{IL}

* : Don't care

4-3 **FLASH/NAND E²PROM**

SILICON STACKED GATE MOS INTEGRATED CIRCUIT

TENTATIVE

TC58257AP/AF-20, -25

TC58257AP / AF 32,768 WORD $\times$ 8 BIT ELECTRICALLY CHIP ERASABLE AND PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

TC58257AP/AF is a 32,768 word $\times$ 8 bit electrically chip erasable and programmable read only memory, and molded in a 28 pin plastic package. The TC58257AP / AF's access time is 200ns / 250ns, and has low power standby mode which reduces the power dissipation without increasing access time. The electrical characteristics are the same as U.V. EPROM TC57256AD's. For program operation, the programming is achieved by using the high speed programming mode. The TC58257AP / AF has an electrically chip erasing mode which can erase whole bits at the same time.

FEATURES

Peripheral circuit : CMOS

Memory cell : NMOS

Fast access time : TC58257AP/AF-20 200ns

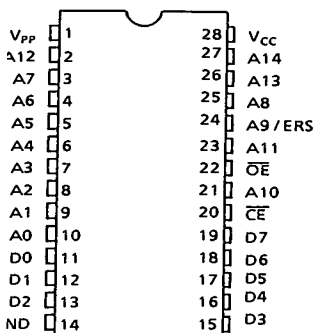
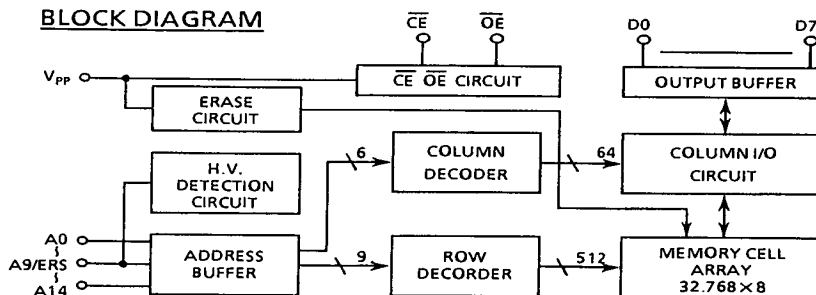
TC58257AP/AF-25 250ns

Low power dissipation

Active : 30mA / 5MHz

Standby : 100 μ A

- Full static operation
- High speed programming mode
- Electrically chip erasing mode
- Inputs and outputs TTL compatibility
- Pin compatible with MASK ROM TC53257P, TMM23256P, EPROM TMM27256D/AD, and TC57256D/AD, one time PROM TMM24256P/AP/AF and TC54256P/AP/AF
- TC58257AP : DIP28 - P - 600
- TC58257AF : SOP28 - P - 450

PIN CONNECTION (TOP VIEW)BLOCK DIAGRAMNAMESMODE SELECTION

Pin	Mode	$\overline{CE}$	$\overline{OE}$	A9	V _{PP}	V _{CC}	A0~A8 (10~14)	D0~D7	Power
A14	Address Inputs								
D7	Output (Input)								
	Chip Enable Input								
	Output Enable Input								
ERS	Address and Enable Control Input								
	Program and Erase Power Supply Voltage								
	VCC Power Supply Voltage								
	Ground								
	Read	L	L	*	5V	5V	*	Data Output	Active
	Output Deselect	*	H	*			*	High Impedance	
	Standby	H	*	*			*	High Impedance	Standby
	Program	L	H	*			*	Data Input	
	Program Inhibit	H	*	*	12.75V or 12V	6.25V or 5V	*	High Impedance	Active
	Program Verify	*	L	*			*	Data Out	
	Chip Erase	L	H		12.75V or 12V	5V	*	Don't Care	
	Chip Erase Inhibit	H	*				*	High Impedance	Active

* : VIH or VIL

TC58257AP/AF-20, -25

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{CC}	V _{CC} Power Supply Voltage	- 0.6~7.0	V
V _{PP}	Program Supply Voltage	- 0.6~14.0	V
V _{IN}	Input Voltage	- 0.6~7.0	V
V _{I/O}	Input/Output Voltage	- 0.6~V _{CC} + 0.5	V
P _D	Power Dissipation	1.0 / 0.6*	W
T _{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
T _{STG}	Storage Temperature	- 65~125	°C
T _{OPR}	Operating Temperature	- 10~70	°C
N _{EW}	Erase Write Endurance	100	Cycles

* SOP

READ OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{IH}	Input High Voltage	2.2	-	V _{CC} + 0.3	V
V _{IL}	Input Low Voltage	- 0.3	-	0.8	V
V _{CC}	V _{CC} Power Supply Voltage	4.50	5.00	5.50	V
V _{PP}	V _{PP} Power Supply Voltage	V _{CC} -0.6	V _{CC}	V _{CC} + 0.6	V

DC AND OPERATING CHARACTERISTICS (Ta = - 10~70°C, VCC = 5V ± 10%)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Current	V _{IN} = 0~V _{CC}	-	-	± 10	μA
I _{CCO}	Operating Current	$\overline{CE}$ = 0V, I _{OUT} = 0mA, f = 5MHz	-	-	30	mA
I _{CCS1}	Standby Current	$\overline{CE}$ = V _{IH}	-	-	1	mA
I _{CCS2}		$\overline{CE}$ = V _{CC} - 0.2V	-	-	100	μA
V _{OH}	Output High Voltage	I _{OH} = - 400μA	2.4	-	-	V
V _{OL}	Output Low Voltage	I _{OL} = 2.1mA	-	-	0.4	V
I _{PP1}	VPP Current	V _{PP} = V _{CC} - 0.6~V _{CC} + 0.6	-	-	± 10	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0.4~V _{CC}	-	-	± 10	μA

TC58257AP/AF-20,-25

AC CHARACTERISTICS ($T_a = -10 \sim 70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, $V_{PP} = V_{CC} \pm 0.6V$)

SYMBOL	PARAMETER	TEST CONDITION	-20		-25		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE} = \overline{OE} = V_{IL}$	—	200	—	250	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE} = V_{IL}$	—	200	—	250	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE} = V_{IL}$	—	70	—	100	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE} = V_{IL}$	0	60	0	90	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE} = V_{IL}$	0	60	0	90	ns
t_{OH}	Output Data Hold Time	$\overline{CE} = \overline{OE} = V_{IL}$	0	—	0	—	ns

AC TEST CONDITIONS

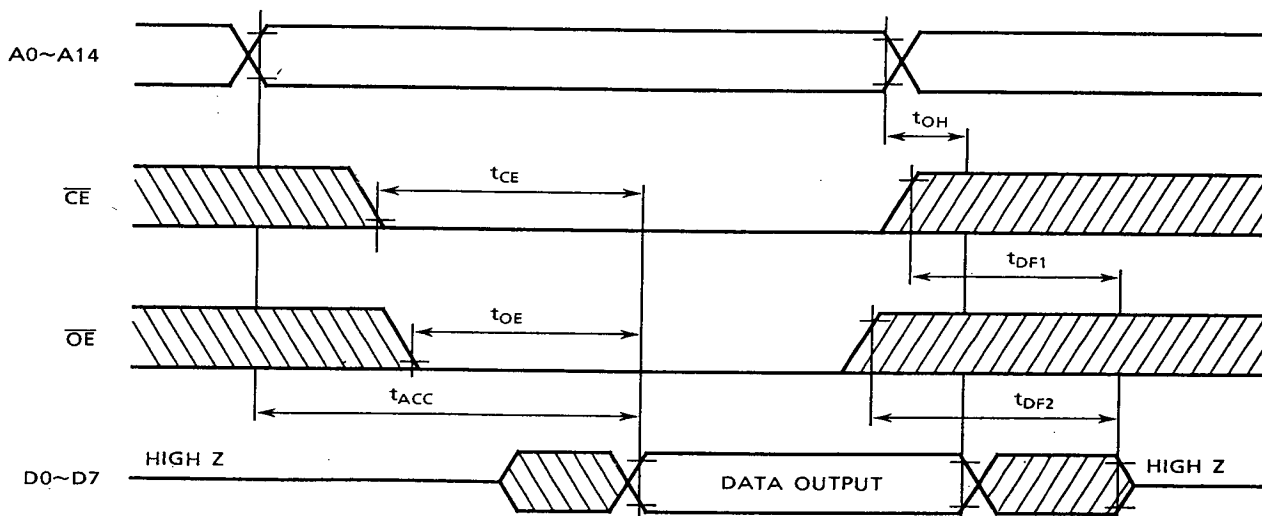
- Output Load : 1 TTL Gate and $C_L = 100\text{pF}$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V~2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE* ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0V$	—	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	—	8	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



TC58257AP/AF-20, -25

PROGRAM OPERATION (MODE – I)

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	$V_{CC} + 1.0$	V
V_{IL}	Input Low Voltage	– 0.3	–	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.50	12.75	13.00	V

DC AND OPERATING CHARACTERISTICS ($T_a = -10 \sim 70^\circ\text{C}$, $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.75\text{V} \pm 0.25\text{V}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	–	–	10	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4	–	–	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{mA}$	–	–	0.4	V
I_{CC}	V_{CC} Supply Current	–	–	–	40	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP} = 13.0\text{V}$	–	–	50	mA

AC PROGRAMMING CHARACTERISTICS ($T_a = -10 \sim 70^\circ\text{C}$, $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.75\text{V} \pm 0.25\text{V}$)

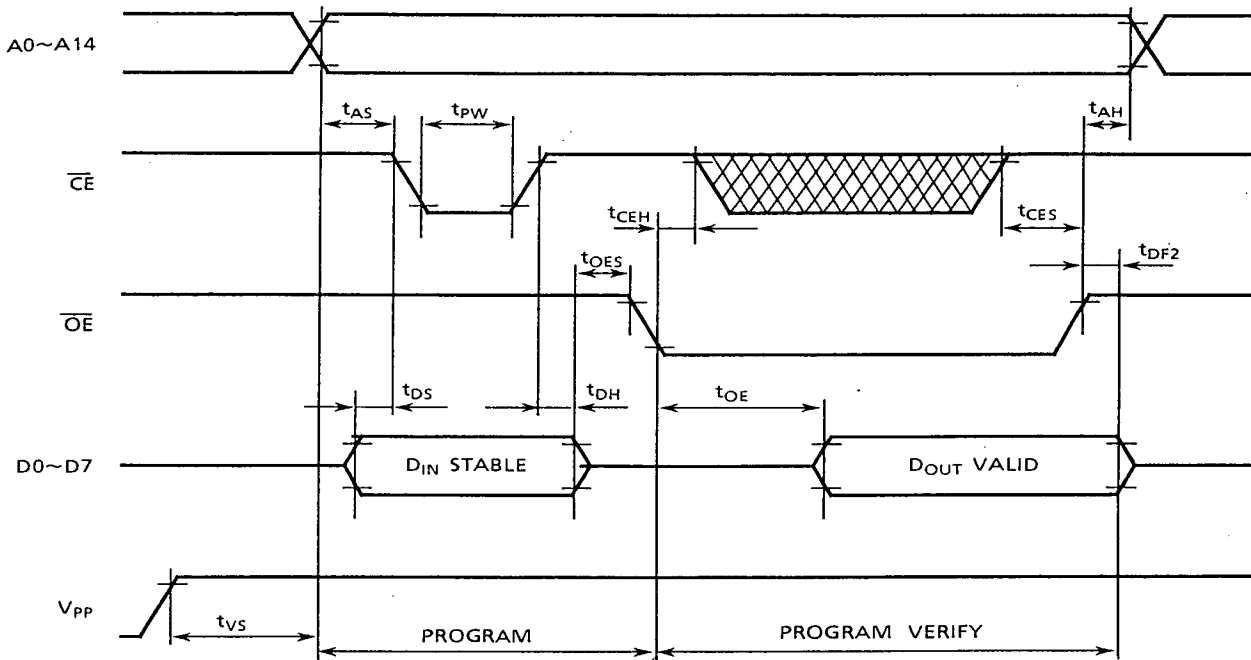
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	–	2	–	–	μs
t_{AH}	Address Hold Time	–	2	–	–	μs
t_{CES}	$\overline{CE}$ Setup Time	–	0	–	–	μs
t_{CEH}	$\overline{CE}$ Hold Time	–	0	–	–	μs
t_{OES}	$\overline{OE}$ Setup Time	–	2	–	–	μs
t_{OEH}	$\overline{OE}$ Hold Time	–	2	–	–	μs
t_{DS}	Data Setup Time	–	2	–	–	μs
t_{DH}	Data Hold Time	–	2	–	–	μs
t_{VS}	V_{PP} Setup Time	–	2	–	–	μs
t_{PW}	Program Pulse Width	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	95	100	105	μs
t_{OE}	$\overline{OE}$ to Output Valid	–	–	–	150	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	–	–	–	130	ns

AC TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V~2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V.

TIMING WAVEFORMS (PROGRAM) (MODE - I)

($V_{CC} = 6.25V \pm 0.25V$, $V_{PP} = 12.75V \pm 0.25V$)



- Note
1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP} .
 2. Removing the device from socket and setting the device in socket with $V_{PP} = 12.75V$ may cause permanent damage to the device.
 3. The V_{PP} supply voltage is permitted up to 14V for program operation.
So the voltage over 14V should not be applied to the V_{PP} terminal.
When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

TC58257AP/AF-20, -25

PROGRAM OPERATION (MODE – II)

DC RECOMMENDED OPERATING CONDITIONS

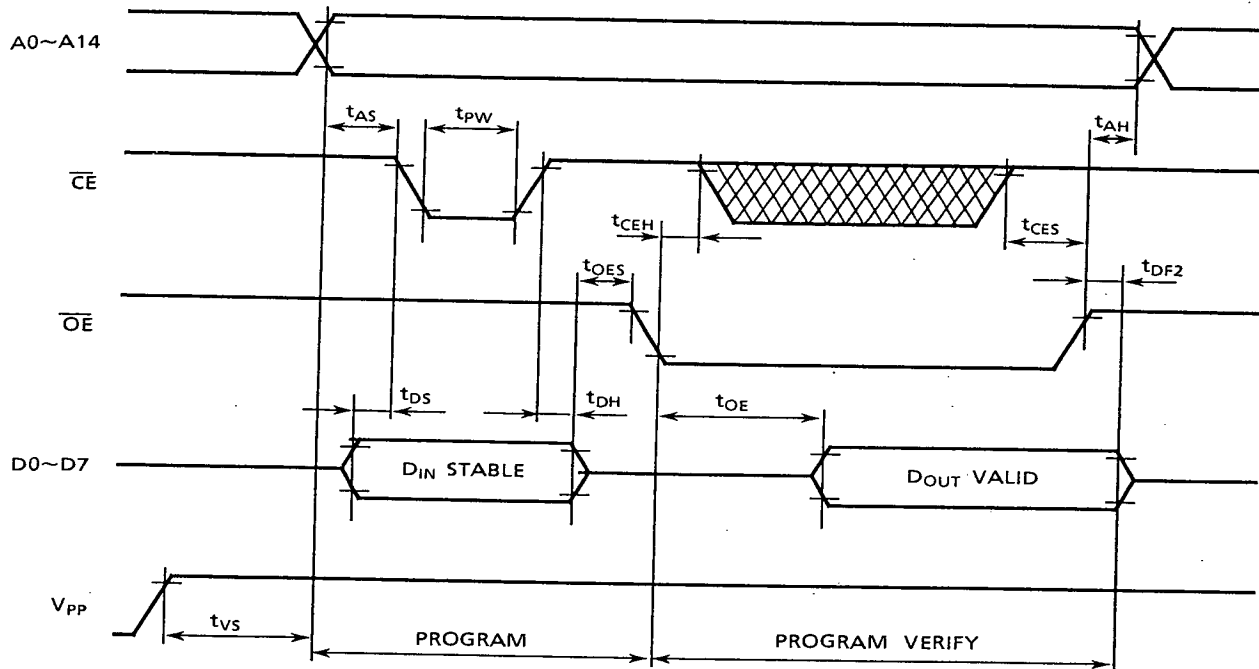
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	$V_{CC} + 1.0$	V
V_{IL}	Input Low Voltage	– 0.3	–	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.5	5.0	5.5	V
V_{PP}	V_{PP} Power Supply Voltage	11.5	12.0	12.5	V

DC AND OPERATING CHARACTERISTICS ($T_a = -10 \sim 70^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$, $V_{PP} = 12.0\text{V} \pm 0.5\text{V}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	–	–	10	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4	–	–	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{mA}$	–	–	0.4	V
I_{CC}	V_{CC} Supply Current	–	–	–	40	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP} = 12.5\text{V}$	–	–	50	mA

AC PROGRAMMING CHARACTERISTICS ($T_a = -10 \sim 70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{PP} = 12.0\text{V} \pm 0.5\text{V}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	–	2	–	–	μs
t_{AH}	Address Hold Time	–	2	–	–	μs
t_{CES}	$\overline{CE}$ Setup Time	–	0	–	–	μs
t_{CEH}	$\overline{CE}$ Hold Time	–	0	–	–	μs
t_{OES}	$\overline{OE}$ Setup Time	–	2	–	–	μs
t_{OEH}	$\overline{OE}$ Hold Time	–	2	–	–	μs
t_{DS}	Data Setup Time	–	2	–	–	μs
t_{DH}	Data Hold Time	–	2	–	–	μs
t_{VS}	V_{PP} Setup Time	–	2	–	–	μs
t_{PW}	Program Pulse Width	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	0.95	1.0	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	0.95	1.0	26.25	ms
t_{OE}	$\overline{OE}$ to Output Valid	–	–	–	150	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	–	–	–	130	ns

$$(V_{CC} = 5.0V \pm 10\%, V_{PP} = 12.0V \pm 0.5V)$$
$$(V_{CC} = 5.0V \pm 10\%, V_{PP} = 12.0V \pm 0.5V)$$


Note

1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP} .
2. Removing the device from socket and setting the device in socket with $V_{PP}=12.0V$ may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted up to 14V for program operation.
So the voltage over 14V should not be applied to the V_{PP} terminal.
When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

TC58257AP/AF-20, -25

ERASE OPERATION (MODE - I)

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	$V_{CC} + 1.0$	V
V_{IL}	Input Low Voltage	-0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.5	5.0	5.5	V
V_{PP}	V_{PP} Power Supply Voltage	12.50	12.75	13.00	V
V_{IHH}	Input High Voltage H	11.5	12.0	12.5	V

DC AND OPERATING CHARACTERISTICS ($T_a = -10 \sim 70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	—	—	± 10	μA
I_{LIE}	A9 / ERS Input Current	$A9 / ERS = 0 \sim V_{IHH}$	—	—	± 100	μA
I_{CC}	V_{CC} Supply Current	—	—	—	40	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP} = 13.0V$	—	—	50	mA

AC ERASING CHARACTERISTICS ($T_a = -10 \sim 70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, $V_{PP} = 12.75V \pm 0.25V$)

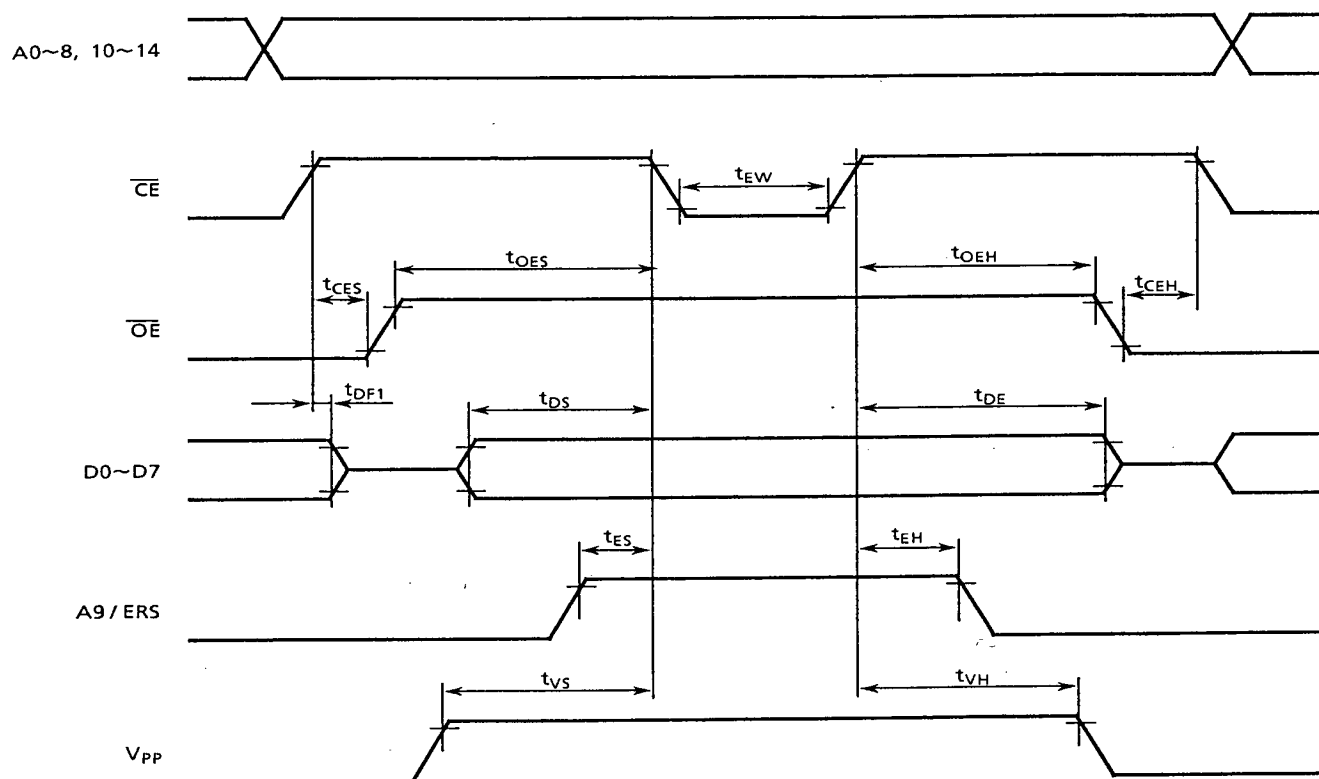
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{CES}	$\overline{CE}$ Setup Time	—	2	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	2	—	—	μs
t_{OES}	$\overline{OE}$ Setup Time	—	2	—	—	μs
$t_{OE H}$	$\overline{OE}$ Hold Time	—	500	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	500	—	—	μs
t_{VS}	V_{PP} Setup Time	—	2	—	—	μs
t_{VH}	V_{PP} Hold Time	—	500	—	—	μs
t_{ES}	A9 / ERS Setup Time	—	2	—	—	μs
t_{EH}	A9 / ERS Hold Time	—	2	—	—	μs
t_{EW}	Erase Pulse Width	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, $A9 = V_{IHH}$	950	1000	1050	ms
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE} = V_{IL}$	—	—	150	ns

Input Pulse Rise and Fall Time: 10ns Max.
Input Pulse Levels : 0.45V~2.4V

PROGRAM VERIFY MODE

TIMING WAVEFORMS (ERASE MODE – I)

(VCC = 5V ± 10%, VPP = 12.75V ± 0.25V)



Note 1. VCC must be applied simultaneously or before VPP and cut off simultaneously or after VPP.

2. Removing the device from socket and setting the device in socket with VPP=12.75V may cause permanent damage to the device.
3. The VPP supply voltage is permitted up to 14V for erase operation.
So the voltage over 14V should not be applied to the VPP terminal.
When the switching pulse voltage is applied to the VPP terminal, the overshoot voltage of its pulse should not be exceeded 14V.

TC58257AP/AF-20, -25

ERASE OPERATION (MODE – II)

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	$V_{CC} + 1.0$	V
V_{IL}	Input Low Voltage	– 0.3	–	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.5	5.0	5.5	V
V_{PP}	V_{PP} Power Supply Voltage	11.5	12.0	12.5	V
V_{IHH}	Input High Voltage H	11.5	12.0	12.5	V

DC AND OPERATING CHARACTERISTICS ($T_a = -10 \sim 70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$)

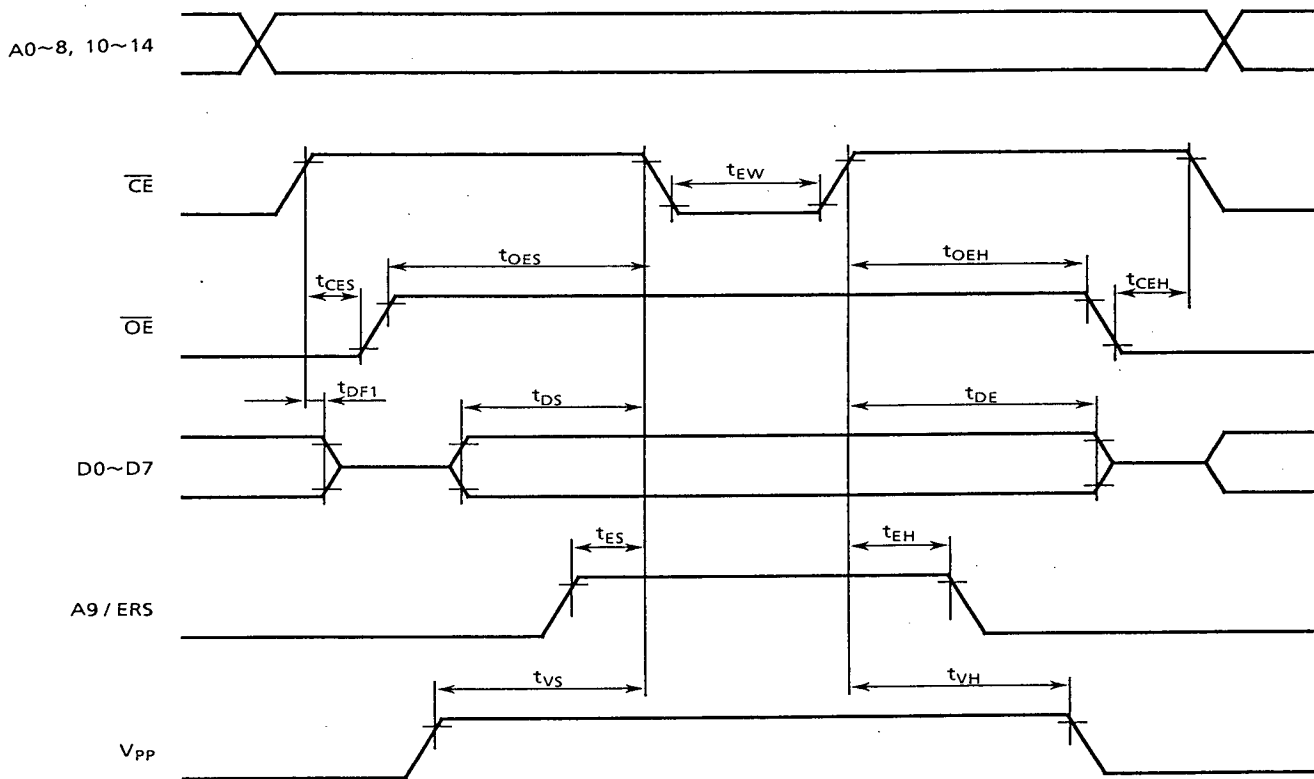
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	–	–	± 10	μA
I_{LIE}	A9 / ERS Input Current	$A9 / ERS = 0 \sim V_{IHH}$	–	–	± 100	μA
I_{CC}	V_{CC} Supply Current	–	–	–	40	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP} = 12.5V$	–	–	50	mA

AC ERASING CHARACTERISTICS ($T_a = -10 \sim 70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, $V_{PP} = 12.0V \pm 0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{CES}	$\overline{CE}$ Setup Time	–	2	–	–	μs
t_{CEH}	$\overline{CE}$ Hold Time	–	2	–	–	μs
t_{OES}	$\overline{OE}$ Setup Time	–	2	–	–	μs
t_{OEH}	$\overline{OE}$ Hold Time	–	500	–	–	μs
t_{DS}	Data Setup Time	–	2	–	–	μs
t_{DH}	Data Hold Time	–	500	–	–	μs
t_{VS}	V_{PP} Setup Time	–	2	–	–	μs
t_{VH}	V_{PP} Hold Time	–	500	–	–	μs
t_{ES}	A9 / ERS Setup Time	–	2	–	–	μs
t_{EH}	A9 / ERS Hold Time	–	2	–	–	μs
t_{EW}	Erase Pulse Width	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, $A9 = V_{IHH}$	1950	2000	2050	ms
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE} = V_{IL}$	–	–	150	ns

Input Pulse Rise and Fall Time: 10ns Max.
Input Pulse Levels : 0.45V~2.4V

TIMING WAVEFORMS (ERASE MODE - II)
($V_{CC} = 5V \pm 10\%$, $V_{PP} = 12.0V \pm 0.5V$)



- Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP} .
2. Removing the device from socket and setting the device in socket with $V_{PP}=12.0V$ may cause permanent damage to the device.
 3. The V_{PP} supply voltage is permitted up to 14V for erase operation.
So the voltage over 14V should not be applied to the V_{PP} terminal.
When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

TC58257AP/AF-20, -25

(MODE – I)

Mode	pin	$\overline{CE}$	$\overline{OE}$	A9	V _{PP}	V _{CC}	D0~D7	Power
Read Operation	Read	L	L	*	5V	5V	Data Out	Active
	Output Deselect	*	H	*			High Impedance	
	Standby	H	*	*			High Impedance	Standby
Program Operation	Program	L	H	*	12.75V	6.25V	Data In	Active
	Program Inhibit	H	*	*			High Impedance	
	Program Verify	*	L	*			Data Out	
Erase Operation	Erase	L	H	12V	12.75V	5V	Don't Care	Active
	Erase Inhibit	H	*				High Impedance	

Note : H ; V_{IH}, L ; V_{IL}, * ; V_{IH} or V_{IL}

(MODE – II)

Mode	pin	$\overline{CE}$	$\overline{OE}$	A9	V _{PP}	V _{CC}	D0~D7	Power
Read Operation	Read	L	L	*	5V	5V	Data Out	Active
	Output Deselect	*	H	*			High Impedance	
	Standby	H	*	*			High Impedance	Standby
Program Operation	Program	L	H	*	12V	5V	Data In	Active
	Program Inhibit	H	*	*			High Impedance	
	Program Verify	*	L	*			Data Out	
Erase Operation	Erase	L	H	12V	12V	5V	Don't Care	Active
	Erase Inhibit	H	*				High Impedance	

Note : H ; V_{IH}, L ; V_{IL}, * ; V_{IH} or V_{IL}

STANDBY MODE

The TC58257AP/AF has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC58257AP/AF is placed in the standby mode which reduce the operating current to 100 μ A by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC58257AP/AF are in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming. The TC58257AP/AF is in the programming mode when the V_{PP} input is at 12.75V or 12.0V and $\overline{CE}$ is at TTL-Low under $\overline{OE}$ =V_{IH}. The TC58257AP/AF can be programmed any location at anytime either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check if desired data is correctly programmed on the programmed bits. The verify is accomplished with $\overline{OE}$ at V_{IL} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (12.75V or 12.0V) is applied to V_{PP} terminal, a high level $\overline{CE}$ input inhibits the TC58257AP/AF from being programmed. Programming of two or more TC58257AP/AF's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other device.

HIGH SPEED PROGRAMMING MODE - I

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the V_{PP} terminal with $V_{CC}=6.25V$. The programming is achieved by applying a single TTL low level $100\mu s$ pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of $100\mu s$ is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

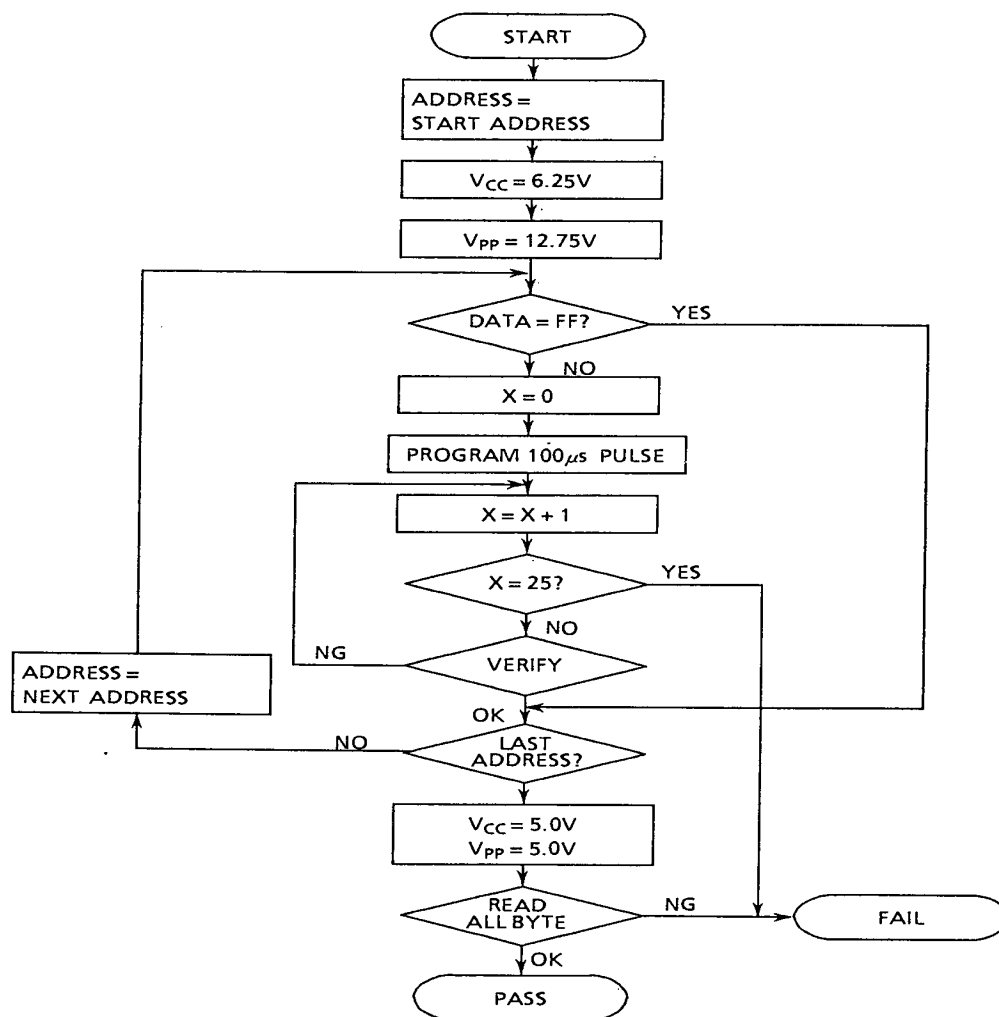
HIGH SPEED PROGRAMMING MODE - II

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.0V) is applied to the V_{PP} terminal with $V_{CC}=5.0V$. The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

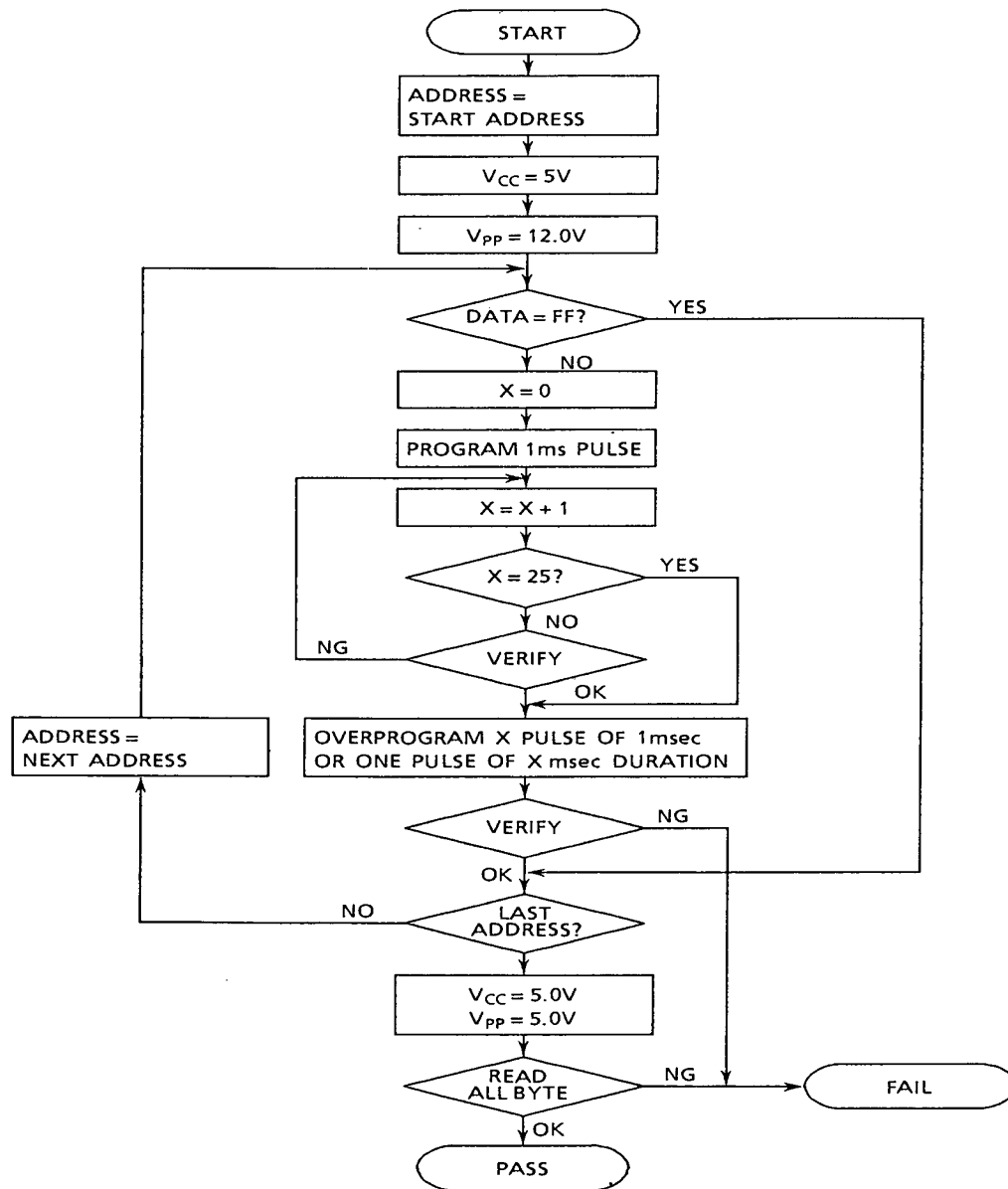
After correctly programming the selected address, one additional program pulse with pulse width 1 time that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM MODE - I FLOW CHART



HIGH SPEED PROGRAM MODE - II FLOW CHART



TC58257AP/AF-20, -25

ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC58257AP/AF which identifies its manufacture and device type.

The programming equipment may read out manufacture code and device code from TC58257AP/AF by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH} . These two codes possess an odd parity with the parity bit of MSB (D7).

The following table shows electric signature of TC58257AP/AF.

SIGNATURE \ PINS	A0 (10)	D7 (19)	D6 (18)	D5 (17)	D4 (16)	D3 (15)	D2 (13)	D1 (12)	D0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	0	1	0	0	1	0	0	A4

Notes: A9=12V $\pm$ 0.5V

A1~A8, A10~A14, $\overline{CE}$, $\overline{OE}$ = V_{IL}

SILICON STACKED GATE MOS INTEGRATED CIRCUIT

TENTATIVE

TC584000P/F/FT/TR

4MEGA BIT (524,288 WORD×8 BIT) CMOS NAND E²PROM

DESCRIPTION

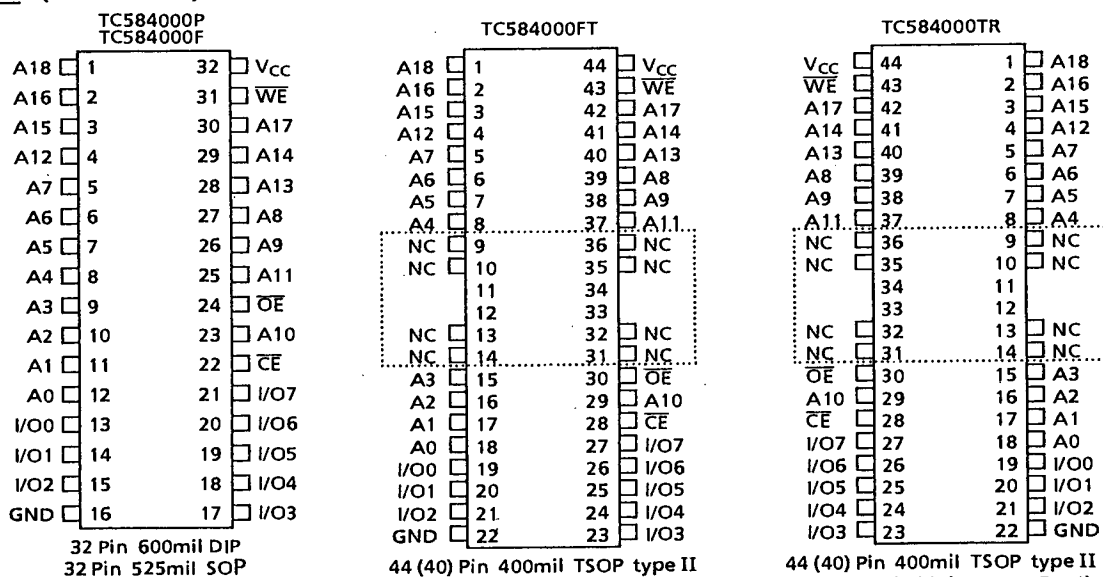
The TC584000P/F/FT/TR is a 4M bits electrically erasable and programmable nonvolatile memory equipped with a 512K×8 nonvolatile memory array and a 512K×8 data register, which can operate with a single 5V power supply. It has a 512-byte data register inside. A program operation and a read operation are performed by transferring the 512 byte page of data between the register and the memory cell array. Data in the register can be clocked out at a very high speed during page read operations. An erase operation can be performed on either a 4K-byte block or the whole chip.

The TC584000P/F/FT/TR is suitable for large capacity buffer memory applications such as semiconductor disk, voice recording and replaying, digital still camera, and so on where nonvolatility is necessary.

FEATURES

- Organization Memory Cell Array : 512K×8
Register : 512×8
- Single 5V Power Supply
- Operation
 - Page Program : 40μs×100 loops max.(TC584000P/F/FT/TR)
 - Chip Erase : 10ms (TC584000P/F/FT/TR)
 - Block Erase : 10ms (TC584000P/F/FT/TR) (4K byte / block)
 - Random Read : 15μs
 - Page Read : 120ns
- Input/Output Level : TTL Compatible
- Operation Control : Command Control
- Operation Current
 - Page Read : 30mA (tcycle=120ns)
 - Program : 5mA (tcycle=1μs)
 - Program : 60mA
 - Data Input : 70mA
 - Erase : 50mA
 - Stand by : 100μA
- W/E Endurance : 10⁵ Cycles Target

PIN CONNECTION (TOP VIEW)



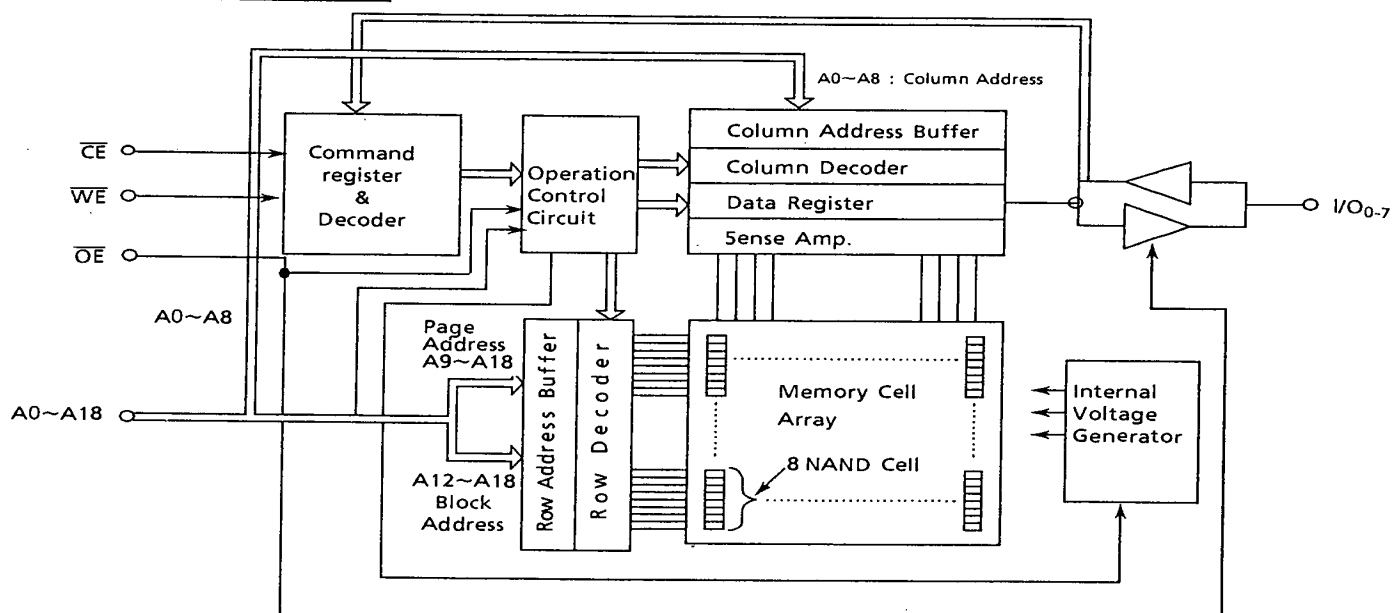
PIN ASSIGNMENT

A ₀ -18	Address Inputs
I/O ₀ -7	Data Inputs/Outputs
CE	Chip Enable Input
OE	Output Enable Input
WE	Write Enable input
V _{CC}	Power Supply (+5V)
GND	Ground
NC	No Connection

- Package
 - TC584000P : DIP32-P-600
 - TC584000F : SOP32-P-525
 - TC584000FT : TSOP44-P-400B
 - TC584000TR : TSOP44-P-400C

TC584000P/F/FT/TR

CIRCUIT BLOCK DIAGRAM



OPERATING MODE

Mode	WE	CE	OE	VCC	I/O ₀₋₇	Power
Read	Read	H	L	5V	Data Out	Active
	Output Deselect	*	*		Hi-Z	Standby
	Standby	*	H		Hi-Z	
Command Input		L	H		Command In	Active
Program/Erase	H	*	H		Hi-Z	
Program/Erase Verify	H	L	L		Data Out	

* : V_{IH} or V_{IL}

COMMAND TABLE

	1st Step			2nd Step			3rd~513th Step			No. of Step
	Mode	Address	Data	Mode	Address	Data	Mode	Address	Data	
Program	Write	*1	40H	Write	A9-18: Page Add. A0-8: 000H	Program Data	Write	A9-18: *1 A0-8: 001H~1FFH	Program Data	513 *2
Program Verify	Write	*1	C0H	Write	A9-18: Page Add. A0-8: 000H	Data Out	Read	A9-18: Page Add. A0-8: 001H~1FFH	Data Out	2~513 *3
Chip Erase	Write	*1	20H	Write	*1	20H	-	-	-	2
Block Erase	Write	*1	60H	Write	A12-18: Block Add. A0-11: *1	60H	-	-	-	2
Read	Write	*1	00H	-	-	-	-	-	-	1
Reset	Write	5555H	FFH	Write	5555H	FFH	-	-	-	2

*1 : V_{IH} or V_{IL}

*2 : Detecting Add0~8=1FFH stops 512byte serial data input operation and starts program operation internally. Therefore 512 byte serial data must be input from Add0~8=000H to Add0~8=1FFH in serial.

*3 : The No. of steps of Program Verify depends on the address where the Program Verify fails.

ABSOLUTE MAXIMUM RATINGS

Symbols	Parameter	Rating	Units
V _{CC}	Power Supply Voltage	- 0.6~7.0	V
V _{IN}	Input Voltage	- 0.6~7.0	V
V _{IO}	Output Voltage	- 0.6~V _{CC} + 0.5(≦ 7.0V)	V
P _D	Power Dissipation	1.0 ¹⁾ / 0.6 ²⁾ / 0.5 ³⁾	W
T _{SOLDER}	Soldering Temperature Time	260 · 10	°C · sec
T _{STG}	Storage Temperature	- 55~150	°C
T _{OPR}	Operating Temperature	0~70	°C

1) : DIP, 2) : SOP, 3) : TSOP

CAPACITANCE *(T_a = 25°C, f = 1MHz)

Symbols	Parameter	Conditions	Min.	Typ.	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	-	.10	15	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	-	10	15	pF

* : This parameter is periodically sampled and is not 100% tested.

D.C. RECOMMENDED OPERATING CONDITIONS (T_a = 0~70°C)

Symbols	Parameter	Min.	Typ.	Max.	Units
V _{CC}	Power Supply Voltage	4.75	5.0	5.25	V
V _{IH}	Input High Voltage	2.2	-	V _{CC} + 0.5	V
V _{IL}	Input Low Voltage	- 0.3	-	0.8	V

* -2V at pulse width ≦ 20ns

D.C. CHARACTERISTICS (T_a = 0~70°C, V_{CC} = 5V ± 5%)

Symbols	Parameter	Condition	Min.	Max.	Units
I _{IL}	Input Leakage Current	V _{IN} = 0V~V _{CC}	-	± 10	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0.4V~V _{CC}	-	± 10	μA
I _{CCO1}	Operating Current (Page Read)	$\overline{CE} = V_{IL}$ t _{cycle} = 120ns	-	30	mA
I _{CCO2}	Operating Current (Page Read)	I _{OUT} = 0mA t _{cycle} = 1μs	-	5	mA
I _{CCO3}	Operating Current (Command Input)	t _{cycle} = 100ns	-	30	mA
I _{CCO4}	Operating Current (512 byte Data Input)	t _{cycle} = 100ns	-	70	mA
I _{CCO5}	Operating Current (Program)		-	60	mA
I _{CCO6}	Operating Current (Erase)		-	50	mA
I _{CCS1}	Standby Current	$\overline{CE} = V_{IH}$	-	1	mA
I _{CCS2}	Standby Current	$\overline{CE} = V_{CC} - 0.2V$	-	100	μA
V _{OH}	Output High Voltage	I _{OH} = - 400μA	2.4	-	V
V _{OL}	Output Low Voltage	I _{OL} = 2.1mA	-	0.4	V

TC584000P/F/FT/TR

A.C. CHARACTERISTICS ($T_a=0\sim70^\circ\text{C}$, $V_{CC}=5V\pm5\%$)

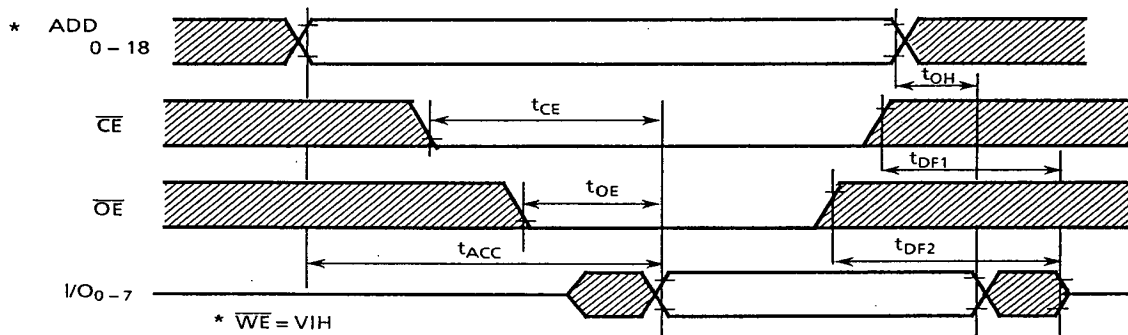
1. Read Operation

Symbol	Parameter	Min.	Max.	Unit
t_{ACC}	Address Access Time	—	15	μs
t_{PAC}	Page Mode Access Time	—	120	ns
t_{CE}	Chip Enable Access Time	—	15	μs
t_{OE}	Output Enable Access Time	—	50	ns
t_{DF1}	Chip Enable to Output in High-Z	0	50	ns
t_{DF2}	Output Enable to Output in High-Z	0	50	ns
t_{OH}	Output Data Hold Time	0	—	ns

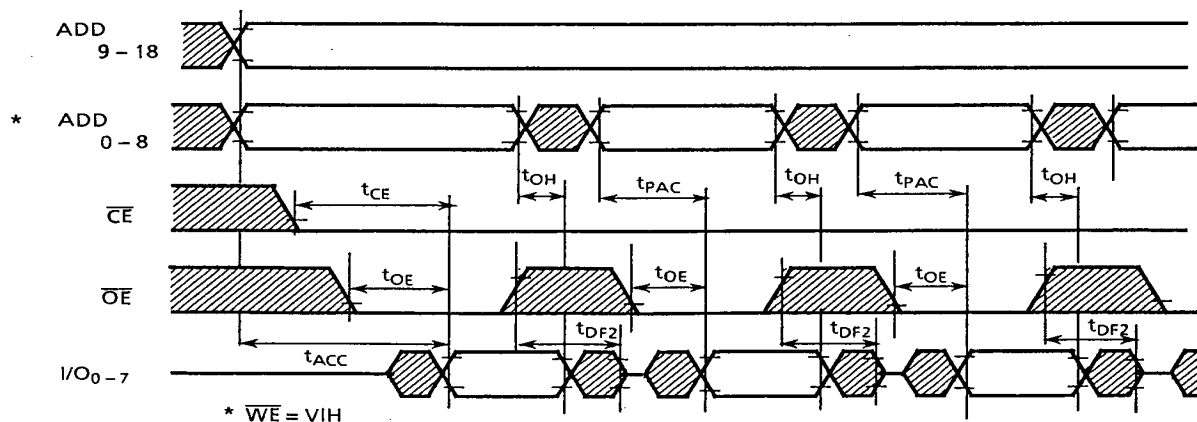
A.C. Test Conditions

- Output Load : 1TTL Gate and $C_L=100\text{pF}$
- Input Pulse Rise and Fall Time (10~90%) : 5ns Max.
- Input Pulse Level : 0.4V/2.6V
- Timing Reference Level : Input 0.8V/2.2V, Output 0.8V/2.0V

RANDOM READ TIMING WAVEFORM



PAGE READ TIMING WAVEFORM



- * Column addresses A0-8 must be fixed and can not be changed in the time period of t_{ACC} and t_{CE} in a read operation.
- * A skew among column addresses A0-8 must be less than 15ns.

2. Program / Erase Operation (Ta=0~70°C, VCC=5V±5%)

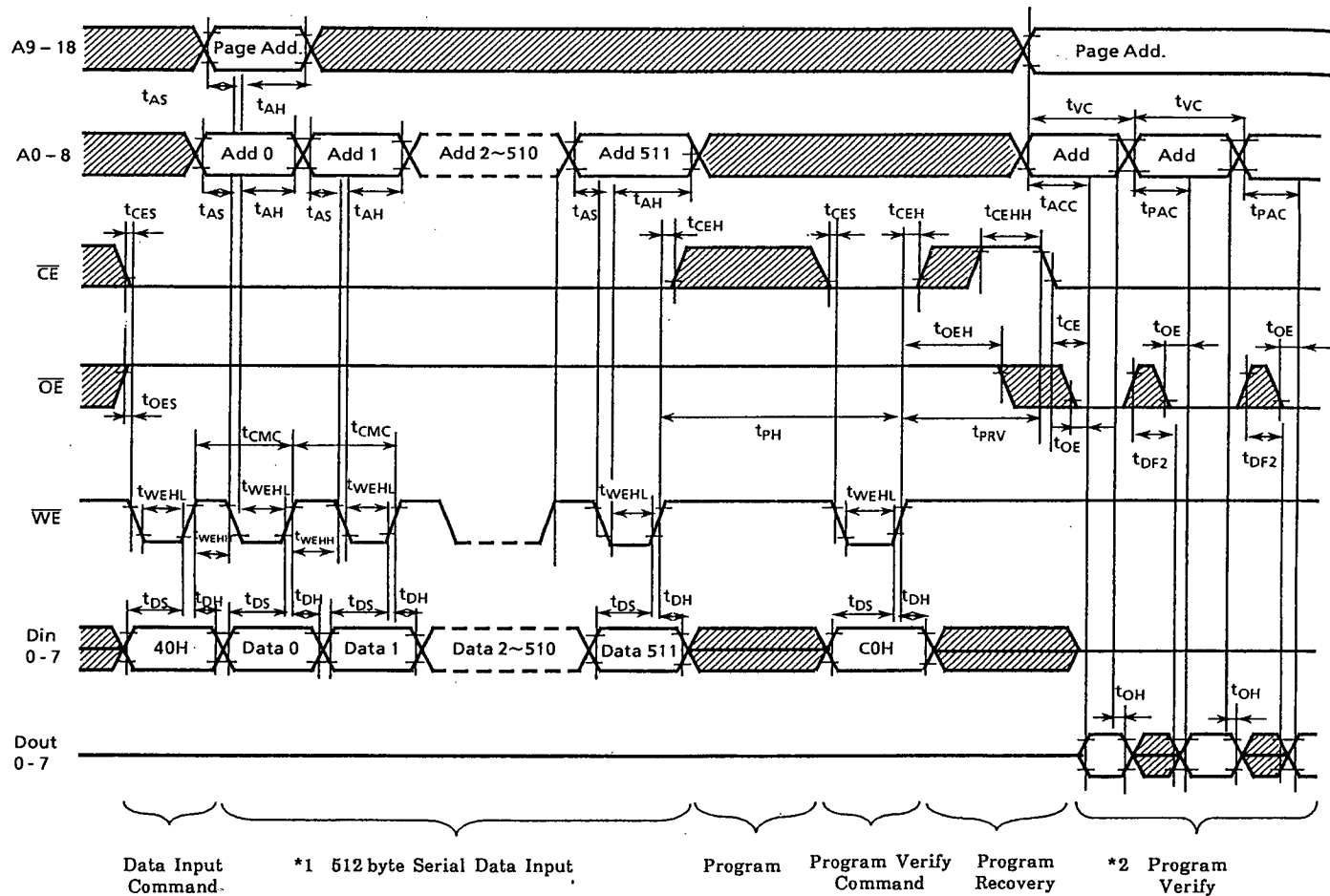
Symbol	Parameter	TC584000P/F/FT/TR			Units
		MIN.	TYP.	MAX.	
tAS	Address Setup Time	0	—	—	ns
tAH	Address Hold Time	70	—	—	
tCES	CE Setup Time (Command Cycle)	0	—	—	
tCEH	CE Hold Time (Command Cycle)	10	—	—	
toES	OE Setup Time	0	—	—	
toEH	OE Hold Time	10	—	—	
tDS	Data Setup Time	50	—	—	
tDH	Data Hold Time	0	—	—	
tWEHL	WE Low Level Hold Time	50	—	—	
tWEHH	WE High Level Hold Time	40	—	—	
tCMC	Command Cycle Time	100	—	—	
tPH	Program Hold Time	35	40	45	μs
tPRV	Program Recovery Time	5	—	—	
tEH	Erase Hold Time	9.5	10.0	10.5	ms
terv	Erase Recovery Time	2	—	—	
tACC	Address Access Time	—	—	15	μs
tPAC	Page Mode Address Access Time	—	—	120	ns
tCE	CE Access Time	—	—	15	μs
toE	OE Access Time	—	—	50	ns
tOH	Output Data Hold Time	0	—	—	
tDF1	CE to Output in High-Z	—	—	50	
tDF2	OE to Output in High-Z	—	—	50	
tVC	Verify Cycle Time	1st Cycle	15	—	μs
		2nd Cycle~	120	—	—
tCEHH	CE High Level Hold Time	100	—	—	ns

A.C. Test Condition

- Output Load : 1TTL Gate and CL=100pF
- Input Pulse Rise and Fall Time (10%~90%) : 5ns Max.
- Input Pulse Level : 0.4V / 2.6V
- Timing Reference Level : Input 0.8V / 2.2V, Output 0.8V / 2.0V

TC584000P/F/FT/TR

PROGRAM AND PROGRAM VERIFY TIMING WAVEFORM



* : 512 byte Serial Data Input 512byte data must be input from Add0 to Add511 in serial in the page.

* : Program Verify Column Addresses A0-8 must be fixed and can not be changed in the time period of t_{ACC} and t_{CE} .
A skew among column addresses A0-8 must be less than 15ns.

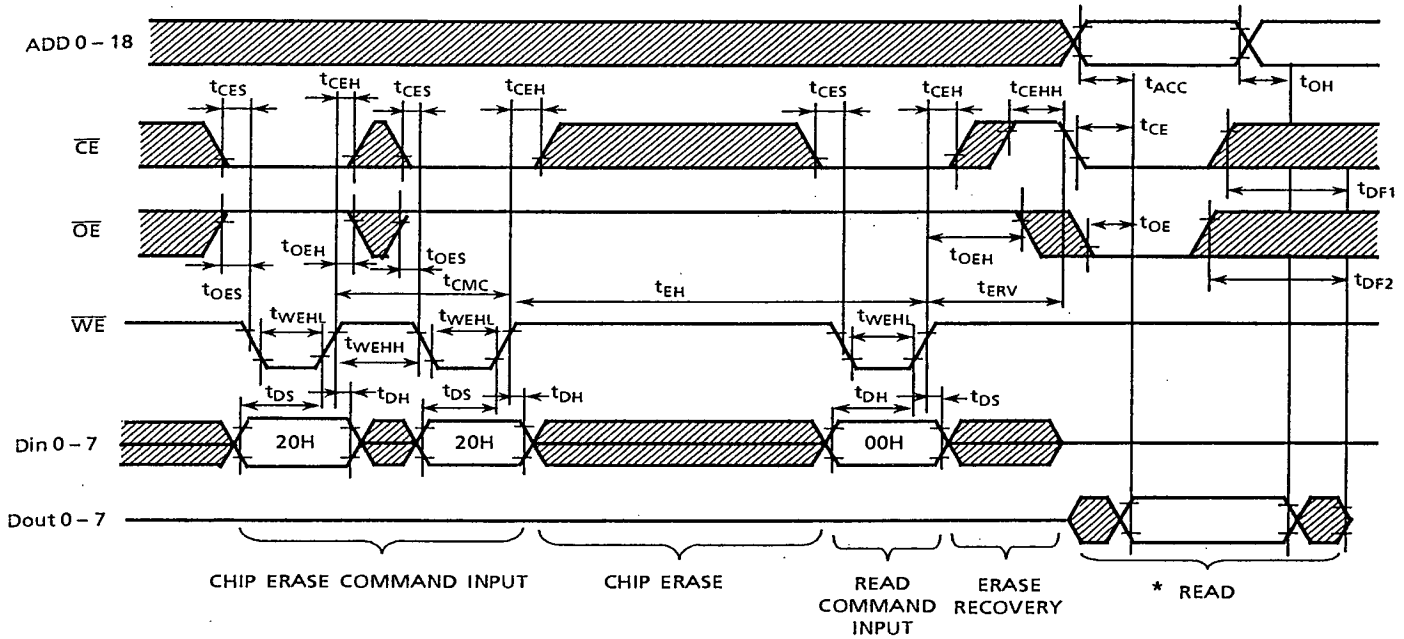


. . . . V_{IH} or V_{IL}

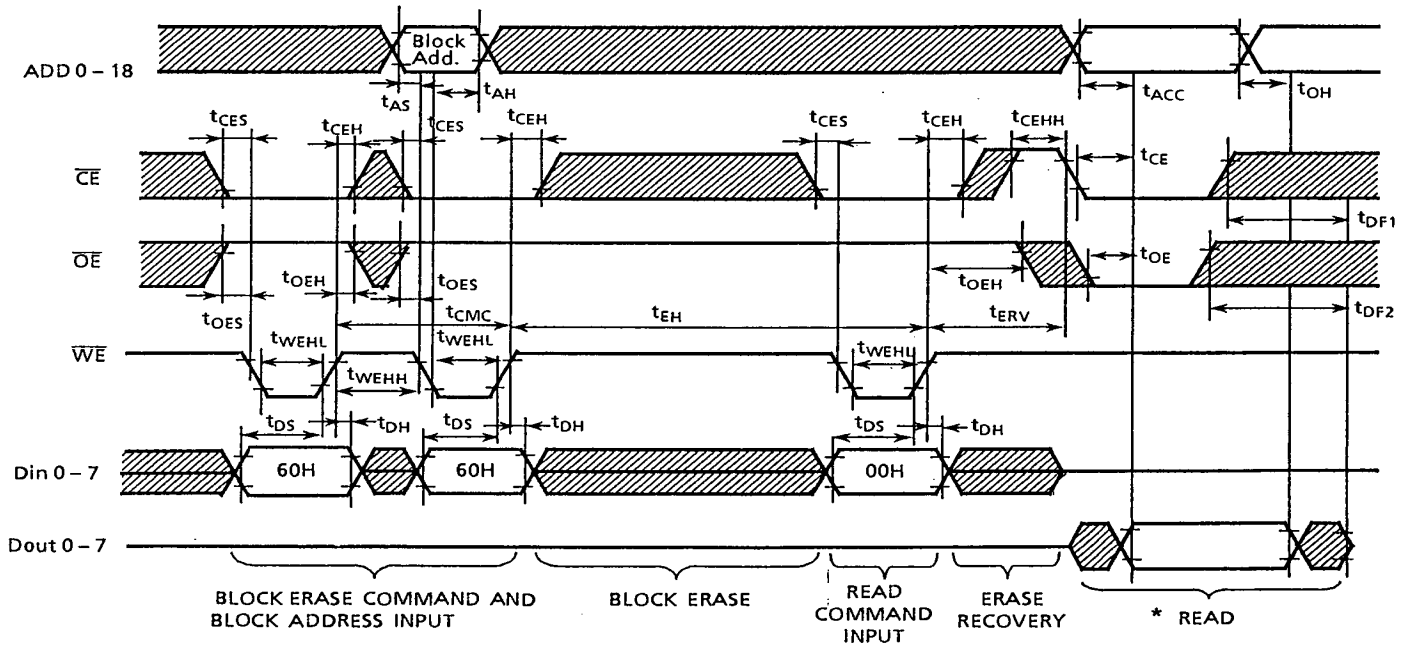


. . . . V_{IH} , V_{IL} or Hi-Z

CHIP ERASE AND ERASE VERIFY TIMING WAVEFORM

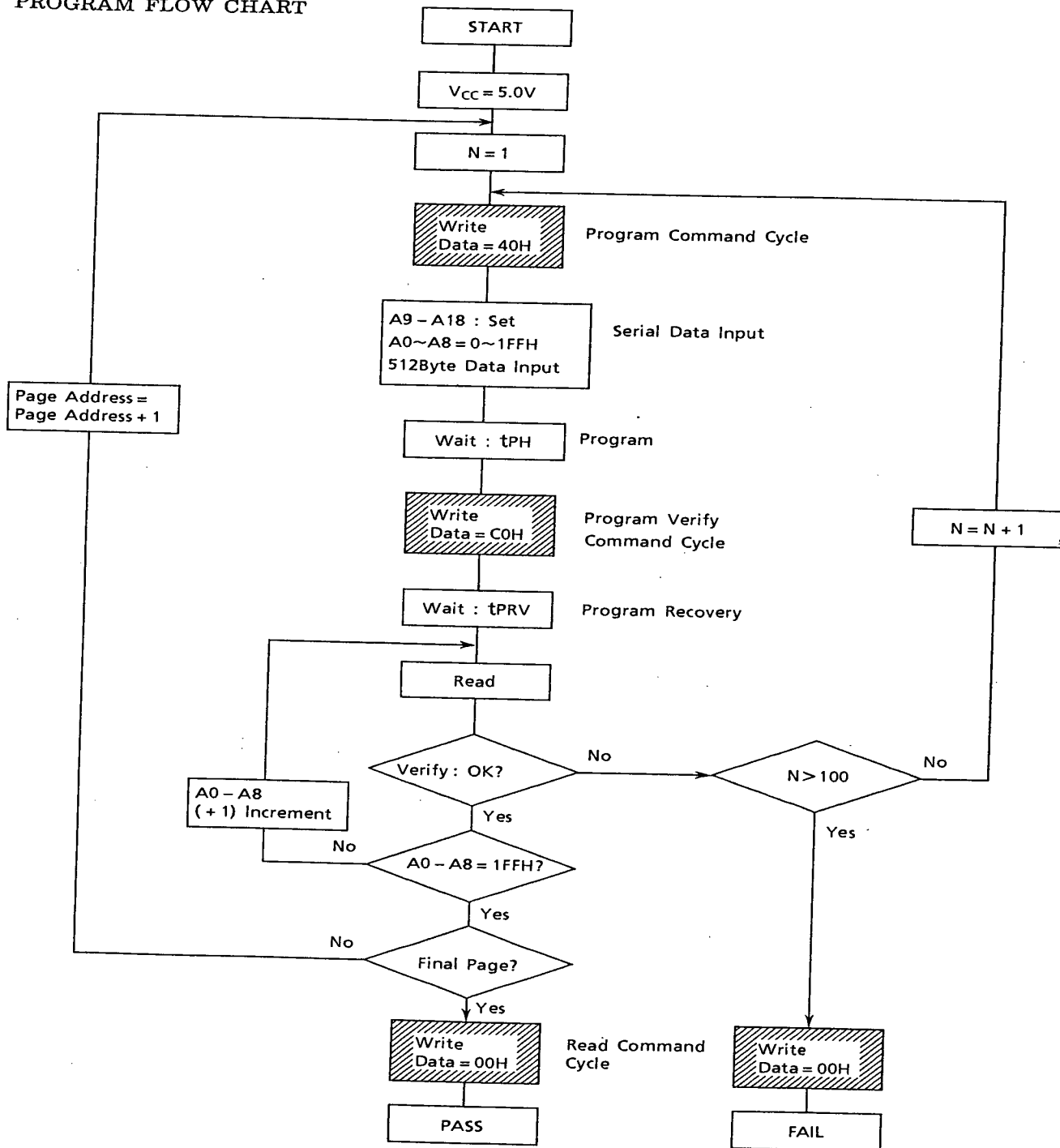


BLOCK ERASE AND ERASE VERIFY TIMING WAVEFORM

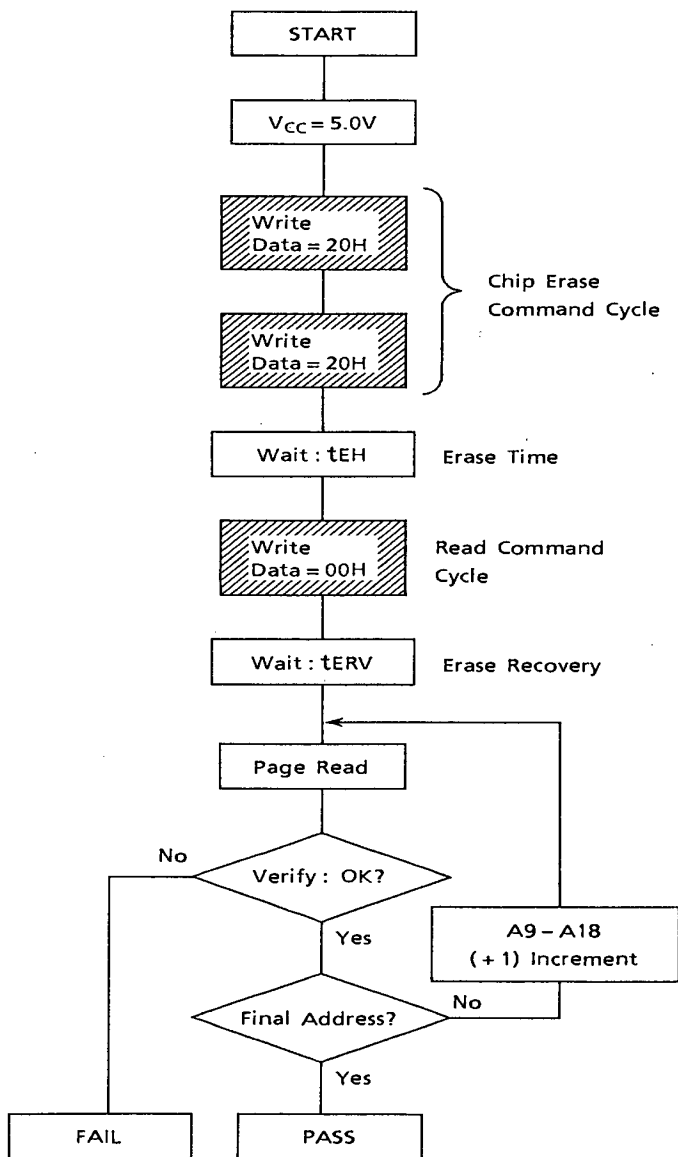


* READ : Column addresses A0-8 must be fixed and can not be changed in the time period of t_{ACC} and t_{CE} .
A skew among column addresses A0-8 must be less than 15ns.

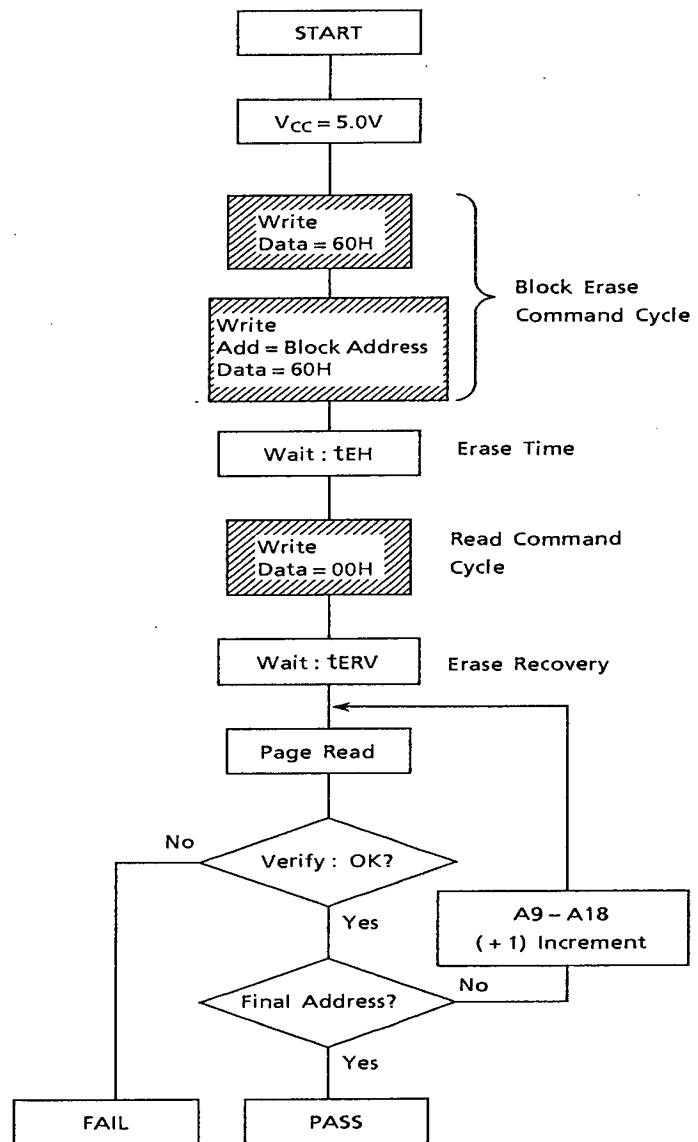
PROGRAM FLOW CHART



CHIP ERASE FLOW CHART



BLOCK ERASE FLOW CHART



DEVICE STRUCTURE AND OPERATION

The TC584000P/F/FT/TR consists of 8 sets corresponding to 8 I/Os of nonvolatile memory cell arrays organized as 512 columns by 1024 rows. A 512-bit data register is connected to each set of memory cell arrays. A NAND cell structure in which 8 cells are connected in serial is employed for memory cells. Each of the 8 cells is connected to a different page. (Fig.1)

A block is consisted of 512 NAND structures $\times$ 8 I/Os.

The program and read operations are performed on a page level. The erase operation is performed either on a block or on the whole chip.

PROGRAM OPERATION

Since the program operation of TC584000P/F/FT/TR is performed at every 512 bytes (=1page), 512 bytes data of the page must be input from the column address 000H to 1FFH (A0~A8) after the program command 40H is input. The address of the page on which the program operation is done must be input in the cycle in which the first byte data is input, however, no page address has to be valid in the following 511 cycles. The internal programming operation starts at the rising edge of $\overline{WE}$ in the last byte data input cycle and stops at the rising edge of $\overline{WE}$ in the following program verify command input cycle, thus this time period must be controlled by timing parameter t_{PH} (Program Hold Time).

A time delay of t_{PRV} after the program verify command is input, the programmed data can be read out and verified. The column address and page address must be input in these verify cycles.

The first verify cycle needs $15\mu s$, however the following verify cycles can be done by page mode with the cycle time of 120ns. If the data read out is not correct in these verify cycles, return to the beginning of the program operation and repeat the same routine from the program command input cycle until all 512 bytes of data read out in verify cycles are correct. (cf. program and program verify timing, program flow chart).

CHIP ERASE OPERATION

The chip erase operation is initiated by two cycles of chip erase command 20H input. The internal chip erase operation starts at the rising edge of $\overline{WE}$ in the second cycle and stops at the rising edge of $\overline{WE}$ in the following read command input cycle. This time period must be controlled by t_{EH} (Erase Hold Time). The erase operation completes in 10ms.

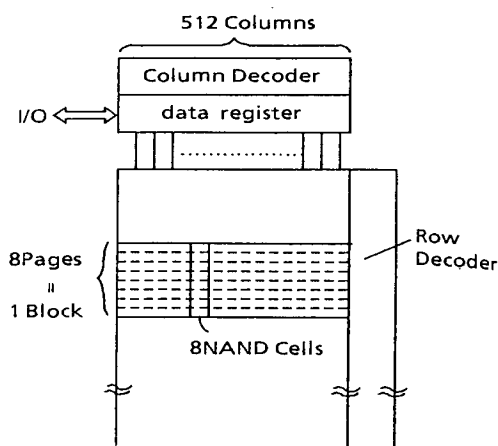
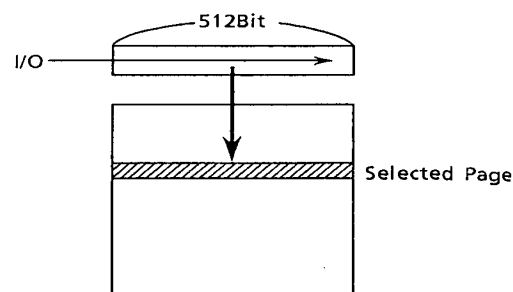


Fig.1 Structure of TC584000



BLOCK ERASE OPERATION

The TC584000P/F/FT/TR is organized as 8 pages/block $\times$ 128 blocks internally and the block erase operation can be performed on any 4K bytes (8pages) block. The block erase operation is started by two cycles of block erase command 60H input with the block address (A₁₂~A₁₈) in the second cycle.

Like the chip erase operation, the internal block operation starts at the rising edge of $\overline{WE}$ in the second cycle and stops at the rising edge of $\overline{WE}$ in the following read command input cycle. The block erase operation completes in 10ms.

READ OPERATION

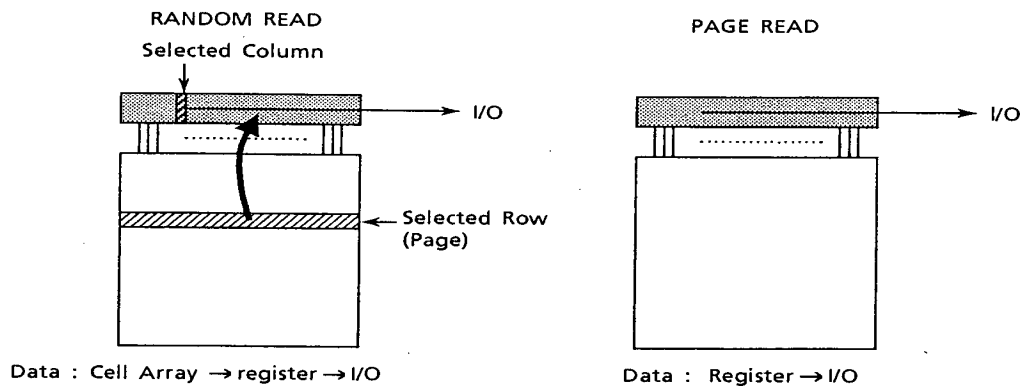
The read operation can be performed after read command 00H input. Two types of read operations are available; random read and page read.

The random read operation occurs when the page address is changed or $\overline{CE}$ is clocked. First, 512 bytes of data are transferred from the new selected page on a nonvolatile cell array to the register. Then, the data in the selected column address on the register is read out.

The page read operation occurs when no page address is changed and $\overline{CE}$ is not clocked. The 512 bytes data transfer is very slow and takes approximately 15 μ s, therefore, t_{ACC} (Random Address Access time) is 15 μ s.

However, the read out from the register is very fast and t_{PAC} (Page Address Access Time) is 120ns.

In the page read operation, the data is read out by fixing the page address and changing the column address.



RESET

The reset operation is achieved by writing the reset command FFH into the address 55555H in two cycles. This operation is used in order to break the data input cycles in the program or program and erase operation. The reset does not necessarily have to be performed in a normal operation. The device mode after reset is a read operation.

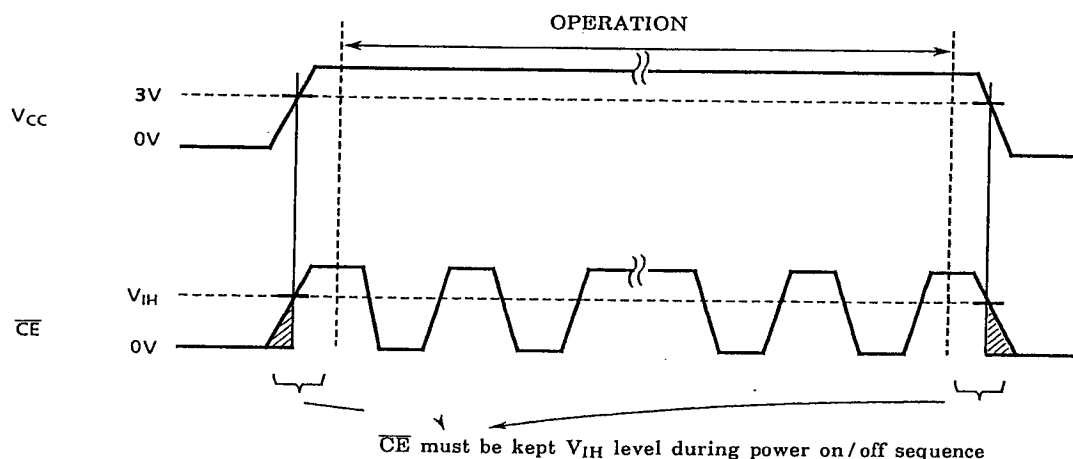
OPERATION MODE AFTER POWER ON

The operation mode after the power-on becomes a read operation automatically. However, it is recommended to input the read command 00H at the beginning of device operation after the power supply becomes stable.

TC584000P/F/FT/TR

POWER ON/OFF SEQUENCE

An accidental command input cycle during power on/off sequence may cause data corruption, therefore $\overline{CE}$ must be kept high level when V_{CC} is higher than 3V during power on/off sequence.



OPERATION PRINCIPLE

PROGRAM OPERATION

Fig. 2 shows the program operation principle of the TC584000P/F/FT/TR. The program operation is to program data '0's into cells in the erased state (data '1') by employing tunneling phenomenon. The following explains the program operation principle with an example in which data '0' and '1' are programmed into the TR1 and TR2 individually in the selected page.

The select line 1 is given 'H' level and the select line 2 is given 'L' level so that 8 cells in the NAND are connected to the bit line and isolated from GND. Then V_{pp} (approximately 20V) is given to the word line of the selected page and V_{PI} (approximately 10V) is given to the word line of the other unselected pages.

On the other hand, 0V is given to the bit line connected to the NAND that has TR1 in which data '0' is going to be programmed and V_{DPI} (approximately 10V) is given to the bit line connected to the NAND that has TR2 in which data '1' is going to be programmed.

With this condition of voltages on each road, TR1 has approximately 20V between its control gate and channel, and electrons are injected to the floating gate from the channel by tunneling phenomenon.

Once this happens, even though V_{pp} is cut off, the electrons are retained in the floating gate which is surrounded by SiO_2 until an erase operation is performed.

At TR2, 20V is given to the control gate, however 10V given to the channel make the potential difference between the control gate and channel approximately 10V which is not high enough for tunneling phenomenon. Thus, electron injection does not occur. The cells in the unselected page have approximately 10V on their control gate so no tunneling phenomenon will occur.

The floating gate of a '0' data cell is charged negative and that of a '1' data cell is charged positive, thus the '0' and '1' data are retained after the program operation has been done.

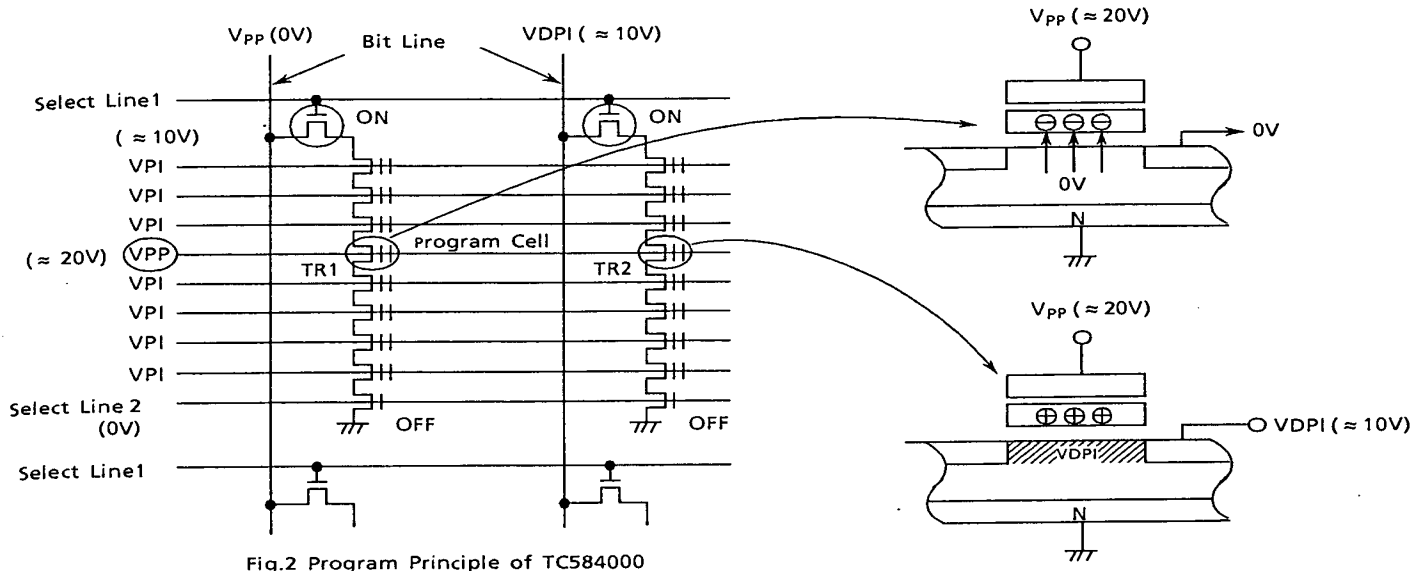


Fig.2 Program Principle of TC584000

ERASE OPERATION

The erase operation principle of the TC584000 is shown in Fig.3. The erase operation changes the cell state in a selected block or in a whole chip from '0' to '1' by pulling electrons out from the floating gate to the channel by tunneling phenomenon.

0V and VPP (approximately 20V) are given to the control gates and substrate respectively in the operation. This gives 20V potential difference between the control gates and substrate, and results in tunneling phenomenon which pulls electrons in the floating gate out to the substrate.

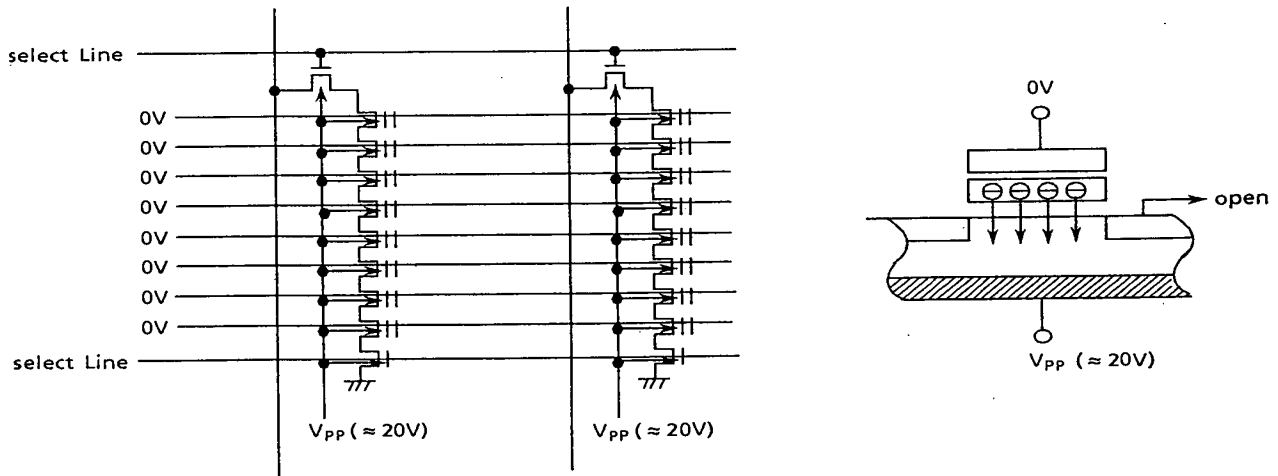


Fig.3. Erase Principle of TC584000

READ OPERATION

As explained in the program operation above, the state of the cells are '0' in which the floating gate is charged negative or '1' in which the floating gate is charged positive after the program operation. This is described by threshold voltage V_{TH} ; the characteristics parameter of MOS transistor as shown in Fig.4.

The threshold voltage of '0' data cells distribute in positive side and that of '1' data cells distribute in negative side.

The reason why they distribute in a certain area is that the memory cell transistors have some dispersion.

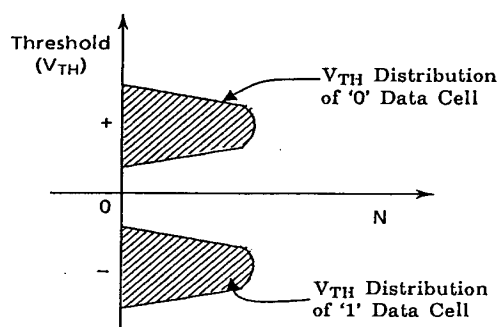


Fig.4. Threshold Voltage Distribution of '0' Data/'1' Data Cell

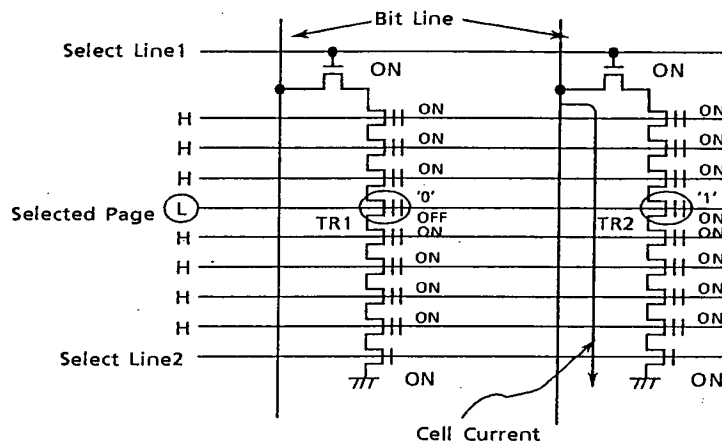


Fig.5 Read Principle of TC584000

Fig.5 shows the read operation principle.

The select line 1 and 2 of the block which has the selected page are biased 'H' level and 8 cells in the NAND are connected to the bit line and GND. The control gates of 7 unselected page are given 'H' level and that of the selected page is given 0V.

In Fig.5, TR2, since it is in '1' state, turns on and all the other unselected transistors also turn on, therefore cell current flows and the precharged bit line discharges. On the contrary, since it is in '0' state, TR1 does not turn on and cell current does not flow. The bit line levels at this point are sensed '1' and '0' respectively by the sense amplifier.

RECOMMENDATION FOR PROGRAM OPERATION

- 1) Over programming by t_{PH} (program Hold Time) being longer than the specified value may make it impossible to read data out of the cell correctly. If this happened, an erase operation will be necessary to recover from the over programmed state.
Over program means that the threshold voltage of the programmed cells shifted too much in the positive direction. Thus, the cell transistors of the unselected pages during a read operation can not turn on.
- 2) The page address within a block ($A_9 \sim A_{11}$) must be incremented in order from LSB to MSB when the device is programmed.
- 3) Comment on the program on a already programmed page : There is a restriction for the number of times of new data programming operations on a already programmed page.
- 4) In case of programming several devices in parallel, programming inhibit for a device which has already been programmed successfully should be done by command input instead of programming '1' data.

4-4 MASK ROM

SILICON STACKED GATE MOS INTEGRATED CIRCUIT

TC531000CP/CF-12,-15

1M BIT (128K WORD × 8 BIT) COMS MASK ROM

DESCRIPTION

The TC531000CP/CF is a 1, 048, 576 bits read only memory organized as 131, 072 words by 8 bits with a low bit cost, thus being suitable for use in program memory of microprocessor, especially character generator. The TC531000CP/CF using CMOS technology is most suitable for low power applications where battery operation are required. The TC531000CP/CF has one chip enable input $\overline{CE}/CE$, programmable for device selection.

FEATURES

TC531000CP/CF	- 12	- 15
Access Time (max)	120ns	150ns
Power Dissipation		
Operation Current (max)	40mA	35mA
Power Dissipation		
Standby Current (max)	20 μ A	20 μ A

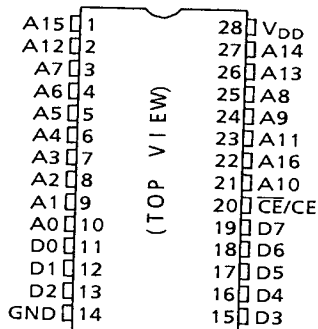
- Single 5V power supply

- All Inputs and Outputs : TTL Compatible
- Three State Outputs
- Fully Static Operation
- Programmable Chip Enable
- Package

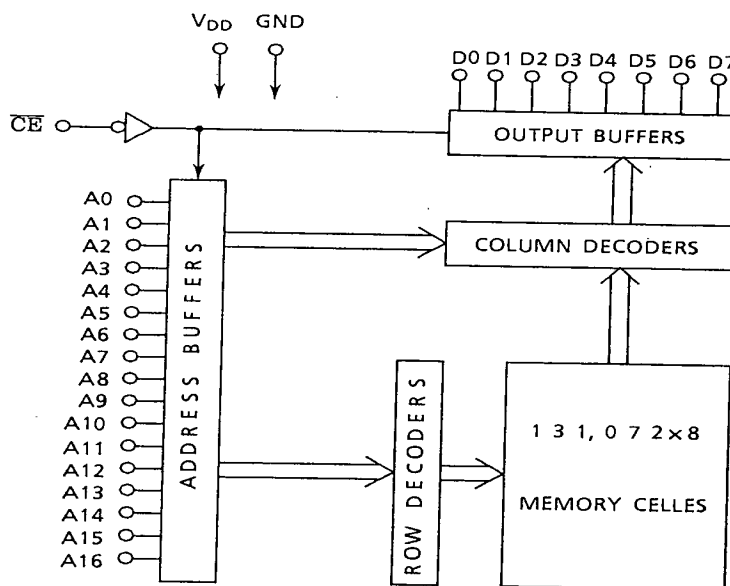
TC531000CP : DIP28-P-600

TC531000CF : SOP28-P-450

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

A0~A16	Address Inputs
D0~D7	Data Outputs
$\overline{CE}/CE$	Chip Enable Input
V _{DD}	Power Supply
GND	Ground

TC531000CP/CF-12, -15

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	- 0.5~7.0	V
V_{IN}	Input Voltage	- 0.5~ V_{DD}	
V_{OUT}	Output Voltage	0~ V_{DD}	
P_D	Power Dissipation	1.0/0.6*	W
T_{STG}	Storage Temperature	- 55~150	°C
T_{OPR}	Operating Temperature	- 40~70	
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec

Note : *Plastic SOP

D C. OPERATING CONDITIONS ($T_a = -40\sim70^\circ\text{C}$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.3$	
V_{IL}	Input Low Voltage	- 0.3	—	0.8	

D C. and OPERATING CHARACTERISTICS ($T_a = -40\sim70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
I _{IL}	Input Leakage Current	V _{IN} = 0~V _{DD}		—	± 1.0	μA
I _{LO}	Output Leakage Current	$\overline{CE}$ = V _{IH} , V _{OUT} = 0~V _{DD}		—	± 5.0	
I _{OH}	Output High Current	V _{OH} = 2.4V		− 1.0	—	mA
I _{OL}	Output Low Current	V _{OL} = 0.4V		3.2	—	
I _{DDs1}	Standby Current	CE = 0.8V ($\overline{CE}$ = 2.2V)		—	2	
I _{DDs2}	Standby Current	CE = 0.2V ($\overline{CE}$ = V _{DD} − 0.2V)		—	20	μA
I _{DDO1}	Operating Current	V _{IN} = V _{IH} / V _{IL} I _{OUT} = 0mA	t _{cycle} = 120ns	—	50	mA
			t _{cycle} = 150ns	—	45	
I _{DDO2}		V _{IN} = V _{DD} − 0.2V / 0.2V I _{OUT} = 0mA	t _{cycle} = 120ns	—	40	
			t _{cycle} = 150ns	—	35	

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	$f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$	—	10	pF
C_{OUT}	Output Capacitance	$f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$	—	10	

Note : This parameter is periodically sampled and is not 100% tested.

TC531000CP/CF-12, -15

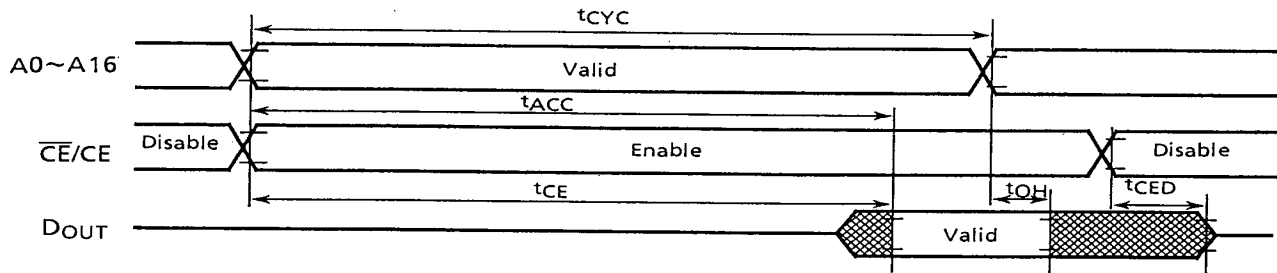
A.C. CHARACTERISTICS ($V_{DD} = 5V \pm 10\%$, $T_a = -40 \sim 70^\circ C$)

SYMBOL	PARAMETER	120ns Version		150ns Version		SYMBOL
		MIN.	MAX.	MIN.	MAX.	
t_{cycle}	Cycle Time	120	—	150	—	ns
T_{ACC}	Access Time	—	120	—	150	
T_{CE}	Chip Enable Access Time	—	120	—	150	
T_{CED}	Output Disable Time	—	50	—	50	
T_{OH}	Output Hold Time	5	—	5	—	

AC TEST CONDITIONS

- Output Load : 100pF + 1TTL
- Input Levels : 0.6V, 2.4V
- Timing Measurement Reference Levels
 - Input : 0.8V, 2.2V
 - Output : 0.8V, 2.0V
- Input Rise and Fall Time : 5ns

TIMING WAVEFORMS



OPERATION MODE

MODE	$\overline{CE}$ (CE)	A0~A15	Outputs	Power
Read	L (H)	Valid	Data Out	Operating
Standby	H (L)	*	High-Z	Standby

H : V_{IH} , L : V_{IL} , * : V_{IH} or V_{IL}

SILICON STACKED GATE MOS INTEGRATED CIRCUIT

TC531001CP/CF-12,-15

1M BIT (128K WORD × 8 BIT) CMOS MASK ROM

DESCRIPTION

The TC531001CP/CF is a 1, 048, 576 bits read only memory organized as 131, 072 words by 8 bits memory, especially character generator. The TC531001CP/CF using CMOS technology is most suitable for low power applications where battery operations are required.

The TC531001CP/CF has one chip enable input $\overline{CE}$ for device selection.

FEATURES

TC531001CP/CF	- 12	- 15
Access Time (max)	120ns	150ns
Power Dissipation Operation Current (max)	40mA	35mA
Power Dissipation Standby Current (max)	20 μ A	20 μ A

- Single 5V power supply

- All Inputs and Outputs : TTL Compatible
- Three State Outputs
- Fully Static Operation
- Package

TC531001CP : DIP32-P-600

TC531001CF : SOP32-P-525

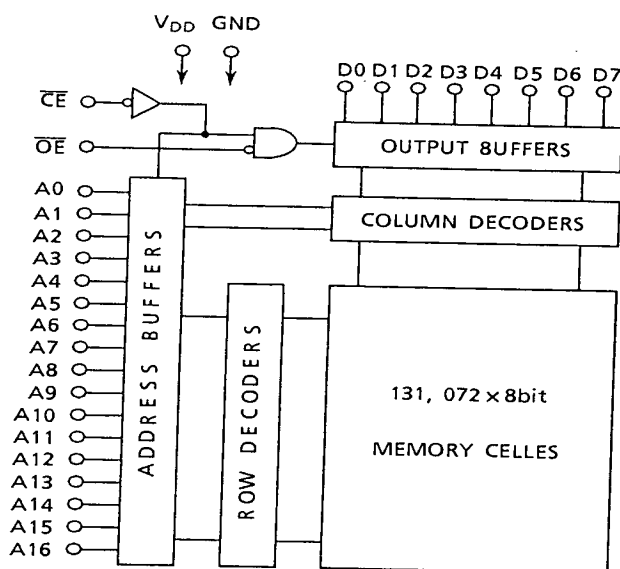
PIN CONNECTION

N.C.	1	32	V _{DD}
A16	2	31	N.C.
A15	3	30	N.C.
A12	4	29	A14
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	$\overline{OE}$
A2	10	23	A10
A1	11	22	$\overline{CE}$
A0	12	21	D7
D0	13	20	D6
D1	14	19	D5
D2	15	18	D4
GND	16	17	D3

PIN NAMES

A0~A16	Address Inputs
D0~D7	Data Outputs
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
V _{DD}	Power Supply
GND	Ground
N.C.	No connection

BLOCK DIAGRAM



TC531001CP/CF-12, -15

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	- 0.5~7.0	V
V_{IN}	Input Voltage	- 0.5~ V_{DD}	V
V_{OUT}	Output Voltage	0~ V_{DD}	V
P_D	Power Dissipation	1.0/0.6*	W
T_{STG}	Storage Temperature	- 55~150	°C
T_{OPR}	Operating Temperature	- 40~70	°C
T_{SOLDER}	Soldering Temperature Time	260 · 10	°C · sec

* : Plastic SOP

D C. OPERATING CONDITIONS ($T_a = -40 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.3$	
V_{IL}	Input Low Voltage	- 0.3	—	0.8	

D C. and OPERATING CHARACTERISTICS ($T_a = -40 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
I _{IL}	Input Leakage Current	V _{IN} = 0~V _{DD}		—	± 1.0	μA
I _{LO}	Output Leakage Current	CE = V _{IH} , V _{OUT} = 0V~V _{DD}		—	± 5.0	μA
I _{OH}	Output High Current	V _{OH} = 2.4V		- 1.0	—	mA
I _{OL}	Output Low Current	V _{OL} = 0.4V		3.2	—	mA
I _{DDs1}	Standby Current	CE = 2.2V		—	2	mA
I _{DDs2}	Standby Current	CE = V _{DD} - 0.2V		—	20	μA
I _{DDO1}	Operating Current	V _{IN} = V _{IH} / V _{IL}	t _{cycle} = 120ns	—	50	mA
		I _{OUT} = 0mA	t _{cycle} = 150ns	—	45	
I _{DDO2}		V _{IN} = V _{DD} - 0.2V / 0.2V	t _{cycle} = 120ns	—	40	
		I _{OUT} = 0mA	t _{cycle} = 150ns	—	35	

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	$f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$	—	10	pF
C_{OUT}	Output Capacitance	$f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$	—	10	

Note : This parameter is periodically sampled and is not 100% tested.

TC531001CP/CF-12, -15

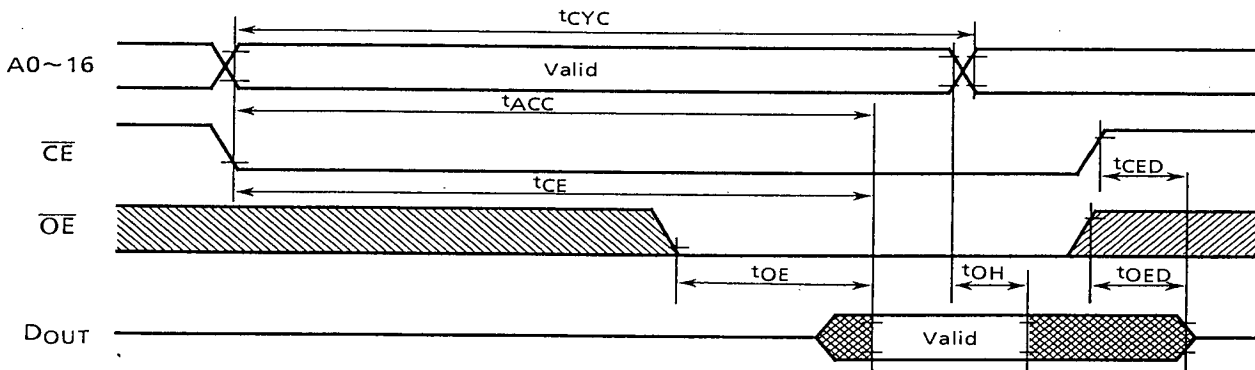
A.C. CHARACTERISTICS (Ta = -40~70°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	120ns Version		150ns Version		SYMBOL
		MIN.	MAX.	MIN.	MAX.	
t _{cycle}	Cycle Time	120	—	150	—	ns
T _{ACC}	Access Time	—	120	—	150	
T _{CE}	Chip Enable Access Time	—	120	—	150	
T _{OE}	Output Enable Access Time	—	70	—	70	
T _{CED}	Output Disable Time from $\overline{CE}$	—	50	—	50	
T _{OED}	Output Disable Time from $\overline{OE}$	—	50	—	50	
T _{OH}	Output Hold Time	5	—	5	—	

AC TEST CONDITIONS

- Output Load : 100pF + 1TTL
- Input Levels : 0.6V, 2.4V
- Timing Measurement Reference Levels Input : 0.8V, 2.2V
Output : 0.8V, 2.0V
- Input Rise and Fall Time : 5ns

TIMING WAVEFORMS



OPERATION MODE

MODE	$\overline{CE}$	$\overline{OE}$	A0~A16	Outputs	Power
Read	L	L	Valid	Data Out	Operating
Standby	H	*	*	High-Z	Standby
Output Deselect	L	H	*	High-Z	Operating

H : V_{IH}, L : V_{IL}, *: V_{IH} or V_{IL}

TC531024P/F-12, -15

1M BIT (65,536 WORD × 16 BIT) CMOS MASK ROM

DESCRIPTION

The TC531024P/F is a 1,048,576 bits read only memory organized as 65,536 words by 16 bits.

The TC531024P/F is fabricated using Toshiba's advanced CMOS technology which provides the high speed and low power features with access time of 120ns/150ns, an operation current of 40mA at 8.3MHz and a standby current of 20μA.

The TC531024P/F is packaged in a standard 600mil 40pin DIP, or 525mil 40pin SOP.

FEATURES

TC531024P/F	- 12	- 15
Power Supply	5V ± 5%	5V ± 10%
Access Time (Max.)	120ns	150ns
Power Dissipation : Operating Current (Max.)	40mA	35mA
Power Dissipation : Standby Current (Max.)	20μA	20μA

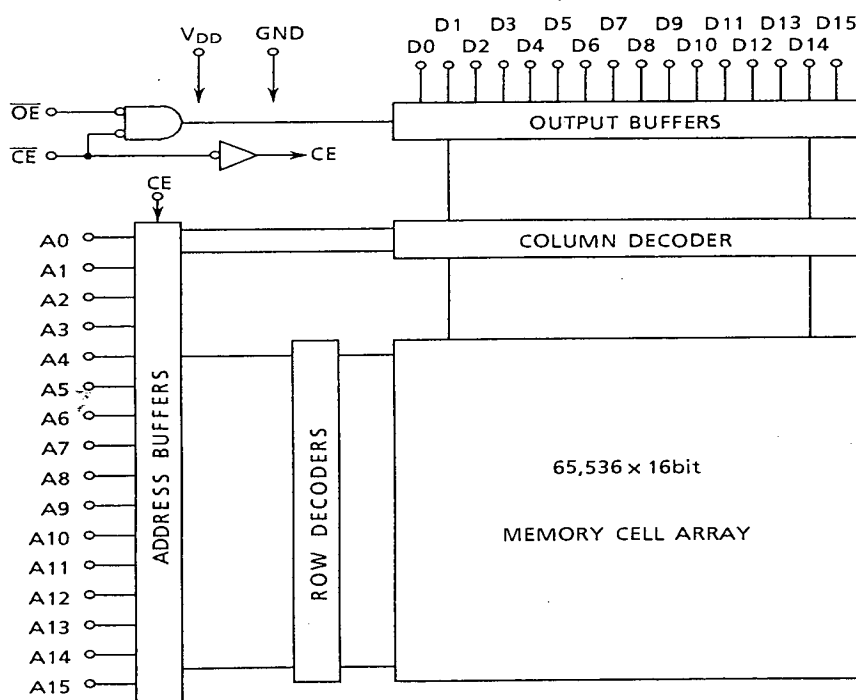
- Single 5V Power Supply
- Fully Static Operation
- All Input and Output : TTL Compatible
- Three State Output
- TC531024P : DIP40 - P - 600
- TC531024F : SOP40 - P - 525

PIN CONNECTION

(TOP VIEW)

N.C.	1	40	V _{DD}
CE	2	39	N.C.
D15	3	38	N.C.
D14	4	37	A15
D13	5	36	A14
D12	6	35	A13
D11	7	34	A12
D10	8	33	A11
D9	9	32	A10
D8	10	31	A9
GND	11	30	GND
D7	12	29	A8
D6	13	28	A7
D5	14	27	A6
D4	15	26	A5
D3	16	25	A4
D2	17	24	A3
D1	18	23	A2
D0	19	22	A1
OE	20	21	A0

BLOCK DIAGRAM



PIN NAMES

A0~A15	Address inputs
D0~D15	Data Outputs
OE	Output Enable Input
CE	Chip Enable Input
V _{DD}	Power Supply
GND	Ground
N.C.	No Connection

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	- 0.5~7.0	V
V_{IN}	Input Voltage	- 0.5~ V_{DD}	V
V_{OUT}	Output Voltage	0~ V_{DD}	V
P_D	Power Dissipation	1.0/0.6*	W
T_{STG}	Storage Temperature	- 55~150	°C
T_{OPR}	Operating Temperature	0~70	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec

Note : * Plastic SOP.

D.C. OPERATING CONDITIONS ($T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.5	V
V_{IH}	Input High Voltage	2.2	$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage	- 0.3	0.8	V

D.C. OPERATING CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
I _{IL}	Input Leakage Current	0V ≤ V _{IN} ≤ V _{DD}		–	± 1.0	μA
I _{LO}	Output Leakage Current	0V ≤ V _{OUT} ≤ V _{DD}		–	± 5.0	
I _{OH}	Output High Current	V _{OH} = 2.4V		– 1.0	–	mA
I _{OL}	Output Low Current	V _{OL} = 0.4V		3.2	–	
I _{DD} S1	Standby Current	CE = 2.2V		–	2.0	
I _{DD} S2		CE = V _{DD} – 0.2V		–	20	μA
I _{DD} O1	Operating Current	CE = V _{IL} , V _{IN} = V _{IH} / V _{IL} I _{OUT} = 0mA	t _{cycle} = 120ns	–	50	mA
			t _{cycle} = 150ns	–	45	
I _{DD} O2		CE = 0.2V , V _{IN} = V _{DD} – 0.2V / 0.2V I _{OUT} = 0mA	t _{cycle} = 120ns	–	40	
			t _{cycle} = 150ns	–	35	

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	$f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$	-	10	pF
C_{OUT}	Output Capacitance	$f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$	-	10	pF

Note : This Parameter is periodically sampled and is not 100% tested.

TC531024P/F-12, -15

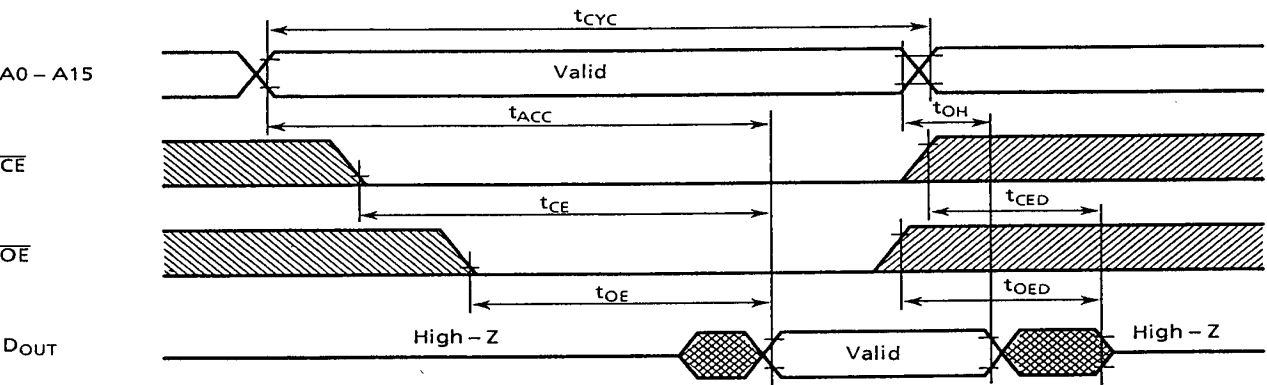
A.C. CHARACTERISTICS (Ta = 0°C~70°C)

SYMBOL	PARAMETER	VDD = 5V ± 5%		VDD = 5V ± 10%		UNIT
		MIN.	MAX.	MIN.	MAX.	
tACC	Access Time	—	120	—	150	ns
tCE	Chip Enable Access Time	—	120	—	150	ns
tOE	Output Enable Access Time	—	70	—	70	ns
tCED	Output Disable Time from $\overline{CE}$	0	60	0	60	ns
tOED	Output Disable Time from $\overline{OE}$	0	60	0	60	ns
tOH	Output Hold Time	5	—	5	—	ns
tCYC	Cycle Time	120	—	150	—	ns

A.C. TEST CONDITIONS

Output Load	: 100pF + 1TTL
Input Levels	: 0.6V / 2.4V
Timing Measurement Reference Levels	Input : 0.8V / 2.2V
	Output : 0.8V / 2.0V
Input Rise and Fall Time (10%~90%)	: 5ns

TIMING WAVEFORMS



OPERATION MODE

MODE	$\overline{CE}$	$\overline{OE}$	A0~A15	Outputs	Power
Read	L	L	Valid	Data Out	Operating
Standby	H	*	*	High-Z	Standby
Output Deselect	L	H	*	High-Z	Operating

H : VIH L : VIL * : VIH or VIL

SILICON STACKED GATE MOS INTEGRATED CIRCUIT

TC532000AP/AF

2M BIT (256K WORD × 8 BIT) CMOS MASK ROM

DESCRIPTION

The TC532000AP/AF is a 2,097,152 bits read only memory organized as 262,144 words by 8bits.

The TC532000AP/AF is fabricated using Toshiba's advanced CMOS technology which provides the high speed and low power features with access time of 150ns, an operation current of 40mA at 6.7MHz and a standby current of 20μA.

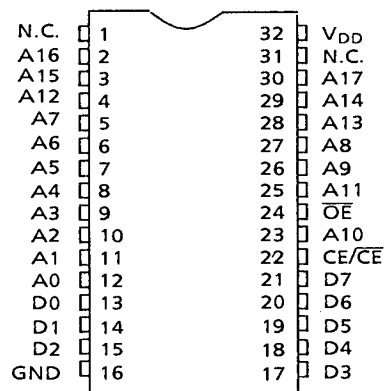
The TC532000AP/AF has one programmable chip enable input $\overline{CE}/CE$ for device selection.

The TC532000AP/AF is packaged in a standard 600mil 32pin DIP or 525mil 32pin SOP.

FEATURES

- Single 5V Power Supply
- Access Time : 150ns (Max.) $V_{DD}=5V \pm 10\%$
- Power Dissipation
 - Operating Current : 40mA (Max.)
 - Standby Current : 20μA (Max.)
- All Inputs and Outputs : TTL Compatible
- Three State Outputs
- Fully Static Operation
- Programmable Chip Enable
- TC532000AP : DIP32-P-600
- TC532000AF : SOP32-P-525

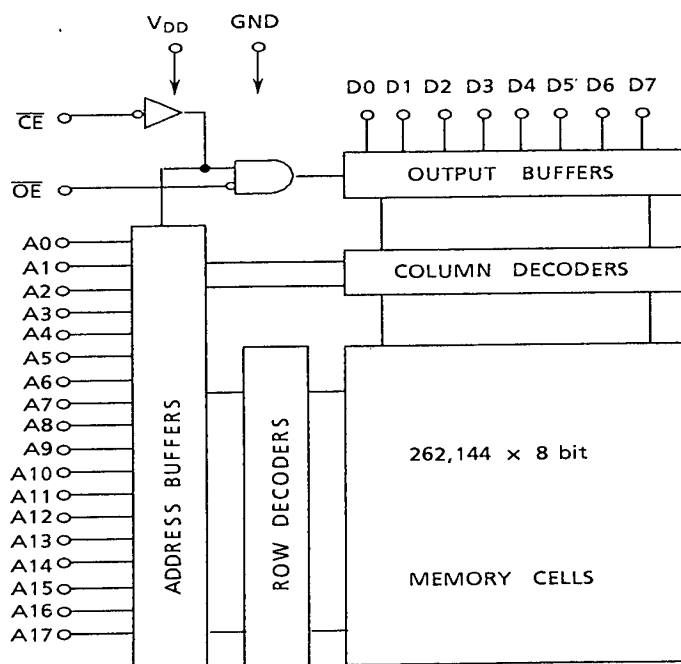
PIN CONNECTION



PIN NAMES

A0~A17	Address inputs
D0~D7	Data Outputs
$\overline{OE}$	Output Enable Input
$CE/\overline{CE}$	Chip Enable Input
V_{DD}	Power Supply
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



TC532000AP/AF

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	- 0.5~7.0	V
V_{IN}	Input Voltage	- 0.5~ V_{DD}	V
V_{OUT}	Output Voltage	0~ V_{DD}	V
P_D	Power Dissipation	1.0/0.6*	W
T_{STG}	Storage Temperature	- 55~150	°C
T_{OPR}	Operating Temperature	0~70	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec

Note : * Plastic SOP

D.C. OPERATING CONDITIONS ($T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.5	V
V_{IH}	Input High Voltage	2.2	$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage	- 0.3	0.8	V

D.C. and OPERATING CHARACTERISTICS ($V_{DD} = 5V \pm 10\%$, $T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	-	± 1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$, $V_{OUT} = 0 \sim V_{DD}$	-	± 5.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$	- 1.0	-	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$	2.0	-	mA
I_{DD51}	Standby Current	$\overline{CE} = V_{IH}$	-	2	mA
I_{DD52}		$\overline{CE} = V_{DD}$ and $V_{IN} = 0V (V_{DD})$	-	20	μA
I_{DDO1}	Operating Current	$V_{IN} = V_{IH} / V_{IL}$, $t_{cycle} = 150\text{ns}$	-	50	mA
I_{DDO2}		$V_{IN} = V_{DD} / 0V$, $t_{cycle} = 150\text{ns}$	-	40	mA

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	$f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$	-	10	pF
C_{OUT}	Output Capacitance	$f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$	-	10	pF

Note : This Parameter is periodically sampled and is not 100% tested.

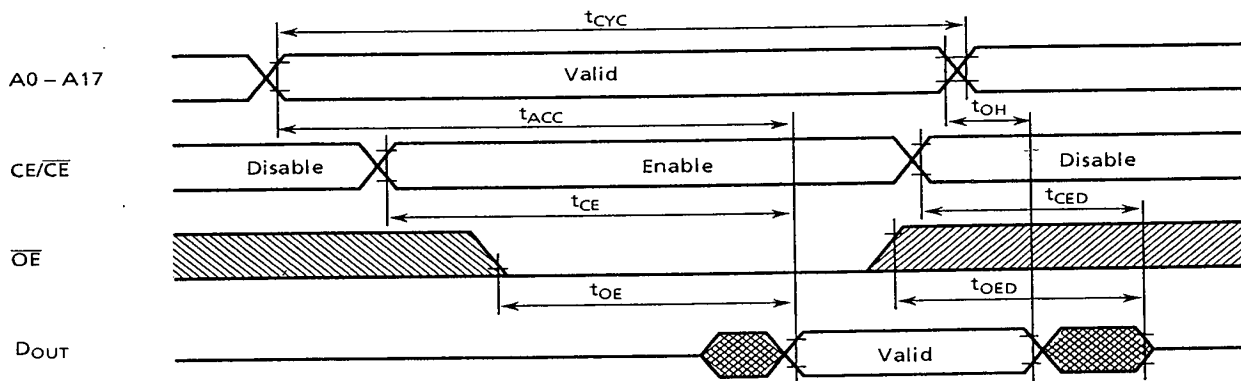
A.C. CHARACTERISTICS ($V_{DD} = 5V \pm 10\%$, $T_a = 0 \sim 70^\circ C$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{ACC}	Access Time	—	150	ns
t_{CE}	Chip Enable Access Time	—	150	ns
t_{OE}	Output Enable Access Time	—	70	ns
t_{CED}	Output Disable Time from $\overline{CE}$	0	60	ns
t_{OED}	Output Disable Time from $\overline{OE}$	0	60	ns
t_{OH}	Output Hold Time	5	—	ns
t_{CYC}	Cycle Time	150	—	ns

A.C. TEST CONDITIONS

Output Load	: 100pF + 1TTL
Input Levels	: 0.6V, 2.4V
Timing Measurement Reference Levels	Input : 0.8V, 2.2V
	Output : 0.8V, 2.0V
Input Rise and Fall Time	: 5ns

TIMING WAVEFORMS



OPERATION MODE

MODE	$\overline{CE}$ (CE)	$\overline{OE}$	A0~A17	Outputs	Power
Read	L (H)	L	Valid	Data Out	Operating
Standby	H (L)	*	*	High-Z	Standby
Output Deselect	L (H)	H	*	High-Z	Operating

H : VIH L : VIL * : VIH or VIL

TC534000AP/AF

4M BIT (512K WORD × 8 BIT) CMOS MASK ROM

DESCRIPTION

The TC534000AP/AF is a 4,194,304 bits read only memory organized as 524,288 words by 8 bits.

The TC534000AP/AF is fabricated using Toshiba's advanced CMOS technology which provides the high speed and low power features with access time of 150ns, an operation current of 40mA at 6.7MHz and a standby current of 20 μ A.

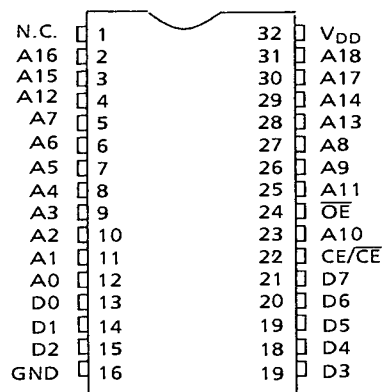
The TC534000AP/AF has one programmable chip enable input $\overline{CE}/CE$ for device selection.

The TC534000AP/AF is packaged in a standard 600mil 32pin DIP or 525mil 32pin SOP.

FEATURES

- Single 5V Power Supply
- Access Time : 150ns (Max.) $V_{DD}=5V \pm 10\%$
- Power Dissipation
 - Operating Current : 40mA (Max.)
 - Standby Current : 20 μ A (Max.)
- All Inputs and Outputs : TTL Compatible
- Three State Outputs
- Fully Static Operation
- Programmable Chip Enable
- TC534000AP : DIP32-P-600
- TC534000AF : SOP32-P-525

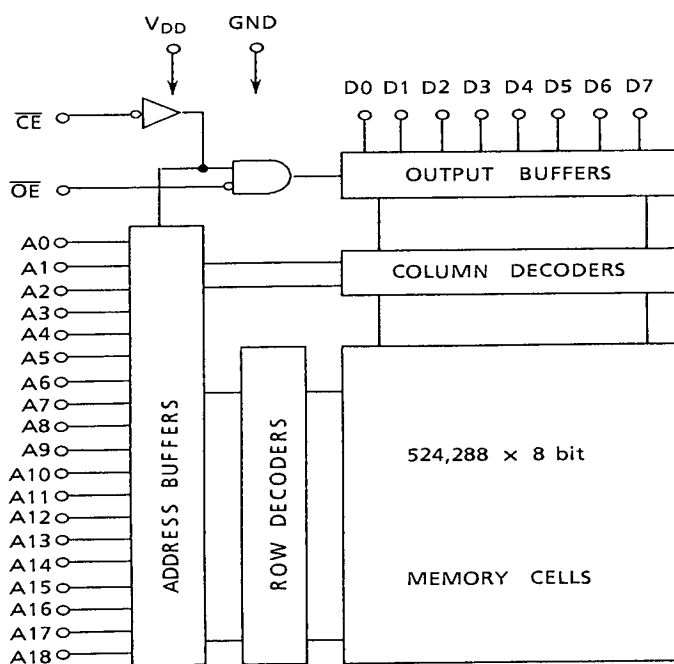
PIN CONNECTION



PIN NAMES

A0~A18	Address inputs
D0~D7	Data Outputs
$\overline{OE}$	Output Enable Input
CE/ $\overline{CE}$	Chip Enable Input
V _{DD}	Power Supply
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	- 0.5~7.0	V
V_{IN}	Input Voltage	- 0.5~ V_{DD}	V
V_{OUT}	Output Voltage	0~ V_{DD}	V
P_D	Power Dissipation	1.0 / 0.6*	W
T_{STG}	Storage Temperature	- 55~150	°C
T_{OPR}	Operating Temperature	0~70	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec

Note : * Plastic SOP

D.C. OPERATING CONDITIONS ($T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.5	V
V_{IH}	Input High Voltage	2.2	$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage	- 0.3	0.8	V

D.C. and OPERATING CHARACTERISTICS ($V_{DD} = 5V \pm 10\%$, $T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	-	± 1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$, $V_{OUT} = 0 \sim V_{DD}$	-	± 5.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$	- 1.0	-	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$	2.0	-	mA
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$	-	2	mA
I_{DDS2}		$\overline{CE} = V_{DD}$ and $V_{IN} = 0V (V_{DD})$	-	20	μA
I_{DDO1}	Operating Current	$V_{IN} = V_{IH} / V_{IL}$, $t_{cycle} = 150\text{ns}$	-	50	mA
I_{DDO2}		$V_{IN} = V_{DD} / 0V$, $t_{cycle} = 150\text{ns}$	-	40	mA

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	$f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$	-	10	pF
C_{OUT}	Output Capacitance	$f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$	-	10	pF

Note : This Parameter is periodically sampled and is not 100% tested.

TC534000AP/AF

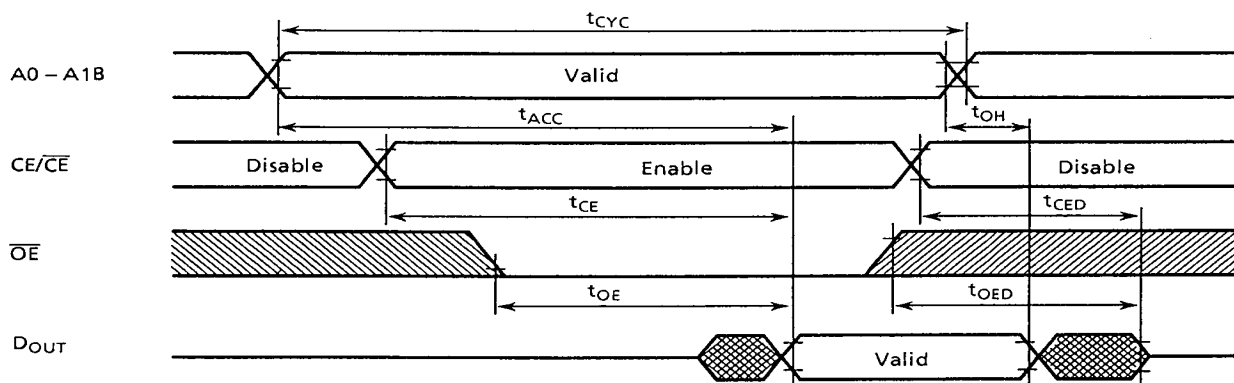
A.C. CHARACTERISTICS ($V_{DD} = 5V \pm 10\%$, $T_a = 0 \sim 70^\circ C$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{ACC}	Access Time	—	150	ns
t_{CE}	Chip Enable Access Time	—	150	ns
t_{OE}	Output Enable Access Time	—	70	ns
t_{CED}	Output Disable Time from $\overline{CE}$	0	60	ns
t_{OED}	Output Disable Time from $\overline{OE}$	0	60	ns
t_{OH}	Output Hold Time	5	—	ns
t_{CYC}	Cycle Time	150	—	ns

A.C. TEST CONDITIONS

Output Load	: 100pF + 1TTL
Input Levels	: 0.6V, 2.4V
Timing Measurement Reference Levels	Input : 0.8V, 2.2V Output : 0.8V, 2.0V
Input Rise and Fall Time	: 5ns

TIMING WAVEFORMS



OPERATION MODE

MODE	$\overline{CE}$ (CE)	$\overline{OE}$	A0~A18	Outputs	Power
Read	L (H)	L	Valid	Data Out	Operating
Standby	H (L)	*	*	High-Z	Standby
Output Deselect	L (H)	H	*	High-Z	Operating

H : VIH L : VIL * : VIH or VIL

SILICON STACKED GATE MOS INTEGRATED CIRCUIT

TC534000AFT

TENTATIVE

4M BIT (512K WORD × 8 BIT) CMOS MASK ROM

DESCRIPTION

The TC534000AFT is a 4,194,304 bits read only memory organized as 524,288 words by 8 bits.

The TC534000AFT is fabricated using Toshiba's advanced CMOS technology which provides the high speed and low power features with access time of 150ns, an operation current of 40mA at 6.7MHz and a standby current of 20μA.

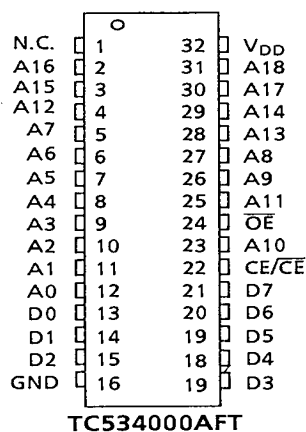
The TC534000AFT has one programmable chip enable input $\overline{CE}/CE$ for device selection.

The TC534000AFT is packaged in a 400mil 32 pin TSOP Type II.

FEATURES

- Single 5V Power Supply
- Access Time : 150ns (Max.) $V_{DD}=5V \pm 10\%$
- Power Dissipation
 - Operating Current : 40mA (Max.)
 - Standby Current : 20μA (Max.)
- All Inputs and Outputs : TTL Compatible
- Three State Outputs
- Fully Static Operation
- Programmable Chip Enable
- TC534000AFT : TSOP32-P-400

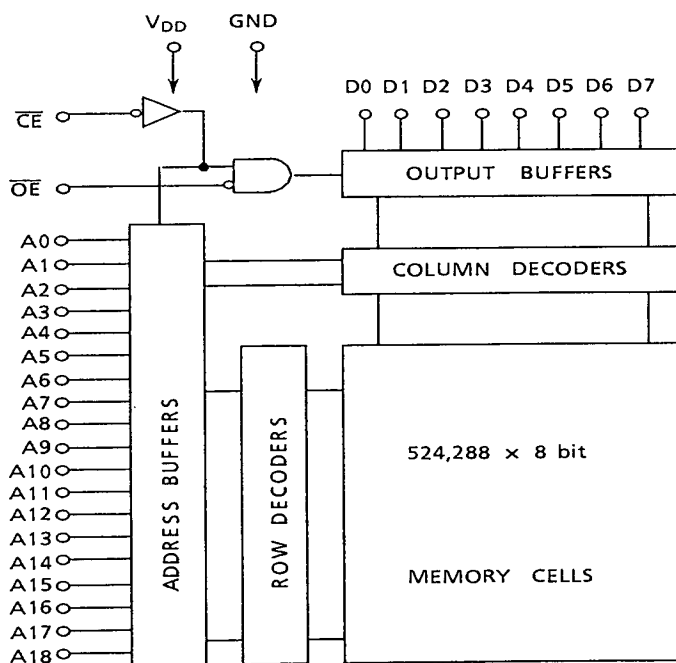
PIN CONNECTION



PIN NAMES

A0~A18	Address inputs
D0~D7	Data Outputs
$\overline{OE}$	Output Enable Input
$\overline{CE}/CE$	Chip Enable Input
V_{DD}	Power Supply
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



TC534000AFT

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	$-0.5 \sim 7.0$	V
V_{IN}	Input Voltage	$-0.5 \sim V_{DD}$	V
V_{OUT}	Output Voltage	$0 \sim V_{DD}$	V
P_D	Power Dissipation	0.6	W
T_{STG}	Storage Temperature	$-55 \sim 150$	$^{\circ}\text{C}$
T_{OPR}	Operating Temperature	$0 \sim 70$	$^{\circ}\text{C}$
T_{SOLDER}	Soldering Temperature · Time	$260 \cdot 10$	$^{\circ}\text{C} \cdot \text{sec}$

D.C. OPERATING CONDITIONS ($T_a = 0 \sim 70^{\circ}\text{C}$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.5	V
V_{IH}	Input High Voltage	2.2	$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage	-0.3	0.8	V

D.C. and OPERATING CHARACTERISTICS ($V_{DD} = 5\text{V} \pm 10\%$, $T_a = 0 \sim 70^{\circ}\text{C}$)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	-	± 1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$, $V_{OUT} = 0 \sim V_{DD}$	-	± 5.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4\text{V}$	-1.0	-	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4\text{V}$	2.0	-	mA
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$	-	2	mA
I_{DDS2}		$\overline{CE} = V_{DD}$ and $V_{IN} = 0\text{V} (V_{DD})$	-	20	μA
I_{DDO1}	Operating Current	$V_{IN} = V_{IH} / V_{IL}$, $t_{\text{cycle}} = 150\text{ns}$	-	50	mA
I_{DDO2}		$V_{IN} = V_{DD} / 0\text{V}$, $t_{\text{cycle}} = 150\text{ns}$	-	40	mA

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	$f = 1\text{MHz}$, $T_a = 25^{\circ}\text{C}$	-	10	pF
C_{OUT}	Output Capacitance	$f = 1\text{MHz}$, $T_a = 25^{\circ}\text{C}$	-	10	pF

Note : This Parameter is periodically sampled and is not 100% tested.

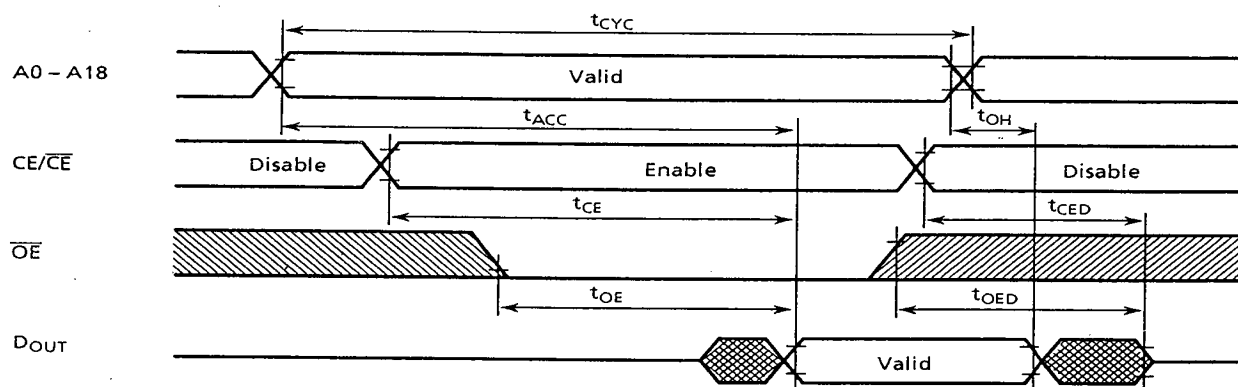
A.C. CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{ACC}	Access Time	—	150	ns
t_{CE}	Chip Enable Access Time	—	150	ns
t_{OE}	Output Enable Access Time	—	70	ns
t_{CED}	Output Disable Time from $\overline{CE}$	0	60	ns
t_{OED}	Output Disable Time from $\overline{OE}$	0	60	ns
t_{OH}	Output Hold Time	5	—	ns
t_{CYC}	Cycle Time	150	—	ns

A.C. TEST CONDITIONS

Output Load : 100pF + 1TTL
Input Levels : 0.6V , 2.4V
Timing Measurement Reference Levels Input : 0.8V , 2.2V
Output : 0.8V , 2.0V
Input Rise and Fall Time : 5ns

TIMING WAVEFORMS



OPERATION MODE

MODE	$\overline{CE}$ (CE)	$\overline{OE}$	A0~A18	Outputs	Power
Read	L (H)	L	Valid	Data Out	Operating
Standby	H (L)	*	*	High-Z	Standby
Output Deselect	L (H)	H	*	High-Z	Operating

H : VIH L : VIL * : VIH or VIL

TC534200P/F

4M BIT (256K WORD × 16 BIT / 512K WORD × 8BIT) CMOS MASK ROM

DESCRIPTION

The TC534200P/F is a 4,194,304 bits read only memory organized as 262,144 words by 16 bits when $\overline{\text{BYTE}}$ is logical high, and is organized as 524,288 words by 8 bits when $\overline{\text{BYTE}}$ is logical low.

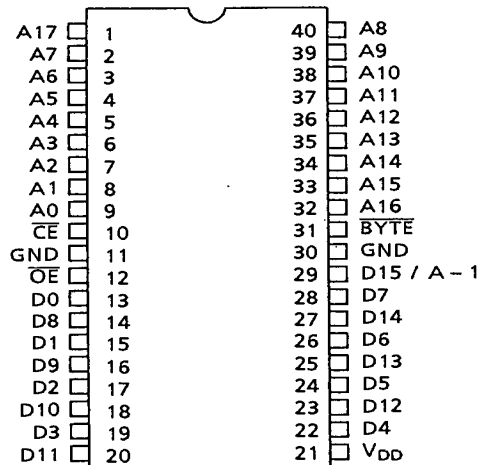
The TC534200P/F is most suitable for the program memory, data memory, and character generator.

The TC534200P/F is packaged in a standard 600mil 40pin DIP, or 525mil 40 pin SOP.

FEATURES

- Single 5V Power Supply
- Access Time : 150ns (Max.)
- Power Dissipation
 - Operating Current : 50mA (Max.)
 - Standby Current : 20 μ A (Max.)
- Fully Static Operation
- All Inputs and Outputs : TTL Compatible
- Three State Outputs
- TC534200P : DIP40 – P – 600
- TC534200F : SOP40 – P – 525

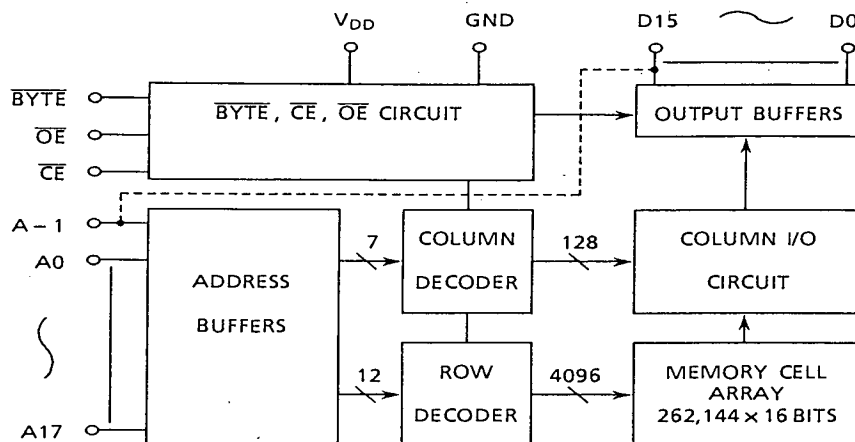
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A17	Address inputs
D0~D14	Data Outputs
$\overline{\text{CE}}$	Chip Enable Input
$\overline{\text{OE}}$	Output Enable Input
D15 / A – 1	Data Output / Addrss Input
$\overline{\text{BYTE}}$	Word, Byte selection Input
V _{DD}	Power Supply
GND	Ground

BLOCK DIAGRAM



MODE SELECTION

MODE	CE	OE	BYTE	D0 - D7	D8 - D14	D15 / A - 1	Power
Read (16 Bit)	L	L	H	Data Out			Active
Read (8 Bit)	L	L	L	Data Out (Lower 8bit)	High Impedance	L	Active
Read (8 Bit)	L	L	L	Data Out (Upper 8bit)	High Impedance	H	Active
Output Deselect	L	H	*	High Impedance			Active
Standby	H	*	*	High Impedance			Standby

H : VIH L : VIL * : VIH or VIL

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
VDD	Power Supply Voltage	- 0.5~7.0	V
VIN	Input Voltage	- 0.5~VDD	V
VOUT	Output Voltage	0~VDD	V
PD	Power Dissipation	1.0 / 0.6*	W
TSTG	Storage Temperature	- 55~150	°C
TOPR	Operating Temperature	0~70	°C
TSOLDER	Soldering Temperature · Time	260 · 10	°C · sec

* SOP

TC534200P/F

D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.2	—	V _{DD} + 0.3	V
V _{IL}	Input Low Voltage	- 0.3	—	0.8	V

D.C. and OPERATING CHARACTERISTICS (Ta = 0~70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I _{IL}	Input Leakage Current	V _{IN} = 0~V _{DD}	—	± 1.0	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0~V _{DD}	—	± 5.0	μA
I _{OH}	Output High Current	V _{OH} = 2.4V	- 1.0	—	mA
I _{OL}	Output Low Current	V _{OL} = 0.4V	2.0	—	mA
I _{DDs1}	Standby Current	$\overline{CE} = V_{IH}$	—	2	mA
I _{DDs2}		$\overline{CE} = V_{DD} - 0.2V$	—	20	μA
I _{DDO1}	Operating Current	V _{IN} = V _{IH} / V _{IL} , t _{cycle} = 150ns	—	60	mA
I _{DDO2}		V _{IN} = V _{DD} - 0.2V / 0.2V, t _{cycle} = 150ns	—	50	mA

CAPACITANCE f = 1MHz, Ta = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = 0V	—	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	—	12	pF

Note : This Parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

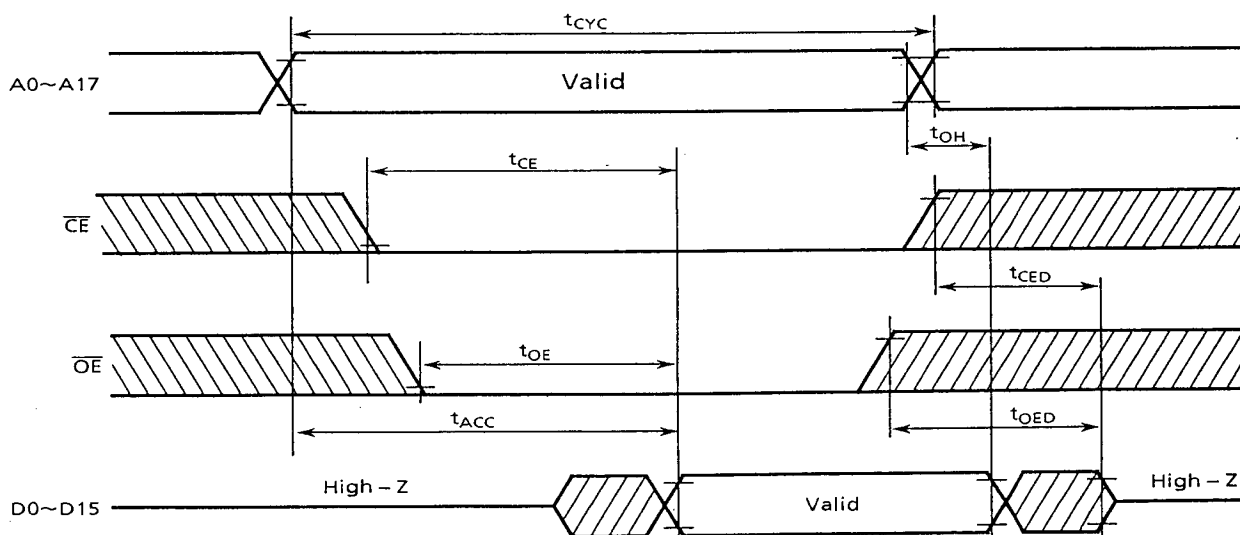
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{CYC}	Cycle Time	150	—	ns
t_{ACC}	Address Access Time	—	150	ns
t_{CE}	Chip Enable Access Time	—	150	ns
t_{BT}	$\overline{\text{BYTE}}$ Access Time	—	150	ns
t_{OE}	Output Enable Access Time	—	70	ns
t_{CED}	Output Disable Time from $\overline{\text{CE}}$	—	60	ns
t_{OED}	Output Disable Time from $\overline{\text{OE}}$	—	60	ns
t_{BTD}	Output Disable Time from $\overline{\text{BYTE}}$	—	60	ns
t_{OH}	Output Hold Time	5	—	ns

A.C. TEST CONDITIONS

Output Load : 100pF + 1TTL
 Input Levels : 0.6V, 2.4V
 Timing Measurement Reference Levels Input : 0.8V, 2.2V
 Output : 0.8V, 2.0V
 Input Rise and Fall Time : 5ns

TIMING WAVEFORMS

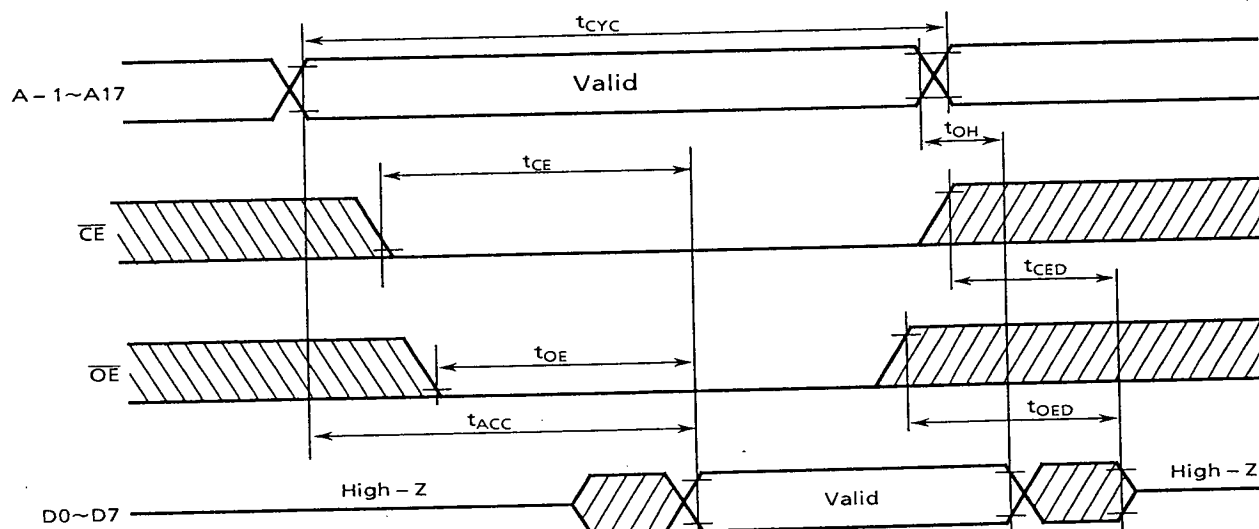
WORD - WIDE READ MODE



Note: $\overline{\text{BYTE}} = V_{IH}$

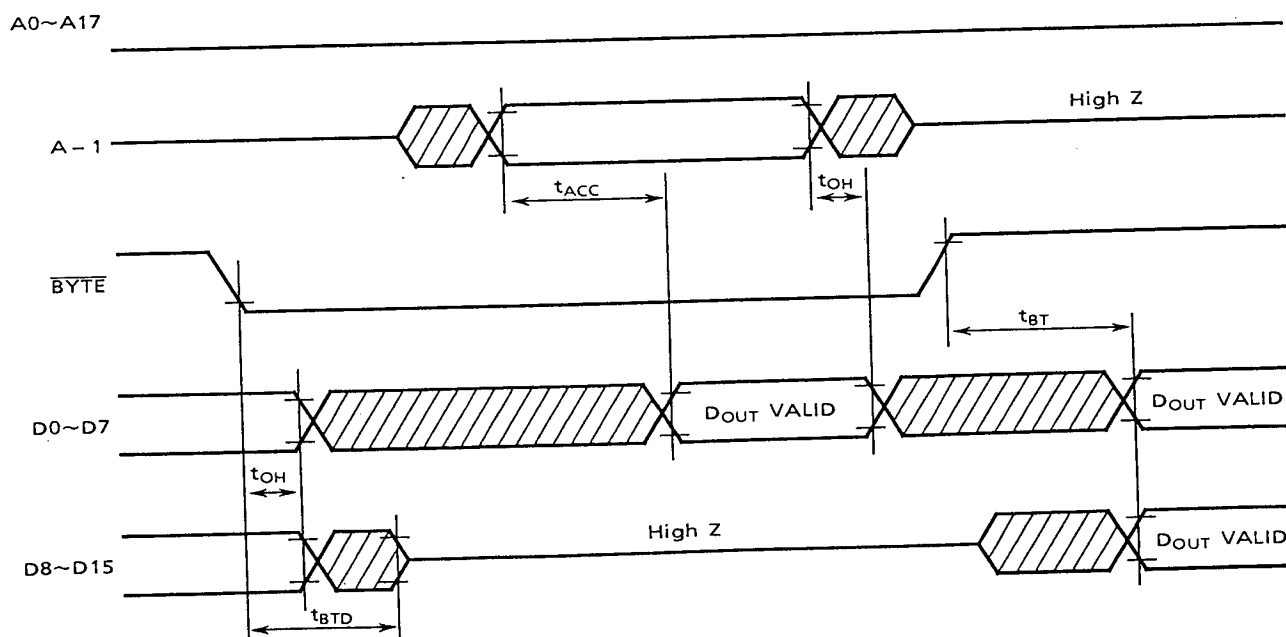
TC534200P/F

BYTE – WIDE READ MODE



Note: $\overline{\text{BYTE}} = V_{IL}$

BYTE TRANSITION



Note: $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$

SILICON STACKED GATE MOS INTEGRATED CIRCUIT

TC538000AP/AF

8M BIT (1M WORD × 8 BIT) CMOS MASK ROM

DESCRIPTION

The TC538000AP/AF is a 8,388,608 bits read only memory organized as 1,048,576 words by 8bits.

The TC538000AP/AF is fabricated using Toshiba's advanced CMOS technology which provides the high speed and low power features with access time of 150ns, an operation current of 55mA at 6.7MHz and a standby current of 100 μ A.

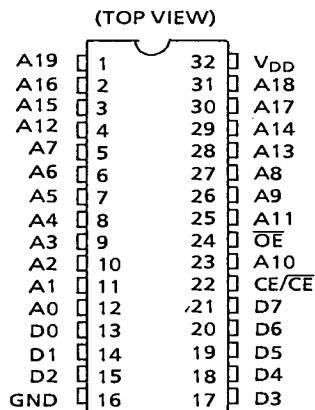
The TC538000AP/AF has one programmable chip enable input $\overline{CE}/CE$ for device selection.

The TC538000AP/AF is packaged in a standard 600mil 32pin DIP , 525mil 32pin SOP

FEATURES

- Single 5V Power Supply
- Access Time : 150ns (Max.) $V_{DD}=5V \pm 10\%$
- Power Dissipation
 - Operating Current : 55mA (Max.)
 - Standby Current : 100 μ A (Max.)
- All Inputs and Outputs : TTL Compatible
- Three State Outputs
- Fully Static Operation
- Programmable Chip Enable
- TC538000AP : DIP32-P-600
- TC538000AF : SOP32-P-525

PIN CONNECTION

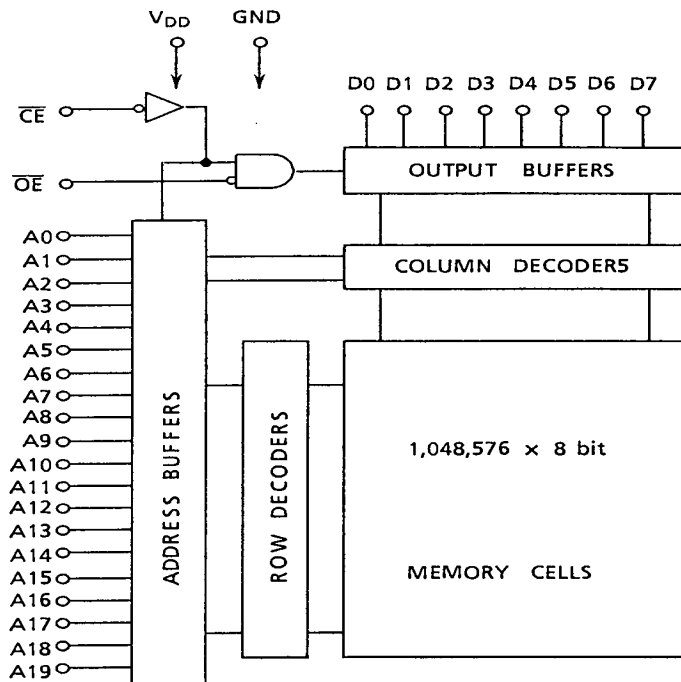


TC538000AP/AF

PIN NAMES

A0~A19	Address inputs
D0~D7	Data Outputs
$\overline{OE}$	Output Enable Input
$\overline{CE}/CE$	Chip Enable Input
V_{DD}	Power Supply
GND	Ground

BLOCK DIAGRAM



TC538000AP/AF

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	- 0.5~7.0	V
V_{IN}	Input Voltage	- 0.5~ V_{DD}	V
V_{OUT}	Output Voltage	0~ V_{DD}	V
P_D	Power Dissipation	1.0 / 0.6*	W
T_{STG}	Storage Temperature	- 55~150	°C
T_{OPR}	Operating Temperature	0~70	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec

Note : * Plastic FP.

D.C. OPERATING CONDITIONS ($T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.5	V
V_{IH}	Input High Voltage	2.2	$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage	- 0.3	0.8	V

D.C. and OPERATING CHARACTERISTICS ($V_{DD} = 5V \pm 10\%$, $T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	-	± 5.0	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$, $V_{OUT} = 0 \sim V_{DD}$	-	± 5.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$	- 1.0	-	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$	2.0	-	mA
I_{DDs1}	Standby Current	$\overline{CE} = V_{IH}$	-	2	mA
I_{DDs2}		$\overline{CE} = V_{DD}$ and $V_{IN} = 0V$ (V_{DD})	-	100	μA
I_{DDO1}	Operating Current	$V_{IN} = V_{IH} / V_{IL}$, $t_{cycle} = 150\text{ns}$	-	60	mA
I_{DDO2}		$V_{IN} = V_{DD} / 0V$, $t_{cycle} = 150\text{ns}$	-	55	mA

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	$f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$	-	10	pF
C_{OUT}	Output Capacitance	$f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$	-	10	pF

Note : This Parameter is periodically sampled and is not 100% tested.

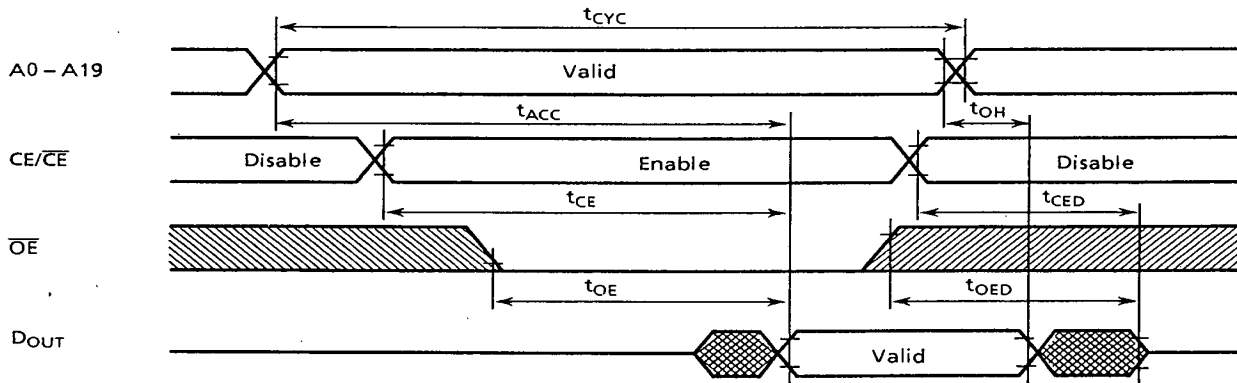
A.C. CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{ACC}	Access Time	—	150	ns
t_{CE}	Chip Enable Access Time	—	150	ns
t_{OE}	Output Enable Access Time	—	70	ns
t_{CED}	Output Disable Time from $\overline{CE}$	0	60	ns
t_{OED}	Output Disable Time from $\overline{OE}$	0	60	ns
t_{OH}	Output Hold Time	5	—	ns
t_{CYC}	Cycle Time	150	—	ns

A.C. TEST CONDITIONS

Output Load	: 100pF + 1TTL
Input Levels	: 0.6V , 2.4V
Timing Measurement Reference Levels	Input : 0.8V , 2.2V
	Output : 0.8V , 2.0V
Input Rise and Fall Time	: 5ns

TIMING WAVEFORMS



OPERATION MODE

MODE	$\overline{CE}$ (CE)	$\overline{OE}$	A0~A19	Outputs	Power
Read	L (H)	L	Valid	Data Out	Operating
Standby	H (L)	*	*	High-Z	Standby
Output Deselect	L (H)	H	*	High-Z	Operating

H : VIH L : VIL * : VIH or VIL

TC538200AP/AF

TENTATIVE

8M BIT (512K WORD × 16 BIT / 1M WORD × 8BIT) CMOS MASK ROM

DESCRIPTION

The TC538200AP/AF is a 8,388,608 bits read only memory organized as 524,288 words by 16 bits when $\overline{\text{BYTE}}$ is logical high, and is organized as 1,048,576 words by 8 bits when $\overline{\text{BYTE}}$ is logical low.

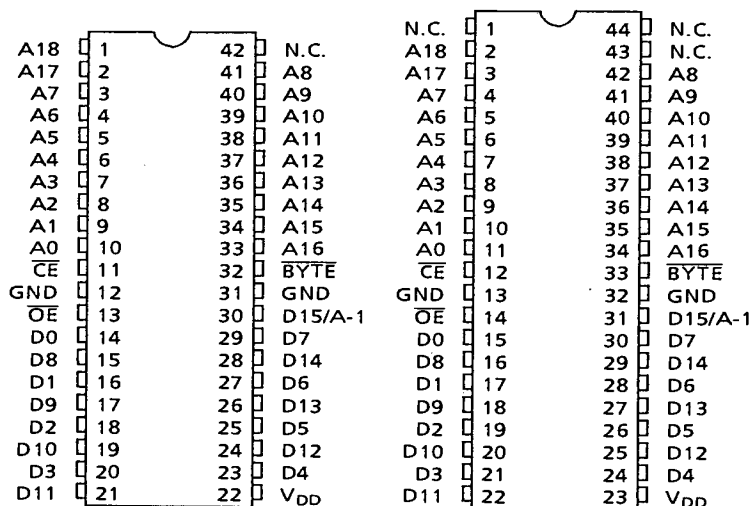
The TC538200AP/AF is most suitable for the program memory, data memory, and character generator.

The TC538200AP/AF is packaged in a standard 600mil 42pin DIP, or 600mil 44 pin SOP.

FEATURES

- Single 5V Power Supply
- Access Time : 150ns (Max.)
- Power Dissipation
 - Operating Current : 60mA (Max.)
 - Standby Current : 100 μ A (Max.)
- Fully Static Operation
- All Inputs and Outputs : TTL Compatible
- Three State Outputs
- TC538200AP : DIP42-P-600
- TC538200AF : SOP44-P-600

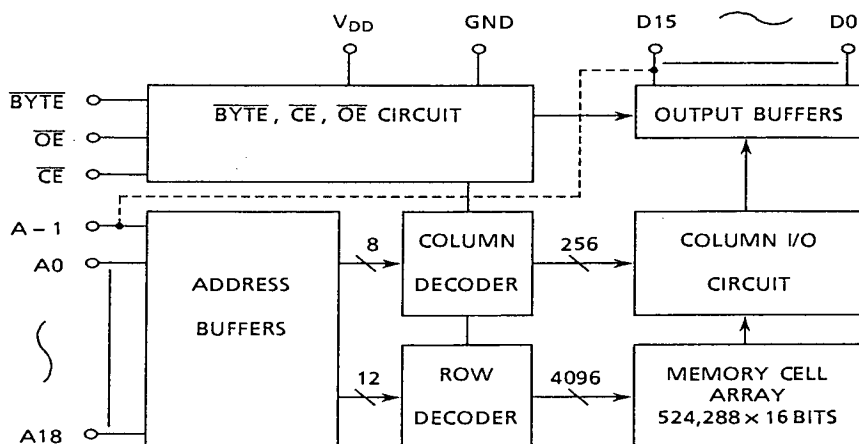
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A18	Address inputs
D0~D14	Data Outputs
$\overline{\text{CE}}$	Chip Enable Input
$\overline{\text{OE}}$	Output Enable Input
D15/A-1	Data Output/Addrss Input
$\overline{\text{BYTE}}$	Word, Byte selection Input
V _{DD}	Power Supply
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MODE SELECTION

MODE	$\overline{CE}$	$\overline{OE}$	BYTE	D0 - D7	D8 - D14	D15 / A - 1	Power
Read (16 Bit)	L	L	H	Data Out			Active
Read (8 Bit)	L	L	L	Data Out (Lower 8bit)	High Impedance	L	Active
Read (8 Bit)	L	L	L	Data Out (Upper 8bit)	High Impedance	H	Active
Output Deselect	L	H	*	High Impedance			Active
Standby	H	*	*	High Impedance			Standby

H : V_{IH} L : V_{IL} * : V_{IH} or V_{IL}

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	- 0.5~7.0	V
V_{IN}	Input Voltage	- 0.5~ V_{DD}	V
V_{OUT}	Output Voltage	0~ V_{DD}	V
P_D	Power Dissipation	1.0 / 0.6*	W
T_{STG}	Storage Temperature	- 55~150	°C
T_{OPR}	Operating Temperature	0~70	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec

* SOP

TC538200AP/AF

D.C. OPREATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.2	—	V _{DD} + 0.3	V
V _{IL}	Input Low Voltage	-0.3	—	0.8	V

D.C. and OPERATING CHARACTERISTICS (Ta = 0~70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I _{IL}	Input Leakage Current	V _{IN} = 0~V _{DD}	—	± 1.0	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0~V _{DD}	—	± 5.0	μA
I _{OH}	Output High Current	V _{OH} = 2.4V	-1.0	—	mA
I _{OL}	Output Low Current	V _{OL} = 0.4V	2.0	—	mA
I _{DDs1}	Standby Current	$\overline{CE} = V_{IH}$	—	2	mA
I _{DDs2}		$\overline{CE} = V_{DD} - 0.2V$	—	100	μA
I _{DDO1}	Opereating Current	V _{IN} = V _{IH} / V _{IL} , t _{cycle} = 150ns	—	70	mA
I _{DDO2}		V _{IN} = V _{DD} - 0.2V / 0.2V, t _{cycle} = 150ns	—	60	mA

CAPACITANCE f = 1MHz, Ta = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = 0V	—	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	—	12	pF

Note : This Paramenter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

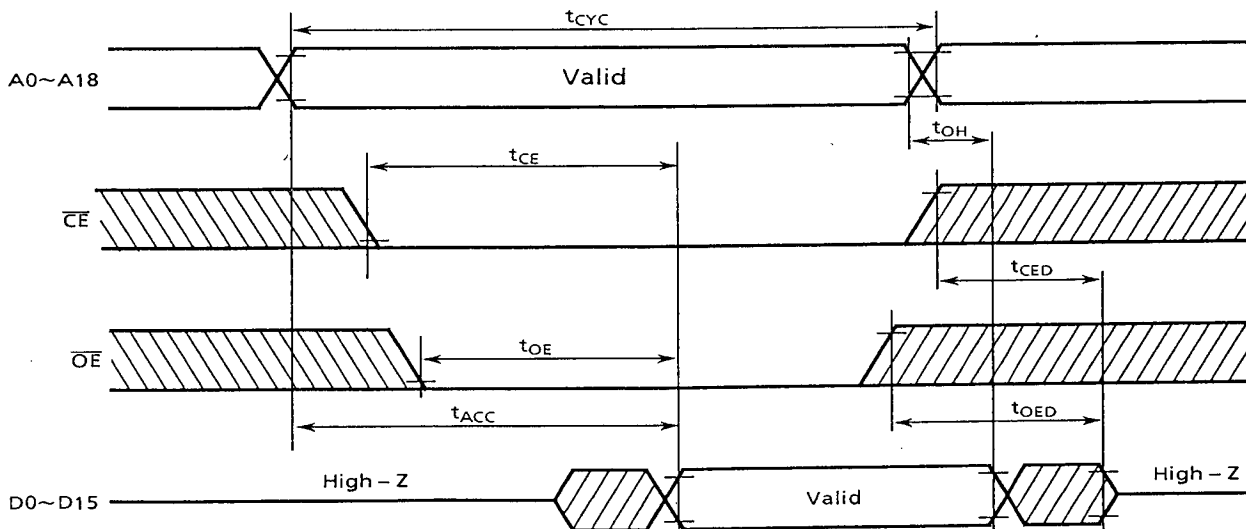
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{CYC}	Cycle Time	150	—	ns
t_{ACC}	Address Access Time	—	150	ns
t_{CE}	Chip Enable Access Time	—	150	ns
t_{BT}	BYTE Access Time	—	150	ns
t_{OE}	Output Enable Access Time	—	70	ns
t_{CED}	Output Disable Time from $\overline{CE}$	—	60	ns
t_{OED}	Output Disable Time from $\overline{OE}$	—	60	ns
t_{BTD}	Output Disable Time from $\overline{BYTE}$	—	60	ns
t_{OH}	Output Hold Time	5	—	ns

A.C. TEST CONDITIONS

Output Load : 100pF + 1TTL
 Input Levels : 0.6V , 2.4V
 Timing Measurement Reference Levels Input : 0.8V , 2.2V
 Output : 0.8V , 2.0V
 Input Rise and Fall Time : 5ns

TIMING WAVEFORMS

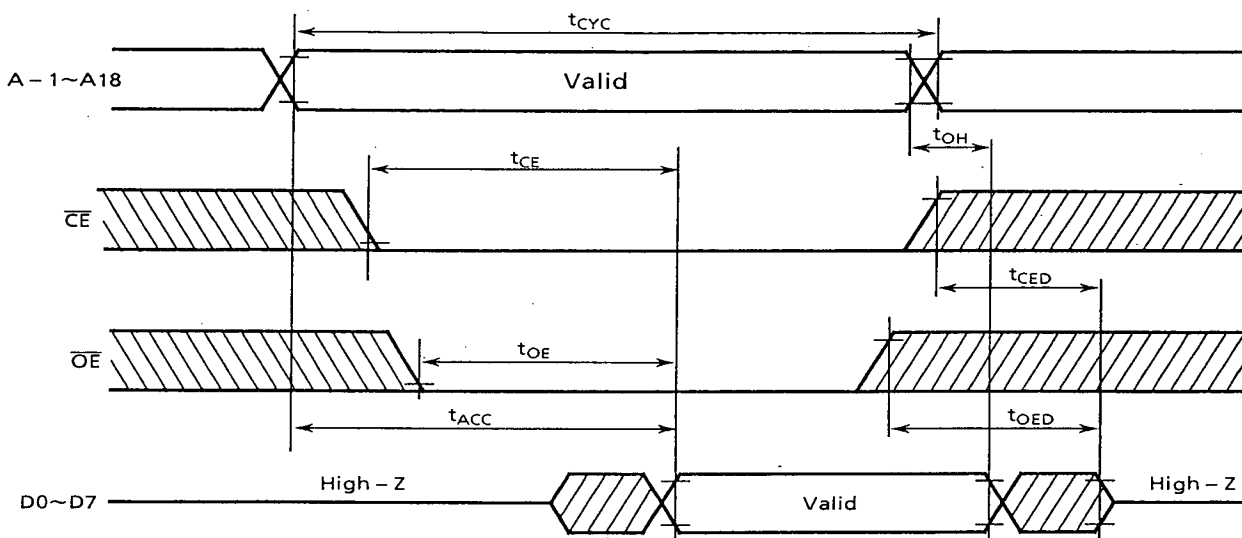
WORD - WIDE READ MODE



Note: $\overline{BYTE} = V_{IH}$

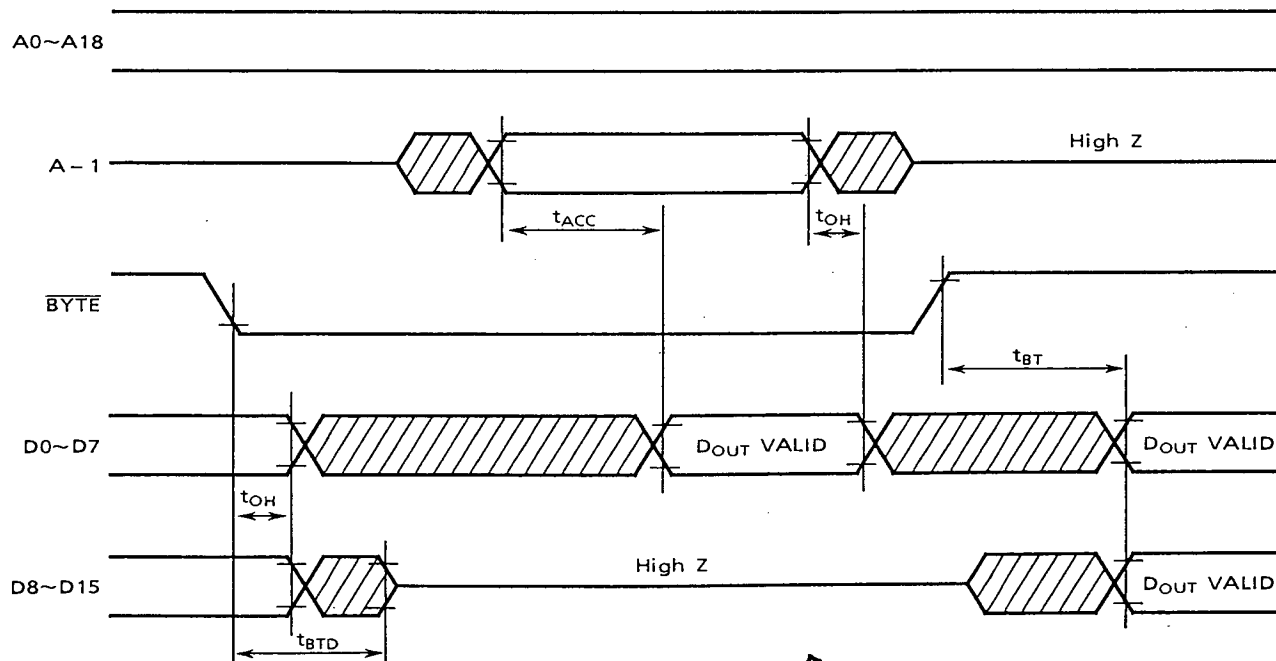
TC538200AP/AF

BYTE - WIDE READ MODE



Note: $\overline{BYTE} = V_{IL}$

BYTE TRANSITION



Note: $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$

SILICON STACKED GATE MOS INTEGRATED CIRCUIT

TC5316200AP/AF

16M BIT (1M WORD × 16 BIT/2M WORD × 8BIT) CMOS MASK ROM

DESCRIPTION

The TC5316200AP/AF is a 16,777,216 bits read only memory organized as 1,048,576 words by 16 bits when BYTE is logical high, and is organized as 2,097,152 words by 8 bits when BYTE is logical low.

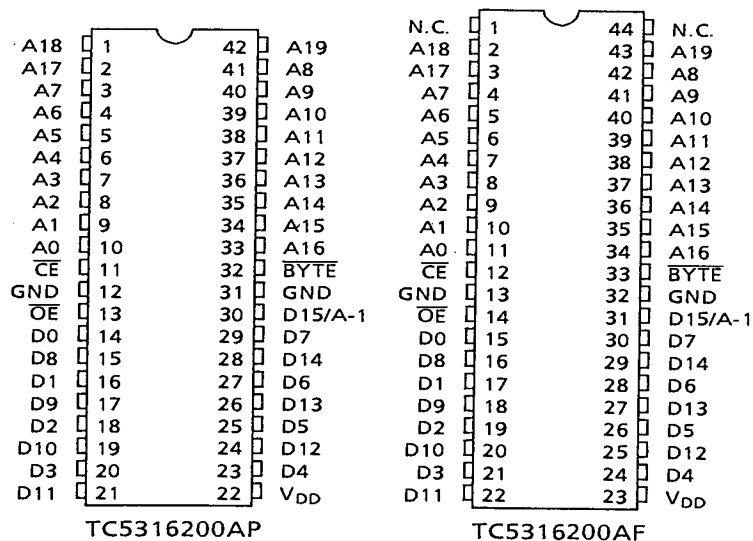
The TC5316200AP/AF is most suitable for the program memory, data memory, and character generator.

The TC5316200AP/AF is packaged in a standard 600mil 42pin DIP, or 600mil 44 pin SOP.

FEATURES

- Single 5V Power Supply
- Access Time : 150ns (Max.)
- Power Dissipation
 - Operating Current : 60mA (Max.)
 - Standby Current : 100 μ A (Max.)
- Fully Static Operation
- All Inputs and Outputs : TTL Compatible
- Three State Outputs
- TC5316200AP : DIP42-P-600
- TC5316200AF : SOP44-P-600

PIN CONNECTION (TOP VIEW)

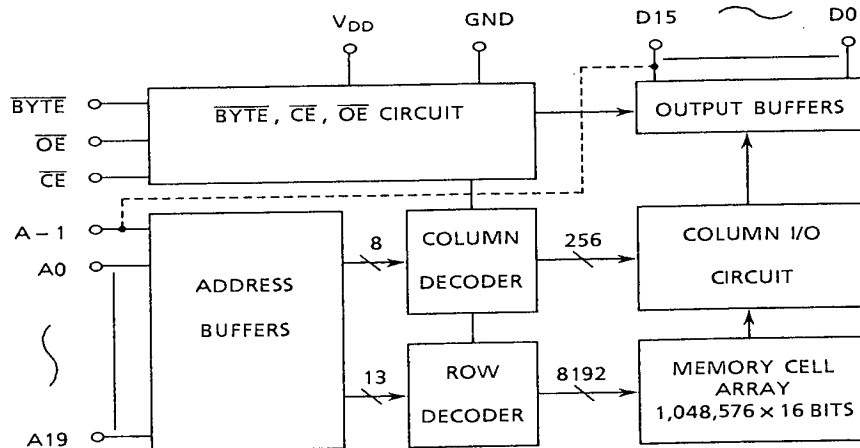


PIN NAMES

A0~A19	Address inputs
D0~D14	Data Outputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
D15/A-1	Data Output/ Addrss Input
<u>BYTE</u>	Word, Byte selection Input
V _{DD}	Power Supply
GND	Ground
N.C.	No Connection

TC5316200AP/AF

BLOCK DIAGRAM



MODE SELECTION

MODE	CE	OE	BYTE	D0 - D7	D8 - D14	D15 / A - 1	Power
Read (16 Bit)	L	L	H	Data Out			Active
Read (8 Bit)	L	L	L	Data Out (Lower 8bit)	High Impedance	L	Active
Read (8 Bit)	L	L	L	Data Out (Upper 8bit)	High Impedance	H	Active
Output Deselect	L	H	*	High Impedance			Active
Standby	H	*	*	High Impedance			Standby

H : V_{IH} L : V_{IL} * : V_{IH} or V_{IL}

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5~7.0	V
V_{IN}	Input Voltage	-0.5~ V_{DD}	V
V_{OUT}	Output Voltage	0~ V_{DD}	V
P_D	Power Dissipation	1.0/0.6*	W
T_{STG}	Storage Temperature	-55~150	°C
T_{OPR}	Operating Temperature	0~70	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec

* SOP

D.C. OPREATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.2	—	V _{DD} + 0.3	V
V _{IL}	Input Low Voltage	− 0.3	—	0.8	V

D.C. and OPERATING CHARACTERISTICS (Ta = 0~70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I _{IL}	Input Leakage Current	V _{IN} = 0~V _{DD}	—	± 1.0	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0~V _{DD}	—	± 5.0	μA
I _{OH}	Output High Current	V _{OH} = 2.4V	− 1.0	—	mA
I _{OL}	Output Low Current	V _{OL} = 0.4V	2.0	—	mA
I _{DD51}	Standby Current	$\overline{CE} = V_{IH}$	—	2	mA
I _{DD52}		$\overline{CE} = V_{DD} - 0.2V$	—	100	μA
I _{DDO1}	Opereating Current	V _{IN} = V _{IH} / V _{IL} , t _{cycle} = 150ns	—	70	mA
I _{DDO2}		V _{IN} = V _{DD} − 0.2V / 0.2V, t _{cycle} = 150ns	—	60	mA

CAPACITANCE f = 1MHz, Ta = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = 0V	—	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	—	12	pF

Note : This Paramenter is periodically sampled and is not 100% tested.

TC5316200AP/AF

A.C. CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{CYC}	Cycle Time	150	—	ns
t_{ACC}	Address Access Time	—	150	ns
t_{CE}	Chip Enable Access Time	—	150	ns
t_{BT}	BYTE Access Time	—	150	ns
t_{OE}	Output Enable Access Time	—	70	ns
t_{CED}	Output Disable Time from $\overline{CE}$	—	40	ns
t_{OED}	Output Disable Time from $\overline{OE}$	—	40	ns
t_{BTD}	Output Disable Time from BYTE	—	40	ns
t_{OH}	Output Hold Time	5	—	ns

A.C. TEST CONDITIONS

Output Load

: 100pF + 1TTL

Input Levels

: 0.6V, 2.4V

Timing Measurement Reference Levels

Input : 0.8V, 2.2V

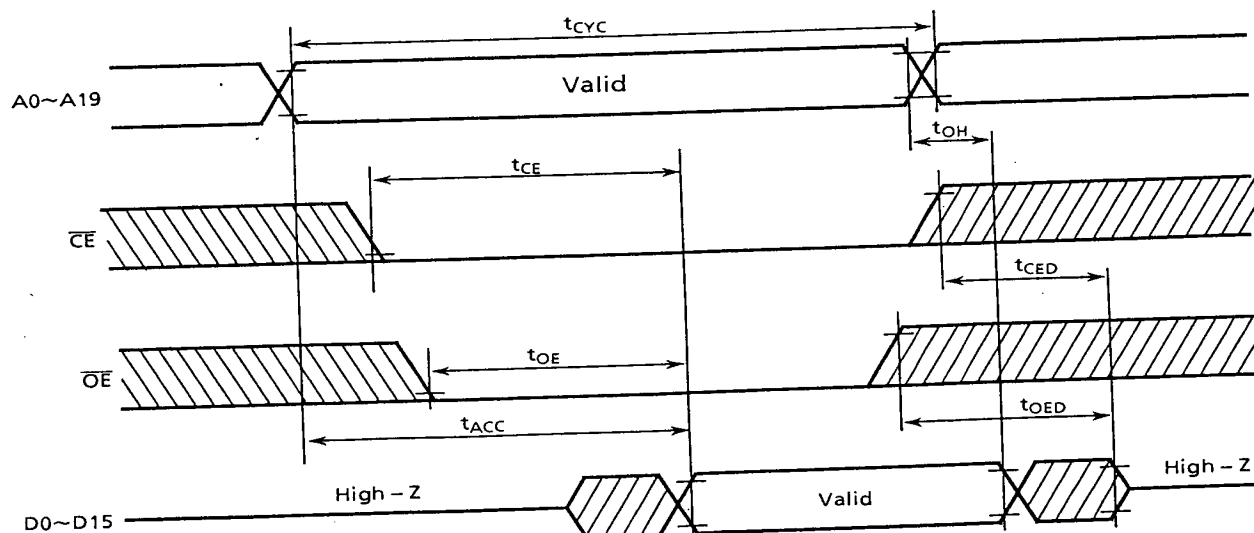
Output : 0.8V, 2.0V

Input Rise and Fall Time

: 5ns

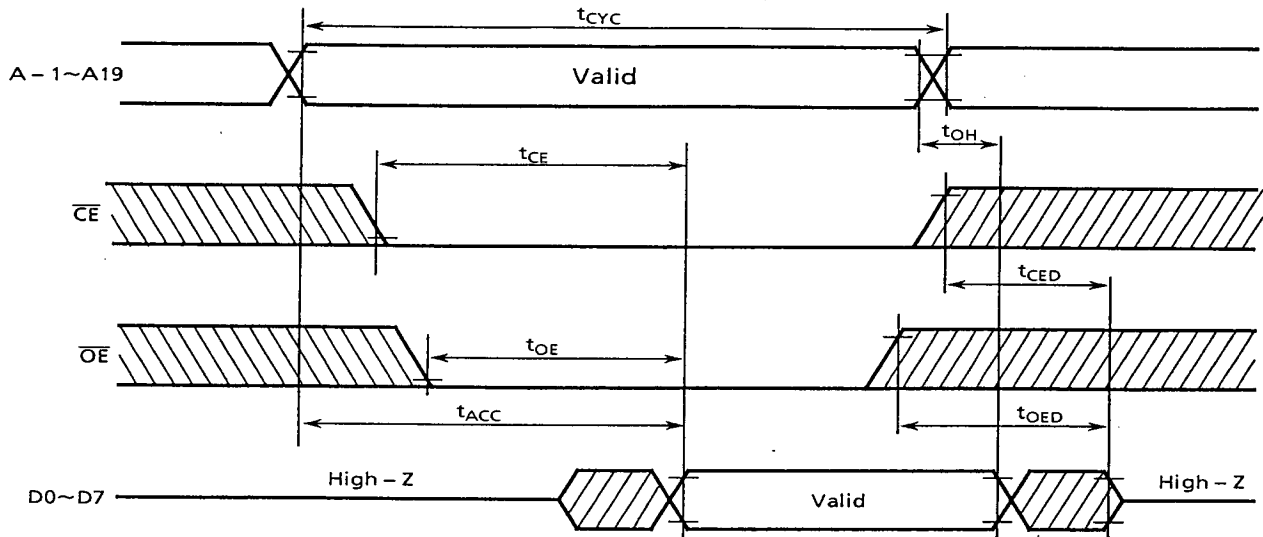
TIMING WAVEFORMS

WORD - WIDE READ MODE



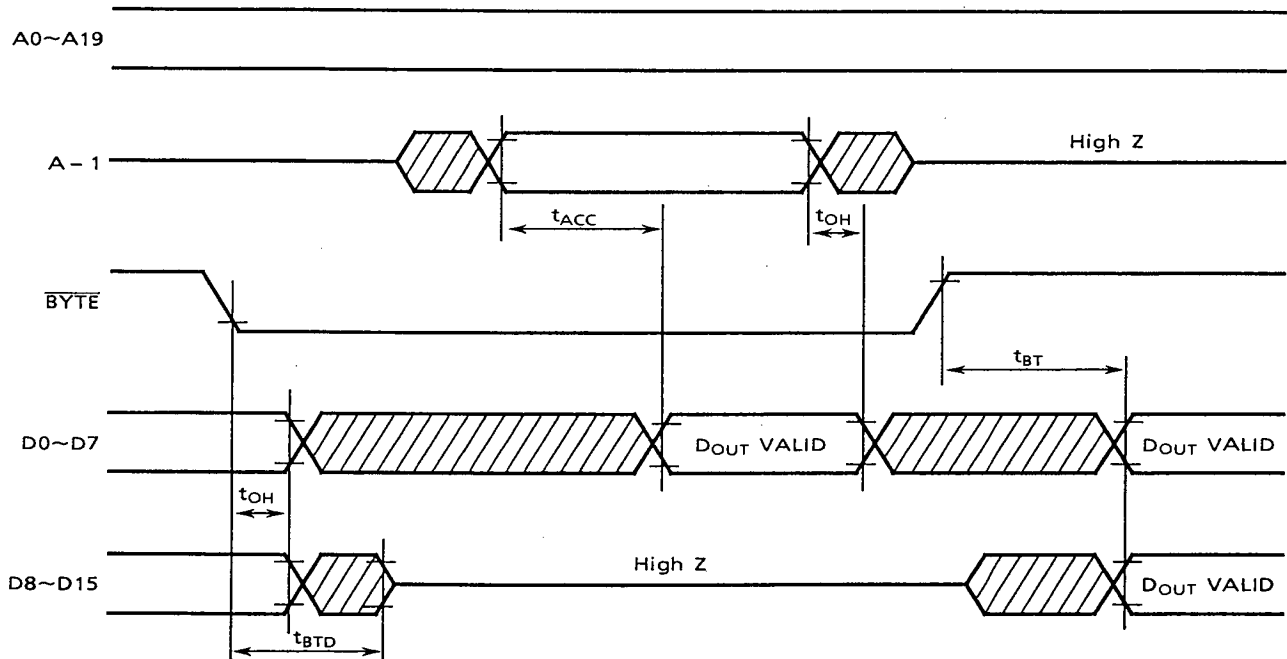
Note: $\overline{BYTE} = V_{IH}$

BYTE - WIDE READ MODE



Note: $\overline{BYTE} = V_{IL}$

BYTE TRANSITION



Note: $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$

TC5316200AFT

TENTATIVE

16M BIT (1M WORD × 16 BIT/2M WORD × 8BIT) CMOS MASK ROM

DESCRIPTION

The TC5316200AFT is a 16,777,216 bits read only memory organized as 1,048,576 words by 16 bits when $\overline{\text{BYTE}}$ is logical high, and is organized as 2,097,152 words by 8 bits when $\overline{\text{BYTE}}$ is logical low.

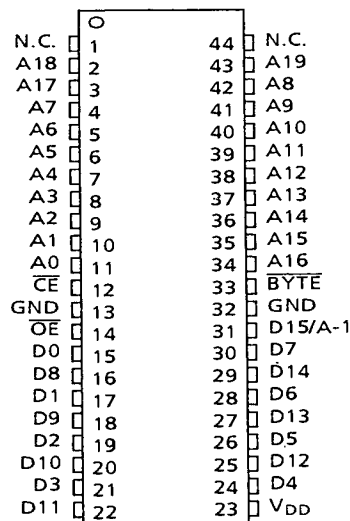
The TC5316200AFT is most suitable for the program memory, data memory, and character generator.

The TC5316200AFT is packaged in a 400mil 44pin TSOP Tepe II.

FEATURES

- Single 5V Power Supply
- Access Time : 150ns (Max.)
- Power Dissipation
 - Operating Current : 60mA (Max.)
 - Standby Current : 100 μ A (Max.)
- Fully Static Operation
- All Inputs and Outputs : TTL Compatible
- Three State Outputs
- TC5316200AFT : TSOP44-P-400

PIN CONNECTION (TOP VIEW)

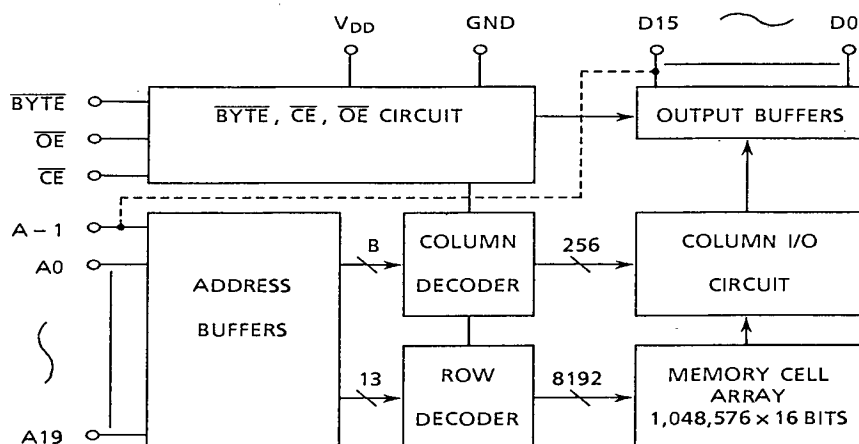


TC5316200AFT

PIN NAMES

A0~A19	Address inputs
D0~D14	Data Outputs
$\overline{\text{CE}}$	Chip Enable Input
$\overline{\text{OE}}$	Output Enable Input
D15/A-1	Data Output/Addrss Input
$\overline{\text{BYTE}}$	Word, Byte selection Input
VDD	Power Supply
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MODE SELECTION

MODE	$\overline{CE}$	$\overline{OE}$	BYTE	D0 - D7	D8 - D14	D15 / A - 1	Power
Read (16 Bit)	L	L	H	Data Out			Active
Read (8 Bit)	L	L	L	Data Out (Lower 8bit)	High Impedance	L	Active
Read (8 Bit)	L	L	L	Data Out (Upper 8bit)	High Impedance	H	Active
Output Deselect	L	H	*	High Impedance			Active
Standby	H	*	*	High Impedance			Standby

H : V_{IH} L : V_{IL} * : V_{IH} or V_{IL}

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	- 0.5~7.0	V
V_{IN}	Input Voltage	- 0.5~ V_{DD}	V
V_{OUT}	Output Voltage	0~ V_{DD}	V
P_D	Power Dissipation	0.6	W
T_{STG}	Storage Temperature	- 55~150	°C
T_{OPR}	Operating Temperature	0~70	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec

TC5316200AFT

D.C. OPREATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.2	—	V _{DD} + 0.3	V
V _{IL}	Input Low Voltage	− 0.3	—	0.8	V

D.C. and OPERATING CHARACTERISTICS (Ta = 0~70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I _{IL}	Input Leakage Current	V _{IN} = 0~V _{DD}	—	± 1.0	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0~V _{DD}	—	± 5.0	μA
I _{OH}	Output High Current	V _{OH} = 2.4V	− 1.0	—	mA
I _{OL}	Output Low Current	V _{OL} = 0.4V	2.0	—	mA
I _{DDs1}	Standby Current	$\overline{CE} = V_{IH}$	—	2	mA
I _{DDs2}		$\overline{CE} = V_{DD} - 0.2V$	—	100	μA
I _{DDO1}	Opereating Current	V _{IN} = V _{IH} / V _{IL} , t _{cycle} = 150ns	—	70	mA
I _{DDO2}		V _{IN} = V _{DD} − 0.2V / 0.2V, t _{cycle} = 150ns	—	60	mA

CAPACITANCE f = 1MHz , Ta = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = 0V	—	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	—	12	pF

Note : This Paramenter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5\text{V} \pm 10\%$)

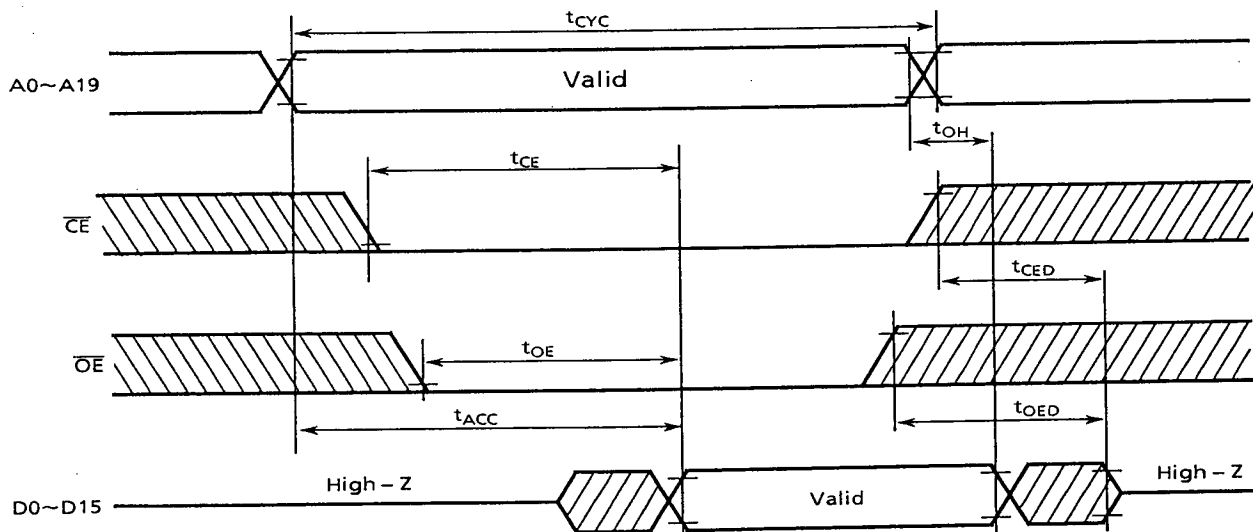
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{CYC}	Cycle Time	150	—	ns
t_{ACC}	Address Access Time	—	150	ns
t_{CE}	Chip Enable Access Time	—	150	ns
t_{BT}	BYTE Access Time	—	150	ns
t_{OE}	Output Enable Access Time	—	70	ns
t_{CED}	Output Disable Time from $\overline{CE}$	—	40	ns
t_{OED}	Output Disable Time from $\overline{OE}$	—	40	ns
t_{BTD}	Output Disable Time from BYTE	—	40	ns
t_{OH}	Output Hold Time	5	—	ns

A.C. TEST CONDITIONS

Output Load : 100pF + 1TTL
 Input Levels : 0.6V , 2.4V
 Timing Measurement Reference Levels Input : 0.8V , 2.2V
 Output : 0.8V , 2.0V
 Input Rise and Fall Time : 5ns

TIMING WAVEFORMS

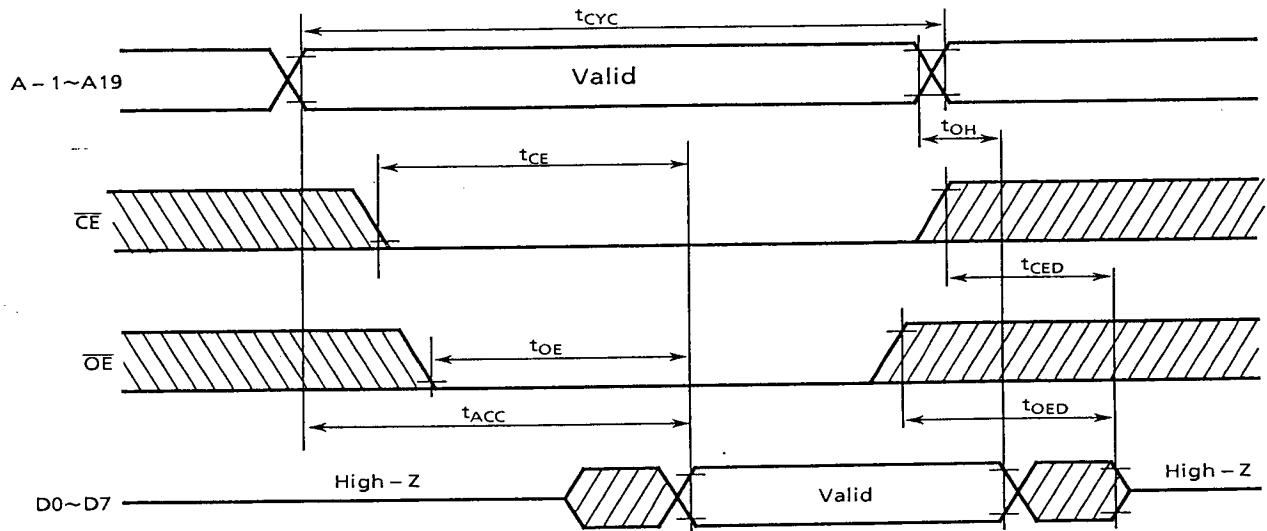
WORD - WIDE READ MODE



Note: $\overline{BYTE} = V_{IH}$

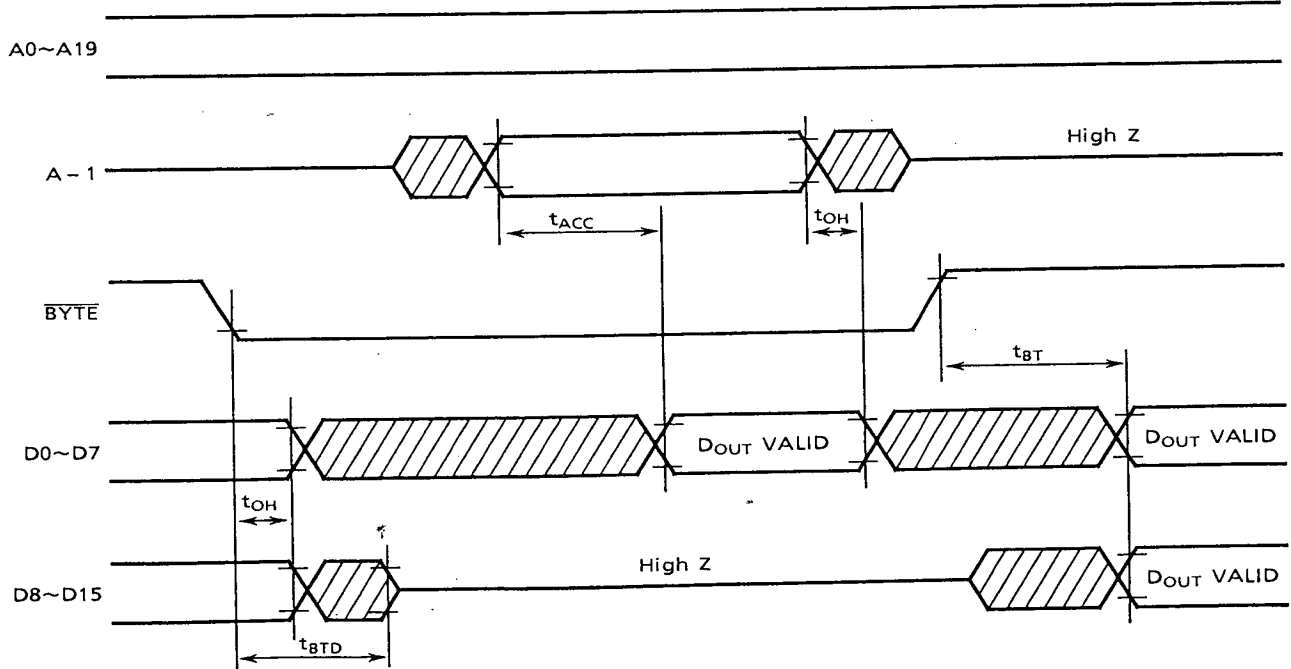
TC5316200AFT

BYTE - WIDE READ MODE



Note: $\overline{BYTE} = V_{IL}$

BYTE TRANSITION



Note: $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$

SILICON STACKED GATE MOS INTEGRATED CIRCUIT

TC5316200BP/BF

16M BIT (1M WORD × 16 BIT/2M WORD × 8BIT) CMOS MASK ROM

DESCRIPTION

The TC5316200BP/BF is a 16,777,216 bits read only memory organized as 1,048,576 words by 16 bits when $\overline{\text{BYTE}}$ is logical high, and is organized as 2,097,152 words by 8 bits when $\overline{\text{BYTE}}$ is logical low.

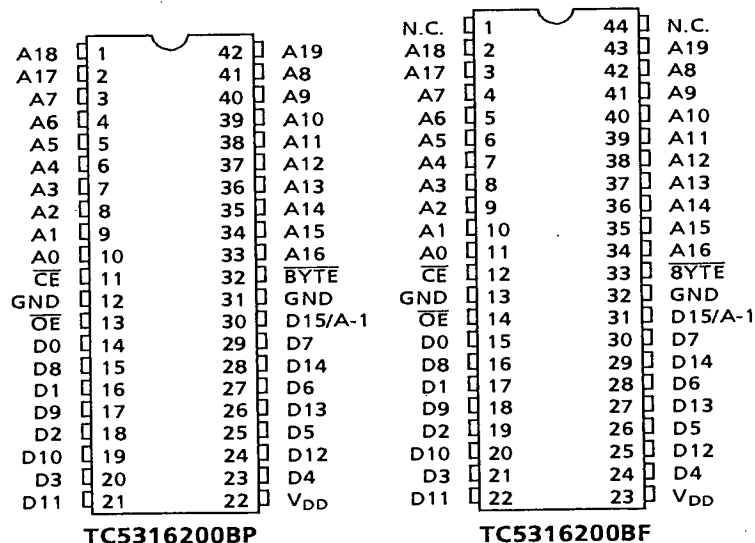
The TC5316200BP/BF is most suitable for the program memory, data memory, and character generator.

The TC5316200BP/BF is packaged in a standard 600mil 42pin DIP, or 600mil 44 pin SOP.

FEATURES

- Single 5V Power Supply
- Access Time : 200ns (Max.)
- Power Dissipation
 - Operating Current : 50mA (Max.)
 - Standby Current : 100 μ A (Max.)
- Fully Static Operation
- All Inputs and Outputs : TTL Compatible
- Three State Outputs
- TC5316200BP : DIP42-P-600
- TC5316200BF : SOP44-P-600

PIN CONNECTION (TOP VIEW)

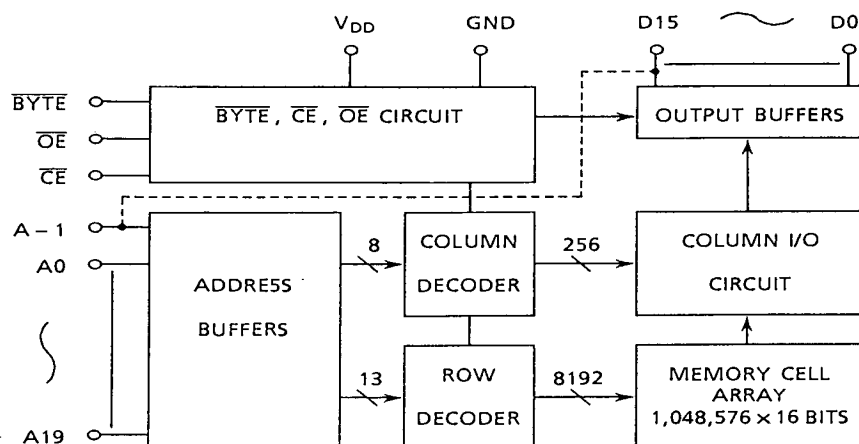


PIN NAMES

A0~A19	Address inputs
D0~D14	Data Outputs
$\overline{\text{CE}}$	Chip Enable Input
$\overline{\text{OE}}$	Output Enable Input
D15/A-1	Data Output/Addrss Input
$\overline{\text{BYTE}}$	Word, 8yte selection Input
V _{DD}	Power Supply
GND	Ground
N.C.	No Connection

TC5316200BP/BF

BLOCK DIAGRAM



MODE SELECTION

MODE	$\overline{CE}$	$\overline{OE}$	BYTE	D0 - D7	D8 - D14	D15 / A - 1	Power
Read (16 Bit)	L	L	H	Data Out			Active
Read (8 Bit)	L	L	L	Data Out (Lower 8bit)	High Impedance	L	Active
Read (8 Bit)	L	L	L	Data Out (Upper 8bit)	High Impedance	H	Active
Output Deselect	L	H	*	High Impedance			Active
Standby	H	*	*	High Impedance			Standby

H : V_{IH} L : V_{IL} * : V_{IH} or V_{IL}

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	- 0.5~7.0	V
V_{IN}	Input Voltage	- 0.5~ V_{DD}	V
V_{OUT}	Output Voltage	0~ V_{DD}	V
P_D	Power Dissipation	1.0 / 0.6*	W
T_{STG}	Storage Temperature	- 55~150	°C
T_{OPR}	Operating Temperature	0~70	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec

* SOP

D.C. OPREATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.2	—	V _{DD} + 0.3	V
V _{IL}	Input Low Voltage	- 0.3	—	0.8	V

D.C. and OPERATING CHARACTERISTICS (Ta = 0~70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I _{IL}	Input Leakage Current	V _{IN} = 0~V _{DD}	—	± 5.0	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0~V _{DD}	—	± 5.0	μA
I _{OH}	Output High Current	V _{OH} = 2.4V	- 1.0	—	mA
I _{OL}	Output Low Current	V _{OL} = 0.4V	2.0	—	mA
I _{DDs1}	Standby Current	$\overline{CE} = V_{IH}$	—	2	mA
I _{DDs2}		$\overline{CE} = V_{DD} - 0.2V$	—	100	μA
I _{DDO1}	Opereating Current	V _{IN} = V _{IH} / V _{IL} , t _{cycle} = 200ns, I _{OUT} = 0mA	—	60	mA
I _{DDO2}		V _{IN} = V _{DD} - 0.2V / 0.2V, t _{cycle} = 200ns, I _{OUT} = 0mA	—	50	mA

CAPACITANCE f = 1MHz , Ta = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = 0V	—	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	—	12	pF

Note : This Paramenter is periodically sampled and is not 100% tested.

TC5316200BP/BF

A.C. CHARACTERISTICS (Ta = 0~70°C, VDD = 5V ± 10%)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t _{CYC}	Cycle Time	200	—	ns
t _{ACC}	Address Access Time	—	200	ns
t _{CE}	Chip Enable Access Time	—	200	ns
t _{BT}	BYTE Access Time	—	200	ns
t _{OE}	Output Enable Access Time	—	70	ns
t _{CED}	Output Disable Time from $\overline{\text{CE}}$	—	60	ns
t _{OED}	Output Disable Time from $\overline{\text{OE}}$	—	60	ns
t _{BSD}	Output Disable Time from $\overline{\text{BYTE}}$	—	60	ns
t _{OH}	Output Hold Time	5	—	ns

A.C. TEST CONDITIONS

Output Load : 100pF + 1TTL

Input Levels : 0.6V, 2.4V

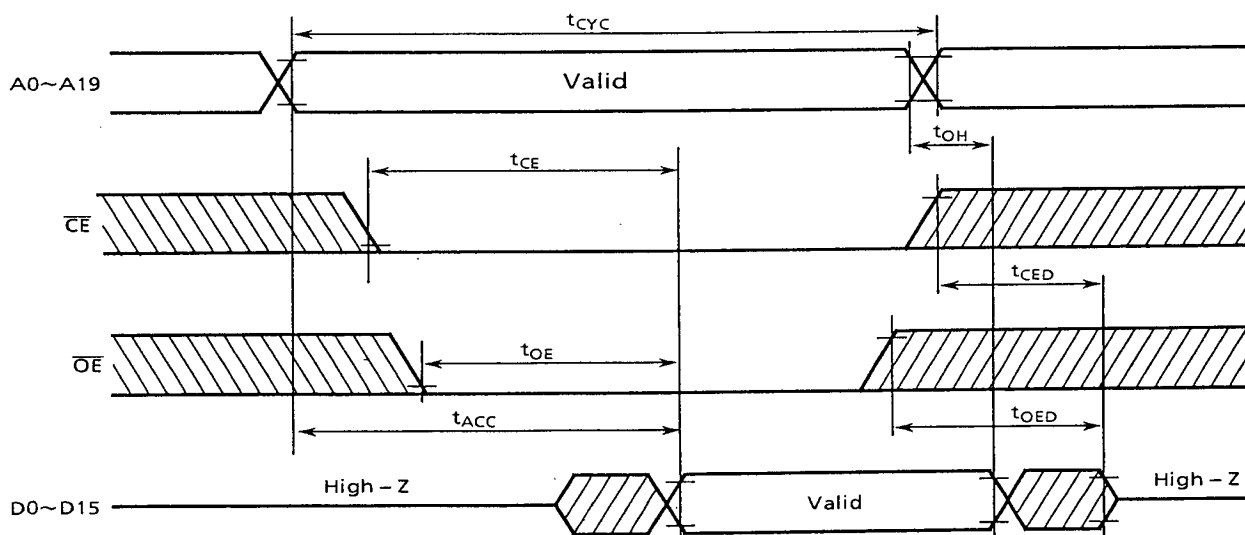
Timing Measurement Reference Levels Input : 0.8V, 2.2V

Output : 0.8V, 2.0V

Input Rise and Fall Time : 5ns

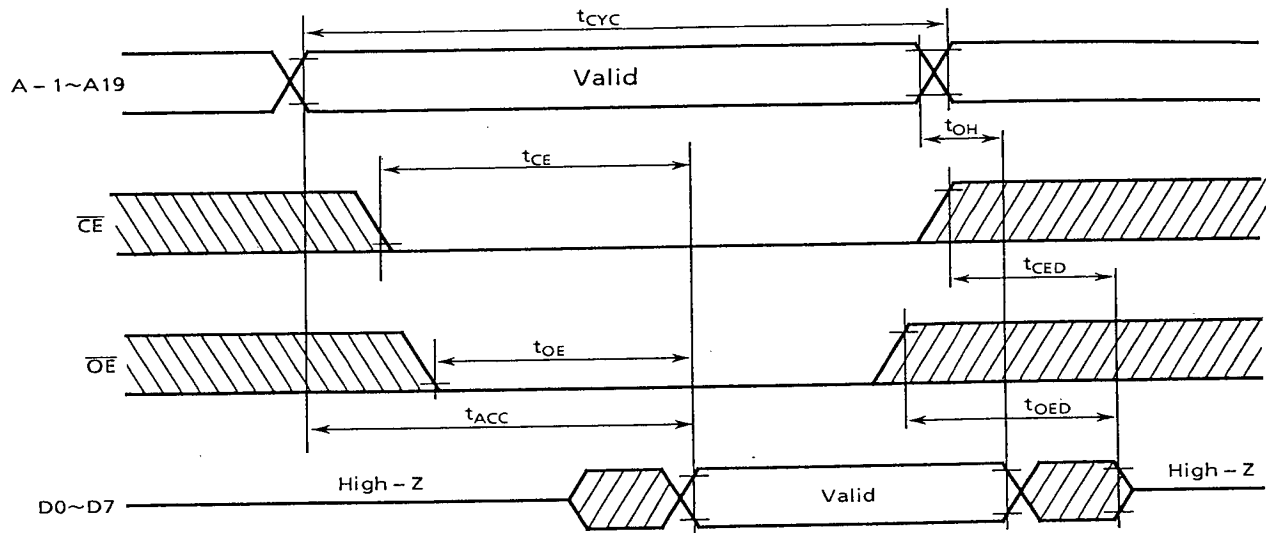
TIMING WAVEFORMS

WORD - WIDE READ MODE



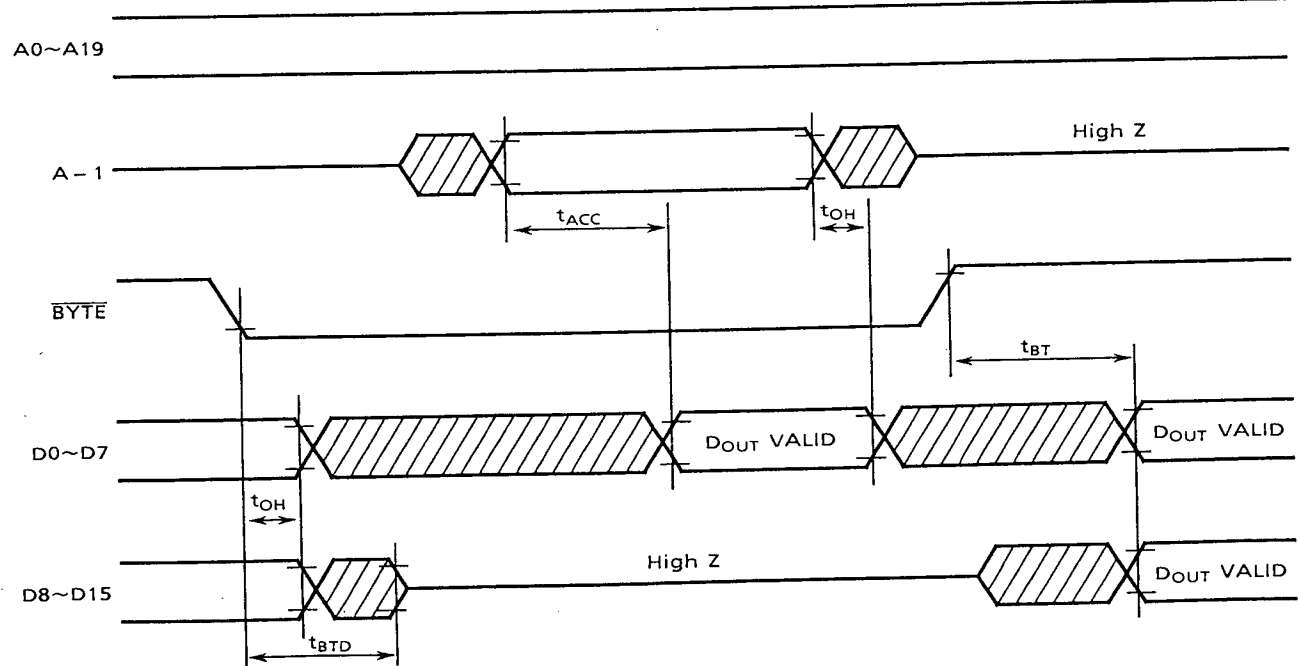
Note: $\overline{\text{BYTE}} = V_{IH}$

BYTE - WIDE READ MODE



Note: $\overline{BYTE} = V_{IL}$

BYTE TRANSITION



Note: $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$

TC5316210BP/BF/BFT

TENTATIVE

16M BIT (1M WORD × 16 BIT / 2M WORD × 8BIT) CMOS MASK ROM

DESCRIPTION

The TC5316210BP/BF/BFT is a 16,777,216 bits read only memory organized as 1,048,576 words by 16 bits when $\overline{\text{BYTE}}$ is logical high, and is organized as 2,097,152 words by 8 bits when $\overline{\text{BYTE}}$ is logical low.

The TC5316210BP/BF/BFT is most suitable for the program memory, data memory, and character generator.

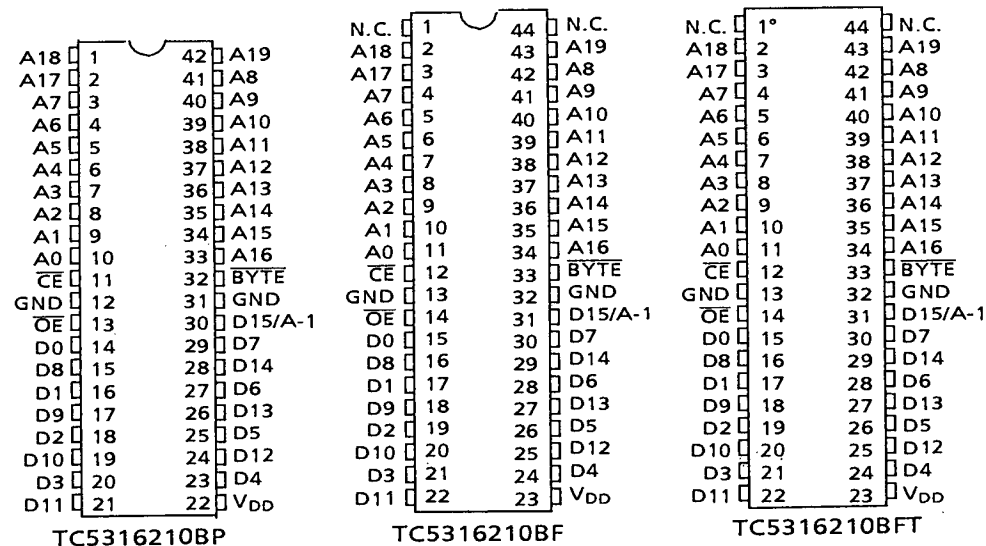
Page read mode allows two to eight words of data to be read fast in the same page. $\overline{\text{CE}}$ and (A3...A19) must not change. Page access is 60ns.

The TC5316210BP/BF/BFT is packaged in a standard 600mil 42pin DIP, 600mil 44 pin SOP or 400mil 44pin TYPE II TSOP.

FEATURES

- Single 5V Power Supply
- Access Time (Normal mode): 150ns (Max.)
- (Page Access mode): 60ns (Max.)
- Power Dissipation
 - Operating Current : 150mA (Max.)
 - Standby Current : 1mA (Max.)
- Fully Static Operation
- All Inputs and Outputs : TTL Compatible
- Three State Outputs
- TC5316210BP : DIP42-P-600
- TC5316210BF : SOP44-P-600
- TC5316210BFT : TSOP44-P-400

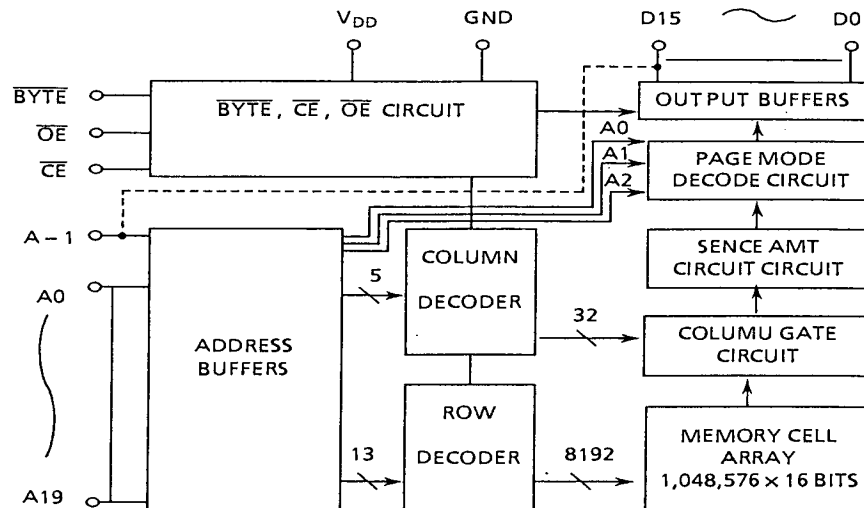
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A19	Address inputs
D0~D14	Data Outputs
$\overline{\text{CE}}$	Chip Enable Input
$\overline{\text{OE}}$	Output Enable Input
D15/A-1	Data Output/Addrss Input
$\overline{\text{BYTE}}$	Word, Byte selection Input
VDD	Power Supply
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MODE SELECTION

MODE	$\overline{CE}$	$\overline{OE}$	BYTE	D0 - D7	D8 - D14	D15 / A - 1	Power
Read (16 Bit)	L	L	H	Data Out			Active
Read (8 Bit)	L	L	L	Data Out (Lower 8bit)	High Impedance	L	Active
Read (8 Bit)	L	L	L	Data Out (Upper 8bit)	High Impedance	H	Active
Output Deselect	L	H	*	High Impedance			Active
Standby	H	*	*	High Impedance			Standby

H : V_{IH} L : V_{IL} * : V_{IH} or V_{IL}

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	- 0.5~7.0	V
V_{IN}	Input Voltage	- 0.5~ V_{DD}	V
V_{OUT}	Output Voltage	0~ V_{DD}	V
P_D	Power Dissipation	1.0 / 0.6*	W
T_{STG}	Storage Temperature	- 55~150	°C
T_{OPR}	Operating Temperature	0~70	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec

* SOP / TSOP

TC5316210BP/BF/BFT

D.C. OPREATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.2	—	V _{DD} + 0.3	V
V _{IL}	Input Low Voltage	- 0.3	—	0.8	V

D.C. and OPERATING CHARACTERISTICS (Ta = 0~70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I _{IL}	Input Leakage Current	V _{IN} = 0~V _{DD}	—	± 5.0	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0~V _{DD}	—	± 5.0	μA
I _{OH}	Output High Current	V _{OH} = 2.4V	- 1.0	—	mA
I _{OL}	Output Low Current	V _{OL} = 0.4V	2.0	—	mA
I _{DD51}	Standby Current	$\overline{CE} = V_{IH}$	—	5	mA
I _{DD52}		$\overline{CE} = V_{DD} - 0.2V$	—	1	mA
I _{DDO1}	D.C. Current	V _{IN} = V _{IH} /V _{IL}	—	100	mA
I _{DDO2}	Operating Current	V _{IN} = V _{IH} /V _{IL} , Normal (t _{CYCLE} = 150ns)	—	150	mA
I _{DDO3}		V _{IN} = V _{IH} /V _{IL} , Page (t _{CYCLE} = 60ns)	—	150	mA

CAPACITANCE f = 1MHz , Ta = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = 0V	—	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	—	12	pF

Note : This Parameter is periodically sampled and is not 100% tested.

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TC5316210BP/BF/BFT

A.C. CHARACTERISTICS (Ta = 0~70°C, VDD = 5V ± 10%)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t _{CYC}	Cycle Time	150	—	ns
t _{ACC}	Address Access Time	—	150	ns
t _{PAC}	Page Access Time	—	60	ns
t _{CE}	Chip Enable Access Time	—	150	ns
t _{BT}	BYTE Access Time	—	150	ns
t _{OE}	Output Enable Access Time	—	60	ns
t _{CEE}	Output Enable Time from $\overline{CE}$	0	—	ns
t _{OEE}	Output Enable Time from $\overline{OE}$	0	—	ns
t _{BTE}	Output Enable Time from BYTE	0	—	ns
t _{CED}	Output Disable Time from $\overline{CE}$	—	35	ns
t _{OED}	Output Disable Time from $\overline{OE}$	—	25	ns
t _{BDT}	Output Disable Time from BYTE	—	35	ns
t _{OH}	Output Hold Time(Normal)	10	—	ns
t _{POH}	Output Hold Time(Page)	5	—	ns

A.C. TEST CONDITIONS

Output Load

: 100pF + 1TTL

Input Levels

: 0.6V , 2.4V

Timing Measurement Reference Levels

Input : 0.8V , 2.2V

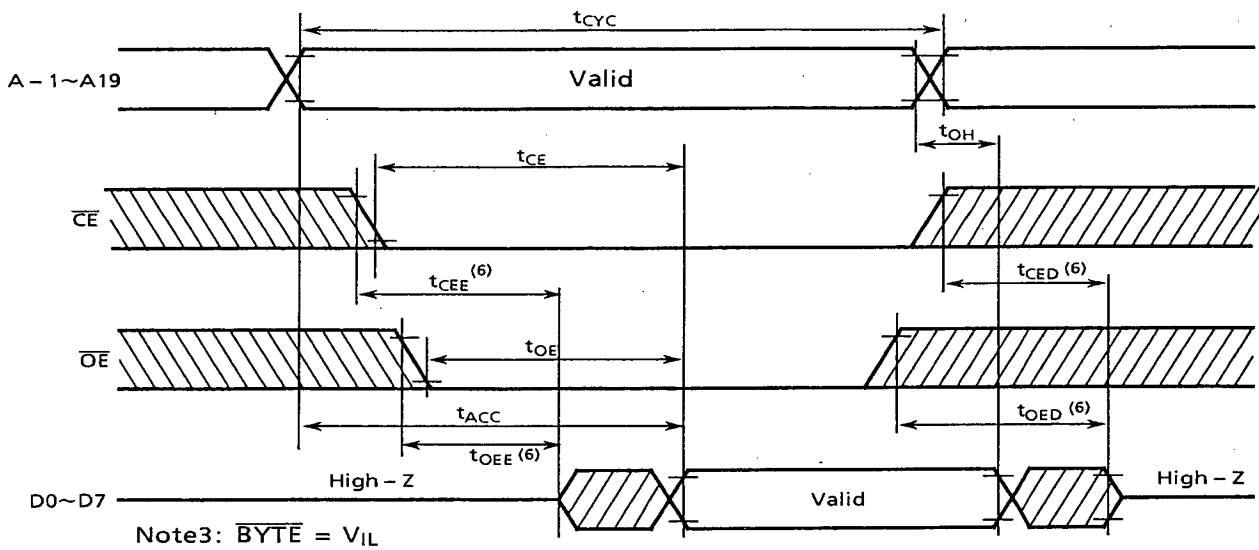
Output : 0.8V , 2.0V

Input Rise and Fall Time

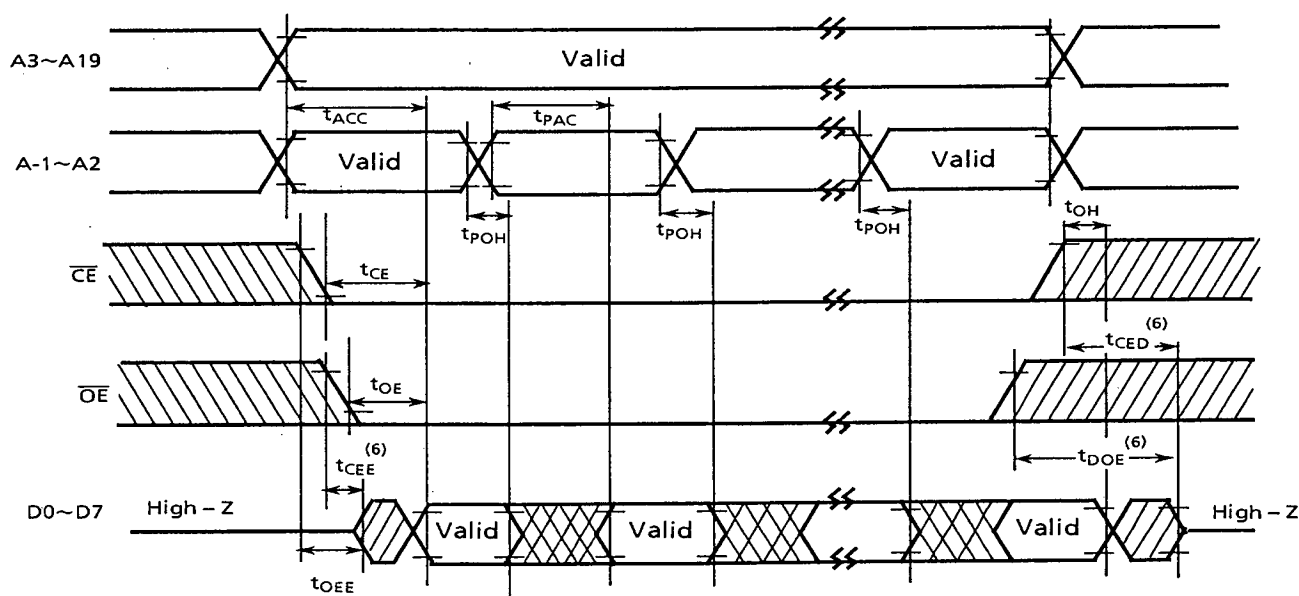
: 5ns

TC5316210BP/BF/BFT

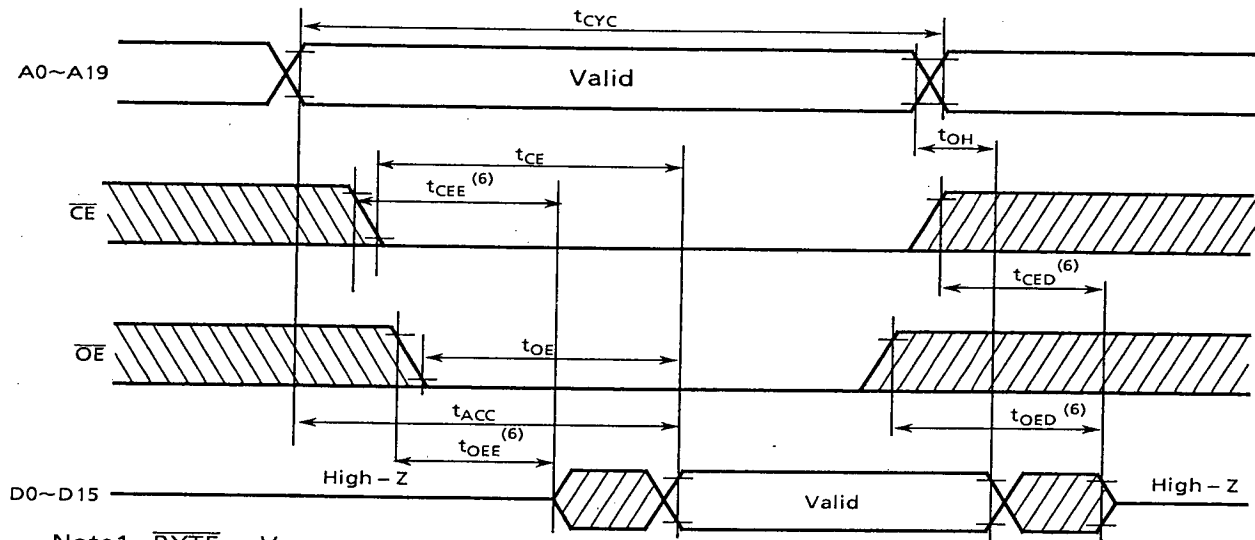
BYTE - WIDE READ MODE



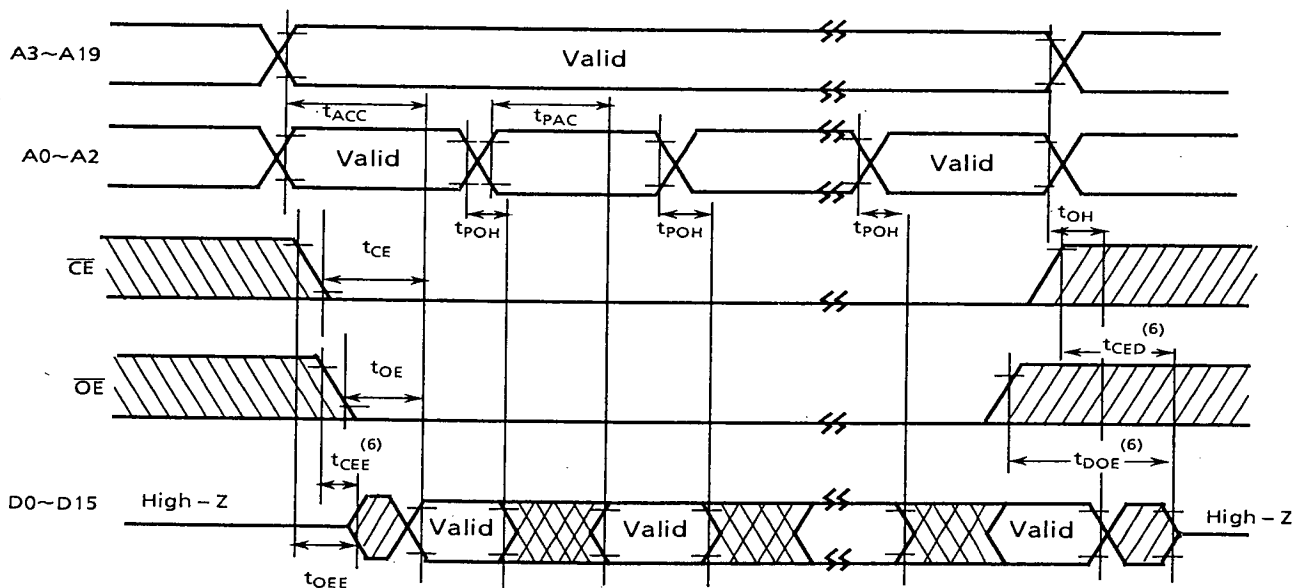
BYTE - WIDE PAGE READ MOAD



WORD - WIDE READ MODE

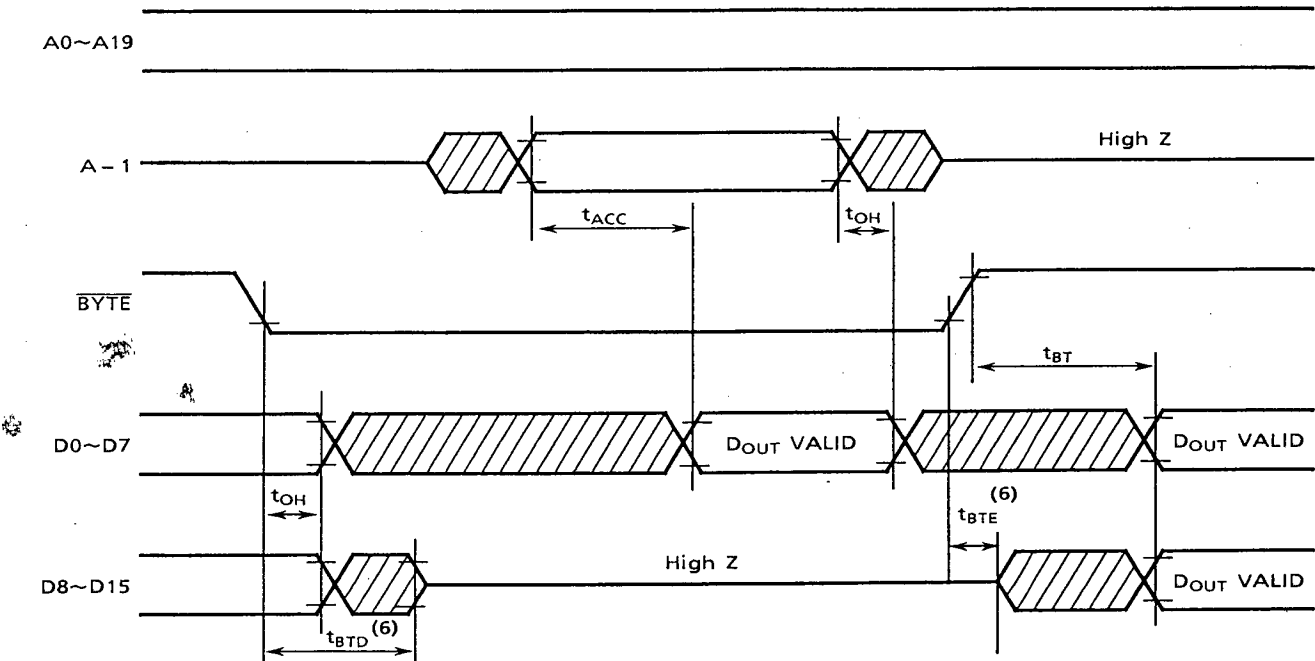


WORD - WIDE PAGE READ MOAD



TC5316210BP/BF/BFT

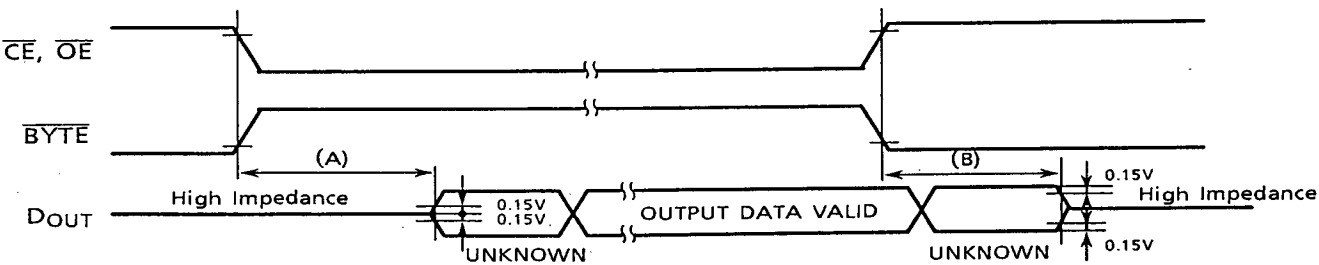
BYTE TRANSITION



Note 5: $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$

Note 6 : These parameters are specified

- (A) t_{CEE} , t_{OEE} , t_{BTE} Output Enable Time
- (B) t_{CED} , t_{OED} , t_{BTD} Output Disable Time



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