

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TOSHIBA CORPORATION, TOSHIBA AMERICA, INC.,
TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC.,
and TOSHIBA AMERICA INFORMATION SYSTEMS, INC.
Petitioner

v.

INTELLECTUAL VENTURES I LLC
Patent Owner

Case IPR2014-00113
Patent 6,058,045

Before KEVIN F. TURNER, TREVOR M. JEFFERSON,
and DAVID C. McKONE, *Administrative Patent Judges*.

JEFFERSON, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

A. Background

Toshiba Corporation, Toshiba America, Inc., Toshiba America Electronic Components, Inc., and Toshiba America Information Systems, Inc. Toshiba Corporation (collectively “Petitioner”) filed a Petition (Paper 1, “Pet.”) to institute an *inter partes* review of claims 1 and 4 of U.S. Patent No. 6,058,045 (Ex. 1001, “the ’045 patent”). *See* 35 U.S.C. § 311. Intellectual Ventures I LLC (“Patent Owner”) filed a Preliminary Response (Paper 10, “Prelim. Resp.”).

The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides as follows:

THRESHOLD.—The Director may not authorize an *inter partes* review to be instituted unless the Director determines that the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.

Upon consideration of the Petition and the Preliminary Response, we conclude that Petitioner has established a reasonable likelihood that it would prevail with respect to claims 1 and 4 of the ’045 patent. Accordingly, we institute an *inter partes* review of claims 1 and 4 of the ’045 patent.

B. Related Matters

Patent Owner has sued Petitioner for infringement of the ’045 patent in *Intellectual Ventures I LLC and Intellectual Ventures II LLC v. Toshiba Corporation, Toshiba America, Inc., Toshiba America Electronic Components, Inc., and Toshiba America Information Systems, Inc.*, No. 1:13-cv-00453 (D.

Del.), filed on March 20, 2013. Pet. 1; Paper 7 (Patent Owner's Mandatory Notices).

C. References Relied Upon

Petitioner relies upon the following prior art references:

Ex. 1005 Nakai US 5,297,029 Mar. 22, 1994
(filed Dec. 18, 1992)

1993 MOS Memory (Non-Volatile) Databook containing Datasheet for Toshiba's TC584000P/F/FT/TR CMOS NAND (Ex. 1009, "1993 Databook").

D. The Asserted Grounds

Petitioner contends that the challenged claims are unpatentable based on the following two grounds (Pet. 3-4):

Reference	Basis	Claims challenged
Nakai	§ 102(b)	1 and 4
1993 Databook	§ 102(b)	1 and 4

E. The '045 Patent

The '045 patent, titled "Serial Flash Memory," issued on May 2, 2000, and claims the benefit of a provisional application dated September 9, 1996. Ex. 1001, first page. The '045 patent discloses a "scaleable flash memory cell structure and method of manufacture that improves data retention, increases capacitive coupling and speed of operation, and improves reliability." *Id.* at 2:39-42. "The flash cell of the ['045 patent] permits implementation of arrays of flash memory cells that allow the designer to program and/or erase individual bytes of memory as well as blocks of memory." *Id.* at 2:44-46. Figure 4 of the '045 Patent shown below, provides the exemplary memory array circuit disclosed.

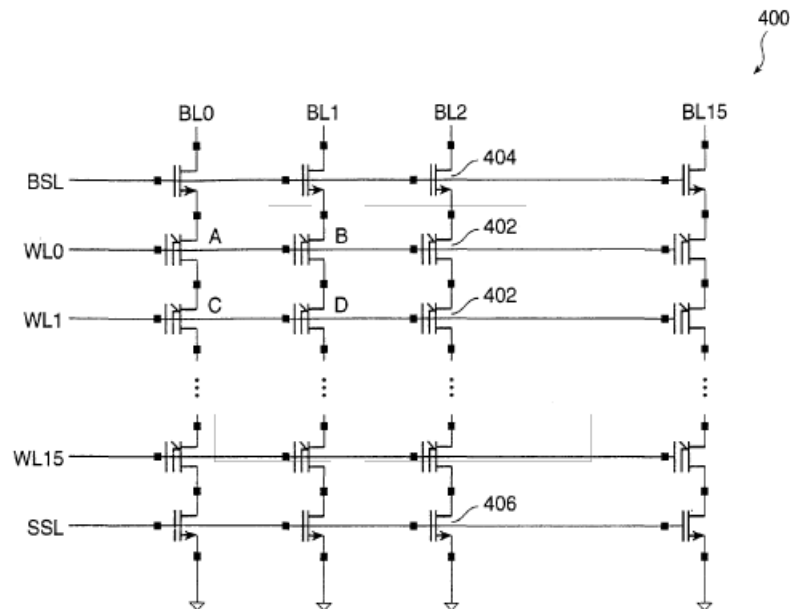


FIG. 4

Figure 4 depicts “a circuit schematic for an exemplary memory array made of flash cells.” *Id.* at 3:25-26. The disclosed memory array 400 in Figure 4 includes columns of serially connected flash memory cells located at the intersection of bit lines (BL0-BL15) and word lines (WL0-WL15). *Id.* at 6:22-28. Bit select control line (BSL) controls gate terminals of bit select transistors 404, which couple bit lines to memory cells. *Id.* at 30-31. Source select control line (SSL) controls gate terminals for source select transistors 406, which couple ground to memory cells. *Id.* at 31-32.

Table 1 of the '045 patent, reproduced below, provides a biasing scheme that discloses voltages that are applied to lines of the array to perform program, read, or erase operations for selected or unselected portions of the array.

TABLE I

Control Line	Erase	Program	Read	Condition
BSL	V _{cc}	V _{cc}	V _{cc}	Selected
SSL	V _{ss}	V _{ss}	V _{cc}	Selected
BLO	V _{cc}	V _{ss}	1.0–1.4V	Selected
BL1	V _{ss}	V _{cc}	0.5V	Unselected
WL0	V _{cc}	V _{cc}	V _{cc}	Unselected
WL1	–12 to –15V	15–20V	V _{ss}	Selected

Id. at 6:37-45. Table 1 provides an example of a biasing scheme for an individual cell, showing voltages applied to various control lines (i.e, V_{cc}, V_{ss}, etc.), and the desired function (erase, program, or read) for the selected or unselected portions of the array. *Id.* at 6:48-56.

F. Claims

Challenged claims 1 and 4 are reproduced below:

1. An array of flash memory cells comprising:
 - a plurality of columns of serially connected flash memory cells, each memory cell having a gate terminal;
 - a plurality of bit lines respectively coupled to drain side of said plurality of columns of memory cells via a respective plurality of bit line select transistors, said plurality of bit line select transistors having gate terminals coupled to a bit line select control line;
 - a plurality of word lines, each one coupling to a gate terminal of one memory cell in each of said plurality of columns to form rows of memory cells with common gate terminals; and
 - a plurality of source select transistors respectively coupling a source side of said plurality of columns of memory cells to a logic low voltage, and having

gate terminals coupled to a source select control line,

wherein, during programming:

a logic high voltage is applied to said bit line select control line to turn on bit line select transistors,

a logic low voltage is applied to source select control line to turn off source select transistors;

a logic low voltage is applied to a selected bit line while a logic high voltage is applied to unselected bit lines, and

a logic high voltage is applied to unselected word lines, while a boosted positive voltage is applied to a selected word line.

4. A method of operating a flash memory device wherein programming memory cells is accomplished by the steps of:

applying a logic high voltage to a bit line select control line to turn on bit line select transistors,

applying a logic low voltage to a source select control line to turn off source select transistors;

applying a logic low voltage to a selected bit line while a logic high voltage is applied to unselected bit lines, and

applying a logic high voltage to unselected word lines, while a boosted positive voltage is applied to a selected word line.

II. ANALYSIS

A. Claim Construction

We determine the meaning of the claims as the first step of our analysis. The Board interprets claims using the broadest reasonable construction. *See* 37 C.F.R. § 42.100(b); Office Patent Trial Practice Guide, 77 Fed. Reg. 48756, 48766 (Aug. 14, 2012). Claim terms generally are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). If an inventor acts as his or her own lexicographer, the definition must be set forth in the specification with reasonable clarity, deliberateness, and precision. *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1249 (Fed. Cir. 1998).

Petitioner asserts that claim terms should be given their ordinary and customary meanings, consistent with the disclosure, as understood by a person of ordinary skill in the art. Pet. 9. Accordingly, Petitioner offers constructions for “logic low voltage” and “logic high voltage,” “boosted positive voltage,” “selected bit line” and “unselected bit line,” and “selected word line” and “unselected word line.” Pet. 9-12. Patent Owner provides no construction for any of the terms identified by Petitioner and no argument regarding claim construction. We address Petitioner’s proposed claim constructions below.

1. “logic low voltage” (claims 1 and 4)

We agree with Petitioner that the broadest reasonable interpretation of logic low voltage is a “low voltage such as ground or Vss.” Pet. 9. The term “logic low voltage” only appears in the ’045 patent claims. The ’045 patent specification states that a selected bit line is programmed by grounding it at voltage Vss.

Ex. 1001, 7:29; 6:37-45. In addition, the '045 patent specification describes memory cell programming as occurring when the source select transistors couple memory cells 402 to ground (or Vss). *Id.* at 6:29-30. Accordingly, on this record, we construe “logic low voltage” as a low voltage such as ground or Vss.

2. *“logic high voltage” (claims 1 and 4)*

We agree with Petitioner that logic high voltage means “a positive voltage higher than logic low voltage, such as Vcc.” Pet. 10. The term “logic high voltage” is used only in the claims of the '045 patent. Petitioner’s proposed construction is consistent with the specification that states voltage Vcc is applied to bit select control line (BSL), the unselected bit line, and the unselected word line during programming. *Id.* at 6:37-45; 7:26-40; Ex. 1006 ¶ 17. Thus, on this record, we are persuaded that “logic high voltage” is construed as a positive voltage higher than logic low voltage, such as Vcc.

3. *“boosted positive voltage” (claims 1 and 4)*

Petitioner contends that “boosted positive voltage” is “a positive voltage higher than the logic high voltage.” Pet. 10. This term only appears in the '045 patent claims. The '045 patent specification states that “applying a high voltage (e.g., 15 to 20 V) on the selected word line (WL1)” is used to program a memory cell. Ex. 1001, 7:26-40. Based on the record, we agree with Petitioner and conclude that “boosted positive voltage” is a positive voltage higher than logic high voltage.

4. *“selected bit line” and “unselected bit line” (claims 1 and 4)*

Petitioner proposes that “selected bit line” is the bit line connected to the column of memory cells containing the memory cell to be operated on, and

“unselected bit line[s]” are the bit lines connected to the columns of memory cells not containing the memory cell to be operated on. Pet. 11-12.

We agree with Petitioner. The '045 patent specification describes programming operations referring to selected bit lines and unselected bit lines as receiving different voltages. Ex. 1001, 7:27-30. In addition, these selected and unselected bit lines are described by lines on the array of memory cells shown in Figure 4. *Id.* at 7:27-34. Thus, on this record, we are persuaded that the broadest reasonable interpretation of “selected bit line,” in light of the specification, is the bit line connected to the column of memory cells containing the memory cell to be operated on. Similarly, the broadest reasonable interpretation of “unselected bit lines,” in light of the specification, is bit lines connected to the columns of memory cells not containing the memory cell to be operated on.

5. *“selected word line” and “unselected word line” (claims 1 and 4)*

Petitioner proposes construing “selected word line” as the word line connected to the row of memory cells containing the memory cell to be operated on, and “unselected word lines” as “the word lines connected to the rows of memory cells not containing the memory cell to be operated on.” Pet. 12. We agree The '045 specification describes selected and unselected word lines by reference to Figure 4, based on the voltages that are applied to the word lines shown in Figure 4. Ex. 1001, 7:27-37. Accordingly, on this record, we are persuaded that “selected word line” means a word line connected to the row of memory cells. We are persuaded also that “unselected word line” means the word lines connected to the rows of memory cells not containing the memory cell to be operated on.

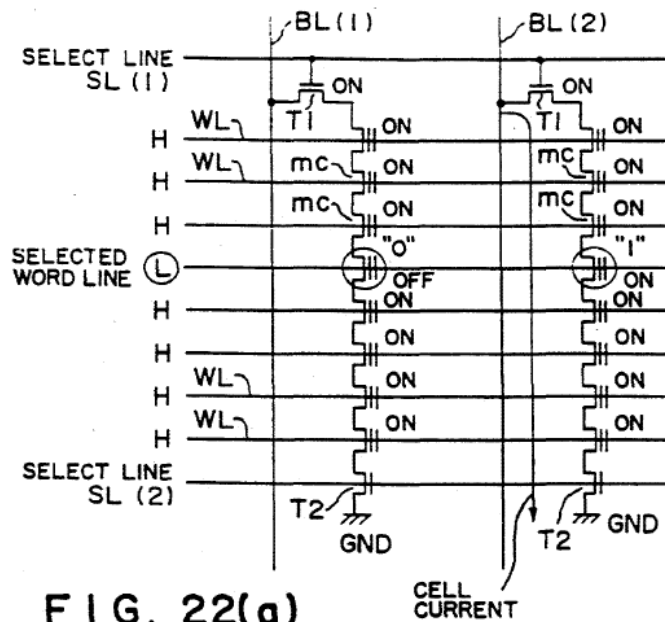
B. Asserted Grounds of Unpatentability

1. Anticipation by Nakai

Petitioner contends that Nakai anticipates claims 1 and 4. Pet. 13-16. Petitioner relies on the Declaration of Robert J. Murphy (Ex. 1006) (“Murphy declaration”) and provides detailed claim charts showing the claim limitations and the corresponding disclosure in Nakai (Pet. 17-29).

a. Nakai (Ex. 1005)

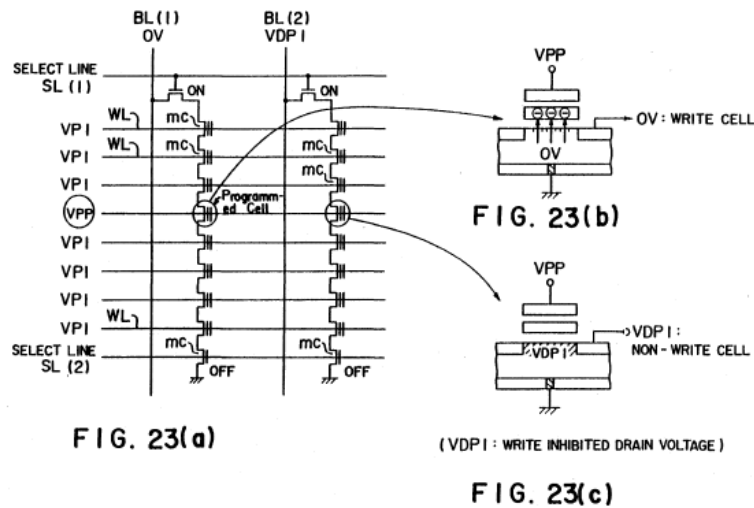
Nakai describes a semiconductor memory device that is a NAND type EEPROM arranged as an array. Ex. 1005, 1:20-26, Figs. 22(a), 25(a), and 26. Nakai describes selecting a programmable memory cell within the array for read, write, and erase operations. *Id.* at 1:10-15, 1:46; 2:10. Figure 22(a), shown below, illustrates the structure of the array memory cells. *Id.* at 1:20-23, 6:65-66.



“Fig[ure] 22(a) shows the structure of two NAND bundles each having eight memory cells MC of a floating gate structure and connected between a bit line and a source.” *Id.* at 1:2-23. Figure 22(a) shows select lines (SL), word lines (WL), bit

lines (BL) and memory cells (MC). By setting select voltages to high or low levels at select lines and word lines, data in the selected memory cell can be read. *Id.* at 24-45.

Similarly, Figures 23(a)-(c), shown below, depict a write operation for the memory cells of Figure 22(a). *Id.* at 1:46-47; 6:67-68.



Figures 23(a)-(c) show a high voltage V_{pp} of about 20 V applied in a row to select a gate (Fig. 23(b) and (c) showing V_{pp}) and intermediate voltage V_{pi} of above 10 V applied to the remaining seven memory cells for unselected gates. *Id.* at 1:46-52. When the bit lines are set to specified voltages, write operations are performed at the selected write line (*see* Fig. 23(b) showing write cell at 0 V) and write operations are not performed at the non-write cells (*see* Fig. 23(c) showing non-write cell at VDP).

Figure 25(a), reproduced below, shows the operation mode of a NAND structure semiconductor memory. *Id.* at 2:24-26.

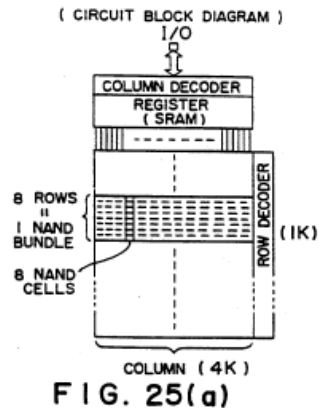


Figure 25(a) shows the semiconductor memory array laid out in bundles where “bit lines are laid out in the column direction, and 128 NAND bundles [equaling] 1024 word lines are laid out in the row direction.” *Id.* at 2:25-31.

b. Analysis

Petitioner contends that Nakai anticipates claims 1 and 4. Pet. 13-16. In support of its contentions, Petitioner provides a detailed claim chart with citations to Nakai and corresponding references to each limitation of claims 1 and 4. Pet. 16-29. Petitioner also cites the Murphy Declaration in support of what Nakai discloses to one of ordinary skill in the art. *See* Pet. 17-29.

With respect to the “flash memory” limitations of claims 1 and 4, Petitioner cites the Murphy declaration in support of the contention that one of ordinary skill in the art would have understood the cell arrays of NAND type EEPROMs disclosed in Nakai to be flash memory cells as recited in claim 1. Pet 17 (citing Ex. 1006 ¶ 22). With respect to the “array of flash memory cells” limitation of claim 1 regarding the structure of bit lines, word lines, and source select transistors, Petitioner shows that Figure 4 of the '045 patent and Figure 22(a) of Nakai are the same, showing an array configuration of gates or cells with select, bit and word lines. Pet. 14.

Petitioner also provides evidence that the programming voltages described in Nakai and Figure 23(a) are the same selected and unselected lines and voltages claimed in the “programming” limitations of claims 1 and 4. Pet. 14-15. Petitioner also relies on the Murphy declaration to show that one of ordinary skill in the art would understand Nakai to disclose applying a logic low voltage to a selected bit line as recited in claims 1 and 4 (“a logic low voltage is applied to a selected bit line while a logic high voltage is applied to unselected bit lines”). Petitioner also provides evidence that Nakai discloses that “a logic high voltage is applied to unselected word lines, while a boosted positive voltage is applied to a selected word line” in the write operation described and shown in Figure 23(a). Pet. 27-28; *see* Ex. 1005, 1:45-2:9. Finally, Petitioner provides a chart showing the correspondence between the programming voltages disclosed in Nakai and the programming voltages recited in claims 1 and 4. Pet. 16.

Patent Owner makes no substantive arguments regarding the disclosures of Nakai. Prelim. Resp. 2-11. Instead, Patent Owner argues that the 1993 Databook and Nakai are virtually identical references, containing identical descriptions. Prelim. Resp. 5-11 (comparing 11993 Databook and Nakai). Patent Owner argues that Petitioner is not entitled to a trial on both grounds and, therefore, we should deny at least one of the Petitioner’s proposed grounds of unpatentability as redundant. *See id.* Because the 1993 Databook was published before Nakai issued as a patent, Patent Owner contends that we should select the ground with the earliest publication date and deny the remaining ground as redundant. Prelim. Resp. 11 (citing *Liberty Mut. Ins. Co. v. Progressive Cas. Ins. Co.*, CBM2012-00003 (Paper No. 7), as an example of denying in part based on redundancy).

We disagree with Patent Owner that our prior case limits us to selecting the ground with the earliest publication date. Instead, *Liberty Mutual* establishes that,

when multiple grounds are presented in a redundant manner in a Petition, we have the discretion to deny the Petition as to redundant grounds. *See Liberty Mut. Ins. Co. v. Progressive Cas. Ins. Co.*, CBM2012-00003, Paper 7 at 6 (PTAB Oct. 25, 2012) (ordering Petitioner to select one of three groups of obviousness grounds and denying those two grounds not selected).

We find that Petitioner has shown that the programming modes described in Nakai and corresponding to Figure 23(a) disclose the limitations of claims 1 and 4 of the '045 patent. Thus, Petitioner has provided sufficient evidence that the memory array configuration of claim 1 and the programming limitations of claims 1 and 4 are disclosed in Nakai.

Based on the foregoing, Petitioner has shown a reasonable likelihood that it will prevail as to claims 1 and 4 as anticipated by Nakai.

2. *Anticipation by 1993 Databook (Ex. 1009)*

Petitioner asserts that the 1993 Databook anticipates claims 1 and 4 of the '045 patent. Pet 30-44. Petitioner has not explained why the 1993 Databook ground is better in any respects than the ground on which we institute review, discussed above. *See* Prelim. Resp. 5-11. Accordingly, Petitioner's ground alleging anticipation of claims 1 and 4 by 1993 Databook is denied as redundant given the determination above that there is a reasonable likelihood that the challenged claims are unpatentable based on Nakai.

III. CONCLUSION

We institute an *inter partes* review of claims 1 and 4 of the '045 patent based on 35 U.S.C. § 102(b) as anticipated by Nakai.

IV. ORDER

For the reasons given, it is

ORDERED that *inter partes* review is instituted as to claims 1 and 4 on the grounds listed in the Conclusion, above;

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(a), *inter partes* review of the '045 patent is hereby instituted commencing on the entry date of this Order, and pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial;

FURTHER ORDERED that all grounds not listed in the Conclusion are *denied*, and no ground other than those specifically granted above is authorized for the *inter partes* review as to claims 1 and 4 of the '045 patent.

Case IPR2014-00113

Patent 6,058,045

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