

UNITED STATES PATENT AND TRADEMARK OFFICE

---

BEFORE THE PATENT TRIAL AND APPEAL BOARD

---

TOSHIBA CORPORATION

Petitioner

v.

INTELLECTUAL VENTURES I LLC

Patent Owner

---

Case IPR2014-00113  
U.S. Patent No. 6,058,045

---

**PATENT OWNER'S RESPONSE TO PETITION**

Mail Stop PATENT BOARD  
Patent Trial and Appeal Board  
U.S. Patent & Trademark Office  
P.O. Box 1450  
Alexandria, VA 22313-1450

## TABLE OF CONTENTS

TABLE OF AUTHORITIES .....	ii
LIST OF EXHIBITS .....	iii
INTRODUCTION .....	1
I. Overview of the Claimed Invention .....	1
A. Basic Flash Memory Array Programming Operation .....	1
B. The Claimed Program Mode Requires Particular Voltages .....	4
II. Claim Construction for the Claimed Programming Voltages .....	7
A. Toshiba Provides No Persuasive Support for Its Constructions or Analysis .....	8
B. Toshiba’s Construction of “Logic High Voltage” Is Incorrect .....	10
C. Properly Construed, the Upper Boundary for Logic High Voltage Is Vcc .....	12
III. When the Proper Claim Construction for “Logic High Voltage” Is Applied, Nakai Does Not Anticipate Claims 1 or 4 of the ’045 Patent .....	15
A. Claims 1 and 4 Require the Application of Logic High Voltage to Certain Nodes of the Memory Array During Programming .....	16
B. Nakai Does Not Anticipate Because Its Alleged “Logic High Voltages” Are “Boosted Positive Voltages” .....	17
1. Application of Properly Construed Claims to Nakai .....	17
2. Toshiba’s Flawed Application of Its Improper Proposed Claim Constructions to Nakai Cannot Stand .....	20
C. Advantages of the Claimed Invention over Nakai’s Programming Scheme .....	22
IV. Conclusion .....	24
CERTIFICATION OF SERVICE .....	25

## TABLE OF AUTHORITIES

### Cases

<i>Karsten Mfg. Corp. v. Cleveland Golf Co.</i> , 242 F.3d 1376, 1383 (Fed. Cir. 2001) .....	15
<i>Verdegaal Bros. v. Union Oil Co. of California</i> , 814 F.2d 628, 631 (Fed. Cir. 1987) .....	15

## LIST OF EXHIBITS

<u>IV Exhibit No.</u>	<u>Document Description</u>
2001	Declaration of Louis J. Morales
2002	Declaration of John E. Berg
2003	Transcript of Deposition of Robert J. Murphy on June 17, 2014
2004	Table Mapping Exhibits from Deposition of Robert J. Murphy to Exhibits/Papers in IPR2014-00113
2005	Weste, Neil H.E. <i>et al.</i> , “Principles of CMS VLSI Design, A Systems Perspective,” Second Edition, 1994.
2006	Thomas, Roland E., <i>et al.</i> , “The Analysis and Design of Linear Circuits,” 1998.
2007	“Oral History of George Perlegos,” Jeff Katz, Interviewer, 2013.
2008	“FLASH Memories,” accessed on July 9, 2014, accessed at <a href="http://noel.feld.cvut.cz/hw/amd/flash_.htm">http://noel.feld.cvut.cz/hw/amd/flash_.htm</a> , 1999.
2009	D’Arrigo, Sebastiano, <i>et al.</i> , “A 5V-Only 256k Bit CMOS Flash EEPROM,” 1989.
2010	Sanvido, Marco A. A., <i>et al.</i> , “NAND Flash Memory and Its Role in Storage Architectures,” 2008.
2011	Chen, IH-Chin, <i>et al.</i> , “Electrical Breakdown in Thin Gate and Tunneling Oxides,” 1985.
2012	Kang, Sung-Mo, <i>et al.</i> , “CMOS Digital Integrated Circuits, Analysis and Design,” 1996.
2013	Haznedar, Haldun, “Digital Microelectronics,” 1991.

## INTRODUCTION

The challenged claims of U.S. Patent 6,058,045 (“’045 patent”) relate to programming flash memory cells using relatively low voltages. This confers advantages over existing programming techniques, including improved reliability, reduced power consumption, and an overall reduced chip footprint. These advantages are particularly important because they support the ongoing goal of making memory chips physically smaller, which reduces their cost, and denser, which increases their memory capacity and economic value. By contrast, the identified Nakai reference<sup>1</sup> uses traditionally higher voltages during programming. Specifically, Nakai’s programming technique applies various high “boosted positive voltages” to certain nodes of its memory array, while the ’045 patent claims dictate lower “logic high voltages” at those nodes. Because Nakai discloses only this old programming technique that is dependent on the use of boosted voltages, Nakai does not anticipate either of the challenged claims of the ’045 patent.

### **I. Overview of the Claimed Invention**

#### **A. Basic Flash Memory Array Programming Operation**

Flash memory devices include various modes of operation, including program, erase and read. (Ex. 1001, ’045 patent, 6:20-23.) These modes of

---

<sup>1</sup> Ex. 1005, U.S. Patent No. 5,297,029.

operation are implemented by applying different voltages to nodes of the memory array. Independent claims 1 and 4—the only challenged claims in this *inter partes* review—are directed to the program mode of operation.

In the program mode, the goal is to store information in a memory cell. (*See id.*, 6:17-20.) In the memory array described in the '045 patent specification, information is stored by tunneling electrons onto the floating-gates of the selected memory cells. (*See id.*) For example, “boosted positive voltages” (15-20 V) and “logic low voltages” (V<sub>ss</sub> or 0V) are applied to control gates and drain terminals of selected memory cells, respectively. (*See id.*, 7:27-40.) This forms a strong electric field between the control gate and the channel region of the floating-gate transistor of the selected memory cell, which then induces the tunneling of electrons into the memory cell structure. (*See id.*, 6:17-20.) The presence of the trapped electrons, in turn, increases the turn-on voltage of the memory cell. (*See id.*) It is this increased turn-on voltage that represents the information stored in the memory cell. (*See id.*; *see also* Ex. 2001, Morales Dec., ¶¶ 18-20.)

The '045 patent discloses a novel tunnel oxide window structure that is consistent with the application of lower voltages (e.g., “logic high voltages”) to the control terminals of flash memory cells during program:

Broadly, the flash cell according to the present invention limits the tunnel oxide to a window having dimensions at the minimum feature size located over the drain side of the

transistor. The tunnel oxide window is separated from the field oxide and has no edges abutting field oxide. Thus, leakage due to defects caused by the field edge is eliminated, resulting in higher data retention rates for the cell. The reduced dimensions of the tunnel oxide region significantly increase the gate capacitive coupling ratio of the cell. ***The higher gate coupling allows the cell to be smaller yet operate at higher speed (larger read current). The higher coupling ratio also reduces the level of the maximum required voltage resulting in higher endurance.*** (Ex. 1001, '045 patent, 2:50-62, emphasis added.)

In addition, lowering the voltages applied to the control terminals of the flash memory cells improves overall tunnel oxide reliability. (See Ex. 2002, Berg Dec., ¶ 69 (stating that “lowering the voltage across the tunnel oxide by ~0.8V increases the time to breakdown by an order of magnitude”).)

An important part of programming the memory cell also includes ensuring that unselected memory cells are not programmed. Preventing unintended programming of unselected memory cells is accomplished, as recited in claims 1 and 4, by applying “logic high voltages” to the unselected word lines, unselected bit lines, and the bit select control line. (See Ex. 2001, Morales Dec., ¶ 22.) This arrangement results in the unselected memory cells having a smaller electric field between their respective control gates and channel regions than the selected memory cell. (See *id.*, ¶ 23.) The smaller electric field in the unselected memory cells is not strong enough to induce tunneling in these devices. (See *id.*) This

prevents programming of the unselected memory cells. (*See id.*) This is referred to as “program inhibit.” (*See id.*)

**B. The Claimed Program Mode Requires Particular Voltages**

The claimed program mode applies three different voltages to store information on selected memory cells, and to ensure that unselected memory cells are not programmed. The claims recite (1) “logic low voltage,” (2) “logic high voltage” and (3) “boosted positive voltage.” (*See* Ex. 2001, Morales Dec., ¶¶ 18-21; *see* Ex. 2002, Berg Dec., ¶¶ 24-25.)

Independent claim 1 is directed to an array of flash memory cells and the voltages applied to the array during a program mode of operation. (*See id.*) Claim 1 first recites the structural aspects of the array. The array includes a plurality of columns of serially connected flash memory cells, a plurality of bit lines with a respective plurality of bit line select transistors, a plurality of word lines, and a plurality of source select transistors. (*See* Ex. 1001, '045 patent, claim 1, 8:23-39.)

Claim 1 requires application of particular voltages during a program mode of operation. (*See id.*, claim 1, 8:40-50.) The relevant portion of claim 1 that relates to these particular voltages recites:

1. An array of flash memory cells comprising:  
[the claimed array structure]  
wherein, during programming:



a logic high voltage is applied to said bit line select control line to turn on bit line select transistors,

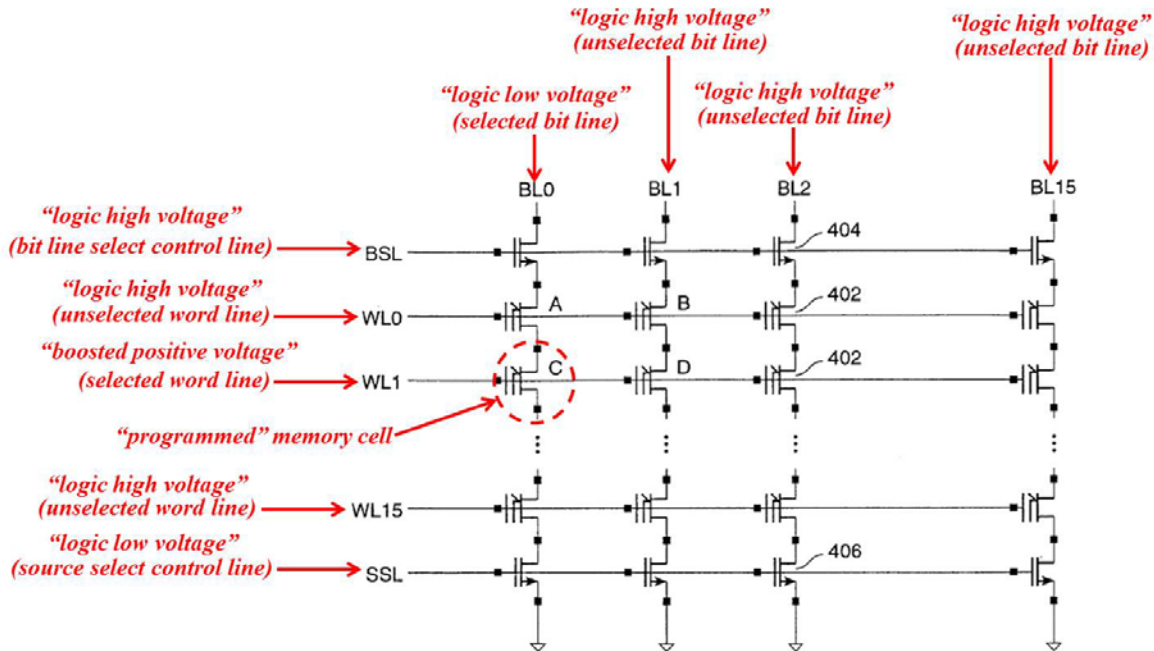
a logic low voltage is applied to source select control line to turn off source select transistors;

a logic low voltage is applied to a selected bit line while a logic high voltage is applied to unselected bit lines, and

a logic high voltage is applied to unselected word lines, while a boosted positive voltage is applied to a selected word line.

The relevant portion of independent method claim 4 is substantially similar. Accordingly, the arguments made with respect to claim 1 are equally applicable to independent claim 4.

Referring to FIG. 4 of the '045 patent, if bit line BL1 is a selected bit line and bit lines BL2-BL15 are unselected bit lines, and if word line WL1 is a selected word line and word lines WL0 and WL2-WL15 are unselected word lines, then the memory array in program mode looks like this (*see* Ex. 2001, Morales Dec., ¶¶ 18-21):



**FIG. 4 of the '045 Patent (Annotations in Red Italics)**

Table 1 of the '045 patent (6:36-45) shows exemplary applied voltages in program mode, which are reproduced in the table below along with the corresponding language from claim 1:

Table 1: Control Line	Table 1: Program Voltage	Table 1: Condition	Claim 1 Voltages
BSL	Vcc	Selected	"logic high voltage"
SSL	Vss	Selected	"logic low voltage"
BL0	Vss	Selected	"logic low voltage"
BL1	Vcc	Unselected	"logic high voltage"
WL0	Vcc	Unselected	"logic high voltage"
WL1	15-20V	Selected	"boosted positive voltage"

### Chart Comparing the Voltages of Table 1 with Claim 1

As shown above, the claims require a "boosted positive voltage" for the selected word line *only*. The unselected word lines, unselected bit lines, and the bit line select control line *do not require boosted positive voltages*, as was required in

conventional flash memories. (*See* Ex. 2001, Morales Dec., ¶ 32; *see* Ex. 2002, Berg. Dec., ¶¶ 55-58.) Instead of applying various boosted voltages, the '045 patent discloses a programming scheme where a lower voltage (*i.e.*, a “logic high voltage”) is applied to the unselected word lines, unselected bit lines, and the bit line select control line. (*See* Ex. 2002, Berg. Dec., ¶¶ 59-65.) By contrast, the Nakai reference requires multiple different boosted positive voltages on the unselected lines and on the bit line select transistors. (*See id.*) Thus Nakai does not anticipate either challenged claim.

## II. Claim Construction for the Claimed Programming Voltages

Claims 1 and 4 recite three different voltage terms relating to voltages applied to an array of flash memory cells during a program mode of operation: (1) a “logic low voltage,” (2) a “logic high voltage,” and (3) a “boosted positive voltage.” Toshiba proposed a construction for these voltages, which the Board provisionally adopted without material change. (*See* Paper 13, pp. 7-8.) The following table summarizes these preliminary constructions.

Claim Term	Board’s Preliminary Construction
“logic low voltage”	“a low voltage such as ground or Vss.” (Paper 13, pp. 7-8.)
“logic high voltage”	“a positive voltage higher than logic low voltage, such as Vcc.” (Paper 13, p. 8.)
“boosted positive voltage”	“a positive voltage higher than logic high voltage.” (Paper 13, p. 8.)

**A. Toshiba Provides No Persuasive Support for Its Constructions or Analysis**

Outside of the '045 patent specification itself, the only support Toshiba provided for its claim construction was the declaration of its technical expert, Robert Murphy. Toshiba and Mr. Murphy both agree that “[t]he '045 Patent relates to a flash memory cell structure and an array configuration of flash memory cells. More specifically, claims 1 and 4 of the '045 Patent are directed to the voltages used to program a specific array configuration of flash memory cells.” (Paper 1, p. 3; *see also* Ex. 1006, Murphy Dec., pp. 4-5.) And, more specifically, the '045 patent is directed to NAND flash memory. (*See* Ex. 1001, '045 patent at 7:37-40; *see* Ex. 2002, Berg Dec., ¶¶ 20 and 67.)

Because flash memory cells and NAND flash memory cells are the relevant art, Mr. Murphy is not qualified to opine on the technology of the '045 patent. Indeed, he is not even one of ordinary skill in the art in the field of flash memory technology, by his own admission.

Mr. Murphy provided a proposed level of ordinary skill in the art that includes a degree in electrical engineering<sup>2</sup> and work experience in the field of

---

<sup>2</sup> Mr. Murphy obtained both his bachelors and masters degrees, and much of his work experience, years before flash memory was invented in about 1984. (*See* Ex. 2003, Murphy Depo. Transcript, pp. 45-74.)

*non-volatile memory devices.* (See Ex. 1006, Murphy Dec., ¶ 9, emphasis added.)

But the field of non-volatile memory devices is too broad, because as Mr. Murphy admits, it would include such unrelated technologies as floppy disks, hard drives, and magnetic tape. (See Ex. 2003, Murphy Depo. Transcript, p. 18, ln. 18 - p. 20, ln. 17.) None of those non-volatile memory technologies are relevant to the '045 patent. (See *id.*) Mr. Murphy relied on this over-inclusive categorization for the simple reason that he is not one of ordinary skill in the art in the field of NAND flash memory, or even flash memory generally:

[Question:] Do you have any experience working with NAND flash?

[Mr. Murphy:] *No, I don't believe I do.*

(Ex. 2003, Murphy Depo. Transcript, p. 126, lns. 16-18, emphasis added.)

[Question:] So if the last clause, instead of saying “working in the field of non-volatile memory devices” read “working in the field of NAND flash memory devices,” would you be one of ordinary skill in the art or not?

. . .

[Mr. Murphy:] *I -- I don't have three years of relevant experience on NAND flash memory devices, so, no, I would not be.*

(*Id.*, p. 127, ln. 23 – p. 128, ln. 6, emphasis added.)

[Question:] If this definition, rather than saying as it does now,

“working in the field of non-volatile memory devices”

[Mr. Murphy:] Mm-hmm.

[Question:] -- said “working in the field of flash memory,”  
would you be one of skill in the art then?

[Mr. Murphy:] *I don't see that I would clear the hurdle if that was where the bar was set.* However, that would seem to me to be very narrow definition.

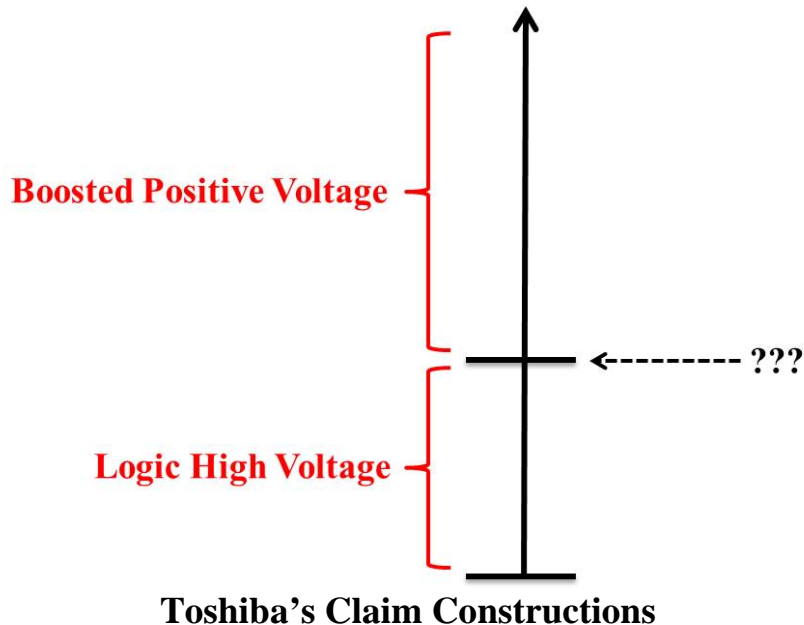
(*Id.*, p. 112, lns. 15-23, emphasis added.)

Accordingly, Toshiba provided no support for its constructions beyond that of a person without any NAND flash memory experience, who is admittedly not one of ordinary skill in the art under any reasonable definition of the art. Mr. Murphy's declaration should therefore be given little or no weight.

**B. Toshiba's Construction of “Logic High Voltage” Is Incorrect**

Toshiba's constructions are designed to read out of the claims the distinction between “logic high voltage” and “boosted positive voltage” because Nakai uses “boosted positive voltages” where the challenged claims require “logic high voltages.” Toshiba accomplishes this by defining the terms only relative to each other (“logic low” < “logic high” < “boosted positive”). But as a result, it is impossible to determine where one begins and the other ends. Indeed, when asked “[s]o those terms don't impart a limitation on the respective magnitudes of those voltages other than that they be in relative order?,” Mr. Murphy responded “I think that's correct, yes.” (Ex. 2003, Murphy Depo. Transcript, p. 168, lns. 10-13.)

Toshiba's proposed claim constructions, which the Board preliminarily adopted, can be viewed pictorially as follows:



As shown in the figure above, the preliminary constructions are imprecise because there is no clear demarcation between a “logic high voltage” and a “boosted positive voltage.”<sup>3</sup> (*See* Ex. 2002, Berg Dec., ¶¶ 27-30.) For example, with respect to the programming voltages shown above, if two or more different

---

<sup>3</sup> The preliminary constructions are also imprecise because there is not clear demarcation between “logic low voltage” and “logic high voltage.” (*See* Ex. 2002, Berg Dec., ¶ 26.) That imprecision, however, does not raise the same issues as the imprecision regarding the demarcation between “logic high voltage” and “boosted positive voltage” discussed herein. (*See* Ex. 2002, Berg Dec., ¶¶ 39-42 and 60-61.)

voltages are applied to BSL, BL1, and WL0 during programming, it is impossible to tell under Toshiba's construction which is a "logic high voltage," and which is a "boosted positive voltage."

But this is precisely how Nakai programs its memory array – using at least two different boosted positive voltages for unselected lines. Faced with this dilemma, Toshiba arbitrarily labels Nakai's voltages under its ambiguous definition to suit the needs of its invalidity argument. But claim constructions are intended to clarify claim scope, not render the scope impossible to ascertain

**C. Properly Construed, the Upper Boundary for Logic High Voltage Is Vcc**

The defect in the preliminary construction can be readily resolved by one of ordinary skill in the art reading the '045 patent. One of ordinary skill in the art would understand that a "logic high voltage" would be less than or equal to the nominal value of the memory array's power supply, or what one of skill in the art would recognize as "Vcc." (*See* Morales Dec., ¶¶ 25-33 and 39; *see* Berg Dec., ¶¶ 27-32.) So a proper construction of "logic high voltage" is "a positive voltage higher than logic low voltage *and less than or equal to the nominal value for Vcc.*" (*See id.*)

Toshiba and Mr. Murphy tacitly admit this in their proposed construction ("a positive voltage higher than logic low voltage, *such as Vcc*"). But they insert "such



as” to render the Vcc portion of their construction completely inoperative.<sup>4</sup> The memory devices disclosed in the ’045 patent (and also in Nakai) have a nominal power supply that is referred to as “Vcc,” as was common in art. (*See* Ex. 2001, Morales Dec., ¶¶ 24-33 and 39; *see* Ex. 2002, Berg. Dec., ¶¶ 21-23.) And boosted positive voltages are higher than the nominal value for Vcc. (*See id.*) The power supply voltage Vcc is thus the only principled and precise dividing line between a logic high voltage, and the higher voltages that are boosted over Vcc. (*See* Ex. 2001, Morales Dec., ¶¶ 24-33 and 39; *see* Ex. 2002, Berg. Dec., ¶¶ 33-44.)

The ’045 patent supports this construction. Table 1 shows that the “logic high voltage” is associated with values not higher than the power supply voltage Vcc. (’045 patent, Table 1.)

Nakai confirms this as well. For example, Nakai’s Fig. 20 illustrates a timing chart for Nakai’s memory device during a power-on reset operation. (*See* Ex. 2001, Morales Dec., ¶¶ 35-37.)

---

<sup>4</sup> When asked “[i]s the ‘such as Vcc’ in this construction also a nonlimiting example?,” Mr. Murphy responded “yes.” Also, when asked “[s]o neither of the ‘such as’ clauses limits the scope of those definitions?,” Mr. Murphy responded “I don’t believe that it does, no. It just gives an example.” (Ex. 2003, Murphy Depo. Transcript, p. 131, lns. 4-10.)

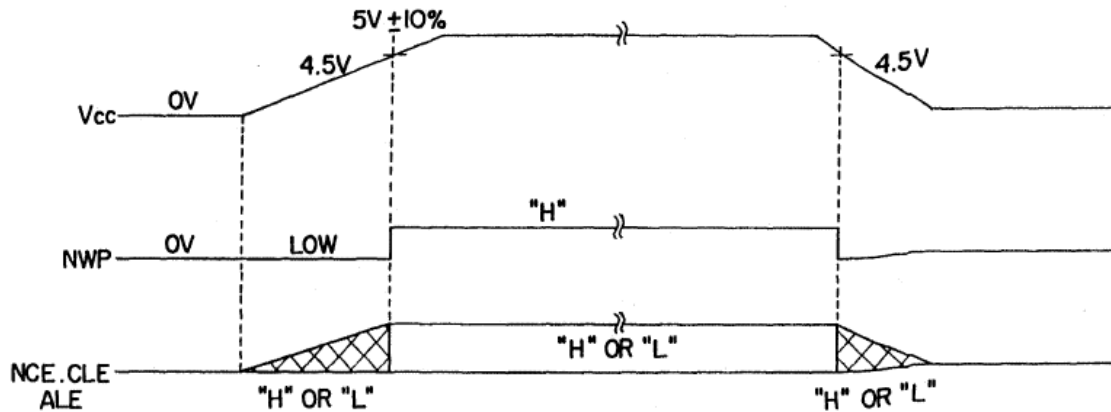


FIG. 20

As is common in integrated circuits, a power-on reset circuit prevents logic circuits from operating until the power supply voltage reaches the specified level at which a “logic high voltage” can be reliably produced by those logic circuits. (*See id.*)

During this operation, the nominal power supply voltage  $V_{cc}$  transitions from 0V to the memory device’s nominal operating voltage of 5V. (*See id.*) One of ordinary skill in the art would understand that Nakai’s memory device includes logic circuits,<sup>5</sup> that logic circuits may not function properly to produce logic high outputs until the primary positive power supply voltage reaches its specified operating range, and that the power-on reset operation is complete when  $V_{cc}$  reaches a level high enough for those logic circuits to reliably perform logic functions, i.e., to provide a logic high voltage to its logic circuits. (*See id.*)

---

<sup>5</sup> *See, e.g.,* Nakai’s Fig. 1 which shows logic circuitry including a command register, a command decoder, a row decoder and a column decoder.

Nakai's Vcc is its power-supply voltage and is the nominal voltage at which the logic circuits on Nakai's memory device produce a logic high voltage at their respective outputs. (*See id.*) Nakai's Vcc thus represents its "logic high voltage," which is consistent with the construction proposed above. And voltages higher than the nominal power supply voltage Vcc are higher than a "logic high voltage." (*See id.*, ¶ 34.) These other voltages are "boosted positive voltages."

### **III. When the Proper Claim Construction for "Logic High Voltage" Is Applied, Nakai Does Not Anticipate Claims 1 or 4 of the '045 Patent**

The only issue before the Board is whether Nakai anticipates independent claims 1 and 4 of the '045 patent. To establish anticipation under 35 U.S.C. § 102, "all of the elements and limitations of the claim must be shown in a single prior reference, arranged as in the claim." *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383 (Fed. Cir. 2001). "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987).

Nakai does not anticipate because its programming scheme applies a "boosted positive voltage" to unselected word lines, unselected bit lines and a bit line select control line (for bit line select transistors). This scheme is materially different from the programming scheme recited in claims 1 and 4, which require

the application of a “logic high voltage” to these same nodes of the array of flash memory cells during programming.

**A. Claims 1 and 4 Require the Application of Logic High Voltage to Certain Nodes of the Memory Array During Programming.**

Independent claims 1 and 4 require the application of certain voltages to program a flash memory array. Specifically, claim 1 requires, in relevant part:

a **logic high voltage** is applied to said bit line select control line to turn on bit line select transistors,

...

a logic low voltage is applied to a selected bit line while a **logic high voltage** is applied to unselected bit lines, and a **logic high voltage** is applied to unselected word lines, while a boosted positive voltage is applied to a selected word line.

Similarly, claim 4 also requires the application of a “logic high voltage” to the same nodes of a flash memory device (emphasis added):

applying a **logic high voltage** to a bit line select control line to turn on bit line select transistors,

...

applying a logic low voltage to a selected bit line while a **logic high voltage** is applied to unselected bit lines, and applying a **logic high voltage** to unselected word lines, while a boosted positive voltage is applied to a selected word line.

The '045 patent's method for programming a memory array thus requires the application of certain "logic high voltages" to certain nodes of the memory array. And, as discussed above, an exemplary "logic high voltage" from the '045 patent is  $V_{cc}$ . This is consistent with the patent owner's proposed construction for "logic high voltage" as "a positive voltage higher than logic low voltage and less than or equal to the nominal value for  $V_{cc}$ ."

**B. Nakai Does Not Anticipate Because Its Alleged "Logic High Voltages" Are "Boosted Positive Voltages"**

Nakai does not employ the same programming scheme set forth in challenged claims 1 and 4. Instead of applying "logic high voltages" to the relevant memory array nodes, Nakai applies various boosted positive voltages.

**1. Application of Properly Construed Claims to Nakai**

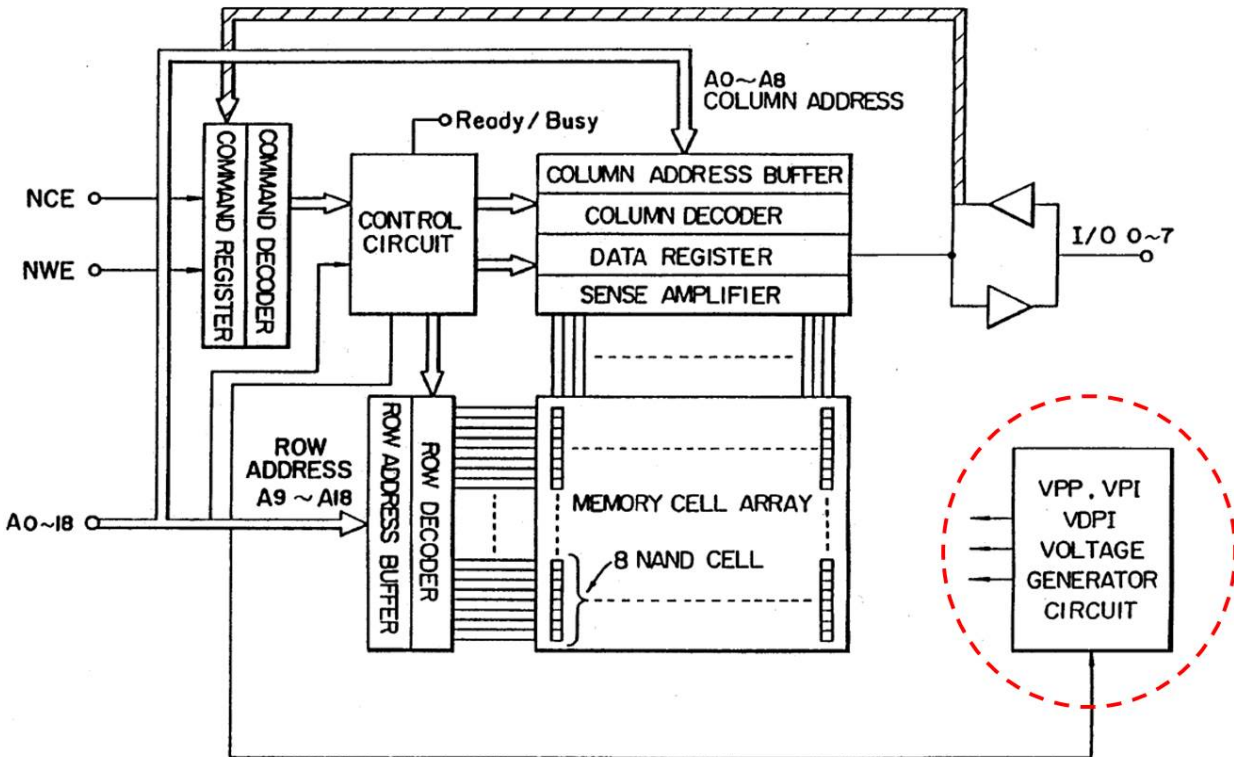
Nakai discloses a nominal power supply voltage  $V_{cc}$  of  $5V \pm 10\%$ . This is the only principled and precise dividing line between a "logic high voltage" and a "boosted positive voltage." (*See* Ex. 2001, Morales Dec., ¶¶ 31 and 39; *see* Ex. 2002, Berg Dec., ¶¶ 27-44; *see* Nakai, FIG. 20.) With this demarcation, it is clear that Nakai's  $V_{PI}$  (10V),  $V_{DPI}$  (10V) and 12V, which are applied to unselected word lines, unselected bit lines and a bit line select control line (for bit line select transistors), respectively, are all "boosted positive voltages." (*See* Ex. 2001, Morales Dec., ¶ 30; *see* Ex. 2002, Berg Dec., ¶¶ 59-65.)

FIG. 20 of Nakai (reproduced above) illustrates a timing chart of Nakai's memory device during a power-on reset operation.<sup>6</sup> (*See* Ex. 2001, Morales Dec., ¶¶ 35-37.) During this operation, the nominal power supply voltage  $V_{cc}$  transitions from 0V to the memory device's nominal operating voltage of 5V. (*See id.*) One of ordinary skill in the art would understand that the power-on reset operation is complete when  $V_{cc}$  reaches a level high enough to reliably perform logic functions, i.e., to provide a logic high voltage to its logic circuits. (*See id.*) Thus voltages higher than the nominal power supply voltage  $V_{cc}$  are higher than a logic high voltage. (*See id.*) These voltages are therefore boosted positive voltages.

This conclusion is consistent with Nakai's own disclosure. For example, Nakai's "boosted positive voltage" is generated on-chip—i.e., on the same chip containing the array of flash memory cells—using voltage generators or charge pumps. According to Nakai, "the power VDPI potential (10 V) [is] supplied from the voltage booster built in the chip." (Nakai, 20:14-20.) The voltage booster is described in Nakai's FIG. 26:

---

<sup>6</sup> Applied to Nakai, the Board's preliminary construction for "logic low voltage" is 0V. (*See* Ex. 2001, Morales Dec., ¶ 35.)

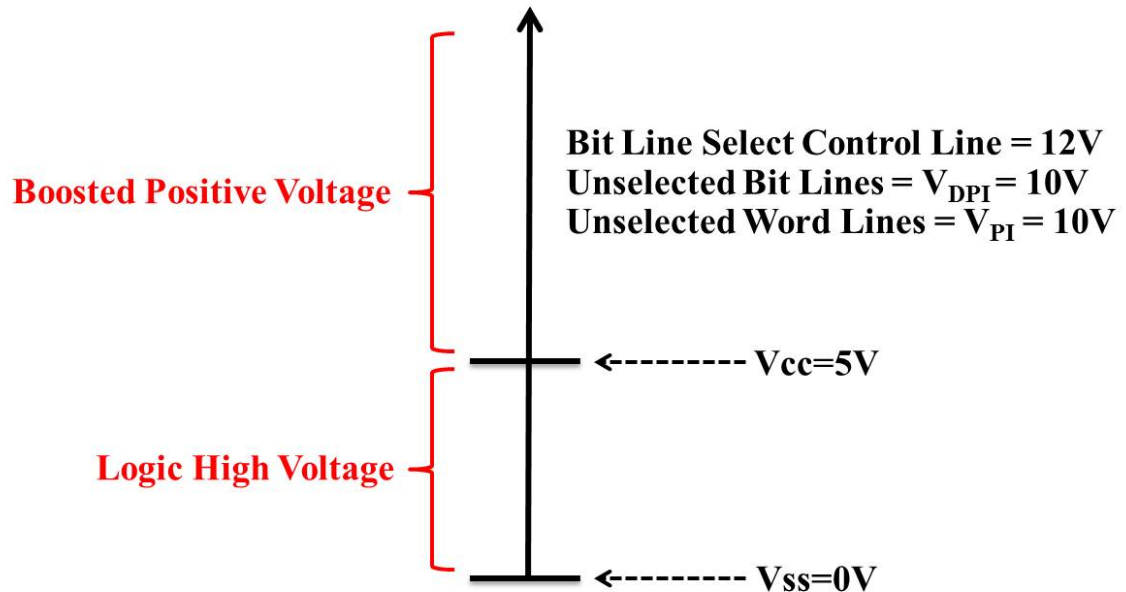


**FIG. 26 of Nakai (Annotated)**

As Nakai shows,  $V_{PP}$ ,  $V_{PI}$ , and  $V_{DPI}$  are all on-chip generated voltages that are higher than Nakai's power supply  $V_{CC}$ —i.e., Nakai's logic high voltage. Such voltage generator circuits were well known during the timeframe of the Nakai patent. Since  $V_{CC}$  is the only identified power supply, one of ordinary skill in the art would understand that the voltage generator circuits of Nakai generate  $V_{PP}$ ,  $V_{PI}$ , and  $V_{DPI}$  from  $V_{CC}$ . (See Ex. 2001, Morales Dec., ¶ 38; see Ex. 2002, Berg Dec., ¶¶ 45-54.)

Accordingly, when the constructions of “logic high voltage” and “boosted positive voltage” are properly applied to Nakai, a clear demarcation is defined

between the logic high voltage range and the boosted positive voltage range. The demarcation looks like this:



### **Properly Construed Claims as Applied to Nakai**

Therefore, Nakai applies the use of “boosted positive voltages” higher than Nakai’s  $V_{cc}$  of 5V (i.e., Nakai’s “logic high voltage”) and does not disclose the use of a “logic high voltage” as required by challenged claims 1 and 4.

### **2. Toshiba’s Flawed Application of Its Improper Proposed Claim Constructions to Nakai Cannot Stand**

Toshiba’s construction does not include any clear demarcation between logic high voltage and boosted positive voltage. Toshiba relies on this ambiguity for its assertion anything less than the 20V in Nakai on the selected word line is a “logic high voltage.” The chart from Toshiba’s petition is reproduced below:



Array Element	Voltages – '045 Patent claims 1 & 4	Voltages – Nakai
BSL	Logic High	12 V on SL(1) – i.e. logic high
SSL	Logic Low	0 V on SL(2) – i.e. logic low
Selected Bit Line	Logic Low	0 V on BL(1) – i.e. logic low
Unselected Bit Lines	Logic High	VDPI (10V) on BL(2) – i.e. logic high
Selected Word Line	Boosted Positive	V <sub>pp</sub> (20 V) on WL with Programmed Cell – i.e. boosted positive
Unselected Word Lines	Logic High	V <sub>PI</sub> (10V) on WL's without Programmed Cell – i.e. logic high

**Table from Toshiba's Petition Comparing Voltages Applied to Unselected Word Lines, Unselected Bit Line and Bit Line Select Control Line (with Dashed-Line, Highlighted Annotations)**

As applied to Nakai, Toshiba ignores the fact that Nakai defines V<sub>cc</sub> as 5V. (Nakai, FIG. 20.) In fact, Toshiba's technical expert Mr. Murphy overlooks the disclosure of V<sub>cc</sub> in Nakai:

So my recollection is that I don't recall V<sub>cc</sub> being talked about in Nakai, and I'm trying to see if there is a location that I've missed or—I don't see V<sub>cc</sub> specifically being quoted as what voltage it is. And I don't recall reading that it was set at a specific voltage. I'm sure it is. It just whether the patentee put in the spec or not.

(Murphy Depo. Transcript, p. 175, lns. 14-21.)

When Nakai's V<sub>cc</sub> is taken into account, and the proper construction is applied to Nakai, it becomes clear that Nakai's V<sub>PI</sub> (10V), V<sub>DPI</sub> (10V) and 12V are all "boosted positive voltages" since they are positive voltages higher than Nakai's V<sub>cc</sub> of 5V. Since claims 1 and 4 require a "logic high voltage" for the array

elements shown above rather than a “boosted positive voltage,” Nakai does not anticipate.<sup>7</sup>

**C. Advantages of the Claimed Invention over Nakai’s Programming Scheme**

The difference between the two programming schemes is material. The ’045 patent’s programming scheme confers distinct advantages over Nakai’s use of multiple boosted positive voltages. The advantages of avoiding Nakai’s multiple boosted positive voltages include improved reliability of the memory array transistors and reduced power consumption. (*See* Ex. 2002, Berg Dec., ¶ 66.) And obviating the need for multiple different boosted positive voltages could also reduce the need for multiple charge pumps or other on-chip circuitry to boost voltages, which reduces overall chip footprint. (*See id.*) Each of these improvements is commercially important to flash memory manufacturers and their customers. (*See id.*, ¶¶ 45-54.)

To be more specific, FIG. 4 of the ’045 patent illustrates two types of transistors used in its memory array: (1) an n-type transistor (for the bit line select

---

<sup>7</sup> Indeed, even if the Board does not alter its ambiguous preliminary claim construction, Nakai still does not anticipate. As shown, when the Board’s construction is *actually applied* to Nakai and to the ’045 patent, the upper boundary for “logic high voltage” becomes Vcc (instead of the indefinite “such as Vcc”).

transistors 404), and (2) a floating-gate transistor (for the flash memory cells 402).

The application of a “logic high voltage”— $V_{cc}$  in the '045 patent—to each of these types of transistors confers advantages over the application of a higher voltage, such as a “boosted positive voltage.”

For the n-type transistors, reducing the voltages on the bit line select transistors, the source and drain regions of the transistor can have the same diffusion construction. This, in turn, reduces the process complexity and device size. (*See* '045 patent, 2:14-16 (describing that, in reducing the voltage on a transistor junction, “[t]his allows the source junction to be the same size as the drain junction, and eliminates the high-voltage junction process requirements.”).) For the floating gate transistor a lower voltage (*e.g.*, a “logic high voltage”) applied to the control line of the floating gate transistor reduces stress on the floating gate of the memory cell, thus increasing reliability. (*See* Ex. 2002, Berg Dec., ¶¶ 67-70.)

Finally, being able to apply logic high voltage instead of various boosted positive voltages can save on-chip space. (*See id.*, ¶ 67.) Every additional boosted positive voltage that needs to be applied to the memory array could add increased complexity to the chip and increases chip space. This is because such boosted voltages are typically produced using on-chip charge pumps or other circuits. One of ordinary skill in the art would appreciate the benefits of reduced chip space and

complexity.

#### **IV. Conclusion**

For at least the foregoing reasons, Patent Owner respectfully requests the Board to deny the proposed ground of rejection that Nakai anticipates independent claims 1 and 4 of the '045 patent.

Respectfully submitted,

/Jon E. Wright/

Date: July 10, 2014

Robert Greene Sterne (Reg. No. 28,912)  
Jon E. Wright (Reg. No. 50,720)  
Raymond J. Werner (Reg. No. 34,752)  
Christian A. Camarce (Reg. No. 65,021)

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Donald J. Coulman (Reg. No. 50,406)

INTELLECTUAL VENTURES MANAGEMENT

Andrew G. Heinz (Reg. No. 59,996)

DESMARAIS LLP

**CERTIFICATION OF SERVICE**

The undersigned hereby certifies that the foregoing INTELLECTUAL  
VENTURES I LLC'S PATENT OWNER'S RESPONSE TO PETITION was  
served electronically via e-mail on July 10, 2014, in its entirety on the following:

Alan A. Limbach at **alan.limbach@dlapiper.com**

Gerald T. Sekimura at **gerald.sekimura@dlapiper.com**

**CC: IV-Toshiba-DLA-Team@dlapiper.com**

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Jon E. Wright/

Jon E. Wright  
Registration No. 50,720  
Attorney for Patent Owner

Date: July 10, 2014

1100 New York Avenue, N.W.  
Washington, D.C. 20005  
(202) 371-2600

1857726\_6