

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TOSHIBA CORPORATION
Petitioner

v.

INTELLECTUAL VENTURES I LLC
Patent Owner

CASE: IPR2014-00113
Patent 6,058,045

**DECLARATION OF LOUIS J. MORALES IN SUPPORT OF PATENT
OWNER'S RESPONSE TO PETITION**

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Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

IPR2014-00113
Toshiba Corporation v.
Intellectual Ventures I LLC
IV 2001

I, Louis J. Morales, a resident of Somerville, Massachusetts, declare as follows:

1. I have been retained on behalf of Intellectual Ventures I LLC to provide declaratory evidence in *inter partes* review of U.S. Patent 6,058,045 (“the ’045 patent”).

2. I am being compensated at my standard rate of \$300/hour for my work related to this *inter partes* review proceeding. My compensation is not dependent on and in no way affects the substance of my statements in this Declaration.

3. I have reviewed and am familiar with the specification and the claims of the ’045 patent. I will cite to the specification using the following format: (the ’045patent, 1:1-10.) This example citation points to the ’045patent specification at column 1, lines 1-10.

4. I have reviewed and am familiar with following references used in the petition for *inter partes* review of the ’045 patent:

- U.S. Patent No. 6,058,045 to Pourkeramati (“Pourkeramati”; TOSH-1001);
- Prosecution File History for U.S. Patent No. 6,058,045 (TOSH-1002);
- Prosecution File History for U.S. Patent No. 5,953,254 (TOSH-1003);

- Provisional Patent Application 60/025,698 (TOSH-1004);
- U.S. Patent No. 5,297,029 to Nakai (“Nakai”; TOSH-1005);
- Declaration of Robert J. Murphy (“Murphy Dec.”; TOSH-1006);
- *A 35 ns Cycle Time 3.3 V Only 32 Mb NAND Flash EEPROM*, Yoshihisa Iwata, *et al.*, IEEE Journal of Solid-State Circuits, (November 1995) (“Toshiba IEEE Article”; TOSH-1007);
- Declaration of Doug Wong (“Wong Dec.”; TOSH-1008); and
- Datasheet for TC584000P/F/FT/TR CMOS NAND E²PROM electrically erasable and programmable Nonvolatile Memory, published in Toshiba 1993 MOS Memory (Non-Volatile) Databook (“1993 Databook”; TOSH-1009).

5. I have also reviewed and refer to the Board’s Decision to Institute *Inter Partes* Review in this proceeding (Paper 13, “Decision”) and the transcript of the deposition of Robert Murphy, the declarant for Petitioner.

6. I am familiar with the technology at issue and the state of the art at the time the application leading to the ’045 patent was filed, as well as the state of the art at the time of filing of provisional application no. 60/025,698, from which the ’045 patent claims priority.

7. I have been asked to provide my technical review, analysis, insights and opinions regarding the above-noted references, as well as various semiconductor industry practices.

Qualifications

8. My academic and professional pursuits are closely related to the subject matter of the '045 patent, including experience working with flash memory and NAND flash memory in particular.

9. I have over 34 years of experience in the field of semiconductors and integrated circuit (IC) design.

10. I received a Bachelor of Science degree in Electrical Engineering with graduate coursework in semiconductor design and processing from the State University of New York at Stony Brook (also known as Stony Brook University) in 1979.

11. From 1979 to 1980, I was a Design Engineer at General Instrument Corporation Microelectronics Division. While at General Instrument, I debugged and re-designed a 64K Read Only Memory (ROM) chip used in Mattel's

Intellivision video game system. I also significantly improved chip yield per wafer by over 100 times.

12. From 1980 to 1989, I was employed by Standard Microsystems Corporation, first as a Design Engineer and later as an Engineering Manager.

During this period my work included:

- Designing a high-speed token-bus local area network controller IC;
- Jointly developing an application-specific integrated circuit (ASIC) simulation system with Standard Microsystems' software group;
- Negotiating process design rules for new processes with wafer fab managers, accounting for manufacturing and design constraint tradeoffs;
- Specifying and designing Standard Microsystems' first standard cell library; and
- Managing an entire hard disk controller group in both design and test.

13. From 1989 to 1991, I was employed by Arrow Electronics as Manager of Arrow's Boston Design Center. During this period my work included:

- Providing technical support of sales efforts to identify potential clients and reviewing prospects regularly;
- Maintaining excellent relationships with customers;
- Collaborating with clients for custom and semi-custom IC development; and
- Supervising the Boston Design Center managing engineering staff.

14. In 1991, I founded co-founded iSine, Inc. and have been with iSine since its inception. I currently serve as iSine's Chief Technology Officer. While at iSine, my work has included:

- Managing an implementation group for an IC combining NAND flash memory and random access memory (RAM) for peripheral component interconnect (PCI) express products, including on-the-fly error correction code (ECC) without frame buffering;
- Developing many custom circuit blocks, including custom RAM, read-only memory (ROM), and non-volatile memory arrays. My most recent non-volatile circuit design was for a programmable voltage regulator IC. This used a custom-sized floating-gate

electrically erasable programmable read-only memory (EEPROM) circuit to store program values. I've also designed low-jitter phase-locked loops, analog-to-digital converters, digital-to-analog converters, delay lines, I/O pad cells (e.g., programmable impedance, low-jitter, low-voltage differential signaling, controlled impedance), Positive Emitter-Coupled Logic (PECL), and High-Speed Transceiver Logic (HSTL); and

- Supervising development and designing of dozens of mixed-signal ICs for networking, lighting, and consumer electronics.

15. In addition to my semiconductor industry experience, I am an inventor on 4 U.S. patents and 2 pending patent applications that relate to integrated circuit design.

Level of Skill in the Art

16. I have been asked to consider the level of ordinary skill in the field that someone would have had at the time the claimed invention was made. In deciding the level of ordinary skill, I considered the following:

- the levels of education and experience of persons working in the field;

- the types of problems encountered in the field; and
- the sophistication of the technology.

17. Based on the technologies disclosed in the '045 patent, one of ordinary skill in the art would have a Bachelor of Science degree in Electrical Engineering or an equivalent field, as well as at least 3 years of academic or industry experience in the field of flash memory.

Technical Statements

Configuration and voltages of the flash memory of the '045 patent

18. Claims 1 and 4 of the '045 patent are directed to a programming operation for a flash memory array. In reference to Fig. 4 of the '045 patent (reproduced below with annotations), during the programming operation, a “boosted positive voltage” (e.g., 15-20V) is applied to a selected word line (WL1) and a “logic low voltage” (e.g., V_{ss}) is passed to the drain terminal of the selected memory cell.

19. The “logic low voltage” is passed to the drain terminal of the selected memory cell via a bit line select transistor and an unselected memory cell, which both have a “logic high voltage” (e.g., V_{cc}) applied to their respective control terminals.

20. The application of the “boosted positive voltage” and “logic low voltage” to the control line and drain terminal of the selected memory cell, respectively, produces a strong electric field necessary to induce Fowler-Nordheim tunneling of electrons onto the floating gate of the selected flash memory cell—where the electrons are trapped. In turn, the presence of the trapped electrons increases the turn-on voltage of the selected flash memory cell. It is this increased turn-on voltage that represents a data value stored in the selected flash memory cell. (See the '045 patent, 6:17-20.)

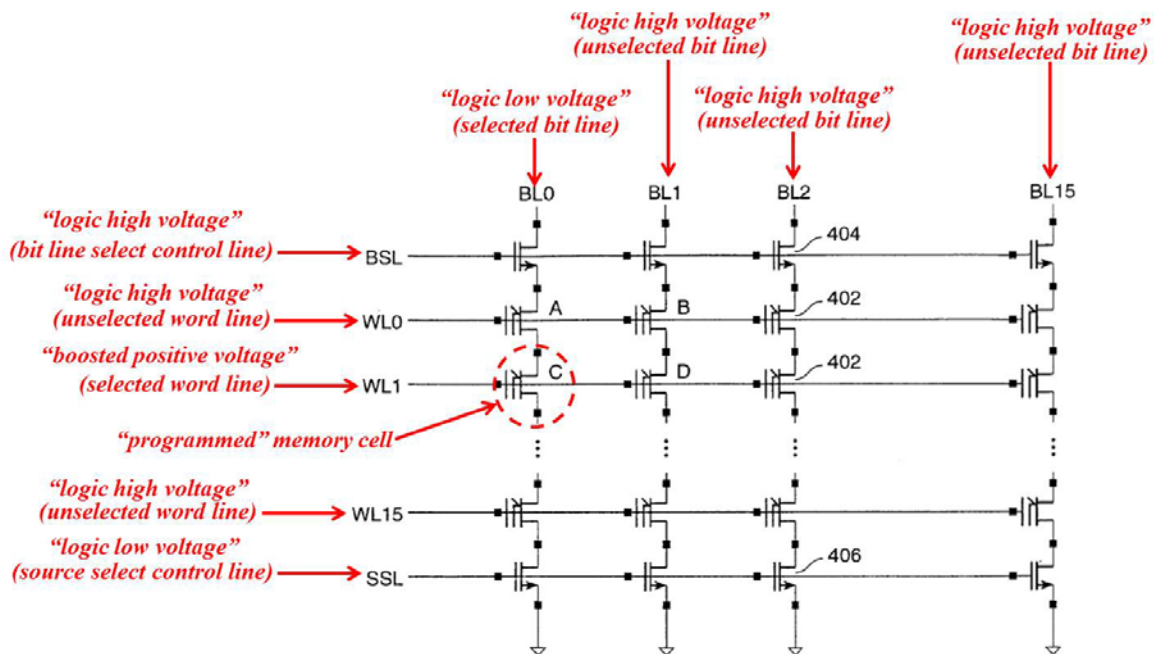


FIG. 4 from the '045 Patent (with Annotations)

21. Table 1 from the '045 patent (reproduced below with an annotation) provides example voltages for a “logic low voltage,” a “logic high voltage” and a

“boosted positive voltage.” Based on the voltages illustrated above in Fig. 4 and the example voltages provided in Table 1 below, an example of a “logic low voltage” is V_{ss} , an example of a “logic high voltage” is V_{cc} , and an example of a “boosted positive voltage” is a voltage between 15 and 20V.

TABLE I

Control Line	Erase	Program	Read	Condition
BSL	V_{cc}	V_{cc}	V_{cc}	Selected
SSL	V_{ss}	V_{ss}	V_{cc}	Selected
BLO	V_{cc}	V_{ss}	1.0–1.4V	Selected
BL1	V_{ss}	V_{cc}	0.5V	Unselected
WL0	V_{cc}	V_{cc}	V_{cc}	Unselected
WL1	-12 to -15V	15–20V	V_{ss}	Selected

Table 1 from the '045 Patent (with Annotation Indicating Example Voltages Applied During Programming Operation)

22. An important part of programming the flash memory cell also includes ensuring that unselected memory cells are not inadvertently programmed. ('045 patent, 8:4-8.) To that end claims 1 and 4, include limitations that “a logic high voltage is applied to unselected word lines,” “a logic high voltage is applied to unselected bit lines,” and “a logic high voltage is applied to said bit line select control line to turn on bit line select transistors.”

23. This arrangement results in unselected memory cells having a smaller electric field between their respective control gates and channel regions than the selected memory cell. The smaller electric field in unselected memory cells is not strong enough to induce tunneling in these devices. This prevents programming of unselected memory cells. This is referred to as “program inhibit.”

24. The '045 patent describes Vss as referring to ground or 0V: “Source select transistors 406 couple **ground (or Vss)** to memory cells 402.” ('045 patent, 6:29-30, emphasis added.) A logic low voltage on a complementary metal-oxide-semiconductor (CMOS) IC, such as the CMOS IC described in the '045 patent is nominally equal to a ground node of the power supply voltage to the IC and is usually referred to as “VSS” (or “Vss”). By “nominally equal,” I mean that because these are real-world devices and not mathematical models, it is understood by those skilled in the art that there will be small variations within an expected tolerance range.

25. The '045 patent specification does not provide an explicit definition for the term “Vcc,” but this term is commonly understood as the primary positive supply voltage to an IC. The upper bound of a logic high voltage on a CMOS IC is typically equal to the value of the primary positive supply voltage to the IC.

26. When the '045 patent was filed, the primary positive power supply voltage provided to a flash memory devices was normally either 3.3V or 5.0V. These values for the positive supply voltages are consistent with the program mode of operation described in the '045 patent: “The programming operation is done by . . . grounding the selected bit line (BL0) . . . ***Vcc is applied to BSL control line and [unselected word line] WL0*** to couple [the grounded] BL0 to the drain terminal of cell 402-C.” ('045 patent, 7:27-34, emphasis added.)

27. The '045 patent discloses that power supply voltages, such as Vcc, can provide sufficient voltage levels to pass ground voltage to the drain of the flash memory cell selected for programming. Specifically, ground is passed from the selected bit line through a bit line select transistor, and through an unselected flash memory cell. ('045 patent, 7:27-35.)

28. With regard to the boosted positive voltage between 15 and 20V applied to the selected word line (WL1), this voltage is higher than the typical primary positive voltage supply, i.e., Vcc, in CMOS integrated circuits.

Logic levels in integrated circuits

29. By definition, logic levels are Boolean representations having only two logic states—logic high and logic low. This is well known to design engineers

in the field of logic design for integrated circuits. Some relevant references showing this concept are as follows:

a) In S. Kang *et al.*, *CMOS Digital Integrated Circuits: Analysis and Design*, Chapter 5, p. 134, (Lynn Cox ed., The McGraw-Hill Companies, Inc., 1996), this reference states that “[u]sing positive logic convention, the Boolean (or logic) value of ‘1’ can be represented by a high voltage of VDD [the notational equivalent of VCC], and the Boolean (or logic) level of ‘0’ can be represented by a low voltage of 0 [volts].” (Ex. 2012, p. 134.)

b) In H. Haznedar, *Digital Microelectronics*, 2 (Benjamin Cummings Publishing Company, Inc., 1991), this reference states that “logic states are described by two nominal voltage levels, the higher of which, corresponding to the power supply voltage, Vcc, represents 1 in positive logic while the ground (i.e., 0V) represents 0.” (Ex. 2013, p. 2.)

Configuration and voltages of the flash memory of Nakai

30. The manner of programming and the programming voltages in Nakai are described at 1:45-2:9, and Figs. 23(a)-(c). Unselected bit lines and unselected word lines are set to a boosted positive voltage of about 10V; the selected word

line is set to another boosted positive voltage (V_{PP} or 20V); the bit-line (BSL) gates are at yet another boosted positive voltage of 12V; and source select gates (SSL) and selected bit line voltage are at 0V.

31. The memory devices disclosed in the '045 patent and Nakai both have a nominal power supply that is referred to as " V_{CC} ," as was common in the art. And both describe boosted positive voltages that are higher than V_{CC} and that are applied to the memory array. The power supply voltage V_{CC} is the upper limit of the logic high voltage for the memory devices disclosed by both the '045 patent and Nakai. V_{CC} provides a practical dividing line between a "logic high voltage" and the higher "boosted positive voltage" that appears in claims 1 and 4.

Differences between Nakai and the '045 patent

32. The '045 patent claims only reference one "boosted positive voltage," for example the requirement that "a boosted positive voltage is applied to a selected word line." All other signals are described as "logic high voltage" or "logic low voltage." As discussed above, an example of the logic high voltage is " V_{CC} " and an example of the logic low voltage is " V_{SS} ." ('045 patent, Table 1.) And one of ordinary skill in the technical field of flash memory would understand that "logic high voltage" would be nominally equal to or lower than V_{CC} .

33. The primary positive voltage supply described in Nakai is V_{cc} . The V_{cc} level is shown to be $5V \pm 10\%$ in Nakai's Fig. 20 (reproduced below).

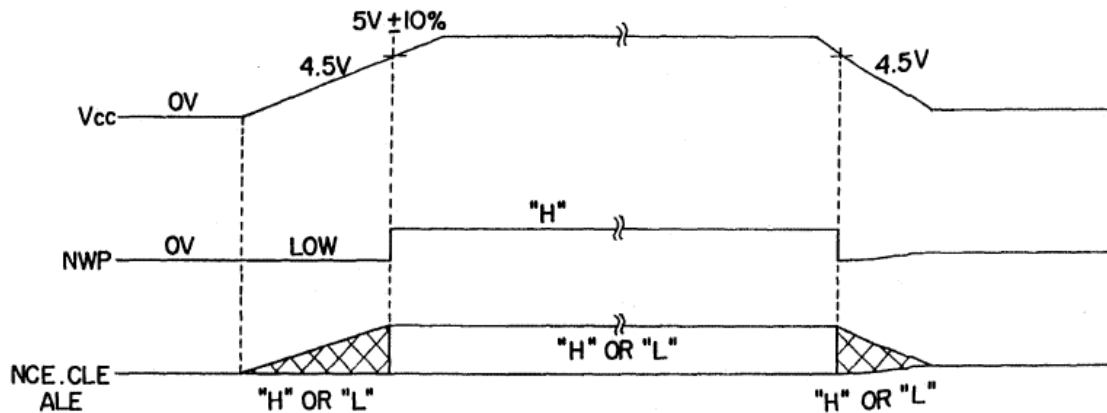


FIG . 20

34. Fig. 20 of Nakai illustrates a timing chart of Nakai's memory device during a power-on reset operation. As is common in integrated circuits, a power-on reset circuit prevents logic circuits from operating until the power supply voltage reaches the specified level at which a "logic high voltage" can be reliably produced by those logic circuits. During this operation, the nominal power supply voltage V_{cc} transitions from 0V to the memory device's nominal operating voltage of 5V.

35. The logic levels shown in Nakai's Fig. 14 (reproduced below) have voltages specified for boosted positive voltages. For example, bit lines BL1 and NBL1 are shown as having three possible voltage states: 0V, V_{cc} , and V_{DPI} .

These are clearly distinguished from the logic levels shown for most of the signals in the diagram.

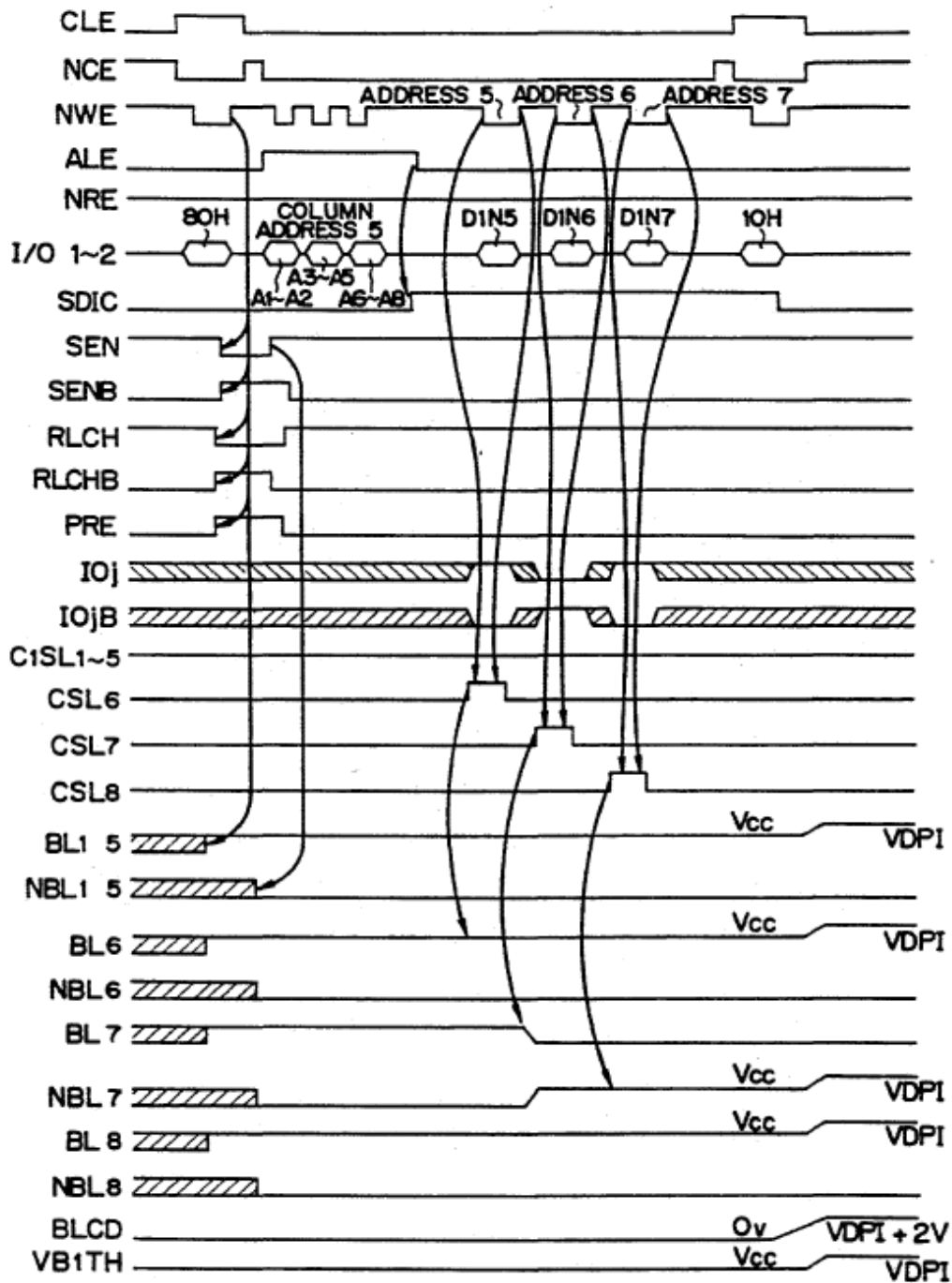


FIG. 14

36. One of ordinary skill in the art would understand that Nakai's memory device includes logic circuits.¹ Logic circuits may not function properly to produce logic high outputs until the primary positive power supply voltage reaches its specified operating range. Accordingly, the power-on reset operation is complete when V_{cc} reaches a level high enough for those logic circuits to reliably perform logic functions, i.e., to provide a logic high voltage to its logic circuits.

37. That is, Nakai's V_{cc} is the power-supply voltage at which the logic circuits on Nakai's memory device produce a logic high voltage at their respective outputs. Thus Nakai's V_{cc} represents the "logic high voltage" and voltages higher than the nominal power supply voltage V_{cc} are higher than a logic high voltage. Nakai's other voltages are therefore boosted positive voltages.

38. In Nakai's Figs. 1 and 26 (reproduced below), voltages V_{PI} , V_{DPI} , and V_{PP} are shown as originating from the "voltage generator circuit." Since the V_{cc} is the only identified supply, one of ordinary skill in the art would understand that the voltage generator circuit is generating these higher positive voltages from V_{cc} .

¹ See, e.g., Nakai's Fig. 1 which shows logic circuitry including a command register, a command decoder, a row decoder and a column decoder.

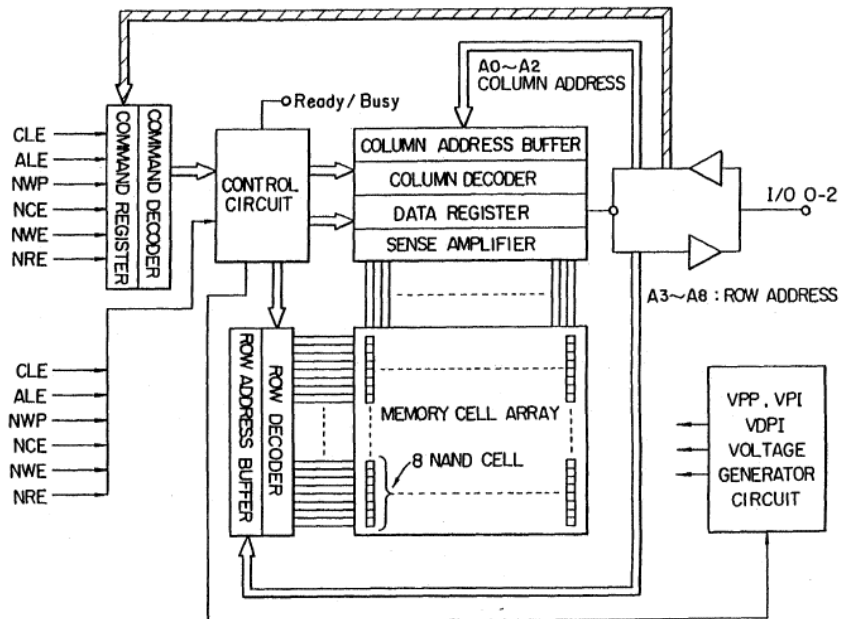


FIG. 1

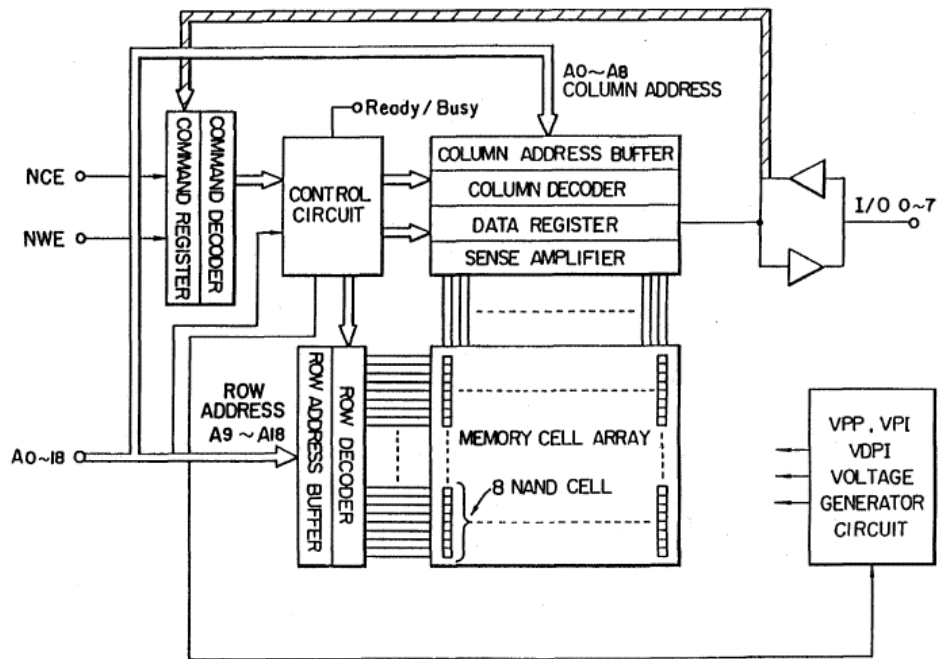


FIG. 26

Conclusion

39. The claims of the '045 patent advantageously recite only one “boosted positive voltage” in its programming mode of operation. Nakai discloses a different programming mode of operation. Nakai however, applies such higher “boosted positive voltages” to the unselected word lines, the unselected bit lines, and the bit line select transistors. Indeed, Nakai uses three “boosted positive voltages” in its programming mode of operation. Nakai’s voltages VPI and VDPI are higher than Vcc. And, Vcc is the only reasonable and principled boundary between logic high voltages and boosted positive voltages as I explain above.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the '045 patent.

Executed this 10th day of July 2014 in Somerville, MA.

Respectfully submitted,

A handwritten signature in black ink, appearing to read 'Louis J Morales', written over a horizontal line.

Louis J Morales

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