

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TOSHIBA CORPORATION
Petitioner

v.

INTELLECTUAL VENTURES I LLC
Patent Owner

CASE: IPR2014-00113
Patent 6,058,045

**DECLARATION OF JOHN E. BERG IN SUPPORT OF
PATENT OWNER'S RESPONSE TO PETITION**

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IPR2014-00113
Toshiba Corporation v.
Intellectual Ventures I LLC
IV 2002

I, John E. Berg, a resident of Palo Alto, California, declare as follows:

1. I have been retained on behalf of Intellectual Ventures I LLC, to provide declaratory evidence in *inter partes* review of U.S. Patent 6,058,045 (“’045 patent”).
2. I am being compensated at my standard rate of \$300/hour for my work related to this *inter partes* review proceeding. My compensation is not dependent on and in no way affects the substance of my statements in this Declaration.
3. I have reviewed and am familiar with the specification and the claims of the ’045 patent. I will cite to the specification using the following format: (’045 patent, 1:1-10). This example citation points to the ’045 patent specification at column 1, lines 1-10.
4. I have reviewed and am familiar with following references used in the petition for *inter partes* review of the ’045 patent:
 - U.S. Patent No. 6,058,045 to Pourkeramati (TOSH-1001, “Pourkeramati;”);
 - Prosecution File History for U.S. Patent No. 6,058,045 (TOSH-1002);
 - Prosecution File History for U.S. Patent No. 5,953,254 (TOSH-1003);

- Provisional Patent Application 60/025,698 (TOSH-1004);
- U.S. Patent No. 5,297,029 to Nakai (TOSH-1005, “Nakai”);
- Declaration of Robert J. Murphy (TOSH-1006, “Murphy Dec.”);
- *A 35 ns Cycle Time 3.3 V Only 32 Mb NAND Flash EEPROM*, Yoshihisa Iwata, *et al.*, IEEE Journal of Solid-State Circuits, (November 1995) (TOSH-1007, “Toshiba IEEE Article”);
- Declaration of Doug Wong (TOSH-1008, “Wong Dec.”); and
- Datasheet for TC584000P/F/FT/TR CMOS NAND E²PROM electrically erasable and programmable Nonvolatile Memory, published in Toshiba 1993 MOS Memory (Non-Volatile) Databook (TOSH-1009, “1993 Databook”).

5. I have also reviewed and refer to the Board’s Decision to Institute *Inter Partes* Review in this proceeding (Paper 13, “Decision”), and I attended the deposition of Toshiba’s declarant, Robert Murphy, and reviewed his deposition transcript.

6. I am familiar with the technology at issue and the state of the art at the time the application leading to the ’045 patent was filed, as well as the state of the art at the time of the filing of provisional application no. 60/025,698, from which the ’045 patent claims priority.

7. I have been asked to provide my technical review, analysis, insights, and opinions regarding the above-noted references, as well as various semiconductor industry practices.

Qualifications

8. My academic and professional pursuits are closely related to the subject matter of the '045 patent.

9. I have more than 34 years of experience in the management and hands-on product development, process development, and design of high speed, complex commercial semiconductor products, including the design of standalone and embedded memory devices (*e.g.*, SRAM, EEPROM, NOR Flash, and NAND flash memory devices) and CMOS logic devices (*e.g.*, microcontrollers, digital signal processors, and application specific standard products).

10. I earned a Bachelor of Science degree in Physics in 1980 from Massachusetts Institute of Technology in Cambridge, Massachusetts. I also undertook additional graduate coursework in semiconductor process and circuit design at Stanford University in Palo Alto, California ("Stanford") from 1998 to

2002. In 2003, I earned a Master of Science degree in Management from the Graduate School of Business at Stanford.

11. I am currently the Chief Technologist at American Semiconductor Incorporated in Santa Clara, CA. American Semiconductor fabricates radiation-hard CMOS products for military and aerospace customers. At American Semiconductor, I have developed front-end and back-end wafer scale processes for antenna array products, integrated the company's double-gate CMOS process into production, and developed a 45 nm radiation-hard CMOS process for aerospace applications.

12. Prior to American Semiconductor, I was the Chief Operating Officer at Transfer Devices of Santa Clara, CA from 2004-2005, where I oversaw the building of a class 10 manufacturing clean room and launched the ExaGlide 10r nano-patterning production tool development program. Prior to Transfer Devices, I was Vice President of New Product Development at Nantero, Incorporated ("Nantero") of Woburn, MA from 2003-2004, where I led the design and production of a 4 Mb NOR FLASH non-volatile memory chip.

13. Prior to Nantero, I was Managing Director of Programmable Logic at Cypress Semiconductor, where I managed the company's Programmable Logic Business Unit and designed CPLD products with NOR FLASH.

14. From 1990 to 1998, I was Vice President of Technology Development at Zilog Corporation of Nampa, ID. As Vice President at Zilog, I oversaw the design and production of over 45 microcontroller products and patented the transistor and process technology instrumental in launching the company's infrared remote microcontroller product family.

15. From 1980-1990, I was Engineering Director at Standard Microsystems Corporation of Hauppauge, NY. As Engineering Director at Standard Microsystems, I delivered the company's first CMOS process used in the fabrication of product storage microcontrollers, and I managed the company's process development group. At Standard Microsystems, I worked, from 1988 to 1989, with Frank Wanlass, who was the first person to build fully functional CMOS circuits (Neil H. E. Weste & Kamran Eshraghian, *Principles of CMOS VLSI Design* 3-4 (2nd edition, 1993) (Ex. 2005)).

16. In addition to my semiconductor industry experience, I am an inventor on 15 U.S. patents that relate to semiconductor process and circuit design. I am also active in the semiconductor community as an author of technical articles published in well-known semiconductor publications and as a member of a number of semiconductor organizations.

17. For example, I have published peer-reviewed articles in IEEE Transactions on Electron Devices and Silicon Valley Engineering Council Journal. I am also an Electronics & Nanotechnology Phase I & II SBIR Reviewer for the National Science Foundation. I am the Chair Emeritus and Founding Member of the IEEE San Francisco Bay Area Nanotechnology Council. I am on the Executive Committee of the Silicon Valley IEEE Silicon Valley Section.

Level of Skill in the Art

18. I have been asked to consider the level of ordinary skill in the field that someone would have had at the time the claimed invention was made. In deciding the level of ordinary skill, I considered the following:

- the levels of education and experience of persons working in the field;

- the types of problems encountered in the field; and
- the sophistication of the technology.

19. Based on the technologies disclosed in the '045 patent, one of ordinary skill in the art would have a Bachelor of Science degree in Electrical Engineering or an equivalent field, as well as at least 3 years of academic or industry experience with flash memory

Technical Statements

20. The '045 patent discloses a NAND flash memory. The '045 patent claims at issue here focus on programming a flash memory array using different voltages. To evaluate the '045 patent properly, I now provide some background information with respect to transistor voltages.

Typical Transistor Voltage Description

21. One of ordinary skill in the art would recognize a voltage, or potential difference, is measured across two terminals: “voltage is defined between two points.” (Ex. 2006, Thomas, p. 12.) As a matter of convention, there is a point in a circuit, which is defined as ground potential: “it is often useful to define a

common voltage reference point called ground.” (Ex. 2006, Thomas, p. 12.) All other potentials are then measured relative to that ground potential point: “[t]he voltages at all other points in a circuit are then defined with respect to this common reference.” (Ex. 2006, Thomas, p. 12.) In order to define any voltage on an integrated circuit, it necessary to define the reference voltage point.

22. By convention in the semiconductor chip industry, all voltages are typically referenced to the lowest external power supply, which is connected to the chip. One of ordinary skill in the art would recognize this is typically referred to as V_{ss} , and this V_{ss} potential is typically, by convention, defined as ground potential, or nominally 0V. “[L]ow voltage ... is normally set to zero volts and called GROUND (GND) or Vss.” (Ex. 2005, Weste, p. 7.) Usually, all other on-chip voltages are referenced to their respective potential differences to V_{ss} . Typically, for CMOS logic circuits such as an inverter and a NOR gate to work properly, at least one NMOS device source and its p-type substrate are tied to V_{ss} , which again is typically the ground potential.

23. Absent any other indication in a reference, “Vcc” is understood by those of ordinary skill in the art to represent the positive terminal of a power

supply coupled to an integrated circuit, such as a flash memory chip. Vcc is also understood by those of ordinary skill in the art to represent the magnitude of the voltage at the positive terminal of the power supply. And Vcc is typically used to refer to the positive voltage supply node used by logic circuits on an integrated circuit.

Claim Terms

24. Claims 1 and 4 of the '045 patent recite three voltages: a “logic low voltage;” a “logic high voltage;” and a “boosted positive voltage.” Given that the claims recites three voltage terms, these voltages must have ranges that are different from one another.

25. These voltages, according to independent claims 1 and 4 are used to program a flash memory array.

Logic Low Voltage

26. The Board preliminarily construed “logic low voltage” to mean a low voltage such as ground or Vss. (Decision, p. 7.) I do not agree with this construction. Standing alone, the Board’s construction is imprecise because, it does

not provide a clear demarcation between the range of “logic low voltage” and the range of the recited voltage—a “logic high voltage.”

Logic High Voltage

27. The Board preliminarily construed “logic high voltage” as “a positive voltage higher than a logic low voltage, such as V_{cc} .” (Decision, p.8.) I do not agree with this construction. Standing alone, the Board’s construction is imprecise because, it does not provide a clear demarcation between the range of “logic high voltage” and the range of the third recited voltage—a “boosted positive voltage.”

28. A more precise construction would be to define the boundary between a “logic high voltage” and a “boosted positive voltage” as the nominal value of V_{cc} . That is, a “logic high voltage” would be greater than a logic low, and less than or equal to the nominal value of V_{cc} , i.e., the power supply to the flash memory chip.

29. But even when the Board’s imprecise definition is actually applied to the ’045 patent, logic high voltage has an upper bound set by the voltage of the V_{cc} power node within the disclosed chip. Indeed, one of ordinary skill

reading the '045 patent would understand the upper bound of its “logic high voltage” to be the upper bound of the nominal power supply voltage, i.e., V_{cc} .

30. So when the Board’s construction of “logic high voltage” is applied to the '045 patent, the “logic high voltage” applied to the unselected word lines, unselected bit lines, and the bit line select control signal during the program mode of operation is V_{cc} . This is reflected in Table 1 of the '045 patent. ('045 patent, Table 1.)

31. I now turn to Nakai. Nakai discloses that its power supply voltage V_{cc} is nominally 5V (i.e., $5V \pm 10\%$). (See *e.g.*, Nakai, Fig. 20.) Thus, when the Board’s construction of “logic high voltage” is applied to Nakai in same manner as it is understood in the '045 patent, one of ordinary skill in the art would understand that Nakai’s “logic high voltage” is also nominally V_{cc} .

32. However, during programming, Nakai does not apply its “logic high voltage” (i.e., its V_{cc}) to the unselected word lines, unselected bit lines, or the bit line select control signal during the program mode of operation. Rather, it applies one of several boosted positive voltages. Nakai is thus different from the '045 patent at least in this regard.

Boosted Positive Voltage

33. The Board preliminarily construed “boosted positive voltage” as “a positive voltage higher than the logic high voltage.” (Decision, p. 8.) As long as there is a consistent method to determine an actual value for “logic high voltage,” and to delineate and differentiate that value from the value of the “boosted positive voltage,” this construction is reasonable.

34. The '045 patent’s “boosted positive voltage” is higher than its “logic high voltage”—i.e., higher than V_{cc} . Specifically, the '045 patent applies a boosted positive voltage in the range of 15-20V. (*See e.g.*, '045 patent, Table 1.)

35. When the Board’s construction of “boosted positive voltage” is applied to Nakai, it can be seen that Nakai applies boosted positive voltages to the unselected word lines, unselected bit lines, and to the bit line select control signal during the program mode of operation.

36. Specifically, Nakai applies its VPI (i.e., 10V) to the unselected word lines, its VDPI (i.e., 10V) to the unselected bit lines, and 12V (i.e., VDPI + 2V) to the bit line select control signal, during the program mode of operation. (Ex. 1005, Nakai, 1:46-2:19.) Each of these voltages (VPI, VDPI, and VDPI +

2V) are boosted above Nakai's V_{cc} power supply voltage—that is, above Nakai's logic high voltage. Therefore, these voltages are “boosted positive voltages.”

37. Whereas Nakai teaches the use of a boosted positive voltage for the bit select line during the write operation, the '045 patent teaches to use a logic voltage high for the bit select line during the write operation. For this and other reasons, Nakai's scheme for programming a flash memory array is different from the programming scheme described and claimed by the '045 patent

38. I now provide further support for my position.

The relationship between logic low voltage and logic high voltage

39. The range for “logic low voltage” and the range for “logic high voltage” do not (and cannot) overlap. If these two voltage ranges overlapped, then a logic circuit has a high likelihood of malfunctioning. A lower limit of the range of “logic high voltage” is referred to as the minimum input high voltage and may be represented as “ V_{ihmin} .” An upper limit of the range of “logic low voltage” is referred to maximum input low voltage and may be represented as “ V_{ilmax} .” An example is shown in a textbook used in the 1990's for integrated circuit design (Ex. 2005, Weste, p. 70); in this case, it is for an inverter. Note that Weste defines

a region between the logic high input range and the logical low input range as being an “indeterminate region.”

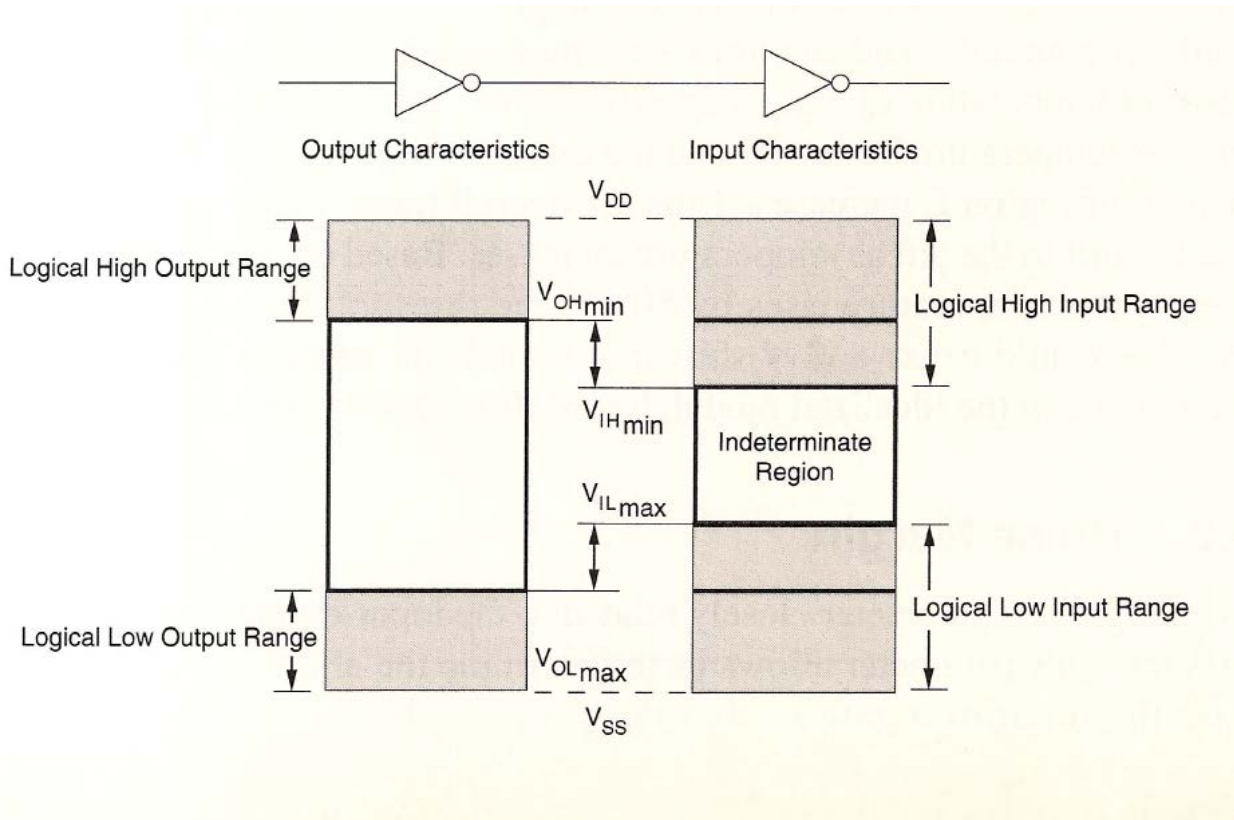


Figure 1: Logical High Voltage and Logical Low Voltages (Ex. 2005, Weste, p. 70)

40. To provide a scale to the “logic low voltage” and “logic high voltage,” that uses the ‘045 definitions and compares them to the Weste voltages, I have drawn the following exemplary diagram to provide visualization for the voltages, relative to one another.

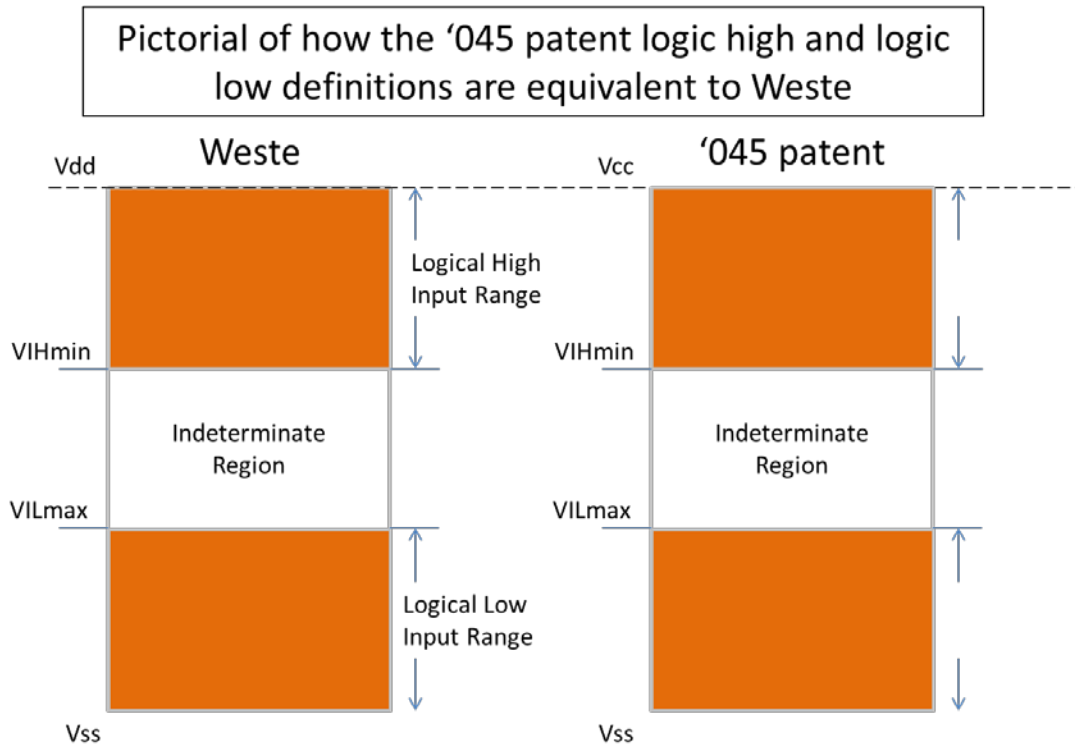


Fig. 2: Logic High Voltage, and Logic Low Voltage with '045 nomenclature

41. Similarly, this equivalency can be expressed in a table, which is shown below. Note the similarities in nomenclature (e.g., “logic high voltage” and logical high input voltage.) As Weste’s book concerns itself with digital logic CMOS circuits, it can be ascertained that the '045 patent used terms that were consistent with the logic textbooks at the time

Table 1: Mapping Weste and the '045 terms

	'045 patent term	Weste term
Logic high power supply	Vcc	Vdd
Logic low power supply, Ground	Vss	Vss
Logic "1" voltage range	Logic High Voltage	Logical High Input Range
Logic "0" voltage range	Logic Low Voltage	Logical Low Input Range

42. It is my opinion that a person of ordinary skill in the art would understand “logic high voltage,” in view of the specification and as confirmed by Weste to be: positive voltages extending from an upper specification of an external positive supply rail (i.e., Vcc) and down to a value above the trip point of a logic circuit. Specifically, claims 1 and 4 recite that the “logic high voltage” is applied to the “bit line select control line” (BSL), the unselected bit line and the unselected word line during programming. The '045 patent specification discloses that voltage Vcc is applied to those same lines during programming. (See '045 patent, 6:37-45 and 7:26-40.)

43. Within the '045 patent, the “logic high voltage” is not the same as a “boosted positive voltage.” One of ordinary skill in the art would understand them not to be the same as each other. Put differently, they cannot overlap.

44. Claims 1 and 4 of the '045 patent recite a “boosted positive voltage.” It is my opinion that a person of ordinary skill in the art would understand a

“boosted positive voltage” in view of the specification to be a positive voltage that is higher than the logic high voltage, i.e., higher than a nominal V_{cc}. At the time of Nakai’s patent filing, it was typical to generate boosted positive voltages using on-chip circuitry such as voltage generators or charge pumps. The ’045 patent specification discloses the benefits of reducing the number of pump circuits as one of the major benefits of the invention by “allow[ing] for the pump circuits to be aggressively down-sized, for a more compact overall design.” (’045 patent, 7:46-47.)

Advantages of reducing the number of boosted positive voltages required for programming.

45. The sizes of the charge pump circuits used to create “boosted positive voltage” in FLASH EEPROM devices are commercially important. And reducing the number and size of the charge pumps in order to produce more cost-effective circuits is known to be important. (’045 patent, 7:46-47.)

46. As another example beyond the ’045 patent, the Texas Instruments (“TI”) part below shows the area consumed by charge pumps required to generate boosted positive voltages. It is well known that reducing chip size reduces the cost of a chip. Thus the benefit of eliminating these large charge pumps can be easily

understood. The size of the charge pumps in its 256K CMOS FLASH EEPROM device (Ex. 2009, TI 1989, p. 208) are illustrated in red:

Fig. 3: Charge Pump areas in a TI 256k Bit CMOS FLASH EEPROM



47. The notion of “boosted positive voltages” is critical. It was well known that boosted voltages were being used on non-volatile memory circuits. This was first done with the EEPROM devices designed at Seeq Technology in 1981.¹

48. George Perlegos, one of the key inventors of EEPROM, which was a technology developed prior to FLASH EEPROM, discussed recently why “boosted positive voltages” were important in building products for the EEPROM:

“We had to have 20 volts in the system to be able to program and erase the devices. Then, after—I don't know if you want to go there, after I left Intel in 1981, then I went to SEEQ Technology. There we were able to develop a new technique. I developed a new technique that was able to create these high voltages on-chip. We developed on-chip charge pumps and everything else, all the other circuits, so now we didn't need any [extra] external voltage at all, [only the 5v that the microcontroller used]. The advantage of E-squared was that, as I said before, we required very little current, okay? So, we just needed a high voltage with very little current. So, we were able to then create

¹ <http://archive.computerhistory.org/resources/access/text/2013/11/102746703-05-01-acc.pdf> (Ex. 2007.)

the charge pumps on-board to do that. Which created 5-volt-only E-squared memory. We were the first to do that.”²

49. George Perlegos presented why boosted voltages on EEPROMs were important: one needed to route only a high voltage supply, Vcc, and a low voltage supply, Vss, to the chip. Reducing the number of external power supplies to the chip reduces the number of power traces on a printed circuit board and the number of pins on the chip; both of these reduce overall system cost. As an example, a 5.0 Volt-only, single power supply operation typically eliminates a DC/DC converter on the system board, thereby reducing overall system cost by “\$2 to \$4.”³

50. Furthermore, the single high power supply and the single low power supply are typically, as taught by Perlegos, the power supplies Vcc and Vss that are used by the digital circuitry in the chip.

51. My personal experience is consistent with that of Perlegos. At Standard Microsystems, which was building microcontrollers at that time, the n-channel metal-oxide semiconductor (NMOS) products we were building were +5V

² <http://archive.computerhistory.org/resources/access/text/2013/11/102746703-05-01-acc.pdf> (Ex. 2007)

Vcc parts. In other words, the microcontroller products, which were one type of logic device built in 1981, used one power supply that had a potential difference that was 5V higher than the low voltage power supply (e.g., a Vss power supply of ground or nominally 0V). Embedded memory and standalone memory products at Zilog and Cypress were designed and built with a single Vcc and ground.

52. With the development of on-chip current and voltage generators for EEPROM, it became apparent that building FLASH EEPROM devices with the same on-chip voltage generators was beneficial. Although one of the first disclosed FLASH EEPROM designs (Ex. 1007) did have a high voltage external power supply, the industry quickly worked on designs to have only two external supplies, Vcc and Vss. This quickly became a requirement for the FLASH EEPROM products. (Ex. 2009, p. 208.)

53. The same line of reasoning for using a “boosted positive voltage” in EEPROMs is equally applicable to FLASH EEPROMs, as discussed in the ’045 patent. Reducing the number of external power supplies to the chip reduces the number of power traces on a printed circuit board and the number of pins on the

3 http://noel.feld.cvut.cz/hw/amd/flash_.htm

chip; both of these reduce overall system cost. This is seen in one of the references that the '045 patent examiner cited: Iwata 1995, and in the TI paper mentioned above (Ex. 2009, TI 1989, pp. 206-208.) In both cases, a single high power supply is used. Iwata presents a 32Mb NAND FLASH EEPROM, where “[a]ll functions are operable with 3.3V only or 5 V only power supply.” (Ex. 1007, p.1.) TI presents a “5V-Only 256k Bit CMOS Flash EEPROM.” In both papers, charge pumps are shown and used to create voltages that are boosted above Vcc.

54. One of the challenges with charge pumps is that each charge pump takes up silicon area and draws current. Often, a charge pump is required for every specific voltage that is required to be boosted. Therefore, keeping the number of generated boosted positive voltages in floating gate transistor based non-volatile memories is of value, as it reduces the number of charge pumps (thus reducing silicon area) and correspondingly reduces the current draw of the part. The '045 patent specification also discusses these advantages, disclosing that reducing the number of charge pumps provides “for a more compact overall design.” ('045 patent, 7:47.)

Detailed Technical Comparison between Nakai and the '045 patent

55. I now turn to a more detailed analysis of Nakai. Like most of the prior art at that time, Nakai requires multiple, different, boosted positive voltages for programming.

56. Nakai discloses a NAND type EEPROM non-volatile memory array, also known as a NAND FLASH memory, which includes columns of memory cells “MC” connected in series. Each column is connected at the top to a bit line “BL” via a select transistor T1 and at the bottom to ground GND via a select transistor T2. Select lines SL(1) and SL(2) operate the row of select transistors T1 and the row of select transistors T2, respectively. The array includes word lines, WL, each of which connects to the select gates of one of the memory cells from each column. (Ex. 1005, 1:20-30.) The array is shown in Fig. 23(a) of Nakai (reproduced below along with FIG. 4 of the '045 patent). The array configurations are different: Nakai uses an 8-word high stack and the '045 patent uses a 16-word high stack.

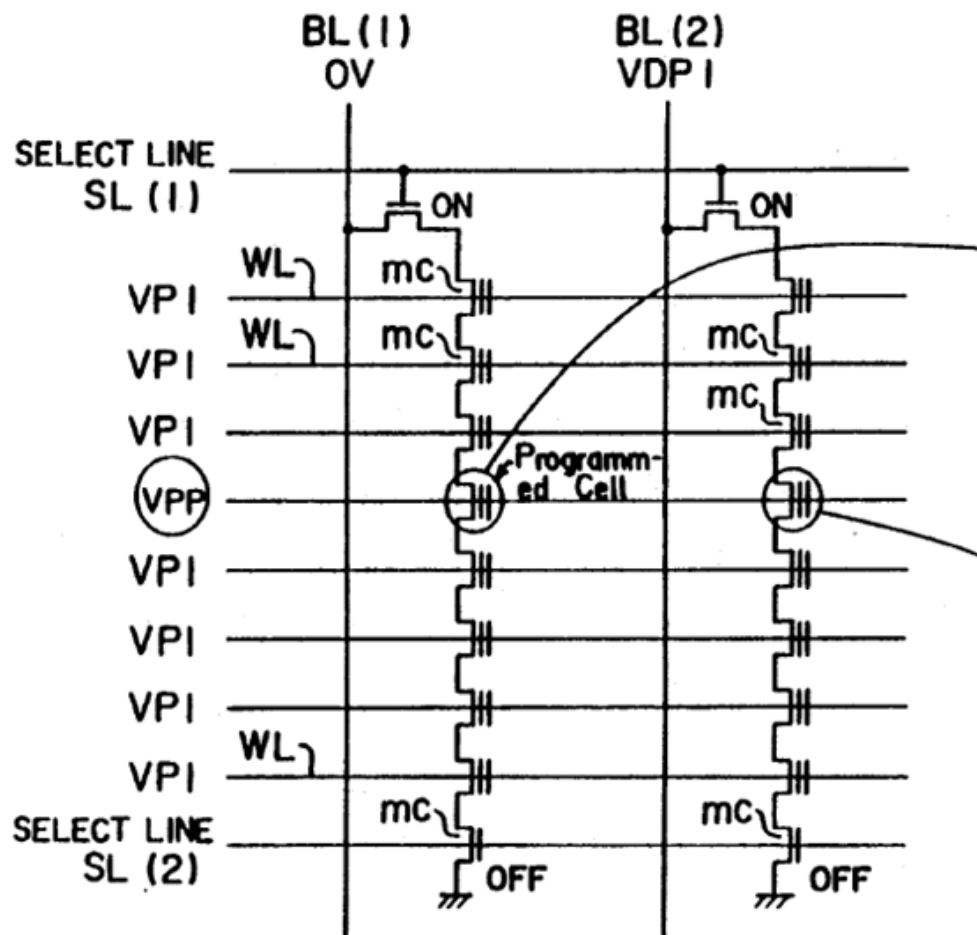


FIG. 23(a)

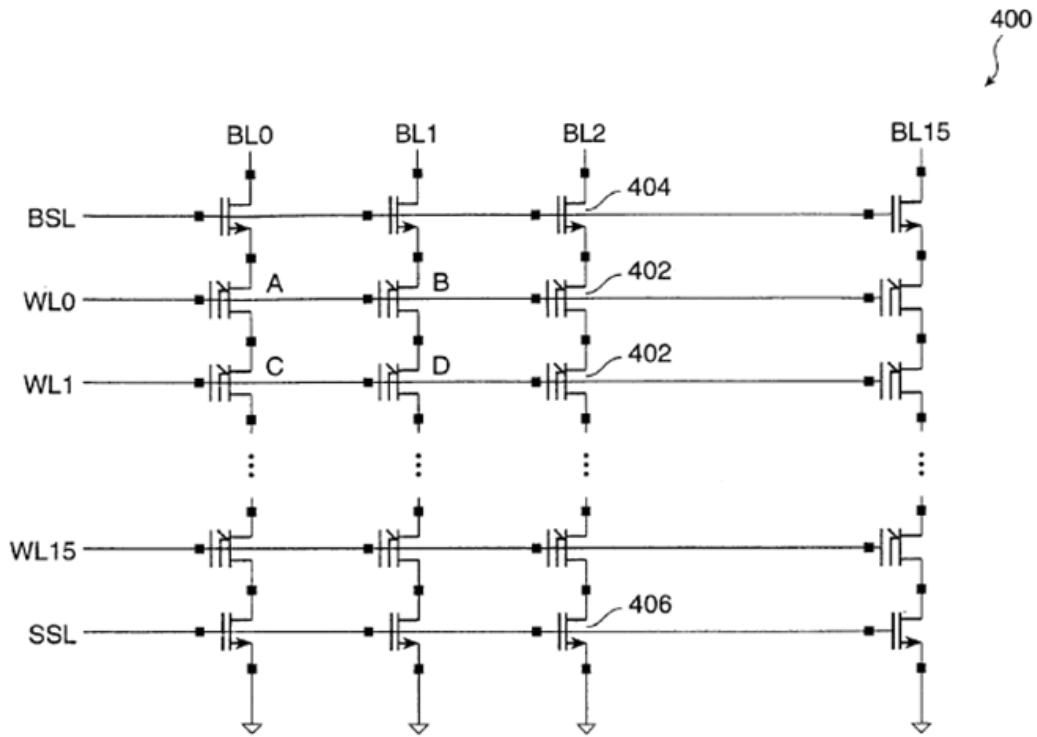


FIG. 4

57. The Nakai patent describes its write (programming) procedure in the specification, when describing Fig. 23(a) (Ex. 1005, 2:46 to 3:9):

Next, the write operation will be described. As shown in FIG. 23(a), a high voltage (V_{pp}) of about 20 V is applied from a row decoder to the select gate of a selected memory cell, and an intermediate voltage (V_{PI}) of about 10 V is applied to the select gates of the other seven memory cells of the NAND bundle 0 V is applied to the select gates of the other NAND bundle. The gate voltage of the select transistor between the NAND bundle containing the selected memory cell and the bit line is set to 12 V, and the gate voltage of the select transistor between the NAND bundle and the source line is set to 0 V. When the bit line is set to 0 V in this condition, the potentials of the drain, source, and channel of all the memory cells in the NAND bundle selected by the select transistors, become 0 V. Therefore, a potential difference of 20 V is generated between the select gate of the selected memory cell and its channel to inject electrons from the substrate into the floating gate. Although a potential difference of 10 V is generated between the select gates of the other seven memory cells of the NAND bundle and their channels, "0" data will not be written in the other seven memory cells because the oxide film thickness between each floating gate and channel is set so as not to allow the injection of electrons at the potential difference of 10 V. If a write inhibit drain voltage ($VDPI$) of about 10 V is applied to the bit line, the potential difference between the select gate and channel of the selected memory cell becomes 10 V, and data write is not effected. In the above manner, "0" data is written in the selected memory cell by setting the bit line to 0 V, and "1" data is written by setting the bit line to the $VDPI$ voltage.

58. The following is Fig. 23(a), which is annotated in red with the actual voltages from the Nakai specification.

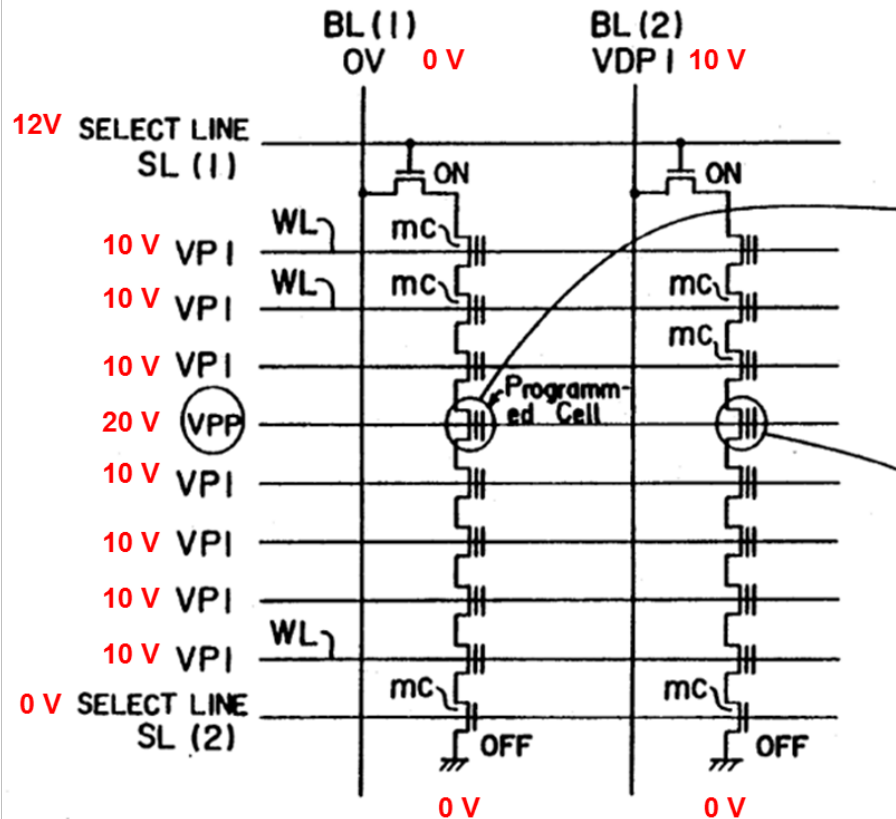
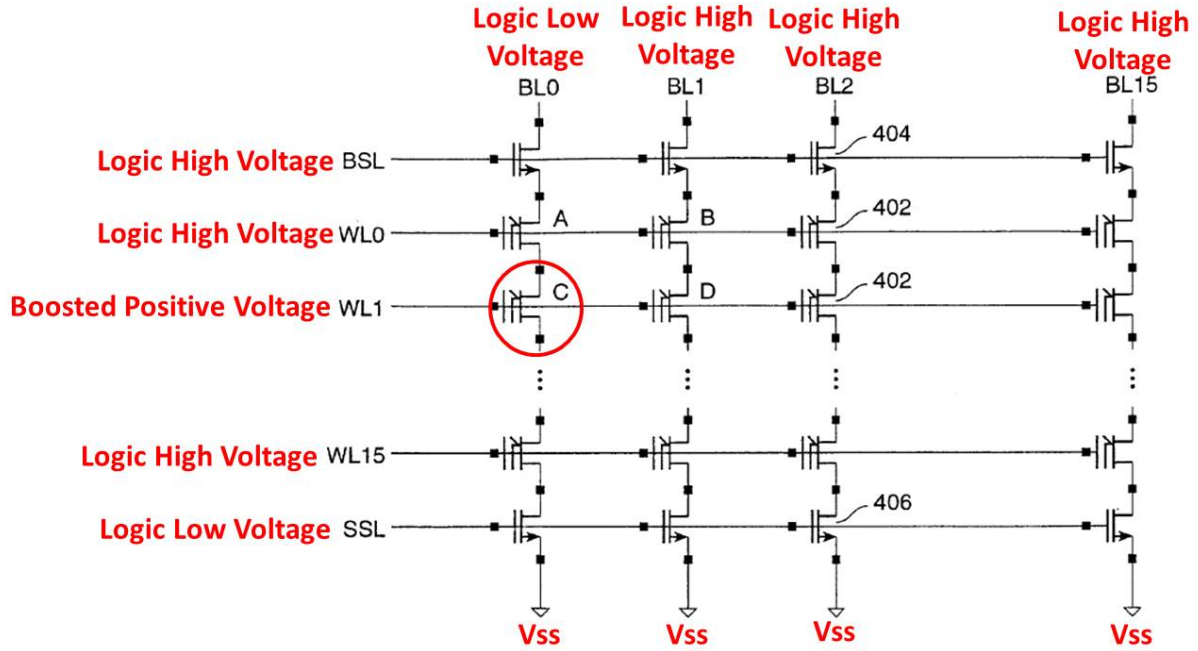


FIG. 23(a)

Summary of Differences Between Nakai and the '045 patent

59. For comparison, the '045 patent specifies the following voltages in claims 1 and 4, as annotated from its Fig. 4, where the cell marked "D" is being programmed:



From the above figures, a table of voltages can be created that provides the equivalent nodes for Nakai and the '045 patent, and their respective voltages:

Table 2: Comparison of Nakai Voltages and '045 patent Voltages during programming

Nakai Node	Equivalent '045 Node	Nakai Voltage relative to Vss	'045 Voltage	Comment
BL (1)	BL0	0V	Logic Low Voltage	equivalent
BL (2)	BL1, BL2, BL15	10V (VDPI)	Logic High Voltage	not equivalent
Select Line SL (1)	BSL	12V	Logic High Voltage	not equivalent
Unselected Word Line	WL0	10V (VPI)	Logic High Voltage	not equivalent
Selected Word Line	WL1	20V (VPP)	Boosted Positive Voltage	equivalent
Selected Line SL (2)	SSL	0V	Logic Low Voltage	equivalent
Stack Ground	Stack Ground	0V	Vss (0V)	equivalent

60. “Equivalent” in Table 2 is used when the voltage that Nakai uses and the voltage specified by the '045 patent are similar. For example, 0V and “Logic Low Voltage” are equivalent, because the “Logic Low Voltage” includes 0V as a value. Likewise, 20V (VPP) and “Boosted Positive Voltage” are equivalent because “Boosted Positive Voltage” is a voltage above Vcc. Since Vcc is 5V in the Nakai patent, the 20V VPP is a “Boosted Positive Voltage,” defined in the '045 patent, because it is boosted above Vcc.

61. “Not equivalent” in Table 2 is used when the voltages in the Nakai patent and the voltages in the '045 patent are dissimilar. For the Nakai nodes BL(1), Select Line (1), and Unselected Word Line, the Nakai patent uses voltages that are boosted above Vcc (i.e., 10V, 12V, and 20V), whereas the '045 patent uses “Logic High Voltage,” which in the embodiments disclosed in the '045 patent is approximately equal to Vcc. ('045 patent. 6:37-53.)

62. The Nakai patent uses voltages that are boosted above Vcc for the BL (2), the Select Line SL (1), and unselected word lines. Nakai uses the term “voltage booster” to describe how several of these voltages are created (Ex. 1005, 20:14-33):

“In the data latch circuit shown in FIG. 13, the potential of the power source VBITH of the latch circuit for the data register changes from the external power source potential Vcc to the power source VDPI potential (10 V) supplied from the **voltage booster** built in the chip, and the signal BLCD changes from 0 V to the internal power source potential 12 V. Under these conditions, the node BLj of the data register connected to the defective bit line becomes "H" level by the preset operation. Therefore, the P-channel transistor of the clocked inverter CINV6 becomes conductive to flow a leakage current from the power source VBITH to the ground. The power source potential VDPI supplied from the **voltage booster** has a small current supply capability, generally of 1 mA or smaller. Therefore, as the leakage current flows through the defective bit line, the power source VBITH potential becomes lower than 12 V. The potentials of other write inhibit bit lines also become lower than 12 V, causing an erroneous data write.”

63. I understand that the voltage boosters mentioned in Nakai, above, are also known as voltage generators or charge pumps in the industry. Nakai discloses these pumps in both the specification and in its Fig. 1, where Nakai discloses the “VPP, VPI, VDPI Voltage Generator Circuit.”

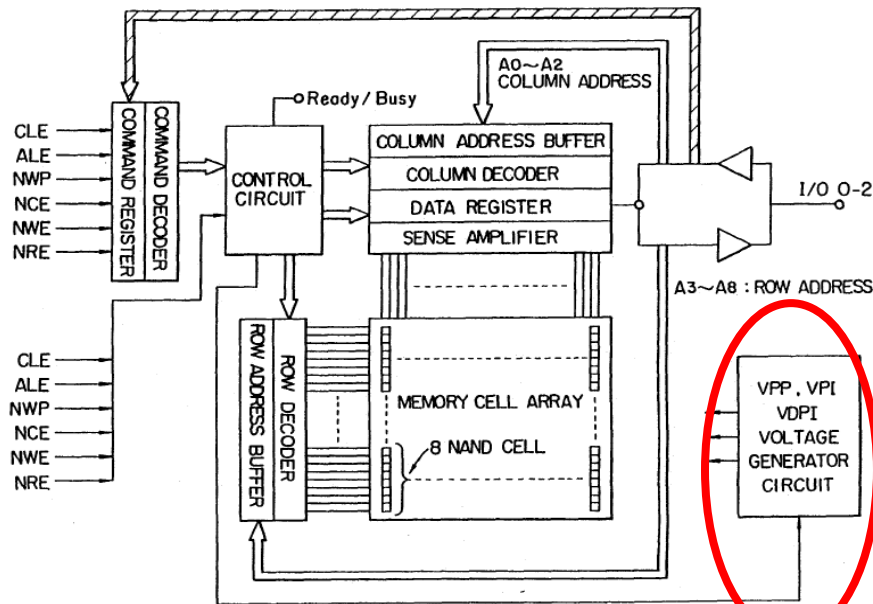


FIG. 1

64. Unlike Nakai, the '045 patent uses logic high voltages which are, per the specification, nominally Vcc. ('045 patent, 6:36-56.) Thus, these voltages are not the same as Nakai's boosted positive voltages.

Advantages of the '045 patent's lower voltages

65. From a technical perspective, the differences in the voltages used in the '045 patents programming scheme and Nakai's programming scheme is significant. The Nakai patent requires three different boosted positive voltages for

programming, whereas the '045 patent requires only one. Generating Nakai's multiple boosted positive voltages requires additional circuitry, which undesirably increases silicon area and power consumption. Thus, the '045 patent is superior in that regard.

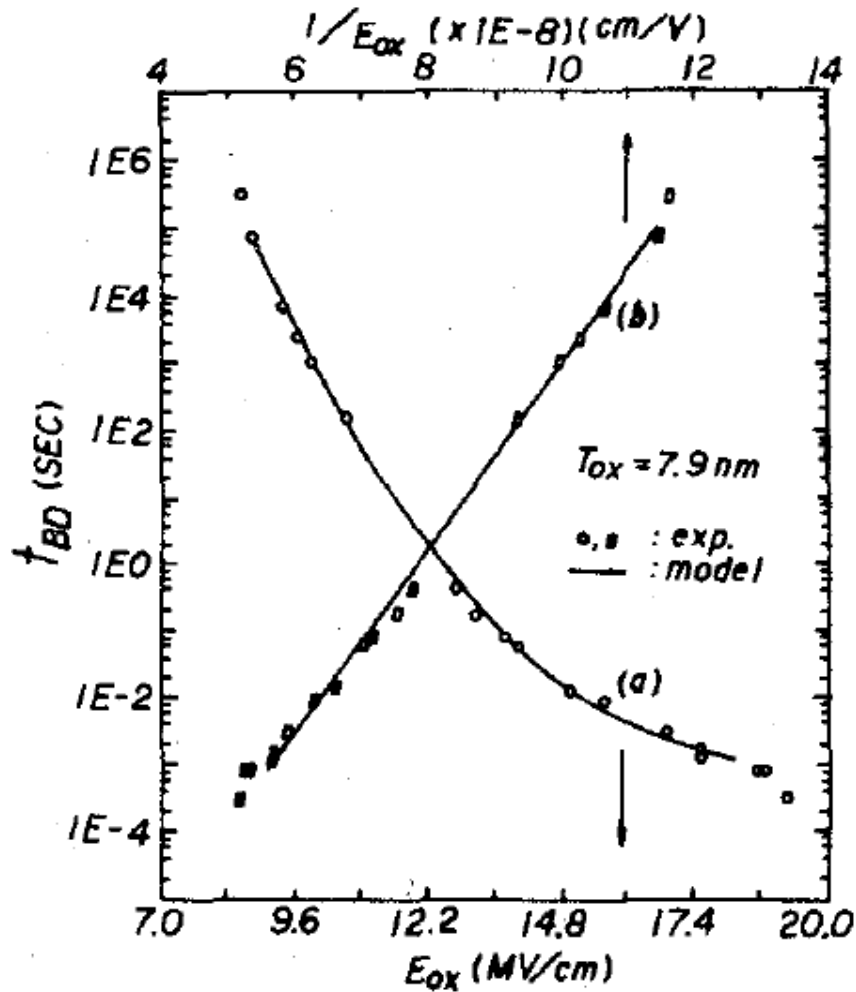
66. Furthermore, the '045 patent programming scheme allows lower voltages to be seen across the tunneling oxide of the unselected word line bits. This is important because a NAND FLASH failure mechanism, called write disturb, becomes worse when the voltage of the unselected wordlines is increased:

“Write disturb: The writing of a page requires high voltages to be applied to the cells in a page. These high voltages might affect neighboring cells and overwrite those cells, and if this happens, the error can remain undetected. The adjacent pages have to rely on the ECC in order to detect and correct this write induced error.” (Ex. 2010, Sanvido, p. 1867.)

67. The lower voltages on the unselected word lines thus reduce the probability of write disturb problems. This also reduces the overall stress on those gate dielectrics, thereby increasing reliability.

68. Lowering the overall voltages applied to selected or unselected word lines also improves overall tunnel oxide reliability. Specifically, Chen evaluated the time to oxide breakdown for a constant electric field (voltage/oxide thickness) in order to determine the lifetime of the oxide. (Ex. 2011, Chen, p. 340.) Chen's graph of a 79A oxide, which is comparable to the oxide thickness of the tunnel oxide used in FLASH EEPROM's, shows that lowering the voltage across the tunnel oxide by $\sim 0.8V$ increases the time to breakdown by an order of magnitude:

Figure 4: Time-to-breakdown versus Eox (Voltage) for a 79A oxide (Chen)



69. Reducing the voltages across the unselected word lines, as the '045 patent teaches, reduces the overall stress on those gate dielectrics, thereby increasing reliability.

Conclusion

70. In conclusion, there are significant and technically relevant differences between Nakai's scheme for programming a flash memory array, and the programming scheme claimed by the '045 patent. Nakai requires the application of multiple boosted positive voltages to corresponding multiple nodes of its memory array, during the programming mode of operation. The '045 patent requires only one boosted positive voltage during its programming mode of operation, and is able to use logic high voltages (e.g., V_{cc}) for the other nodes where Nakai requires boosted positive voltages. The '045 patent's programming significantly improves flash memory products. The reduced voltages used in the '045 patent improve reliability and endurance by reducing stress on the transistor dielectric layers. And the elimination of the requirement for multiple boosted positive voltages during the programming mode of operation reduces the amount of power consumed by these operations.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the '045 patent.

Executed this 10th day of July 2014 in Palo Alto, CA.

Respectfully submitted,



John E. Berg

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