UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TOSHIBA CORPORATION,

Petitioner,

VS.

Case: IPR2014-00113 U.S. Patent No. 6,058,045

INTELLECTUAL VENTURES I LLC,

Patent Owner.

/

VIDEOTAPED DEPOSITION OF

ROBERT J. MURPHY

Tuesday, June 17, 2014

REPORTED BY: RACHEL FERRIER, CSR 6948

(SF-002971)

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1	BE IT REMEMBERED that, pursuant to the
2	laws governing the taking and use of depositions, on
3	Tuesday, June 17, 2014, commencing at 9:31 a.m.
4	thereof, at DLA Piper LLP, 2000 University Avenue,
5	Room 107, Palo Alto, California 94303-2214, before
6	me, RACHEL FERRIER, a Certified Shorthand Reporter,
7	personally appeared ROBERT J. MURPHY, called as a
8	witness by Patent Owner, who, being by me first duly
9	sworn, was thereupon examined as a witness in said
10	action.
11	APPEARANCES OF COUNSEL
12	For the Patent Owner:
13	DESMARAIS LLP BV. ANDREW C. HEINZ Attornov. at Law
14	230 Park Avenue
15	Telephone: 212.351.3402
16	Email: aneinz@desmaraislip.com
17	For the Petitioner TOSHIBA CORPORATION:
18	DLA PIPER. BY: ALAN A. LIMBACH, Attorney at Law
19	2000 University Avenue East Palo Alto, CA 94303
20	Telephone: 650.833.2433 Email: alan.limbach@dlapiper.com
21	
22	
23	
24	
25	

1	APPEARANCES (Continued)
2	For INTELLECTUAL VENTURES I LLP
3	STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C
4	JON WRIGHT, Attorney at Law (via phone)
5	phone)
6	1100 New York Avenue, N.W. Washington, D.C. 2005
7	Telephone: 206.371.2600 Email: rwerner@skgf.com
8	ccamarce@skgf.com
9	
10	ALSO PRESENT: TED HOPPE, Videographer
11	JOHN BIRD, Intellectual Ventures
12	000
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Page 5 1 PALO ALTO, CALIFORNIA 2 TUESDAY, JUNE 17, 2014 3 9:31 A.M. ---000----4 5 PROCEEDINGS 09:30:29 6 7 THE VIDEOGRAPHER: Video is going, so let's 09:31:16 09:31:18 8 begin. 09:31:18 9 Here begins Video 1 in the deposition of 09:31:22 10 Robert Murphy in the matter of Toshiba Corporation 11 versus Intellectual Properties (sic) in the United 09:31:28 09:31:31 12 States Patent and Trade Office, Case 09:31:40 13 No. IPR 2014-00113. 09:31:42 14 Today's date is June 17th, 2014. The time on 15 09:31:48 the video monitor is 9:31. 09:31:51 16 The video operator today is Ted Hoppe. 17 This video deposition is taking place at the 09:31:54 18 Law Offices of DLA Piper, 2000 University Avenue, 09:31:57 Palo Alto. 19 09:32:02 20 09:32:03 Counsel, could you please voice identify 09:32:06 21 yourselves for the record. 2.2 MR. HEINZ: Andrew Heinz from Desmarais LLP 09:32:08 23 on behalf of the patent owner. 09:32:11 2.4 MR. LIMBACH: Al Limbach for Petitioner, 09:32:14 25 Toshiba Corporation. 09:32:17

Page 6 MR. COULMAN: Don Coulman for Intellectual 09:32:20 1 09:32:22 2 Ventures. 09:32:23 3 MR. WERNER: Ray Werner of Sterne, Kessler 09:32:26 for Intellectual Ventures. 4 MR. BIRD: John Bird for Intellectual 09:32:27 5 Ventures. 09:32:37 6 7 09:32:37 MR. HEINZ: Ray, can you -- can you introduce 09:32:38 8 the people on the phone. 09:32:40 9 MR. WERNER: Oh, yes, of course. 09:32:41 10 And on the phone Jon Wright of Sterne, 11 Kessler and Christian Camarce, Sterne, Kessler, both 09:32:45 09:32:49 12 for Intellectual Ventures. 09:32:49 13 THE VIDEOGRAPHER: Rachel, could you please 09:27:22 14 swear the witness in. 09:27:22 15 ---000---ROBERT J. MURPHY 09:27:22 16 17 09:27:22 18 called as a witness, having been 09:27:22 19 first duly sworn, was examined and 09:27:22 20 testified as follows: 09:27:22 09:27:22 21 ---000----2.2 THE VIDEOGRAPHER: Please proceed. 09:33:14 23 EXAMINATION 09:33:15 09:33:15 24 BY MR. HEINZ: 25 09:33:15 Q Good morning.

		Page	7
1	A	Good morning.	09:33:16
2	Q	Can you please state your name.	09:33:17
3	A	My name is Robert J. Murphy.	09:33:18
4	Q	Mr. Murphy, by whom are you employed?	09:33:20
5	А	I am employed in this with respect to	09:33:22
6	this m	natter or my my firm?	09:33:27
7	Q	Your firm, just your general employment.	09:33:29
8	А	Oh, my general employment is I have my own	09:33:31
9	busine	ess, Firenza, LLC.	09:33:35
10	Q	What is your business address?	09:33:36
11	А	My business does basically two types of	09:33:38
12	things	. It does design consulting for sem the	09:33:42
13	semico	onductor business, and it also does legal	09:33:46
14	legal	work for patent cases, mostly.	09:33:51
15	Q	What's the the street address of your	09:33:54
16	busine	ess? Where is it located?	09:33:56
17	A	It's 72 Fairview Plaza, Los Gatos, California	09:33:57
18	95030.		09:34:03
19	Q	Mr. Murphy, have you been deposed before?	09:34:06
20	A	I have.	09:34:09
21	Q	Approximately how many times?	09:34:09
22	А	I don't remember the exact number. More than	09:34:14
23	ten, I	think.	09:34:16
24	Q	So you know the rules of the road; you are	09:34:17
25	famili	ar with the process?	09:34:19

Page 8 А 09:34:20 1 I am. 09:34:22 2 MR. HEINZ: I've premarked some exhibits, and 09:34:23 3 I would like to go ahead and -- and hand you that 09:34:25 4 now. 09:34:26 5 Hand you Exhibit 10. (Exhibit 10 was marked for 09:34:27 6 7 identification by the Reporter.) 09:34:33 BY MR. HEINZ: 09:34:33 8 09:34:34 9 And Exhibit 10 is entitled "Notice of Ο 09:34:36 10 Deposition of Robert Murphy"? 09:34:41 11 А Yes, it is. That's you; right? 09:34:41 12 Q 09:34:42 13 А That is me. 09:34:43 14 MR. HEINZ: All right. That's what brought 09:34:45 15 us here today. 09:34:49 16 Okay. Looks like 11. 17 (Exhibit 11 was marked for 09:34:49 18 identification by the Reporter.) 09:34:49 BY MR. HEINZ: 19 09:34:49 20 09:34:49 0 Do you recognize Exhibit 11? 09:35:05 21 А I do. 2.2 What is it? 09:35:05 Ο 23 It's a petition for an inter partes review. 09:35:06 А 09:35:10 2.4 And it's the petition we're here to talk 0 09:35:12 25 about today; right?

			Page 9	
1	A	That is correct.		09:35:14
2		MR. HEINZ: This is Exhibit 12.		09:35:15
3		(Exhibit 12 was marked for		09:35:15
4		identification by the Reporter.)		09:35:16
5	BY MR.	HEINZ:		09:35:16
6	Q	Do you recognize Exhibit 12?		09:35:17
7	A	I do. It's my declaration in this matter.		09:35:26
8		MR. HEINZ: 13.		09:35:40
9		(Exhibit 13 was marked for		09:35:40
10		identification by the Reporter.)		09:35:40
11	BY MR.	HEINZ:		09:35:40
12	Q	Do you recognize Exhibit 13?		09:35:40
13	A	I do. It's a United States Patent		09:35:42
14	No. 6,	058,045, which is the patent in question in		09:35:44
15	this m	atter.		09:35:48
16		MR. HEINZ: And last, but not least,		09:35:57
17	Exhibi	t 14.		09:35:59
18		(Exhibit 14 was marked for		09:36:01
19		identification by the Reporter.)		09:36:01
20	BY MR.	HEINZ:		09:36:01
21	Q	Do you recognize Exhibit 14?		09:36:01
22	A	I do. It is also a United States patent.	It	09:36:02
23	is lab	eled Patent No. 5,297,029, and it is a prior		09:36:06
24	art pa	tent in this matter.		09:36:14
25	Q	And just to provide some framework for		09:36:15

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1	discussion, so in this matter, y	ou understand that	09:36:19
2	Toshiba alleges that Exhibit	the '045 patent that	09:36:22
3	you mentioned before, 6,058,045,	is the Intellectual	09:36:31
4	Ventures patent that's being cha	llenged, and the	09:36:36
5	Nakai patent, which bears the nu	mber 5,297,029, is	09:36:40
6	the asserted prior art reference	in this case?	09:36:46
7	A Yes.		09:36:49
8	Q And it's your view that t	he can we let	09:36:49
9	me strike that.		09:36:52
10	For the purposes of this	deposition, is it	09:36:54
11	okay if we refer to those as the	"'045 patent" and	09:36:56
12	the "'029 patent," respectively?		09:36:58
13	A Yes.		09:37:00
14	Q And it's your view that t	he '029 patent	09:37:01
15	anticipates claims 1 and 4 of th	e '045 patent; is	09:37:04
16	that right?		09:37:08
17	A Yes, it is.		09:37:08
18	Q I would like to start out	by asking about	09:37:09
19	some terminology that I expect i	s going to come up	09:37:19
20	in the questioning today, and I	would like to start	09:37:22
21	out by asking you about EEPROM a	nd flash.	09:37:26
22	A Yes.		09:37:32
23	Q Are those the same thing?		09:37:32
24	A No, I don't believe they	are the same thing.	09:37:38
25	Q What's the difference?		09:37:40

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1	A The difference is related to how many how	09:37:42
2	many cells you can erase at the same time. That's	09:37:47
3	probably, I think, the big I think the biggest	09:37:52
4	difference.	09:37:54
5	Q Is it the case that flash is a subset of	09:38:01
6	EEPROM, but not the the reverse of that?	09:38:05
7	A Is it the case I don't know whether I	09:38:07
8	would call it a subset of it or not. It's	09:38:27
9	definitely different.	09:38:30
10	Q Let me ask you to refer to your declaration,	09:38:30
11	which is which exhibit number? Is that up? Sorry.	09:38:33
12	A 12.	09:38:35
13	Q 12.	09:38:37
14	And to paragraph 22, please.	09:38:42
15	The first sentence of paragraph 22 reads:	09:38:51
16	It was well known to those skilled	09:38:55
17	in the art that NAND-type EEPROMs	09:38:57
18	were commonly referred to as "flash	09:39:05
19	memory" for their ability to program	09:39:06
20	and erase multiple memory cells at	09:39:09
21	once.	09:39:11
22	Is that statement accurate?	09:39:13
23	A I believe it is, yes.	09:39:14
24	Q So it's your view that NAND-type EEPROMs were	09:39:15
25	commonly referred to as "flash memory"?	09:39:21

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1	A	Yes.	09:39:23
2	Q	Are there other types of EEPROMs that are	09:39:24
3	referr	ed to as "flash memory"?	09:39:30
4	A	There are there are NOR types.	09:39:41
5	Q	So there would be NOR-type EEPROMs that would	09:39:42
6	also b	e referred to as "flash memory"?	09:39:45
7	A	Yes, they could.	09:39:48
8	Q	Any others?	09:39:49
9	A	Nothing comes to mind right now, no.	09:39:50
10	Q	Other than the NAND-type EEPROMs and the	09:39:54
11	NOR-ty	pe EEPROMs, are there other types of memory	09:40:00
12	that w	ould be referred to as "flash memory"?	09:40:05
13	A	I think in the normal usage of the term for	09:40:09
14	one of	ordinary skill in the art, those two types	09:40:21
15	define	most of the flash memory that one of ordinary	09:40:24
16	skill	in the art would would talk about.	09:40:26
17	Q	Can you think of any other types that would	09:40:28
18	be cor	ner cases or would be an exception to that	09:40:30
19	rule?		09:40:33
20	A	No, not right now at this time.	09:40:33
21	Q	Next I would like to ask you about the term	09:40:41
22	"boost	ed," which shows up in the patent and one of	09:40:47
23	the cl	aim some of the claim constructions.	09:40:51
24		What does "boosted" mean in the in this	09:40:52
25	contex	t?	09:40:55

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1	A In the context of the '045?	09:40:55
2	Q Yes.	09:40:58
3	A Boosted is talked about in the patent in the	09:40:59
4	specification. Let me see if I can find the exact	09:41:17
5	spot for you.	09:41:25
6	With respect to at least one of ordinary	09:41:35
7	skill in the art would understand that boosted is	09:41:38
8	talked about in the patent with respect to the	09:41:40
9	programming operation, around column 7 at line 26,	09:41:43
10	where it says, "The programming operation is done by	09:41:48
11	applying a high voltage (for example, 15 to	09:41:52
12	20 volts) on the selected word line (WL1)."	09:41:56
13	And, generally, one of ordinary skill in the	09:42:04
14	art understands that, in this time frame, that was	09:42:06
15	not the 15 to 20 volts applied was not an	09:42:10
16	external voltage applied to the part. It was a	09:42:15
17	voltage created within the part and generally by	09:42:17
18	circuits called "boost circuits" or "pump circuits"	09:42:21
19	that raised that voltage up above the normal	09:42:25
20	operating voltage of the part.	09:42:29
21	Q So just to make sure the record is clear, so	09:42:32
22	I think I understood you, but what does the term	09:42:36
23	"boosted" mean, then, in the context of the '045?	09:42:39
24	A Well, in terms of the '045, a a boosted	09:42:42
25	voltage is called out specifically, for example, at	09:42:54
		1

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1	the at the end of claim 1 where it says, "while a	09:43:00
2	boosted positive voltage is applied to a selected	09:43:05
3	word line."	09:43:07
4	And the the same almost the same	09:43:13
5	language is found in claim 4, at the end of claim 4,	09:43:16
6	where it says, "while a boosted positive voltage is	09:43:20
7	applied to a selected word line."	09:43:23
8	And with reference to those two cites in the	09:43:26
9	claims, one of ordinary skill in the art would look	09:43:32
10	to the specification and see that, as I talked about	09:43:35
11	before, column 7, line 26, "The programming	09:43:40
12	operation is done by applying a high voltage (for	09:43:44
13	example, 15 to 20 volts) on the selected word line	09:43:50
14	(WL1) and grounding the selected bit line (BL0),	09:43:57
15	while the unselected bit lines (BL1-BL15) are at	09:44:10
16	Vcc," and that specifically shows that that that	09:44:22
17	that voltage, 15 to 20 volts, is applied to the	09:44:29
18	selected word line during programming.	09:44:33
19	And then referencing back to claim 1, we look	09:44:35
20	to the language that prefaces the application of the	09:44:42
21	voltages, and we see a phrase that says, "wherein,	09:44:47
22	during" program (sic), and then the last phrase, "a	09:44:51
23	logic high voltage is applied to unselected word	09:44:59
24	lines, while a boosted positive voltage is applied	09:45:00
25	to a selected word line."	09:45:03

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1	And that same basic language appears in	09:45:05
2	claim 4 where the programming language has been	09:45:13
3	changed to "wherein programming memory cells is	09:45:18
4	accomplished by the steps of."	09:45:22
5	Q I appreciate you telling me that, but that	09:45:26
6	was not my question.	09:45:27
7	A Oh.	09:45:28
8	Q Let me see if I can ask my question again.	09:45:29
9	What does the term "boosted" mean in the '045	09:45:31
10	patent?	09:45:35
11	A The term "boosted" means that you are have	09:45:35
12	a voltage that you have to have a special circuit to	09:45:42
13	get this particular voltage to apply it to a	09:45:51
14	selected word line during programming.	09:45:54
15	Q The next term I would like to ask about is	09:45:59
16	Vss. That shows up in both patents, I believe.	09:46:01
17	What is "Vss"?	09:46:05
18	A One of ordinary skill in the art understands	09:46:07
19	Vss to normally be ground.	09:46:10
20	Q What is "Vcc"?	09:46:12
21	A Vcc is normally understood by one of ordinary	09:46:15
22	skill in the art to be the power supply for the	09:46:20
23	product in question, and since this part is at least	09:46:25
24	in the embodiment this is all directed to an NMOS	09:46:30
25	part Vcc is the voltage applied, commonly called,	09:46:35

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1	from the old days, the "collector voltage," but	09:46:42
2	it's it's the main power supply voltage of the	09:46:45
3	part.	09:46:47
4	Q Then I would like to ask you about volatile	09:46:49
5	versus non-volatile memory.	09:46:52
6	First let me ask you: What's the difference	09:46:55
7	between those terms?	09:46:58
8	A A volatile memory is one in which the data	09:46:58
9	stored in the device is lost either when the device	09:47:05
10	is operating, because you didn't operate the device	09:47:14
11	correctly, or is lost when the device has its power	09:47:21
12	removed and the data is lost.	09:47:26
13	Q How about a non-volatile memory?	09:47:29
14	A A non-volatile memory is a memory that	09:47:32
15	actually will store the data that's been placed into	09:47:36
16	it even when the power is removed from the device.	09:47:39
17	Q Can you provide some examples of volatile	09:47:41
18	memories?	09:47:44
19	A A volatile memory of the type I first	09:47:44
20	described, where if you operate the part	09:47:51
21	incorrectly, you lose the data, would be a DRAM in	09:47:55
22	that if you don't refresh it every so often, the	09:48:00
23	data will go away.	09:48:03
24	The second type I mentioned would be like an	09:48:05
25	SRAM. It doesn't require refresh, but if you remove	09:48:08

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1	the power from actually either the SRAM or the DRAM,	09:48:14
2	the data will disappear.	09:48:18
3	And those are two examples of volatile	09:48:22
4	memory.	09:48:24
5	Q How about some examples of non-volatile	09:48:25
6	memory?	09:48:28
7	A Well, there can be many types of non-volatile	09:48:28
8	memory. I guess it depends upon how broadly you	09:48:38
9	want to how broadly you want to let memory be.	09:48:41
10	Q Please explain the the distinction there.	09:48:49
11	A Well, I think one of ordinary skill in the	09:48:50
12	art understands that a memory is something you put	09:48:52
13	data into and then you get data back from, and there	09:48:56
14	can be many devices which are memory. And over the	09:49:00
15	50- or 60-odd years that we have in the business	09:49:03
16	doing this stuff, there are lots of various ways to	09:49:06
17	do it.	09:49:10
18	For instance, you can put information on a	09:49:12
19	magnetic tape and retrieve it later. That may	09:49:14
20	qualify as a memory from that point of view. You	09:49:18
21	there used to be an old way I've heard of	09:49:24
22	recording information on a wire. I think it was	09:49:26
23	magnetic, but I don't really recall that well.	09:49:31
24	That that would be another way of memory. You	09:49:34
25	know, this is using the very broad concept of a	09:49:42
1		1

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1	memory device, so a CD-ROM, for instance, could be a	09:49:45
2	memory, if if you wanted to interpret it that	09:49:49
3	way. It it you write data on it somehow and	09:49:54
4	you read the data back later.	09:49:57
5	A read-only memory is a type of chip that you	09:50:01
6	put data into, usually, but not always, through a	09:50:03
7	manufacturing process, and then you read it back	09:50:08
8	later.	09:50:10
9	Some memories are electrically programmable,	09:50:13
10	like a UV-EPROM, written electrically, erased with	09:50:16
11	ultraviolet light, so there are some examples.	09:50:23
12	Q So the examples you provided included	09:50:26
13	CD-ROMs, magnetic tapes.	09:50:29
14	Those were two examples you just provided;	09:50:30
15	right?	09:50:32
16	A I did, yes.	09:50:32
17	Q Computer hard drive, would that be an example	09:50:33
18	of non-volatile memory?	09:50:36
19	A Yes, I think so. It you write data to it,	09:50:37
20	and as long as you don't as long as you don't	09:50:41
21	mistreat it, it will still be there when you come	09:50:46
22	back to get it, hopefully.	09:50:48
23	Q The old floppy disks we might have carried in	09:50:50
24	the 1980s, those are non-volatile too; right?	09:50:53
25	A Well, yeah. You don't have to continuously	09:50:56

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		1
1	apply power to them to have them remember the	09:50:58
2	information stored on them, correct.	09:51:00
3	Q And flash memory is non-volatile memory too;	09:51:01
4	is that correct?	09:51:05
5	A Yes. It doesn't it doesn't lose the data	09:51:05
6	when you take the power away.	09:51:08
7	Q When you a few minutes ago, when we first	09:51:10
8	started talking about these memories, you had some	09:51:19
9	hesitation about the term "memory" and how broad or	09:51:22
10	narrow it should be.	09:51:24
11	In the context of the '045 patent and what we	09:51:25
12	are talking about today, do you feel that the	09:51:28
13	context we described is the appropriate breadth or	09:51:30
14	that it should be something different?	09:51:33
15	A Given the context of this patent, I think	09:51:34
16	the the the context is better served with the	09:51:41
17	concept of an integrated circuit type of memory, and	09:51:48
18	I think, in all of the claims, they specifically	09:51:54
19	talk about flash memory cells. So it seems like,	09:52:01
20	limiting it to one of ordinary skill in the art, I	09:52:05
21	think would would limit it to an integrated	09:52:09
22	circuit memory that has flash memory cells on it.	09:52:12
23	Q What's the maybe I'm just not	09:52:18
24	understanding, but what's the when you say an	09:52:20
25	integrated circuit memory that has flash memory on	09:52:23
		÷

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1	it, is that different are you trying to draw a	09:52:26
2	distinction between that and flash memory, or is	09:52:29
3	it I just want to make sure there's no	09:52:31
4	distinction there.	09:52:33
5	A Well, I don't know of a way you can create	09:52:34
6	flash memory without having it integrated onto a	09:52:38
7	chip. It it's possible that you could build a	09:52:42
8	single cell of flash memory, right? And that's	09:52:46
9	possible, but I don't I'm not aware of any other	09:52:51
10	flash memory cells that are built that are not	09:52:55
11	integrated circuits.	09:52:59
12	Q That's I was I think my I understand	09:53:04
13	the question now.	09:53:05
14	So we listed some examples of non-volatile	09:53:06
15	memory, but the non-volatile memory that's germane	09:53:11
16	here is particularly flash memory?	09:53:14
17	A Yes, I believe so.	09:53:18
18	Q I would like to draw your attention back to	09:53:19
19	your declaration, which is Exhibit 12.	09:53:30
20	So on page 3 of that exhibit in paragraph 7,	09:53:34
21	you describe some of the things you have worked on	09:53:41
22	during the course of your your career there.	09:53:44
23	Do you see that?	09:53:46
24	A I do.	09:53:47
25	Q I just want to make sure I understand what	09:53:47

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1	all those acronyms mean, because I was a little	09:53:50
2	unclear on those. So let I just want to walk	09:53:54
3	through them one at a time and just make sure we are	09:53:56
4	on the same page.	09:53:59
5	So the first one is E2CMOS and BiCMOS PALs;	09:53:59
6	is that right?	09:54:05
7	A Yes.	09:54:05
8	Q Can you explain what those are, please?	09:54:05
9	A So you previously were using EEPROM.	09:54:07
10	Q Uh-huh.	09:54:14
11	A Normally another term not normally, but	09:54:14
12	another term that people use is "e-squared,"	09:54:17
13	electrically erasable. So the first one is	09:54:20
14	electrically erasable CMOS PAL, which is a	09:54:24
15	Programmable Array Logic element, so it's a chip	09:54:28
16	that actually implements logic using an array of	09:54:32
17	flash cells. Okay? And because of the particular	09:54:37
18	structure of that part, the configuration typically	09:54:42
19	chosen for that was a NOR-type configuration.	09:54:47
20	A BiCMOS PAL is made with a completely	09:54:52
21	different technology. It has both bipolar	09:54:56
22	transistors on it and CMOS transistors on it, and	09:55:01
23	they are mixed together. In fact, I'm I was	09:55:04
24	lucky enough to make the first ever BiCMOS PAL, and	09:55:08
25	so you use a CMOS transistors in that to get	09:55:12

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1	functionality, and in certain places you use bipolar	09:55:17
2	transistors, like in the sense amplifiers and some	09:55:21
3	of the driver circuits because they are more	09:55:25
4	appropriate there, and so they are both Programmable	09:55:27
5	Array Logic types.	09:55:30
6	Q Are those memories, or would they be used as	09:55:32
7	memories?	09:55:36
8	A A PAL is not normally well, I got to be	09:55:39
9	careful about this, because the PALs actually have	09:55:43
10	registers on them, so you can actually store things	09:55:46
11	in them and then get them back later. So you could	09:55:49
12	use them as a memory. They would be very small, not	09:55:55
13	a lot of elements, but the function of what we	09:56:01
14	talked about in the broad sense of could you put a	09:56:04
15	piece of information in and then hold it there and	09:56:07
16	then retrieve it later, the answer is yes. But the	09:56:09
17	majority of the chip is logic-oriented.	09:56:14
18	Q What's a typical use case for one of those	09:56:18
19	components?	09:56:21
20	A A typical use case would be to take do you	09:56:22
21	know the term "TTL"?	09:56:28
22	Q No.	09:56:30
23	A Okay. So there was an older technology	09:56:31
24	called Transistor Transistor Logic which a lot of	09:56:35
25	systems that were built in the '70s and the '80s and	09:56:41

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the '60s even were built around TTL, and so TTL came	09:56:44
in the same little integrated circuit chip fashion,	09:56:49
and they were as small as four logic gates per chip,	09:56:57
so so you had a whole chip, meaning you needed a	09:57:03
power supply and you had power expended and you got	09:57:06
four whole gates.	09:57:10
So PALs came along when people decided, hey,	09:57:12
there's another way to do logic, and I can take 20	09:57:15
or 30 of these TTL guys and stick the logic function	09:57:18
into one PAL.	09:57:23
And so the the function for PALs the	09:57:25
general usage is what you asked for was mostly as	09:57:29
a replacement for multiple of these other TTL parts	09:57:32
to make the system less expensive, and because all	09:57:36
the logic was done on the integrated circuit itself,	09:57:45
the logic ended actually actually ended up being	09:57:48
faster. You didn't have to take a signal out of the	09:57:51
chip, drive it down the board, and then get it back	09:57:54

18 chip, drive it down the board, and then get it back onto another chip. And you did that all in one chip 19 20 and it goes faster.

Are you aware of anybody using these PALs 21 Ο 2.2 that you worked on as memory devices?

23 As a memory device. I don't think they would Α 24 call it a memory device. I think they would call it 25 a PAL. If you -- especially if you -- you are

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09:58:00

09:58:03

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09:58:15

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1	talking about comparing today or back then or?	09:58:23
2	Q Back then, either way.	09:58:27
3	A Either way.	09:58:28
4	Q What I'm what I'm trying to get at is:	09:58:29
5	Would you consider this to be a memory device or a	09:58:31
6	logic device?	09:58:34
7	A It's it's it's generally considered to	09:58:36
8	be a logic device; although, as I talked about	09:58:38
9	before, they have registers on them, and the	09:58:41
10	registers are memory elements, so.	09:58:43
11	Q If I was somebody around the time that you	09:58:47
12	were working on these things so they were	09:58:51
13	contemporary would I use that if I had a large	09:58:53
14	number of data files I needed to store somewhere	09:58:58
15	instead of a hard drive, for example?	09:59:00
16	A Oh, no. No. You wouldn't consider that. As	09:59:01
17	I said already, they have a few registers on them,	09:59:06
18	and those registers can store the result of a logic	09:59:10
19	operation and then deliver it later, so, no.	09:59:14
20	Q But they wouldn't be used for large-scale	09:59:19
21	storage, that type of thing?	09:59:22
22	A No.	09:59:23
23	Q The next thing you list is CMOS and NMOS	09:59:23
24	SRAMs?	09:59:30
25	A Yes.	09:59:31

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		1
1	Q Can you describe what those are, please?	09:59:31
2	A So an SRAM is a Static Random Access Memory.	09:59:33
3	It is a device and these and these, by the	09:59:39
4	way, are all integrated circuits. This is a device	09:59:43
5	that you put information into, and then later you	09:59:46
6	draw it out and it it's a memory.	09:59:51
7	"Random access" basically means that you can	09:59:55
8	pick in the in the space of the number of	09:59:58
9	addresses that the product has, you can pick any	10:00:03
10	address and sort of jump to any other address	10:00:06
11	without regard to how or where you jumped. Okay?	10:00:11
12	S static RAM is unlike dynamic. It's	10:00:18
13	a a part that does not need to be refreshed, so	10:00:22
14	it as long as the power is applied, it will hold	10:00:26
15	the data basically forever, barring some other	10:00:29
16	upset, like a cosmic ray, but it's it's you	10:00:34
17	don't have to a DRAM, you have to go back to	10:00:41
18	every so often and refresh the data; otherwise, it	10:00:45
19	will leak away. SRAMs don't have that problem.	10:00:48
20	And the two words in front of this word,	10:00:51
21	"CMOS," is a technology that involves having both an	10:00:53
22	N-channel device and a P-channel transistor. Those	10:00:58
23	two devices are both available to make the	10:01:02
24	functionality work. And an NMOS SRAM, it's a	10:01:04
25	simpler process, so it's less expensive, but you	10:01:09

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1	only get N-channel transistors to work with.	10:01:12
2	And so, for example, this is another area	10:01:16
3	that because of speed issues, for instance, you	10:01:26
4	might have occasion to use boosting circuits or pump	10:01:28
5	circuits in an NMOS SRAM.	10:01:32
6	Q Why would you need to use boosting circuits	10:01:35
7	in an NMOS SRAM?	10:01:39
8	A Well, the first reason is that the devices	10:01:41
9	the N-channel transistors will draw more current the	10:01:47
10	higher the gate voltage goes. So there are there	10:01:55
11	are circuit tricks that you can use to take the	10:02:00
12	normal power supply that's applied let's just	10:02:05
13	take an example of 5 volts and boost the 5 volts	10:02:08
14	up to 7 and a half or 8 volts and make the circuit	10:02:13
15	go faster. It's possible to do that. People	10:02:17
16	especially in the early days, people did do that.	10:02:21
17	The second was something that's probably more	10:02:25
18	common for or more often used for NMOS SRAMs, and	10:02:28
19	that is a pump circuit to provide a negative back	10:02:32
20	bias to the substrate of the part to literally make	10:02:37
21	the transistors have a better-controlled threshold	10:02:42
22	voltage and to make the transistors have higher	10:02:47
23	breakdown voltages.	10:02:53
24	So we would take in the external supply,	10:02:54
25	which was normally the SS would normally have	10:02:58

#### Page 27 10:03:02 been ground, and the Vcc or Vdd, depending upon 1 10:03:05 2 which terminology you want to use, it might be, 3 let's say, 5 volts. And then, from that, we would 10:03:08 create a minus-one-and-a-half volts that would be 10:03:11 4 10:03:15 5 put on the substrate of the device that would change the characteristics of the transistors and make them 10:03:18 6 7 faster, as I said, and then also raise their 10:03:21 10:03:25 8 breakdown voltage. 10:03:25 9 So it was for performance reasons and also Ο 10:03:31 10 control reasons; is that --11 А Yeah, I would -- I would say that's probably 10:03:35 10:03:37 12 the best match, yeah. 13 0 Is -- is 5 volts a common value for Vcc, in 10:03:38 10:03:42 14 your experience? 10:03:43 15 Α It's one of them. There are many others. 10:03:46 16 You just picked 5 there. 0 10:03:51 17 Why did you pick 5? 18 I picked 5 -- it's the -- it's the original 10:03:52 А 19 10:03:59 common voltage for TTL parts, and we talked about 20 TTL earlier. 10:04:02 21 If -- depending upon how far back you want to 10:04:06 2.2 go in history, original voltages probably were 15 or 10:04:09 23 12, and the technology wasn't NMOS, it was PMOS, and 10:04:15 10:04:20 24 so it wasn't 12 positive, it was 12 negative. 25 And then as the technology moves forward, the 10:04:24

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1	devices get smaller and smaller and smaller, so they	10:04:27
2	can support they can't support such big voltages	10:04:31
3	because the distance keeps getting smaller, so	10:04:36
4	the over over time, the well, over time,	10:04:41
5	starting from the old days moving forward, the power	10:04:43
6	supplies have consistently just gone down.	10:04:46
7	So today, for example, you might see people	10:04:52
8	using .7 volts or .75 volts as the Vcc or Vdd.	10:04:54
9	Q So, generally, as the components have gotten	10:05:01
10	smaller, the voltages, the Vcc-type voltages, have	10:05:05
11	gotten smaller as well?	10:05:09
12	A Yes, and that all comes from scaling theory.	10:05:10
13	Q SRAM is volatile memory; is that correct?	10:05:13
14	A Yes. If you take the power away, it forgets.	10:05:19
15	Q The last item here and I'm not sure if	10:05:22
16	this is one or two items, so bear with me.	10:05:30
17	Is CCDS something different from the second	10:05:33
18	thing?	10:05:37
19	A Yes.	10:05:37
20	Q So what is "CCDS"?	10:05:37
21	A Okay. Sorry. It's "CCDs"	10:05:39
22	Q Oh, I'm sorry.	10:05:42
23	A and they are charge-coupled displays, so	10:05:43
24	I've done both surface channel and buried channel.	10:05:47
25	This is where you put packets of charge into the	10:05:52
		1

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1	device and you it's it's a memory. And you	10:05:57
2	you store the charge in usually in a in a	10:06:07
3	linear fashion, so it goes in here, and then you	10:06:13
4	move it along, and then you can only detect it at	10:06:17
5	the end.	10:06:21
6	Q Like a register?	10:06:21
7	A Yeah, like a series of registers, actually,	10:06:23
8	correct.	10:06:26
9	But it's for instance, it's not random	10:06:29
10	access, because since I only have one detector, I	10:06:31
11	have to wait till the right address gets to here,	10:06:35
12	and then I can actually see the data. And then	10:06:39
13	so they used to operate them in a group of different	10:06:42
14	races. One was a race track. You put the data in	10:06:46
15	here and then it went down here. And then if you	10:06:48
16	wanted to remember it, you just put it around in a	10:06:51
17	circle and fed it back to the input and went back in	10:06:54
18	again.	10:06:58
19	So, effectively, you could see that bit.	10:06:58
20	Maybe the register was 512 bits long or 256 bits.	10:07:01
21	They had various, but you could only see that after	10:07:06
22	clocking that piece all the way around.	10:07:09
23	And the other thing that's unique about them	10:07:12
24	is they they don't just store digital memory,	10:07:15
25	they store analog memory also. So the you you	10:07:18

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1	literally could put an analog effectively, put an	10:07:23
2	analog voltage in by adjusting how much charge you	10:07:27
3	put into the input of the CCD and then save it until	10:07:30
4	later.	10:07:34
5	One example an easy example would be, you	10:07:36
6	can think of them as a delay line, right? So in	10:07:41
7	audio work, you awful (sic) you often hear of,	10:07:44
8	like, an echo effect where you shout into a canyon	10:07:49
9	and it comes back. Well, when you do that, you get	10:07:52
10	the you get the first audio instantly, and the	10:07:56
11	echo takes a certain amount of time to come back to	10:08:01
12	you and get another.	10:08:04
13	So the way they do that is they they give	10:08:05
14	you the first audio and they stick it into one of	10:08:07
15	these long shift-register CCDs. Then let it go	10:08:09
16	around in a circle and then present it back to you	10:08:13
17	and it sounds like an echo.	10:08:16
18	Q What would be a use case, a typical use case,	10:08:18
19	for a CCD?	10:08:21
20	A Oh, man, there are lots of uses.	10:08:22
21	So I've worked on hundred-megahertz radar	10:08:25
22	data in the '70s. I've worked on a projection	10:08:31
23	device, of all things; like, you know, you buy a	10:08:41
24	projector and you so in	10:08:45
25	Q Wait.	10:08:45
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1	Like for PowerPoints in a room and that type	10:08:47
2	of thing?	10:08:49
3	A Correct. And we were doing that in maybe '76	10:08:49
4	or '77?	10:08:52
5	We we so we made a we made a CCD,	10:08:56
6	and it had a serial register, and then you could	10:09:00
7	take that data and dump it into another set of	10:09:05
8	parallel registers going down, and then there was	10:09:09
9	another serial register at the bottom, so the the	10:09:14
10	term for them are "serial, parallel serial."	10:09:17
11	And so what we did is we filled up the front	10:09:22
12	register, the input register, and then stored it	10:09:24
13	into the array. And then once the array was full,	10:09:27
14	we pushed all that charge to the backside of the	10:09:31
15	wafer, and then on that side of the wafer, we read	10:09:36
16	the amount of charge using a laser.	10:09:39
17	Q And what was the the purpose was a	10:09:47
18	projection system; is that	10:09:49
19	A Well, that the laser was for the	10:09:50
20	hundred-megahertz radar data, and you could do real	10:09:52
21	time for a transform on that data with the system.	10:09:55
22	And then somebody else figured out that	10:09:56
23	instead of reading them with a laser, they could	10:09:59
24	just slap an LCD onto the back and the charge would	10:10:02
25	light up spots on the LCD and then you could hit	10:10:06

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1	it that with lamp and a lens, and on the wall	10:10:10
2	would be a TV picture.	10:10:13
3	So those are just two of the wacky examples	10:10:16
4	that I did at Hughes that so CCDs are a separate	10:10:21
5	thing.	10:10:25
6	The RAD Hard SOS/CMOS was specifically	10:10:26
7	radiation-hardened logic chips for outer space.	10:10:32
8	SO so RAD Hard means they are	10:10:43
9	radiation-hardened. You can put them in space; they	10:10:46
10	will still work. SOS is silicon on sapphire, so the	10:10:48
11	underlying material here is not a P-wafer or an	10:10:54
12	N-wafer, it's a piece of sapphire onto which a thin	10:10:57
13	EPI is built, and then the transistors are built on	10:11:02
14	the top. And it was well known that the sapphire	10:11:05
15	could take much more radiation than a regular wafer	10:11:08
16	and the and the parts would still function.	10:11:12
17	And so those were logic parts developed for	10:11:13
18	the Hughes Aircraft Company for some of their	10:11:16
19	spacecraft.	10:11:21
20	Q The CCDs, you mentioned that they had this	10:11:21
21	register concept, and you mentioned the use case.	10:11:26
22	Would people use CCDs as memory devices?	10:11:30
23	A Oh, yeah. Yeah. They well, for instance,	10:11:33
24	I gave an example of them as a memory device in the	10:11:37
25	delay line. You are remembering the actual analog	10:11:42
		4

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1	information over a period of time and then	10:11:46
2	delivering it back to the user.	10:11:50
3	Now, it was a type of memory that occupied	10:11:53
4	its particular marketplace. Was it standard usage	10:11:57
5	in a PC, for example? No. Was it standard usage in	10:12:01
6	systems that required its unique properties as a	10:12:06
7	memory? Yes.	10:12:09
8	Q And what were those unique properties that	10:12:10
9	enabled it to have certain use cases but not, for	10:12:13
10	example, be germane to the PC world?	10:12:18
11	A Probably the most unique property would have	10:12:19
12	been the ability of a CCD memory to deal with	10:12:25
13	electrical signals as elements of charge.	10:12:34
14	So, for instance, a good example would be	10:12:38
15	that CCDs were also used for filter functions and	10:12:43
16	a like a cone filter. I don't know if you know	10:12:48
17	what a cone filter is, but it's a it's a it's	10:12:51
18	an elec filter of electrical signals that has a	10:12:54
19	certain characteristic. And they were very	10:12:57
20	common they have very common usage in the '70s	10:13:00
21	and '80s for for that type of thing.	10:13:04
22	And to implement that filter, you put the	10:13:07
23	information in. You put the signal in, and you have	10:13:09
24	to store it for a while, and you have to break the	10:13:12
25	charge up into various packets, see if it matches	10 <b>:</b> 13 <b>:</b> 17

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1	the filter function, so it's a very unique type of	10:13:20
2	device. You wouldn't well, it was the '70s, so	10:13:25
3	nobody was storing music like in a flash device	10:13:30
4	today. You wouldn't ever store music in a CCD. And	10:13:35
5	CCDs are volatile. They they are built on DRAM	10:13:40
6	technology, basically well, sort of DRAM, dynamic	10:13:44
7	technology. And so you had to have the power	10:13:48
8	applied, so as soon as you turn the power off, it	10:13:51
9	forgets.	10:13:53
10	Q So CCDs are volatile; is that right?	10:13:54
11	A Yes.	10:14:02
12	Q And you said they are built on DRAM	10:14:03
13	technology; is that right?	10:14:05
14	A They're they're they're built on the	10:14:06
15	same concept that well, sort of the same concept.	10:14:09
16	DRAM stores its charge on a capacitor that is	10:14:14
17	literally built as a capacitor.	10:14:20
18	A CCD stores its charge in a potential well	10:14:23
19	that you create by manipulating the voltage on the	10:14:27
20	gate. So you put this voltage on the gate. You get	10:14:31
21	a potential well below it, and you either allow or	10:14:34
22	don't allow a certain measured amount of charge to	10:14:37
23	go into that potential well. So it's similar to,	10:14:39
24	let's just say.	10:14:47
25	Q So it's similar to but has some differences	10:14:48
		1

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1	than DRAM technology	10:14:51
2	A Yes.	10:14:52
3	Q the CCD technology you mentioned?	10:14:52
4	A Correct.	10:14:54
5	Q The radiation-hardened SOS/CMOS, that's not a	10:14:55
6	memory, is it?	10:15:04
7	A Well, here again, it's a logic it's a	10:15:04
8	logic part. But we built logic parts that had	10:15:08
9	pieces of memory on them, so it could be the	10:15:11
10	memory on them could be a group of registers, for	10:15:14
11	instance. I really don't remember if we built a	10:15:17
12	part that was just a memory. It's been too long	10:15:22
13	now. There's no reason we couldn't have. I just	10:15:25
14	can't remember if we did or not.	10:15:28
15	Q To the extent it would have had memory, to	10:15:32
16	the extent you remember, would it have been volatile	10:15:34
17	memory?	10:15:37
18	A Oh, yeah, it's a it's another it's	10:15:37
19	another part that's volatile. It's it's a part	10:15:40
20	where if you take the power away, the information	10:15:47
21	disappears.	10:15:49
22	Q I would like to move on to paragraph 29 of	10:15:58
23	your declaration.	10:16:02
24	You with me there?	10:16:17
25	A I am.	10:16:17

		Pa	age 36	
1	Q	The first sentence, in part, reads:		10:16:18
2		I have reviewed, had input into, and		10:16:24
3		adopt the analysis and claim charts		10:16:26
4		in the accompanying Petition for		10:16:29
5		Inter Partes Review of U.S. Patent		10:16:32
6		6,058,045.		10:16:34
7		Do you see that?		10:16:37
8	A	I do.		10:16:38
9	Q	I would like to ask you: What what did		10:16:38
10	you re	view? What did you have input into? And if		10:16:56
11	уои са	n explain to me how that process worked in		10:16:59
12	putting	g this together.		10:17:02
13	A	Well, the process began with well, the		10:17:04
14	the who	ole process began when I got hired and then		10:17:12
15	proceed	ded with me reviewing the documents, and then		10:17:16
16	that in	nvolved back and forth, give and take with		10:17:24
17	counse	l about their perceptions of certain things		10:17:29
18	and my	perceptions of certain things		10:17:34
19	Q	And let me just caution, I'm not asking abou	t	10:17:36
20	the com	nversations you had with your counsel.		10:17:38
21	A	and then they they started to coalesce		10:17:40
22	their :	ideas and talk to me about them as far as		10:17:58
23	whethe	r or not I would see one of ordinary skill in		10:18:03
24	the art	t seeing the same thing that they were lookin	g	10:18:09
25	at.			10:18:11
1	There were times when that I change	10:18:19		
----	--	----------		
2	that I changed some of the stuff for them in that	10:18:21		
3	you know, adjusted the understanding and explained	10:18:25		
4	why I thought one of ordinary skill in the art would	10:18:30		
5	see something different than maybe what they had.	10:18:34		
6	And then, eventually, that got to I don't	10:18:38		
7	know how many rounds we went on that. I don't	10:18:43		
8	remember, but, eventually, that that document	10:18:45		
9	the inter the petition sort of started coming	10:18:49		
10	together, and it was given to me to review and make	10:18:53		
11	sure that that it was accurate from my	10:18:56		
12	understanding from one of ordinary skill in the art	10:19:01		
13	and what somebody would would come to when	10:19:03		
14	when reading the the '045 patent.	10:19:07		
15	And then, eventually, it was it was done	10:19:11		
16	to their liking and my liking and off it went.	10:19:14		
17	Q And when you say you "adopt the analysis and	10:19:22		
18	claim charts in the petition," does that mean you	10:19:24		
19	are adopting the whole petition, or is that	10:19:29		
20	statement meant to cabin the portion that you are	10:19:31		
21	adopting?	10:19:34		
22	A No. There's no cabining. It's the whole	10:19:35		
23	petition.	10:19:39		
24	Q I would like to ask you to go back to the	10:19:52		
25	petition here.	10:19:52		

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1	A	Yes.	10:19:52
2	Q	Page 2?	10:19:53
3	A	Page 2, yes.	10:19:54
4	Q	The bottom of that page has a section	10:19:54
5	entitl	ed "Grounds for Standing." Oh, I'm sorry.	10:19:57
6	A	Oh, I'm on ii. Sorry.	10:20:00
7	Q	Yeah, the numeral 2.	10:20:03
8	A	Yes.	10:20:05
9	Q	You see that section?	10:20:10
10	А	I do.	10:20:12
11	Q	Do you know independently whether Toshiba has	10:20:13
12	ground	ls for standing?	10:20:17
13	А	Independently, I don't know, no.	10:20:19
14	Q	You didn't do anything to determine one way	10:20:22
15	or another whether Toshiba had standing in this		
16	case,	did you?	10:20:29
17	A	No. I relied on counsel for that	10:20:30
18	inform	nation.	10:20:32
19	Q	So you adopted this portion of the petition,	10:20:33
20	but yc	ou don't really know one way or the other	10:20:36
21	whethe	er it's correct; is that right?	10:20:38
22	А	I don't well, if if if Toshiba	10:20:39
23	doesn'	t have if Toshiba doesn't have grounds for	10:20:52
24	standi	ng, you know, from what I know about it, then	10:20:59
25	we wou	aldn't be here today.	10:21:04
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1	Q But you didn't know that when you adopted	10:21:05
2	this petition, did you?	10:21:07
3	A Well, I know it gen I knew it generally	10:21:09
4	that that somebody has to have a reason to do	10:21:11
5	this stuff, of course.	10:21:17
6	Q But you didn't know, under 37 CFR	10:21:19
7	Section 42.104(a), whether Toshiba had standing; you	10:21:26
8	just took your counsel's word for that, didn't you?	10:21:30
9	A That's correct.	10:21:32
10	Q Anything else in this petition that you just	10:21:33
11	took your counsel's word for?	10:21:44
12	A I don't recall. I don't think so. I don't	10:21:46
13	think so as of right now.	10:21:57
14	Q I would like to go back to your declaration,	10:21:58
15	and this time I would like to start on page 4,	10:22:09
16	paragraph 10.	10:22:13
17	You with me?	10:22:25
18	A I am.	10:22:26
19	Q This is a section about the background of the	10:22:26
20	'045 patent; is that right?	10:22:33
21	A It is.	10:22:34
22	Q I would like to start out with the second	10:22:34
23	sentence of paragraph 10, and it says:	10:22:41
24	In general, the '045 patent	10:22:42
25	describes a scalable flash memory	10:22:45

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Page 40 cell structure and a method of 10:22:47 1 10:22:49 2 manufacture. 10:22:49 3 Do you see that? 10:22:50 I do. 4 А 10:22:50 5 Is that statement accurate? Ο I believe it is. 10:22:52 6 А 7 Let me ask you just about the rest of the 10:22:58 0 10:23:01 8 statements in paragraph 10 regarding the subject 10:23:04 9 matter of the '045 patent. 10:23:07 10 All of paragraph 10 is accurate, as you sit 11 here today? You don't have any amendments or 10:23:10 12 10:23:12 adjustments to that? 10:23:13 13 А Right now, no. 14 10:23:15 So moving on to page 5, the last sentence of 0 10:23:23 15 that paragraph says: 10:23:26 16 I have been informed that only 17 claims 1 and 4 of the '045 patent 10:23:28 18 are subject to the inter -- this 10:23:30 19 10:23:32 inter partes review. 20 10:23:34 I'll stop there. That's your understanding; right? 10:23:35 21 2.2 А It is. 10:23:37 23 And it's also your understanding that 10:23:37 0 10:23:41 24 claims 1 and 4 are, continuing on: 25 Directed to the structural 10:23:44

Page 41 10:23:46 1 configuration of an array of flash 10:23:50 2 memory cells and the application of 3 certain voltages on various memory 10:23:51 10:23:54 4 array lines of the array to 10:23:56 5 implement memory cell program. That's right; right? 10:24:02 6 10:24:03 7 А I believe it is, yes. 10:24:04 8 And you agree with that statement -- it's 0 10:24:06 9 your statement; is that right? 10:24:06 10 А That's right. 11 0 So that represents your opinion about what 10:24:07 12 claims 1 and 4 are directed to? 10:24:09 Yes. 10:24:11 13 А 10:24:12 14 Do you want to take a break? I'm about ready 0 10:24:24 15 to switch gears, but if you -- happy to keep going. 10:24:26 16 А I'm cool. 10:24:27 17 0 Okay. I would like to go ahead and walk 18 through your CV, which you have attached to your 10:24:29 19 declaration. 10:24:31 20 10:24:42 And just for the record, this is Exhibit 10:24:47 21 1006, and I believe it's corrected Exhibit 1006; is 2.2 that right? 10:24:54 23 Your CV was originally not attached as filed, 10:24:55 24 and then the corrected exhibit was filed, so just 10:24:57 25 for the record, I want to make sure we have the 10:25:00

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1	right B	Exhibit 6 (sic)	10:25:02
2		MR. LIMBACH: This appears to be the correct	10:25:03
3	one.		10:25:05
4	BY MR.	HEINZ:	10:25:05
5	Q	Okay. So, Mr. Murphy, can you peruse that	10:25:05
6	and let	t me know if that's your CV?	10:25:10
7	A	Looks like it is, yes.	10:25:18
8	Q	All right. Before I start out, let me just	10:25:19
9	ask you	: You mentioned earlier you have been hired	10:25:22
10	to t	to work on this case on behalf of Toshiba.	10:25:25
11		What's your hourly rate that you are	10:25:28
12	chargir	ng?	10:25:30
13	A	450.	10:25:30
14	Q	Does it vary based on whether you are	10:25:32
15	testify	ying or whether you are doing general work?	10:25:36
16	A	No.	10:25:38
17	Q	Does it vary for any reason?	10:25:38
18	A	No.	10:25:41
19	Q	How much total time have you put in on this	10:25:41
20	case so	far, just an estimate?	10:25:45
21	A	I don't I don't have an estimate.	10:25:46
22	Q	Is it more than a hundred hours?	10:25:57
23	A	I don't think it's more than a hundred, no.	10:25:59
24	Q	Is it more than 50?	10:26:03
25	A	It might be, but I I haven't I haven't	10:26:05

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1	added it up.	10:26:11
2	Q But in the ballpark, somewhere 50 to a	10:26:12
3	hundred hours? Is that a reasonable estimate based	10:26:16
4	on what you know today?	10:26:19
5	A That would be a guess, yes.	10:26:20
6	Q Have you done work for Toshiba before?	10:26:22
7	A I believe I worked on one other Toshiba	10:26:28
8	thing. It's too long ago for me to remember what it	10:26:33
9	was.	10:26:40
10	Q What was the general nature of it, just to	10:26:40
11	the extent you remember?	10:26:42
12	A Some sem semiconductor thing, of course.	10:26:42
13	But it never went anywhere because the parties	10:26:47
14	settled, so that's why I don't really have a big	10:26:50
15	I remember I remember doing a very small expert	10:26:55
16	report, but I don't even know that it got filed, and	10:26:59
17	the next thing I heard was that, you know, the	10:27:02
18	case the case got settled and it went away and I	10:27:05
19	never did any more work on it than that.	10:27:09
20	Q So you have been an expert witness for	10:27:11
21	Toshiba once before; is that right?	10:27:15
22	A I believe only once, yeah. That's my	10:27:17
23	recollection.	10:27:20
24	Q Do you remember who the opposing party was?	10:27:20
25	A No.	10:27:23

1	Q	Have you ever worked for DLA Piper before?	10:27:24
2	A	Yeah, I have.	10:27:27
3	Q	How many times?	10:27:28
4	A	Maybe two or three, I think. I don't keep	10:27:29
5	track	of it. Sorry.	10:27:43
6	Q	Were those all litigation consulting?	10:27:44
7	A	As opposed to?	10:27:46
8	Q	Semiconductor consulting.	10:27:48
9	A	I haven't done any semiconductor consulting	10:27:52
10	for	at least what I consider semiconductor	10:27:55
11	consul	ting for DLA Piper, no.	10:28:01
12	Q	So your work for DLA Piper has been	10:28:04
13	litiga	tion consulting, and you estimate you have	10:28:08
14	worked	for them before two or three times?	10:28:10
15	A	That's my recollection, yes.	10:28:13
16	Q	I'd like to start out with your resume and go	10:28:15
17	throug	h it chronologically, starting from the	10:28:16
18	earlie	st date, which would be on page 5, I believe	10:28:17
19	of you	r CV?	10:28:20
20	A	Sure.	10:28:22
21		Sorry. I just saw something on page 1.	10:28:26
22	Q	Sure.	10:28:28
23	A	Well, there's a Toshiba versus Hynix ITC case	10:28:30
24	listed	there.	10:28:36
25	Q	This is toward the bottom of page 1 $$	10:28:36

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1	A	Towards the bottom	10:28:39
2	Q	you're identifying?	10:28:39
3	A	towards the bottom of page 1. It says	10:28:40
4	Q	Is that the case you were referring to	10:28:41
5	earlie	r?	10:28:45
6	A	Maybe. I mean, this is this is in	10:28:45
7	chrono	logical order, so it it was a while ago.	10:28:48
8	Q	It's a candidate, at least?	10:28:52
9	A	It is a candidate, yeah. I don't see any	10:28:53
10	other	Toshiba matters placed there, so.	10:28:56
11		I'm sorry. You wanted to start at 5?	10:29:00
12	Q	Yeah, let's start at the the earliest in	10:29:02
13	time,	and then we'll come forward to the present.	10:29:04
14	A	Okay.	10:29:07
15	Q	I would like to start out with your	10:29:10
16	educat	ion.	10:29:12
17	А	Sure.	10:29:12
18	Q	You have a B.S.E.E. from Drexel University?	10:29:13
19	А	I do.	10:29:17
20	Q	That you received in June 1974?	10:29:18
21	А	Correct.	10:29:20
22	Q	M.S.E.E. from UCLA?	10:29:21
23	A	Yes.	10:29:24
24	Q	Received in 1976?	10:29:24
25	А	Correct.	10:29:26
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1	Q Beyond the electrical engineering degree, did	10:29:26
2	you specialize in any particular fields during your	10:29:33
3	master's work, or was it more of a general	10:29:36
4	electrical engineering degree?	10:29:39
5	A It was specifically in electronics in	10:29:40
6	in at Drexel. And at UCLA, it was it was a	10:29:45
7	master's in EE in solid-state devices.	10:29:52
8	Q Did you study memory while you were there as	10:29:54
9	part of your work with either the electronics or	10:30:06
10	solid-state devices work?	10:30:09
11	A I'm sure there was some course matter that	10:30:10
12	had memory in it, certainly at the register level.	10:30:17
13	Whether we did whether we did full-blown memory	10:30:23
14	design at the time, I don't think that was part of	10:30:30
15	the course material, but you are you know, you	10:30:33
16	are asking me about something 40 years ago. So	10:30:36
17	so I would probably, if I was answering this, say	10:30:46
18	that I at that point in time at university, I got	10:30:48
19	maybe a slight introduction to memory, but I don't	10:30:55
20	think I got more than that.	10:30:58
21	Q So in the course of your education, you got a	10:31:01
22	slight introduction to memory, but not more than	10:31:04
23	that?	10:31:07
24	A I don't I don't believe so. I mean, they	10:31:07
25	may have described what memories were at very	10:31:11

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1	high-levels, but probably never down into the	10:31:15
2	details that I learned later.	10:31:18
3	Q We talked earlier about flash memory, which	10:31:20
4	is the subject of the patents that we are talking	10:31:27
5	about today.	10:31:30
6	When was flash memory invented, just a best	10:31:30
7	estimate?	10:31:33
8	A I think, generally, 1984.	10:31:33
9	Q So flash memory hadn't been invented yet at	10:31:36
10	the time you did your studies at UCLA and Drexel?	10:31:39
11	A That's right.	10:31:45
12	Q So, correspondingly, you didn't study flash	10:31:46
13	memory during your academic career because it hadn't	10:31:48
14	been invented yet; right?	10:31:52
15	A Correct.	10:31:53
16	Q So after your bachelor's degree, it looks	10:31:55
17	like you started at Hughes and then went to school	10:31:57
18	while you were working; is that right?	10:32:00
19	A Sort of. Drexel is a work/study school, so	10:32:02
20	first year and last year of a five-year school is	10:32:08
21	full-time school work. The other three years are	10:32:13
22	part-time; six months in school, six months in	10:32:17
23	industry, and I spent my time at the FAA facility	10:32:20
24	NAFEC, it was called at the time. I don't know if	10:32:27
25	it still exists at near Atlantic City, so	10:32:29

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1	and then when I left Drexel, I won a Hughes master's	10:32:33
2	fellowship, and I worked part-time at Hughes and I	10:32:36
3	got my master's degree at UCLA.	10:32:40
4	Q And in the course of your work at Hughes,	10:32:42
5	this is where you worked on the CCD memories that we	10:32:52
6	talked about earlier?	10:32:55
7	A Among other things, yes.	10:32:55
8	Q Did you work on any other memories while you	10:32:57
9	were at Hughes, beyond the CCD memories?	10:33:03
10	A Any other memories. I don't recall that I	10:33:05
11	did. I think mostly just the CCD memories.	10:33:16
12	Q And what rough percentage of your time from	10:33:24
13	June of 1974 to February of 1978 did you spend	10:33:30
14	working on those CCD memories?	10:33:34
15	A Well, let's see. We did a full chip design.	10:33:36
16	It's at least it's at least nine months of that	10:33:46
17	time. Might be longer than that. As I said, we may	10:33:51
18	have designed some some memory for this this	10:33:57
19	LSI using SOS/CMOS in a standard cell approach. I	10:34:02
20	just don't remember.	10:34:09
21	And let's see. The work in Canoga Park	10:34:10
22	was almost all analog or a mixed mixed-signal	10:34:17
23	work, so that was not memory per se. So I would say	10:34:22
24	9 to 12 months.	10:34:27
25	Q So 9 to 12 months of your period at Hughes	10:34:29

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1	were working o	n memory?	10:34:32
2	A Yes.		10:34:33
3	Q And it	was the CCD memory that we already	10:34:34
4	discussed?		10:34:37
5	A I belie	ve it was mostly that, yes.	10:34:37
6	Q And tha	t CCD memory is volatile memory; is	10:34:39
7	that right?		10:34:44
8	A That's	correct.	10:34:44
9	Q Let me	move on to your next position, which,	10:34:45
10	as it says her	e, is SRAM design manager at National	10:34:56
11	Semiconductor?		10:34:59
12	A Yes.		10:34:59
13	Q You wer	e there from February of 1978 to April	10:34:59
14	of 1982?		10:35:03
15	A Yes.		10:35:04
16	Q Can you	please describe your your duties,	10:35:05
17	generally, in	that position?	10:35:10
18	A Well, I	was originally hired to do CCD	10:35:11
19	memories, but	that program didn't last very long.	10:35:19
20	National kille	d it, wanting to spend more effort on	10:35:27
21	DRAMs, but in	between, we tried to we tried to	10:35:31
22	get the CCDs t	o be what you see there, called a	10:35:36
23	pseudostatic D	RAM.	10:35:40
24	And the	n when that project died, I moved over	10:35:44
25	into the SRAM	group, and I designed the first 4-T	10:35:47

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1	cell SRAM product for National. Part came out.	10:35:52
2	Worked the first time. Went to production on a	10:35:57
3	10 percent shrink, and I was promoted to be the	10:36:02
4	section head of the static RAM group.	10:36:05
5	Later, I took a the promotion required a	10:36:13
6	transfer, and so I transferred to the West Jordan	10:36:16
7	facility in Utah, and I was responsible for all the	10:36:20
8	static RAMs built in that fab, so it was a fab	10:36:25
9	downstairs and the design community upstairs. I	10:36:30
10	think peak production was 90,000 4-inch wafers a	10:36:36
11	month, of which SRAM I was responsible for about	10:36:39
12	30,000 designs that were for about 30,000 wafers	10:36:42
13	a month.	10:36:49
14	Q So when you began there, you were actually	10:36:49
15	designing the chips; is that right?	10:36:52
16	A When I began at National in I was in	10:36:55
17	Santa Clara, and I was actually designing chips,	10:36:57
18	correct.	10:37:00
19	Q When you moved to your management role, were	10:37:00
20	you continuing to do the design yourself, or were	10:37:04
21	you overseeing other designers who did the design?	10:37:07
22	A Yes. Both.	10:37:10
23	Q Okay. Both.	10:37:11
24	A Yes.	10:37:12
25	Q And you mentioned you worked on SRAM there	10:37:12
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1	and also, at the beginning, the pseudostatic DRAM	10:37:16
2	memory?	10:37:21
3	A Yeah, so that's what it was called, but	10:37:21
4	internally it was called a C CCD.	10:37:23
5	Q And both of those are volatile memories. We	10:37:25
6	already talked about that; right?	10:37:28
7	A That's correct.	10:37:29
8	Q Did you work on anything other than memories	10:37:30
9	while you were at National Semiconductor?	10:37:35
10	A You mean this time at National?	10:37:37
11	Q Is there another National Semiconductor?	10:37:40
12	A Oh, yeah.	10:37:43
13	Q Oh, there is. Okay. Yeah, let's just	10:37:44
14	let's cabinet to this time	10:37:46
15	A Sure.	10:37:46
16	Q the one from '78 to '82.	10:37:49
17	A I worked on other things, but more from a	10:37:53
18	point of view of how would you call this? How	10:38:01
19	would you call this? Assistance rather than owning	10:38:05
20	the design. So the the the the group	10:38:08
21	involved SRAMs, DRAMs, UV-EPROMs, NMOS first, then	10:38:12
22	CMOS.	10:38:23
23	And there was a group next door that did	10:38:24
24	microprocessor parts. And it was a small design	10:38:27
25	community. Let's see, my manager had maybe, I'm	10:38:32
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1	going to say, tops, 20 people, and the	10:38:37
2	microprocessor group maybe had another 15 or so.	10:38:44
3	The reason I say other things is that when	10:38:52
4	parts got into problem in the production line,	10:38:55
5	almost always everybody in the design community was	10:38:59
6	available to help, so I often got called in to,	10:39:03
7	effectively, consult on other people's problems, so	10:39:10
8	you not only learned about the products you were	10:39:15
9	making, you helped other people solve problems in	10:39:19
10	their products, right?	10:39:22
11	So I would say more intimately in the memory	10:39:23
12	group that I was in, so SRAMs, which was mine, DRAMs	10:39:29
13	and EPROMs, and then less less occasionally for	10:39:35
14	the microprocessor area.	10:39:42
15	Q What percentage of your time, roughly, would	10:39:43
16	you say was spent on SRAM and DRAM, your primary job	10:39:46
17	versus these other these other activities?	10:39:51
18	A Well, DRAM wasn't my primary job, but so	10:39:54
19	it was a another activity. I would say, in the	10:39:58
20	memory group itself, I probably spent up to an	10:40:01
21	average of 20 percent of my time on other products.	10:40:07
22	Usually all occurred in the same week, which meant	10:40:13
23	everything in SRAM stopped. We have a problem in	10:40:17
24	DRAM or we have a problem in $E-$ in the EPROM	10:40:20
25	area, and we throw all the resources over there and	10:40:23

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1	then we go fix it.	10:40:27
2	So they are estimates. I don't I don't	10:40:28
3	I don't believe it would be more than 20 percent.	10:40:34
4	Q Beyond the the DRAM project you mentioned	10:40:35
5	and the SRAM, which was your primary responsibility,	10:40:40
6	did you ever do any design work on EPROMs?	10:40:45
7	A Well, I definitely would say that I helped	10:40:51
8	with the sense amps, probably, and participated in	10:40:58
9	design reviews. So every when you are in such a	10:41:05
10	small community and you are sort of betting the	10:41:08
11	company that the design is going to work right.	10:41:12
12	Usually people like to get other people involved and	10:41:14
13	examine it's like sort of like having somebody	10:41:17
14	else read your brief. Same kind of thing.	10:41:20
15	Q Happens all the time.	10:41:25
16	A Same kind of thing, and so we would take all	10:41:27
17	the guys in the group, and there would be a	10:41:30
18	designer, so I sat through many design reviews of	10:41:30
19	EPROMs, CMOS EPROMs, and since the CMOS EPROM stuff	10:41:35
20	is in some ways some of the circuits are similar	10:41:40
21	to SRAMs we would try and collaborate like	10:41:43
22	especially on the sense amplifiers and the output	10:41:48
23	drivers and input buffers, we tried not to reinvent	10:41:50
24	them every time, because the schedules were so tight	10:41:53
25	that you didn't have time to reinvent them anyway,	10:41:56

1	so.	10:41:59
2	Q So you participated in design reviews on the	10:42:02
3	EPROMs, but you weren't the primary designer of the	10:42:06
4	EPROMs?	10:42:08
5	A No, but I was the resident I was the	10:42:08
6	resident sense amplifier guru, so I I "Come	10:42:10
7	over here and talk to me," you know.	10:42:14
8	Q So this period here, this this position	10:42:15
9	you left in 1982; right?	10:42:22
10	A Yes.	10:42:23
11	Q And that was before, we established, that	10:42:23
12	flash memory had been invented?	10:42:29
13	A That's correct.	10:42:29
14	Q So when you're the EPROMs you are talking	10:42:29
15	about were not flash memory per se; is that right?	10:42:31
16	A They were not at all. They were all U	10:42:34
17	UV-EPROMs.	10:42:35
18	Q Are UV-EPROMs memory?	10:42:36
19	A Oh, of course.	10:42:44
20	Q And can you explain how those work?	10:42:45
21	A Sure. They they you you program	10:42:47
22	them well, actually, first you erase them, so	10:42:55
23	unlike other semiconductors, they have a clear lid	10:42:59
24	on them. At the beginning, I think it was quartz,	10:43:02
25	but I don't really I'm not positive, but I think	10:43:06

1	it was quartz, and so you could literally see the	10:43:08
2	chip, right? And so you would put them in a small	10:43:12
3	unit that had an ultraviolet light in it, and that	10:43:18
4	light energy would go through the quartz cover and	10:43:21
5	it would erase the device.	10:43:26
6	Then you would take the device and put it in	10:43:30
7	a programming box, add your file that you wanted	10:43:32
8	programmed, and then it would program the device,	10:43:35
9	and then forever it was non-volatile forever.	10:43:38
10	Until it got hit with a lot of UV energy, it would	10:43:43
11	remember what you programmed it with, so that was	10:43:46
12	definitely a memory and definitely non-volatile.	10:43:49
13	Q And it was programmed with ultraviolet light;	10:43:51
14	is that right?	10:43:55
15	A No. I thought I told you it was erased.	10:43:55
16	Q Oh, erased with ultraviolet light	10:43:59
17	A Right.	10:43:59
18	Q but programmed through some other means?	10:44:02
19	A Right, because when you hit when you hit	10:44:04
20	the device with ultraviolet light, it goes	10:44:05
21	everywhere, so all the cells get to see the	10:44:08
22	ultraviolet light, so they all become the same, and	10:44:10
23	they are all erased, and then you specifically go in	10:44:13
24	and change certain of the other ones to enable the	10:44:16
25	pattern that you want in the memory to be resident.	10:44:21

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1	Q What was a typical use case back in that time	10:44:24
2	from EPROM?	10:44:31
3	A The typical use case, I think, would have	10:44:33
4	probably been for booting information.	10:44:36
5	Q Like in a computer?	10:44:44
6	A Like in a computer, right, depending upon	10:44:45
7	depending another usage would have been that your	10:44:52
8	whole if you could fit it, your whole program was	10:44:55
9	stored in in in this UV-EPROM, because they	10:44:58
10	were able to be changed relatively quickly. It took	10:45:02
11	about 20 minutes, I think, to erase them. Maybe a	10:45:06
12	half an hour.	10:45:09
13	But if you were building a product where, for	10:45:10
14	instance, the you wanted the ability to modify	10:45:12
15	the code later on, you literally just had to pull	10:45:15
16	the device out, erase it, reprogram it, stick it	10:45:22
17	right back in the socket and off you go. You would	10:45:26
18	have either new features or changes implemented into	10:45:27
19	the product you had.	10:45:31
20	So computer rebooting is one and and	10:45:33
21	and code adjustable or changeable code storage would	10:45:41
22	be another, I think.	10:45:43
23	Q Did they use EPROMs for data that needed to	10:45:44
24	get read and written very often?	10:45:54
25	A Well, in the case of a boot PROM, it	10:46:02

1	doesn't maybe once a day. It doesn't get written	10:46:04
2	very often, no.	10:46:06
3	And in the case of a variable code type of	10:46:07
4	thing, I guess it might depend upon the usage. So,	10:46:14
5	for instance, if you are trying to develop a system	10:46:18
6	and the code is stored in these EPROMs, you might	10:46:21
7	rewrite the code four, five times a day, for	10:46:25
8	example. Once the product was finished, you know,	10:46:30
9	maybe you changed the code once a year, once every	10:46:32
10	six months, or whenever you needed to.	10:46:37
11	Q So you could	10:46:40
12	A So it depends upon what you mean by "often."	10:46:41
13	Q It wasn't the case that it was marketed to	10:46:50
14	consumers as a memory device they could read and	10:46:51
15	write and store files on and erase files and that	10:46:53
16	type of thing? Is that the is that the case?	10:46:55
17	A So this is an integrated circuit that, at	10:46:56
18	that time, and even still today, requires that it	10:47:03
19	goes into a socket on a circuit board. They were	10:47:08
20	generally not marketed to consumers at all, but that	10:47:14
21	didn't make any difference because there weren't any	10:47:20
22	consumer uses at the time anyhow, so.	10:47:23
23	Q Fair enough.	10:47:25
24	Let's move on to your next position with RCA.	10:47:31
25	A Mm-hmm.	10:47:35
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1	Q And that was from April of 1982 to October of	10:47:36
2	1983; is that right?	10:47:39
3	A Correct.	10:47:40
4	Q Can you briefly describe your duties while	10:47:41
5	you were at RCA?	10:47:45
6	A So I was the project manager for a 64k-SRAM	10:47:46
7	product, and I had responsibility for the design,	10:47:50
8	the process, the preproduction, production, and	10:47:56
9	delivery of the part to the corporation so they	10:48:04
10	could sell it. So all of those all of those	10:48:07
11	activities actually, when I got there, all those	10:48:12
12	activities were were had people on them, but	10:48:15
13	they were all in different divisions, and so the	10:48:22
14	the CEO of the solid-state division at RCA hired me	10:48:26
15	in to knit all these people together as a single	10:48:31
16	entity and then make it happen.	10:48:38
17	Q How big was your team, was the team you just	10:48:41
18	mentioned?	10:48:45
19	A Well, around 15. That's my recollection.	10:48:45
20	Q So here you say you were responsible for the	10:48:49
21	team oh, 15 people. I see who developed the	10:48:57
22	process, did modeling, designed the circuits,	10:49:00
23	created the layout, and performed the testing.	10:49:02
24	So you oversaw those activities?	10:49:05
25	A Yeah, it's RCA had a very unique way of	10:49:08

1	doing things, so none of those people reported to me	10:49:12
2	directly, but they all worked on my program. So I	10:49:15
3	told them what the program needed, and they told me	10:49:19
4	what they could do, and then we haggled about when	10:49:22
5	it would get done, and but, yeah, I I had	10:49:25
6	done I had done very close I had a very close	10:49:33
7	interaction with the process development people at	10:49:38
8	National. Because to be a memory designer at	10:49:40
9	National, you had to know what the process was. You	10:49:43
10	just couldn't design memory and not know what the	10:49:46
11	process was.	10:49:49
12	And so I would the the guys developing	10:49:49
13	the process were actually at the David Sarnoff	10:49:55
14	Research Center in Princeton, and we talked. We	10:49:57
15	talked often. And I also the circuit designers	10:50:03
16	were there also. I was often in Princeton talking	10:50:09
17	to them, explaining to them how things were done	10:50:14
18	somewhere else versus how they were doing them. The	10:50:18
19	layout was done in Somerville. The preproduction	10:50:22
20	was done in Somerville. The manufacturing was	10:50:27
21	planned to be done in Florida, and the testing at	10:50:31
22	the beginning was done in Somerville, so I knit all	10:50:35
23	that together.	10:50:39
24	Q So you oversaw all those activities in your	10:50:40
25	role?	10:50:43

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1	A Yes. The the administrative aspects of	10:50:44
2	those people were still done in their own division.	10:50:49
3	Q Right.	10:50:52
4	They had their own division for that, but you	10:50:53
5	oversaw their work with regard to this product?	10:50:55
6	A That's correct.	10:50:57
7	Q Did you, personally, do any of the design	10:50:57
8	work for this product?	10:51:01
9	A Oh, yes.	10:51:02
10	Q Please explain.	10:51:04
11	A So I did most of the test chip work with	10:51:05
12	respect to teaching people things that were well	10:51:11
13	known on the West Coast but weren't known on the	10:51:16
14	East Coast, and so I was involved heavily in the	10:51:18
15	test chip.	10:51:24
16	Then I was involved heavily in the circuit	10:51:26
17	design for the real product, for the so the test	10:51:29
18	chip was a 4k, and the final product was a 64k. I	10:51:33
19	also I also taught people about polyfuses, and	10:51:40
20	that stuff that had been done at National before	10:51:48
21	hadn't been done at RCA yet. Same is true for	10:51:51
22	polyresistors.	10:51:55
23	So, yeah, I was sort of like a working	10:52:00
24	program manager, which is the way some people like	10:52:03
25	it, actually, but.	10:52:07

1	Q What percentage of your time would you say,	10:52:08
2	roughly, you spent doing this design work versus the	10:52:10
3	management responsibilities you had for the group?	10:52:12
4	A I would say I prob at least in the	10:52:15
5	beginning, I would say I probably did 60 percent	10:52:18
6	of my time was design work and 40 percent was	10:52:22
7	managing. And towards the end of it, because we	10:52:25
8	were getting ready to move the product to its final	10:52:30
9	production facility, then it was you know, by	10:52:33
10	then we had a working test chip and the 64k design	10:52:37
11	was doing pretty well, so I was doing less	10:52:41
12	managing I mean less circuit design and more	10:52:44
13	managing.	10:52:47
14	Q Because the design was effectively done by	10:52:48
15	that point, because you were building the new chip?	10:52:50
16	A Well, it wasn't done, but I think the I	10:52:53
17	think the sort of like any let's take an	10:52:58
18	example in your in your world.	10:53:00
19	You read a brief. You think about, in your	10:53:02
20	history, all the things that could go wrong or could	10:53:05
21	be a problem with briefs. You input that to the	10:53:08
22	people who actually wrote the brief, and you explain	10:53:12
23	why, and you are, effectively, giving them your view	10:53:14
24	of the elephant and as much as you can teaching,	10:53:20
25	right?	10:53:23

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1	I had done something at at at National	10:53:26
2	that the people all of the people at RCA had	10:53:29
3	never done. I had products in production at	10:53:32
4	National where, when we started a product, we	10:53:34
5	started 10,000 wafers. Nobody at RCA had ever done	10:53:39
6	that. None none of these people. They were more	10:53:44
7	in the well, the David Sarnoff Research Center at	10:53:46
8	Princeton was all research guys. If they made two,	10:53:50
9	they were doing really well.	10:53:53
10	But so the ins and outs of of the sort	10:53:56
11	of "gotchas" when you move to volume right? is	10:54:03
12	something that I could teach, and that also applies	10:54:05
13	to, "That's a really nice circuit, but in	10:54:10
14	production in production it won't work, and let	10:54:13
15	me show you why," right?	10:54:15
16	And, you know, that involves understanding	10:54:17
17	the circuitry, making sure the models of the	10:54:20
18	circuitry are right, making sure that they ran the	10:54:22
19	simulations correctly, and so it's a combin for	10:54:25
20	me, it was a combination of teaching, right? And	10:54:31
21	then and both ways. You guys do it this way.	10:54:35
22	Tell me why. Why did you do it that way? What was	10:54:38
23	special about it? You know, did you ever take it to	10:54:40
24	production? How many wafers a month did you run?	10:54:43
25	You get very jaded when you are in a factory that	10:54:46
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1	runs so many wafers, because just one little thing	10:54:49
2	can make your life a nightmare.	10:54:55
3	You walk in one day in the factory and you	10:54:57
4	see that there's the factory is running 90,000	10:54:59
5	wafers and 60,000 wafers are stuck at poly, and	10:55:03
6	it's, like, oh, no. No, no. No, no. You sort of	10:55:07
7	want to turn around and go home.	10:55:10
8	So it was this constant mix of doing circuit	10:55:12
9	design and doing managing and making sure the people	10:55:15
10	had the what they needed and then dealing with	10:55:20
11	the RCA hierarchy.	10:55:21
12	Q So the you did a little more design-level	10:55:23
13	work when you got there. I think you said	10:55:29
14	60 percent design level, and then that transitioned	10:55:31
15	as the products became closer to being produced to	10:55:34
16	more of this teaching and oversight role?	10:55:37
17	A No, the other the other way around. The	10:55:39
18	teaching was more in the beginning, and just like	10:55:41
19	the the the example with the brief, once you	10:55:44
20	have taught it all right? then, you know, you	10:55:47
21	don't I've told you that already, you know. If	10:55:52
22	you implement it right and it works and we test it	10:55:55
23	right and I'm I'm done. You know, we move on to	10:55:58
24	the next thing.	10:56:00
25	And so I would say, at the end, I spent more	10:56:01
		1

1	time doing management-oriented things, trying to get	10:56:05
2	everything aligned so that the part could actually	10:56:09
3	move into production, because at the time, the	10:56:12
4	production facility in Florida wasn't very good.	10:56:16
5	Q So at the beginning, you spent more time	10:56:21
6	designing and being involved in the design and	10:56:26
7	teaching, and then, toward the end, you transitioned	10:56:28
8	into more management-level things, making sure the	10:56:31
9	product got done	10:56:33
10	A Right.	10:56:33
11	Q is that fair?	10:56:34
12	A Yeah.	10:56:35
13	Q Other than the SRAM project that we have	10:56:36
14	discussed, did you work on any other projects at	10:56:43
15	RCA?	10:56:46
16	A I did not on a project per se, but I	10:56:47
17	had so this gets back to a knowledge sort of	10:56:52
18	thing, so I had more knowledge about ESD circuits	10:56:54
19	than the people at RCA did. They had some really	10:56:59
20	good ESD circuits for TV sets, because TV, you tend	10:57:02
21	to get pretty archy-type electrical characteristics,	10:57:07
22	but everything they had was not very amenable to a	10:57:12
23	standard integrated circuit flow.	10:57:16
24	And from National, because of the products I	10:57:19
25	made, they all had to be ESD robust, and so that was	10:57:22

1	another area where I so pretty soon people found	10:57:29
2	out, oh, you know about you know about contract	10:57:33
3	law. Next thing you know, you get a phone call, and	10:57:38
4	so I know I did some of that. But it was never from	10:57:41
5	my project because I had already told my guys how to	10:57:44
6	do that. And that's the biggest thing the	10:57:48
7	biggest other thing in RCA that I can remember	10:57:50
8	doing. It was something I did do at National, and	10:57:53
9	then I also so I helped other and and very	10:57:55
10	much like what I talked about in in Salt Lake	10:57:59
11	City, in West Jordan right? when you had a	10:58:03
12	problem, you started to seek out, well, who knows	10:58:05
13	who knows about this or who knows about that, and	10:58:07
14	once people found out I worked on these things, I	10:58:10
15	was I would be consulted. It's not a big deal.	10:58:13
16	I mean but it's not my project.	10:58:16
17	Q So just so the record is clear, ESD is	10:58:17
18	electrostatic discharge; is that right?	10:58:21
19	A Correct. Mm-hmm.	10:58:23
20	Q And other than that project, nothing comes to	10:58:24
21	mind in terms of other things you worked on at RCA?	10:58:27
22	A There wasn't really anything. This was	10:58:31
23	this was a lot.	10:58:33
24	Q And during this period this is still	10:58:33
25	before flash memory was invented; right?	10:58:44

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1	A	Correct.	10:58:47
2	Q	And SRAM is volatile memory, as we already	10:58:48
3	talked	about; right?	10:58:51
4	A	That's correct.	10:58:51
5	Q	You didn't work on any non-volatile memory	10:58:52
6	during	your time at RCA?	10:58:57
7	A	At RCA, non-volatile memory. I don't believe	10:58:59
8	so.		10:59:06
9		Andy Dingwall, I think, did most of that for	10:59:06
10	the la	os, which is the Princeton the David	10:59:11
11	Sarnof	f Research Center. Other than potentially	10:59:18
12	having	some conversations, no.	10:59:23
13	Q	Let's move on to your next position, which is	10:59:23
14	back to	o National Semiconductor.	10:59:27
15	A	Yes.	10:59:29
16	Q	And that position is senior engineering	10:59:29
17	manage	r, and you were there from October of 1983 to	10:59:34
18	Februa	ry of 1989; is that right?	10:59:38
19	A	That's correct.	10:59:40
20	Q	Can you briefly describe your duties in that	10:59:40
21	positio	on?	10:59:43
22	A	So, originally, I came back into the speech	10:59:43
23	group a	at National, and I seem to have this talent	10:59:53
24	for pic	cking groups that were about to die.	10:59:58
25	Q	What was the speech group? What do you mean	11:00:01

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1	by that?	11:00:03
2	A Literally, it was speech recognition. They	11:00:03
3	were going to make actually, they did make chips	11:00:06
4	that did both things.	11:00:08
5	So at the time, they would one example	11:00:09
6	would be they used phonetics, and they would a	11:00:14
7	computer voice that would say things for you. You	11:00:20
8	could program into it what you wanted to say and	11:00:22
9	phonetically it would say it.	11:00:24
10	And then the other corollary was: Okay. We	11:00:26
11	are going to have people speak into it and or	11:00:29
12	into a different chip, and it was going to recognize	11:00:31
13	what they said. So that was what I was originally	11:00:33
14	hired for, and National got out of that business	11:00:38
15	maybe six months after I got there. So a bunch of	11:00:42
16	people that I knew from my first tour there had now	11:00:52
17	moved on into a PAL group where they were doing	11:00:56
18	bipolar PALs, so this would be TTL and ECL PALs.	11:01:00
19	Q Like we talked about earlier when we were	11:01:05
20	talking about the technologies; is that right?	11:01:07
21	A Correct. ECL is Emitter Coupled Logic.	11:01:09
22	And at the time, they were what a great	11:01:15
23	group. They were printing money, selling bipolar	11:01:20
24	PALs. I mean, costs were really low. Product value	11:01:23
25	was really high, and they were one of the biggest	11:01:27

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contributors to the profitability of National that	11:01:30
they had.	11:01:35
The trouble was, some guys over here in the	11:01:35
valley had just invented CMOS PALs using ultraviolet	11:01:38
cells, and they were they could sort of see the	11:01:42
future that they needed to they needed to have	11:01:50
something. And their first entry into it was this	11:01:54
BiCMOS PAL.	11:01:59
So basically I ran that project to begin	11:02:04
with, and I took I stole as much as I could from	11:02:07
the bipolar arena and then wrapped it in a CMOS	11:02:13
wrapper, so it still had metal fuses in the core and	11:02:21
it still was a logic device, mostly, with registers,	11:02:27
and but it used a bipolar transistor to blow up	11:02:31
the fuses in the core, and that's how you programmed	11:02:36
the logic into it, but the ins and the outs were all	11:02:38
CMOS.	11:02:46
And then I stole from the SRAM world, I	11:02:46
stole a power-down feature, which bipolar PALs	11:02:49
didn't have, and so this part, the part we made, it	11:02:54
would actually power down you could power it	11:03:00
down. Like when you weren't using it, it drew	11:03:02
almost no power because it's CMOS. And so that part	11:03:05
was made, and I was I wrote a paper about it, and	11:03:09
it was presented at the ISSCC, which is the	11:03:15
	contributors to the profitability of National that they had. The trouble was, some guys over here in the valley had just invented CMOS PALs using ultraviolet cells, and they were they could sort of see the future that they needed to they needed to have something. And their first entry into it was this BiCMOS PAL. So basically I ran that project to begin with, and I took I stole as much as I could from the bipolar arena and then wrapped it in a CMOS wrapper, so it still had metal fuses in the core and it still was a logic device, mostly, with registers, and but it used a bipolar transistor to blow up the fuses in the core, and that's how you programmed the logic into it, but the ins and the outs were all CMOS. Mand then I stole from the SRAM world, I stole a power-down feature, which bipolar PALs didn't have, and so this part, the part we made, it would actually power down you could power it down. Like when you weren't using it, it drew almost no power because it's CMOS. And so that part was made, and I was I wrote a paper about it, and it was presented at the ISSCC, which is the

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1	International Solid State Circuits Conference in	11:03:18
2	San Francisco, and that was the first portion of my	11:03:22
3	stay here.	11:03:27
4	The second portion was that National had done	11:03:31
5	a deal with sorry. I'll have to remember the	11:03:34
6	name Lattice Semiconductor to be a second source,	11:03:40
7	and Lattic made an e-squared PAL, so it was	11:03:47
8	e-squared CMOS. It was electrically erasable, and	11:03:50
9	National had arranged this deal to second-source	11:03:53
10	first of all, second-source their products and	11:03:59
11	then and replicate, so replicate the process that	11:04:05
12	they used at the National facility in Salt Lake City	11:04:10
13	and let's see. Lattic was the foun fabless	11:04:19
14	semiconductor, and their foundry was Seiko Epsom, so	11:04:27
15	we replicated Seiko Epsom's process in first in	11:04:31
16	Santa Clara and then in the foundry in our	11:04:36
17	foundry in Salt Lake City, and and then on the	11:04:40
18	second part of the deal so that was the first	11:04:44
19	thing.	11:04:46
20	The first thing was to make Lattic's parts	11:04:46
21	using Seiko Epsom's process in at National, and	11:04:49
22	so we did that, and and you will see here, we	11:04:53
23	went from zero revenue to a million dollars a month	11:04:57
24	in 12 months, which wasn't bad.	11:04:59
25	And then the second part of it was to design	11:05:03

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1	new products that we would co-license with Lattic,	11:05:07
2	so we would design new products, and so I	11:05:11
3	participated. And by that time, I was running this	11:05:13
4	group, doing e-squared PALs.	11:05:17
5	Q So just to take those in chronological order,	11:05:19
6	so at the beginning, the BiCMOS PAL, it sounds like	11:05:24
7	you were heavily involved in the design of that one;	11:05:28
8	is that right?	11:05:32
9	A There was there was my I was the lead	11:05:32
10	engineer, and I had one junior guy and one layout	11:05:38
11	person or two layout people, yeah, so I was	11:05:42
12	pretty much everything.	11:05:46
13	Q And then in the the second-sourcing aspect	11:05:46
14	of that position, those were designs you got from	11:05:51
15	another company; right?	11:05:53
16	A That's right.	11:05:55
17	Q And then, finally, in the last portion that	11:05:55
18	you mentioned, when you were making the different	11:06:00
19	designs and, by that time, had been promoted, how	11:06:03
20	active were you in the design of those products?	11:06:06
21	A Yes, active, because you couldn't as a	11:06:09
22	manager at this level, even at senior engineering	11:06:14
23	manager, you still had to know all of this technical	11:06:18
24	stuff.	11:06:21
25	And then the part that you sort of glossed	11:06:22

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1	over was the concept of: Oh, you got these designs	11:06:24
2	from somebody else? Well, the process that those	11:06:28
3	designs ran in was at Seiko Epsom in Japan. That	11:06:33
4	process had to be transferred to the facility in	11:06:40
5	Salt Lake City I mean in Santa Clara first and	11:06:43
6	then Salt Lake City.	11:06:46
7	So we actually had to build some test chips	11:06:47
8	first, see if we could get our parameters to match	11:06:52
9	as closely to the parameters in Japan. Then we had	11:06:55
10	to take the design that was given to us from Lattic	11:07:00
11	and rework it all to make sure that it worked right,	11:07:04
12	given what our fab looked like versus what the Seiko	11:07:08
13	Epsom fab looked like.	11:07:13
14	So we actually reworked the the designs	11:07:14
15	given to us. You couldn't just make something with	11:07:17
16	them. You had to literally well, you had to	11:07:20
17	prove to the management that they were going to work	11:07:24
18	right, and that meant you had to do it all over	11:07:26
19	again. So that's what I did. It wasn't just the	11:07:28
20	simple, oh, yeah, get the designs and throw them in	11:07:30
21	and, hey, you are all done.	11:07:34
22	Q Ultimately, were the chips made in Japan and	11:07:35
23	the chips made by you the same? Were those fungible	11:07:40
24	or not?	11:07:44
25	A Well, they all met the same spec. You could	11:07:45

1	probably have an interesting discussion with people	11:07:50
2	about which one was better, but but they all sold	11:07:53
3	to the same specification in the data book.	11:07:59
4	Q Earlier, we talked about flash being invented	11:08:02
5	circa 1984.	11:08:09
6	Do you remember that?	11:08:11
7	A Yes.	11:08:11
8	Q That's during this period you were in this	11:08:11
9	position at National Semiconductor; is that right?	11:08:15
10	A That's correct.	11:08:17
11	Q Were you involved in flash memory during this	11:08:18
12	period? In other words, did you have any job duties	11:08:22
13	at National Semiconductor while you were here	11:08:29
14	related to flash memory, or were you involved in	11:08:32
15	some way in the initial designs of flash memory or	11:08:34
16	anything of that nature?	11:08:37
17	A Well, the product that I worked on is not a,	11:08:38
18	quote/unquote, flash memory, but the underlying	11:08:44
19	technology is all pretty much identical. So you	11:08:47
20	couldn't have you couldn't have designed a flash	11:08:54
21	memory without knowing everything I had to know for	11:08:58
22	the e-squared PAL. It still gets programmed and it	11:09:02
23	gets erased. Then you have bit lines and select	11:09:07
24	lines and boost circuits. They are all they are	11:09:11
25	all there.	11:09:15
		1
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1	Q So you worked on technology that's related or	11:09:18
2	used in flash memory; is that right?	11:09:22
3	A I don't think it's just related. I think	11:09:24
4	it's the same technology. I mean, the the for	11:09:27
5	ex for example, some of the flash devices we	11:09:35
6	talked about earlier have a NOR configuration on the	11:09:38
7	bit line. These PALs have a NOR configuration on	11:09:41
8	the bit line. Okay?	11:09:46
9	The the difference, if there is one, is	11:09:46
10	that they are not storing individual bits of data to	11:09:50
11	be read as data. They are storing indi	11:09:55
12	individual bits of information that will be used as	11:09:59
13	logic elements, if you will.	11:10:03
14	Q You did not work on flash memory at National	11:10:12
15	Semiconductor Corporation during this period of 1983	11:10:18
16	to 1989, did you?	11:10:19
17	A Well, no. This doesn't say that I worked on	11:10:21
18	flash memory. It says I worked on e-squared CMOS	11:10:26
19	PALs, which is what the products what they	11:10:29
20	what they built.	11:10:32
21	What I've told you is that the underlying	11:10:33
22	technology for the e-squared PAL in a flash device	11:10:35
23	are not different.	11:10:40
24	Q So it's your opinion that the underlying	11:10:42
25	technology of the e-squared CMOS PAL and flash	11:10:44
		1

1	memory are the same?	11:10:48
2	A Correct.	11:10:49
3	Q But you did not work on flash memory during	11:10:50
4	this period at National Semiconductor, did you?	11:10:55
5	A Not a product that was called flash memory	11:10:57
6	specifically, no, but the devices were the same	11:11:00
7	types of cells. They had thin oxide. They had a	11:11:05
8	select gate. They had bit lines. They were	11:11:08
9	organized on the bit lines. They had programming	11:11:10
10	voltages, so.	11:11:13
11	Q So the answer to my question is no?	11:11:16
12	A They were not called flash memories, that's	11:11:18
13	correct.	11:11:21
14	Q Did you work on any NAND devices while you	11:11:21
15	were at National Semiconductor?	11:11:26
16	A The only place that I think we may have used	11:11:27
17	a NAND would have been in the test circuitry put on	11:11:37
18	this PAL device, but as a NAND device, no, I did	11:11:40
19	not.	11:11:43
20	Q Let's move on to Weitek.	11:11:43
21	MR. LIMBACH: Would now be a good time for a	11:11:53
22	break?	11:11:55
23	MR. HEINZ: Sure.	11:11:56
24	THE WITNESS: If you guys want, that's fine.	11:11:57
25	THE VIDEOGRAPHER: Very good.	11:11:58

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1		Going off the record, the time now is 11:12.	11:11:59
2		(Recess taken.)	11:12:02
3		THE VIDEOGRAPHER: Back on the record.	11:32:59
4		The time now is 11:32. This also marks the	11:33:01
5	beginn	ing of Video 2.	11:33:04
6		Please continue.	11:33:06
7	BY MR.	HEINZ:	11:33:07
8	Q	Mr. Murphy, before the break, we were going	11:33:07
9	throug	h your CV.	11:33:09
10	A	Yes.	11:33:10
11	Q	And I believe we were up to the Weitek	11:33:10
12	A	Weitek, yes.	11:33:14
13	Q	position, and you held that position from	11:33:15
14	Februa	ry of 1989 to June of 1992; is that right?	11:33:18
15	A	That's correct.	11:33:22
16	Q	Your title was director of engineering?	11:33:23
17	A	Yes.	11:33:26
18	Q	Please describe your duties in that role.	11:33:26
19	A	Well, my duties here were, in many ways,	11:33:28
20	simila	r to places other places I had been. I	11:33:33
21	starte	d out as a design manager and had a	11:33:39
22	respon	sibility for an individual chip. It was a, as	11:33:42
23	they s	ay, working design manager position, meaning	11:33:48
24	that I	still did circuit design and still helped	11:33:51
25	people	understand the best ways to design their	11:33:57
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		1
1	circuits, so for this device, I did some memory	11:34:01
2	portions of it, the output drivers and the ESD. The	11:34:12
3	device was a floating point co-processor.	11:34:18
4	And then, after that, I was promoted to	11:34:26
5	director, and then I had circuit design architecture	11:34:28
6	and the layout groups, and the products included a	11:34:31
7	microcontroller for printers or or small	11:34:40
8	microprocessor, whichever way you want to look at	11:34:44
9	it, floating floating point chips and eventually	11:34:49
10	a eventually a a three-way-designed floating	11:34:54
11	point for supercomputer made in combination with	11:35:03
12	Toshiba and SGI and NEC. Sorry. Forgot them.	11:35:07
13	Q Just so I make sure I have the right product	11:35:12
14	list, so the first one was a floating point	11:35:16
15	co-processor?	11:35:18
16	A Mm-hmm.	11:35:19
17	Q And the next one was a printer?	11:35:19
18	A It's a microprocessor controller for a	11:35:23
19	printer.	11:35:25
20	Q And then the subsequent ones were also	11:35:26
21	related to floating point, but were they different	11:35:29
22	projects from the first one?	11:35:32
23	A They were different projects, yes.	11:35:33
24	Q And they were also floating point	11:35:34
25	co-processors?	11:35:36
		1

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1	A	Correct.	11:35:37
2	Q	What are floating point co-processors used	11:35:37
3	for?		11:35:45
4	A	So numbers can be numbers can be	11:35:45
5	identi	fied in different ways or written in different	11:35:51
6	ways.	One of those unique ways is scientific	11:35:56
7	notati	on, and a floating point co-processor is one	11:35:59
8	that p	rocesses numbers, so typical arithmetic	11:36:05
9	operat	ions; add, subtract, multiply, divide. They	11:36:11
10	are	they are the easiest to do, and they are done	11:36:15
11	on flo	ating point numbers.	11:36:17
12		A floating point number is a number who has a	11:36:19
13	single	digit to the left of the decimal point and	11:36:22
14	then m	ultiple digits to the right of the decimal	11:36:28
15	point,	and then that number gets multiplied by ten	11:36:31
16	raised	to a power, and so you store you store	11:36:34
17	the	it's called the mantissa and the exponent,	11:36:40
18	and yo	u work on them inside this chip to to	11:36:45
19	provid	e accurate mathematical answers.	11:36:49
20		So, for instance, if you are dealing with	11:36:53
21	number	s that are both very large and very small, a	11:36:55
22	floati	ng a floating point is the normal	11:37:00
23	method	ology used to deal with those numbers.	11:37:01
24		A good example would be things in space. You	11:37:05
25	know,	they are hundreds of millions of light years	11:37:09

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1	away, and then you have something that's sort of	11:37:12
2	right next door. One is a very large number, and	11:37:14
3	the other is a very small number, effectively, and	11:37:17
4	yet you can still do math with them and still be	11:37:20
5	relatively have good relative accuracy.	11:37:22
6	Q Is it called a co-processor because there's a	11:37:25
7	main processor and then that offloads these floating	11:37:29
8	point calculations to the floating point processor;	11:37:32
9	is that right?	11:37:37
10	A That's correct.	11:37:37
11	And then and back in this time, the	11:37:38
12	product that I worked on was for a 486 Intel chip,	11:37:39
13	and that Intel chip actually had its own floating	11:37:47
14	point co-processor on board, and so our chip was	11:37:50
15	external to that and actually looked very much like	11:37:55
16	a memory. You addressed it as a memory. You know,	11:37:58
17	you you you basically you usually wrote	11:38:02
18	three things into it. You wrote operand A,	11:38:05
19	operand B and then a command, like multiply.	11:38:13
20	And even though we were off chip compared to	11:38:16
21	the floating point that was placed in the Intel 486	11:38:18
22	chip, we provided 2x the performance.	11:38:22
23	So if you were doing something that had a lot	11:38:26
24	of floating point numbers in it, the boards,	11:38:29
25	computer PC boards, were made with an extra socket	11:38:33

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1	for this floating point chip that you added in.	11:38:37
2	Some some people put it in some models, put it	11:38:42
3	there automatically; in others, it was an upgrade.	11:38:47
4	Q And it would provide better performance for	11:38:51
5	these floating point calculations if you included	11:38:53
6	the chip?	11:38:55
7	A That that's correct.	11:38:56
8	Q Were your subsequent floating point	11:38:56
9	co-processor projects obviously they had	11:39:00
10	different applications, but were they conceptually	11:39:04
11	similar to what you just described?	11:39:07
12	A Yes.	11:39:08
13	Q What about the printer microcontroller?	11:39:08
14	A The printer the the the	11:39:11
15	microcontroller for the printer is a project that I	11:39:15
16	managed when I became director. It was one of the	11:39:19
17	projects that was in the group, and then I became	11:39:21
18	the manager of it, so I didn't do very much circuit	11:39:23
19	design on that. It was more management only.	11:39:27
20	Q What did that do? I mean obviously it has	11:39:30
21	something to do with printers, but what was the	11:39:34
22	purpose of that component?	11:39:37
23	A It literally is the brain in a printer. Any	11:39:37
24	printer that you use has a brain. It gets	11:39:41
25	information from the host, and then it turns it into	11:39:43

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1	printed information on the page, and so the format	11:39:48
2	that you get the data in from the host is not the	11:39:52
3	format that you need to spit the ink out, if you	11:39:55
4	will, in the right place on the page.	11:39:59
5	Q So it does that translation?	11:40:00
6	A Correct, among other things.	11:40:03
7	Q The floating point co-processors, being that	11:40:04
8	they are co-processors, can we agree those weren't	11:40:15
9	memories?	11:40:18
10	A Generally, I think people would talk about	11:40:19
11	them not as memories, right. They would talk about	11:40:28
12	them as even like I said, even though our	11:40:31
13	floating our floating point co-processor in the	11:40:33
14	Intel system occupied a position in memory space, it	11:40:36
15	wasn't really a memory. It was doing math.	11:40:41
16	Q Right.	11:40:44
17	Its purpose was to do these calculations, not	11:40:45
18	to store data, for example?	11:40:47
19	A That's correct.	11:40:48
20	Q The microcontroller for the printers, that	11:40:54
21	wasn't a memory either; right?	11:40:57
22	A No.	11:40:58
23	Q To the extent	11:40:58
24	A I'm sorry. It had memory in it, but it	11:41:03
25	wasn't its main function was not as a memory.	11:41:06
1		

1	Q To the extent the floating point co-processor	11:41:08
2	had memory in it, was that memory volatile or	11:41:11
3	non-volatile?	11:41:14
4	A In a floating point co-processor, the memory	11:41:15
5	was all volatile.	11:41:21
6	Q Was the same true for microcontroller for	11:41:23
7	printers?	11:41:27
8	A For the printers, we did I believe it was.	11:41:27
9	Not all printer microcontrollers were the same way,	11:41:37
10	I don't believe.	11:41:42
11	Q But to the extent you remember	11:41:43
12	A For the ones we did, I don't I don't	11:41:44
13	believe that they were I believe they were all	11:41:46
14	volatile.	11:41:47
15	Q So during your career at Weitek, you did not	11:41:47
16	design any memories; is that right?	11:41:52
17	A Well, I thought I said in the beginning that	11:41:54
18	I designed a memory blocks for the floating	11:41:59
19	point floating point co-processor, so it's not a	11:42:02
20	memory chip, but it's a block inside a bigger thing,	11:42:06
21	and like a register file is a memory. It just	11:42:10
22	happens to be a sub-component in a floating point	11:42:15
23	co-processor.	11:42:17
24	Q So you may have designed subcomponents that	11:42:18
25	were memories, but you did not design memory chips?	11:42:21

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1	A	I would probably say that's pretty accurate,	11:42:27
2	yeah.		11:42:30
3	Q	You didn't work with any non-volatile	11:42:30
4	memori	es when you were at Weitek?	11:42:35
5	A	I I don't believe so, no.	11:42:39
6	Q	So you didn't work with any flash memory	11:42:42
7	while	you were at Weitek?	11:42:45
8	A	No, I don't believe so.	11:42:46
9	Q	Let's move on to the next position, which was	11:42:50
10	at Sil	icon Graphics. This was on page spanning	11:42:58
11	betwee	n pages 2 and 3 of your CV.	11:43:02
12	A	I see it, yes.	11:43:03
13	Q	You are also director of engineering at	11:43:04
14	Silico	n Graphics?	11:43:07
15	A	Yes.	11:43:08
16	Q	And you held that position from June of 1992	11:43:08
17	to Apr	il of 1998; is that right?	11:43:12
18	A	In general, yes.	11:43:15
19	Q	Can you please describe your duties while you	11:43:16
20	were a	t Silicon Graphics?	11:43:20
21	A	So I was originally hired in during the time	11:43:21
22	that W	eitek, SGI, NEC, and Toshiba had this	11:43:29
23	effect	ively, it was a three-way deal to build a	11:43:37
24	floati	ng point a standalone floating point chip	11:43:43
25	to wor	k with a standalone integer unit that,	11:43:45
			1

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1	effectively, implemented a supercomputer, and so I	11:43:51
2	was responsible for the circuit design, the	11:44:01
3	architecture of the floating point unit, the layout.	11:44:06
4	All the pieces for the floating point unit	11:44:12
5	originally reported to me, and I had to staff and	11:44:14
6	manage.	11:44:23
7	Q So you played a design role during this time,	11:44:23
8	though; is that right?	11:44:26
9	A Also still, yeah.	11:44:26
10	Q And, in addition, you had these staffing and	11:44:27
11	management responsibilities?	11:44:30
12	A I did.	11:44:31
13	Q What would you say, roughly, your percentage	11:44:31
14	of time was between those different duties?	11:44:34
15	A Maybe 60/40. 60 percent in management,	11:44:38
16	40 percent in technical design issues.	11:44:44
17	Q Other than the the floating point	11:44:49
18	co-processor project that you mentioned, I see	11:44:53
19	several things listed on here.	11:44:58
20	Are those all floating point co-processors,	11:44:59
21	or were there other projects that you worked on	11:45:02
22	during that time?	11:45:05
23	A No, there were other projects.	11:45:05
24	So the the floating point co-processor	11:45:07
25	project I talked about is listed here as the TFP,	11:45:12
l		

1	which stands for two floating points. And there was	11:45:16
2	a an integer unit that went along with that.	11:45:20
3	The eventually that product finished, went into	11:45:26
4	production, and the T5 was the internal name for the	11:45:30
5	R10K, or the R10,000, which was a full-blown	11:45:36
6	microprocessor with a floating point on it, and that	11:45:43
7	project had started to bog down, so they took people	11:45:49
8	from the old Twin Peaks group and put it on the T5	11:45:52
9	group, and so I went over and and managed three	11:45:57
10	of the units, which is about 10 percent of the total	11:46:01
11	chip. I managed those people for that.	11:46:04
12	Then after that chip taped out, I was in	11:46:07
13	charge of all of the circuit design for the next	11:46:12
14	microprocessor, which was called Beast at the time,	11:46:15
15	and that was a 500-megahertz design, and about that	11:46:22
16	time is when Silicon Graphics started to have	11:46:29
17	problems, and that project actually never got	11:46:32
18	finished, but we almost got there.	11:46:37
19	Q So the projects here that are listed, the	11:46:41
20	Beast is the latest in time, and then the TFP is the	11:46:45
21	earliest in time	11:46:49
22	A Yeah	11:46:50
23	Q is that right?	11:46:50
24	A it's chronological, correct.	11:46:51
25	Q So during your time at Silicon Graphics, you	11:46:53

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1	worked on floating point co-processors and	11:46:55
2	potentially the integer mate of them and then also	11:46:57
3	microprocessors; is that right?	11:47:00
4	A Well, yeah, the the	11:47:02
5	Q You mentioned an integer aspect to that too.	11:47:08
6	I wasn't sure how much you worked on that, but just	11:47:10
7	in the interest of completeness.	11:47:13
8	A Well, the the okay. So in the early	11:47:14
9	days, because of what we were building, because it	11:47:17
10	was a supercomputer, you couldn't get enough	11:47:26
11	performance on a single chip, so it was multiple	11:47:28
12	chips. It was it was the integer unit, which did	11:47:31
13	all of the function well, not all, but most of	11:47:35
14	the functions of a microprocessor, and it had an	11:47:38
15	off-board tag RAM, and it had a and it had a	11:47:42
16	and it had two floating point units.	11:47:51
17	In in combination, that was equivalent to	11:47:54
18	a Cray Y-M we were equivalent to a Cray Y-MP	11:47:56
19	machine, which, at the time, sold for about	11:48:01
20	\$3 million, and you could buy our machine for, what	11:48:05
21	I recall, about \$90,000 per per per CPU, so	11:48:10
22	and the T5 was not a not a microprocessor	11:48:20
23	targeted at a supercomputer market, rather had at a	11:48:23
24	regular box market, regular, you know, PC box market	11:48:28
25	or you know, or engineering workstation market,	11:48:31

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1	and it so it had the floating point built into it,	11:48:35
2	and it had everything was on a single chip,	11:48:38
3	except for, you know, the system controller and the	11:48:41
4	memory and what you would expect today with an Intel	11:48:43
5	Pentium, for example. And Beast was to be yet	11:48:48
6	another mainstream microprocessor project.	11:48:51
7	Q Beyond those microprocessor projects and the	11:48:55
8	floating point projects you mentioned, and to the	11:49:03
9	extent there's an integer unit involved there, I'll	11:49:08
10	include that too, beyond those projects, did you	11:49:10
11	work on anything else while you were at Silicon	11:49:14
12	Graphics?	11:49:16
13	A Well, I ended up fixing the phase-locked-loop	11:49:16
14	problems that all of SGI had, because they didn't	11:49:21
15	know how to do a phase-locked loop, and I had done	11:49:24
16	one of them at Weitek.	11:49:27
17	Q Can you just describe what a	11:49:29
18	phase-locked-loop problem is for the record.	11:49:31
19	A Oh, sorry. A phase a phase-locked loop is	11:49:33
20	a circuit that takes an incoming signal and where	11:49:35
21	that signal changes from low to high, for example,	11:49:41
22	it takes an internal signal and matches the timing	11:49:45
23	of those two waveforms together so that when the	11:49:51
24	external waveform switches low to high, the internal	11:49:55
25	waveform switches at approximately the same time, so	11:49:58

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1	their phase, if you will, is locked to each other.	11:50:03
2	Q Like a synchronization type of thing?	11:50:06
3	A It is a synchronization-type thing, yes.	11:50:08
4	Q Gotcha. Okay.	11:50:10
5	Please continue with your other projects.	11:50:11
6	A So so the campus, meaning SGI campus, had	11:50:13
7	some parts that came from other people off campus,	11:50:20
8	and the phase-locked loops did not work correctly,	11:50:22
9	and I had some background there, and I had some	11:50:28
10	smart kids I had hired from Stanford who were	11:50:33
11	working for me, and we went and debugged the	11:50:36
12	problem, showed this outside vendor why the	11:50:41
13	circuitry they built wouldn't work correctly and	11:50:44
14	then what they had to do to fix it. And also the	11:50:47
15	part of the three units that I managed here on the	11:50:54
16	T5 project, the the internal PLL is is in	11:50:57
17	that is in that one of those three blocks. So	11:51:02
18	that so that was one of the things.	11:51:06
19	The other one was that I also repaired the	11:51:07
20	Toshiba tag RAM for SGI, so that's down in the TFP	11:51:15
21	R8K program.	11:51:20
22	So the tag RAM is an external memory for an	11:51:23
23	integer unit that holds information about where to	11:51:26
24	go get the data in in main memory, and so if	11:51:31
25	if if you basically, it's effectively like	11:51:40

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1	a look-up table. You look to see if you have	11:51:42
2	maybe you maybe you ask the machine to multiply A	11:51:45
3	times B or add A times B, and you have to have A and	11:51:49
4	B around to do that. So the the the tag is	11:51:54
5	part of a look-up table that let's you know whether	11:51:59
6	you have it locally or it's over there in the hard	11:52:01
7	drive or in the main memory or it's not resident on	11:52:05
8	the chip or not	11:52:08
9	Q Like	11:52:10
10	A okay?	11:52:10
11	Q in a cache or something like that?	11:52:10
12	A Like it's part of a it's part of a cache	11:52:12
13	system, yes.	11:52:15
14	Q Oh, so the tag RAM is part of the cache	11:52:15
15	system?	11:52:18
16	A Effectively, yes.	11:52:19
17	Q Okay.	11:52:20
18	A Yeah.	11:52:20
19	But for a supercomputer, tags can be pretty	11:52:21
20	big, so we didn't have room to put it on the same	11:52:24
21	silicon. Had to be its own piece of silicon.	11:52:27
22	So Toshiba designed that for SGI, and when	11:52:31
23	all the chips came back, we put the board together	11:52:34
24	and they powered it up and turned it on and ran the	11:52:36
25	tests and it was broken. And it was broken because	11:52:39
		1

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1	the tag RAM didn't work correctly. So being the	11 <b>:</b> 52 <b>:</b> 44
2	resident sort of memory guy, I go, "Well, this is	11:52:48
3	your problem now. Go fix it," so and we already	11:52:53
4	had guys on the team from part of this three-way	11:53:00
5	deal agreement was that NEC engineers and Toshiba	11:53:03
6	engineers would be resident at Silicon Graphics	11:53:08
7	working on working on this design.	11:53:11
8	And so I knew some of them, and I had for	11:53:17
9	Weitek, I had been to Japan more than a few times,	11:53:19
10	and so they sent me to Japan to go do an analysis	11 <b>:</b> 53 <b>:</b> 22
11	and find out what it was and how to fix it, and so I	11:53:27
12	did that, and we worked with the guys from Japan.	11:53:34
13	Actually even brought some of them to the U.S. and	11:53:39
14	worked through the issues and fixed it and turned	11 <b>:</b> 53 <b>:</b> 42
15	the product around and got it working. So I did	11 <b>:</b> 53 <b>:</b> 46
16	that also.	11:53:49
17	And then the rest is mostly hiring and	11:53:53
18	development of people skills and then also working	11:53:59
19	with the two Japanese partners to understand,	11:54:08
20	because I had worked in a big fab. Both Toshiba and	11 <b>:</b> 54 <b>:</b> 12
21	NEC had big fabs, and so it's like, well, you are a	11 <b>:</b> 54 <b>:</b> 17
22	good guy to do this, and I don't want to go to	11:54:21
23	Japan, so you go, so I did that too.	11:54:24
24	Q So with regard to this tag RAM, I think you	11 <b>:</b> 54 <b>:</b> 26
25	said Toshiba originally designed it, and then you	11 <b>:</b> 54 <b>:</b> 29

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1	fixed it once you realized	11:54:31
2	A I helped them	11:54:31
3	Q there were shortcomings?	11:54:34
4	A I helped them fix it, yeah, and it was	11:54:35
5	also BiCMOS.	11:54:38
6	Q "BiCMOS" referring to the technology we	11:54:39
7	talked about earlier that you worked on at Hughes?	11:54:41
8	A National.	11:54:44
9	Q National.	11:54:45
10	A Yes.	11:54:47
11	Q Other than the the tag RAM project that we	11:54:48
12	just discussed, did you work on any projects that	11:54:52
13	were developing memory?	11:54:56
14	A Well, yes, because in in in the Beast	11:54:57
15	program, I was I had all of the circuit	11:55:04
16	designers, so the people designing the caches on	11:55:06
17	that project reported to me, so ICache, DCache, the	11:55:10
18	tags, the register files, they were all under my	11:55:17
19	tutelage.	11:55:25
20	Q What types of memories were those?	11:55:25
21	A They were all static RAMs.	11:55:28
22	Q Is the tag RAM static RAM?	11:55:33
23	A Yes.	11:55:36
24	Q And I believe we established earlier that	11:55:36
25	these static RAMs are volatile memories?	11:55:38
		1

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1	A That's correct.	11:55:42
2	Q Did you work with any flash memory while you	11:55:43
3	were at Silicon Graphics?	11:55:45
4	A No, I don't believe I did.	11:55:46
5	Q After the Silicon Graphics position, that's	11:55:47
6	when you started your consulting company where you	11:55:57
7	work today; is that right?	11:56:00
8	A That's correct.	11:56:01
9	Q I'm going to apologize if we talked about	11:56:01
10	this earlier, but your company, Firenza, is that	11:56:06
11	just you or is that other people too?	11:56:09
12	A As an LLC, it requires two people, so my wife	11:56:11
13	and I are the owners.	11:56:18
14	Q Okay.	11:56:19
15	A We don't have any employees. Everybody who	11:56:19
16	works with me works as a contractor, and so I do	11:56:24
17	circuit design things or circuit designs that	11:56:32
18	usually you can't find anywhere else.	11:56:36
19	Q Have you ever had any employees?	11:56:39
20	A No. Never.	11:56:41
21	Q Just your wife and yourself?	11:56:43
22	A Correct.	11:56:45
23	Q Is your wife an engineer?	11:56:45
24	A She's an ex-layout person, so no no to an	11:56:46
25	engineer, but she's been in the business. She was	11:56:54
		1

1	on the bipolar side previously.	11:56:56
2	Q So my next question was going to be: Is she	11:56:58
3	kind of a silent partner in this, or is she actually	11:57:02
4	doing this technical work?	11:57:05
5	A No, she's a silent partner.	11:57:07
6	Q Okay. Fair enough.	11:57:09
7	So you are doing the heavy lifting for	11:57:10
8	Firenza?	11:57:12
9	A Yeah.	11:57:13
10	Q Over the years, it looks like you have done	11:57:13
11	some amount of this litigation consulting work and	11:57:15
12	then some amount of other work.	11:57:18
13	And let me first ask you, you know: Other	11:57:22
14	than litigation consulting, what would you generally	11:57:24
15	call the other types of work that you do?	11:57:26
16	A What would I call it.	11:57:28
17	Q I just want to get some way we can talk about	11:57:32
18	it.	11:57:35
19	A Sure. Sure.	11:57:35
20	So, generally, I'm called to do people	11:57:36
21	call me to do usually one of two things: The first	11:57:39
22	thing is to fix silicon that they have that's broken	11:57:44
23	and doesn't work right. So they did their design.	11:57:46
24	They put it into the fab. It came back and	11:57:50
25	(unreportable sound), and since I have multiple	11:57:57
		1

1	years of experience doing that at multiple places,	11:57:59
2	it's something that I continue to do and get calls	11:58:03
3	for it. I don't know I don't know about often,	11:58:07
4	but more than one call a year. More than two calls	11:58:11
5	a year usually is to go make an assessment of what's	11:58:16
6	wrong with some piece of silicon and try and help	11:58:19
7	people fix it quickly.	11:58:22
8	The second part is to design for people	11:58:24
9	things that they things that they do not or	11:58:29
10	cannot get elsewhere.	11:58:35
11	So, for instance, generally I've always	11:58:38
12	worked in the very high-speed memory area. My work,	11:58:43
13	especially at National, was the fastest thing you	11:58:50
14	could literally buy at the time, and if it wasn't	11:58:54
15	if we weren't the fastest, we were, like, No. 2 or	11:58:57
16	we were making a compatible product. So I've always	11:59:00
17	sort of lived on the bleeding edge, but my	11:59:05
18	background is in technology, and especially with	11:59:10
19	memory, working so close with the process engineers,	11:59:14
20	you end up learning a lot of things about processes	11:59:19
21	and why things happen, and you are guided by the	11 <b>:</b> 59 <b>:</b> 22
22	physics of all of that, and that's the background I	11:59:28
23	had in school, in solid-state devices.	11:59:31
24	So, for example, there's a non-volatile	11 <b>:</b> 59 <b>:</b> 32
25	memory here shown in line one, two three from the	11:59:40

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1	bottom, and it says, Designed an EFUSE circuit for	11:59:44
2	another 65-nanometer microprocessor. So this is a	11:59:47
3	sub-block of a microprocessor that has programmable	11:59:51
4	fuses in it in which information is stored about the	11:59:56
5	device. You might store you might store, for	12:00:00
6	instance, which wafer lot it was. You might store	12:00:08
7	characteristics of a circuit that you want to	12:00:14
8	electrically trim, and and basically this is	12:00:19
9	this is a memory which it comes unprogrammed. You	12:00:23
10	program it when you do the testing of the device,	12:00:29
11	and then it remembers that information forever.	12:00:32
12	Power on, power off doesn't make a difference.	12:00:36
13	Q Is that I'm just trying to see where that	12:00:39
14	kind of fits in what we are talking about.	12:00:44
15	So sounds like it's non-volatile?	12:00:46
16	A It's definitely non-volatile, and it's	12:00:48
17	definitely a memory.	12:00:51
18	Q Is it a reprogrammable once it's been	12:00:52
19	programmed?	12:00:55
20	A No.	12:00:56
21	Q So it's programmed once and then non-volatile	12:00:56
22	and it never forgets?	12:00:58
23	A Correct.	12:01:00
24	Q So it's not a memory in the sense of, like, a	12:01:00
25	consumer read/write type of memory; it's more of a	12:01:04

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1	single-purpose type of memory?	12:01:07
2	A Well, actually, no. The technology the	12:01:09
3	exact same technology was being pursued for, oh,	12:01:13
4	gosh, I'm going to say four or five years by I	12:01:18
5	might have the name wrong I think, Matrix	12:01:25
6	Semiconductor, and what they were trying to make was	12:01:30
7	a one-time programmable what you would call	12:01:31
8	flashcard. So for this would be one-time	12:01:37
9	programable card that you would put in your camera,	12:01:43
10	much like a flashcard, but inexpensive enough that	12:01:46
11	you it was so cheap that you would program it	12:01:50
12	once and it would store your pictures forever and	12:01:55
13	you didn't care, and they and they you know,	12:01:57
14	they obtained funding, and I'm pretty sure they were	12:02:05
15	alive for four or five years trying to do this.	12:02:08
16	Their unique part was that they figured out	12:02:11
17	how to stack these cells in multiple layers	12:02:14
18	vertically so that the magnitude of the file size	12:02:17
19	that you could store was very large for the size of	12:02:23
20	the silicon that you used, and that was and that	12:02:27
21	literally was, as I recall, an EFUSE-type circuit.	12:02:31
22	Q Was that the trade name for it? What was	12:02:35
23	the	12:02:38
24	A The trade I don't	12:02:39
25	Q What would people have	12:02:39

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1	A I don't think they went public, first of	12:02:41
2	all.	12:02:42
3	Q Oh, okay. I'm kind of getting at what would	12:02:42
4	people in the field call it?	12:02:46
5	A I thought they were calling it, like,	12:02:47
6	one-time flashcards, but I really like I said,	12:02:50
7	they never they never went public, but the but	12:02:53
8	the technology was this, if you will, programmable	12:02:55
9	link type of type of thing. And, of course,	12:03:00
10	programmable links had been around a very long time	12:03:06
11	from PLD world, the programmable logic world, where	12:03:08
12	you you know, rather than storing memory bits,	12:03:15
13	you stored logic configurations, in effect.	12:03:18
14	Q Is this the blown fuse concept	12:03:21
15	A Yeah, so you have	12:03:21
16	Q you were talking about earlier?	12:03:24
17	A you have fuse and fuse and anti-fuse,	12:03:25
18	and there are various there are various manners	12:03:27
19	in which those fuses are created. EFUSE was	12:03:32
20	EFUSE was another one. This was literally was a	12:03:35
21	silicon-based fuse.	12:03:38
22	They also have other ones that you can	12:03:43
23	some you program electrically and/or you program	12:03:46
24	them with a laser beam. You just come by with a	12:03:49
25	laser at wafer test and you blow the links and so	12:03:52
		1

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1	the way you program them is with a laser as opposed	12:03:56
2	to actually blowing the silicon up.	12:03:59
3	Q Was	12:04:00
4	A This was this was electrically	12:04:03
5	programmable, so we literally blew the links with	12:04:04
6	programming circuitry.	12:04:09
7	Q For this EFUSE project, first of all, you	12:04:10
8	talked about the consumer version that maybe never	12:04:13
9	took off, but just so the record is clear, you	12:04:16
10	didn't work on that consumer version	12:04:19
11	A Mm-hmm.	12:04:19
12	Q did you?	12:04:22
13	A That's correct. I did not work on that. I	12:04:22
14	was merely saying that the same technology had been	12:04:24
15	used in a product like that.	12:04:27
16	Q And with regard to this EFUSE circuit that	12:04:30
17	you designed, where did you get the silicon for	12:04:33
18	that? I mean, did you buy it somewhere, or did you	12:04:35
19	design it and have it built from scratch, or where	12:04:38
20	did that come from?	12:04:41
21	A So the company that Firenza did this for was	12:04:41
22	Montalvo, and I don't think they went public either.	12:04:46
23	I think they eventually were purchased by Sun	12:04:48
24	Microsystems, and they were building a	12:04:57
25	486-compatible microprocessor, and where did they	12:04:59

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1	get this. I don't remember where they got the	12:05:06
2	silicon. They were they were fabless, so	12:05:08
3	somebody, I believe in Japan my best recollection	12:05:12
4	is Fujitsu was operating as the foundry.	12:05:17
5	MR. LIMBACH: I'm going to caution the	12:05:21
6	witness to be careful not to divulge anything that's	12:05:23
7	confidential to another party. You are talking a	12:05:26
8	lot of	12:05:29
9	THE WITNESS: Oh	12:05:29
10	MR. LIMBACH: old	12:05:29
11	THE WITNESS: sure.	12:05:29
12	MR. LIMBACH: old history. There's no	12:05:30
13	Protective Order in this case, so I'll caution you	12:05:30
14	that if you think of something that you that is	12:05:33
15	responsive to an answer that may be confidential to	12:05:35
16	let counsel know and then he will proceed	12:05:39
17	accordingly.	12:05:41
18	MR. HEINZ: Sure. Yeah, don't tell me	12:05:42
19	anything secret.	12:05:44
20	THE WITNESS: I don't believe that I have,	12:05:45
21	and most of this is more than five years old, so	12:05:47
22	MR. LIMBACH: Just as you get	12:05:49
23	THE WITNESS: and a lot of companies are	12:05:53
24	now defunct.	12:05:53
25	MR. LIMBACH: Right.	12:05:56

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1	THE WITNESS: But, no, I haven't given away	12:05:56
2	any secrets.	12:06:00
3	MR. LIMBACH: I don't think you have. I just	12:06:00
4	want to caution you, because as you get closer in	12:06:01
5	time	12:06:03
6	THE WITNESS: Yeah, as you get closer in	12:06:03
7	time	12:06:03
8	MR. LIMBACH: it might be an issue.	12:06:03
9	MR. HEINZ: Yeah. If we get there, let me	12:06:07
10	know and then we'll we'll deal with it at that	12:06:07
11	point.	12:06:07
12	THE WITNESS: Got it.	12:06:07
13	BY MR. HEINZ:	12:06:07
14	Q So let me ask you	12:06:13
15	A Let let me	12:06:15
16	Q Okay.	12:06:15
17	A so let me finish.	12:06:16
18	Q Yeah, yeah.	12:06:16
19	A So part of my work that's nonlegal is repair	12:06:17
20	work. De "debug" would be the official name.	12:06:20
21	And then the other part of it is design work	12:06:27
22	for things that you can't get anywhere else.	12:06:29
23	So, for instance, today in the valley, as far	12:06:34
24	as I'm aware of, if you are looking for an	12:06:37
25	independent person to build you a 3-gigahertz SRAM,	12:06:40

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1	I'm pr	robably one of the only people still in	12:06:46
2	busine	ess doing that that's not associated with Intel	12:06:48
3	or AMI	) or some other big house. So if you you	12:06:52
4	have a	a you know, if you are a fabless kind of guy	12:06:58
5	and yo	ou can't find the memory that you want from the	12:07:01
6	standa	ard memory block suppliers, then you could get	12:07:04
7	that t	ype of block from Firenza. Firenza would do	12:07:08
8	the de	esign for you.	12:07:13
9	Q	So just to to kind of summarize our our	12:07:13
10	groupi	ings, you have the legal work, the debug work,	12:07:18
11	and th	ne design work.	12:07:21
12		Is that a fair assessment?	12:07:22
13	A	Design and debug?	12:07:23
14	Q	Or design and debug and the legal aspect?	12:07:30
15	A	Yeah.	12:07:32
16	Q	What percentage would you estimate that you	12:07:33
17	spend	on the legal work and the design and debug	12:07:36
18	work?		12:07:40
19	A	It really depends upon which month you ask	12:07:40
20	me.		12:07:43
21	Q	Let me ask you from 1998 to the present.	12:07:43
22	A	Oh, gosh.	12:07:43
23	Q	Just a rough estimate.	12:07:47
24	A	Well, here's what I can tell you, because I	12:07:48
25	can't	I don't really think I can answer that, but	12:07:52

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		1
1	I can tell you the following: I try very, very hard	12:07:55
2	not to have an engineering project going on and then	12:08:00
3	legal work on top of it, because legal guys kind of	12:08:03
4	think they can just call you up at any moment and	12:08:09
5	say, "Okay. For the next eight days, you are mine,"	12:08:14
6	and that doesn't fit with doing engineering work	12:08:16
7	that you have committed to that will take five or	12:08:18
8	six months to get done. So I have had periods of	12:08:21
9	overlap. They have been very painful.	12:08:23
10	So from a from a percentage point of view,	12:08:28
11	man, I would probably say that it's in the	12:08:34
12	beginning, it was much more circuit-type work, debug	12:08:40
13	and circuit design, than it was legal. In fact, it	12:08:44
14	was all because I started doing that before I	12:08:51
15	started doing legal. And even when I was doing	12:08:54
16	legal in the beginning, it just wasn't you know,	12:08:56
17	it sort of came and went.	12:08:59
18	But there have been other times where, like,	12:09:06
19	when the industry has gotten really slow, that there	12:09:08
20	was no circuit design work and all I had was legal,	12:09:10
21	and sometimes there were times luckily I'm	12:09:11
22	only I have no employees, so sometimes there was	12:09:14
23	no money. There was no work. Didn't make any	12:09:16
24	difference whether it was legal or not. So it it	12:09:20
25	really sort of varies all over all over the	12:09:24
		1

1	place.	12:09:26
2	Firenza, as a company right now, is presently	12:09:28
3	designing a memory for somebody else, and and you	12:09:30
4	can't know about it because I am covered under	12:09:38
5	NDA	12:09:40
6	Q Sure.	12:09:41
7	A so but so and and because of some	12:09:42
8	personal issues, I don't participate in that. I	12:09:48
9	mean, I keep track of the project, but I have a	12:09:53
10	friend of mine as a contractor who's doing most of	12:09:56
11	it, and we talk, but he's still doing most of the	12:10:00
12	work.	12:10:04
13	So I mean, so, like, if we took a point in	12:10:05
14	time right now, it might be 50/50. It's just that	12:10:10
15	I'm doing all the legal stuff and he's doing all the	12:10:14
16	design stuff.	12:10:17
17	Q So let me ask you: You, personally, in the	12:10:18
18	last year or so, how much of your personal time has	12:10:22
19	been litigation consulting versus the design and	12:10:26
20	debug work?	12:10:29
21	A In the last year, I have had two I think	12:10:30
22	two design types of things. One is the one I talked	12:10:39
23	about right now, and one is something previous which	12:10:43
24	was a debug.	12:10:46
25	And then from a legal point of view, last	12:10:48

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1	year I was involved in an ITC case, the last one on	12:10:53
2	my list, the Ericsson one well, it doesn't say	12:11:03
3	Ericsson there.	12:11:10
4	Q So the one that says "Certain Wireless	12:11:11
5	Communications Equipment"?	12:11:13
6	A Correct.	12:11:14
7	Q Okay.	12:11:14
8	A And and this matter, which you already	12:11:17
9	know what my estimate on hours is for that. And I	12:11:29
10	don't think much of not much of anything else.	12:11:33
11	Nothing significant, I would say.	12:11:36
12	Q And just to clarify, I think this is probably	12:11:38
13	clear from the document, but the expert-witness-work	12:11:42
14	cases are listed from earliest in time on page 1 in	12:11:45
15	chronological order?	12:11:49
16	A As best I could remember them all, yes.	12:11:50
17	Q Sure.	12:11:53
18	A But, yes. NeoMagic was my first case.	12:11:54
19	Q And as far as you know, this is a complete	12:11:58
20	list of your expert witness work; is that right?	12:12:00
21	A I believe as far as the anything that ever	12:12:03
22	went to either deposition or expert testimony. But	12:12:08
23	like as I said before, I think that I think	12:12:17
24	that Toshiba/Hynix thing actually settled before we	12:12:20
25	actually did anything, but here it is on the list,	12:12:25

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1	so it might actually be everything I worked on.	12:12:27
2	Q I was going to comment that, on page 2,	12:12:29
3	several of these are re-examination proceedings?	12:12:33
4	A Oh, yes.	12:12:35
5	Q And those typically, I believe, would not	12:12:36
6	involve your testimony or your being deposed or	12:12:39
7	testifying in a proceeding; is that right?	12:12:43
8	A Well, certainly it's no testimony in court.	12:12:45
9	I've definitely been deposed for some of those	12:12:52
10	things, and I have done some of them were	12:12:55
11	ex parte, and I have done ex parte meetings with the	12:13:03
12	PTO, which I don't think is qualifies as	12:13:11
13	testimony, but I'm not an expert in that, so I don't	12:13:14
14	really know. Two guys down from you might be able	12:13:17
15	to help you with the answer.	12:13:23
16	Q I think we can figure that one out.	12:13:24
17	A Yeah, I think so.	12:13:26
18	Q So you believe, just so the record is clear,	12:13:27
19	that this is a complete list, or this is a list of	12:13:33
20	only ones you have testified in or or is a list	12:13:38
21	that's been cabined in some way?	12:13:41
22	A I don't I don't think I've left anything	12:13:45
23	out on purpose. I think it is a complete list, and	12:13:46
24	I would just have to I would just have to I	12:13:54
25	don't think there's anything other than this that	12:13:57

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1	I've done.	12:13:59
2	Q You mentioned the EFUSE circuit project	12:14:01
3	earlier, which was a non-volatile memory	12:14:05
4	A Mm-hmm.	12:14:05
5	Q in your view; is that right?	12:14:07
6	A Yes.	12:14:09
7	Q Have you worked on any other projects at	12:14:09
8	Firenza relating to non-volatile memories?	12:14:14
9	A So to get back to your statement, EFUSE is	12:14:17
10	not just it's not just my opinion that EFUSE is	12:14:22
11	non-volatile. EFUSE is non-volatile, and it's not	12:14:26
12	just my belief; that the industry understands that	12:14:30
13	EFUSE is non-volatile.	12:14:34
14	Q Okay. Recognizing that position about	12:14:37
15	EFUSE	12:14:37
16	A Yeah.	12:14:37
17	Q other than EFUSE, have you worked on any	12:14:37
18	other non-volatile memories since you have been at	12:14:40
19	Firenza?	12:14:45
20	A The only other non-volatile work that I have	12:14:45
21	done at Firenza is the ITC matter listed on page 2.	12:14:51
22	Q In the Matter of Certain MLC Flash Memory	12:15:04
23	Devices and Products Containing Same?	12:15:05
24	A Correct.	12:15:07
25	Q And that was a litigation consulting project;	12:15:08
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1	is that right?	12:15:14
2	A That's correct.	12:15:14
3	Q The EFUSE memory was non-volatile memory, but	12:15:15
4	it was not flash memory; is that right?	12:15:30
5	A That's correct. We talked about one-time	12:15:32
6	programmable.	12:15:35
7	Q In the ITC case, that was MLC flash memory;	12:15:37
8	is that right?	12:15:49
9	A That's correct, yes.	12:15:49
10	Q Other than this ITC case now that we have	12:15:50
11	been through your CV here, other than that case,	12:15:52
12	have you worked on flash memory?	12:15:57
13	A The only the only parts of it the only	12:16:01
14	parts of flash that I've worked on is the like I	12:16:14
15	said, the flash technology that's used in an	12:16:20
16	e-squared CMOS PAL, and that is given the way you	12:16:22
17	are defining flash memory, that's not flash memory	12:16:28
18	per se, and I've told you that we we definitely	12:16:31
19	had some individual flash cells, specifically on	12:16:39
20	the on the test chips, for those things that we	12:16:49
21	could operate individually, but as a commercial,	12:16:52
22	quote/unquote, flash memory product, I think that	12:16:58
23	what's here is is is all I've done.	12:17:04
24	Q So you worked on the E2CMOS PALs, which had	12:17:07
25	flash memory technology, but as we already	12:17:13
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1	established, I believe, those were not flash memory?	12:17:16
2	A The device was a logic device, correct.	12:17:19
3	Q And you worked on this ITC case regarding	12:17:21
4	flash memory, but other than that and the to the	12:17:26
5	extent the E2CMOS PAL bears on it, beyond that, you	12:17:29
6	don't have any flash memory experience; is that	12:17:35
7	right?	12:17:38
8	A Beyond that, I don't think there's anything	12:17:38
9	else, no.	12:17:41
10	Q I would like to go back to your CV here and	12:17:41
11	ask you about paragraph 5 on page 2?	12:18:10
12	A I'm confused, because my CV doesn't have	12:18:20
13	paragraphs.	12:18:24
14	Q Oh, I'm sorry. Your declaration.	12:18:24
15	A Okay.	12:18:26
16	Q Sorry. The declaration that's attached to	12:18:26
17	the front of that, it's the same	12:18:28
18	A Oh	12:18:29
19	Q exhibit.	12:18:29
20	A it's the same thing. Yeah. Okay.	12:18:30
21	Q So the second sentence in paragraph 5 reads:	12:18:43
22	As set forth in my curriculum vitae,	12:18:45
23	I have over 39 years of experience	12:18:48
24	with memory devices.	12:18:50
25	Do you see that?	12:18:52

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1	A I do.	12:18:53
2	Q Is that statement accurate?	12:18:53
3	A I believe it is. If you are asking me did I	12:18:55
4	work on memory devices every day of the 39 years,	12:19:08
5	then I think my answer would be no, but I think that	12:19:12
6	I have done memory off and on over that 39 years of	12:19:19
7	experience, and I've done it in multiple	12:19:22
8	technologies and I'm I'm happy with that	12:19:24
9	sentence.	12:19:26
10	Q But in in your view, the meaning of this	12:19:27
11	sentence is that, in the 39 years, you have worked	12:19:33
12	with memory off and on, not that you have worked on	12:19:35
13	memory continuously for 39 years; is that right?	12:19:37
14	A Well, it's clear from my CV that I haven't	12:19:40
15	worked on memory every day of my 39 years, so I	12:19:44
16	don't think I've expressed it as anything other than	12:19:50
17	I have 39 years of experience with memory devices.	12:19:54
18	As I've already stated, oftentimes when I'm working	12:19:58
19	on a project, the fact just the fact that I have	12:20:01
20	made memory before made people find me and ask me	12:20:05
21	about a memory device that they are working on or	12:20:11
22	a memory how how does this work or how did you	12:20:15
23	do this. So that reservoir of knowledge, to my	12:20:18
24	mind, has been constantly tapped for 39 years, so.	12:20:21
25	Q And if I'm doing the math right, the 39 years	12:20:25
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1	here, since this declaration was filed in 2013,	12:20:29
2	spans the entire period from the time you graduated	12:20:33
3	with your bachelor's degree until the time you did	12:20:36
4	this declaration; is that right?	12:20:38
5	A Oh, I'm sorry, I haven't done the math.	12:20:40
6	Q 1974 to 2013?	12:20:42
7	A Well, that math works, so, yeah.	12:20:56
8	Q So and this is meant to refer to your	12:20:58
9	entire span of experience?	12:21:05
10	A I you you seem to have decided that	12:21:12
11	unless a memory device is a standalone product, that	12:21:17
12	it's not a memory device. And many products have	12:21:22
13	memory in them, and they and they are that	12:21:25
14	particular block is called a memory could be	12:21:30
15	called a memory device, so I don't agree with your	12:21:32
16	assessment of how that comes about, but I still	12:21:39
17	stand by the statement I have here.	12:21:42
18	Q I'm not trying to assess anything. I'm just	12:21:44
19	trying to figure out what you meant by the	12:21:46
20	statement.	12:21:48
21	A I think I've told you.	12:21:48
22	Q If this statement said designing memory	12:21:53
23	devices, what would the time frame be?	12:22:00
24	MR. LIMBACH: Objection; form.	12:22:07
25	THE WITNESS: If this said designing gee,	12:22:10

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1	I I don't know exactly because, as I've told you,	12:22:21
2	there were, oftentimes, where I did some memory	12:22:23
3	thing in some device. Let's take the example of a	12:22:28
4	floating point unit.	12:22:32
5	A floating point unit has memory in it,	12:22:33
6	right? I helped people design those things. Is it	12:22:36
7	a memory device? Well, that's a good question.	12:22:42
8	It's certainly its main function is as a floating	12:22:44
9	point unit, but it has memory in it. You have to	12:22:47
10	design it. I helped do the design. I think that	12:22:50
11	counts.	12:22:53
12	So I have would have a very hard time	12:22:54
13	figuring out over, effectively, 40 years how many	12:22:57
14	days I actually spent doing the design of an	12:23:03
15	individual piece of memory for someone or consulting	12:23:07
16	with them on that memory versus doing other work.	12:23:10
17	BY MR. HEINZ:	12:23:17
18	Q But we can agree that number is not	12:23:17
19	100 percent?	12:23:19
20	A Yeah, I think we can agree that's not	12:23:21
21	100 percent.	12:23:23
22	Q I would like to move to your declaration and	12:23:53
23	ask you about paragraph 8 and paragraph 9, which are	12:23:53
24	on page 4.	12:23:54
25	A Yes.	12:23:55

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1	Q Here you discuss one of ordinary skill in the	12:23:56
2	art, and in paragraph 9 in particular, you give your	12:24:00
3	opinion about the level of ordinary skill in the art	12:24:05
4	related to the '045 patent.	12:24:08
5	Do you see that?	12:24:10
6	A I do.	12:24:11
7	Q Are you one of ordinary skill in the art for	12:24:11
8	the '045 patent?	12:24:15
9	A I believe I have more than ordinary skill in	12:24:16
10	the art for the '045 patent.	12:24:28
11	Q Based on what?	12:24:33
12	A Based on of my knowledge of the underlying	12:24:34
13	technology, based on my memory knowledge at a	12:24:37
14	minimum.	12:24:44
15	Q So you have a master's of science degree in	12:24:45
16	electrical engineering; right?	12:24:47
17	A I do.	12:24:48
18	Q And, in your view, one of ordinary skill in	12:24:53
19	the art needed to have a master's degree in	12:24:56
20	electrical engineering and three years of relevant	12:24:59
21	experience working in the field of non-volatile	12:25:00
22	memory devices?	12:25:02
23	A Yes.	12:25:03
24	Q What's your three years of relevant	12:25:08
25	experience or more working in the field of	12:25:10

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1	non-volatile memory devices?	12:25:13
2	A So you have the EFUSE work. You have the	12:25:14
3	memory devices. You have the work that I did in	12:25:38
4	unison with the people designing the EPROMs at	12:25:43
5	National Semiconductor in Utah. You have you	12:25:45
6	have the work done on the ITC matter. You have the	12:26:01
7	work done for the e-squared CMOS PAL devices. You	12:26:23
8	have the BiCMOS PAL devices, which are also	12:26:30
9	non-volatile. You have the test chip work done for	12:26:33
10	the e-squared CMOS PAL. You have the test chip work	12:26:41
11	done for the EFUSE part, the EFUSE block. I think	12:26:47
12	that is more than enough to cover the requirements.	12:27:05
13	Q Do you think that adds up to three years?	12:27:07
14	A I do.	12:27:11
15	Q If this definition, rather than saying as it	12:27:11
16	does now, "working in the field of non-volatile	12:27:27
17	memory devices"	12:27:29
18	A Mm-hmm.	12:27:29
19	Q said "working in the field of flash	12:27:32
20	memory," would you be one of skill in the art then?	12:27:35
21	A I don't see that I would clear the hurdle if	12:27:37
22	that was where the bar was set. However, that would	12:28:13
23	seem to me to be very narrow definition.	12:28:18
24	Q I recognize it's different than the	12:28:21
25	definition you had here.	12:28:23
		1

1	A Mm-hmm.	12:28:27
2	Q But you would agree with me that if	12:28:27
3	paragraph 9 was the same except the last clause said	12:28:29
4	"working in the field of flash memory devices"	12:28:35
5	instead of just "non-volatile memory devices," you	12:28:37
6	would not clear that bar; is that right?	12:28:40
7	A If you are if you are defining a flash	12:28:43
8	memory device as a device that their only the	12:28:48
9	only function of that device is to store data and	12:28:53
10	give the data back, if that's the definition of a	12:28:58
11	flash memory device and the and the underlying	12:29:02
12	technology has nothing to do with it, then I would	12:29:07
13	agree.	12:29:11
14	Q Let me ask you in a way that one of ordinary	12:29:11
15	skill in the art would have understood the term	12:29:16
16	"flash memory" in the concept in the context of	12:29:18
17	the '045 patent.	12:29:22
18	With that understanding of the term "flash	12:29:23
19	memory," in other words, not the restrictive	12:29:25
20	definition you just said, which I believe is more	12:29:31
21	restrictive than that, if the last clause said	12:29:33
22	"working in the field of flash memory devices,"	12:29:36
23	would you be over that bar or not?	12:29:39
24	MR. LIMBACH: Objection; form.	12:29:42
25	THE WITNESS: Well, what do you mean when you	12:29:44
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1	say a "flash memory device"?	12:29:47
2	BY MR. HEINZ:	12:29:50
3	Q What I want what I'm intending to ask	12:29:51
4	is the '045 patent is entitled "Serial Flash	12:29:53
5	Memory."	12:30:00
6	Do you see that?	12:30:03
7	A I do.	12:30:03
8	Q So you understand what the flash memory part	12:30:04
9	of that means; right?	12:30:07
10	A I do.	12:30:08
11	Q So going back to my earlier question in	12:30:09
12	paragraph regarding paragraph 9, with that	12:30:13
13	understanding of flash memory, if paragraph 9, the	12:30:18
14	last clause, said "working in the field of flash	12:30:22
15	memory devices," would you clear that hurdle or not?	12:30:25
16	A Well, part of my confusion comes in the fact	12:30:32
17	that there are other ways to work on flash devices	12:30:34
18	that are not literally flash memory. Flash memory	12:30:39
19	is often or can be a component of a bigger device,	12:30:44
20	like a block, like I talked about earlier. Like,	12:30:50
21	for instance, the EFUSE block that I talked about,	12:30:54
22	it's it's every time you have talked today	12:30:57
23	about a flash memory, you have talked about a	12:30:59
24	consumer-oriented flash memory, and yet, they are	12:31:02
25	not the only ones out there. Flash memory blocks	12:31:05
		1

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1	are often put on semiconductor devices that their	12:31:09
2	main function is just not a generic consumer flash	12:31:13
3	memory device.	12:31:17
4	Q I haven't been meaning to restrict flash	12:31:18
5	memory to the consumer application at all. And I	12:31:22
6	don't believe I've asked any questions that had that	12:31:24
7	as a predicate. So I would disagree with your	12:31:27
8	statement, and I will ask you again.	12:31:30
9	With the flash memory as it's defined or as	12:31:32
10	that term is used in the title of the '045 patent,	02:14:13
11	which is entitled "Serial Flash Memory," with that	02:14:13
12	understanding of flash memory as it's used in the	02:14:13
13	'045 patent, are you one of ordinary skill in the	02:14:13
14	art with three years of relevant experience working	02:14:13
15	in the field of flash memory or not?	02:14:13
16	MR. LIMBACH: Objection; form.	02:14:13
17	THE WITNESS: Are you specifically limiting	02:14:13
18	this to the example shown in the the embodiment	02:14:13
19	shown here	02:14:13
20	MR. HEINZ: No.	02:14:13
21	THE WITNESS: and but but you are	02:14:13
22	limiting yourself to the claims shown here.	02:14:13
23	MR. HEINZ: No.	02:14:13
24	Q I'm just asking you about the word or the	02:14:13
25	term "flash memory" as that term is used in the	02:14:13

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1	patent, and I believe it's used more broadly than	02:14:13
2	the specific embodiment in the patent, wouldn't you	02:14:13
3	agree?	02:14:13
4	A Specific embodiment in the patent. I do I	02:14:13
5	do agree it's used broadly. It's the part I seem	02:14:13
6	to be unable to have you understand is that if a	02:14:13
7	flash memory array stores logic information, that	02:14:13
8	the storage of that information is still done in a	02:14:13
9	flash memory.	02:14:13
10	You seem to be continuing to say that if the	02:14:13
11	device the whole device is in a flash memory,	02:14:13
12	then it doesn't then it doesn't apply or my	02:14:13
13	experience doesn't apply, and I disagree with that.	02:14:13
14	The the reality here, if you look at if	02:14:13
15	you look at the way the cells store the information,	02:14:13
16	the way the cells are constructed according to the	02:14:13
17	embodiment, this is not any different from how it's	02:14:13
18	done in an e-squared CMOS PAL. It's just that the	02:14:13
19	information stored is different information.	02:14:13
20	So if if your if your suggestion is	02:14:13
21	accurate that the patentee believes that flash	02:14:13
22	memory is a very broad thing, then I definitely meet	02:14:13
23	the requirements, because the information stored in	02:14:14
24	a CMOS PLD is stored in a flash memory array. It's	02:14:14
25	not consumer data, as you've talked about before,	02:14:14

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1	but it's still information stored in a flash array,	02:14:14
2	so I think I don't have a problem with this.	02:14:14
3	Q The only thing I'm asking is: Would you	02:14:14
4	clear the bar or not?	02:14:14
5	A And I think I do and for the reasons I just	02:14:14
6	said.	02:14:14
7	Q So let me ask you this: You understand what	02:14:14
8	memory devices are; right, because you wrote that in	02:14:14
9	your declaration in paragraph 9?	02:14:14
10	A Yes.	02:14:14
11	Q What's a memory device?	02:14:14
12	A Well, that's a very big subject.	02:14:14
13	Q Well, what did you mean when you wrote it in	02:14:14
14	paragraph 9?	02:14:14
15	A I I meant any any type of a device that	02:14:14
16	stores memory. So it could be a whole device. It	02:14:14
17	could be a portion of a device. It's a device.	02:14:14
18	It's a it's a it's a it's a thing that	02:14:14
19	performs a certain function.	02:14:14
20	Q So if I said "flash memory device," what does	02:14:14
21	that mean to you?	02:14:14
22	A It means a device that remembers something,	02:14:14
23	and where I mean device when I say "device," I	02:14:14
24	mean it could be a whole device; it could be a	02:14:14
25	portion of a device which stores stores	02:14:14

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1	information. Therefore, it's memory and it uses a	02:14:14
2	flash technique to do it.	02:14:14
3	Q And is all non-volatile memory with regard to	02:14:14
4	this discussion we are having now flash memory? Are	02:14:14
5	those co-terminus?	02:14:14
6	A No. All non-volatile memory is not flash	02:14:14
7	memory. We have covered that pretty much earlier, I	02:14:14
8	believe.	02:14:14
9	Q So this last clause that we have been	02:14:14
10	discussing, "the working in the field of	02:14:14
11	non-volatile memory devices," if that said "working	02:14:14
12	in the field of flash memory devices," the flash	02:14:14
13	memory devices version would be narrower.	02:14:14
14	Would you agree with that?	02:14:14
15	A Of flash memory yes, I would agree with	02:14:14
16	that.	02:14:14
17	Q And it's your testimony that you have three	02:14:14
18	years or more of relevant experience working in the	02:14:14
19	field of flash memory devices?	02:14:14
20	A As I've said as I've said before, the	02:14:14
21	storage of information in a CMOS e-squared CMOS	02:14:14
22	PAL is done in a flash memory array. The fact that	02:14:14
23	the data is logical configuration is doesn't make	02:14:14
24	any difference. The underlying technology is still	02:14:14
25	flash cells in an organization with word lines and	02:14:14
		I

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1	bit lines and columns and rows, same thing. And,	02:14:14
2	yes, that would that qualifies that, along	02:14:14
3	with my other experience, qualifies me easily.	02:14:14
4	Q Is the CMOS memory array, the one you are	02:14:14
5	referring to, the one you worked on at Hughes?	02:14:14
6	A No.	02:14:14
7	Q Is a CMOS memory array which CMOS memory	02:14:14
8	array are you referring to in the statement that you	02:14:14
9	just said?	02:14:15
10	A The e-squared CMOS PAL devices were done at	02:14:15
11	National.	02:14:15
12	Q Those devices were done before flash memory	02:14:15
13	was even invented; isn't that right?	02:14:15
14	A They were done before individual flash memory	02:14:15
15	chips were invented, yes.	02:14:15
16	Q So you are relying on that experience to get	02:14:15
17	you over the three-years-of-relevant-experience	02:14:15
18	barrier?	02:14:15
19	A Yes. It had thin gate oxide. It was	02:14:15
20	programmed electrically. It was erased	02:14:15
21	electrically, and it was a flash array.	02:14:15
22	Q I believe we said earlier we asked about	02:14:15
23	when flash memory was invented, and you said circa	02:14:15
24	1984; is that right?	02:14:15
25	A Yes.	02:14:15

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1	Q	Since 1984, have you had three years or more	02:14:15
2	of rel	evant experience working in the field of flash	02:14:15
3	memory	devices?	02:14:15
4	A	So I think there's something that you missed	02:14:15
5	here.	The the the the e-squared-CMOS-PAL	02:14:15
6	work c	ontinued through '89, which is after when	02:14:15
7	flash	was invented.	02:14:15
8	Q	So let me ask the same question: Since 1984,	02:14:15
9	do you	have three years or more of relevant	02:14:15
10	experi	ence working in the field of flash memory	02:14:15
11	device	s?	02:14:15
12	A	Yes, I believe I do.	02:14:15
13	Q	And what is that three years composed of?	02:14:15
14	A	It's composed of the time I spent doing the	02:14:15
15	e-squa	red CMOS PAL.	02:14:15
16	Q	Anything else?	02:14:15
17	A	For flash.	02:14:15
18	Q	Right.	02:14:15
19	A	I don't believe so, other than the work at	02:14:15
20	the IT	С.	02:14:15
21	Q	With regard to the work you did at the ITC	02:14:15
22	relate	d to the flash memory, we already mentioned	02:14:15
23	that w	as a litigation consulting project; right?	02:14:15
24	A	Yes.	02:14:15
25	Q	It didn't involve any design of memory?	02:14:15

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1	A Didn't involve any design. Well, it depends	02:14:15
2	upon what you mean by "design."	02:14:15
3	Q Let me ask a different question.	02:14:15
4	In connection with that project, you did not	02:14:15
5	design any flash memory; is that right?	02:14:15
6	A Do you do you consider analyzing	02:14:15
7	analyzing programming circuits for multilevel flash	02:14:15
8	cells to be design?	02:14:15
9	Q No.	02:14:15
10	A So you don't think design has any analyzation	02:14:15
11	portion to it?	02:14:15
12	Q I'm not trying to define design. I'm just	02:14:15
13	asking a question.	02:14:15
14	And my question is: Did you do any memory	02:14:15
15	design in connection with that ITC project?	02:14:15
16	MR. LIMBACH: Objection; form.	02:14:15
17	THE WITNESS: And I'm and I'm only trying	02:14:15
18	to answer the question. There are many different	02:14:15
19	aspects to doing a design. One of the aspects is	02:14:15
20	analysis. You analyze things. You see how they	02:14:15
21	work. You may do some simulations. That's part of	02:14:15
22	design.	02:14:15
23	Did I do that type of work with respect to	02:14:15
24	the ITC matter that we are presently talking about?	02:14:15
25	The answer is yes. I did analysis to understand	02:14:15

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1	what the patent was talking about and how the patent	02:14:15
2	work worked and how the prior art that was	02:14:16
3	involved in that matter worked also.	02:14:16
4	BY MR. HEINZ:	02:14:16
5	Q Did you do any simulations in connection with	02:14:16
6	that ITC case?	02:14:16
7	A I don't recall right now that I did, but I	02:14:16
8	may have. I don't I don't remember. I don't	02:14:16
9	remember.	02:14:16
10	Q Beyond analyzing the patents and doing the	02:14:16
11	analysis work you just mentioned, did you do any	02:14:16
12	other design of flash memory in connection with your	02:14:16
13	ITC project?	02:14:16
14	A Well, I actually had an interesting idea,	02:14:16
15	having been involved in that in that memory at	02:14:16
16	the ITC and spent some time looking at potential	02:14:16
17	ways to increase the endurance of multilevel flash	02:14:16
18	cells compared to ways that I saw in other patents	02:14:16
19	that I pulled after the ITC case was over, I	02:14:16
20	pulled some patents from SanDisk because it had come	02:14:16
21	to my attention that retention and endurance seemed	02:14:16
22	to be very big problems for the multilevel cell	02:14:16
23	flash, and I thought maybe there would be some	02:14:16
24	given my background as a device guy, maybe there	02:14:16
25	would be some insights that I could find and maybe	02:14:16

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1	come up with something new and exciting that I	02:14:16
2	could that I could sell. So I did do that, but I	02:14:16
3	didn't I didn't do, like, an end-to-end design	02:14:16
4	if if you know, from beginning to to	02:14:16
5	finished product, no.	02:14:16
6	Q Did you come up with anything as a result of	02:14:16
7	that exercise?	02:14:17
8	A I I came up with something, but I I	02:14:17
9	wasn't sure I wasn't sure it was going to make	02:14:17
10	that much of a difference. But it continues to be a	02:14:17
11	problem in the industry in that for every every	02:14:17
12	time they move the technology, the endurance level	02:14:17
13	of these cells, the new cells in the new technology,	02:14:17
14	goes down, down, down, down.	02:14:17
15	So in the old days, cell programmability was	02:14:17
16	maybe you get 100,000 write/erase cycles. Now those	02:14:17
17	numbers are down to about a thousand, so it	02:14:17
18	continues to be a problem. If I had a good	02:14:17
19	solution, I could probably make a lot of money, but.	02:14:17
20	Q Maybe some day.	02:14:17
21	A I don't know.	02:14:17
22	Q Mr. Murphy, in any of these expert witness	02:14:17
23	cases that you have worked on that are listed on	02:14:17
24	page 1 to 2 of your CV	02:14:17
25	A Yes.	02:14:17

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1	Q that we talked about earlier, in any of	02:14:17
2	those cases, have you had any opinions rejected by	02:14:17
3	the Court or by the Patent Office?	02:14:17
4	MR. LIMBACH: Objection; form.	02:14:17
5	THE WITNESS: Not to my knowledge, no.	02:14:17
6	BY MR. HEINZ:	02:14:17
7	Q Do you know what a Daubert motion is?	02:14:17
8	A I have heard the name. Is it sorry. Not	02:14:17
9	a lawyer. Is it a move-to-strike testimony? I	02:14:17
10	don't you will have to describe it to me. That's	02:14:17
11	how little I know.	02:14:17
12	Q It's a challenge to an expert's opinion that	02:14:17
13	they didn't do the proper analysis or they don't	02:14:17
14	have the proper foundation to opine on the issue. I	02:14:17
15	mean, generally, that is what it is.	02:14:17
16	A Okay.	02:14:17
17	Q And a successful Daubert motion would cause	02:14:17
18	you not to be able to testify about certain things.	02:14:17
19	A Yeah, I don't know if I was involved in one	02:14:17
20	of those or not.	02:14:17
21	Q You may be; you may not be. You just don't	02:14:17
22	know one way or the other?	02:14:17
23	A Nobody specific that I that I recall,	02:14:17
24	nobody specifically came to me and said, "You can't	02:14:17
25	testify about this."	02:14:17
		1

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1	MR. HEINZ: Is this a good time for lunch?	02:14:17
2	MR. LIMBACH: Sure.	02:14:17
3	THE VIDEOGRAPHER: Going off the record, the	02:14:17
4	time now is 12:47.	02:14:17
5	(Lunch recess taken.)	02:14:18
6	000	02:14:18
7		02:14:18
8		
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1	AFTERN	COON SESSION	2:15 P.M.	02:14:18
2				02:16:06
3		THE VIDEOGRAPHER: Very good. The	video is	02:16:06
4	rollin	d.		02:16:06
5		The time now is 2:15. This also ma	rks the	02:16:07
6	beginn	ing of Tape 3.		02:16:10
7		Please proceed.		02:16:12
8	BY MR.	HEINZ:		02:16:14
9	Q	Welcome back.		02:16:14
10	A	Thank you.		02:16:15
11	Q	I would like to ask a few more ques	tions just	02:16:15
12	to fol	low up on some points we were talkin	g about	02:16:20
13	before	lunch regarding paragraphs 8 and 9	in your	02:16:22
14	declar	ation. Get those out, please.		02:16:26
15	A	Yes.		02:16:34
16	Q	Do you have any experience working	with NAND	02:16:34
17	flash?			02:16:41
18	A	No, I don't believe I do.		02:16:42
19	Q	So if in paragraph 9 the last claus	e said	02:16:49
20	"worki	ng in the field of NAND flash memory	devices,"	02:16:57
21	you wo	uld not be one of ordinary skill in	the art;	02:17:02
22	is tha	t right?		02:17:04
23	A	And you are dropping non-volatile?		02:17:04
24	Q	Right.		02:17:08
25		If I replaced let me let me j	ust ask	02:17:10

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1	the que	stion again.	02:17:12
2	A	Yes.	02:17:13
3	Q	In paragraph 9 of your declaration you give	02:17:13
4	an opin	ion about the level of ordinary skill in the	02:17:18
5	art rel	ated to the '045 patent; is that right?	02:17:20
6	A	Yes.	02:17:23
7	Q	And the last clause, which relates to the	02:17:24
8	relevan	t experience, reads "working in the field of	02:17:30
9	non-vol	atile memory devices"?	02:17:32
10	A	It does.	02:17:35
11	Q	And, in your view, the level of skill of	02:17:36
12	ordinar	y skill in the art would either be a Bachelor	02:17:42
13	of Scie	nce Degree in electrical engineering and five	02:17:46
14	years of	f relevant experience or a Master of Science	02:17:47
15	degree	in electrical engineering and three years of	02:17:51
16	relevan	t experience working in the field of	02:17:54
17	non-vol	atile memory devices?	02:17:55
18	A	Yes. That's what it says here in	02:17:58
19	paragra	ph 9.	02:18:00
20	Q	And you have a Master of Science in	02:18:01
21	electri	cal engineering?	02:18:03
22	A	I do.	02:18:03
23	Q	So if the last clause, instead of saying	02:18:04
24	"workin	g in the field of non-volatile memory	02:18:09
25	devices	" read "working in the field of NAND flash	02:18:12

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1	memory devices," would you be one of ordinary skill	02:18:16
2	in the art or not?	02:18:22
3	MR. LIMBACH: Objection; form.	02:18:23
4	THE WITNESS: I I don't have three years	02:18:24
5	of relevant experience on NAND flash memory devices,	02:18:28
6	so, no, I would not be.	02:18:33
7	BY MR. HEINZ:	02:18:34
8	Q I would like to move on and talk about some	02:18:44
9	of the claim constructions in this case.	02:18:46
10	A Okay.	02:18:48
11	Q They start on page 6 of your declaration	02:18:49
12	or the section about claim construction starts on	02:18:58
13	page 6 of the declaration.	02:19:01
14	Are you with me there?	02:19:02
15	A I am.	02:19:05
16	Q How did you go about coming up with these	02:19:10
17	constructions?	02:19:13
18	A Well, first, I read the patent and the and	02:19:14
19	the application and the parent patent, except for	02:19:26
20	the specification in the parent is identical to the	02:19:31
21	child, so only the claims are different there. And	02:19:35
22	then once I had the background of the patent, then I	02:19:40
23	came into discussion with counsel about what the	02:19:47
24	claim terms should be.	02:19:52
25	Q And you arrived at the constructions that you	02:19:57

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1	offered in your declaration; is that right?	02:19:59
2	A I did.	02:20:00
3	Q In paragraph 13 of your declaration, you	02:20:03
4	first explain that, in order to properly evaluate	02:20:12
5	the '045 patent, the terms of the claims must first	02:20:16
6	be interpreted?	02:20:19
7	A Yes.	02:20:23
8	Q And you go on to say that it's your	02:20:23
9	understanding that they are to be given their	02:20:26
10	broadest reasonable interpretation in light of the	02:20:28
11	specification?	02:20:29
12	A Yes.	02:20:29
13	Q And it's your further understanding that	02:20:33
14	claim terms are given their ordinary and accustomed	02:20:35
15	meaning as would be understood by one of ordinary	02:20:37
16	skill in the art unless the inventor acts as his own	02:20:40
17	lexicographer?	02:20:45
18	A Correct.	02:20:46
19	Q And is that what you did here?	02:20:47
20	A Yes.	02:20:49
21	Q And, in your view, the inventor did not act	02:20:49
22	as a lexicographer with regard to any of these	02:20:55
23	terms; is that right?	02:20:58
24	A That's correct.	02:20:59
25	Q I would like to start out with the term	02:20:59

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1	"logic low voltage," which is on page 7, starting at	02:21:01
2	paragraph 16 or, actually, take that back. It's	02:21:07
3	just paragraph 16 of your declaration.	02:21:12
4	A I'm there.	02:21:16
5	Q In your view, a person of ordinary skill in	02:21:17
6	the art would understand that the term "logic low	02:21:21
7	voltage," as used in the '045 patent, means a low	02:21:26
8	voltage such as ground or Vss; is that right?	02:21:30
9	A Yes.	02:21:33
10	Q With regard to your construction, the portion	02:21:34
11	after the comma, the "such as ground or Vss"	02:21:40
12	portion?	02:21:43
13	A Yes.	02:21:44
14	Q Is that limiting, in your view?	02:21:44
15	A I don't think it's limiting because it	02:21:48
16	it's the words "such as" are words that define	02:22:05
17	what an example would be.	02:22:08
18	Q So the "such as ground or Vss" just provides	02:22:10
19	nonlimiting examples; is that right?	02:22:14
20	A Yes.	02:22:16
21	Q Let me move on to logic high voltage, which	02:22:16
22	is paragraph 17 of your declaration?	02:22:28
23	A I have it.	02:22:33
24	Q And for logic high voltage, in your view, the	02:22:34
25	proper construction is a positive voltage higher	02:22:40

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1	than the logic low voltage such as Vcc.	02:22:43
2	Do you see that?	02:22:46
3	A I do.	02:22:47
4	Q Is the "such as Vcc" in this construction	02:22:47
5	also a nonlimiting example?	02:22:52
6	A Yes.	02:22:53
7	Q So neither of the "such as" clauses limits	02:22:55
8	the scope of those definitions?	02:23:00
9	A I don't believe that it does, no. It just	02:23:08
10	gives an example.	02:23:11
11	Q Now, going back to logic low voltage, which	02:23:12
12	is on the previous page, paragraph 16.	02:23:16
13	A Yes.	02:23:21
14	Q The term you are construing, "logic low	02:23:21
15	voltage," the first wor word in there is	02:23:24
16	"logic."	02:23:26
17	Do you see that?	02:23:28
18	A I do.	02:23:29
19	Q In your definition, it just begins with: A	02:23:29
20	low voltage, and then gives the nonlimiting	02:23:35
21	examples.	02:23:39
22	So it appears that the term "logic" is not	02:23:40
23	included in your proposed construction; is that	02:23:43
24	right?	02:23:45
25	A Well, I don't necessarily think that's true.	02:23:45
		1

1	Two of the the two examples given for logic low	02:24:14
2	voltage, ground and Vss, are well known to one of	02:24:19
3	ordinary skill in the art to be a logic low voltage.	02:24:24
4	Q But those are nonlimiting examples, as we	02:24:27
5	just established; is that right?	02:24:30
6	A That's correct. So in the case of a ground	02:24:31
7	signal, the voltage could be a .01 volts or .1 volts	02:24:34
8	or 50 millivolts. I think one of ordinary skill in	02:24:42
9	the art would still understand that it doesn't have	02:24:46
10	to be exactly ground or exactly Vss to be a low	02:24:49
11	voltage and that the two examples there are voltages	02:24:53
12	commonly understood to be related to logic levels to	02:24:59
13	one of ordinary skill in the art.	02:25:02
14	Q But since those examples are nonlimiting, all	02:25:04
15	it needs to do to satisfy your construction is be a	02:25:09
16	low voltage; is that right?	02:25:13
17	A Well, I think this term is is broad enough	02:25:14
18	to meet the scope of how it's used in the claim,	02:25:23
19	and and if you if you do much more than this,	02:25:29
20	then you are going to be importing limitations from	02:25:44
21	the specification, and I don't think that's proper.	02:25:47
22	Q In the original term "logic low voltage,"	02:25:51
23	what does the "logic" word mean?	02:25:55
24	A Well, "logic," to one of ordinary skill in	02:25:59
25	the art, is a form of usage of the devices to	02:26:08

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```
02:26:13
 1
      implement logic.
                                                                   02:26:14
 2
             The term "logic low voltage" actually doesn't
                                                                   02:26:17
 3
      appear in the specification anywhere, so one of
                                                                   02:26:21
      ordinary skill reading the claim and then reading
 4
                                                                   02:26:23
 5
      the specification will use their knowledge of what a
      logic low voltage is, and it's a low voltage such as
                                                                   02:26:30
 6
 7
      ground or Vss. It doesn't -- it's not limited to
                                                                   02:26:36
                                                                   02:26:39
 8
      ground or Vss. It just needs to be a low voltage
                                                                   02:26:44
 9
      and -- and -- and that's all.
                                                                   02:26:49
             So to the ex- -- let me start over.
10
         0
                                                                   02:26:54
11
             So the original term "logic low voltage,"
                                                                  02:27:02
12
      what would the difference be between a logic low
                                                                   02:27:04
13
      voltage and a low voltage if you omitted the word
                                                                   02:27:09
14
      "logic" from the phrase, if any?
15
                                                                   02:27:12
         Δ
             Well, I think the only thing that the word
                                                                   02:27:26
16
      "logic" brings to the other two words in logic low
      voltage is that the level is low enough so as to
                                                                   02:27:33
17
18
      effectively be a logic 0.
                                                                   02:27:40
19
             But that's not reflected in your proposed
                                                                   02:27:43
         0
20
      construction, is it?
                                                                   02:27:46
                                                                   02:27:46
21
             Well, it is when you look at the examples
         Α
2.2
      that are given.
                                                                   02:27:49
23
             But the examples are nonlimiting, so they
                                                                   02:27:50
         0
                                                                   02:27:52
2.4
      don't --
                                                                   02:27:55
25
             But there aren't --
         Α
```

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1	Q I'm sorry.	02:27:56
2	Because the examples are nonlimiting, they	02:27:57
3	don't limit the scope to a low voltage that	02:27:59
4	represents a logic low.	02:28:01
5	Would you agree with that?	02:28:03
6	A Well, I agree that the phrase "a low voltage	02:28:04
7	such as ground or Vss" is very broad, but I also	02:28:10
8	understand that one of ordinary skill in the art is	02:28:16
9	going to be looking at these terms and understanding	02:28:18
10	from the specification how they are to be used. And	02:28:24
11	when I apply a broadest reasonable interpretation,	02:28:31
12	then this is what I came to.	02:28:38
13	Q How high could a voltage be and still be a	02:28:39
14	low voltage in accordance with the construction that	02:28:45
15	you have provided in paragraph 16?	02:28:50
16	A Well, it cannot be so high as to be	02:28:52
17	considered a high voltage, which I identified in	02:28:58
18	column sorry, paragraph 17. So it is it's	02:29:02
19	also a number that varies depending upon which	02:29:11
20	technology you are using, how if you are if	02:29:15
21	you are asking what an absolute number would be, it	02:29:19
22	varies for different process technologies.	02:29:22
23	Q Let me confine my question to the '045 patent	02:29:28
24	and the technology in the '045 patent.	02:29:36
25	With that, how high could a voltage be and	02:29:41

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1	still be a low voltage in accordance with your	02:29:44
2	proposed construction?	02:29:48
3	A And you are looking at and you are looking	02:29:49
4	for a number here?	02:29:53
5	Q Yes.	02:29:55
6	A Well, given the embodiment, it would have to	02:29:58
7	be a voltage well, given the embodiment and	02:30:09
8	the well, the the embodiment says so the	02:30:22
9	embodiment specifically says a low voltage as	02:30:50
10	grounded; for example, column 7, line 34, "With BLO	02:30:53
11	grounded." So that's the only that's the only	02:30:58
12	definition we see from the embodiment itself.	02:31:08
13	There's no definition in the claim. The	02:31:12
14	claims language as I've already stated, a logic	02:31:17
15	low voltage, that phrase is only used in the claim.	02:31:20
16	It's never used in the patent. So the you would	02:31:25
17	have to for the particular embodiment shown in	02:31:29
18	the patent, you would have to look at the things	02:31:33
19	that are controlled by this low logic logic low	02:31:37
20	voltage.	02:31:46
21	So, for example, if we go to claim 1, the	02:31:51
22	next two elements from the bottom, it says "a logic	02:31:57
23	low voltage is applied to source select control line	02:32:01
24	to turn off source select transistors." So the	02:32:08
25	voltage must be below a voltage that the transistors	02:32:11

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1	would turn on at, commonly called the VT.	02:32:16
2	So I don't recall seeing in the patent what	02:32:21
3	the VT of a very of a specific NMOS transistor is	02:32:27
4	in this technology. So it's very difficult to say	02:32:33
5	what that logic low voltage absolutely is, but it	02:32:42
6	clearly, from the claims language, has to be a	02:32:48
7	voltage low enough so that the source select	02:32:50
8	transistors, for example, are off.	02:32:54
9	Q Your construction doesn't say any of that,	02:32:57
10	though; is that right?	02:33:00
11	A My construction doesn't say that. It's a	02:33:00
12	very broad construction.	02:33:06
13	Q If I was trying to determine whether a	02:33:06
14	particular product fell within the scope of these	02:33:09
15	claims using your construction, how would I know	02:33:13
16	whether the voltage was low enough to fit within the	02:33:18
17	scope of your proposed construction?	02:33:21
18	A Well, the reason that the proposed	02:33:24
19	construction is the way it is, is that the	02:33:26
20	definition that you just asked for actually comes in	02:33:29
21	the rest of the line of the sentence of the claim.	02:33:34
22	So the the sentence in the claim says: A	02:33:37
23	logic low voltage is applied to source select	02:33:41
24	control line. That tells you where it goes. It's	02:33:44
25	the next portion of the claim that tells you,	02:33:48
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1	effectively, how low that voltage has to be. It has	02:33:51
2	to turn off source select transistors.	02:33:54
3	Now, if we weave that information to turn off	02:33:59
4	the source select transistors into the claims term,	02:34:02
5	then, effectively, it's duplicated and the rest of	02:34:07
6	the sentence there is redundant; you don't need it.	02:34:10
7	So I didn't feel it was appropriate to put it into	02:34:14
8	the claim term for a logic low voltage.	02:34:16
9	Q But you felt it was appropriate to provide a	02:34:19
10	construction for logic low voltage, which is a	02:34:21
11	construction that's in paragraph 16 of your	02:34:24
12	declaration; isn't that right?	02:34:26
13	A Yes.	02:34:27
14	Q And your construction redefines logic low	02:34:28
15	voltage to be a low voltage and then includes a	02:34:32
16	nonlimiting example; isn't that right?	02:34:36
17	A Yes. As we have talked about, there is	02:34:38
18	there's no limitation to the voltage. Either of the	02:34:45
19	two voltages expressed in my construction would	02:34:50
20	qualify to satisfy the second portion of the	02:34:57
21	sentence in the claims term.	02:35:01
22	Q Is it your view now that your construction	02:35:03
23	can be either ground or Vss, but not other values?	02:35:07
24	A No. The the language is "such as." They	02:35:11
25	are given as as examples. It's it's still	02:35:22

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1	nonlimiting, it just gives most people understand	02:35:24
2	ground or Vss to be the same thing, especially	02:35:30
3	read when read in light of this patent. But as I	02:35:34
4	talked about before, a number of very close to	02:35:38
5	ground would qualify just as well, and it's not	02:35:41
6	actually ground. It's maybe 10 millivolts.	02:35:45
7	Q How close?	02:35:49
8	A Close enough to meet the requirements for the	02:35:52
9	rest of the sentence that is listed in the claim.	02:35:54
10	Q And what what number is that? If you	02:35:58
11	don't know, you don't know.	02:36:03
12	A Well, the the the term generally used	02:36:04
13	by a person of ordinary skill is a number below the	02:36:08
14	threshold of the transistor of the source select	02:36:12
15	transistors.	02:36:16
16	Q So is your oh	02:36:17
17	A So	02:36:17
18	Q I'm sorry. Go ahead.	02:36:18
19	A given that the patentee didn't describe	02:36:19
20	any of this, one of ordinary skill in the art would	02:36:21
21	understand that, you know, given given the other	02:36:24
22	technological details they see here, that the	02:36:27
23	threshold is probably somewheres of those	02:36:30
24	transistors, is probably lower than a volt, but	02:36:34
25	it's it it is not apropos, I don't think, to	02:36:40
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1	bring specific voltages into this patent claim,	02:36:48
2	given that it's written so broadly.	02:36:51
3	Q Well, didn't you in your analysis apply these	02:36:53
4	exact constructions to specific voltages in the	02:36:57
5	Nakai reference and then opine that the Nakai	02:37:01
6	reference anticipates on that basis?	02:37:03
7	A Well, that's just the easiest way to make the	02:37:06
8	comparison.	02:37:10
9	Q I I understand that.	02:37:11
10	Is that why you did it?	02:37:11
11	A No. I did it because the the	02:37:12
12	the reference the Nakai reference has the very	02:37:15
13	same structure, the almost the very same voltage	02:37:19
14	levels as defined in the specification here on the	02:37:23
15	'045. Okay? They are applied in the same way, and	02:37:28
16	they are used to generate actions that are identical	02:37:30
17	to what's shown here in claims 1 and claims 4.	02:37:36
18	Q Is there any upper limit, in your view, on	02:37:39
19	your construction for logic low voltage which is a	02:37:44
20	low voltage such as ground or Vss?	02:37:48
21	A Yes, there is.	02:37:50
22	Q What is it?	02:37:53
23	A Well, I've tried to explain this before, that	02:37:54
24	in the element claim that's in in the element of	02:37:58
25	claim 1 that says, "a logic low voltage is applied	02:38:05

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1	to a source select control line to turn off source	02:38:08
2	select transistors." So there are voltages that	02:38:12
3	will not turn off those source select transistors,	02:38:15
4	and so those voltages would not qualify as logic low	02:38:18
5	voltages.	02:38:22
6	Q So you need the rest of the claim, then, in	02:38:23
7	order to determine whether a logic low voltage falls	02:38:26
8	within the scope of your definition?	02:38:30
9	MR. LIMBACH: Objection; form.	02:38:33
10	THE WITNESS: Well, it is true that if I pick	02:38:39
11	a voltage and arbitrarily declare it to be a logic	02:38:41
12	low voltage and then I apply it to the selected bit	02:38:47
13	lines or the selected control line, is the example I	02:38:52
14	was using, and it does not turn off the source	02:38:56
15	select transistors, then, first of all, this claim	02:38:59
16	wouldn't be met, and, secondly, since the claim	02:39:03
17	wouldn't be met and it requires this, the claim	02:39:08
18	requires this, that would lead one of ordinary skill	02:39:11
19	in the art to understand that that voltage is not a	02:39:14
20	logic low voltage, because it didn't turn the	02:39:17
21	transistors off.	02:39:20
22	BY MR. HEINZ:	02:39:21
23	Q And, again, none of that is reflected in your	02:39:21
24	construction?	02:39:25
25	A The construction is appropriate for the	02:39:27

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1	broadness of the claim, and	02:39:30
2	Q Right.	02:39:32
3	A and it has in it what it has in it.	02:39:33
4	Q I understand.	02:39:36
5	But I my question is: That entire	02:39:37
6	explanation you gave about turning on, turning off,	02:39:40
7	whatever the case may be, none of that's in your	02:39:43
8	construction; is that right?	02:39:46
9	A And it doesn't have to be.	02:39:47
10	Q I'm not asking whether it has to be or not,	02:39:49
11	in your opinion. I'm just saying, it's not there.	02:39:52
12	Can we agree on that?	02:39:54
13	A Yeah, it's it's not there.	02:39:55
14	Q And if I was trying to evaluate a particular	02:39:57
15	voltage in a particular product, I would have no way	02:40:00
16	of knowing whether it was low enough or not to fall	02:40:04
17	within your definition of logic low voltage other	02:40:07
18	than whether it had the aspects of the rest of the	02:40:10
19	claim you pointed to; is that right?	02:40:15
20	A Given how broadly the claim is written, yes,	02:40:16
21	that's correct.	02:40:22
22	Q Let me move on to logic high voltage, which	02:40:22
23	is in paragraph 17 of your declaration.	02:40:34
24	You with me?	02:40:46
25	A I am.	02:40:47

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1	Q So here, again, we have the "such as" clause,	02:40:47
2	and I believe we already discussed that that's also	02:40:52
3	a nonlimiting example; is that right?	02:40:54
4	A Yes.	02:40:56
5	Q So logic high voltage does not have to be	02:40:56
6	Vcc?	02:40:59
7	A That is correct.	02:41:00
8	Q Could be higher. Could be lower; is that	02:41:01
9	right?	02:41:04
10	A It's possible, yes.	02:41:04
11	Q How high could a voltage be and still fall	02:41:05
12	within the scope of your construction?	02:41:13
13	A Well, it wouldn't be so high as to force	02:41:17
14	programming to happen in the flash cells, so it	02:41:36
15	would have it would have to be less than that.	02:41:40
16	Q And, again, that's not reflected in your	02:41:44
17	construction here, is it?	02:41:47
18	A I wrote the construction based on what I see	02:41:48
19	was needed from the claim, and I didn't see that	02:41:53
20	that was needed, so it's not in there.	02:41:57
21	Q Again, your construction omits the word	02:41:59
22	"logic" in the sense that it references it relative	02:42:09
23	to the logic low voltage we have talked about, but	02:42:14
24	not in relation to the high voltage; is that right?	02:42:16
25	MR. LIMBACH: Objection; form.	02:42:19
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THE WITNESS: I'm sorry. Could you read	02:42:21
that	02:42:23
BY MR. HEINZ:	02:42:23
Q Let me let me ask let me ask a	02:42:23
different question.	02:42:25
So, before, we discussed the base term "logic	02:42:26
low voltage."	02:42:31
Do you remember that?	02:42:32
A Yes.	02:42:33
Q This base term is "logic high voltage"?	02:42:33
A Yes.	02:42:38
Q How is the logic part of that base term	02:42:38
reflected in your construction, if at all?	02:42:41
A Well, it's reflected in the fact that it's a	02:42:43
positive voltage higher than the logic low voltage,	02:42:54
so logic low would, in in generic terms, be	02:42:57
something that is a zero, and logic high would be a	02:43:02
positive voltage that doesn't give you a logic load;	02:43:06
gives you a one.	02:43:09
Q But you don't have a number for me?	02:43:10
A There are no numbers in the claims. Why	02:43:12
why does this term need a number? And if I gave it	02:43:17
a number, that would really limit this patent;	02:43:20
because as soon as the technology changed, then this	02:43:26
claim would be stuck with a number that somebody	02:43:29
	<pre>THE WITNESS: I'm sorry. Could you read that BY MR. HEINZ: Q Let me let me ask let me ask a different question. So, before, we discussed the base term "logic low voltage." Do you remember that? A Yes. Q This base term is "logic high voltage"? A Yes. Q How is the logic part of that base term reflected in your construction, if at all? A Well, it's reflected in the fact that it's a positive voltage higher than the logic low voltage, so logic low would, in in generic terms, be something that is a zero, and logic high would be a positive voltage that doesn't give you a logic load; gives you a one. Q But you don't have a number for me? A There are no numbers in the claims. Why why does this term need a number? And if I gave it a number, that would really limit this patent; because as soon as the technology changed, then this claim would be stuck with a number that somebody</pre>

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1	else could easily get around by just changing the	02:43:33
2	technology, and that's not what anybody does when	02:43:36
3	they are writing broad patent claims.	02:43:42
4	Q So you don't have a number for me?	02:43:43
5	A No.	02:43:47
6	Q How much higher than the logic low voltage	02:43:47
7	does this need to be? Could it be a .1 volt? Does	02:43:55
8	it need to be at least a volt? What's that delta,	02:43:59
9	in your view, as a minimum?	02:44:02
10	A Well, the delta would be understood by one of	02:44:04
11	ordinary skill in the art as being related to the	02:44:08
12	particular logic low voltage that you are using, the	02:44:12
13	trip point of the circuitry that you are giving it	02:44:18
14	to, and the magnitude of additional voltage that you	02:44:20
15	would need, for instance, to cover noise margin,	02:44:25
16	etc.	02:44:30
17	So if you had a very a very sharp trip	02:44:33
18	point, the number could be quite small. It could	02:44:40
19	be, like you say, as a as low as a 10th of a	02:44:43
20	volt. And it if you have something that has not	02:44:48
21	such a sharp trip point function, it would require a	02:44:53
22	bigger a bigger voltage, so it's it's not easy	02:44:56
23	to say what exact voltage it is.	02:45:04
24	Q You don't have a number for me again; is that	02:45:09
25	right?	02:45:12
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1	A No; although, I've given an example in the	02:45:12
2	in the in the claims term.	02:45:18
3	Q Right, in that limited example, in your view?	02:45:19
4	A It's a it's a good example.	02:45:25
5	Q But it doesn't limit the scope of the	02:45:27
6	construction?	02:45:29
7	A No. It could be Vcc. It could be Vcc plus a	02:45:30
8	10th or minus a 10th, and they are all voltages that	02:45:35
9	will work in the in the claims language we	02:45:39
10	have in the claim elements we have at hand.	02:45:40
11	Q How high could this voltage be? Could it be	02:45:42
12	a hundred volts?	02:45:47
13	A For the technology shown in the patent, the	02:45:49
14	answer to that is no.	02:45:53
15	Q What's the highest it could be, in your view?	02:45:54
16	A Well, we talked or I talked about,	02:45:56
17	earlier, the fact that this voltage level needs to	02:46:01
18	be less than the voltage level to elicit	02:46:04
19	programming. Programming voltage in the preferred	02:46:08
20	embodiment is talked about as 15 to 20 volts, so I	02:46:11
21	think one of ordinary skill in the art reading the	02:46:16
22	material here in the patent would understand that	02:46:19
23	this that this number wouldn't be north of	02:46:22
24	15 volts; would not be higher than 15 volts.	02:46:26
25	Q But they would have to understand that	02:46:31

1	because that's not reflected in your construction;	02:46:32
2	is that right?	02:46:35
3	A Well, I didn't realize that constructions	02:46:35
4	were required to explain every possible element of	02:46:39
5	the claim language. It was my understanding that,	02:46:44
6	in fact, you do not bring specifics out of the	02:46:47
7	specification into the claims language so as to	02:46:55
8	limit the claims language, and the aspect of these	02:46:59
9	claim terms is the broadest reasonable definition,	02:47:06
10	and that's what I've used.	02:47:12
11	Q In your view, do the terms, as used in the	02:47:13
12	claim, "logic high voltage" and "logic low voltage"	02:47:22
13	limit the scope of the claim at all?	02:47:28
14	A Yes, they do.	02:47:33
15	So, for example, a logic the logic high	02:47:42
16	voltage in the claims language specifically is used	02:47:49
17	in sentences where it turns on transistors, and the	02:47:57
18	logic low voltage specifically is used in claims	02:48:04
19	in the claims in sentences that turn off	02:48:08
20	transistors. So the the limitation there is that	02:48:13
21	a logic low voltage is lower than a logic high	02:48:21
22	voltage is, and that's that's the limitation that	02:48:25
23	they bring to to the claims language.	02:48:32
24	Q Just that the logic low voltage has to be	02:48:34
25	lower than the logic high voltage?	02:48:37

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1	A It has to not only be that, but it also has	02:48:39
2	to be for instance, the logic high voltage has to	02:48:43
3	be able to turn on certain transistors, and the	02:48:46
4	logic vol low voltage has to be able to turn off	02:48:50
5	other transistors.	02:48:53
6	Q If those two phrases, "logic high voltage"	02:48:54
7	and "logic low voltage," were just replaced with the	02:48:58
8	word or the phrase "a voltage" in the claim,	02:49:00
9	would the scope of the claim be the same or	02:49:05
10	different?	02:49:08
11	MR. LIMBACH: Objection; form.	02:49:08
12	THE WITNESS: I think the scope of the claim	02:49:12
13	would be different because substituting just the	02:49:29
14	words "a logic" or, sorry, "a voltage" is an even	02:49:36
15	broader term than "a logic high voltage" or "a logic	02:49:41
16	low voltage," and so the scope of the claim, I	02:49:45
17	think, is would be actually even broader than	02:49:49
18	what's written here.	02:49:53
19	BY MR. HEINZ:	02:49:58
20	Q Earlier, you mentioned that to define the	02:49:58
21	numbers or define the ranges, you would look to the	02:50:01
22	rest of the claim language.	02:50:03
23	A Yes.	02:50:04
24	Q And what I'm getting at is, if you took out	02:50:04
25	"high voltage" and just put in "a voltage," you	02:50:12
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1	would still have the definition that comes from the	02:50:15
2	subsequent claim language, wouldn't you?	02:50:17
3	MR. LIMBACH: Objection; form.	02:50:19
4	THE WITNESS: Well, actually, no, I don't	02:50:22
5	I don't think that's true, because when you do	02:50:24
6	when you change "logic high voltage" to just	02:50:27
7	"voltage" and you change "logic low voltage" to just	02:50:29
8	"voltage," you now have no connection between the	02:50:32
9	two. The words "high" and "low" disappear, and so	02:50:36
10	it's less defining to do it that way than it is to	02:50:44
11	do it the way it was done.	02:50:47
12	BY MR. HEINZ:	02:50:50
13	Q But wouldn't one of skill in the art know	02:50:50
14	that one voltage had to be lower than the other from	02:50:52
15	the context of the claim?	02:50:56
16	A Context of the claim. I don't think just	02:50:57
17	from the context of the claim, no.	02:51:26
18	Q What if the term "logic low voltage" was	02:51:34
19	replaced with the term "a low voltage"?	02:51:44
20	A A	02:51:49
21	MR. LIMBACH: Objection; form.	02:51:51
22	BY MR. HEINZ:	02:51:52
23	Q Let me ask the same question except for,	02:51:52
24	instead of replacing "logic low voltage" and "logic	02:51:54
25	high voltage" in the claim, we replace those with	02:51:58
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1	the terms "low voltage" and "high voltage"	02:52:02
2	respectively.	02:52:06
3	Would that change the scope of the claim?	02:52:07
4	MR. LIMBACH: Objection; form.	02:52:08
5	THE WITNESS: I think it would. I think it	02:52:10
6	would remove from the reader the the concept that	02:52:20
7	it was that it was a specific voltage that they	02:52:28
8	wanted to put on these lines.	02:52:36
9	For a part like a CMOS part, logic high	02:52:44
10	voltage is very often the the most positive power	02:52:49
11	supply rail that you have, and a logic low voltage	02:52:57
12	is the lowest power supply rail that you have, being	02:53:00
13	that CMOS is used to generate signals that go rail	02:53:03
14	to rail.	02:53:09
15	So if you change the words like that, I think	02:53:11
16	you I think you remove information from the	02:53:15
17	specification I mean the the claims language	02:53:20
18	that impart a certain type of knowledge to the	02:53:26
19	reader, and without them, then I believe the	02:53:30
20	knowledge just wouldn't be the same.	02:53:33
21	BY MR. HEINZ:	02:53:35
22	Q So if I replaced "logic low voltage" with	02:53:35
23	just "low voltage," that would deprive the reader of	02:53:39
24	the knowledge regarding the scope of the claim like	02:53:44
25	you said; is that right?	02:53:47

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1	A I think so.	02:53:48
2	And and, of course, you know, we have the	02:53:51
3	situation here where the patentee had all the	02:53:53
4	language in the world available to him, and he	02:53:56
5	didn't use terms that are in the specification. He	02:54:02
6	used unique terms in the claims, and he had the	02:54:05
7	opportunity, for instance, to say instead of	02:54:10
8	saying "a logic high voltage," he the patentee	02:54:14
9	could have said "a Vcc voltage is applied to said	02:54:17
10	bit line select control line to turn on the bit line	02:54:22
11	select transistors," and the patentee chose not to	02:54:24
12	do that.	02:54:27
13	So the patentee here specifically avoided	02:54:28
14	using specific voltage numbers, I believe, in an	02:54:32
15	effort to make the claim broad, and I believe that's	02:54:38
16	exactly that's true for the the "logic high	02:54:42
17	voltage" term and the "logic low voltage" term, and	02:54:46
18	I believe that's that's what the patentee	02:54:49
19	intended. Clearly, the patentee could have written	02:54:53
20	in a Vcc voltage or a Vss voltage and didn't.	02:54:56
21	And in in in keeping with that, the	02:55:02
22	the constructions that that I've come up with	02:55:07
23	follow that broadness and preserve, I think, to the	02:55:10
24	best of our ability, the the intent of what the	02:55:14
25	patentee wrote in the claims.	02:55:17

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1	Q So if you replaced the term "logic low	02:55:18
2	voltage" in the claim with just "low voltage," would	02:55:32
3	that have the same scope or not?	02:55:38
4	MR. LIMBACH: Objection; form.	02:55:42
5	THE WITNESS: The same scope. And when you	02:55:43
6	refer to "scope," you are referring to?	02:55:47
7	MR. HEINZ: The scope of the claim.	02:55:50
8	MR. LIMBACH: Same objection.	02:55:52
9	THE WITNESS: And sorry. One more time.	02:55:55
10	You want to replace "logic low voltage" with?	02:56:06
11	MR. HEINZ: "Low voltage." I want to omit	02:56:10
12	the word "logic."	02:56:11
13	THE WITNESS: You want to omit the word	02:56:12
14	"logic."	02:56:13
15	BY MR. HEINZ:	02:56:13
16	Q And I'm asking you if the claim would have	02:56:14
17	the same scope if we omit the word "logic" from	02:56:15
18	"logic low voltage" as it does in the form you see	02:56:18
19	right there?	02:56:22
20	A Yeah, I think	02:56:23
21	MR. LIMBACH: Objection; form.	02:56:25
22	THE WITNESS: I think it does change the	02:56:27
23	scope, and and part of the reason that I say that	02:56:29
24	is the patentee could have left the word "logic"	02:56:33
25	out, easily, and just said a low voltage is applied	02:56:37

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1	to this guy and high voltage is applied to that guy.	02:56:40
2	Either way, had the patentee done that, we he	02:56:43
3	still didn't specify what the voltage level was,	02:56:46
4	right? But the fact that the patentee chose to	02:56:50
5	include that word means it meant something to the	02:56:55
6	patentee, and I think it's you know, it's	02:57:00
7	understandable for one of ordinary skill in the art	02:57:04
8	to understand what a logic high voltage level is and	02:57:06
9	a logic low voltage level is.	02:57:09
10	And very commonly, as I've said and I've	02:57:12
11	put in the the claims terms there's "such as	02:57:15
12	ground or Vss" or "such as Vcc."	02:57:18
13	BY MR. HEINZ:	02:57:23
14	Q But it could be something different than	02:57:23
15	that, in your view?	02:57:24
16	A It is possible to be something different,	02:57:25
17	yes. It's not nailed down to be exactly Vcc or Vss	02:57:27
18	or ground.	02:57:31
19	Q So just to summarize, you agree that the	02:57:32
20	scope would be different if we replaced the term	02:57:35
21	"logic low voltage" in the claim with "low voltage"?	02:57:39
22	MR. LIMBACH: Objection; form.	02:57:44
23	THE WITNESS: I think it would be, yes.	02:57:45
24	BY MR. HEINZ:	02:57:47
25	Q Same question with regard to "logic high	02:57:49
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1	voltage"; if we replace that with just "high	02:57:50
2	voltage," would the scope of the claim be different?	02:57:54
3	A I think it does change change the scope,	02:57:55
4	yes.	02:58:02
5	Q Let me ask you about boosted positive	02:58:02
6	voltage, which you address at paragraph 18 of your	02:58:10
7	declaration.	02:58:14
8	A Yes, I have it.	02:58:15
9	Q What does "boosted" mean in "boosted positive	02:58:16
10	voltage," in your view?	02:58:22
11	A In my view, it's the the "boosted" term is	02:58:23
12	a term that identifies to one of ordinary skill in	02:58:32
13	the art how that voltage is created and the fact	02:58:34
14	that it is above other positive voltages in in	02:58:39
15	the part.	02:58:46
16	Q Does it require that the voltage comes out of	02:58:46
17	a booster?	02:58:51
18	A I think one of ordinary skill in the art	02:58:52
19	in this was provision '96 in 96, reading this	02:59:18
20	claim, would understand that that boosted positive	02:59:24
21	voltage did come from a circuit that boosts voltage,	02:59:32
22	the reason being that the industry tried very hard	02:59:40
23	to get away from products that had two or three	02:59:43
24	power supplies required, and and there was a very	02:59:48
25	hard push to go to chips that ran off a single-power	02:59:52

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1	supply. So if you needed plus 12 inside and the	02:59:58
2	power supply you had to work with was five, you had	03:00:00
3	to find a way to create the 12-volt supply inside	03:00:03
4	the chip, and a boosting circuit it's not the	03:00:08
5	only use for a boosting circuit, but it's one of the	03:00:12
6	uses for a boosting circuit.	03:00:14
7	And so I believe that's that's what one of	03:00:17
8	ordinary skill in the art understands from the word	03:00:20
9	"boosted" in that positive voltage, the fact that	03:00:23
10	it's you know, it's created with a boosting	03:00:29
11	circuit and that it and that it's higher than the	03:00:31
12	other voltages that are considered high in the part.	03:00:36
13	Q You propose a construction for boosted	03:00:40
14	positive voltage of a positive voltage higher than	03:00:44
15	the logic high voltage.	03:00:48
16	Do you see that?	03:00:49
17	A I do.	03:00:50
18	Q So your proposed construction doesn't reflect	03:00:50
19	the the boosting concept that you just discussed;	03:00:53
20	is that right?	03:00:56
21	A It doesn't have that in it, but I didn't feel	03:00:56
22	that it needed to be limited to to any particular	03:01:02
23	boosting circuit, so I didn't include it.	03:01:04
24	Q Does it need to be limited to a boosting	03:01:06
25	circuit, no matter what kind?	03:01:10

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1	A No. I'm happy with the construction I have.	03:01:12
2	I think it just has to be a positive higher voltage	03:01:15
3	than the logic high voltage.	03:01:19
4	Q The original base term has the word "boosted"	03:01:20
5	in it, and that concept does not appear, at least	03:01:28
6	that I can see, in the construction you have	03:01:34
7	provided.	03:01:36
8	Would you agree with that?	03:01:38
9	A That the term has the word "boosted" and	03:01:39
10	the and the construction does not have any	03:01:46
11	acknowledgment of the boosting? Is that what you	03:01:51
12	are asking about?	03:01:54
13	Q Close enough.	03:01:55
14	A Sorry. Yeah, I think I think I think	03:01:56
15	that's an accurate characterization.	03:02:17
16	Q So if in the claim we replace "boosted	03:02:18
17	positive voltage" with your proposed construction,	03:02:25
18	the concept of the boosting or the boosted aspect	03:02:26
19	would be lost.	03:02:29
20	Do you agree with that?	03:02:31
21	A It would be lost literally in the language,	03:02:32
22	but it wouldn't be lost to a person of ordinary	03:02:39
23	skill in the art who builds these devices.	03:02:42
24	Q Why not?	03:02:44
25	A Because they understand that to have only a	03:02:45

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1	single-power-supply product and yet provide a	03:02:47
2	voltage in the range of 15 to 20 volts to do	03:02:51
3	programming, it requires some sort of a boosting	03:02:54
4	circuit.	03:02:57
5	Q So you think boosting is implicit in the	03:02:58
6	remainder of the claim language?	03:03:04
7	A Once you have removed oh, you mean once	03:03:05
8	you have taken the boosted positive voltage claim	03:03:08
9	out and substituted in my construction.	03:03:11
10	Q That's right.	03:03:15
11	A Yes. I think it is because of this is the	03:03:21
12	high voltage this is the boosted voltage that's	03:03:26
13	applied to a selected word line, and it's during	03:03:28
14	programming, and that description is very succinctly	03:03:33
15	laid out in the programming operation of the patent	03:03:38
16	in column 7, starting around line 26.	03:03:40
17	Q So the answer to my question is, it is	03:03:43
18	implicit in the remainder of the claim if you were	03:03:51
19	to replace "boosted positive voltage" with your	03:03:54
20	proposed construction?	03:03:56
21	A Yes.	03:03:57
22	Q Getting back to logic high voltage that we	03:03:59
23	talked about a minute ago, could a logic high	03:04:03
24	voltage fall within the scope of the claim and be	03:04:07
25	boosted?	03:04:12

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1	MR. LIMBACH: Objection; form.	03:04:24
2	THE WITNESS: And so so the part of the	03:04:29
3	hypothetical you are asking that I don't understand	03:04:43
4	is boosted from what?	03:04:44
5	MR. HEINZ: Vcc.	03:04:52
6	MR. LIMBACH: Objection; form.	03:04:52
7	THE WITNESS: Well, I think I think the	03:04:54
8	answer to that is that no one of ordinary skill in	03:05:08
9	the art would understand that to be viable or useful	03:05:11
10	in that Vcc is already a logic high voltage. You	03:05:17
11	don't need to boost it any more to be another logic	03:05:25
12	high voltage, and so I don't I don't think	03:05:29
13	that's I don't think that's a a reasonable	03:05:35
14	hypothetical at all, no.	03:05:37
15	BY MR. HEINZ:	03:05:38
16	Q So if I had a voltage that was boosted from	03:05:41
17	Vcc, that couldn't be a logic high voltage in the	03:05:47
18	scope within the scope of the claim?	03:05:50
19	A Well, one of the boosted high voltages is the	03:05:52
20	one called "boosted positive voltage"	03:06:00
21	Q Right.	03:06:03
22	A which is which is the one provided or	03:06:04
23	applied to a selected word line to enforce or make	03:06:05
24	programming happen.	03:06:11
25	Q So we agree that could be boosted and be	03:06:12

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1	within the scope of the claim?	03:06:15
2	A Yes.	03:06:16
3	Q Because the base term says "boosted"?	03:06:16
4	A Yes.	03:06:20
5	Q The other term is "logic high voltage," which	03:06:21
6	does not say "boosted."	03:06:24
7	Could you have a boosted voltage that meets	03:06:27
8	the requirements of logic high voltage in the claim,	03:06:32
9	in your view?	03:06:36
10	MR. LIMBACH: Objection; form.	03:06:36
11	THE WITNESS: Well, the the boosted	03:06:43
12	positive voltage is associated with programming from	03:06:45
13	the claims language, so if you if you take if	03:06:49
14	you take a logic high voltage and you boost it, but	03:06:58
15	it's not high enough to provide programming, I just	03:07:05
16	don't see why anybody would do that. I it it	03:07:10
17	just doesn't there's no logical sense to ever do	03:07:14
18	that. I already have a logical high voltage. Why	03:07:18
19	would I boost it unless I'm going to use it for	03:07:22
20	programming; because, in these devices, that's the	03:07:25
21	only place where boosted voltages are used, in the	03:07:27
22	programming cells or circuits.	03:07:31
23	BY MR. HEINZ:	03:07:32
24	Q So in this context, the only place boosted	03:07:33
25	voltages are used as boosted positive voltage and	03:07:36

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1	not with logic high voltage?	03:07:39
2	A The boosted positive voltage is is is	03:07:41
3	used, and it's only applied to the selected word	03:07:44
4	line, which we know from the specification goes to	03:07:47
5	15 to 20 volts to elicit programming of the cell.	03:07:51
6	If you just put a logic high voltage there, that	03:07:57
7	would not program the cell, so by definition,	03:08:00
8	logic a logic high voltage won't work there.	03:08:07
9	Q My question is a little different than that.	03:08:09
10	Could you have a logic high voltage that came	03:08:14
11	out of a booster that was boosted to a higher level	03:08:20
12	than Vcc?	03:08:24
13	A But not so high as to be a programming	03:08:26
14	voltage?	03:08:33
15	Q Yes.	03:08:33
16	A Is it possible to do?	03:08:34
17	Q What I'm asking, not is it possible, but	03:08:38
18	would that fall within the scope of the claim?	03:08:40
19	A I don't I don't think it's part of the	03:08:42
20	part of the claim in that the claim doesn't talk	03:08:47
21	anywhere about boosted logic high voltages, so it's	03:08:59
22	not part from that aspect. If I look at the	03:09:03
23	function of what a logic high voltage is, I don't	03:09:06
24	need to boost it any more to get a logic high. I	03:09:10
25	already have one. So I just don't see that as being	03:09:14
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1	part of the claim.	03:09:25
2	Q Let me ask another question.	03:09:31
3	Could strike that. Let me ask a different	03:09:35
4	question.	03:10:02
5	With regard to boosted positive voltage, your	03:10:02
6	definition is a positive voltage higher than the	03:10:09
7	logic high voltage; is that right?	03:10:12
8	A Correct.	03:10:14
9	Q How much higher does it need to be than the	03:10:15
10	logic high voltage?	03:10:21
11	A Well, it needs to be high enough to to	03:10:23
12	to force programming to occur.	03:10:29
13	Q Do you have a number for me?	03:10:34
14	A Tell me the technology you want me to give	03:10:36
15	you the number in.	03:10:38
16	Q The scope of the '045 patent. If I have a	03:10:40
17	certain technology, how do I tell if I'm in or out?	03:10:42
18	A Well, you have to know what the programming	03:10:45
19	voltage is. In this in this in the scope of	03:10:48
20	this patent it for example, 15 to 20 volts;	03:10:51
21	column 7, line 27.	03:10:55
22	Q So the definition of boosted positive voltage	03:10:56
23	would change depending on the technology you applied	03:11:00
24	it to?	03:11:03
25	A Oh, absolutely. And, in fact, I believe	03:11:03

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1	that's why this claim was written this way, so that	03:11:07
2	it was broad enough so that as the technology	03:11:10
3	changed, you you would still have a boosted	03:11:13
4	positive voltage from somewhere.	03:11:18
5	So, for instance, in in these particular	03:11:22
6	cases, if you look at sorry. I have to find it.	03:11:25
7	An example is given in column 7, around line 22. It	03:11:37
8	talks about erase as opposed to programming, but the	03:11:42
9	numbers are similar: "The erase speed is primarily	03:11:45
10	a function of the field across the tunnel oxide	03:11:48
11	which can be, for example, approximately 8.5 to 10	03:11:52
12	megavolts per centimeter to achieve block erasure in	03:11:58
13	less than for example 1 millisecond."	03:12:03
14	So for this technology, which I believe the	03:12:07
15	tunnel oxide is given in column 5 at line 6: "The	03:12:20
16	next step involves forming the tunnel oxide by	03:12:26
17	growing a high quality thermal oxide, of for example	03:12:29
18	75 to 80 Angstroms to cover the whole wafer." For	03:12:32
19	that technology, the programming pulse to generate	03:12:38
20	the right number of megavolts per centimeter across	03:12:44
21	that oxide to create Fowler-Nordheim tunneling is 15	03:12:48
22	to 20 volts.	03:12:56
23	From a technology point of view, as you	03:12:56
24	shrink the power supply, you must also shrink the	03:12:59
25	tunnel oxide so that you don't have to create	03:13:03

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		1
1	it's very difficult to create boosted voltages that	03:13:09
2	are, let's say, orders of magnitude bigger than the	03:13:11
3	starting voltage. Okay?	03:13:15
4	In in the case in the in the case of	03:13:17
5	this patent, the Vcc is 5 volts and the programming	03:13:21
6	voltage is 5 15 to 20, so you are boosting up by	03:13:25
7	roughly a factor of four or five.	03:13:30
8	In a newer technology where the transistors	03:13:33
9	require a maximum Vcc of 3.3 volts, because of the	03:13:38
10	way the boosting circuits work, you actually have to	03:13:44
11	lower the gate the tunnel oxide even smaller so	03:13:47
12	that you can program them in a relatively scaled	03:13:51
13	voltage level.	03:13:55
14	So this is why I understand there are no	03:13:59
15	there are no numbers in in the patent claim	03:14:02
16	because it would be so limiting that once the	03:14:06
17	technology moved, the patent would be worthless, so	03:14:09
18	the examples given in the specification are just for	03:14:13
19	this technology. When you move to a different	03:14:18
20	technology, the absolute numbers change.	03:14:21
21	Q If I was designing a NAND flash memory that	03:14:23
22	did not yet exist, is it possible that I could meet	03:14:29
23	the other requirements of the claim but design	03:14:36
24	around the logic low voltage, logic high voltage,	03:14:39
25	and boosted positive voltage, or is that impossible?	03:14:43
		1

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1	MR. LIMBACH: Objection; form.	03:14:48
2	THE WITNESS: Sorry. I'll have to think	03:14:49
3	about that before I answer.	03:14:52
4	BY MR. HEINZ:	03:14:55
5	Q Do you understand my question?	03:14:55
6	A I think so.	03:14:56
7	Q In other words, if I met every requirement of	03:14:56
8	that claim except for these three terms, is there	03:14:59
9	any way that I could design around that claim by	03:15:02
10	falling outside the scope of logic low voltage,	03:15:06
11	logic high voltage, and boosted positive voltage	03:15:10
12	only?	03:15:12
13	MR. LIMBACH: Objection; form.	03:15:12
14	THE WITNESS: Well, that certainly sounds	03:15:14
15	like it calls for an opinion from me that I haven't	03:15:21
16	studied. And I don't think I have the time here to	03:15:24
17	do it justice. It's it's it's a complicated	03:15:35
18	question that you ask, and I think, at this point, I	03:15:43
19	would say that I can't answer without studying it	03:15:53
20	more.	03:15:55
21	BY MR. HEINZ:	03:15:55
22	Q Let me just ask the question with regard to	03:15:58
23	logic low voltage.	03:16:01
24	A Yes.	03:16:03
25	Q If you satisfied the rest of those claim	03:16:03

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1	elements and let's assume that you had a flash	03:16:07
2	memory that actually worked could you do it	03:16:10
3	without a logic low voltage in terms of the patent?	03:16:14
4	MR. LIMBACH: Objection; form.	03:16:20
5	THE WITNESS: A logic low voltage. Without a	03:16:21
6	logic low voltage. I don't think you can, no.	03:16:39
7	BY MR. HEINZ:	03:16:40
8	Q Let me ask the same question with logic high	03:16:41
9	voltage.	03:16:42
10	MR. LIMBACH: Same objection.	03:16:47
11	THE WITNESS: No, I don't think I don't	03:17:00
12	think you can do it without a logic, but because	03:17:01
13	once you remove those portions of the terms, you	03:17:10
14	you you end up with less information being given	03:17:30
15	to the person who is trying to interpret the claims.	03:17:33
16	We talked about this earlier, by where you	03:17:37
17	asked if you changed "logic high voltage" to just "a	03:17:41
18	voltage." I I think I think you change them	03:17:44
19	in a fashion that you don't give enough information	03:17:51
20	to to to follow the claim.	03:17:59
21	BY MR. HEINZ:	03:17:59
22	Q Beyond the fact that the logic low voltage is	03:18:17
23	lower than the logic high and the logic high voltage	03:18:21
24	is lower than the boosted positive, do those three	03:18:25
25	claim phrases add any other limitations besides that	03:18:30

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1	relative order?	03:18:35
2	A I think the only other thing added is the	03:18:52
3	is the oh, I'm sorry, you wanted me to limit it	03:19:03
4	to just those snippets; is that correct?	03:19:07
5	Q No.	03:19:11
6	A A log a logic low, a logic high, and a	03:19:11
7	boosted positive voltage and their relationships	03:19:13
8	between each other?	03:19:17
9	Q Let me ask a different question.	03:19:18
10	A Okay.	03:19:20
11	Q So it appears that your constructions for	03:19:21
12	logic low voltage, logic high voltage, and boosted	03:19:24
13	positive voltage are defined in such a way that the	03:19:28
14	only limiting aspect is that low is lower than high	03:19:32
15	and boosted positive is higher than high; is that	03:19:37
16	right? Or is there some other limiting aspect that	03:19:41
17	I'm missing?	03:19:43
18	A No, I believe that is that is the	03:19:44
19	limitations or those are the limitations.	03:19:47
20	Q And based on just those constructions and	03:19:49
21	right now putting aside the rest of the claim	03:19:53
22	language there's no magnitude requirements?	03:19:55
23	We talked about whether there was a number	03:20:00
24	associated with those, and I believe we established	03:20:02
25	that there was not; is that right?	03:20:03
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1	A That's correct.	03:20:05
2	Q And, finally, with regard to boosted positive	03:20:06
3	voltage, you could have a logic high voltage that	03:20:17
4	was I'm sorry. Strike that.	03:20:27
5	With regard to also those three terms, is	03:20:45
6	there any limitation on how close or far they need	03:20:50
7	to be in terms of a number?	03:20:56
8	In other words, how much higher than a logic	03:20:59
9	low voltage does a logic high voltage need to be and	03:21:03
10	how much higher than a boosted positive voltage	03:21:06
11	or, I'm sorry, how much let me start over.	03:21:10
12	So we are getting back to these three terms.	03:21:14
13	A Yes.	03:21:17
14	Q Okay?	03:21:17
15	A Got 'em.	03:21:19
16	Q Logic high voltage, logic low voltage, and	03:21:19
17	boosted, and you can think of those as defining two	03:21:23
18	ranges where logic low is on one end, logic high is	03:21:27
19	in the middle, boosted positive on the top.	03:21:30
20	A Yes.	03:21:33
21	Q You with me?	03:21:34
22	A Yes.	03:21:34
23	Q And that's what's reflected in your proposed	03:21:34
24	constructions.	03:21:38
25	A Correct.	03:21:38
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1	Q There's an interval between logic low voltage	03:21:38
2	and logic high voltage?	03:21:42
3	A Yes.	03:21:44
4	Q And there's another interval between logic	03:21:44
5	high voltage and boosted positive voltage?	03:21:47
6	A Correct.	03:21:50
7	Q Is there any limitation on how large or small	03:21:51
8	those intervals can be, in your view?	03:21:54
9	MR. LIMBACH: Objection; form.	03:21:56
10	THE WITNESS: Well, there's certainly no	03:21:58
11	limitations shown to us in absolute magnitude of	03:22:01
12	voltages from the claims language.	03:22:06
13	BY MR. HEINZ:	03:22:09
14	Q Nor is there in your construction; right?	03:22:10
15	A Nor is there in my construction. There is	03:22:11
16	only a single-preferred embodiment shown for a	03:22:14
17	particular technology, and as I've talked about	03:22:19
18	before, these voltages will vary as the technology	03:22:23
19	varies, so I think I think it's inappropriate to	03:22:26
20	put in specifics with respect to logic high voltage	03:22:36
21	or boosted positive voltage simply because it limits	03:22:39
22	the scope of the claim and and it's it's just	03:22:45
23	improper, at least how I've been explained how	03:22:50
24	patents work. And I don't think the patentee would	03:22:55
25	want that either because it you know okay? So	03:22:59

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1	maybe you have a patent from one generation of	03:23:03
2	technology, but then the next generation your	03:23:07
3	patent's out. That's that's not a that's not	03:23:10
4	a a broadly written patent.	03:23:12
5	So I I don't believe there's any value to	03:23:15
6	anybody to put numerical values on these on these	03:23:22
7	individual terms. And and as I said before, each	03:23:29
8	of the terms is then qualified by other language	03:23:33
9	that follows in the same sentence.	03:23:37
10	Q So those terms don't impart a limitation on	03:23:39
11	the respective magnitudes of those voltages other	03:23:47
12	that they be in relative order?	03:23:50
13	A I think that's correct, yes.	03:23:52
14	MR. WERNER: Can we take a short break?	03:24:07
15	THE WITNESS: Yeah, let's take a break.	03:24:11
16	MR. HEINZ: Sure.	03:24:13
17	THE VIDEOGRAPHER: Going off the record, the	03:24:13
18	time now is 3:24.	03:24:14
19	(Recess taken.)	03:24:15
20	THE VIDEOGRAPHER: Back on the record, the	03:47:22
21	time now is 3:47.	03:47:23
22	BY MR. HEINZ:	03:47:26
23	Q Welcome back.	03:47:26
24	A Thank you.	03:47:27
25	Q I would like to ask a couple questions now	03:47:28

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1	that kind of relate to several of these exhibits	03:47:30
2	that you have in front of you, but let's start out	03:47:33
3	with the '045 patent.	03:47:35
4	A Got it.	03:47:37
5	Q You got that in front of you?	03:47:37
6	A I do.	03:47:39
7	Q Claim 1, which is one of the claims we are	03:47:39
8	talking about today?	03:47:41
9	A Yes.	03:47:42
10	Q So, earlier, we were talking about the "logic	03:47:42
11	high voltage" term, and that actually appears twice	03:47:44
12	in the claim, once at approximately line 41 and once	03:47:47
13	at approximately line 48.	03:47:52
14	A Correct.	03:47:55
15	Q And the first logic high voltage is applied	03:47:56
16	to said bit line select control line, and the second	03:48:00
17	logic instance of logic high voltage is applied	03:48:06
18	to unselected word lines.	03:48:09
19	Do you see that?	03:48:10
20	A I do.	03:48:11
21	Q In your view, does	03:48:11
22	MR. LIMBACH: Go ahead. I didn't mean to cut	03:48:19
23	you off.	03:48:22
24	BY MR. HEINZ:	03:48:22
25	Q In your view, does the logic high voltage at	03:48:22
1		1

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1	41 refer to the same voltage as the logic high	03:48:24
2	voltage at approximately line 48, or can those be	03:48:28
3	different voltages?	03:48:32
4	MR. LIMBACH: Objection; form.	03:48:33
5	THE WITNESS: In in my view, they can be	03:48:34
6	different voltages. Had they been the same voltage,	03:48:37
7	I would have expected language in the second one to	03:48:43
8	say "the logic high voltage."	03:48:46
9	BY MR. HEINZ:	03:48:51
10	Q Or "said" would be another?	03:48:52
11	A Or "said," yes, would be another example.	03:48:53
12	Q So the absence of the words "the" or "said"	03:48:56
13	and the use of the word "a" indicates to you that	03:49:00
14	those could be different voltages?	03:49:02
15	A Yes, from the claims language. It's also	03:49:03
16	I would I would understand and one of ordinary	03:49:09
17	skill in the art would also understand that those	03:49:12
18	voltages may not be exactly identical in the chip	03:49:15
19	either.	03:49:17
20	Q Could they be?	03:49:17
21	A I think the right answer to that is it's	03:49:20
22	possible on the chip, but often not probable.	03:49:25
23	Q Why is that?	03:49:29
24	A Because making two voltages on a chip be	03:49:30
25	absolutely the same is actually quite difficult to	03:49:36
		1

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1	do.	03:49:38
2	Q Would these two voltages, in the context that	03:49:40
3	we are talking about here, putting aside the	03:49:49
4	whatever variation let me strike that.	03:49:52
5	So the logic high voltage at approximately	03:49:57
6	line 41 and the logic high voltage at approximately	03:50:00
7	line 48, could you design a flash memory where those	03:50:03
8	were nominally the same, even though they might have	03:50:07
9	some variation of a circuit like you were talking	03:50:10
10	about?	03:50:13
11	A I think, potentially, you might be able to,	03:50:13
12	yes.	03:50:16
13	Q Is there an advantage to having those be the	03:50:16
14	same versus two different values?	03:50:19
15	A I don't believe so because they provide two	03:50:21
16	different functions. That voltage provides two	03:50:27
17	different functions for the different connections	03:50:30
18	that it's made.	03:50:33
19	Q Let me draw your attention to Toshiba's	03:50:36
20	Petition for Inter Partes Review.	03:50:51
21	A Exhibit 11?	03:50:57
22	Q Exhibit 11, that's right	03:50:58
23	A Yes.	03:51:00
24	Q and, in particular, page 16. There's a	03:51:00
25	table there on the top of the page.	03:51:14
		1

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1		Do you see it?	03:51:15
2	A	I do.	03:51:16
3	Q	And it compares voltages in the '045 patent	03:51:16
4	to cla	ims 1 and 4 with voltages in Nakai?	03:51:20
5	A	Yes.	03:51:24
6	Q	So in your view I'm sorry, and there's one	03:51:27
7	more c	olumn that lists the array element on the left	03:51:31
8	side.		03:51:34
9	A	Correct.	03:51:34
10	Q	And those array elements correspond to	03:51:37
11	limita	tions in the claims?	03:51:40
12	A	Yes.	03:51:42
13	Q	So, again, as we looked with the claims, the	03:51:42
14	"logic	high" shows up twice in the '045 patent	03:51:47
15	column	?	03:51:51
16	A	Yes.	03:51:51
17	Q	Related to the BSL, which is the bit line	03:51:51
18	select	well, BSL is bit line select control line	03:51:57
19	in the	claim; right?	03:52:02
20	A	Correct.	03:52:04
21	Q	And, again, with unselected or, I'm sorry,	03:52:04
22	with u	nselected word lines is the second time?	03:52:07
23	A	That we see what?	03:52:13
24	Q	That "logic high" shows up in the '045 patent	03:52:14
25	column	•	03:52:20

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1	MR. LIMBACH: Objection; form.	03:52:20
2	THE WITNESS: Oh, I'm sorry, in the '04	03:52:21
3	so we have BSL. We have unselected word lines, you	03:52:23
4	said?	03:52:27
5	MR. HEINZ: Yeah, let me let me let me	03:52:27
6	start over.	03:52:28
7	Q So in the '045 column, "logic high" shows up	03:52:30
8	three different times.	03:52:34
9	A Correct.	03:52:37
10	Q And it shows up in connection, now looking at	03:52:37
11	the array element column, with BSL, with unselected	03:52:39
12	bit lines, and unselected word lines.	03:52:44
13	A Correct.	03:52:46
14	Q And, in your view, the voltage in Nakai for	03:52:46
15	the bit select line is 12 volts, which is a logic	03:52:53
16	high voltage, in your view; is that right?	03:52:58
17	A Yes.	03:53:00
18	Q And for the unselected bit lines and the	03:53:00
19	unselected word lines, the voltages are 10 volts?	03:53:04
20	A Correct.	03:53:09
21	Q Now, obviously you don't need to be an	03:53:10
22	engineer to see that 10 is different than 12.	03:53:18
23	A Yes.	03:53:21
24	Q So those are different voltages; right?	03:53:21
25	A Correct.	03:53:23
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1	Q But both of those different voltages are	03:53:24
2	logic highs.	03:53:25
3	A Correct.	03:53:26
4	Q In the Nakai patent	03:53:27
5	A I'm sorry. Wasn't that weren't we talking	03:53:32
6	about the Nakai?	03:53:35
7	Q Yes. I'm sorry.	03:53:35
8	A Oh.	03:53:35
9	Q I'm predicating another question.	03:53:38
10	A Sorry.	03:53:38
11	Q So I just I just wanted to get this table	03:53:40
12	out there so we had some common frame of reference.	03:53:41
13	A Okay.	03:53:44
14	Q And then I'm going to ask you a little bit	03:53:44
15	about these values in the Nakai patents, the 12 volt	03:53:46
16	and the 10 volt.	03:53:50
17	A Okay.	03:53:50
18	Q So, first of all, with regard before we	03:53:50
19	get into the specification, with regard to that,	03:53:52
20	let's I kind of want to ask you about the table	03:53:55
21	and the patent.	03:53:57
22	A Okay.	03:53:58
23	Q So let's kind of maybe if you can kind of	03:53:58
24	keep both of those in front of you there, then it	03:54:00
25	would be a little easier. Perfect.	03:54:03

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1	So I would like to start out just with regard	03:54:05
2	to the table. We talked about the logic high is a	03:54:07
3	12-volt value in Nakai, and then it shows up twice	03:54:12
4	as 10 volts in the table.	03:54:16
5	A Yes.	03:54:18
6	Q Let me ask you about the 12-volt number in	03:54:20
7	in Nakai.	03:54:24
8	Is that 12 volts in Nakai boosted?	03:54:25
9	MR. LIMBACH: Objection; form.	03:54:28
10	THE WITNESS: I don't believe Nakai	03:54:59
11	specifically quotes it as being boosted.	03:55:38
12	BY MR. HEINZ:	03:55:43
13	Q Is the 12 volts Vcc in Nakai?	03:55:43
14	A No, it's not Vcc. Hold on. So my	03:55:46
15	recollection is that I don't recall Vcc being talked	03:57:01
16	about in Nakai, and I'm trying to see if there is a	03:57:06
17	location that I've missed or I don't see Vcc	03:57:10
18	specifically being quoted as what voltage it is.	03:58:35
19	And I don't recall reading that it was set at a	03:58:52
20	specific voltage. I'm sure it is. It just whether	03:58:54
21	the patentee put it in the spec or not.	03:58:58
22	Q Before we dive in, let me ask you about the	03:59:05
23	Nakai.	03:59:09
24	Is that boosted?	03:59:10
25	MR. LIMBACH: Objection; form.	03:59:10

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1	THE WITNESS: So the 10 volts is boosted as	03:59:24
2	identified in the specification in column 20, around	03:59:27
3	line 18, and the	03:59:31
4	BY MR. HEINZ:	03:59:31
5	Q Okay. Let me I think the the portion	04:00:21
6	you were looking at here in column 20 is similar to	04:00:23
7	the portion I was looking at.	04:00:26
8	Let me, just for the record, read in the	04:00:27
9	portion you identified around line 18.	04:00:30
10	A Okay.	04:00:33
11	Q The potential of the power source VBITH of	04:00:37
12	the latch circuitry for the data register changes	04:00:41
13	from the external power source potential Vcc to the	04:00:44
14	power source VDPI potential 10 volts supplied from	04:00:48
15	the voltage booster built into the chip.	04:00:53
16	That's the part you were looking at; right?	04:00:57
17	A Correct.	04:00:58
18	Q So you would agree with me that the 10-volt	04:00:58
19	value is boosted from Vcc because it's supplied from	04:01:02
20	a voltage booster?	04:01:08
21	A That's	04:01:13
22	MR. LIMBACH: Objection; form.	04:01:14
23	THE WITNESS: That's correct.	04:01:15
24	BY MR. HEINZ:	04:01:18
25	Q And then if you look down a little further	04:01:18

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1	and now I'm looking at line 26.			
2	A	26.	04:01:26	
3	Q	The sentence reads:	04:01:26	
4		The power source potential VDPI	04:01:28	
5		supplied from the voltage booster	04:01:32	
6		has a small current supply	04:01:34	
7		capability generally of 1 milliamp	04:01:36	
8		or smaller; therefore, as the	04:01:39	
9		leakage current flows through the	04:01:42	
10		defective bit line, the power source	04:01:44	
11		VDPI potential becomes lower than	04:01:46	
12		12 volts.	04:01:50	
13	A	So I think you misread that. That's VBDI.	04:01:51	
14	Q	Oh, VBDI. I'm sorry.	04:01:54	
15	A	There's two. There's VPDI and a VBDI.	04:01:57	
16	Q	Okay. Gotcha.	04:02:05	
17	A	The but that still doesn't identify how	04:02:06	
18	many v	olts the Vcc is.	04:02:10	
19	Q	Right.	04:02:12	
20	A	The the the only other thing that I'm	04:02:20	
21	aware	of is Figure 1, which has VPP, VPI, VDPI,	04:02:22	
22	voltag	e generator circuit as a block for the device,	04:02:35	
23	but I		04:02:43	
24	Q	Is that a booster?	04:02:43	
25	A	Well, it's a voltage generator. It doesn't	04:02:46	

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1	really tell you if they they use boosting it or	04:02:48
2	not, but since the voltages are I think most	04:02:51
3	everybody generally agrees that this was probably a	04:02:53
4	5-volt Vcc part, so I would expect that they are all	04:02:56
5	boosted, yes.	04:03:00
6	Q And this voltage generator circuit is a	04:03:02
7	booster; is that right?	04:03:04
8	A Sorry. One second.	04:03:56
9	Yes, it's a booster circuit, but I think you	04:03:56
10	have you have missed the portion of the	04:03:59
11	description. You skipped over column 20, line 21	04:04:00
12	where it says:	04:04:05
13	Under these conditions, the node BLJ	04:04:06
14	of the data register connected to	04:04:10
15	the defective bit line becomes H	04:04:12
16	level by the preset operation, which	04:04:15
17	would basically be voltage high	04:04:19
18	level.	04:04:23
19	Q But we can agree that Vcc is lower than 10	04:04:23
20	and that both the 10-volt value and the 12-volt	04:04:30
21	value come from a booster.	04:04:33
22	Can we agree on that part?	04:04:38
23	A I believe that's correct, yes.	04:04:43
24	Q So with regard to the table I'm sorry.	04:04:44
25	Back in the the petition?	04:04:55
		1

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1	A Yes.	04:04:57
2	Q And, actually, I kind of want to ask a	04:04:57
3	question about the constructions again. Here, let's	04:05:03
4	get the the table in front of you and your	04:05:06
5	declaration again.	04:05:09
6	A Okay. And paragraph?	04:05:13
7	Q 17 and 18.	04:05:17
8	A 17. Yes.	04:05:19
9	Q Okay. We there?	04:05:19
10	A Yes.	04:05:21
11	Q So let me ask you about the 12-volt value in	04:05:21
12	Nakai, which appears adjacent to the VSL line in the	04:05:26
13	table, first of all.	04:05:31
14	A Yes.	04:05:32
15	Q So we agree that value is boosted, and since	04:05:33
16	12 volts is bigger than 10 volts, 12 volts is a	04:05:38
17	positive voltage higher than at least a logic high	04:05:42
18	voltage; is that right?	04:05:47
19	MR. LIMBACH: Objection; form.	04:05:48
20	THE WITNESS: 12 volts is higher than a logic	04:05:50
21	high voltage well, no. 12 volts is just another	04:05:53
22	logic high voltage.	04:06:01
23	BY MR. HEINZ:	04:06:02
24	Q So 10 volts is logic high voltage?	04:06:02
25	A Also, yes.	04:06:04

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1	Q	Right.	04:06:05
2		But 10 volts is logic high voltage?	04:06:06
3	A	Yes.	04:06:08
4	Q	12 volts is more than 10; right?	04:06:08
5	A	Yes.	04:06:10
6	Q	And the 12-volt value is boosted?	04:06:11
7	A	That's correct.	04:06:15
8	Q	So with regard to your construction of	04:06:17
9	booste	d positive voltage, which is a positive	04:06:22
10	voltag	e higher than the logic high voltage, why	04:06:26
11	doesn'	t 12 volts fit that construction?	04:06:34
12	A	Because it won't work in that claim.	04:06:38
13	12 vol	ts in Nakai will not program the devices.	04:06:48
14		So the claim specifically states the '045	04:06:51
15	states	that the preface of the section that we	04:06:52
16	are ta	lking about says "wherein, during	04:06:55
17	progra	mming," and so the 12-volt level is is not	04:06:58
18	a leve	l that's applied to the selected word line	04:07:11
19	during	programming, so it can't be what I mean,	04:07:14
20	the cl	aim says "a boosted positive voltage is	04:07:23
21	applie	d to a select word line." From from here,	04:07:26
22	the se	lected word line in the under the array	04:07:33
23	amount	element column is down one, two, three,	04:07:37
24	four -	- five. It says "selected word line," and	04:07:39
25	when w	e look at the voltages under Nakai, it says	04:07:43

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1	that level is 20 volts.	04:07:45
2	Q So the the determinative aspect of whether	04:07:47
3	it's a boosted positive voltage or not is whether	04:07:51
4	it's applied to the selected word line and not the	04:07:54
5	magnitude or something that's related to the	04:07:58
6	construction you provided for boosted positive	04:08:01
7	voltage?	04:08:03
8	A No. I don't think that's the right	04:08:04
9	characterization. I think that if we or one of	04:08:06
10	ordinary skill in the art looks at this and	04:08:12
11	"looks at this" being the '045, claim 1 and looks	04:08:15
12	at Nakai and says, "Okay. I'm looking for a boosted	04:08:20
13	positive voltage which is applied to a selected word	04:08:23
14	line during programming," and there's only one	04:08:26
15	answer in Nakai that meets that, and it's the VPP of	04:08:32
16	20 volts, so that that in Nakai has to be the	04:08:38
17	boosted positive voltage.	04:08:41
18	Q Why would	04:08:45
19	A The	04:08:45
20	Q oh, I'm sorry. Go ahead.	04:08:48
21	A The the other voltages, 10 volts and	04:08:49
22	12 volts, won't work there, and one of ordinary	04:08:52
23	skill in the art in these devices would know that.	04:08:55
24	Q So the 12-volt value on the bit select line	04:09:00
25	is not a boosted positive voltage, in your view,	04:09:07
		1

		1			
1	why?	04:09:12			
2	A Because in the claim, the only boosted				
3	positive voltage is applied to a very specific spot	04:09:18			
4	and used during a very specific operation. It's	04:09:23			
5	only applied to the selected word line, and it's	04:09:27			
6	only supplied at that boosted level, that boosted	04:09:31			
7	positive voltage level during programming.	04:09:35			
8	During other portions of the operation, it is	04:09:38			
9	not allowed to go that high for fear of incorrectly	04:09:40			
10	programming other cells.	04:09:45			
11	Q So the fact that the the 12 volts comes	04:09:50			
12	from a booster is not determinative one way or the	04:09:57			
13	other as to whether it's boosted positive?	04:10:02			
14	A Boosted positive voltage. No. I don't	04:10:06			
15	think I don't believe it is, no.	04:10:11			
16	And as and as we talked about before, a	04:10:20			
17	logic high voltage doesn't have in this claim,	04:10:23			
18	they don't have to be the same logic high voltage	04:10:27			
19	based on the language of the claim.	04:10:30			
20	And as I also talked about, the there are	04:10:33			
21	two different functions of the voltage applied to	04:10:38			
22	the two different places that you identified in	04:10:41			
23	claim 1, about line 41 and about line 48. The first	04:10:45			
24	logic high voltage is used to turn on bit line	04:10:53			
25	select transistors, while the second logic high	04:10:58			

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1	voltage is applied to the unselected word lines	04:11:01
2	such such that, effectively, they will not be	04:11:07
3	misprogrammed during a program function.	04:11:11
4	Q In the '045 patent, does it use two different	04:11:14
5	logic high voltages in any of the embodiments?	04:11:54
6	A Two different so if we look at the	04:11:56
7	answer, I believe is, yes. If we look at column 6,	04:12:21
8	line 50 well, it starts at 48 under the title of	04:12:27
9	"Erase Operation." It says, "In the exemplary	04:12:32
10	biasing convention described herein, cells are	04:12:37
11	erased by the action of applying negative gate	04:12:40
12	voltage of, for example, minus 12 to minus 15 volts	04:12:43
13	on the selected word lines or a single word line	04:12:49
14	(WL1), and applying a voltage approximately equal to	04:12:57
15	Vcc (e.g., Vcc minus 2Vtn to Vcc) on the selected	04:13:04
16	bit lines or a single bit line (e.g., BL0)."	04:13:24
17	So it clearly says here that Vcc can span	04:13:38
18	from Vcc minus 2Vtn to Vcc, and those voltages would	04:13:42
19	be, effectively, logic high voltages; because if we	04:13:57
20	actually turn to claim 2, we see that the very same	04:14:01
21	terms, "a logic high voltage," is listed in claim 2,	04:14:12
22	which is the erase claim at starting at line 2,	04:14:18
23	and "a logic high voltage" is also listed at	04:14:23
24	line 10.	04:14:28
25	And so, in that case, the patentee has used	04:14:28

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		1
1	the words "logic high voltage" in the erase mode to	04:14:34
2	specifically talk about voltage levels between Vcc	04:14:38
3	minus 2Vn Vtn and Vcc.	04:14:43
4	Q What is "Vtn"?	04:14:47
5	A "Vtn" is the threshold voltage of an	04:14:49
6	end-channel transistor, roughly about 7/10ths of a	04:14:54
7	volt. So if Vcc was 5 minus 2Vtn would span from,	04:14:57
8	if I can do the math in my head, 3.6 to 5 volts.	04:15:04
9	Q So you agree that, in this example, in the	04:15:13
10	context of the patent, the logic high could be in	04:15:16
11	the range of Vcc to Vcc minus 2Vtn?	04:15:19
12	A I wouldn't normally express it that way.	04:15:26
13	Lower voltages first	04:15:28
14	Q Okay. Sorry.	04:15:28
15	A upper upper voltages second	04:15:32
16	Q Yeah, let me	04:15:33
17	A so	04:15:33
18	Q let me fix that.	04:15:34
19	So you would agree in the patent, a logic	04:15:34
20	high voltage could be between Vcc minus 2Vtn and	04:15:36
21	Vcc, which would be a higher voltage?	04:15:42
22	A Correct. That's what this example in	04:15:44
23	column 6 tells us.	04:15:48
24	Q And this example is for erase, but you would	04:15:49
25	apply that same reasoning to the claims at issue;	04:15:53

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1	right, the claims 1 and 4?	04:15:55
2	A I I would believe so, yes.	04:15:57
3	Q Let me go back to your declaration now, which	04:15:58
4	is I believe it's that one. I would like to ask	04:16:13
5	you about paragraph 24, which begins on page 11 and	04:16:23
6	spans through to page 12.	04:16:25
7	A Yes.	04:16:39
8	Q So in that section you say:	04:16:40
9	One skilled in the art would also	04:16:47
10	have understood, as inherent from	04:16:50
11	Nakai, that the additional bit lines	04:16:51
12	beyond BL2 in Figures 22A and 23A	04:16:52
13	that were not intended to be	04:16:58
14	programmed would have the same	04:17:00
15	voltage (i.e., VDPI) as that being	04:17:04
16	applied to BL2 so that memory cells	04:17:10
17	in those columns (i.e., non-right	04:17:15
18	cells) are not programmed.	04:17:20
19	Do you see that?	04:17:23
20	A I do.	04:17:23
21	Q So it's your view that it's inherent that	04:17:24
22	those would all have the same voltage in the context	04:17:41
23	of that sentence I just read?	04:17:46
24	A That they would have the same voltage applied	04:17:47
25	to them, VDPI, within the restrictions, as we talked	04:17:59

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1	about before, that it's impossible in a chip to make	04:18:06
2	all the voltages be exactly identical.	04:18:09
3	Q Okay. That that was my first question.	04:18:11
4	When you say the "same" here, do you mean	04:18:13
5	exactly the same or you mean they could be different	04:18:15
6	within some variation?	04:18:17
7	A I mean that as a normal engineer would	04:18:18
8	understand it, that he intended to apply VDPI, and	04:18:23
9	with within the limitations of the circuitry he	04:18:28
10	has to work with, he did apply VDPI or thereabouts	04:18:31
11	that, in effect, makes all of the bit lines work in	04:18:37
12	the same fashion.	04:18:43
13	Q Could you design one where you did not use	04:18:44
14	the same voltage for every bit line and it would	04:18:47
15	still work?	04:18:51
16	MR. LIMBACH: Object to the form.	04:18:51
17	THE WITNESS: So if you are asking me, "Is it	04:18:57
18	possible to do?" my first answer would be no, given	04:19:06
19	that your intention is to make a product that's the	04:19:18
20	same size as the product you started with, the	04:19:22
21	reason being is that this voltage is applied across	04:19:29
22	many places in the in the array, and if you now	04:19:38
23	suggest to me that, "Well, I want to build one where	04:19:42
24	that voltage is different in all of those places"	04:19:46
25	BY MR. HEINZ:	04:19:48
		1

1	Q Well, let's just say different in at least	04:19:49
2	two places. Half of them could be one voltage; half	04:19:51
3	of them could be the other.	04:19:55
4	In other words, they don't all have to be	04:19:56
5	different. There just has to be any one that's	04:19:58
6	different than any other one.	04:20:01
7	A Hold on a second.	04:20:02
8	MR. LIMBACH: Objection; form.	04:20:11
9	THE WITNESS: And and what is your	04:20:12
10	definition of different?	04:20:23
11	MR. HEINZ: Any voltage greater than the	04:20:28
12	minor variation that you discussed with regard to	04:20:30
13	your use of the same voltage.	04:20:34
14	THE WITNESS: And you simply want to know if	04:20:43
15	it's possible to do?	04:20:45
16	MR. HEINZ: Yes.	04:20:46
17	THE WITNESS: I need more information about	04:21:06
18	the hypothetical.	04:21:08
19	Are we talking about within one page of	04:21:10
20	memory or multiple pages of memory within the same	04:21:16
21	array, within different arrays, sub-arrays?	04:21:22
22	BY MR. HEINZ:	04:21:22
23	Q So in paragraph 23 of your declaration, you	04:21:28
24	point out that Nakai only shows a memory array with	04:21:36
25	two columns of cells but that one would of skill	04:21:39
		1

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1	in the art would understand that's only a portion of	04:21:43
2	the full array.	04:21:45
3	Do you see that?	04:21:46
4	A That's correct.	04:21:47
5	Q So what I want to know is: For the portion	04:21:47
6	that's not shown, which you contend one of skill in	04:21:53
7	the art would know it existed, is it possible to	04:21:58
8	design the rest of that missing portion such that it	04:22:01
9	includes different voltages for the additional bit	04:22:06
10	lines?	04:22:13
11	MR. LIMBACH: Objection; form.	04:22:15
12	THE WITNESS: And we are talking about a	04:22:16
13	program operation; right?	04:22:38
14	MR. HEINZ: Yes, I believe. It's whatever	04:22:42
15	the operation is you are referring to in	04:22:44
16	paragraph 24 of your declaration.	04:22:46
17	THE WITNESS: Yes. Yeah, so it is a program	04:22:48
18	operation, not intended to be programmed, at the	04:22:53
19	bottom of the page.	04:22:57
20	So the problem is the the problem with the	04:23:05
21	hypothetical that you have is the following: If you	04:23:23
22	will turn to Figure 23A, which is the programming	04:23:27
23	figure of	04:23:31
24	BY MR. HEINZ:	04:23:31
25	Q Of Nakai?	04:23:32

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1	A Nakai, you will see one of the word lines	04:23:33
2	specifically connected to VPP, which is the	04:23:37
3	program it will be the programming voltage.	04:23:40
4	Q Right.	04:23:43
5	A Okay?	04:23:43
6	Now, the bit lines that we are talking about,	04:23:46
7	Bit Line 1 there is held to zero volts, it says, and	04:23:49
8	Bit Line 2 is held to the voltage VDPI.	04:23:52
9	So the function of the VDPI voltage is to	04:24:03
10	guarantee that the memory cells circled in the	04:24:10
11	right-hand column of cells, which you will follow an	04:24:15
12	arrow to the right to Figure 23C, and you will see	04:24:21
13	that the the label on the drain of that or	04:24:25
14	source of that transistor, the fact that it has VDPI	04:24:29
15	voltage connected to that drainer source. It also	04:24:34
16	have VPP connected to the gate. And right next to	04:24:39
17	that it says "non-right cell."	04:24:43
18	So the intent here is to never program those	04:24:48
19	cells that are, effectively, not selected.	04:24:53
20	Q Right.	04:24:59
21	And then VDPI, it points out, is the	04:25:00
22	right-inhibited drain voltage, which is consistent	04:25:03
23	with what you just said; right?	04:25:05
24	A Correct. And it guarantees that you don't	04:25:07
25	get enough voltage across the stack of polys and	04:25:11

1	over the thin oxide so as to induce Fowler-Nordheim	04:25:16
2	injection. Okay?	04:25:22
3	So to answer your question, one of the most	04:25:24
4	difficult things in this type of design is to make	04:25:31
5	sure that you don't partially write cells that are	04:25:34
6	unselected. So that means that, to the best of the	04:25:38
7	designer's ability, you want to ensure that the VDPI	04:25:46
8	voltage for all the columns that are next to	04:25:51
9	column 2 that are not selected all have the same or	04:25:54
10	as close to possible as the same exact voltage.	04:25:59
11	Okay? Because if you don't do that, you have the	04:26:03
12	problem of so you talked about, Couldn't I supply	04:26:08
13	that from two sources; correct?	04:26:12
14	Q Yes.	04:26:15
15	A So the problem with that is unless those two	04:26:16
16	voltages are absolutely matched, these portions of	04:26:20
17	that array so now let's say we have a left	04:26:25
18	portion and a right portion. I may not get the same	04:26:28
19	performance out of those two portions of the array	04:26:32
20	because I have partially written some of the cells	04:26:36
21	that I didn't intend to.	04:26:41
22	So your question to me was, Is it possible to	04:26:44
23	do? And the answer I have for you is that if you	04:26:49
24	in in the example I've given, if you wanted to	04:26:55
25	really use bad design form, it is possible. It is	04:26:57

1	not, however, standard practice or a good practice	04:27:04
2	within the array of cells that you are trying to	04:27:09
3	program at that point.	04:27:13
4	Q So it's possible that you could have	04:27:15
5	different voltages, but it wouldn't be the preferred	04:27:18
6	practice?	04:27:20
7	A It it's I I don't know that I've	04:27:24
8	ever seen that done or discussed in any literature	04:27:26
9	about flash memories I've ever read, so it's I	04:27:30
10	don't I don't consider that preferred practice an	04:27:37
11	equivalent statement. It it's at a minimum,	04:27:44
12	would be frowned upon.	04:27:50
13	Q But it's possible?	04:27:51
14	A But if you wanted to be if you wanted to	04:27:52
15	be so poorly selective, you might choose it.	04:27:59
16	Q So it's possible?	04:28:06
17	A I don't know what kind of I don't think	04:28:09
18	you will get anywhere near as good a performance,	04:28:11
19	but it it's it's possible to do anything once.	04:28:14
20	Well, sometimes.	04:28:19
21	Q Let me go back and I would like to ask you	04:28:20
22	about the petition again, and this time I would like	04:28:29
23	to ask you a few questions about the Nakai claim	04:28:33
24	chart, which I believe begins on page 17.	04:28:36
25	A Yes, it does.	04:28:44

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1	Q	On page 18, you include a diagram from Nakai.	04:28:45
2	It's F	igure 22A.	04:28:55
3		Do you see that?	04:28:56
4	A	Yes.	04:28:57
5	Q	Figure 22A has a series of H's and L's along	04:28:57
6	the le	eft side.	04:29:10
7		Do you see that?	04:29:11
8	A	Yes.	04:29:11
9	Q	What do those H's and L's signify?	04:29:11
10	A	They refer to logic high and logic low	04:29:15
11	voltaç	ge levels applied to the array.	04:29:18
12	Q	This Figure 22A in Nakai, is that for program	04:29:20
13	operat	zion?	04:29:26
14	А	No, it's for read operation.	04:29:27
15	Q	Claim 1 is directed to programming, is it	04:29:29
16	not?		04:29:34
17	А	Oh, that's correct. Yes.	04:29:35
18	Q	Why did and Nakai does have a programming	04:29:36
19	figure	e, doesn't it?	04:29:39
20	A	It does.	04:29:40
21	Q	Figure 23 that we just looked at; right?	04:29:41
22	А	It does, yes.	04:29:43
23	Q	Then why did you include the figure for the	04:29:44
24	read c	operation in support of your analysis of	04:29:47
25	Figure	e 1 for claim element 1a?	04:29:51

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1	A Well, claim element 1a deals specifically	04:29:54			
2	with structure, not functionality or operation				
3	that's occurring at that time, and and this				
4	figure has more things on it identified with labels	04:30:07			
5	than does the figure in 23.	04:30:13			
6	In fact, you will look 22A is used on	04:30:19			
7	18 page 18, page 19, page 20, page 21, and the	04:30:22			
8	elements of the claim that are listed there	04:30:31			
9	generally are all elements of structure, and so we	04:30:37			
10	chose this as being more more enlightening from	04:30:42			
11	a from a structure point of view. That's all.	04:30:50			
12	It has more things that are labeled, no other	04:30:52			
13	reason. 04:30:5				
14	Q But you would agree with me that Figure 22A	04:30:57			
15	from Nakai is directed to a read operation; whereas,	04:30:59			
16	Figure 23A of Nakai is directed to a program	04:31:02			
17	operation?	04:31:06			
18	A That's correct. Yes.	04:31:07			
19	Q Now, if we look at Figure 23A, which, as you	04:31:08			
20	pointed out, is reproduced on page 22.	04:31:14			
21	A Yes.	04:31:17			
22	Q And, actually, if we just compare page 21 and	04:31:17			
23	22, that has Figures 22A on page 21 and Figure 23 on	04:31:21			
24	page 22.	04:31:26			
25	Do you see that?	04:31:27			

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1	A Yes.	04:31:34		
2	Q And with regard to Figure 22, we already	04:31:34		
3	talked about the H's and L's indicating logic high	04:31:36		
4	and logic low in Nakai; right?	04:31:39		
5	A Mm-hmm. Yes.	04:31:41		
6	Q So in Figure 23A, it doesn't have H's and	04:31:41		
7	L's, does it?	04:31:44		
8	A No, it does not.	04:31:45		
9	Q So in Nakai, they knew how to use H's and L's	04:31:45		
10	for logic high and logic low, but they elected not	04:31:53		
11	to use that with regard to Figure 23A, did they?	04:31:57		
12	MR. LIMBACH: Objection; form.	04:31:59		
13	THE WITNESS: We have already talked about	04:32:00		
14	the fact that a logic high voltage can be more than	04:32:04		
15	one more than one voltage, and the claim is drawn	04:32:07		
16	to programming, and that's why we use 23A in this 04:			
17	in this page 22. 04:			
18	BY MR. HEINZ:	04:32:18		
19	Q Why, in your view, does Nakai include H's and	04:32:20		
20	L's in connection with the read operation but does	04:32:25		
21	not include H's and L's with respect to the program	04:32:29		
22	operation?	04:32:33		
23	A Because of the particular voltages Nakai	04:32:37		
24	wants to put on the program operation. That doesn't	04:32:42		
25	mean that they are not a logic high or a logic low,	04:32:47		

1	it just means they are a different absolute value.	04:32:50			
2	Q Why would the different absolute value				
3	necessitate a different symbol? Because as we	04:33:09			
4	talked about before, the concept of logic high and	04:33:14			
5	logic low is, I believe, in your view, agnostic to	04:33:16			
6	the particular number.	04:33:20			
7	A I think in in with respect to the '045,	04:33:21			
8	it is, yes.	04:33:25			
9	Q But it's not with respect to Nakai?	04:33:25			
10	MR. LIMBACH: Objection; form.	04:33:28			
11	THE WITNESS: Well, we are looking for	04:33:29			
12	evidence of whether this is prior art to the '045, 0-				
13	and "this" being Nakai, and the action of the 04:				
14	voltages applied in Figure 23A are those voltages 04				
15	are required to perform the programming, and, at the 04				
16	same time, those voltages are required to elicit 04:33				
17	states of the transistors much like a logic high or 0				
18	a logic low, and that's why we identify them the	04:34:13			
19	same way.	04:34:17			
20	For example, if you look at 23A, the level	04:34:21			
21	VPPI is applied to the two-word line actually,	04:34:29			
22	multiple of the word lines there. Had had Nakai	04:34:36			
23	simply applied the Vcc power supply, it's well known	04:34:44			
24	that, in programming, this would have had problems.	04:34:49			
25	So it is it's it's a high a logic high	04:34:53			
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1	voltage level that's appropriate for the operation	04:34:59		
2	at hand.			
3	BY MR. HEINZ:	04:35:03		
4	Q You mentioned, if Nakai would have applied	04:35:03		
5	Vcc in Figure 23, it would have had problems.	04:35:06		
6	Can you please explain what what the	04:35:09		
7	problems would be?	04:35:11		
8	A Well, since you are putting since you are	04:35:11		
9	putting 20 volts on the VPP voltage, or thereabouts,	04:35:20		
10	you want to make sure that the substrate under	04:35:25		
11	the the substrate under the transistor to be	04:35:29		
12	programmed is as close to ground as possible, and	04:35:31		
13	that means that you want the one one issue is	04:35:36		
14	that you want the series resistance of all the other	04:35:41		
15	transistors in the stack to be small. So one way to	04:35:44		
16	get the series resistance to be smaller is to raise	04:35:47		
17	the voltage on it.	04:35:51		
18	The other is that it it it keeps it	04:35:51		
19	keeps next-door-neighbor issues, I think, at	04:35:59		
20	at more controlled by using the VPI voltage.	04:36:05		
21	Q So Nakai had structural structural reasons	04:36:11		
22	that you wouldn't want to use Vcc as the logic high	04:36:15		
23	during programming	04:36:19		
24	A Nakai	04:36:19		
25	Q is that	04:36:20		

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1	A Nakai structure is not any different than	04:36:20		
2	the '045 patent. It has the same sort of issues to	04:36:23		
3	deal with. The difference, mostly, is the fact that			
4	they are not the same technology.	04:36:32		
5	Q And how are they different? I'm sorry.	04:36:35		
6	A Well, they don't this is sorry. Nakai	04:36:37		
7	is is sorry. Nakai is built at Toshiba, and I	04:36:44		
8	don't know where this other part is built, but	04:37:00		
9	the as we talked about before, the voltages are	04:37:09		
10	very much dependent upon which technology you use,	04:37:12		
11	right? And so Nakai felt that and as shown in	04:37:15		
12	Figure 23, that this was the best way to run the	04:37:20		
13	part, and the numbers in not the numbers, but the	04:37:22		
14	language in the claims of the '045 patent, they	04:37:32		
15	they seem like they were able to build a a part	04:37:41		
16	that was able to use lower voltages than the Nakai	04:37:46		
17	part.	04:37:51		
18	An example of that is found in column 6 where	04:37:53		
19	it says "the voltage applied to the bit line can be	04:38:06		
20	as low as Vcc." So that means sometimes it's higher	04:38:10		
21	than Vcc, but it can be as low as Vcc.	04:38:15		
22	And it was a pretty common occurrence through	04:38:19		
23	this period where people were trying to get lower	04:38:22		
24	voltages on the parts and also to make sure they	04:38:25		
25	didn't overstress the gate oxides; otherwise, they	04:38:28		

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1	would lose performance.	04:38:32		
2	MR. HEINZ: I hate to say it, but we have to	04:38:33		
3	change our tape.	04:38:35		
4	THE VIDEOGRAPHER: Thank you.	04:38:36		
5	Going off the record, the time now is 4:38.	04:38:37		
6	6 (Recess taken.)			
7	THE VIDEOGRAPHER: Video is rolling.	04:53:00		
8	The time now is 4:53. We are back on the	04:53:17		
9	9 videotape record.			
10	Please proceed.	04:53:23		
11	MR. HEINZ: I have no further questions.	04:53:24		
12	MR. LIMBACH: Okay. I have a few.	04:53:27		
13	EXAMINATION			
14	BY MR. LIMBACH:	04:53:29		
15	Q Mr. Murphy, do you remember a discussion you	04:53:34		
16	had with counsel earlier today regarding a boosting			
17	circuit?			
18	A Yes.	04:53:44		
19	Q What is a boosting circuit?	04:53:44		
20	A A boosting circuit, effectively, is a	04:53:46		
21	DC-to-DC converter.	04:53:50		
22	Q And what does it convert?	04:53:59		
23	A It converts voltage from one level to	04:54:00		
24	another, so you will have an incoming voltage, and	04:54:04		
25	then a different voltage will be converted out of	04:54:08		

1	it.	04:54:11
2	Q Okay. So the purpose is to create a second	04:54:15
3	voltage that's different than the first?	04:54:18
4	A Correct.	04:54:20
5	Q And is it when you say "boosting voltage,"	04:54:20
6	does that mean it's a higher voltage or lower	04:54:25
7	voltage, or how does that work?	04:54:27
8	A Generally, from what I remember and my	04:54:28
9	history, boosting generally emit higher in voltage.	04:54:33
10	Another name for a type of circuit, which is also	04:54:39
11	DC-to-DC converter, is a pump circuit, and pump	04:54:42
12	circuits are pretty well known. You can pump above	04:54:46
13	or below, so depends upon which voltage which	04:54:49
14	type voltage you need.	04:54:52
15	Q Is a boosting circuit the only way to get a	04:54:54
16	second voltage on a chip?	04:54:58
17	A No.	04:55:00
18	Q Can you name another way?	04:55:05
19	A You can provide a second voltage from an	04:55:07
20	external pin. You can simply take a an incoming	04:55:10
21	voltage and use, for example, a resistive divider,	04:55:17
22	which is not a boosting or a pumping circuit, and	04:55:22
23	create a new voltage that way, so there are multiple	04:55:25
24	ways to do it.	04:55:30
25	Q Could you supply a second power supply?	04:55:31

1	A	Yeah, you could.	04:55:36	
2	Q	If you could go to your declaration on		
3	page 8, please.			
4	A	I have it.	04:55:53	
5	Q	And this is paragraph 18 is the	04:55:54	
6	constr	uction for boosted positive voltage.	04:55:58	
7		Do you see that?	04:56:00	
8	A	I do.	04:56:01	
9	Q	And the construction is a positive voltage	04:56:02	
10	higher	than the logic high voltage.	04:56:05	
11		Do you see that?	04:56:08	
12	A	I do.	04:56:08	
13	Q	Does that construction require the use of a	04:56:09	
14	boosting circuit?			
15	A	Does it require the use of no.	04:56:16	
16	Q	Can you go to the patent now, claim 1.	04:56:21	
17	A	Yes.	04:56:27	
18	Q	And if you go to the end, the last phrase	04:56:30	
19	is or last paragraph of claim 1 is "a logic high			
20	voltage is applied to unselected word lines, while a			
21	boosted positive voltage is applied to a selected			
22	word l	ine."	04:56:50	
23		Do you see that?	04:56:51	
24	A	I do.	04:56:51	
25	Q	Does that claim language require the use of a	04:56:52	

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1	boosting circuit?	04:56:55
2	A No.	04:56:56
3	MR. LIMBACH: Counsel, that's all I have.	04:57:14
4	MR. HEINZ: I have nothing further.	04:57:16
5	MR. LIMBACH: Okay. Great.	04:57:18
6	THE VIDEOGRAPHER: Going off the record, the	04:57:20
7	time now is 4:57.	04:57:23
8	(Whereupon, the deposition was	
9	concluded at 4:57 p.m.)	
10	000	
11	I declare under penalty of perjury that the	
12	foregoing is true and correct. Subscribed at	
13	, California, this day of	
14	, 2014.	
15		
16		
17	Signature of the witness	
18		
19		
20		
21		
22		
23		
24		
25		

1	CERTIFICATE OF REPORTER
2	I, RACHEL FERRIER, a Certified Shorthand
3	Reporter, hereby certify that the witness in the
4	foregoing deposition was by me duly sworn to tell the
5	truth, the whole truth, and nothing but the truth in the
6	within-entitled cause;
7	That said deposition was taken down in
8	shorthand by me, a disinterested person, at the time and
9	place therein stated, and that the testimony was
10	thereafter reduced to typewriting by computer under my
11	direction and supervision and is a true record of the
12	testimony given by the witness;
13	That before completion of the deposition,
14	review of the transcript [X] was [ ] was not requested.
15	If requested, any changes made by the deponent (and
16	provided to the reporter) during the period allowed are
17	appended hereto.
18	I further certify that I am not of counsel or
19	attorney for either or any of the parties to the said
20	deposition, nor in any way interested in the event of
21	this cause, and that I am not related to any of the
22	parties thereto.
23	DATED: June 25, 2014
24	

RACHEL FERRIER, CSR No. 6948

1	June 25, 2014
2	Robert J. Murphy
3	72 Fairview Plaza Los Gatos, California 95030
4	Pot Tashiha Corp & Intellectual Montures I IIC
5	Re: IOSHIDA COLP V INCELLECTUAL VENCULES I LLC
6	Dear Robert J. Murphy:
7	Please be advised that the original transcript of
8	above-entitled matter is available for reading and
9	signing. The original will be held at the offices of Merrill Legal Solutions, 135 Main Street, 4th
10	Floor, San Francisco, California 94105 (415) 357–4300, for thirty (30) days in accordance with Federal Rules of Civil Procedure Section 30(e). If
11	you do not sign your deposition within 30 days, it may be used as fully as though signed.
12	If you are represented by counsel in this matter
13	you may wish to ask your attorney how to proceed. If you are not represented by counsel and wish to
14	review your transcript, please contact our office for a mutually convenient appointment to review your
15	deposition.
16	Thank you for your cooperation in this matter.
17	Sincerely yours,
18	Pachal Forriar CSP 60/9
19	Racher Ferrier, CSR 0940
20	cc: Original transcript All Counsel
21	
22	
23	
24	
25	

SF-002971 – Witness: Robert J. Murphy – June 17, 2014 Toshiba Corporation v. Intellectual Ventures I LLC



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(date)

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