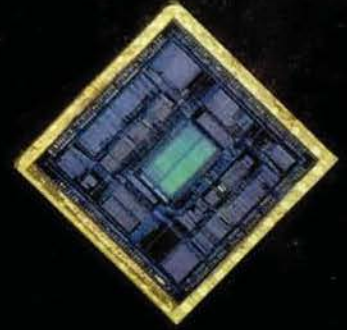


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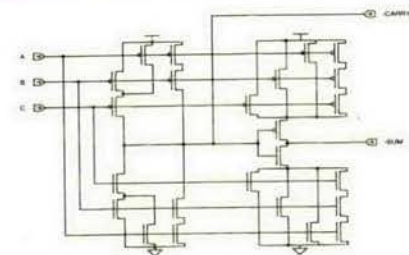
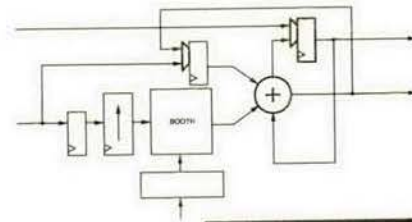
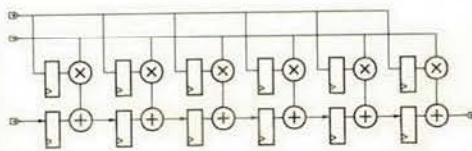
A Systems Perspective

SECOND EDITION

NEIL H. E. WESTE
KAMRAN ESHRAGHIAN



$$H(n) = \sum_{n=0}^M k_n x_n$$



IPR2014-00113

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This book is in the Addison-Wesley VLSI Systems Series.

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PRINCIPLES OF CMOS VLSI DESIGN

A Systems Perspective

Second Edition

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ADDISON-WESLEY PUBLISHING COMPANY

Reading, Massachusetts • Menlo Park, California • New York
Don Mills, Ontario • Wokingham, England • Amsterdam • Bonn
Sydney • Singapore • Tokyo • Madrid • San Juan • Milan • Paris

Sponsoring Editor: Peter S. Gordon
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Library of Congress Cataloging-in-Publication Data

Weste, Neil H. E.

Principles of CMOS VLSI design : a systems perspective / Neil Weste, Kamran Eshraghian -- 2nd ed.

p. cm.

Includes bibliographical references and index.

ISBN 0-201-53376-6

1. Integrated circuits--Very large scale integration--design and construction 2. Metal oxide semiconductors, Complementary.

I. Eshraghian, Kamran. II. Title.

TK7874.W46 1992

621.3'95--dc20

92-16564

Cover Photo: Dick Morton

Cover Art: Neil Weste

Photo Credit: Plates 5, 12, and 13, Melgar Photography, Inc., Santa Clara, CA



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7 8 9 10-MA-9695

rent, I_{ds} , and the input voltage, V_{gs} , and is defined by

$$g_m = \left. \frac{dI_{ds}}{dV_{gs}} \right|_{V_{ds} = \text{constant}} \quad (2.17)$$

It is used to measure the gain of an MOS device. In the linear region g_m is given by

$$g_{m(\text{linear})} = \beta V_{ds} \quad (2.18)$$

and in the saturation region by

$$g_{m(\text{sat})} = \beta (V_{gs} - V_t). \quad (2.19)$$

Since transconductance must have a positive value, the absolute value is used for voltages applied to p-type devices.

2.3 The Complementary CMOS Inverter—DC Characteristics

A complementary CMOS inverter is realized by the series connection of a p- and an n-device, as shown in Fig. 2.11. In order to derive the DC-transfer characteristics for the inverter (output voltage, V_{out} , as a function of the inverter, V_{in}), we start with Table 2.1, which outlines various regions of operation for the n- and p-transistors. In this table, V_{tn} is the threshold voltage of the n-channel device, and V_{tp} is the threshold voltage of the p-channel

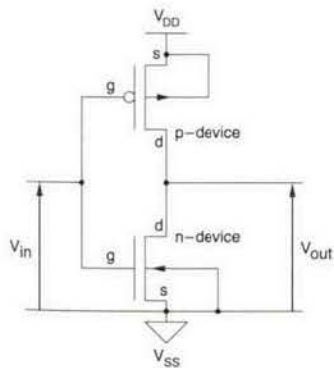


FIGURE 2.11 A CMOS inverter (with substrate connections)

TABLE 2.2 Relations Between Voltages for the Three Regions of Operation of a CMOS Inverter

	CUTOFF	NONSATURATED	SATURATED
p-device	$V_{gsp} > V_{tp}$ $V_{in} > V_{tp} + V_{DD}$	$V_{gsp} < V_{tp}$ $V_{in} < V_{tp} + V_{DD}$ $V_{dsp} > V_{gsp} - V_{tp}$ $V_{out} > V_{in} - V_{tp}$	$V_{gsp} < V_{tp}$ $V_{in} < V_{tp} + V_{DD}$ $V_{dsp} < V_{gsp} - V_{tp}$ $V_{out} < V_{in} - V_{tp}$
n-device	$V_{gsn} < V_{tn}$ $V_{in} < V_{tn}$	$V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$ $V_{dsn} < V_{gs} - V_{tn}$ $V_{out} < V_{in} - V_{tn}$	$V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$ $V_{dsn} > V_{gs} - V_{tn}$ $V_{out} > V_{in} - V_{tn}$

device. The objective is to find the variation in output voltage (V_{out}) for changes in the input voltage (V_{in}).

We begin with the graphical representation of the simple algebraic equations described by Eq. (2.5) for the two inverter transistors shown in Fig. 2.12(a).²⁰ The absolute value of the p-transistor drain current I_{ds} inverts this characteristic. This allows the VI characteristics for the p-device to be reflected about the x-axis (Fig. 2.12b). This step is followed by taking the absolute value of the p-device, V_{ds} , and superimposing the two characteristics yielding the resultant curves shown in Fig. 2.12(c). The input/output transfer curve may now be determined by the points of common V_{gs} intersection in Fig. 2.12(c). Thus, solving for $V_{inn} = V_{inp}$ and $I_{dsn} = I_{dsp}$ gives the desired transfer characteristics of a CMOS inverter as illustrated in Fig. 2.13. The switching point is typically designed to be 50 percent of the magnitude of the supply voltage: $\approx V_{DD}/2$. During transition, both transistors in the CMOS inverter are momentarily "ON," resulting in a short pulse of current drawn from the power supply. This is shown by the dotted line in Fig. 2.13.

The operation of the CMOS inverter can be divided into five regions (Fig. 2.13). The behavior of n- and p-devices in each of the regions may be found by using Table 2.2.

Region A. This region is defined by $0 \leq V_{in} \leq V_{tn}$ in which the n-device is cut off ($I_{dsn} = 0$), and the p-device is in the linear region. Since $I_{dsn} = -I_{dsp}$, the drain-to-source current I_{dsp} for the p-device is also zero. But for $V_{dsp} = V_{out} - V_{DD}$, with $V_{dsp} = 0$, the output voltage is

$$V_{out} = V_{DD} \quad (2.20)$$

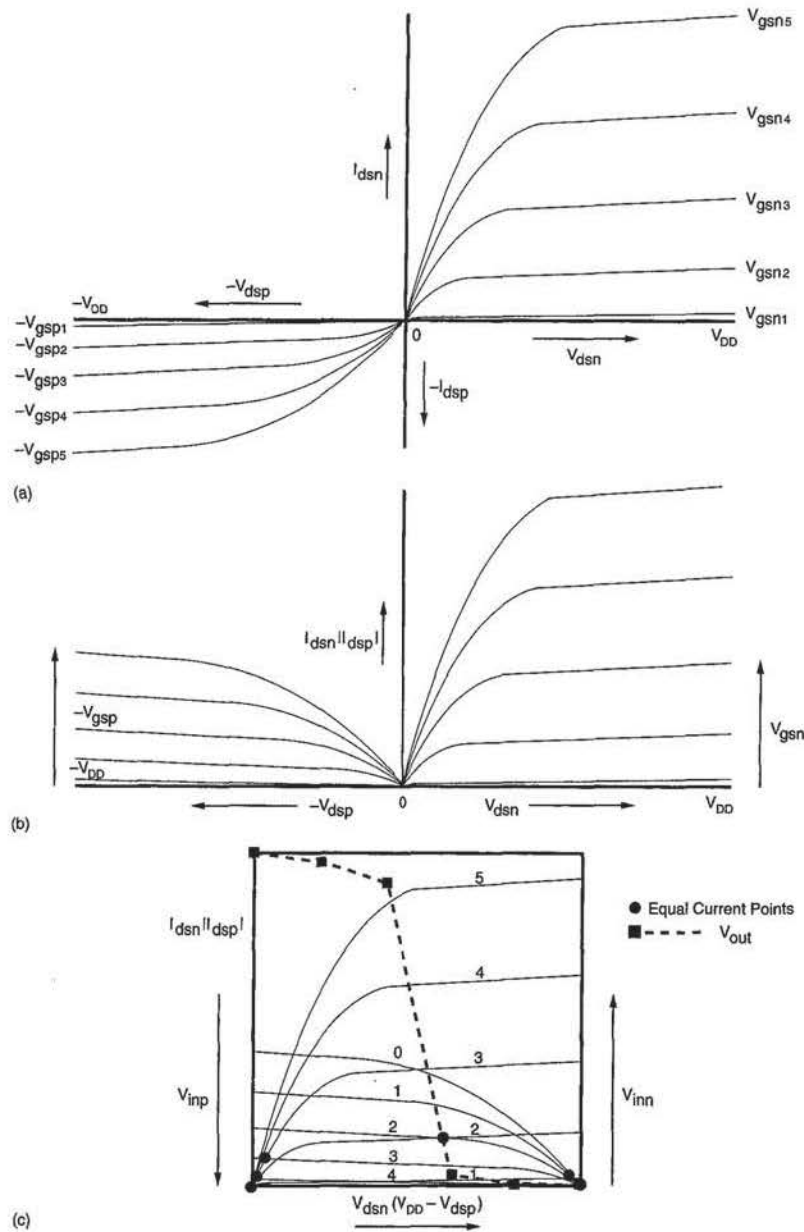


FIGURE 2.12 Graphical derivation of CMOS inverter characteristic

Region B. This region is characterized by $V_{tn} \leq V_{in} < V_{DD}/2$ in which the p-device is in its nonsaturated region ($V_{ds} \neq 0$) while the n-device is in saturation. The equivalent circuit for the inverter in this region can be represented by a resistor for the p-transistor and a current source for the n-

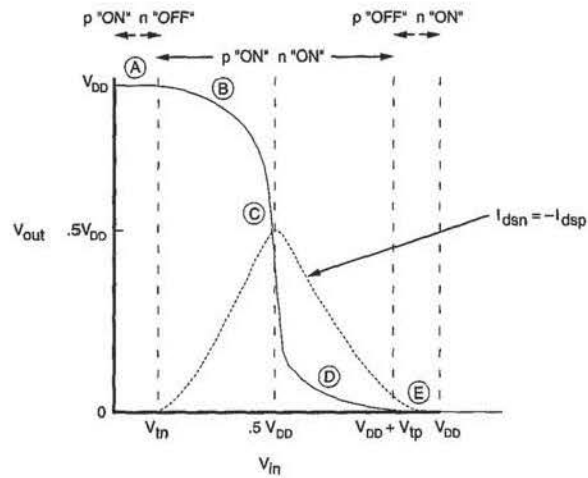


FIGURE 2.13 CMOS inverter DC transfer characteristic and operating regions

transistor as shown by Fig. 2.14(a). The saturation current I_{dsn} for the n-device is obtained by setting $V_{gs} = V_{in}$. This results in

$$I_{dsn} = \beta_n \frac{[V_{in} - V_{tn}]^2}{2} \quad (2.21)$$

where

$$\beta_n = \frac{\mu_n \epsilon}{t_{ox}} \left(\frac{W_n}{L_n} \right)$$

and

V_{tn} = threshold voltage of n-device

μ_n = mobility of electrons

W_n = channel width of n-device

L_n = channel length of n-device.

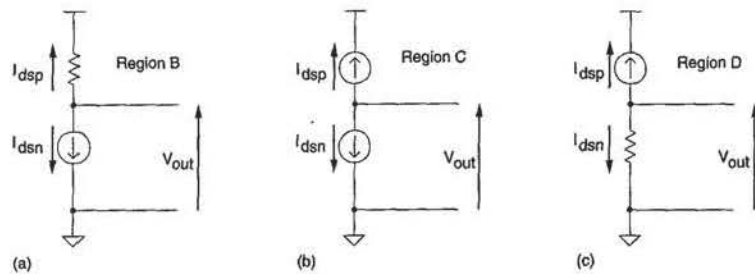


FIGURE 2.14 Equivalent circuits for operating regions of a CMOS inverter

The current for the p-device can be obtained by noting that

$$V_{gs} = (V_{in} - V_{DD})$$

and

$$V_{ds} = (V_{out} - V_{DD})$$

and therefore

$$I_{dsp} = -\beta_p \left[(V_{in} - V_{DD} - V_{tp}) (V_{out} - V_{DD}) - \frac{(V_{out} - V_{DD})^2}{2} \right], \quad (2.22)$$

where

$$\beta_p = \frac{\mu_p \epsilon}{t_{ox}} \left(\frac{W_p}{L_p} \right)$$

and

- V_{tp} = threshold voltage of p-device
- μ_p = mobility of holes
- W_p = channel width of p-device
- L_p = channel length of p-device.

Substituting

$$I_{dsp} = -I_{dsn}$$

the output voltage V_{out} can be expressed as

$$V_{out} = (V_{in} - V_{tp}) + \sqrt{(V_{in} - V_{tp})^2 - 2(V_{in} - \frac{V_{DD}}{2} - V_{tp})V_{DD} - \frac{\beta_n}{\beta_p}(V_{in} - V_{tn})^2}} \quad (2.23)$$

Region C. In this region both the n- and p-devices are in saturation. This is represented by the schematic in Fig. 2.14(b) which shows two current sources in series.

The saturation currents for the two devices are given by

$$I_{dsp} = -\frac{\beta_p}{2} (V_{in} - V_{DD} - V_{tp})^2$$

$$I_{dsn} = \frac{\beta_n}{2} (V_{in} - V_{tn})^2$$

with

$$I_{dsp} = -I_{dsn}.$$

This yields

$$V_{in} = \frac{V_{DD} + V_{tp} + V_{tn} \sqrt{\frac{\beta_n}{\beta_p}}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}. \quad (2.24)$$

By setting

$$\beta_n = \beta_p \text{ and } V_{tn} = -V_{tp},$$

we obtain

$$V_{in} = \frac{V_{DD}}{2}, \quad (2.25)$$

which implies that region *C* exists only for one value of V_{in} . The possible values of V_{out} in this region can be deduced as follows:

$$\begin{aligned} \text{n-channel: } & V_{in} - V_{out} < V_{tn} \\ & V_{out} > V_{in} - V_{tn} \\ \text{p-channel: } & V_{in} - V_{out} > V_{tp} \\ & V_{out} < V_{in} - V_{tp}. \end{aligned}$$

Combining the two inequalities results in

$$V_{in} - V_{tn} < V_{out} < V_{in} - V_{tp}. \quad (2.26)$$

This indicates that with $V_{in} = \frac{V_{DD}}{2}$, V_{out} varies within the range shown. Of course, we have assumed that an MOS device in saturation behaves like an ideal current source with drain-to-source current being independent of V_{ds} . In reality, as V_{ds} increases, I_{ds} also increases slightly; thus region *C* has a finite slope. The significant factor to be noted is that in region *C* we have two current sources in series, which is an “unstable” condition. Thus a small

input voltage has a large effect at the output. This makes the output transition very steep, which contrasts with the equivalent nMOS inverter characteristic. (See Section 2.4.) The relation defined by Eq. (2.24) is particularly useful since it provides the basis for defining the gate threshold V_{in} , which corresponds to the state where $V_{out} = V_{in}$. This region also defines the “gain” of the CMOS inverter when used as a small signal amplifier.

Region D. This region is described by $V_{DD}/2 < V_{in} \leq V_{DD} + V_{tp}$. The p-device is in saturation while the n-device is operating in its nonsaturated region. This condition is represented by the equivalent circuit shown in Fig. 2.14(c). The two currents may be written as

$$I_{dsp} = -\frac{1}{2}\beta_p (V_{in} - V_{DD} - V_{tp})^2$$

and

$$I_{dsn} = \beta_n \left[(V_{in} - V_{tn}) V_{out} - \frac{V_{out}^2}{2} \right]$$

with

$$I_{dsp} = -I_{dsn}.$$

The output voltage becomes

$$V_{out} = (V_{in} - V_{tn}) - \sqrt{(V_{in} - V_{tn})^2 - \frac{\beta_p}{\beta_n} (V_{in} - V_{DD} - V_{tp})^2} \quad (2.27)$$

Region E. This region is defined by the input condition $V_{in} \geq V_{DD} - V_{tp}$, in which the p-device is cut off ($I_{dsp} = 0$), and the n-device is in the linear mode. Here, $V_{gsp} = V_{in} - V_{DD}$, which is more positive than V_{tp} . The output in this region is

$$V_{out} = 0. \quad (2.28)$$

From the transfer curve of Fig. 2.13, it may be seen that the transition between the two states is very steep. This characteristic is very desirable because the noise immunity is maximized. This is covered in more detail in Section 2.3.2. For convenience, the characteristics associated with the five regions are summarized in Table 2.3.

TABLE 2.3 Summary of CMOS Inverter Operation

REGION	CONDITION	p-device	n-device	OUTPUT
A	$0 \leq V_{in} < V_{in}$	nonsaturated	cutoff	$V_{out} = V_{DD}$
B	$V_{in} \leq V_{in} < \frac{V_{DD}}{2}$	nonsaturated	saturated	Eq. (2.23)
C	$V_{in} = \frac{V_{DD}}{2}$	saturated	saturated	$V_{out} \neq f(V_{in})$
D	$\frac{V_{DD}}{2} < V_{in} \leq V_{DD} - V_{tp} $	saturated	nonsaturated	Eq. (2.27)
E	$V_{in} > V_{DD} - V_{tp} $	cutoff	nonsaturated	$V_{out} = V_{SS}$

2.3.1 β_n/β_p Ratio

In order to explore the variations of the transfer characteristic as a function of β_n/β_p , the transfer curve for several values of β_n/β_p are plotted in Fig. 2.15(a). Here, we note the gate-threshold voltage, V_{inv} , where $V_{in} = V_{out}$ is

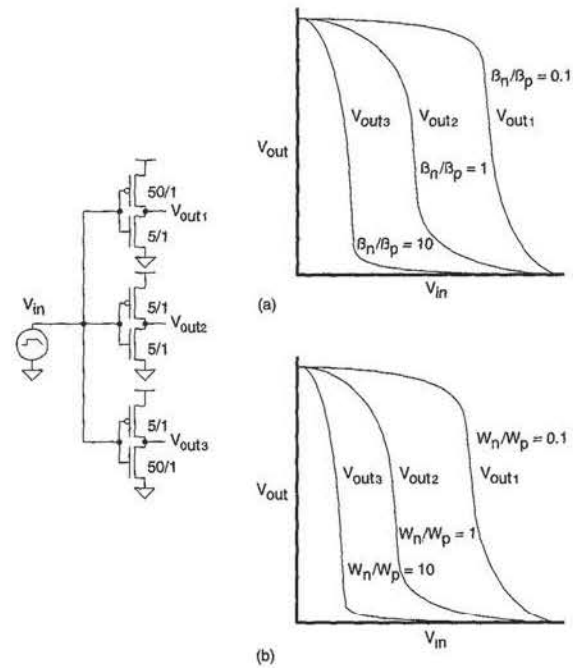


FIGURE 2.15 Influence of $\frac{\beta_n}{\beta_p}$ on inverter DC transfer characteristic

dependent on β_n/β_p . Thus, for a given process, if we want to change β_n/β_p , we need to change the channel dimensions, i.e., channel-length L and channel-width W . From Fig. 2.15(a) it can be seen that as the ratio β_n/β_p is decreased, the transition region shifts from left to right; however, the output voltage transition remains sharp (compare to the inverter responses in Figures 2.19, 2.21, 2.23, and 2.24). For the CMOS inverter a ratio of

$$\frac{\beta_n}{\beta_p} = 1 \quad (2.29)$$

may be desirable since it allows a capacitive load to charge and discharge in equal times by providing equal current-source and -sink capabilities. This will be discussed further in Chapter 4. For interest, the inverter transfer curve is also plotted (Figure 2.15b) for W_n/W_p (the width of the n- and p-transistors). This shows a relative shift to the left compared with the β ratioed case because the p-device has inherently lower gain.

Temperature also has an effect on the transfer characteristic of an inverter.²¹ As the temperature of an MOS device is increased, the effective carrier mobility, μ , decreases. This results in a decrease in β , which is related to temperature T by

$$\beta \propto T^{-1.5} \quad (2.30)$$

Therefore

$$I_{ds} \propto T^{-1.5} \quad (2.31)$$

Since the voltage transfer characteristics depend on the ratio β_n/β_p , and the mobility of both holes and electrons are similarly affected, this ratio is independent of temperature to a good approximation. Both V_{tn} and V_{tp} decrease slightly as temperature increases, and the extent of region A is reduced while the extent of region E increases. Thus the overall transfer characteristics of Fig. 2.15 shift to the left as temperature increases. Based on the figures given earlier, if the temperature rises by 50°C, the thresholds drop by 200mV each. This would cause a .2 V shift in the input threshold of the inverter (although due to the idealized model, less shift is seen in practice).

2.3.2 Noise Margin

Noise margin is a parameter closely related to the input-output voltage characteristics. This parameter allows us to determine the allowable noise voltage on the input of a gate so that the output will not be affected. The

specification most commonly used to specify noise margin (or noise immunity) is in terms of two parameters—the *LOW* noise margin, NM_L , and the *HIGH* noise margin, NM_H . With reference to Fig. 2.16, NM_L is defined as the difference in magnitude between the maximum *LOW* output voltage of the driving gate and the maximum input *LOW* voltage recognized by the driven gate. Thus

$$NM_L = |V_{ILmax} - V_{OLmax}|. \quad (2.32)$$

The value of NM_H is the difference in magnitude between the minimum *HIGH* output voltage of the driving gate and the minimum input *HIGH* voltage recognized by the receiving gate. Thus

$$NM_H = |V_{OHmin} - V_{IHmin}|, \quad (2.33)$$

where

- V_{IHmin} = minimum *HIGH* input voltage
- V_{ILmax} = maximum *LOW* input voltage
- V_{OHmin} = minimum *HIGH* output voltage
- V_{OLmax} = maximum *LOW* output voltage.

These definitions are illustrated in Fig. 2.16.

Generally, it is desirable to have $V_{IH} = V_{IL}$ and for this to be a value that is midway in the “logic swing,” V_{OL} to V_{OH} . This implies that the transfer characteristic should switch abruptly; that is, there should be high gain in the

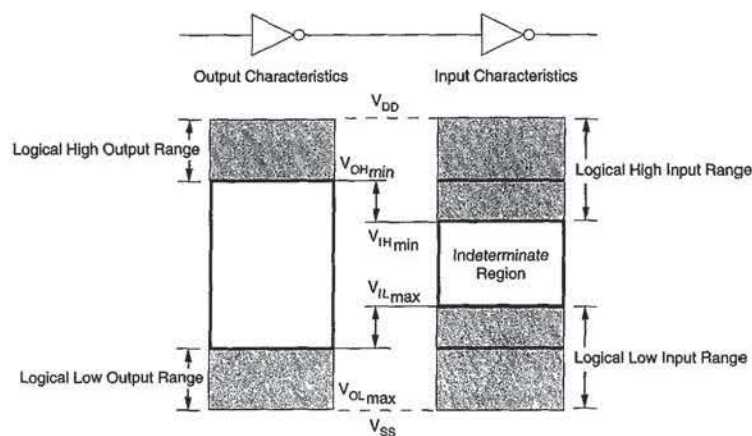


FIGURE 2.16 Noise margin definitions

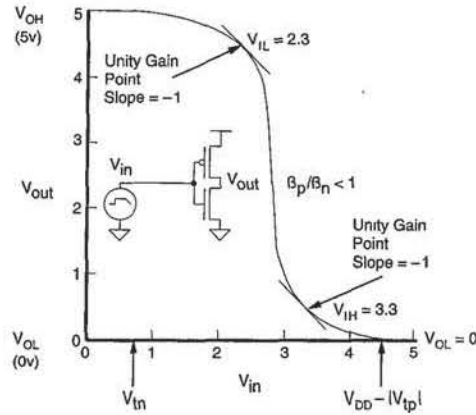


FIGURE 2.17 CMOS inverter noise margins

transition region. For the purpose of calculating noise margins, the transfer characteristic of a typical inverter and the definition of voltage levels V_{IL} , V_{OL} , V_{IH} , V_{OH} are shown in Fig. 2.17. To determine V_{IL} , we note that the inverter is in region B of operation, where the p-device is in its linear region while the n-device is in saturation. The V_{IL} is found by determining the unity gain point in the inverter transfer characteristic where the output transitions from V_{OH} . Similarly, V_{IH} is found by using the unity gain point at the V_{OL} end of the characteristic. For the inverter shown the NM_L is 2.3 volts while the NM_H is 1.7 volts.²²

Note that if either NM_L or NM_H for a gate are reduced ($\approx 0.1 V_{DD}$), then the gate may be susceptible to switching noise that may be present on the inputs. Apart from considering a single gate, one must consider the net effect of noise sources and noise margins on cascaded gates in assessing the overall noise immunity of a particular system. This is the reason to keep track of noise margins. Quite often noise margins are compromised to improve speed. Circuit examples later in this book will illustrate this trade-off.

2.3.3 The CMOS Inverter As an Amplifier

It should be noted that the CMOS inverter when used as a logic element is in reality an analog amplifier operated under saturating conditions. In region C in Fig. 2.14, the CMOS inverter acts as an inverting linear amplifier with a characteristic of

$$V_{out} = -AV_{in} \quad (2.34)$$

where A is the stage gain.

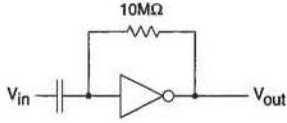


FIGURE 2.18 The CMOS inverter as an amplifier

This region may be further examined with a circuit simulator by using the circuit shown in Fig. 2.18, with a high-value resistor between input and output ($10\text{M}\Omega$). The input is DC isolated using a capacitor. The gain of this amplifier is estimated by using the small-signal model of the amplifier shown in Fig. 2.10. This circuit is valid for small signals around the linear operating point of the amplifier. The gain is approximately given by

$$\begin{aligned} A &= g_{m\text{total}} R_{d\text{effective}} \\ &= (g_{mn} + g_{mp})(r_{dsn} \parallel r_{dsp}) \\ &= g_m r_{ds} \text{ (if } g_{mn} = g_{mp} \text{ and } r_{dsn} = r_{dsp}) \end{aligned} \quad (2.35)$$

This gain is very dependent on the process and transistors used in the circuit but can be in the range from 100 to over 1000. The gain is enhanced by lengthening the transistors to improve the r_{ds} values. This improvement comes at the expense of speed and bandwidth of the amplifier.

2.4 Static Load MOS Inverters

Apart from the CMOS inverter, there are many other forms of MOS inverter that may be used to build logic gates. Figure 2.19(a) shows a generic nMOS inverter that uses either a resistive load or a constant current source. For the resistor case, if we superimpose the resistor-load line on the VI characteristics of the pull-down transistor (Fig. 2.19b), we can see that at a V_{gs} of 5 volts, the output is some small V_{ds} (V_{OL}) (Fig. 2.19c). When $V_{gs} = 0$ volts, V_{ds} rises to 5 volts. As the resistor is made larger, the V_{OL} decreases and the current flowing when the inverter is turned on decreases. Correspondingly, as the load resistor is decreased in value, the V_{OL} rises and the on current rises. Selection of the resistor value would seek a compromise between V_{OL} , the current drawn and the pull-up speed, which vary with the value of the load resistor.

The resistor- and current-source-load inverters shown in Fig. 2.19 are normally implemented using transistors in CMOS processes. In some memory processes, resistors are implemented using highly resistive undoped polysilicon. When transistors are used the inverter is called a saturated load inverter if the load transistor is operated in saturation as a constant current source. If the load transistor is biased for use as a resistor, then it is called an unsaturated load inverter.

In this section we will examine a number of static load inverters that one can implement in CMOS processes. Usually the reason for doing this is to reduce the number of transistors used for a gate to improve density and/or to lower dynamic power consumption.