## Paper 5.10

## A 5V-Only 256k Bit CMOS Flash EEPROM

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THIS PAPER DESCRIBES A Flash EEPROM device which requires only 5V for program, erase, and read operations and has performance and cost comparable to that of the recently-reported dualpower-supply flash EEPROMs which require 12V for programming and erase, and 5V for read<sup>1</sup>. Figure 1 shows the cross section of the 256k bit flash EEPROM memory cell, which consists of a floating-gate transistor and a merged-pass-gate transistor. The process is array-contactless EEPROM (ACEE), with buried source/ drain for the bit lines with a tunnel oxide module and a 20V CMOS module.

The program and erase operations employ the Fowler-Nordheim current tunnelled through 100Å oxide, when the proper electrical voltages are applied to the selected bit (Fig. 2). To program bit 21, a pulse of 18V amplitude and 10ms duration is applied to word line 2 (WL2) with source S1 tied to ground and drain D1 floating. During the same timeframe, to prevent bit 2 from programming, source S2 is tied to 7V with drain D2 floating, so that the total voltage across the tunnel region is not adequate to start the tunnelling current. During programming of bit 21, bit 12 is stressed and could be de-programmed because source S2 is at 7V. This stress is avoided by applying a pulse of 7V to the de-selected WL1. Consequently, the de-selected bit 11 cannot program because the voltage across the tunnel region (7V) is inadequate to start the tunnelling current.

All operating voltages, +18V for program, +7V for program inhibit, -11V for erase, are internally generated from the 5V supply through charge-pump circuits. The bulk erase operation is performed by applying a negative high-voltage pulse to all the word lines and 5V to all the bit lines at the same time. The negative pulse is generated with a cascade of 4 P-channel-only voltage multiplier stages. Figure 3 shows the multiplier stage circuit and the 4 non-overlapping phases required for operation. When the 4 phases become active, node B discharges to node A through T4 and node C discharges to node B through T6, so that a negative voltage is established at node C. T3 and T5 enhance the conduction performance of T4 and T6 and the multiplication efficiency of the stage. Figure 4 shows the negative pulse waveform.

Figure 5 shows the electrical schematic of the level shifter driving the word line to +18V (program) or to -11V (erase) or to +3V (read selected word line) or to 0V (de-selected word line). The P-channel transistor P1 prevents the negative voltage from being clamped by the drain junction of transistor N1 and the Pchannel transistor P2 permits driving all the word lines to -11Vduring erase and isolating one word line from the rest during programming. Figure 6 shows the measured access time. Memory alteration is not possible if the program or the erase mode is not accessed through a specified sequence of 3 commands for programming and 6 commands for erase. Both sequences are loaded in an internal register. Only after the proper sequence of commands has been detected by the device are the programming and erase operations enabled. These sequences and command timings can be easily generated by software in a microprocessor. Protection against inadvertent alterations during power-up or power-down is also provided. Figure 7 shows the typical VTH distribution of the 256k bits after erase and programming. Figure 8 shows the endurance of the cell. Figure 9 is the chip micrograph and Table 1 summarizes the device and technology parameters.

## Acknowledgement

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<sup>1</sup>Kynette, V.N., et. al., "An In-System Reprogrammable 256K CMOS Flash Memory", ISSCC DIGEST of TECHNICAL PAPERS, p.132-133; Feb. 1988.

ACEE - CMOS; ILO = 350A; TOX = 100A
FOWLER-NORDHEIM TUNNELING
FOWLER-NORDHEIM TUNNELING
1.5 UM
40 UM2
46 KMILS2
32KX8
170 NS
150 US/BYTE EQUIVALENT ( PAGE MODE )
10MS

TABLE 1 - Device characteristics



FIGURE 1 - Cross sectional diagram of 5V memory cell

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## CELL "21" OPERATING CONDITIONS **S1**

D1

FLOAT

FLOAT

22

5V

7V

0

D2

FLOAT

FLOAT

 $1\vee$ 

WL2

-11V

18V

ERASE PROGRAM

READ

WL1

-11V

7V

0

OV з 0 1V FIGURE 2 - 5V cell operating conditions

5V











FIGURE 5 - Word line driving circuit



FIGURE 6 - Access time





NEWLY FRILING BYTES



FIGURE 9 - Chip micrograph