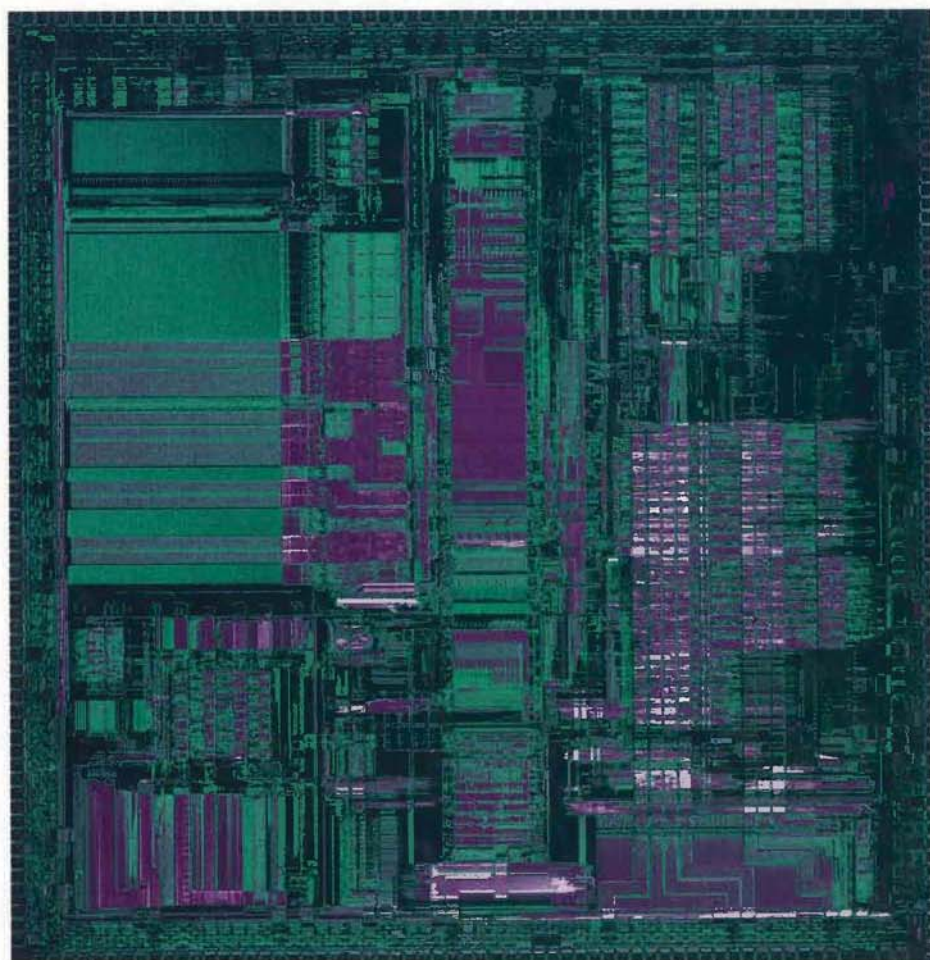

CMOS DIGITAL INTEGRATED CIRCUITS ANALYSIS AND DESIGN



Sung-Mo Kang • Yusuf Leblebici

IPR2014-00113
Toshiba Corporation v.
Intellectual Ventures I LLC
IV 2012

CMOS Digital Integrated Circuits: Analysis and Design

Sung-Mo (Steve) Kang
University of Illinois at Urbana-Champaign

Yusuf Leblebici
Istanbul Technical University

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*To Myoung-A, Jennifer and Jeffrey,
and Anil and Ebru*

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This book is printed on acid-free paper.

2 3 4 5 6 7 8 9 0 DOC DOC 9 0 9 8 7 6

ISBN 0-07-038046-5

The editor was Lynn Cox;
the production supervisor was Denise L. Puryear.
The cover was designed by Amy Becker / Designs & Visions.
R. R. Donnelley & Sons Company was printer and binder.

Library of Congress Cataloging-in-Publication Data

Kang, Sung-Mo, (date).

CMOS digital integrated circuits: analysis and design / Sung-Mo

(Steve) Kang, Yusuf Leblebici.

p. cm.

ISBN 0-07-038046-5

1. Metal oxide semiconductors, Complementary.

2. Digital integrated circuits. I. Leblebici, Yusuf. II. Title.

TK7871. 99. M44K36 1996

621.39'5—dc20

95-21223

CHAPTER 5

MOS INVERTERS: STATIC CHARACTERISTICS

The inverter is the most fundamental logic gate that performs a Boolean operation on a single input variable. In this chapter, we will examine the DC (static) characteristics of various MOS inverter circuits. It will be seen later that many of the basic principles employed in the design and analysis of MOS inverters can be directly applied to more complex logic circuits, such as NAND and NOR gates, as well. The inverter design therefore forms a significant basis for digital circuit design. Consequently, the DC analysis of MOS inverters will be carried out rigorously, and in detail. While analytic techniques constitute most of the material presented in this chapter, numerical comparisons with circuit simulation using SPICE will also be emphasized, since computer-aided techniques are integral components of the analysis and design processes for digital circuits.

5.1. Introduction

The logic symbol and the truth table of the ideal inverter are shown in Fig. 5.1. In MOS inverter circuits, both the input variable A and the output variable B are represented by node voltages, referenced to the ground potential. Using *positive logic convention*, the Boolean (or logic) value of "1" can be represented by a high voltage of V_{DD} , and the Boolean (or logic) value of "0" can be represented by a low voltage of 0. The DC voltage transfer characteristic (VTC) of the ideal inverter circuit is shown in Fig. 5.2.

The voltage V_{th} is called the *inverter threshold voltage*. Note that for any input voltage between 0 and $V_{th} = V_{DD}/2$, the output voltage is equal to V_{DD} (logic "1"). The output switches from V_{DD} to 0 when the input is equal to V_{th} . For any input voltage between V_{th} and V_{DD} , the output voltage assumes a value of 0 (logic "0"). Thus, an input voltage $0 < V_{in} < V_{th}$ is interpreted by this ideal inverter as a logic "0," while an input voltage $V_{th} < V_{in} < V_{DD}$ is interpreted as a logic "1." The DC characteristics of actual inverter circuits will obviously differ in various degrees from the ideal characteristic shown in Fig. 5.2. The accurate estimation and the manipulation of the shape of VTC for various inverter types are actually important parts of the design process.

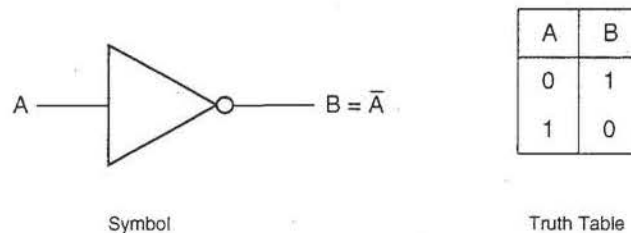


Figure 5.1. Logic symbol and truth table of the inverter.

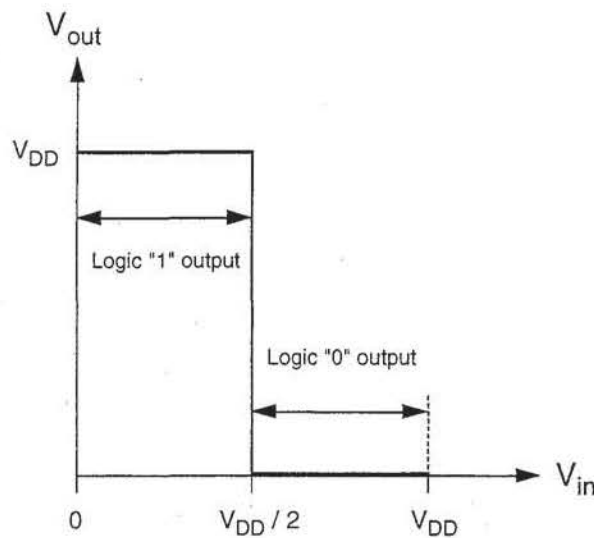


Figure 5.2. Voltage transfer characteristic (VTC) of the ideal inverter.

Figure 5.3 shows the generalized circuit structure of an nMOS inverter. The input voltage of the inverter circuit is also the gate-to-source voltage of the nMOS

transistor ($V_{in} = V_{GS}$), while the output voltage of the circuit is equal to the drain-to-source voltage ($V_{out} = V_{DS}$). The source and the substrate terminals of the nMOS transistor, also called the *driver* transistor, are connected to ground potential; hence, the source-to-substrate voltage is $V_{SB} = 0$. In this generalized representation, the *load* device is represented as a two-terminal circuit element with terminal current I_L and terminal voltage $V_L(I_L)$. One terminal of the load device is connected to the drain of the n-channel MOSFET, while the other terminal is connected to V_{DD} , the power supply voltage. We will see shortly that the characteristics of the inverter circuit actually depend very strongly upon the type and the characteristics of the load device.

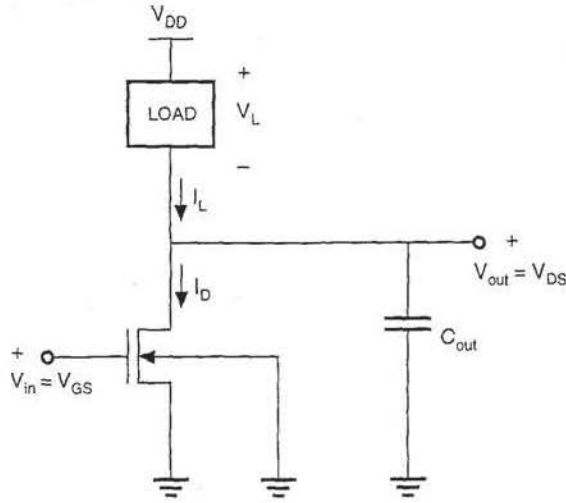


Figure 5.3. General circuit structure of an nMOS inverter.

The output terminal of the inverter shown in Fig. 5.3 is connected to the input of another MOS inverter. Consequently, the next circuit *seen* by the output node can be represented as a lumped capacitance, C_{out} . Since the DC gate current of an MOS transistor is negligible for all practical purposes, there will be no current flow into or out of the input and output terminals of the inverter in DC steady state.

Voltage Transfer Characteristic (VTC)

Applying Kirchhoff's Current Law (KCL) to this simple circuit, we see that the load current is always equal to the nMOS drain current.

$$I_D(V_{in}, V_{out}) = I_L(V_L) \quad (5.1)$$

The voltage transfer characteristic describing V_{out} as a function of V_{in} under DC conditions can then be found by analytically solving (5.1) for various input voltage values. The typical VTC of a realistic nMOS inverter is shown in Fig. 5.4. Upon examination, we can identify a number of important properties of this DC transfer characteristic.

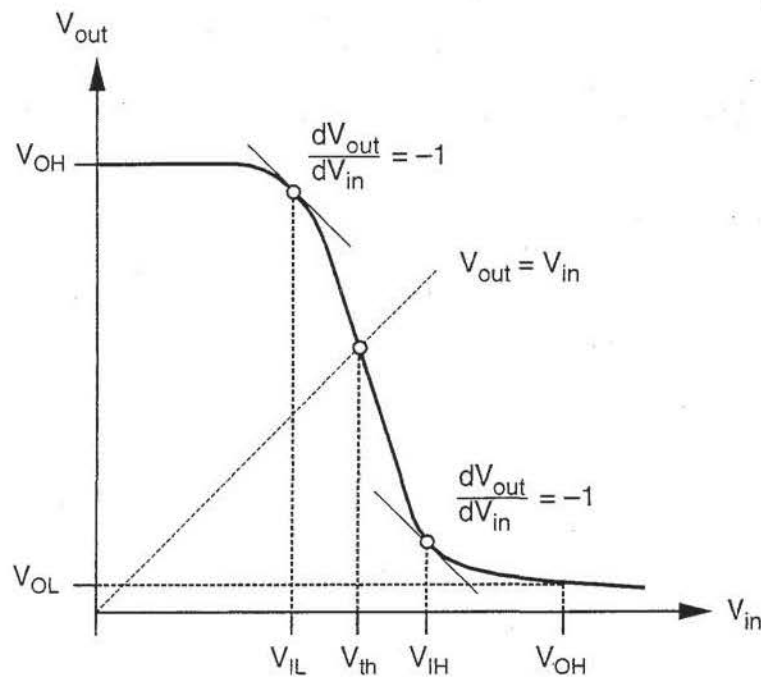


Figure 5.4. Typical voltage transfer characteristic (VTC) of a realistic nMOS inverter.

The general shape of the VTC in Fig. 5.4 is qualitatively similar to that of the ideal inverter transfer characteristic shown in Fig. 5.2. There are, however, several significant differences that deserve special attention. For very low input voltage levels, the output voltage V_{out} is equal to the high value of V_{OH} (output high voltage). In this case, the driver nMOS transistor is in cut-off, and hence, does not conduct any current. Consequently, the voltage drop across the load device is very small in magnitude, and the output voltage level is high. As the input voltage V_{in} increases, the driver transistor starts conducting a certain drain current, and the output voltage eventually starts to decrease. Notice that this drop in the output voltage level does not occur abruptly, such as the vertical drop assumed for the ideal inverter VTC, but rather gradually and with a finite slope. We identify two *critical voltage points* on this curve, where the slope

of the $V_{out}(V_{in})$ characteristic becomes equal to -1 , i.e.,

$$\frac{dV_{out}}{dV_{in}} = -1 \quad (5.2)$$

The smaller input voltage value satisfying this condition is called the *input low voltage* V_{IL} , and the larger input voltage satisfying this condition is called the *input high voltage* V_{IH} . Both of these voltages play significant roles in determining the noise margins of the inverter circuit, as we will discuss in the following sections. The physical justification for selecting these voltage points will also be examined in the context of noise immunity.

As the input voltage is further increased, the output voltage continues to drop and reaches a value of V_{OL} (*output low voltage*) when the input voltage is equal to V_{OH} . The *inverter threshold voltage* V_{th} , which is considered as the transition voltage, is defined as the point where $V_{in} = V_{out}$ on the VTC. Thus, a total of five critical voltages, V_{OL} , V_{OH} , V_{IL} , V_{IH} , and V_{th} , characterize the DC input-output voltage behavior of the inverter circuit. The functional definitions for the first four of these critical voltages are given below.

- V_{OH} : Maximum output voltage when the output level is logic "1."
- V_{OL} : Minimum output voltage when the output level is logic "0."
- V_{IL} : Maximum input voltage which can be *interpreted* as logic "0."
- V_{IH} : Minimum input voltage which can be *interpreted* as logic "1."

These definitions obviously imply that logic levels in digital circuits are not represented by quantized voltage values, but rather by voltage ranges corresponding to these logic levels. According to the definitions above, any input voltage level between the lowest available voltage in the system (usually the ground potential) and V_{IL} is interpreted as a logic "0" input, while any input voltage level between the highest available voltage in the system (usually the power supply voltage) and V_{IH} is interpreted as a logic "1" input. Any output voltage level between the lowest available voltage in the system and V_{OL} is interpreted as a logic "0" output, while any output voltage level between the highest available voltage in the system and V_{OH} is interpreted as a logic "1" output. These voltage ranges are also shown on the inverter voltage transfer characteristic shown in Fig. 5.4.

The ability of an inverter to interpret an input signal within a voltage range as either a logic "0" or as a logic "1" allows digital circuits to operate with a certain *tolerance* to external signal perturbations. This tolerance to variations in the signal

level is especially valuable in environments in which circuit noise can significantly corrupt the signals. Here the *circuit noise* corresponds to unwanted signals that are coupled to some part of the circuit from neighboring lines (usually interconnection lines) by capacitive or inductive coupling, or from outside of the system. The result of this interference is that the signal level at one end of an interconnection line may be significantly different from the signal level at the other end.

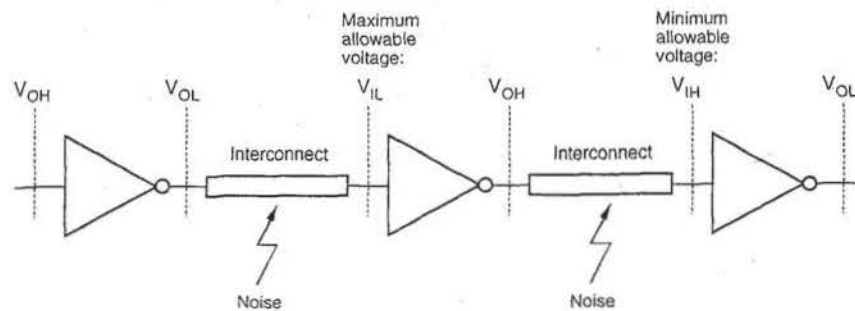


Figure 5.5. Propagation of digital signals under the influence of noise.

Noise Immunity and Noise Margins

To illustrate the effect of noise on the circuit reliability, we will consider the circuit consisting of three cascaded inverters, as shown in Fig. 5.5. Assume that all inverters are identical, and that the input voltage of the first inverter is equal to V_{OH} , i.e., a logic "1." By definition, the output voltage of the first inverter will be equal to V_{OL} , corresponding to a logic "0" level. Now, this output signal is being transmitted to the next inverter input via an interconnect, which could be a metal or polysilicon line connecting the two gates. Since on-chip interconnects are generally prone to signal noise, the output signal of the first inverter will be perturbed during transmission. Consequently, the voltage level at the input of the second inverter will be different from V_{OL} , i.e., either larger or smaller. If the input voltage of the second inverter is smaller than V_{OL} , this signal will be interpreted correctly as a logic "0" input by the second inverter. On the other hand, if the input voltage becomes larger than V_{IL} as a result of noise, then it may not be interpreted correctly by the inverter. Thus, we conclude that V_{IL} is the maximum allowable voltage at the input of the second inverter, which is low enough to ensure a logic "1" output.

Now consider the signal transmission from the output of the second inverter to the input of the third inverter, assuming that the second inverter produces an output voltage level of V_{OH} . As in the previous case, this output signal will be perturbed because of noise interference, and the voltage level at the input of the third inverter will

be different from V_{OH} . If the input voltage of the third inverter is larger than V_{OH} , this signal will be interpreted correctly as a logic "1" input by the third inverter. If the voltage level drops below V_{IH} due to noise, however, the input cannot be interpreted as a logic "1." Consequently, V_{IH} is the minimum allowable voltage at the input of the third inverter which is high enough to ensure a logic "0" output.

These observations lead us to the definition of noise tolerances for digital circuits, called *noise margins* and denoted by NM . The noise immunity of the circuit increases with NM . Two noise margins will be defined: the noise margin for low signal levels (NM_L) and the noise margin for high signal levels (NM_H).

$$NM_L = V_{IL} - V_{OL} \quad (5.3)$$

$$NM_H = V_{OH} - V_{IH} \quad (5.4)$$

Figure 5.6 shows a graphical illustration of the noise margins. Here, the shaded areas indicate the valid regions of the input and output voltages, and the noise margins are shown as the amount of variation in the signal levels that can be allowed while the signal is transmitted from the output of one gate to the input of the next gate.

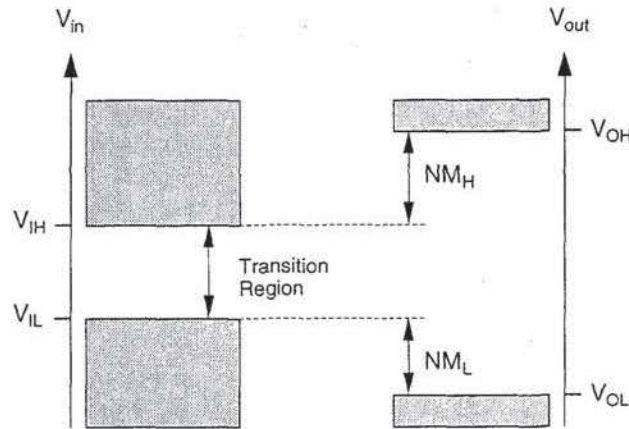


Figure 5.6. Definition of noise margins NM_L and NM_H . Note that the shaded regions indicate valid high and low levels for the input and output signals.

The selection of the two critical voltage points, V_{IL} and V_{IH} , using the slope condition (5.2) can now be justified based on noise considerations. We know that the

output voltage V_{out} of an inverter under noise-free, steady-state conditions is a nonlinear function of the input voltage, V_{in} . The shape of this function is described by the voltage transfer characteristic (VTC).

$$V_{out} = f(V_{in}) \quad (5.5)$$

If the input signal is perturbed from its nominal value because of external influences, such as noise, the output voltage will also deviate from its nominal level. Here, ΔV_{noise} represents the voltage perturbation that is assumed to affect the input voltage of the inverter.

$$V_{out}' = f(V_{in} + \Delta V_{noise}) \quad (5.6)$$

By using a simple first-order Taylor series expansion and by neglecting higher-order terms, we can express the perturbed output voltage V_{out}' as follows.

$$V_{out}' = f(V_{in}) + \frac{dV_{out}}{dV_{in}} \cdot \Delta V_{noise} + \text{higher order terms (neglected)} \quad (5.7)$$

Notice that here, $f(V_{in})$ represents the nominal (non-perturbed) output signal, and the term (dV_{out}/dV_{in}) represents the *voltage gain* of the inverter at the nominal input voltage value V_{in} . Thus, the equation (5.7) can also be expressed as:

$$\text{Perturbed Output} = \text{Nominal Output} + \text{Gain} \times \text{External Perturbation} \quad (5.8)$$

If the magnitude of the voltage gain at the nominal input voltage V_{in} is smaller than unity, then the input perturbation is not amplified and, consequently, the output perturbation remains relatively small. Otherwise, with the voltage gain larger than unity, a small perturbation in the input voltage level will cause a rather large perturbation in the output voltage. Hence, we define the boundaries of the valid input signal regions as the voltage points where the magnitude of the inverter voltage gain is equal to unity.

Finally, note that there is a voltage range between V_{IL} and V_{IH} (Fig. 5.6), corresponding to input voltage values that may not be processed correctly either as a logic "0" input or as a logic "1" input by the inverter. This region is called the *uncertain region* or, alternatively, the *transition region*. Ideally, the slope of the voltage transfer characteristic should be very large between V_{IL} and V_{IH} , because a narrow uncertain (transition) region obviously allows for larger noise margins. We will see that reducing the width of the uncertain region is one of the most important design objectives.

The preceding discussion of inverter static (DC) characteristics shows that the shape of the VTC in general and the noise immunity properties, in particular, are very significant criteria that ultimately dictate the design priorities. For any inverter circuit, the five critical voltage points V_{OL} , V_{OH} , V_{IL} , V_{IH} , and V_{th} fully determine the DC input-output voltage behavior, the noise margins, and the width and location of the transition region. Accurate estimation of these critical voltage points for different inverter designs will be an important task throughout this chapter.

Power and Area Considerations

In addition to these concerns, we can identify two other issues that play significant roles in inverter design: *power* consumption and the *chip area* occupied by the inverter circuit. About one million logic gates can be accommodated on a very-large-scale integrated (VLSI) chip using 0.5 μm MOS technology, and the circuit density is expected to increase even further in future-generation chips. Since each gate on the chip dissipates power and thus generates heat, the removal of this thermal energy, i.e., cooling of the chip, becomes an essential and usually very expensive task (note that the junction temperature is given as $T_j = T_a + \Theta P$, where T_a is the ambient temperature, Θ is the thermal resistance, and P is the amount of power dissipated). Also, most portable systems, such as cellular communication devices and laptop and palmtop computers, operate from a limited power supply, and the extension of battery-based operation time is a significant design goal. Therefore, it is very important to reduce the amount of power dissipated by the circuit in both DC and dynamic operation.

The DC power dissipation of an inverter circuit can be calculated as the product of its power supply voltage and the amount of current drawn from the power supply during steady state.

$$P_{DC} = V_{DD} \cdot I_{DC} \quad (5.9)$$

Notice that the DC current drawn by the inverter circuit may vary depending on the input and output voltage levels. Assuming that the input voltage level corresponds to logic "0" during 50% of the operation time and to logic "1" during the other 50%, the overall DC power consumption of the circuit can be estimated as follows.

$$P_{DC} = \frac{V_{DD}}{2} \cdot [I_{DC}(V_{in} = \text{low}) + I_{DC}(V_{in} = \text{high})] \quad (5.10)$$

It will be seen in the following sections that the DC power dissipation of different

inverter designs varies significantly from each other, and that these differences may become a very important factor in the selection of a particular circuit type, e.g., CMOS vs. depletion-load NMOS, for a given design task.

To reduce the chip area occupied by the inverter circuit, it is necessary to reduce the area of the MOS transistors used in the circuit. As a practical measure, we use the gate area of the MOS transistor, i.e., the product of W and L . Thus, an MOS transistor has minimum area when both of the gate (channel) dimensions are made as small as possible within the constraints of the particular technology. It follows that the ratio of the gate width to gate length (W/L) should also be as close to unity as possible, in order to achieve minimum transistor area. This requirement, however, usually contradicts other design criteria, such as the noise margins, the output current driving capability, and the dynamic switching speed. We will observe in the following sections that the design of inverter circuits involves a detailed consideration and a trade-off of these criteria.

Our examination of different MOS inverter structures will begin with the resistive-load MOS inverter. The analysis of this simple circuit will help illustrate some of the basic aspects encountered in inverter design. We will briefly examine the enhancement-load inverter, and then devote most of our attention throughout the remainder of this chapter to two very important inverter structures: the depletion-load NMOS inverter and the CMOS inverter.

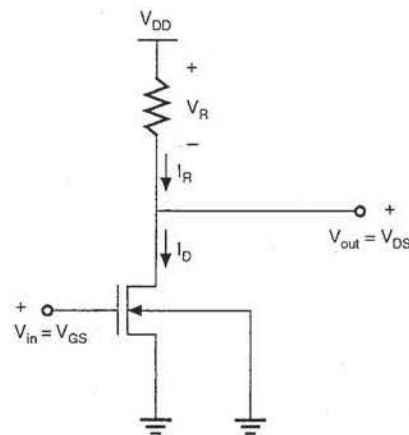


Figure 5.7. Resistive-load inverter circuit.

5.2. Resistive-Load Inverter

The basic structure of the resistive-load inverter circuit is shown in Fig. 5.7. As in the general inverter circuit already examined in Fig. 5.3, an enhancement-type nMOS

transistor acts as the driver device. The load consists of a simple linear resistor, R_L . The power supply voltage of this circuit is V_{DD} . Since the following analysis concentrates on the static behavior of the circuit, the output load capacitance is not shown in this figure.

As already noted in Section 5.1, the drain current I_D of the driver MOSFET is equal to the load current I_R in DC steady-state operation. To simplify the calculations, the channel-length modulation effect will be neglected in the following, i.e., $\lambda = 0$. Also, note that the source and the substrate terminals of the driver transistor are both connected to the ground; hence, $V_{SB} = 0$. Consequently, the threshold voltage of the driver transistor is always equal to V_{T0} . We start our analysis by identifying the various operating regions of the driver transistor under steady-state conditions.

For input voltages smaller than the threshold voltage V_{T0} , the transistor is in cut-off, and does not conduct any drain current. Since the voltage drop across the load resistor is equal to zero, the output voltage must be equal to the power supply voltage, V_{DD} . As the input voltage is increased beyond V_{T0} , the driver transistor starts conducting a nonzero drain current. Note that the driver MOSFET is initially in saturation, since its drain-to-source voltage ($V_{DS} = V_{out}$) is larger than $(V_{in} - V_{T0})$. Thus,

$$I_R = \frac{k_n}{2} \cdot (V_{in} - V_{T0})^2 \quad (5.11)$$

With increasing input voltage, the drain current of the driver also increases, and the output voltage V_{out} starts to drop. Eventually, for input voltages larger than $V_{out} + V_{T0}$, the driver transistor enters the linear operation region. At larger input voltages, the transistor remains in linear mode, as the output voltage continues to decrease.

$$I_R = \frac{k_n}{2} \cdot [2 \cdot (V_{in} - V_{T0}) \cdot V_{out} - V_{out}^2] \quad (5.12)$$

The various operating regions of the driver transistor and the corresponding input-output conditions are listed in the following table.

Input Voltage Range	Operating Mode
$V_{in} < V_{T0}$	cut-off
$V_{T0} \leq V_{in} < V_{out} + V_{T0}$	saturation
$V_{in} \geq V_{out} + V_{T0}$	linear

Figure 5.8 shows the voltage transfer characteristic of a typical resistive-load inverter circuit, indicating the operating modes of the driver transistor and the critical voltage points on the VTC. Now, we start with the calculation of the five critical voltage points, which determine the steady-state input-output behavior of the inverter.

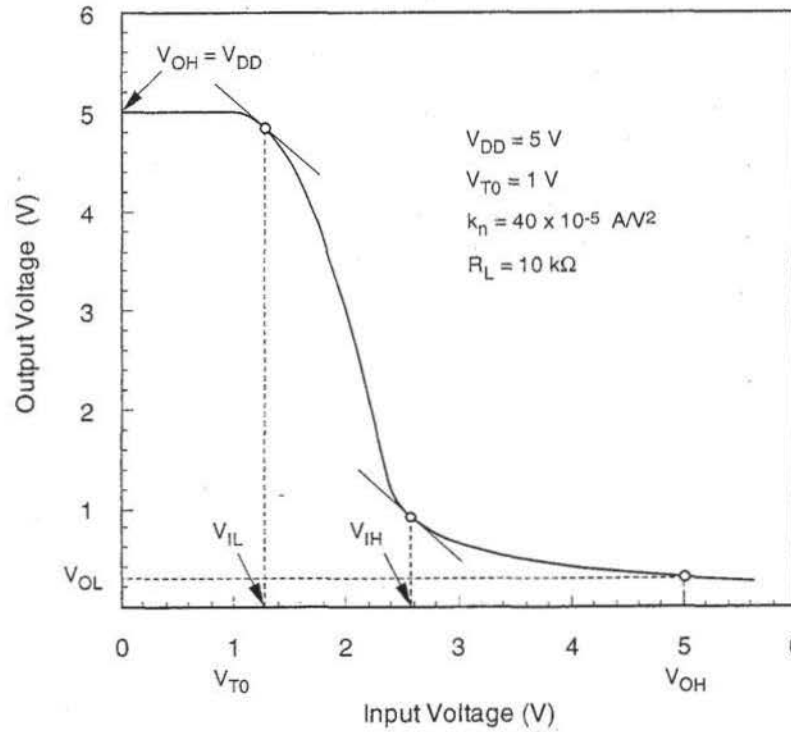


Figure 5.8. Typical VTC of a resistive-load inverter circuit. Important design parameters of the circuit are shown in the inset.

Calculation of V_{OH}

First, we note that the output voltage V_{out} is given by

$$V_{out} = V_{DD} - R_L \cdot I_R \quad (5.13)$$

When the input voltage V_{in} is low, i.e., smaller than the threshold voltage of the driver MOSFET, the driver transistor is cut-off. Since the drain current of the driver transistor is equal to the load current, $I_R = I_D = 0$. It follows that the output voltage of the inverter

under these conditions is:

$$V_{OH} = V_{DD} \quad (5.14)$$

Calculation of V_{OL}

To calculate the output low voltage V_{OL} , we assume that the input voltage is equal to V_{OH} , i.e., $V_{in} = V_{OH} = V_{DD}$. Since $V_{in} - V_{T0} > V_{out}$ in this case, the driver transistor operates in the linear region. Also note that the load current I_R is

$$I_R = \frac{V_{DD} - V_{out}}{R_L} \quad (5.15)$$

Using KCL for the output node, i.e., $I_R = I_D$, we can write the following equation.

$$\frac{V_{DD} - V_{OL}}{R_L} = \frac{k_n}{2} \cdot [2 \cdot (V_{DD} - V_{T0}) \cdot V_{OL} - V_{OL}^2] \quad (5.16)$$

This equation yields a simple quadratic in V_{OL} , which is solved to find the value of the output low voltage.

$$V_{OL}^2 - 2 \cdot \left(V_{DD} - V_{T0} + \frac{1}{k_n R_L} \right) \cdot V_{OL} + \frac{2}{k_n R_L} \cdot V_{DD} = 0 \quad (5.17)$$

Note that of the two possible solutions of (5.17), we must choose the one that is physically correct, i.e., the value of the output low voltage must be between 0 and V_{DD} . The solution of (5.17) is given below. It can be seen that the product $(k_n R_L)$ is one of the important design parameters that determine the value of V_{OL} .

$$V_{OL} = V_{DD} - V_{T0} + \frac{1}{k_n R_L} - \sqrt{\left(V_{DD} - V_{T0} + \frac{1}{k_n R_L} \right)^2 - \frac{2 V_{DD}}{k_n R_L}} \quad (5.18)$$

Calculation of V_{IL}

By definition, V_{IL} is the smaller of the two input voltage values at which the slope of the VTC becomes equal to (-1) , i.e., $dV_{out}/dV_{in} = -1$. Simple inspection of Fig. 5.8 shows that when the input is equal to V_{IL} , the output voltage (V_{out}) is only

slightly smaller than V_{OH} . Consequently, $V_{out} > V_{in} - V_{T0}$, and the driver transistor operates in saturation. We start our analysis by writing the KCL for the output node.

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2} \cdot (V_{in} - V_{T0})^2 \quad (5.19)$$

To satisfy the derivative condition, we differentiate both sides of (5.19) with respect to V_{in} , which results in the following equation.

$$-\frac{1}{R_L} \cdot \frac{dV_{out}}{dV_{in}} = k_n \cdot (V_{in} - V_{T0}) \quad (5.20)$$

Since the derivative of the output voltage with respect to the input voltage is equal to (-1) at V_{IL} , we can substitute $dV_{out} / dV_{in} = -1$ in (5.20).

$$-\frac{1}{R_L} \cdot (-1) = k_n \cdot (V_{IL} - V_{T0}) \quad (5.21)$$

Solving (5.21) for V_{IL} , we obtain

$$V_{IL} = V_{T0} + \frac{1}{k_n R_L} \quad (5.22)$$

The value of the output voltage when the input is equal to V_{IL} can also be found by substituting (5.22) into (5.19), as follows:

$$\begin{aligned} V_{out}(V_{in} = V_{IL}) &= V_{DD} - \frac{k_n R_L}{2} \cdot \left(V_{T0} + \frac{1}{k_n R_L} - V_{T0} \right)^2 \\ &= V_{DD} - \frac{1}{2 k_n R_L} \end{aligned} \quad (5.23)$$

Calculation of V_{IH}

V_{IH} is the larger of the two voltage points on VTC at which the slope is equal to (-1) . It can be seen from Fig. 5.8 that when the input voltage is equal to V_{IH} , the output voltage V_{out} is only slightly larger than the output low voltage V_{OL} . Hence, in this case,

$V_{out} < V_{in} - V_{T0}$, and the driver transistor operates in the linear region. The KCL equation for the output node is given below.

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2} \cdot [2 \cdot (V_{in} - V_{T0}) \cdot V_{out} - V_{out}^2] \quad (5.24)$$

Differentiating both sides of (5.24) with respect to V_{in} , we obtain

$$-\frac{1}{R_L} \cdot \frac{dV_{out}}{dV_{in}} = \frac{k_n}{2} \cdot \left[2 \cdot (V_{in} - V_{T0}) \cdot \frac{dV_{out}}{dV_{in}} + 2 V_{out} - 2 V_{out} \cdot \frac{dV_{out}}{dV_{in}} \right] \quad (5.25)$$

Next, we can substitute $dV_{out}/dV_{in} = -1$ into (5.25), since the slope of the VTC is equal to (-1) also at $V_{in} = V_{IH}$.

$$-\frac{1}{R_L} \cdot (-1) = k_n \cdot [(V_{IH} - V_{T0}) \cdot (-1) + 2 V_{out}] \quad (5.26)$$

Solving (5.26) for V_{IH} yields the following expression.

$$V_{IH} = V_{T0} + 2 V_{out} - \frac{1}{k_n R_L} \quad (5.27)$$

Thus, we obtain two algebraic equations, (5.24) and (5.27), for two unknowns, V_{IH} and V_{out} . To determine the unknown variables, we substitute (5.26) into the current equation given by (5.24) above.

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2} \cdot \left[2 \cdot \left(V_{T0} + 2 V_{out} - \frac{1}{k_n R_L} - V_{T0} \right) \cdot V_{out} - V_{out}^2 \right] \quad (5.28)$$

The positive solution of this second-order equation gives the output voltage V_{out} when the input is equal to V_{IH} .

$$V_{out}(V_{in} = V_{IH}) = \sqrt{\frac{2}{3} \cdot \frac{V_{DD}}{k_n R_L}} \quad (5.29)$$

Finally, V_{IH} can be found by substituting (5.29) into (5.27), as follows.

$$V_{IH} = V_{T0} + \sqrt{\frac{8}{3} \cdot \frac{V_{DD}}{k_n R_L}} - \frac{1}{k_n R_L} \quad (5.30)$$

The four critical voltage points V_{OL} , V_{OH} , V_{IL} , V_{IH} can now be used to determine the noise margins, NM_L and NM_H , of the resistive-load inverter circuit. In addition to these voltage points, which characterize the static input-output behavior, the inverter threshold voltage V_{th} may also be calculated in a straightforward manner. Note that the driver transistor operates in saturation mode at this point. Thus, the inverter threshold voltage can be found simply by substituting $V_{in} = V_{out} = V_{th}$ into (5.19), and by solving the resulting quadratic for V_{th} .

It can be seen from the preceding discussion that the term $(k_n R_L)$ plays an important role in determining the shape of the voltage transfer characteristic, and that it appears as a critical parameter in expressions for V_{OL} (5.18), V_{IL} (5.22), and V_{IH} (5.30). Assuming that parameters such as the power supply voltage V_{DD} and the driver MOSFET threshold voltage V_{T0} are dictated by system- and processing-related constraints, the term $(k_n R_L)$ remains as the only design parameter which can be adjusted by the circuit designer to achieve certain design goals.

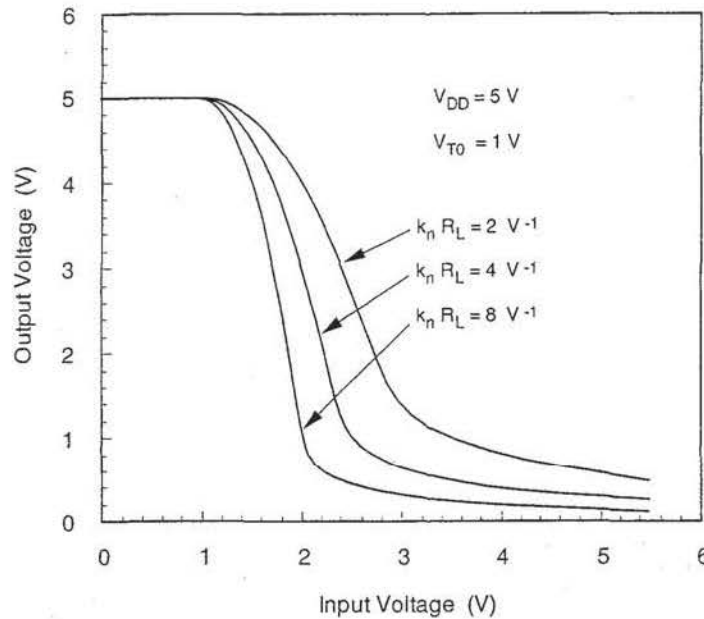


Figure 5.9. Voltage transfer characteristics of the resistive-load inverter, for different values of the parameter $(k_n R_L)$.

The output high voltage V_{OH} is determined primarily by the power supply voltage, V_{DD} . Among the other three critical voltage points, the adjustment of V_{OL} receives primary attention, while V_{IL} and V_{IH} are usually treated as secondary design variables. Figure 5.9 shows the VTC of a resistive-load inverter for different values of $(k_n R_L)$. Note that for larger $(k_n R_L)$ values, the output low voltage V_{OL} becomes smaller and that the shape of the VTC approaches that of the ideal inverter, with very large transition slope. Achieving larger $(k_n R_L)$ values in a design, however, may involve other trade-offs with the area and the power consumption of the circuit.

Power Consumption and Chip Area

The average DC power consumption of the resistive-load inverter circuit is found by considering two cases, $V_{in} = V_{OL}$ (low) and $V_{in} = V_{OH}$ (high). When the input voltage is equal to V_{OL} , the driver transistor is in cut-off. Consequently, there is no steady-state current flow in the circuit ($I_D = I_R = 0$), and the DC power dissipation is equal to zero. When the input voltage is equal to V_{OH} , on the other hand, both the driver MOSFET and the load resistor conduct a nonzero current. Since the output voltage in this case is equal to V_{OL} , the current drawn from the power supply can be found as

$$I_D = I_R = \frac{V_{DD} - V_{OL}}{R_L} \quad (5.31)$$

Assuming that the input voltage is "low" during 50% of the operation time, and "high" during the remaining 50%, the average DC power consumption of the inverter can be estimated as follows:

$$P_{DC}(\text{average}) = \frac{V_{DD}}{2} \cdot \frac{V_{DD} - V_{OL}}{R_L} \quad (5.32)$$

Example 5.1

Consider the following inverter design problem: Given $V_{DD} = 5$ V, $k_n' = 30 \mu\text{A}/\text{V}^2$, and $V_{T0} = 1$ V, design a resistive-load inverter circuit with $V_{OL} = 0.2$ V. Specifically, determine the (W/L) ratio of the driver transistor and the value of the load resistor R_L that achieve the required V_{OL} .

In order to satisfy the design specification on the output low voltage V_{OL} , we start our design by writing the relevant current equation. Note that the driver transistor is

operating in the linear region when the output voltage is equal to V_{OL} and the input voltage is equal to $V_{OH} = V_{DD}$.

$$\frac{V_{DD} - V_{OL}}{R_L} = \frac{k_n'}{2} \cdot \frac{W}{L} \cdot [2 \cdot (V_{OH} - V_{T0}) \cdot V_{OL} - V_{OL}^2]$$

Assuming $V_{OL} = 0.2$ V and using the given values for the power supply voltage, the driver threshold voltage and the driver transconductance k_n' , we obtain the following equation:

$$\frac{5 - 0.20}{R_L} = \frac{30 \times 10^{-6}}{2} \cdot \frac{W}{L} \cdot (2 \cdot 4 \cdot 0.20 - 0.20^2)$$

This equation can be rewritten as:

$$\frac{W}{L} \cdot R_L = 2.05 \times 10^5 \Omega$$

At this point, we recognize that the designer has a choice of different (W/L) and R_L values, all of which satisfy the given design specification, $V_{OL} = 0.2$ V. The selection of the pair of values to use for (W/L) and R_L in the final design ultimately depends on other considerations, such as the power consumption of the circuit and the silicon area. The table below lists some of the design possibilities, along with the average DC power consumption estimated for each design.

$\left(\frac{W}{L}\right)$ - Ratio	Load Resistor R_L [k Ω]	DC Power Consumption $P_{DC, average}$ [μ W]
1	205.0	58.5
2	102.5	117.1
3	68.4	175.4
4	51.3	233.9
5	41.0	292.7
6	34.2	350.8

It is seen that the power consumption increases significantly as the value of the load resistor R_L is decreased, and the (W/L) ratio is increased. If lowering the DC power

consumption is the overriding concern, we may choose a small (W/L) ratio and a large load resistor. On the other hand, if the fabrication of the large load resistor requires a large silicon area, a clear trade-off exists between the DC power dissipation and the area occupied by the inverter circuit.

The chip area occupied by the resistive-load inverter circuit depends on two parameters, the (W/L) ratio of the driver transistor and the value of the resistor R_L . The area of the driver transistor can be approximated by the gate area, ($W \times L$). Assuming that the gate length L is kept at its smallest possible value for the given technology, the gate area will be proportional to the (W/L) ratio of the transistor. The resistor area, on the other hand, depends very strongly on the technology which is used to fabricate the resistor on chip.

We will briefly consider two possibilities for fabricating resistors using the standard MOS process: diffused resistor and polysilicon (undoped) resistor. The diffused resistor is fabricated, as the name implies, as an isolated n-type (or p-type) diffusion region with one contact on each end. The resistance is determined by the doping density of the diffusion region and the dimensions, i.e., the length-to-width ratio, of the resistor. Practical values of the diffusion-region sheet resistance range between 20 to 100 Ω/square . Consequently, very large length-to-width ratios would be required to achieve resistor values on the order of tens to hundreds of $k\Omega$.

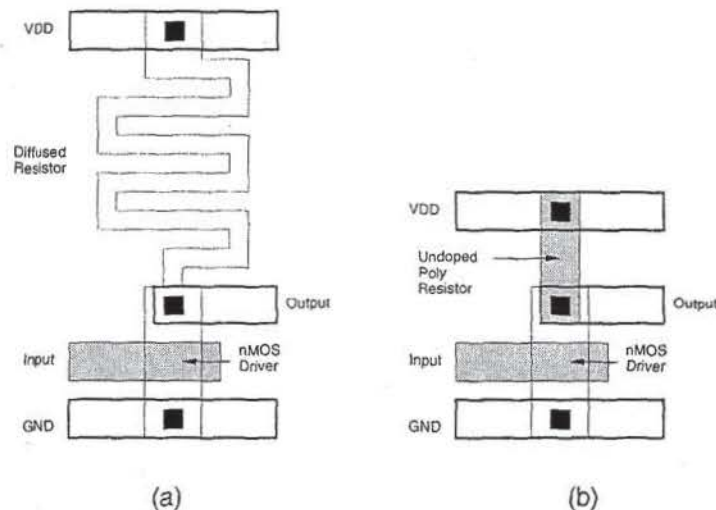


Figure 5.10. Sample layout of resistive-load inverter circuits with (a) diffused resistor and (b) undoped polysilicon resistor.

The placement of these resistor structures on chip, commonly in a serpentine shape for compactness, requires significantly more area than the driver MOSFET, as illustrated in Fig. 5.10(a). A resistive inverter with a large diffused load resistor is, therefore, not a practical component for VLSI applications.

An alternative approach to save silicon area is to fabricate the load resistor using undoped polysilicon. In conventional poly-gate MOS technology, the polysilicon structures forming the gates of transistors and the interconnect lines are heavily doped in order to reduce resistivity. The sheet resistivity of doped polysilicon interconnects and gates is about 20 to 40 Ω/square . If sections of the polysilicon are masked off from this doping step, on the other hand, the resulting *undoped* polysilicon layer has a very high sheet resistivity, in the order of 10 M Ω/square . Thus, very compact and very high-valued resistors can be fabricated using undoped poly layers (Fig. 5.10(b)). One drawback of this approach is that the resistance value can not be controlled very accurately, which results in large variations of the VTC. Consequently, resistive-load inverters with undoped poly resistors are not commonly used in logic gate circuits where certain design criteria, such as noise margins, are expected to be met. Simple inverter structures with large, undoped poly load resistors are used primarily in *low-power* Static Random Access Memory (SRAM) cells, where the primary emphasis is on the reduction of steady-state (DC) power consumption, and the operation of the memory circuit is not significantly affected by the variations of the inverter VTCs. This issue will be discussed in further detail in Chapter 10.

Example 5.2

Consider a resistive-load inverter circuit with $V_{DD} = 5 \text{ V}$, $k_n' = 20 \mu\text{A}/\text{V}^2$, $V_{T0} = 0.8 \text{ V}$, $R_L = 200 \text{ k}\Omega$, and $W/L = 2$. Calculate the critical voltages (V_{OL} , V_{OH} , V_{IL} , V_{IH}) on the VTC and find the noise margins of the circuit.

When the input voltage is low, i.e., when the driver nMOS transistor is cut-off, the output high voltage can be found as

$$V_{OH} = V_{DD} = 5 \text{ V}$$

Note that in this resistive-load inverter example, the transconductance of the driver transistor is $k_n = k_n' (W/L) = 40 \mu\text{A}/\text{V}^2$ and, hence, $(k_n R_L) = 8 \text{ V}^{-1}$.

The output low voltage V_{OL} is calculated by using (5.18):

$$\begin{aligned}
 V_{OL} &= V_{DD} - V_{T0} + \frac{1}{k_n R_L} - \sqrt{\left(V_{DD} - V_{T0} + \frac{1}{k_n R_L}\right)^2 - \frac{2V_{DD}}{k_n R_L}} \\
 &= 5 - 0.8 + \frac{1}{8} - \sqrt{\left(5 - 0.8 + \frac{1}{8}\right)^2 - \frac{2 \cdot 5}{8}} \\
 &= 0.147 \text{ V}
 \end{aligned}$$

The critical voltage V_{IL} is found using (5.22), as follows.

$$V_{IL} = V_{T0} + \frac{1}{k_n R_L} = 0.8 + \frac{1}{8} = 0.925 \text{ V}$$

Finally, the critical voltage V_{IH} can be calculated by using (5.30).

$$V_{IH} = V_{T0} + \sqrt{\frac{8}{3} \cdot \frac{V_{DD}}{k_n R_L}} - \frac{1}{k_n R_L} = 0.8 + \sqrt{\frac{8}{3} \cdot \frac{5}{8}} - \frac{1}{8} = 1.97 \text{ V}$$

Now, the noise margins can be found, according to (5.3) and (5.4).

$$NM_L = V_{IL} - V_{OL} = 0.93 - 0.15 = 0.78 \text{ V}$$

$$NM_H = V_{OH} - V_{IH} = 5.0 - 1.97 = 3.03 \text{ V}$$

At this point, we can comment on the quality of this particular inverter design for DC operation. Notice that the noise margin NM_L found here is quite low, and it may eventually lead to misinterpretation of input signal levels. For better noise immunity, the noise margin for "low" signals should be at least about 25% of the power supply voltage V_{DD} , i.e., about 1.25 V.

5.3. Inverter with Enhancement-Type MOSFET Load

The simple resistive-load inverter circuit examined in the previous section is not a suitable candidate for most digital VLSI system applications, primarily because of the large area occupied by the load resistor. In this section, we will introduce inverter circuits, which use an enhancement-type nMOS transistor as the *active load* device,

instead of the linear load resistor. The main advantage of using a MOSFET as the load device is that the silicon area occupied by the transistor is usually smaller than that occupied by a comparable resistive load. Moreover, inverter circuits with active loads can be designed to have better overall performance compared to that of passive-load inverters. In a chronological view, the development of inverters with an enhancement-type MOSFET load actually precedes other active-load inverter types, since the enhancement-type MOSFET fabrication process was perfected earlier than others.

Depending on the bias voltage applied to its gate terminal, the load transistor can be operated either in the saturation region or in the linear region. The ability to set the operation mode of the load device, regardless of the input and output voltage levels, allows us to design two different types of inverters with an enhancement MOSFET load. Both types of inverters have some distinct advantages and disadvantages from the circuit design point of view. In the following, we will consider the basic DC characteristics of the saturated enhancement load inverter circuit.

Saturated Enhancement-Load Inverter

The circuit configuration of an inverter with a saturated enhancement-type load is shown in Fig. 5.11. Note that both the driver and the load nMOS transistors are fabricated using the same process; hence, we can assume that the device parameters k_n' and V_{T0} are identical for both devices. As in the previous case, the channel-length modulation effect is being neglected for simplicity, i.e., $\lambda = 0$. The substrate terminals

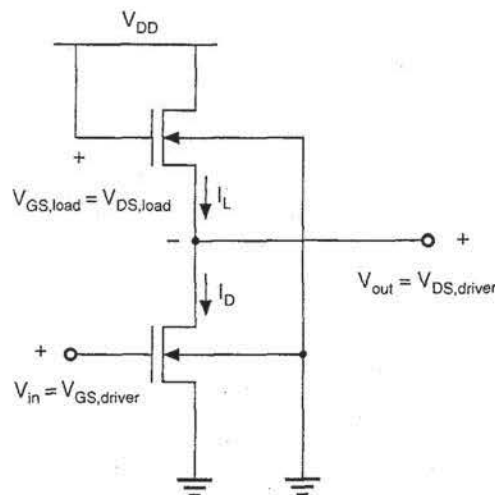


Figure 5.11. Inverter circuit with saturated enhancement-type MOSFET load.

of the driver and the load transistor are both connected to ground. Consequently, the driver transistor, with $V_{SB, driver} = 0$, will not be subject to the substrate-bias effect; thus, $V_{T, driver} = V_{T0}$. The source terminal of the load transistor, however, is at a higher potential, with $V_{SB, load} > 0$. As a result, the threshold voltage of the load device is a function of the source-to-substrate voltage, because of the substrate-bias effect.

First, consider the operating region of the load device shown in Fig. 5.11. Since both the gate and the drain terminals of the load transistor are connected to V_{DD} , we have $V_{GS, load} = V_{DS, load}$. The condition $V_{DS, load} > V_{GS, load} - V_{T, load}$ is always satisfied; hence, the load transistor operates in the saturation region as long as it is on, i.e., $V_{GS, load} > V_{T, load}$. The load current can be expressed as

$$I_{D, load} = \frac{k_n'}{2} \cdot \left(\frac{W}{L} \right)_{load} (V_{GS, load} - V_{T, load})^2 \quad (5.33)$$

For input voltages smaller than V_{T0} , the driver transistor is cut-off and does not conduct a drain current. In this case, the output (high) voltage level is determined by the load transistor. As the input voltage is increased beyond V_{T0} , the driver transistor starts conducting a nonzero drain current, initially in saturation mode. Since the driver current is equal to the load current in steady-state, i.e., $I_{D, driver} = I_{D, load}$,

$$\frac{k_n'}{2} \cdot \left(\frac{W}{L} \right)_{load} (V_{DD} - V_{out} - V_{T, load})^2 = \frac{k_n'}{2} \cdot \left(\frac{W}{L} \right)_{driver} (V_{in} - V_{T0})^2 \quad (5.34)$$

Note that the gate-to-source voltage of the load device is $V_{GS, load} = V_{DD} - V_{out}$. Also, it can be seen from Fig. 5.11 that $V_{GS, driver} = V_{in}$ and $V_{DS, driver} = V_{out}$. The output voltage level starts to decrease with increasing input voltage, and the driver transistor enters the linear operating region.

$$\begin{aligned} \frac{k_n'}{2} \cdot \left(\frac{W}{L} \right)_{load} (V_{DD} - V_{out} - V_{T, load})^2 \\ = \frac{k_n'}{2} \cdot \left(\frac{W}{L} \right)_{driver} [2 \cdot (V_{in} - V_{T0}) \cdot V_{out} - V_{out}^2] \end{aligned} \quad (5.35)$$

The current equations (5.34) and (5.35) describe the DC input-output characteristics of the saturated enhancement-load inverter circuit. In the following, we will briefly examine the critical voltage points which characterize the VTC of this inverter.

Calculation of V_{OH}

When the input voltage V_{in} is smaller than the threshold voltage V_{T0} , the driver transistor is cut-off. Since $I_{D,driver} = I_{D,load} = 0$ in this case, we can solve (5.33) to find the gate-to-source voltage of the load device as $V_{GS,load} = V_{DD} - V_{out} = V_{T,load}$. This equation yields the output high voltage as follows:

$$\begin{aligned} V_{OH} &= V_{DD} - V_{T,load}(V_{OH}) \\ &= V_{DD} - \left[V_{T0} + \gamma \left(\sqrt{|2\phi_F| + V_{OH}} - \sqrt{|2\phi_F|} \right) \right] \end{aligned} \quad (5.36)$$

Note that the threshold voltage of the load transistor $V_{T,load}$ is actually a function of the output voltage because of the substrate-bias effect. To find V_{OH} , we reorganize (5.36), and square both sides.

$$\begin{aligned} V_{OH}^2 - \left[2(V_{DD} - V_{T0} + \gamma\sqrt{|2\phi_F|}) + \gamma^2 \right] V_{OH} \\ + \left[(V_{DD} - V_{T0} + \gamma\sqrt{|2\phi_F|})^2 - \gamma^2 |2\phi_F| \right] = 0 \end{aligned} \quad (5.37)$$

The solution of this quadratic equation yields the output high voltage V_{OH} . The important result here is that the output high voltage V_{OH} cannot exceed $V_{DD} - V_{T,load}$, a limitation which significantly reduces the noise margin NM_H for high signal levels.

Calculation of V_{OL}

For calculating the output low level V_{OL} , we assume that $V_{in} = V_{OH}$. In this case, the driver transistor is operating in the linear region, and the load transistor is operating in the saturation region. Using KCL for the output node, we obtain

$$\begin{aligned} \frac{k_n'}{2} \cdot \left(\frac{W}{L} \right)_{load} [V_{DD} - V_{OL} - V_{T,load}(V_{OL})]^2 \\ = \frac{k_n'}{2} \cdot \left(\frac{W}{L} \right)_{driver} [2 \cdot (V_{OH} - V_{T0}) \cdot V_{OL} - V_{OL}^2] \end{aligned} \quad (5.38)$$

Here, the value of V_{OH} must be found from (5.37) first. Also, we note that the threshold voltage of the load transistor $V_{T,load}$ is a function of the output low voltage, as follows.

$$V_{T,load} = V_{T0} + \gamma \left(\sqrt{|2\phi_F| + V_{OL}} - \sqrt{|2\phi_F|} \right) \quad (5.39)$$

The numerical value of the output low voltage V_{OL} can be found by simultaneously solving (5.38) and (5.39). Alternatively, V_{OL} can be calculated through a simple technique based on numerical iteration, as follows. We start our calculation by assuming that V_{OL} is a small number; hence, we initially assume $V_{T,load} = V_{T0}$. Solving (5.38) with this assumption yields the first estimate for V_{OL} , which can now be substituted into (5.39) to find a better estimate for $V_{T,load}$. The threshold voltage value found in this step is in turn used to solve (5.38) again, to obtain a more accurate estimate for V_{OL} . This cycle can be repeated several times, until subsequent iterations do not cause a significant change in the V_{OL} value. Figure 5.12 illustrates the iterative procedure used to calculate V_{OL} . Since the actual numerical value of V_{OL} is relatively small, only a few iterations are usually sufficient for an accurate result.

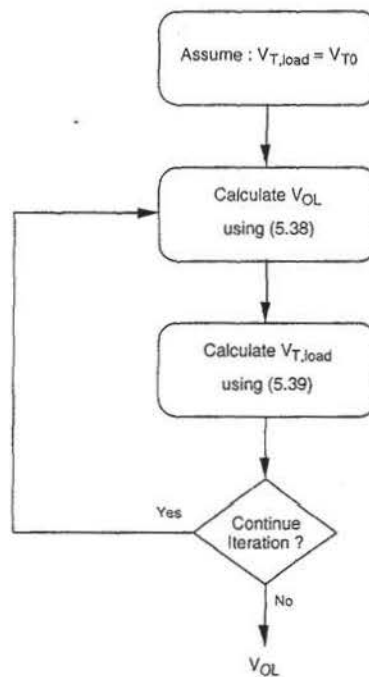


Figure 5.12. Calculation of V_{OL} through numerical iterations.

This simple iterative method can also be implemented as a short program on a computer or on a programmable calculator. The same approach will be used on several

occasions, where the iterative technique may offer a more convenient alternative to tedious analytical calculations.

Calculation of V_{IL}

At $V_{in} = V_{IL}$, we expect that the slope of the inverter VTC is equal to (-1) , i.e., $dV_{out}/dV_{in} = -1$. Since the corresponding output voltage is expected to be very close to V_{OH} , we can assume that the driver transistor is turned on, and that it is operating in the saturation region. Hence, writing KCL for the output node at steady-state yields the following current equation.

$$\frac{k_{load}}{2} \cdot (V_{DD} - V_{out} - V_{T,load})^2 = \frac{k_{driver}}{2} \cdot (V_{in} - V_{T0})^2 \quad (5.40)$$

Differentiating both sides of (5.40) with respect to V_{in} , we obtain :

$$\begin{aligned} k_{load} \cdot (V_{DD} - V_{out} - V_{T,load}) \cdot \left(-\frac{dV_{out}}{dV_{in}} - \frac{dV_{T,load}}{dV_{out}} \cdot \frac{dV_{out}}{dV_{in}} \right) \\ = k_{driver} \cdot (V_{in} - V_{T0}) \cdot \left(\frac{dV_{in}}{dV_{in}} \right) \end{aligned} \quad (5.41)$$

This equation can be rewritten as follows.

$$\frac{dV_{out}}{dV_{in}} = -\frac{k_{driver} \cdot (V_{in} - V_{T0})}{\left(1 + \frac{dV_{T,load}}{dV_{out}} \right) \cdot k_{load} \cdot (V_{DD} - V_{out} - V_{T,load})} \quad (5.42)$$

Assuming that the magnitude of $(dV_{T,load}/dV_{out})$ is negligible compared to 1, we obtain the following relationship.

$$\frac{dV_{out}}{dV_{in}} = -\frac{\sqrt{2 \cdot k_{driver} \cdot I_{D,driver}}}{\sqrt{2 \cdot k_{load} \cdot I_{D,load}}} \quad (5.43)$$

Since $I_{D,load} = I_{D,driver}$ this equation yields

$$\frac{dV_{out}}{dV_{in}} = -\sqrt{k_R} \quad (5.44)$$

with

$$k_R = \frac{k_{driver}}{k_{load}} = \frac{\left(\frac{W}{L}\right)_{driver}}{\left(\frac{W}{L}\right)_{load}} \quad \text{if } k'_{n,driver} = k'_{n,load} \quad (5.45)$$

This result implies that the *slope* of the VTC will be equal to a negative constant, determined by the transconductances of the driver and the load devices, after the driver transistor is turned on and as long as both devices are in saturation. Hence, in this case, V_{IL} is not defined as the point at which the slope of the VTC is equal to -1 as defined by Eq. (5.2). For practical purposes, the voltage V_{IL} is taken as the point at which the driver transistor starts conducting, i.e., $V_{IL} = V_{T0}$.

Calculation of V_{IH}

When the input voltage is equal to V_{IH} , the output voltage V_{out} is expected to be slightly larger than V_{OL} . Assuming that $V_{out} < V_{IH} - V_{T0}$, the driver transistor operates in the linear region, while the load transistor is still in saturation.

$$\frac{k_{load}}{2} \cdot (V_{DD} - V_{out} - V_{T,load})^2 = \frac{k_{driver}}{2} \cdot [2 \cdot (V_{in} - V_{T0}) \cdot V_{out} - V_{out}^2] \quad (5.46)$$

Here, we will define V_{IH} as the voltage point at which the slope of the VTC becomes equal to (-1) . We differentiate both sides of (5.46) with respect to V_{in} , substitute V_{IH} for the input voltage, and let $dV_{out}/dV_{in} = -1$ to obtain the following expression.

$$V_{IH} = V_{T0} - \frac{k_{load}}{k_{driver}} \cdot (V_{DD} - V_{T,load}) + \left(2 + \frac{k_{load}}{k_{driver}}\right) \cdot V_{out} \quad (5.47)$$

We can now substitute this expression into the KCL equation given by (5.46), and solve for the output voltage V_{out} .

$$V_{out} = \sqrt{\frac{k_{load}}{k_{load} + 3 \cdot k_{driver}}} \cdot (V_{DD} - V_{T,load}) \quad (5.48)$$

Note that the threshold voltage of the load device is also a function of the output voltage. Therefore, as in the case of V_{OL} , equations (5.47) and (5.48) must be solved together with equation (5.39), using numerical iterations. Since the output voltage is relatively small, a few iterations usually produce a sufficiently accurate result.

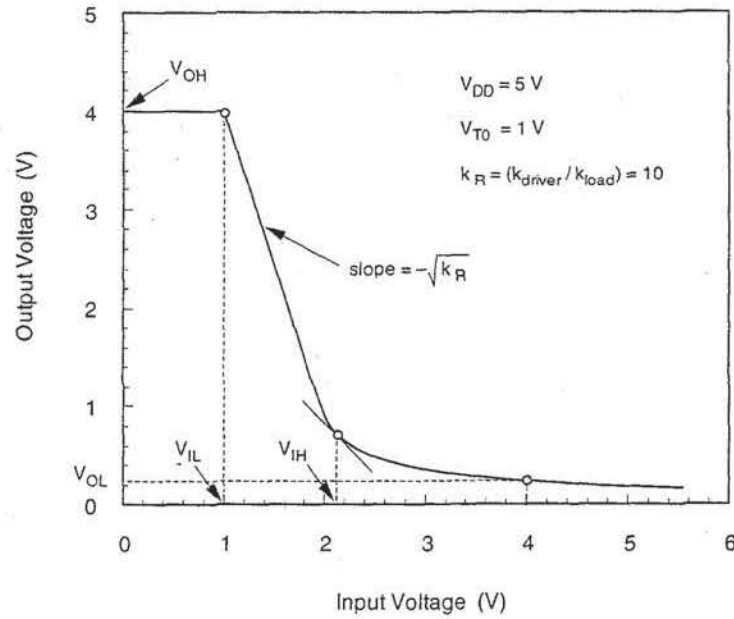


Figure 5.13. Typical VTC of a saturated enhancement-load inverter circuit.

The typical DC voltage transfer characteristic (VTC) of the saturated enhancement-load inverter circuit is shown in Fig. 5.13. Obviously, the most significant performance deficiency of this circuit is that the output high voltage V_{OH} is lower than the power supply voltage V_{DD} , i.e., $V_{OH} = V_{DD} - V_{T,load}$. Thus, the noise margin for high signal levels (NM_H) is greatly reduced for this inverter.

Linear Enhancement-Load Inverter

One possible solution to this problem is to apply the gate bias of the enhancement-type load device from another voltage source V_{GG} , so that the load device operates in the linear region instead of the saturation region. This circuit configuration, illustrated in Fig. 5.14, is called the linear enhancement-load inverter. To ensure that the load transistor operates in the linear region regardless of input and output voltage levels, we must set the gate bias voltage as $V_{GG} > V_{DD} + V_{T,load}$. Upon

examination, we can see that the output voltage reaches a high level of $V_{OH} = V_{DD}$ when the input is low, i.e., when the driver transistor is cut off. Hence, this circuit does not suffer from the limitations imposed on the noise margin NM_H by the lower V_{OH} value, as in the saturated enhancement-load inverter case. The price for this improvement is paid, however, by using two separate power supplies, V_{DD} and V_{GG} . To supply each circuit block designed in this fashion with three power connections (two for supply voltages, one ground) is a costly and complicated proposition in terms of area and routing requirements; this circuit configuration is not widely used in large-scale applications.

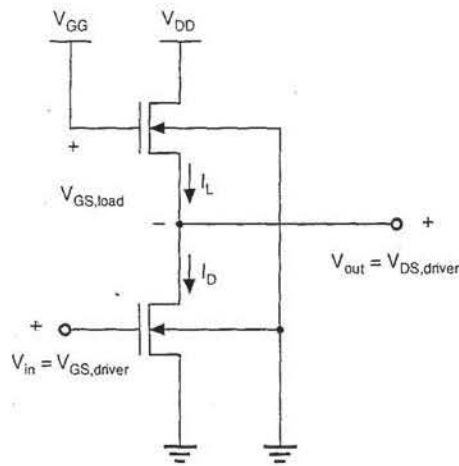


Figure 5.14. Inverter circuit with linear enhancement-type MOSFET load.

In addition, both the saturated enhancement-load inverter and the linear enhancement-load inverter circuits require a relatively large driver-to-load ratio k_R to achieve a sharp VTC transition, lower V_{OL} , and larger noise margins. A large driver-to-load ratio, on the other hand, increases the total area occupied by the inverter circuit and, hence, is not well-suited for large-scale integration.

5.4. Inverter with Depletion-Type MOSFET Load

Several of the disadvantages of the enhancement-type load inverter can be avoided by using a depletion-type nMOS transistor as the load device. Obviously, the fabrication process for producing an inverter with an enhancement-type nMOS driver and a depletion-type nMOS load is slightly more complicated and requires additional processing steps, especially for the channel implant to adjust the threshold voltage of the load device. The resulting improvement of circuit performance and integration

possibilities, however, easily justify the additional processing effort required for the fabrication of depletion-load inverters. The immediate advantages of implementing this circuit configuration are: (i) sharp VTC transition and better noise margins, (ii) single power supply, and (iii) smaller overall layout area.

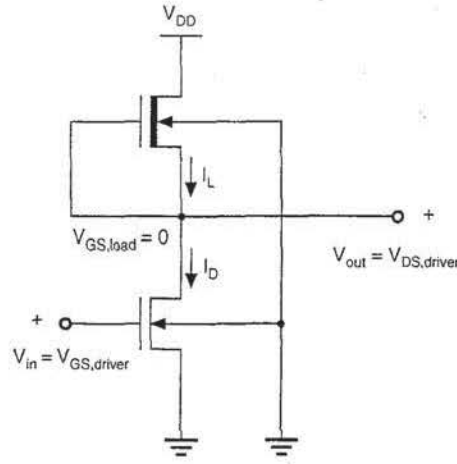


Figure 5.15. Inverter circuit with depletion-type nMOS load.

The circuit diagram of the depletion-load inverter circuit is shown in Fig. 5.15. The driver device is an enhancement-type nMOS transistor, with $V_{T0,driver} > 0$, whereas the load is a depletion-type nMOS transistor, with $V_{T0,load} < 0$. The current-voltage equations to be used for the depletion-type load transistor are identical to those of the enhancement-type device, with the exception of the negative threshold voltage (cf. Section 3.3). The gate and the source nodes of the load transistor are connected, hence, $V_{GS,load} = 0$ always. Since the threshold voltage of the depletion-type load is negative, the condition $V_{GS,load} > V_{T,load}$ is satisfied, and the load device always has a conducting channel regardless of the input and output voltage levels. Also note that both the driver transistor and the load transistor are built on the same p-type substrate, which is connected to the ground. Consequently, the load device is subject to the substrate-bias effect, so that its threshold voltage is a function of its source-to-substrate voltage, $V_{SB,load} = V_{out}$.

$$V_{T,load} = V_{T0,load} + \gamma \left(\sqrt{|2\phi_F| + V_{out}} - \sqrt{|2\phi_F|} \right) \quad (5.49)$$

The operating mode of the load transistor is determined by the output voltage level. When the output voltage is small, i.e., when $V_{out} < V_{DD} + V_{T,load}$, the load transistor

is in saturation. Note that this condition corresponds to $V_{DS,load} > V_{GS,load} - V_{T,load}$. Then, the load current is given by the following equation.

$$I_{D,load} = \frac{k_{n,load}}{2} \cdot [-V_{T,load}(V_{out})]^2 = \frac{k_{n,load}}{2} \cdot |V_{T,load}(V_{out})|^2 \quad (5.50)$$

For larger output voltage levels, i.e., for $V_{out} > V_{DD} + V_{T,load}$, the depletion-type load transistor operates in the linear region. The load current in this case is

$$I_{D,load} = \frac{k_{n,load}}{2} \cdot [2|V_{T,load}(V_{out})| \cdot (V_{DD} - V_{out}) - (V_{DD} - V_{out})^2] \quad (5.51)$$

The voltage transfer characteristic (VTC) of this inverter can be constructed by setting $I_{D,driver} = I_{D,load}$, $V_{GS,driver} = V_{in}$, and $V_{DS,driver} = V_{out}$, and by solving the corresponding current equations for $V_{out} = f(V_{in})$. Figure 5.16 shows the VTC of a typical depletion-load inverter, with $k_{n,driver}' = k_{n,load}'$.

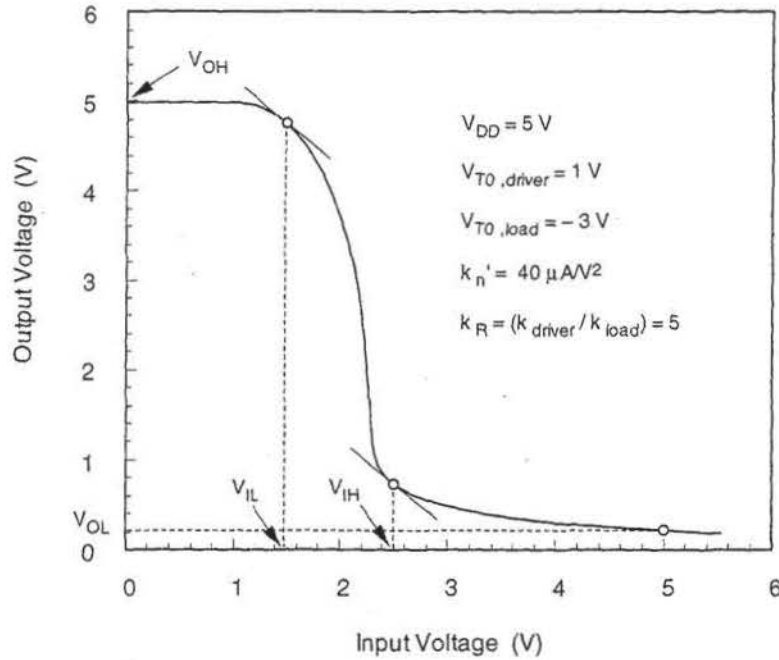


Figure 5.16. Typical VTC of a depletion-load inverter circuit.

Next, we will consider the critical voltage points V_{OH} , V_{OL} , V_{IL} , and V_{IH} for this inverter circuit. The operating regions and the voltage levels of the driver and the load transistors at these critical points are listed below.

V_{in}	V_{out}	Driver operating region	Load operating region
V_{OL}	V_{OH}	cut-off	linear
V_{IL}	$\approx V_{OH}$	saturation	linear
V_{IH}	small	linear	saturation
V_{OH}	V_{OL}	linear	saturation

Calculation of V_{OH}

When the input voltage V_{in} is smaller than the driver threshold voltage V_{T0} , the driver transistor is turned off and does not conduct any drain current. Consequently, the load device, which operates in the linear region, also has zero drain current. Substituting V_{OH} for V_{out} in (5.51), and letting the load current $I_{D,load} = 0$, we obtain

$$I_{D,load} = \frac{k_{n,load}}{2} \cdot \left[2|V_{T,load}(V_{OH})| \cdot (V_{DD} - V_{OH}) - (V_{DD} - V_{OH})^2 \right] = 0 \quad (5.52)$$

The only valid solution in the linear region is $V_{OH} = V_{DD}$.

Calculation of V_{OL}

To calculate the output low voltage V_{OL} , we assume that the input voltage V_{in} of the inverter is equal to $V_{OH} = V_{DD}$. Note that in this case, the driver transistor operates in the linear region while the depletion-type load is in saturation.

$$\frac{k_{driver}}{2} \cdot \left[2 \cdot (V_{OH} - V_{T0}) \cdot V_{OL} - V_{OL}^2 \right] = \frac{k_{load}}{2} \cdot \left[-V_{T,load}(V_{OL}) \right]^2 \quad (5.53)$$

This second-order equation in V_{OL} can be solved by temporarily neglecting the dependence of $V_{T,load}$ on V_{OL} , as follows.

$$V_{OL} = V_{OH} - V_{T0} - \sqrt{(V_{OH} - V_{T0})^2 - \left(\frac{k_{load}}{k_{driver}} \right) \cdot |V_{T,load}(V_{OL})|^2} \quad (5.54)$$

The actual value of the output low voltage can be found by solving the two equations (5.54) and (5.49) using numerical iterations, as illustrated in Fig. 5.12. The iterative method converges rapidly because the actual value of V_{OL} is relatively small.

Calculation of V_{IL}

By definition, the slope of the VTC is equal to (-1) , i.e., $dV_{out}/dV_{in} = -1$ when the input voltage is $V_{in} = V_{IL}$. Note that in this case, the driver transistor operates in saturation while the load transistor operates in the linear region. Applying KCL for the output node, we obtain the following current equation.

$$\frac{k_{driver}}{2} \cdot (V_{in} - V_{T0})^2 = \frac{k_{load}}{2} \cdot \left[2|V_{T,load}(V_{out})| \cdot (V_{DD} - V_{out}) - (V_{DD} - V_{out})^2 \right] \quad (5.55)$$

To satisfy the derivative condition at V_{IL} , we differentiate both sides of (5.55) with respect to V_{in} .

$$\begin{aligned} k_{driver} \cdot (V_{in} - V_{T0}) = \frac{k_{load}}{2} \cdot \left[2|V_{T,load}(V_{out})| \left(-\frac{dV_{out}}{dV_{in}} \right) \right. \\ \left. + 2(V_{DD} - V_{out}) \left(-\frac{dV_{T,load}}{dV_{in}} \right) - 2(V_{DD} - V_{out}) \left(-\frac{dV_{out}}{dV_{in}} \right) \right] \quad (5.56) \end{aligned}$$

In general, we can assume that the term $(dV_{T,load}/dV_{in})$ is negligible with respect to the others. Substituting V_{IL} for V_{in} , and letting $dV_{out}/dV_{in} = -1$, we obtain V_{IL} as a function of the output voltage V_{out} .

$$V_{IL} = V_{T0} + \left(\frac{k_{load}}{k_{driver}} \right) \cdot \left[V_{out} - V_{DD} + |V_{T,load}(V_{out})| \right] \quad (5.57)$$

To account for the substrate-bias effect on $V_{T,load}$, this equation must be solved together with (5.49) and (5.55) using successive iterations.

Calculation of V_{IH}

V_{IH} is the larger of the two voltage points on the VTC at which the slope is equal to (-1) . Since the output voltage corresponding to this operating point is relatively small, the driver transistor is in the linear region and the load transistor is in saturation.

$$\frac{k_{driver}}{2} \cdot [2 \cdot (V_{in} - V_{T0}) \cdot V_{out} - V_{out}^2] = \frac{k_{load}}{2} \cdot [-V_{T,load}(V_{out})]^2 \quad (5.58)$$

Differentiating both sides of (5.58) with respect to V_{in} , we obtain :

$$\begin{aligned} k_{driver} \cdot \left[V_{out} + (V_{in} - V_{T0}) \left(\frac{dV_{out}}{dV_{in}} \right) - V_{out} \left(\frac{dV_{out}}{dV_{in}} \right) \right] \\ = k_{load} \cdot [-V_{T,load}(V_{out})] \cdot \left(\frac{dV_{T,load}}{dV_{out}} \right) \cdot \left(\frac{dV_{out}}{dV_{in}} \right) \end{aligned} \quad (5.59)$$

Now, substitute $dV_{out}/dV_{in} = -1$ into (5.59), and solve for $V_{in} = V_{IH}$.

$$V_{IH} = V_{T0} + 2V_{out} + \left(\frac{k_{load}}{k_{driver}} \right) \cdot [-V_{T,load}(V_{out})] \cdot \left(\frac{dV_{T,load}}{dV_{out}} \right) \quad (5.60)$$

Note that the derivative of the load threshold voltage with respect to the output voltage cannot be neglected in this case.

$$\frac{dV_{T,load}}{dV_{out}} = \frac{\gamma}{2\sqrt{|2\phi_F| + V_{out}}} \quad (5.61)$$

The actual values of V_{IH} and the corresponding output voltage V_{out} are determined by solving (5.61) together with the current equation (5.58) and with the threshold voltage expression (5.49), using numerical iterations. A relatively accurate first-order estimate for V_{IH} can be obtained by assuming that the output voltage in this case is approximately equal to V_{OL} .

It is seen from this discussion that the critical voltage points, the general shape of the inverter VTC, and ultimately, the noise margins, are determined essentially by the threshold voltages of the driver and the load devices, and by the driver-to-load ratio (k_{driver}/k_{load}). Since the threshold voltages are usually set by the fabrication process, the driver-to-load ratio emerges as a primary design parameter which can be adjusted to achieve the desired VTC shape. Notice that with $k'_{n,driver} = k'_{n,load}$, the driver-to-load ratio is solely determined by the (W/L) ratios of the driver and the load transistors, i.e., by the device geometries. Figure 5.17 shows the VTCs of depletion-load inverter circuits with different driver-to-load ratios $k_R = (k_{driver}/k_{load})$.

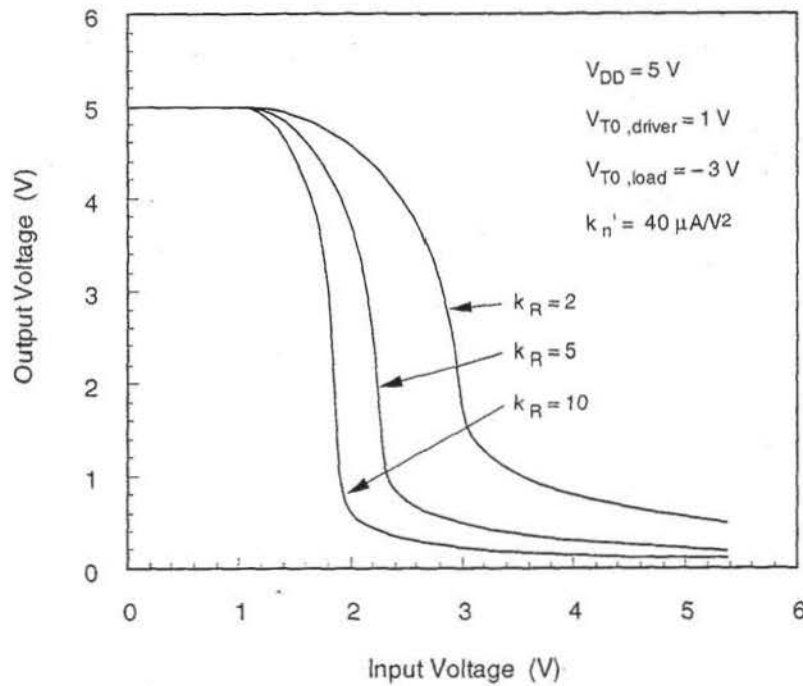


Figure 5.17. Voltage transfer characteristics of depletion-load inverters, with different driver-to-load ratios.

One important observation is that, unlike in the enhancement-load inverter case, a sharp VTC transition and larger noise margins can be obtained with relatively small driver-to-load ratios. Thus, the total area occupied by a depletion-load inverter circuit with an acceptable circuit performance is expected to be much smaller than the area occupied by a comparable resistive-load or enhancement-load inverter.

Design of Depletion-Load Inverters

Based on the VTC analysis given in the previous section, we can now consider the *design* of depletion-load inverters to satisfy certain DC performance criteria. In the broadest sense, the designable parameters in an inverter circuit are: (i) the power supply voltage V_{DD} , (ii) the threshold voltages of the driver and the load transistors, and (iii) the (W/L) ratios of the driver and the load transistors. In most practical cases, however, the power supply voltage and the device threshold voltages are dictated by other

external constraints and by the fabrication process; thus, they cannot be adjusted for every individual inverter circuit to satisfy performance requirements. This leaves the (W/L) ratio of the transistors, and more specifically, the driver-to-load ratio k_R , as the primary design parameter.

Note that the power supply voltage V_{DD} of the inverter circuit also determines the level of the output high voltage V_{OH} , since $V_{OH} = V_{DD}$. Of the remaining three critical voltages on the VTC, the output low voltage V_{OL} is usually the most significant design constraint. Designing the inverter to achieve a certain V_{OL} value will automatically set the other two critical voltages, V_{IL} and V_{IH} , as well. Equation (5.53) can be rearranged to calculate the driver-to-load ratio that achieves a target V_{OL} value, assuming that the power supply voltage and the threshold voltage values are set previously by independent design and processing constraints.

$$k_R = \frac{k_{driver}}{k_{load}} = \frac{|V_{T,load}(V_{OL})|^2}{2(V_{OH} - V_{T0})V_{OL} - V_{OL}^2} \quad (5.62)$$

Here, the driver-to-load ratio is given by

$$k_R = \frac{k'_{n,driver} \cdot \left(\frac{W}{L}\right)_{driver}}{k'_{n,load} \cdot \left(\frac{W}{L}\right)_{load}} \quad (5.63)$$

Since the channel doping densities and, consequently, the channel electron mobilities of the enhancement-type driver transistor and the depletion-type load transistor are not equal, we shall expect that $k'_{n,driver} \neq k'_{n,load}$, in general. Only if $k'_{n,driver} \approx k'_{n,load}$, can the driver-to-load ratio be reduced to

$$k_R = \frac{\left(\frac{W}{L}\right)_{driver}}{\left(\frac{W}{L}\right)_{load}} \quad (5.64)$$

Finally, note that the design procedure summarized above determines the *ratio* of the driver and the load transconductances, but not the specific (W/L) ratio of each transistor. As a result, one can propose a number of designs with different (W/L) ratios

for the driver (and for the load) device, each of which satisfies the driver-to-load ratio condition stated above. The actual sizes of the driver and the load transistors are usually determined by other design constraints, such as the current-drive capability, the steady-state power dissipation, and the transient switching speed.

Power and Area Considerations

The steady-state DC power consumption of the depletion-load inverter circuit can be easily found by calculating the amount of current being drawn from the power supply, during the input-low state and the input-high state. When the input voltage is low, i.e., when the driver transistor is cut-off and $V_{out} = V_{OH} = V_{DD}$, there is no significant current flow through the driver and the load transistors. Consequently, the inverter does not dissipate DC power under this condition. When the input is at the high state with $V_{in} \approx V_{DD}$ and $V_{out} = V_{OL}$, on the other hand, both the driver and the load transistors conduct a significant current, given by

$$\begin{aligned} I_{DC}(V_{in} = V_{DD}) &= \frac{k_{load}}{2} \cdot [-V_{T,load}(V_{OL})]^2 \\ &= \frac{k_{driver}}{2} \cdot [2 \cdot (V_{OH} - V_{T0}) \cdot V_{OL} - V_{OL}^2] \end{aligned} \quad (5.65)$$

Assuming that the input voltage level is low during 50% of the operation time and high during the other 50%, the overall average DC power consumption of this circuit can be estimated as follows.

$$P_{DC} = \frac{V_{DD}}{2} \cdot \frac{k_{load}}{2} \cdot [-V_{T,load}(V_{OL})]^2 \quad (5.66)$$

Figure 5.18(a) shows a simplified layout of the depletion-load inverter circuit. Note that the drain of the enhancement-type driver and the source of the depletion-type load transistor share a common n^+ diffusion region, which saves silicon area compared to two separate diffusion regions. The threshold voltage of the depletion-type load device is adjusted by a donor implant into the channel region. The width-to-length ratio of the driver transistor is seen to be larger than the width-to-length ratio of the load, which yields a driver-to-load ratio of about 4. Overall, this inverter circuit configuration is relatively compact, and it occupies a significantly smaller area compared to those for resistive-load or enhancement-load inverters with similar performance.

The area requirements of the depletion-load inverter circuit can be reduced even further by using a *buried contact* for connecting the gate and the source of the

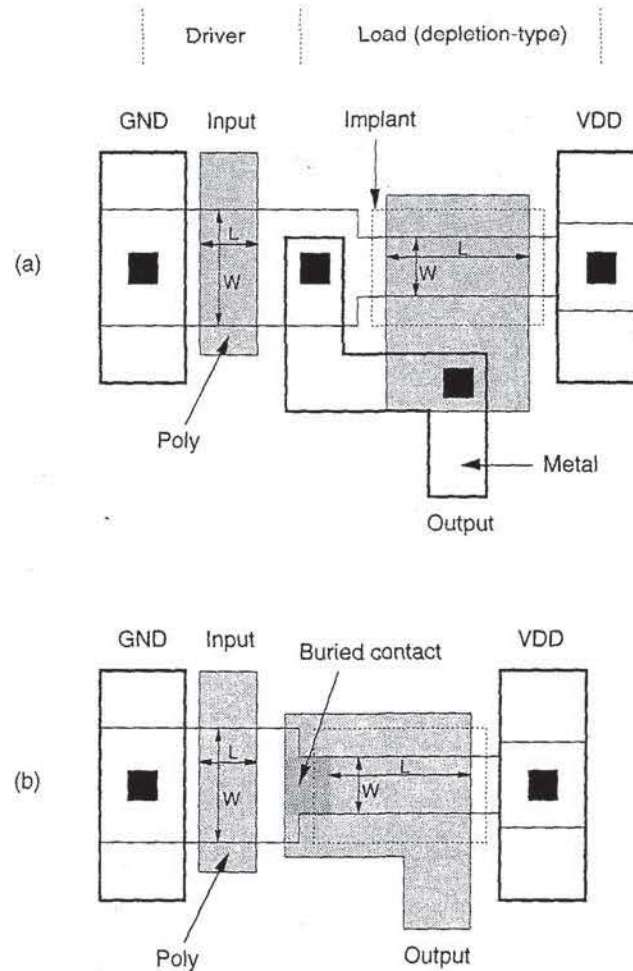
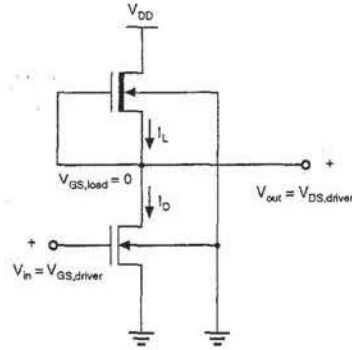


Figure 5.18. Sample layout of depletion-load inverter circuits (a) with output contact on diffusion, and (b) with buried contact.

load transistor, as shown in Figure 5.18(b). In this case, the polysilicon gate of the depletion-mode transistor makes a direct ohmic contact with the n⁺ source diffusion. The contact window on the intermediate diffusion area can be omitted, which results in a further reduction of the total area occupied by the inverter.

Example 5.3

Consider a depletion-load inverter circuit with the following parameters:



$$\begin{aligned}
 V_{DD} &= 5 \text{ V} \\
 V_{T0,driver} &= 1.0 \text{ V} \\
 V_{T0,load} &= -3.0 \text{ V} \\
 (W/L)_{driver} &= 2, (W/L)_{load} = 1/3 \\
 k_{n,driver}' &= k_{n,load}' = 25 \mu\text{A/V}^2 \\
 \gamma &= 0.4 \text{ V}^{1/2} \\
 \phi_F &= -0.3 \text{ V}
 \end{aligned}$$

Calculate the critical voltages (V_{OL} , V_{OH} , V_{IL} , V_{IH}) on the VTC and find the noise margins of the circuit.

First, the output high voltage is simply found according to (5.52) as $V_{OH} = V_{DD} = 5 \text{ V}$.

To calculate the output low voltage V_{OL} , we must solve (5.49) and (5.54) simultaneously, using numerical iterations, since the threshold voltage of the load transistor is also a function of the inverter output voltage. We start the iterations by assuming that the output voltage is equal to zero; thus, letting $V_{T,load} = V_{T0,load} = -3 \text{ V}$. Solving (5.54) with this assumption yields a first-order estimate for V_{OL} .

$$\begin{aligned}
 V_{OL} &= V_{OH} - V_{T0} - \sqrt{(V_{OH} - V_{T0})^2 - \left(\frac{k_{load}}{k_{driver}}\right) \cdot |V_{T,load}(V_{OL})|^2} \\
 &= 5 - 1 - \sqrt{(5 - 1)^2 - \left(\frac{1}{6}\right) |3|^2} = 0.192 \text{ V}
 \end{aligned}$$

Now, the threshold voltage of the depletion-load device can be updated by substituting this output voltage into (5.49).

$$\begin{aligned}
 V_{T,load} &= V_{T0,load} + \gamma \left(\sqrt{|2\phi_F| + V_{OL}} - \sqrt{|2\phi_F|} \right) \\
 &= -3 + 0.4 \left(\sqrt{0.6 + 0.2} - \sqrt{0.6} \right) = -2.95 \text{ V}
 \end{aligned}$$

Using this new value for $V_{T,load}$, we now recalculate V_{OL} , again according to (5.54).

$$\begin{aligned} V_{OL} &= 0.186 \text{ V} \\ V_{T,load} &= -2.95 \text{ V} \end{aligned}$$

At this point, we can stop the iteration process since the threshold voltage of the load device has not changed in the two significant digits after the decimal point. Continuing the iteration would not produce a perceptible improvement of V_{OL} .

The calculation of V_{IL} involves simultaneous solution of (5.49), (5.55), and (5.57), using numerical iterations. When the input voltage is equal to V_{IL} , we expect that the output voltage is slightly lower than the output high voltage, V_{OH} . As a first-order approximation, assume that $V_{out} = V_{OH} = 5 \text{ V}$ for $V_{in} = V_{IL}$. Then, the threshold voltage of the load device can be estimated as $V_{T,load}(V_{out} = 5 \text{ V}) = -2.36 \text{ V}$. Substituting this value into (5.57) gives V_{IL} as a function of the output voltage V_{out}

$$\begin{aligned} V_{IL}(V_{out}) &= V_{T0} + \frac{k_{load}}{k_{driver}} \cdot [V_{out} - V_{DD} + |V_{T,load}(V_{out})|] \\ &= 1 + \left(\frac{1}{6}\right)(V_{out} - 5 + 2.36) = 0.167 V_{out} + 0.56 \end{aligned}$$

This expression can be rearranged as

$$V_{out} = 6 V_{IL} - 3.35$$

Now, substitute this into the KCL equation (5.55) to obtain the following quadratic equation for V_{IL} :

$$\begin{aligned} \frac{k_{driver}}{2} \cdot (V_{IL} - V_{T0})^2 &= \frac{k_{load}}{2} \cdot [2|V_{T,load}(V_{out})| \cdot (V_{DD} - 6 V_{IL} + 3.35) \\ &\quad - (V_{DD} - 6 V_{IL} + 3.35)^2] \\ 2 \cdot (V_{IL} - 1)^2 &= \frac{1}{3} \cdot [2 \cdot 2.36 \cdot (5 - 6 V_{IL} + 3.35) - (5 - 6 V_{IL} + 3.35)^2] \end{aligned}$$

The solution of this second-order equation yields two possible values for V_{IL} .

$$V_{IL} = \begin{cases} 0.98 \text{ V} \\ \underline{\underline{1.36 \text{ V}}} \end{cases}$$

Note that V_{IL} must be larger than the threshold voltage V_{T0} of the driver transistor, hence, $V_{IL} = 1.36 \text{ V}$ is the physically correct solution. The output voltage level at this point can also be found as

$$V_{out} = 6 \cdot 1.36 - 3.35 = 4.81 \text{ V}$$

which significantly improves our initial assumption of $V_{out} = 5 \text{ V}$. At this point, the threshold voltage of the load transistor must be recalculated, in order to update its value. Substituting $V_{out} = 4.81 \text{ V}$ into (5.49) yields $V_{T,load} = -2.38 \text{ V}$. We observe that this value is only slightly higher (by 20 mV) than the threshold voltage value used in the previous calculations. For practical purposes, we can terminate the numerical iteration at this stage and accept $V_{IL} = 1.36 \text{ V}$ as a fairly accurate estimate.

To calculate V_{IH} , we have to find the numerical value of $(dV_{T,load}/dV_{out})$ first, according to (5.61). When the input voltage is equal to V_{IH} , the output voltage is expected to be relatively low. As a first-order approximation, assume that the output voltage level is $V_{out} = V_{OL} \approx 0.2 \text{ V}$ when $V_{in} = V_{IH}$. The threshold voltage of the load device can also be estimated as $V_{T,load}(V_{out} = 0.2 \text{ V}) = -2.95 \text{ V}$. Thus,

$$\frac{dV_{T,load}}{dV_{out}} = \frac{\gamma}{2\sqrt{|2\phi_F| + V_{out}}} = \frac{0.4}{2\sqrt{0.6 + 0.2}} = 0.22$$

This value can now be used in (5.60) to find V_{IH} as a function of the output voltage.

$$\begin{aligned} V_{IH}(V_{out}) &= V_{T0} + 2V_{out} + \frac{k_{load}}{k_{driver}} \cdot [-V_{T,load}(V_{out})] \cdot \left(\frac{dV_{T,load}}{dV_{out}} \right) \\ &= 1 + 2V_{out} + \left(\frac{1}{6} \right) \cdot 2.95 \cdot 0.22 = 2V_{out} + 1.1 \end{aligned}$$

This expression is rearranged as:

$$V_{out} = 0.5V_{IH} - 0.55$$

Next, substitute V_{out} in the KCL equation (5.58), to obtain

$$2 \cdot \left[2 \cdot (V_{IH} - 1) \cdot (0.5 V_{IH} - 0.55) - (0.5 V_{IH} - 0.55)^2 \right] = \frac{1}{3} \cdot (2.95)^2$$

The solution of this simple quadratic equation yields two values for V_{IH} :

$$V_{IH} = \begin{cases} 0.10 \text{ V} \\ \underline{\underline{1.96 \text{ V}}} \end{cases}$$

where $V_{IH} = 1.96 \text{ V}$ is the physically correct solution, since V_{IH} must be larger than the driver threshold voltage. The output voltage level at this point is calculated as

$$V_{out} = 0.5 \cdot 1.96 - 0.55 = 0.43 \text{ V}$$

With this updated output voltage value, we can now reevaluate the load threshold voltage as $V_{T,load}(V_{out} = 0.43 \text{ V}) = -2.9 \text{ V}$, and the $(dV_{T,load}/V_{out})$ value as

$$\frac{dV_{T,load}}{dV_{out}} = 0.19$$

Note both of these values are fairly close to those used at the beginning of this iteration process. Repeating the iterative calculation will provide only a marginal improvement of accuracy, thus, we may accept $V_{IH} = 1.96 \text{ V}$ as a good estimate.

In conclusion, the noise margins for high signal levels and for low signal levels can be found as follows:

$$NM_H = V_{OH} - V_{IH} = 3.04 \text{ V}$$

$$NM_L = V_{IL} - V_{OL} = 1.17 \text{ V}$$

5.5. CMOS Inverter

All of the inverter circuits considered so far had the general circuit structure shown in Fig. 5.3, consisting of an enhancement-type nMOS driver transistor, and a load device which can be a resistor, an enhancement-type nMOS transistor, or a depletion-type nMOS transistor acting as a nonlinear resistor. In this general configuration, the input signal is always applied to the gate of the driver transistor, and the operation of the

inverter is controlled primarily by switching the driver. Now, we will turn our attention to a radically different inverter structure, which consists of an enhancement-type nMOS transistor and an enhancement-type pMOS transistor, operating in complementary mode (Fig. 5.19). This configuration is called Complementary MOS, or CMOS. The circuit topology is complementary push-pull in the sense that for high input, the nMOS transistor drives (pulls down) the output node while the pMOS transistor acts as the load, and for low input the pMOS transistor drives (pulls up) the output node while the nMOS transistor acts as the load. Consequently, both devices contribute equally to the circuit operation characteristics.

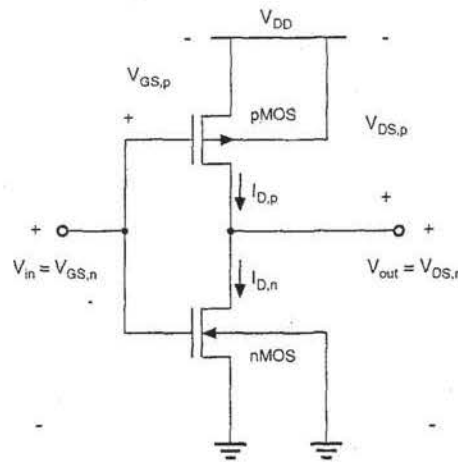


Figure 5.19. CMOS inverter circuit.

The CMOS inverter has two important advantages over the other inverter configurations. The first and perhaps the most important advantage is that the steady-state power dissipation of the CMOS inverter circuit is virtually negligible, except for small power dissipation due to leakage currents. In all other inverter structures examined so far, a nonzero steady-state current is drawn from the power source when the driver transistor is turned on, which results in a significant DC power consumption. The other advantages of the CMOS configuration are that the voltage transfer characteristic (VTC) exhibits a full output voltage swing between 0 V and V_{DD} , and that the VTC transition is usually very sharp. Thus, the VTC of the CMOS inverter resembles that of an ideal inverter.

Since nMOS and pMOS transistors must be fabricated on the same chip side-by-side, the CMOS process is more complex than the standard nMOS-only process. In particular, the CMOS process must provide an n-type substrate for the pMOS

transistors and a p-type substrate for the nMOS transistors. This can be achieved by building either n-type *tubs* (wells) on a p-type wafer, or by building p-type tubs on an n-type wafer (cf. Chapter 2). In addition, the close proximity of an nMOS and a pMOS transistor may lead to the formation of two parasitic bipolar transistors, causing a *latch-up* condition. In order to prevent this undesirable effect, additional *guard rings* must be built around the nMOS and the pMOS transistors as well. The increased process complexity of CMOS fabrication may be considered as the price being paid for the improvements achieved in power consumption and noise margins.

Circuit Operation

In Fig. 5.19, note that the input voltage is connected to the gate terminals of both the nMOS and the pMOS transistors. Thus, both transistors are driven directly by the input signal, V_{in} . The substrate of the nMOS transistor is connected to the ground, while the substrate of the pMOS transistor is connected to the power supply voltage, V_{DD} , in order to reverse-bias the source and drain junctions. Since $V_{SB} = 0$ for both devices, there will be no substrate-bias effect for either device. It can be seen from the circuit diagram in Fig. 5.19 that

$$\begin{aligned} V_{GS,n} &= V_{in} \\ V_{DS,n} &= V_{out} \end{aligned} \quad (5.67)$$

and also,

$$\begin{aligned} V_{GS,p} &= -(V_{DD} - V_{in}) \\ V_{DS,p} &= -(V_{DD} - V_{out}) \end{aligned} \quad (5.68)$$

We will start our analysis by considering two simple cases. When the input voltage is smaller than the nMOS threshold voltage, i.e., when $V_{in} < V_{T0,n}$, the nMOS transistor is cut-off. At the same time, the pMOS transistor is on, operating in the linear region. Since the drain currents of both transistors are approximately equal to zero (except for small leakage currents), i.e.,

$$I_{D,n} = I_{D,p} = 0 \quad (5.69)$$

the drain-to-source voltage of the pMOS transistor is also equal to zero, and the output voltage V_{OH} is equal to the power supply voltage.

$$V_{out} = V_{OH} = V_{DD} \quad (5.70)$$

On the other hand, when the input voltage exceeds $(V_{DD} + V_{T0,p})$, the pMOS transistor is turned off. In this case, the nMOS transistor is operating in the linear region, but its drain-to-source voltage is equal to zero because condition (5.69) is satisfied. Consequently, the output voltage of the circuit is

$$V_{out} = V_{OL} = 0 \quad (5.71)$$

Next, we examine the operating modes of the nMOS and the pMOS transistors as functions of the input and output voltages. The nMOS transistor operates in *saturation* if $V_{in} > V_{T0,n}$ and if the following condition is satisfied.

$$V_{DS,n} \geq V_{GS,n} - V_{T0,n} \Leftrightarrow V_{out} \geq V_{in} - V_{T0,n} \quad (5.72)$$

The pMOS transistor operates in *saturation* if $V_{in} < (V_{DD} + V_{T0,p})$, and if :

$$V_{DS,p} \leq V_{GS,p} - V_{T0,p} \Leftrightarrow V_{out} \leq V_{in} - V_{T0,p} \quad (5.73)$$

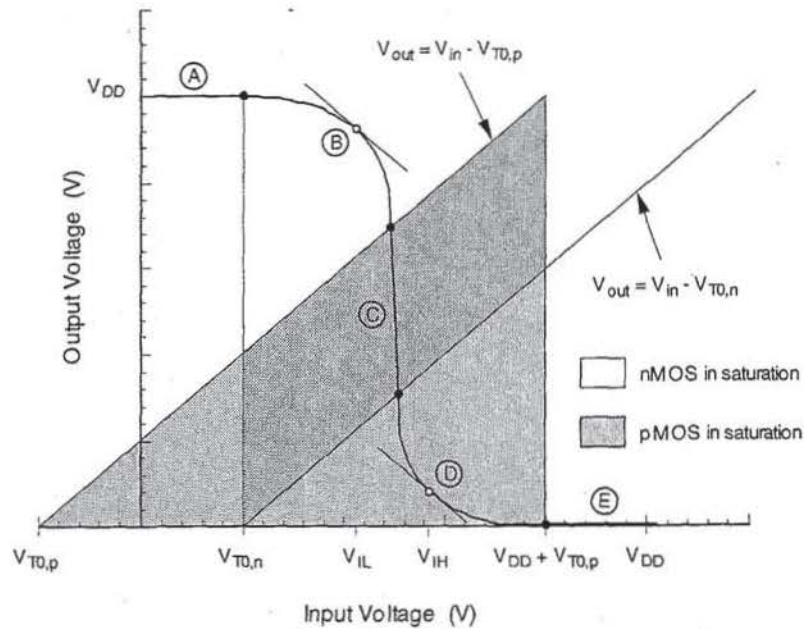


Figure 5.20. Operating regions of the nMOS and the pMOS transistors.

Both of these conditions for device saturation are illustrated graphically as shaded areas on the $V_{out} - V_{in}$ plane in Fig. 5.20. A typical CMOS inverter voltage transfer characteristic is also superimposed for easy reference. Here, we identify five distinct regions, labeled A through E, each corresponding to a different set of operating conditions. The table below lists these regions and the corresponding critical input and output voltage levels.

Region	V_{in}	V_{out}	nMOS	pMOS
A	$< V_{T0,n}$	V_{OH}	cut-off	linear
B	V_{IL}	high $\approx V_{OH}$	saturation	linear
C	V_{th}	V_{th}	saturation	saturation
D	V_{IH}	low $\approx V_{OL}$	linear	saturation
E	$> (V_{DD} + V_{T0,p})$	V_{OL}	linear	cut-off

In Region A, where $V_{in} < V_{T0,n}$, the nMOS transistor is cut-off and the output voltage is equal to $V_{OH} = V_{DD}$. As the input voltage is increased beyond $V_{T0,n}$ (into Region B), the nMOS transistor starts conducting in saturation mode and the output voltage begins to decrease. Also note that the critical voltage V_{IL} which corresponds to $(dV_{out}/dV_{in}) = -1$ is located within Region B. As the output voltage further decreases, the pMOS transistor enters saturation at the boundary of Region C. It is seen from Fig. 5.20 that the inverter threshold voltage, where $V_{in} = V_{out}$, is located in Region C. When the output voltage V_{out} falls below $(V_{in} - V_{T0,n})$, the nMOS transistor starts to operate in linear mode. This corresponds to Region D in Fig. 5.20, where the critical voltage point V_{IH} with $(dV_{out}/dV_{in}) = -1$ is also located. Finally, in Region E, with the input voltage $V_{in} > (V_{DD} + V_{T0,p})$, the pMOS transistor is cut-off, and the output voltage is $V_{OL} = 0$.

In a simplistic analogy, the nMOS and the pMOS transistors can be seen as nearly ideal switches—controlled by the input voltage—that connect the output node to the power supply voltage or to the ground potential, depending on the input voltage level. The qualitative overview of circuit operation, illustrated in Fig. 5.20 and discussed above, also highlights the complementary nature of the CMOS inverter. The most significant feature of this circuit is that the current drawn from the power supply in both of these steady-state operating points, i.e., in Region A and in Region E, is nearly equal to zero. The only current that flows in either case is the very small leakage current of the reverse-biased source and drain junctions. The CMOS inverter can drive any load, such as interconnect capacitance or fanout logic gates which are connected to its output node, either by supplying current to, or by sinking current from, the load.

The steady-state input-output voltage characteristics of the CMOS inverter can be better visualized by considering the interaction of individual nMOS and pMOS transistor characteristics in the current-voltage space. We already know that the drain current $I_{D,n}$ of the nMOS transistor is a function of the voltages $V_{GS,n}$ and $V_{DS,n}$. Hence, the nMOS drain current is also a function of the inverter input and output voltages V_{in} and V_{out} according to (5.67).

$$I_{D,n} = f(V_{in}, V_{out})$$

This two-variable function, which is essentially described by the current equations (3.54)–(3.56), can be represented as a *surface* in the three-dimensional current-voltage space. Figure 5.21 shows this $I_{D,n}(V_{in}, V_{out})$ surface for the nMOS transistor.

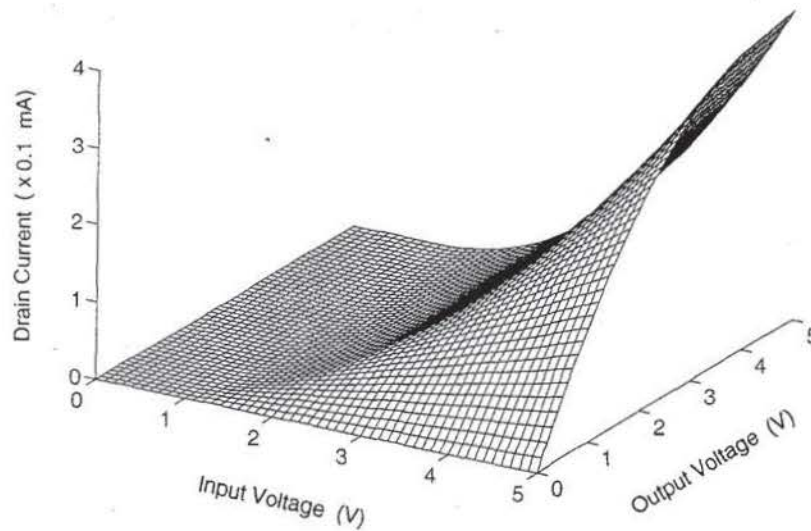


Figure 5.21. Current-voltage surface representing the nMOS transistor characteristics.

Similarly, the drain current $I_{D,p}$ of the pMOS transistor is also a function of the inverter input and output voltages V_{in} and V_{out} according to (5.68).

$$I_{D,p} = f(V_{in}, V_{out})$$

This two-variable function, described by the current equations (3.57)–(3.59), can be represented as another surface in the three-dimensional current-voltage space. Figure 5.22 shows the corresponding $I_{D,p}(V_{in}, V_{out})$ surface for the pMOS transistor.

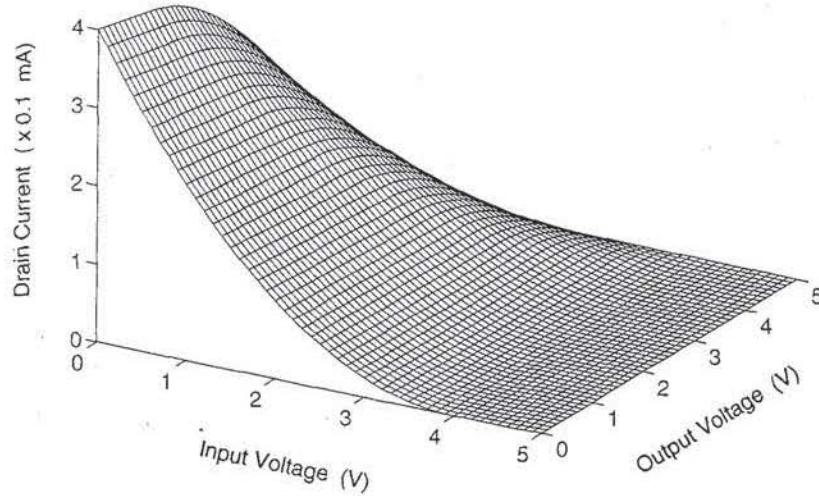


Figure 5.22. Current-voltage surface representing the pMOS transistor characteristics.

Remember that in a CMOS inverter operating in steady-state, the drain current of the nMOS transistor is always equal to the drain current of the pMOS transistor, according to KCL:

$$I_{D,n} = I_{D,p}$$

Thus, the *intersection* of the two current-voltage surfaces shown in Figs. 5.21 and 5.22 will give the operating curve of the CMOS inverter circuit in the three-dimensional current-voltage space. The intersection of the two characteristic surfaces is shown in Fig. 5.23. The intersecting surfaces are shown from a different viewing angle in Fig. 5.24, with the intersection curve highlighted in bold.

It is clear that the vertical projection of the intersection curve on the $V_{in} - V_{out}$ plane produces the typical CMOS inverter voltage transfer characteristic already shown in Fig. 5.20. Similarly, the horizontal projection of the intersection curve on the $I_D - V_{in}$ plane gives the steady-state current drawn by the inverter from the power supply voltage as a function of the input voltage.

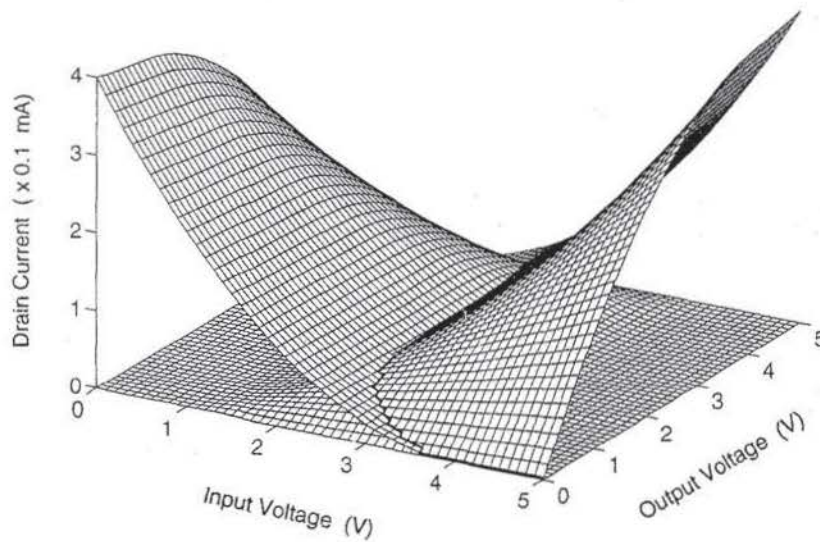


Figure 5.23. Intersection of the current-voltage surfaces shown in Figures 5.21 and 5.22.

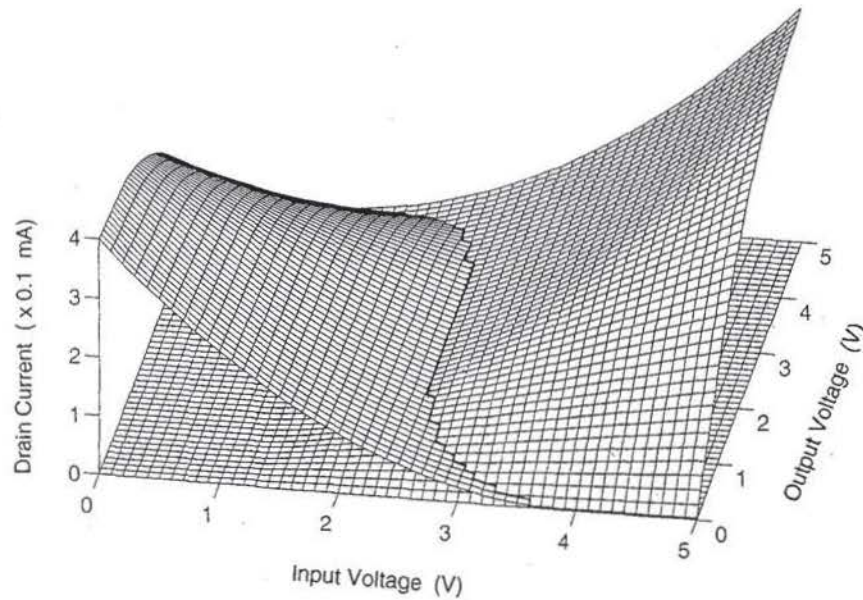


Figure 5.24. The intersecting current-voltage surfaces shown from a different viewing angle. Notice that projection of the intersection curve on the voltage plane gives the VTC.

In the following, we will present an in-depth analysis of the CMOS inverter static characteristics, by calculating the critical voltage points on the VTC. It has already been established that $V_{OH} = V_{DD}$ and $V_{OL} = 0$ for this inverter; thus, we will devote our attention to V_{IL} , V_{IH} and the inverter switching threshold, V_{th} .

Calculation of V_{IL}

By definition, the slope of the VTC is equal to (-1) , i.e., $dV_{out}/dV_{in} = -1$ when the input voltage is $V_{in} = V_{IL}$. Note that in this case, the nMOS transistor operates in saturation while the pMOS transistor operates in the linear region. From $I_{D,n} = I_{D,p}$, we obtain the following current equation.

$$\frac{k_n}{2} \cdot (V_{GS,n} - V_{T0,n})^2 = \frac{k_p}{2} \cdot [2 \cdot (V_{GS,p} - V_{T0,p}) \cdot V_{DS,p} - V_{DS,p}^2] \quad (5.74)$$

Using equations (5.67) and (5.68), this expression can be rewritten as

$$\frac{k_n}{2} \cdot (V_{in} - V_{T0,n})^2 = \frac{k_p}{2} \cdot [2 \cdot (V_{in} - V_{DD} - V_{T0,p}) \cdot (V_{out} - V_{DD}) - (V_{out} - V_{DD})^2] \quad (5.75)$$

To satisfy the derivative condition at V_{IL} , we differentiate both sides of (5.75) with respect to V_{in} .

$$k_n \cdot (V_{in} - V_{T0,n}) = k_p \cdot \left[(V_{in} - V_{DD} - V_{T0,p}) \cdot \left(\frac{dV_{out}}{dV_{in}} \right) + (V_{out} - V_{DD}) - (V_{out} - V_{DD}) \cdot \left(\frac{dV_{out}}{dV_{in}} \right) \right] \quad (5.76)$$

Substituting $V_{in} = V_{IL}$ and $(dV_{out}/dV_{in}) = -1$ in (5.76), we obtain

$$k_n \cdot (V_{IL} - V_{T0,n}) = k_p \cdot (2V_{out} - V_{IL} + V_{T0,p} - V_{DD}) \quad (5.77)$$

The critical voltage V_{IL} can now be found as a function of the output voltage V_{out} as follows.

$$V_{IL} = \frac{2V_{out} + V_{T0,p} - V_{DD} + k_R V_{T0,n}}{1 + k_R} \quad (5.78)$$

where k_R is defined as

$$k_R = \frac{k_n}{k_p}$$

This equation must be solved together with the KCL equation (5.75) to obtain the numerical value of V_{IL} and the corresponding output voltage, V_{out} . Note that the solution is fairly straightforward and does not require numerical iterations as in the previous cases, since none of the transistors is subject to substrate-bias effects.

Calculation of V_{IH}

When the input voltage is equal to V_{IH} , the nMOS transistor operates in the linear region, and the pMOS transistor operates in saturation. Applying KCL to the output node, we obtain

$$\frac{k_n}{2} \cdot [2 \cdot (V_{GS,n} - V_{T0,n}) \cdot V_{DS,n} - V_{DS,n}^2] = \frac{k_p}{2} \cdot (V_{GS,p} - V_{T0,p})^2 \quad (5.79)$$

Using equations (5.67) and (5.68), this expression can be rewritten as

$$\frac{k_n}{2} \cdot [2 \cdot (V_{in} - V_{T0,n}) \cdot V_{out} - V_{out}^2] = \frac{k_p}{2} \cdot (V_{in} - V_{DD} - V_{T0,p})^2 \quad (5.80)$$

Now, differentiate both sides of (5.80) with respect to V_{in} .

$$\begin{aligned} k_n \cdot \left[(V_{in} - V_{T0,n}) \cdot \left(\frac{dV_{out}}{dV_{in}} \right) + V_{out} - V_{out} \cdot \left(\frac{dV_{out}}{dV_{in}} \right) \right] \\ = k_p \cdot (V_{in} - V_{DD} - V_{T0,p}) \end{aligned} \quad (5.81)$$

Substituting $V_{in} = V_{IH}$ and $(dV_{out}/dV_{in}) = -1$ in (5.81), we obtain

$$k_n \cdot (-V_{IH} + V_{T0,n} + 2V_{out}) = k_p \cdot (V_{IH} - V_{DD} - V_{T0,p}) \quad (5.82)$$

The critical voltage V_{IH} can now be found as a function of V_{out} as follows.

$$V_{IH} = \frac{V_{DD} + V_{T0,p} + k_R \cdot (2V_{out} + V_{T0,n})}{1 + k_R} \quad (5.83)$$

Again, this equation must be solved simultaneously with the KCL equation (5.80) to obtain the numerical values of V_{IH} and V_{out} .

Calculation of V_{th}

The inverter threshold voltage is defined as $V_{th} = V_{in} = V_{out}$. Since the CMOS inverter exhibits large noise margins and a very sharp VTC transition, the inverter threshold voltage emerges as an important parameter characterizing the DC performance of the inverter. For $V_{in} = V_{out}$, both transistors are expected to be in saturation; hence, we can write the following KCL equation.

$$\frac{k_n}{2} \cdot (V_{GS,n} - V_{T0,n})^2 = \frac{k_p}{2} \cdot (V_{GS,p} - V_{T0,p})^2 \quad (5.84)$$

Replacing $V_{GS,n}$ and $V_{GS,p}$ in (5.84) according to (5.67) and (5.68), we obtain

$$\frac{k_n}{2} \cdot (V_{in} - V_{T0,n})^2 = \frac{k_p}{2} \cdot (V_{in} - V_{DD} - V_{T0,p})^2 \quad (5.85)$$

The correct solution for V_{in} for this equation is

$$V_{in} \cdot \left(1 + \sqrt{\frac{k_p}{k_n}} \right) = V_{T0,n} + \sqrt{\frac{k_p}{k_n}} \cdot (V_{DD} + V_{T0,p}) \quad (5.86)$$

Finally, the inverter threshold (switching threshold) voltage V_{th} is found as

$$V_{th} = \frac{V_{T0,n} + \sqrt{\frac{1}{k_R}} \cdot (V_{DD} + V_{T0,p})}{\left(1 + \sqrt{\frac{1}{k_R}} \right)} \quad (5.87)$$

Note that the inverter threshold voltage is defined as $V_{th} = V_{in} = V_{out}$. When the input voltage is equal to V_{th} , however, we find that the output voltage can actually attain any value between $(V_{th} - V_{T0,n})$ and $(V_{th} - V_{T0,p})$, without violating the voltage conditions used in this analysis. This is due to the fact that the VTC segment corresponding to Region C in Fig. 5.20 becomes completely vertical if the channel-length modulation effect is neglected, i.e., if $\lambda = 0$. In more realistic cases with $\lambda > 0$, the VTC segment in Region C exhibits a finite, but very large, slope.

It has already been established that the CMOS inverter does not draw any significant current from the power source, except for small leakage and subthreshold currents, when the input voltage is either smaller than $V_{T0,n}$ or larger than $(V_{DD} + V_{T0,p})$. The nMOS and the pMOS transistors conduct a nonzero current, on the other hand, during low-to-high and high-to-low transitions, i.e., in Regions B, C, and D. It can be shown that the current being drawn from the power source during transition reaches its peak value when $V_{in} = V_{th}$. In other words, the maximum current is drawn when both transistors are operating in saturation. Figure 5.25 shows the voltage transfer characteristic of a typical CMOS inverter circuit and the power supply current, as a function of the input voltage.

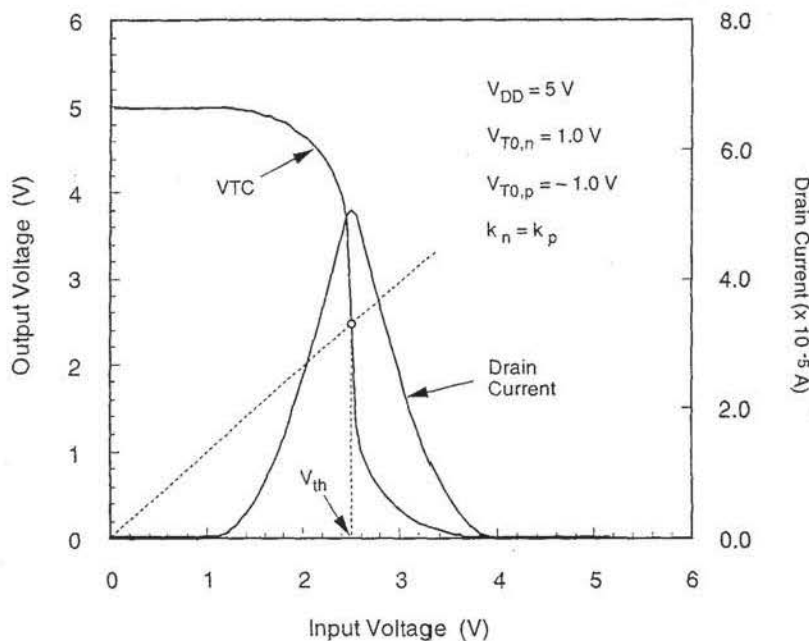


Figure 5.25 Typical VTC and the power supply current of a CMOS inverter circuit.

Design of CMOS Inverters

The inverter threshold voltage V_{th} was identified as one of the most important parameters that characterize the steady-state input-output behavior of the CMOS inverter circuit. The CMOS inverter can, by virtue of its complementary push-pull operating mode, provide a full output voltage swing between 0 and V_{DD} , and therefore, the noise margins are relatively wide. Thus, the problem of designing a CMOS inverter can be reduced to setting the inverter threshold to a desired voltage value.

Given the power supply voltage V_{DD} , the nMOS and the pMOS transistor threshold voltages, and the desired inverter threshold voltage V_{th} , the corresponding ratio k_R can be found as follows. Reorganizing (5.87) yields

$$\sqrt{\frac{1}{k_R}} = \frac{V_{th} - V_{T0,n}}{V_{DD} + V_{T0,p} - V_{th}} \quad (5.88)$$

Now solve for k_R that is required to achieve the given V_{th} :

$$k_R = \frac{k_n}{k_p} = \left(\frac{V_{DD} + V_{T0,p} - V_{th}}{V_{th} - V_{T0,n}} \right)^2 \quad (5.89)$$

Recall that the switching threshold voltage of an *ideal* inverter is defined as

$$V_{th,ideal} = \frac{1}{2} \cdot V_{DD} \quad (5.90)$$

Substituting (5.90) in (5.89) gives

$$\left(\frac{k_n}{k_p} \right)_{ideal} = \left(\frac{0.5 V_{DD} + V_{T0,p}}{0.5 V_{DD} - V_{T0,n}} \right)^2 \quad (5.91)$$

for a near-ideal CMOS VTC that satisfies the condition (5.90). Since the operations of the nMOS and the pMOS transistors of the CMOS inverter are fully complementary, we can achieve completely symmetric input-output characteristics by setting the threshold voltages as $V_{T0} = V_{T0,n} = |V_{T0,p}|$. This reduces (5.91) to:

$$\left(\frac{k_n}{k_p} \right)_{\text{symmetric inverter}} = 1 \quad (5.92)$$

Note that the ratio k_R is defined as

$$\frac{k_n}{k_p} = \frac{\mu_n C_{ox} \cdot \left(\frac{W}{L} \right)_n}{\mu_p C_{ox} \cdot \left(\frac{W}{L} \right)_p} = \frac{\mu_n \cdot \left(\frac{W}{L} \right)_n}{\mu_p \cdot \left(\frac{W}{L} \right)_p} \quad (5.93)$$

assuming that the gate oxide thickness t_{ox} , and hence, the gate oxide capacitance C_{ox} have the same value for both nMOS and pMOS transistors. The unity-ratio condition (5.92) for the ideal symmetric inverter requires that

$$\frac{\left(\frac{W}{L} \right)_n}{\left(\frac{W}{L} \right)_p} = \frac{\mu_p}{\mu_n} \approx \frac{230 \text{ cm}^2/\text{V}\cdot\text{s}}{580 \text{ cm}^2/\text{V}\cdot\text{s}} \quad (5.94)$$

Hence,

$$\left(\frac{W}{L} \right)_p \approx 2.5 \left(\frac{W}{L} \right)_n \quad (5.95)$$

It should be noted that the numerical values used in (5.94) for electron and hole mobilities are *typical* values, and that exact μ_n and μ_p values will vary with surface doping concentration of the substrate and the tub. The VTCs of three CMOS inverter circuits with different k_R ratios are shown in Fig. 5.26. It can be seen clearly that the inverter threshold voltage V_{th} shifts to lower values with increasing k_R ratio.

For a symmetric CMOS inverter with $V_{T0,n} = |V_{T0,p}|$ and $k_R = 1$, the critical voltage V_{IL} can be found, using (5.78), as follows.

$$V_{IL} = \frac{1}{8} \cdot (3V_{DD} + 2V_{T0,n}) \quad (5.96)$$

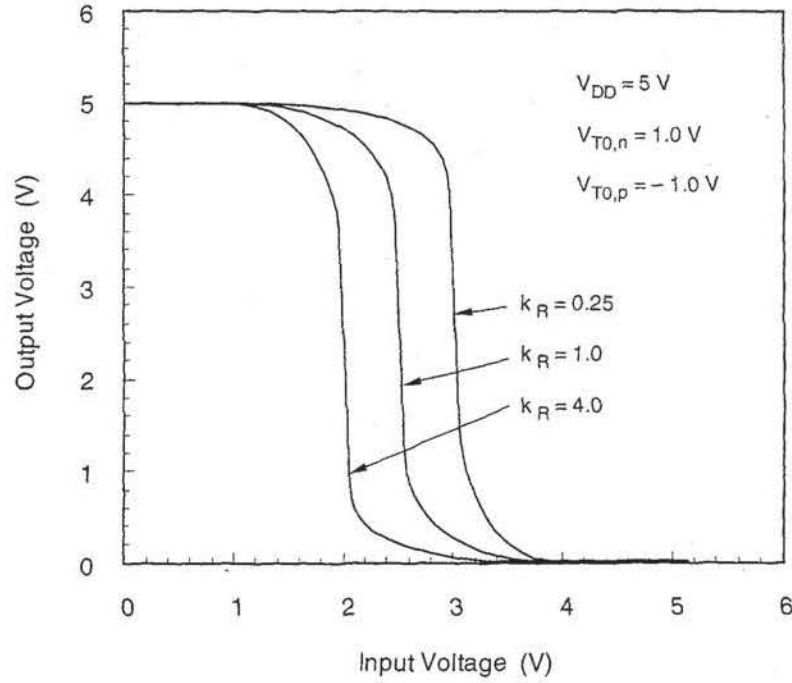


Figure 5.26. Voltage transfer characteristics of three CMOS inverters, with different nMOS-to-pMOS ratios.

Also, the critical voltage V_{IH} is found as

$$V_{IH} = \frac{1}{8} \cdot (5V_{DD} - 2V_{T0,n}) \quad (5.97)$$

Note that the sum of V_{IL} and V_{IH} is always equal to V_{DD} in a symmetric inverter:

$$V_{IL} + V_{IH} = V_{DD} \quad (5.98)$$

The noise margins NM_L and NM_H for this symmetric CMOS inverter are now calculated using (5.3) and (5.4):

$$\begin{aligned} NM_L &= V_{IL} - V_{OL} = V_{IL} \\ NM_H &= V_{OH} - V_{IH} = V_{DD} - V_{IH} \end{aligned} \quad (5.99)$$

which are equal to each other, and also to V_{IL} .

$$NM_L = NM_H = V_{IL} \quad (5.100)$$

Example 5.4

Consider a CMOS inverter circuit with the following parameters :

$$\begin{aligned} V_{DD} &= 5 \text{ V} \\ V_{T0,n} &= 1.0 \text{ V} \\ V_{T0,p} &= -1.2 \text{ V} \\ k_n &= 100 \mu\text{A/V}^2 \\ k_p &= 40 \mu\text{A/V}^2 \end{aligned}$$

Calculate the noise margins of the circuit. Notice that the CMOS inverter being considered here has $k_R = 2.5$ and $V_{T0,n} \neq |V_{T0,p}|$; hence, it is not a symmetric inverter.

First, the output low voltage V_{OL} and the output high voltage V_{OH} are found, using (5.70) and (5.71), as $V_{OL} = 0$ and $V_{OH} = 5 \text{ V}$.

To calculate V_{IL} in terms of the output voltage, we use (5.78):

$$\begin{aligned} V_{IL} &= \frac{2V_{out} + V_{T0,p} - V_{DD} + k_R V_{T0,n}}{1 + k_R} \\ &= \frac{2V_{out} - 1.2 - 5 + 2.5}{1 + 2.5} = 0.57V_{out} - 1.06 \end{aligned}$$

Now substitute this expression into the KCL equation (5.75).

$$2.5(0.57V_{out} - 1.06 - 1)^2 = 2(0.57V_{out} - 1.06 - 5 + 1.2)(V_{out} - 5) - (V_{out} - 5)^2$$

This expression yields a second-order polynomial in V_{out} as follows.

$$0.66 V_{out}^2 - 0.46 V_{out} - 13 = 0$$

Only one root of this quadratic equation corresponds to a physically correct solution for V_{out} (i.e., $V_{out} > 0$).

$$V_{out} = 4.8 \text{ V}$$

From this value, we can calculate the critical voltage V_{IL} as:

$$V_{IL} = 0.57 \cdot 4.8 - 1.06 = \underline{\underline{1.68 \text{ V}}}$$

To calculate V_{IH} in terms of the output voltage, use (5.83):

$$\begin{aligned} V_{IH} &= \frac{V_{DD} + V_{T0,p} + k_R \cdot (2 V_{out} + V_{T0,n})}{1 + k_R} \\ &= \frac{5 - 1.2 + 2.5(2 V_{out} + 1)}{1 + 2.5} = 1.43 V_{out} + 1.8 \end{aligned}$$

Next, substitute this expression into the KCL equation (5.80) to obtain a second-order polynomial in V_{out}

$$2.5[2(1.43 V_{out} + 1.8 - 1)V_{out} - V_{out}^2] = (1.43 V_{out} - 2)^2$$

$$2.61 V_{out}^2 + 9.72 V_{out} - 4 = 0$$

Again, only one root of this quadratic equation corresponds to the physically correct solution for V_{out} at this operating point, i.e., when $V_{in} = V_{IH}$.

$$V_{out} = 0.37 \text{ V}$$

From this value, we can calculate the critical voltage V_{IH} as :

$$V_{IH} = 1.43 \cdot 0.37 + 1.8 = \underline{\underline{2.33 \text{ V}}}$$

Finally, we find the noise margins for low voltage levels and for high voltage levels using (5.3) and (5.4).

$$NM_L = V_{IL} - V_{OL} = 1.68 \text{ V}$$

$$NM_H = V_{OH} - V_{IH} = 2.66 \text{ V}$$

Power and Area Considerations

Since the CMOS inverter does not draw any significant current from the power source in both of its steady-state operating points ($V_{out} = V_{OH}$ and $V_{out} = V_{OL}$), the DC power dissipation of this circuit is almost negligible. The drain current that flows through the nMOS and the pMOS transistors in both cases is essentially limited to the reverse leakage current of the source and drain pn-junctions, and in short-channel MOSFETs, the relatively small subthreshold current. This unique property of the CMOS inverter was already identified as one of the most important advantages of this configuration. In many applications requiring a low overall power consumption, CMOS is preferred over other circuit alternatives for this reason. It must be noted, however, that the CMOS inverter does conduct a significant amount of current during a *switching event*, i.e., when the output voltage changes from a low to high state, or from a high to low state. The detailed calculation of this *dynamic power dissipation* will be examined in Chapter 6.

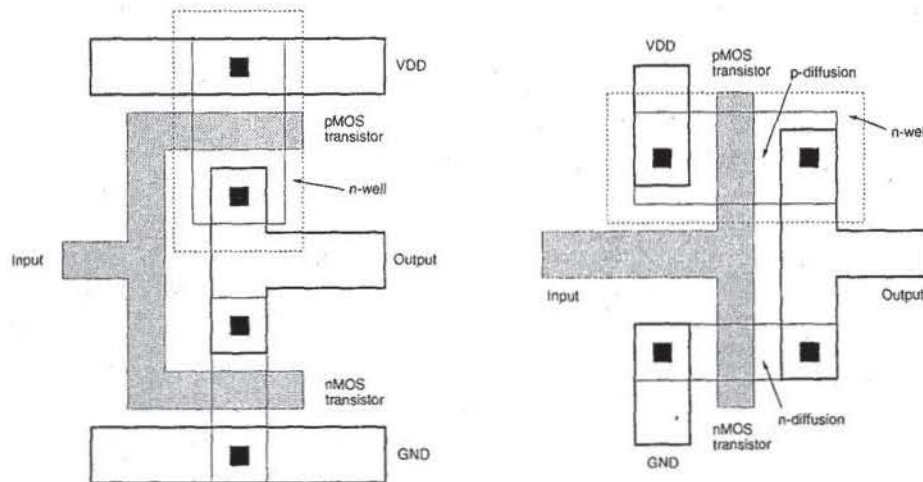


Figure 5.27. Sample layouts of CMOS inverter circuits (for p-type substrate).

Figure 5.27 shows two layout examples for the simple CMOS inverter circuit. In both cases, it is assumed that the circuit is being built on a p -type wafer, which also provides the substrate for the nMOS transistor. The pMOS transistor, on the other hand, must be placed in an n-well (dotted lines), which becomes the substrate for this device. Also note that in Fig. 5.27 the channel width of the pMOS transistor is larger than that of the nMOS transistor. This is typical for symmetric inverter configurations, in which the k_R ratio is set approximately equal to unity.

Compared to other inverter layouts examined in previous sections, the CMOS inverters shown in Fig. 5.27 do not occupy significantly more area. The added complexity of the fabrication process (creating n-well diffusion, separate p -type and n -type source and drain diffusions, etc.) appears to be the only drawback for the inverter example. Because of the complementary nature of this circuit configuration, however, CMOS random logic circuits require significantly more transistors for the same function than their nMOS counterparts. Consequently, CMOS logic circuits tend to occupy more area than comparable nMOS logic circuits, which apparently affects the integration density of pure-CMOS logic. The actual integration density of nMOS logic, on the other hand, is limited by power dissipation and heat generation problems.

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Exercise Problems

- 5.1** Consider an inverter with an enhancement-type nMOS driver transistor and an enhancement-type saturated nMOS load transistor with its gate and drain terminals tied. For the following parameters, calculate the noise margin, NM_L , i.e., the noise margin corresponding to the "0" level signal.

$$\begin{aligned} k_{\text{driver}}/k_{\text{load}} &= 10.0 \\ V_{T0} &= 0.8 \text{ V}, V_{DD} = 5.0 \text{ V} \\ \gamma &= \lambda = 0 \end{aligned}$$

- 5.2** For the saturated enhancement-load inverter in exercise problem (5.1), determine the highest output voltage V_{OH} when the input gate voltage is less than the threshold voltage by using the following device parameters:

$$\begin{aligned} \mu_n \cdot C_{ox} &= 20 \mu\text{A/V}^2 \\ V_{T0} &= 1.0 \text{ V}, \quad \gamma = 0.4 \text{ V}^{1/2} \\ \text{channel length modulation factor } (\lambda) &= 0.0 \text{ V}^{-1} \\ \text{surface potential } |2\phi_F| &= 0.64 \text{ V} \end{aligned}$$

- 5.3** Determine the steady-state voltage across the load capacitor shown in Fig. P5.3 below. You must include the body effect of both transistors. Use the following device parameters:

$$\begin{aligned} V_{T0} &= 1.0 \text{ V} \\ \gamma \text{ (body effect coefficient)} &= 0.2 \text{ V}^{1/2} \\ \phi_F &= -0.3 \text{ V} \end{aligned}$$

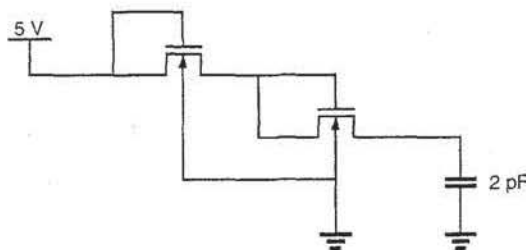
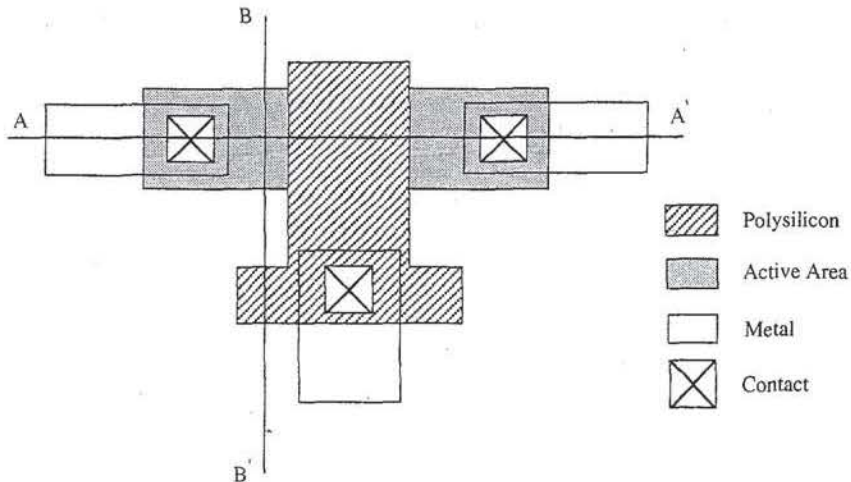


Figure P5.3

- 5.4** Consider a resistive-load inverter circuit with a $100 \text{ k}\Omega$ load resistor, where the input terminal (gate terminal of the nMOS transistor) is connected to its output (drain terminal of the nMOS transistor).

- (a) Sketch the load line for this circuit.
- (b) Is the transistor operating in the linear or saturation region?
- (c) For $V_T = 1\text{ V}$, $k' = 40\text{ }\mu\text{A/V}^2$ and $V_{OUT} = 2.5\text{ V}$, solve for W/L .

5.5 Refer to the CMOS fabrication process described in Chapter 2. Draw cross-sections of the following device along the lines A-A' and B-B'.



5.6 Design a resistive-load inverter with $R = 1\text{ k}\Omega$ such that $V_{OL} = 0.6\text{ V}$ when the enhancement-type nMOS driver transistor has the following parameters:

$$\begin{aligned} V_{DD} &= 5.0\text{ V} \\ V_{T0} &= 1.0\text{ V} \\ \gamma &= 0.2\text{ V}^{1/2} \\ \lambda &= 0.0\text{ V}^{-1} \\ k' &= 22.0\text{ }\mu\text{A/V}^2 \end{aligned}$$

- (a) Determine the required aspect ratio, W/L .
- (b) Determine V_{IL} and V_{IH} .
- (c) Determine noise margins NM_L and NM_H .

5.7 Layout of the resistive-load inverter design.

- (a) Draw the layout of the R-load inverter designed in exercise problem (5.6) using a polysilicon resistor with sheet resistivity of $25\text{ }\Omega/\text{square}$.

and the minimum feature size of $2\text{ }\mu\text{m}$. It should be noted that L stands for the effective channel length which is related to the mask channel length as $L = L_M + \delta - 2L_D$, where we assume δ (process error) = 0 and $L_D = 0.25\text{ }\mu\text{m}$. To save chip area, one should use the minimum sizes for L and W . Also, the resistor area can be reduced by using the folded layout (snake pattern) of the resistor.

- (b) Perform circuit extraction to obtain the SPICE input list from the layout.
- (c) Run the SPICE simulation of the circuit to obtain the DC voltage transfer characteristic (VTC) curve. Plot the VTC and check whether the calculated values in Problem 5.6 match with the SPICE results.

5.8 The nMOS and pMOS transistors in a CMOS inverter have the following parameters:

$$|V_{T0}| = 1.0\text{ V for both nMOS and pMOS transistors}$$

$$\lambda = 0.0\text{ V}^{-1}$$

$$k'_n = 50.0\text{ }\mu\text{A/V}^2$$

$$k'_p = 20.0\text{ }\mu\text{A/V}^2$$

The CMOS inverter is designed with $(W/L)_p = 20$ and $(W/L)_n = 10$, and its capacitive load is 2 pF . It is assumed that the load capacitance includes all parasitic capacitances connected to the drain node.

- (a) Calculate the average power dissipation in the inverter when its input signal is a rectangular pulse with 100 ns period which swings between 5 V and 0 V .
- (b) Repeat part (a) for the case when each transistor channel width is exactly twice as that used in (a), but the load capacitance and input signal remain the same.
- (c) What observations can you make from the results of part (b)? Can you explain the results?
- (d) Verify your answer using the power meter with SPICE simulation. For SPICE simulation, you can set the parasitic capacitances in drain and source regions to zero by setting AD, AS, PD, PS to zero.