

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TOSHIBA CORPORATION
Petitioner

v.

INTELLECTUAL VENTURES I LLC
Patent Owner

Case No. IPR2014-00113
Patent 6,058,045

PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE

Mail Stop "Patent Board"
Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandra, VA 22313-1450

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I. INTRODUCTION

The two challenged claims in this *inter partes* review (claims 1 and 4 of the U.S. Patent 6,058,045 -- “the ’045 Patent”) recite array configuration limitations as well as voltage limitations as applied to the claimed array configuration. Patent Owner’s Response does not dispute that U.S. Patent 5,297,029 to Nakai et al. (“**Nakai**”) anticipates the array configuration limitations of challenged claims 1 and 4. Moreover, other than an unsupported footnote, the Patent Owner’s Response does not dispute that Nakai anticipates the voltage limitations of challenged claims 1 and 4 according to the claim constructions proposed by Petitioner and adopted by the Board. Rather, Patent Owner’s sole defense is that Nakai is distinguishable based upon a limitation (the “logic high voltage” cannot exceed the power supply voltage V_{cc}) that is not recited in the challenged claims. In fact, this upper limit on the logic high voltage it is not even disclosed in the specification. Yet, the Patent Owner did not file a motion to amend its patent to add this new limitation. Rather, Patent Owner attempts to re-write the challenged claims under the pretense of claim construction.

Patent Owner’s attempt to use claim construction to rewrite its patent must fail. Neither Patent Owner, nor its experts, applied the proper “broadest reasonable construction” standard in advocating its proposed construction of “logic high voltage.” Moreover, there is no merit to Patent Owner’s arguments that the claims

should be rewritten as proposed. The issue of validity in this case is simple: without reading into the claims a new limitation not previously recited in the claims or disclosed in the specification, it is clear and undisputed that both challenged claims of the '045 patent are anticipated and rendered invalid by Nakai.

II. ARGUMENT

A. Patent Owner Does Not Meaningfully Dispute Challenged Claims Are Invalid Under Petitioner's Proposed Constructions

It is essentially undisputed that the challenged claims are anticipated and invalid under the claim constructions proposed by Petitioner and adopted by the Board. The Patent Owner's only argument of validity under Petitioner's claim constructions is:

- A single footnote that reads in its entirety:

“Indeed, even if the Board does not alter its ambiguous preliminary claim construction, Nakai still does not anticipate. As shown, when the Board's construction is actually applied to Nakai and to the '045 patent, the upper boundary for “logic high voltage” becomes Vcc (instead of the indefinite “such as Vcc”).”

(Response, at 22.)
- Three sentences in Mr. Berg's declaration stating nothing more than that Vcc would be the upper bound of logic high voltage, and one of skill would understand this. (Berg Decl. ¶ 29-30.)

Patent Owner and its expert provides no serious explanation or argument to support this allegation, and it makes no sense. The preliminary construction for “logic high voltage” is “a positive voltage higher than the logic low voltage, such as Vcc.” This construction does not establish Vcc as an upper boundary. Nor does the construction of “boosted positive voltage,” which does not even refer to Vcc. Therefore, Patent Owner’s footnote is unsupported, nonsensical and should be summarily dismissed.

Should the Board maintain the constructions it has adopted, there is no real dispute that the challenged claims are invalid over the Nakai reference.

B. Patent Owner’s Challenge to Petitioner’s Expert Has No Merit

Patent Owner argues that Petitioner’s expert, Mr. Murphy, is not qualified to opine on the technology of the ’045 patent because he is not one of ordinary skill in the art in the field of NAND flash memory or even flash memory generally. (Response at 8-10.) This argument has no merit and is disingenuous.

Patent Owner first argues that that Mr. Murphy lacks the requisite level of skill in the art for the ’045 patent (i.e. is not one of ordinary skill in the art) if that requires three year’s work experience in the field of “NAND flash memory.” (Response at 8-9.) Yet, Patent Owner’s own experts have opined that one skilled in the art for the ’045 patent would have “at least 3 years of academic or industry experience with *flash memory*,” not NAND flash memory as alleged by Patent

Owner. (IV-2001, at ¶17; IV-2002, at ¶19.) Moreover, Patent Owner admits that “flash memory cells and NAND flash memory cells are the relevant art.”

(Response, at 8.) Therefore, by Patent Owner's own admission, and those of its experts, there is no basis to require the level of skill in the art to include experience with “NAND flash memory” as opposed to “flash memory.”

Patent Owner next argues that Mr. Murphy lacks the requisite experience in the field of flash memory, citing to a question/answer from Mr. Murphy's cross examination which appears to suggest that he does not have three years of work experience in the field of flash memory. (Response at 9-10.) Here, Patent Owner disingenuously misleads the Board. What Patent Owner fails to tell the Board is that the quoted answer as understood by Mr. Murphy was limited to stand alone flash memory devices. (See IV-2003, Murphy Depo. Transcript, 113:2-13.) However, when the question was clarified to refer to flash memory in general, as contemplated by the '045 patent, Mr. Murphy testified his experience more than met Patent Owner's proposed definition of ordinary skill in the art of flash memory. (Id. at 114:11-117:6, and 118:9-119:3.) Mr. Murphy explained in his deposition that he developed electrically erasable CMOS chips using arrays of flash cells. (Id. at 20:18-22:17)

Therefore, Patent Owner's challenge to the qualifications of Petitioner's expert has not merit.

C. Patent Owner Proposes An Alternate Construction For Only One Claim Term

The following are the Petitioner's proposed claim constructions:

Claim Term	Petitioner's Proposed Construction (Petition, at 9-12.)
logic low voltage	a low voltage, such as ground or Vss
logic high voltage	a positive voltage higher than <u>the</u> logic low voltage, such as Vcc
boosted positive voltage	a positive voltage higher than <u>the</u> logic high voltage
selected bit line	the bit line connected to the column of memory cells containing the memory cell to be operated on
unselected bit lines	the bit lines connected to the columns of memory cells not containing the memory cell to be operated on
selected word line	the word line connected to the row of memory cells containing the memory cell to be operated on
unselected word lines	the word lines connected to the rows of memory cells not containing the memory cell to be operated on

The Board adopted these constructions (but without the word “the” underlined above.). (Decision, at 7-9). While the Patent Owner generally alleges these constructions are imprecise, it only specifically challenges and provides an alternate construction for just one claim term: “logic high voltage.” (Response, at 10-12.) The Patent Owner's proposed construction for “logic high voltage” is “a positive voltage higher than logic low voltage **and less than or equal to the nominal value for Vcc.**” (Response at 12.) This proposed construction is identical to the construction adopted by the Board, except it adds the highlighted/underlined text above. As set forth below, the added phrase is not the broadest reasonable

construction for “logic high voltage,” and there is no basis to read this limitation into the claims.

D. Patent Owner Fails to Apply Proper Standard of Claim Construction

In *inter partes* review, “[A] claim in an unexpired patent shall be given its broadest reasonable construction in light of the specification of the patent in which it appears.” (37 C.F.R 42.100(b).) Patent Owner’s Response never applies this standard in arguing the construction for “logic high voltage.” In fact, the Patent Owner’s response never even acknowledges the “broadest reasonable construction” standard. Instead, the Patent Owner’s standard for construing this claim term is to provide a “clear demarcation between a ‘logic high voltage’ and a ‘boosted positive voltage’.” (Response at 11.) This is the wrong standard for claim construction in *inter partes* review. Not once does Patent Owner allege, let alone establish, that the “clear demarcation” its proposed construction allegedly provides is the broadest reasonable construction for this claim term. Therefore, all of Patent Owner’s arguments regarding the construction of “logic high voltage” should be summarily dismissed.

Likewise, Patent Owner’s first expert, Mr. Morales, opines that, while Vcc is given as an example of the “logic high voltage” (IV-2001, at ¶21), one skilled in the art would understand that the “logic high voltage” would be nominally equal to

or lower than Vcc. (IV-2001, at ¶32.) Mr. Morales states that Vcc provides “a practical dividing line” between a “logic high voltage” and the higher “boosted positive voltage” (IV-2001, at ¶31), and that Vcc is the only “reasonable and principled boundary” between the terms. (IV-2001, at ¶39.) However, the applicable claim construction standard is “broadest reasonable construction,” not “practical dividing lines” or “reasonable and principled boundaries.” Therefore, because Mr. Morales failed to apply the proper standard for claim construction, all of his opinions on claim construction should be given no weight.

Finally, Patent Owner's second expert, Mr. Berg, opines that the Board's preliminary construction of “logic high voltage” is imprecise because it fails to provide “a clear demarcation between the range of ‘logic high voltage’ and the range of the third recited voltage – a ‘boosted positive voltage’.” (IV-2002, at ¶27.) Mr. Berg opines that “a more precise construction” would be “greater than logic low, and less than or equal to the nominal value of Vcc.” (IV-2002, at ¶28.) Again, the applicable claim construction standard is “broadest reasonable construction,” not “clear demarcation” or “more precise construction.” Therefore,

because Mr. Berg failed to apply the proper standard for claim construction, all of his opinions on claim construction should be given no weight.¹

Patent Owner and its experts cleverly or negligently failed to propose and argue any claim constructions under the proper standard of “broadest reasonable construction.” In contrast, Petitioner and its expert did provide and support proposed claim constructions under the proper claim construction standard specified by 37 C.F.R 42.100(b). (Petition, at 8-13; TOSH-1006, at ¶¶13-20.) Therefore, the claim constructions proposed by Petitioner and adopted by the Board should stand.

E. The Limitation That “Logic High Voltage” Cannot Exceed Vcc Should Not Be Read Into The Claims

Patent Owner provides a number of arguments why the “logic high voltage” should be limited to Vcc or lower. None have any merit.

¹ A second reason to give Mr. Berg's opinion on the construction of “logic high voltage” no weight is because he gives a second contradictory construction for logic high voltage: “positive voltages extending from an upper specification of an external positive supply rail (i.e., Vcc) and down to a value above the trip point of a logic circuit.” (IV-2002, at ¶42.)

1. Claimed Voltages Can Only Be Construed Relative To Each Other

The terms “logic low voltage,” “logic high voltage” and “boosted positive voltage” are not defined or even used in the specification. While the specification does give numerical examples for these voltages, the specification does not provide numerical limits on these voltages. Therefore, the broadest reasonable constructions for these claimed voltages are their values relative to each other. (Petition, at 9-11; TOSH-1006, at ¶¶16-18.)

Patent owner criticizes Petitioner's proposed constructions of logic low, logic high and boosted positive voltages, saying that defining them only relative to each other makes it “impossible to determine where one begins and the other ends.” (Response at 10.) This is untrue. Under the preliminary constructions, logic low ends before logic high begins, and logic high ends before boosted positive begins. It makes no sense to pick arbitrary numerical voltages, without support in the intrinsic record, merely for the sake of a having “a more precise construction.”

Patent owner argues there is no clear demarcation between a “logic high voltage” and “a boosted positive voltage” because if two or more voltages are applied to BSL, BL1 and WL0 during programming, it is impossible to tell which is a “logic high voltage” and which is a “boosted positive voltage.” (Response, at

10-11). Patent Owner's argument misses the mark for many reasons. First, if multiple different logic high voltages are applied, the challenged claims as properly construed simply require the boosted positive voltage to be greater than the logic high voltages (plural). No other limitations on these voltages were recited in the claims or described in the specification. Second, there actually is a clear demarcation between the claimed voltages: logic high must be greater than logic low, and less than boosted positive. This is admitted by Patent Owner's own equation describing the preliminary constructions: "logic low" < "logic high" < "boosted positive". (Response at 11.) Third, placing an arbitrary numerical upper limit on the logic high voltage does not solve Patent Owner's alleged concern, as the same alleged dilemma will exist under its construction if all the voltages are below Vcc. Fourth, Patent Owner does not propose placing a similar numerical upper limit on "logic low" to differentiate it from "logic high." This alone shows that Patent Owner's proposed upper limit on "logic high" is arbitrary (i.e. Patent Owner arbitrarily proposes adding a numerical upper limit to "logic high," without proposing any similar numerical upper limit on "logic low").

2. There Is No Intrinsic Support For Adding A Numerical Limit of Vcc to "Logic High Voltage"

Patent owner argues that one of ordinary skill in the art would understand that a "logic high voltage" would be less than or equal to the nominal value of the

memory array's power supply, or what one of skill in the art would recognize as "Vcc," and therefore a proper construction of "logic high voltage" is "a positive voltage higher than logic low voltage **and less than or equal to the nominal value for Vcc.**" (Response, at 12). This argument has no merit for numerous reasons:

First, the claims recite no numerical limits on any of the voltages. Clearly the intent of the inventor at the time was not to limit the claims to any numerical values by instead using terms such a logic low, logic high and boosted positive as opposed to actual voltage values. Had the inventor wanted to limit the claims to any specific numerical values, he could have originally included those numerical limitations in the claims. He specifically chose not to.

Second, no numerical limits are disclosed in the specification for dividing lines among logic low, logic high, and boosted positive voltages, let alone a Vcc upper limit on just the logic high voltage. In fact, there isn't even a numerical example of Vcc in the specification, nor any disclosure or description of a power supply for generating Vcc.

Third, the specification directly contradicts Patent Owner's proposed construction. When describing the erase operation, the specification states that a voltage of "about Vcc" is applied to bit line select control line BSL. (TOSH-1001, at 6:53-55.) The plain meaning of "about Vcc" contemplates voltages slightly above and below Vcc. Yet, claims 2 and 5 recite, during erase, applying a "logic

high voltage” to the bit line select control line. (Id, at 9:2-3 and 10:16-17.)

Therefore, the specification clearly discloses that the logic high voltage can exceed Vcc. Moreover, the specification states that during erase, the voltage applied to the selected bit line “can be as low as Vcc,” which contemplates this voltage can exceed Vcc. Id, at 6:60-65. Yet, claims 2 and 5 recite, during erase, applying a “logic high voltage” to the selected bit line. Id, at 9:6 and 10:21. Therefore, the specification expressly teaches that the logic high voltage can exceed Vcc, in direct contradiction to Patent Owner’s proposed construction of “logic high voltage.”

Fourth, the Patent Owner justifies the Vcc numerical limitation based upon the memory array’s power supply. Yet, the memory array’s power supply that supplies Vcc is not recited in the challenged claims. In fact, no such power supply is disclosed or described in the specification. Further, the claims do not recite the source(s) of the claimed voltages, or place any limitations on where the voltages can originate (external versus internal, single supply versus multiple supplies, etc.). In fact, there is no limitation in the claims that requires any of the voltages to be Vcc or derived from a power supply that supplies Vcc. Finally, as admitted by Mr. Berg, the nominal value of Vcc is dictated by the power supply to the flash memory chip. (IV-2002, at ¶28.) However, he also admits that the power supplies providing Vss and Vcc are external to the flash memory chip. (IV-2002, at ¶¶ 22-23, 49, 52-53.) Therefore, the absurdity of Patent Owner’s construction is that the

scope of the claims would depend upon an unclaimed voltage, from an unclaimed power supply, that is separate from the claimed memory array device.

Fifth, Patent Owner's proposed claim construction would render claim 1 invalid as indefinite. Claim 1 is directed to an array of flash memory cells. The claim does not recite any power supplies, and as stated above, such power supplies are external to flash memory cell devices. Therefore, the scope of claim 1 under Patent Owner's proposed construction would depend upon an unclaimed, variable object: the external power supply that supplies Vcc. There is no industry standard for Vcc, nor for power supplies used to provide Vcc when connected to flash memory devices. Therefore, one skilled in the art could not determine what is covered by claim 1. (See *Ex parte Brummer*, 12 USPTQ2d 1653 (Bd. Pat. App. & Int. 1989) (reference to height of rider "that the bicycle was designed for" rendered the claim indefinite.))

3. Patent Owner's Alleged Advantages Do Not Necessarily Result From Its Claim Construction.

Patent Owner argues the claimed invention is advantageous over Nakai's programming scheme because it results in improved reliability, reduced power consumption, and could also reduce the need for multiple charge pumps. (Response, at 22.) However, none of the argued advantages necessarily result from Patent Owner's construction of "logic high voltage." Specifically, Patent Owner

argues that its construction means the source and drain regions of the transistor **can have** the same diffusion construction. (Response, at 23.) Yet, the claims are not directed to the memory cell components, Patent Owner's construction does not require such diffusion construction, and Petitioner's construction for logic high does not preclude such diffusion construction. Patent owner further argues that the claimed invention could reduce chip space and complexity because it avoids on-chip charge pumps and other circuits. Yet, the claims do not recite any such voltage sources, and place no limitations on where the voltages originate. Because any number of charge pumps can be used to generate any of the voltages in the challenged claims even under Patent Owner's construction for logic high voltage, none of these advantages necessarily result from its construction.

4. Patent Owner's Attempt To Rewrite Claims With New Limitations Is An End Run Around A Motion To Amend, And Is Not Claim Construction

Patent Owner argues for a clearer demarcation and a more principled and precise dividing line between the claimed logic high and boosted positive voltages. (Response, at 11 and 13.) Yet, the inventor had ample opportunity to do this at any time during the original prosecution of the '045 patent. Had the inventor intended to place an upper numerical limit of V_{cc} on the claims, he could have done so. But instead, he chose a more broad dividing line, so his claims were not limited to just those devices using V_{cc} or lower for the logic high voltages.

Now that Patent Owner has been confronted with the Nakai reference, it attempts to rewrite the claims with a new numerical limitation in an attempt to save its patent. Patent Owner chose not to file a motion to amend in this proceeding, likely because doing so would confer upon Petitioner intervening rights in the co-pending litigation, and it would have provided the Petitioner the opportunity to respond with new grounds of invalidity for the amended claims (including arguing the amended claims are obvious over Nakai and/or relying on additional prior art). Instead, Patent Owner is doing an end run around a motion to amend, and attempts to amend the claims under the pretext of claim construction. This is improper, and contrary to the PTAB rules and regulations.

III. CONCLUSION

It is requested that the Board maintain the adopted constructions, and find claims 1 and 4 of the '045 patent invalid as being anticipated by Nakai.

Respectfully submitted,

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/Alan A. Limbach/

Alan A. Limbach
Registration No. 39,749

DLA PIPER LLP (US)
2000 University Avenue
East Palo Alto, CA 94303-2215
Telephone: 650.833.2433
Facsimile: 650.687.1182

CERTIFICATE OF SERVICE

The undersigned certifies that a true copy of the foregoing **PETITIONER'S
REPLY TO PATENT OWNER'S RESPONSE** was served electronically via e-mail on September 11, 2014, in its entirety on the following:

Robert Greene Sterne, Esq.
Email: rsterne-PTAB@skgf.com

Jon E. Wright, Esq.
Email: jwright-PTAB@skgf.com

Donald J. Coulman, Esq.
Email: dcoulman@intven.com

Andrew G. Heinz, Esq.
Email: aheinz@desmaraisllp.com

Raymond J. Werner, Esq.
Email: rwerner-PTAB@skgf.com

Christian A. Camarce, Esq.
Email: ccamarce-PTAB@skgf.com

Dated: September 11, 2014

/Alan A. Limbach/

Alan A. Limbach
Registration No. 39,749

DLA PIPER LLP (US)
2000 University Avenue
East Palo Alto, CA 94303-2215
Telephone: 650.833.2433
Facsimile: 650.687.1182