

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TOSHIBA CORPORATION
Petitioner

v.

INTELLECTUAL VENTURES I LLC
Patent Owner

Case IPR2014-00113
Patent 6,058,045

**PATENT OWNER INTELLECTUAL VENTURES I LLC'S
DEMONSTRATIVE EXHIBITS**

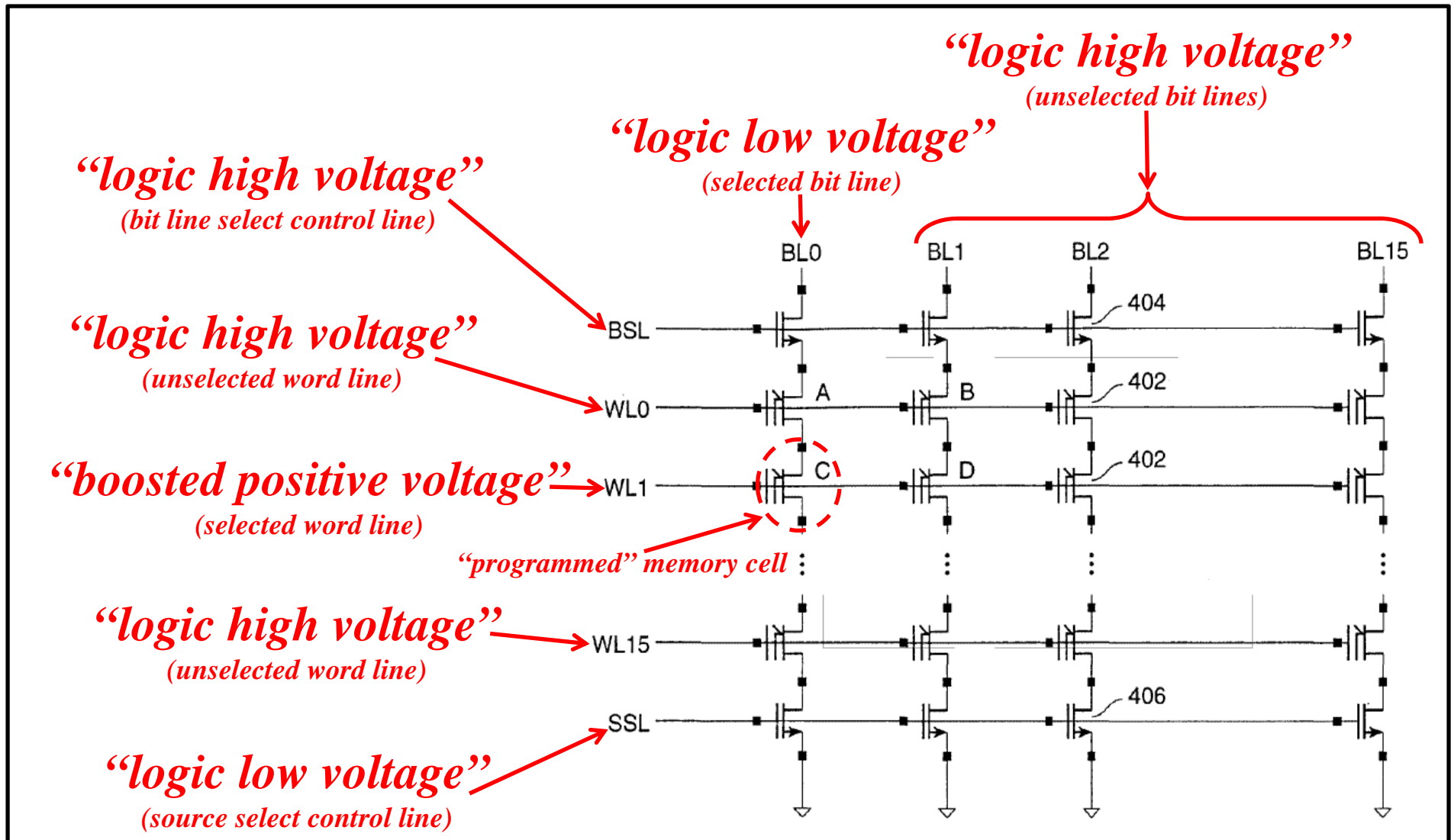
Toshiba Corporation
v.
Intellectual Ventures I LLC

IPR2014-00113
Patent 6,058,045

Demonstratives of Patent Owner
Intellectual Ventures I LLC

Hearing: November 6, 2014

'045 Patent – Programming



(Paper 20, PO Response, p. 6.)

'045 Patent – Programming

Programming operation:

The programming operation is done by applying a high voltage (e.g., 15 to 20 V) on the selected word line (WL1) and grounding the selected bit line (BL0), while the unselected bit lines (BL1–BL15) are at Vcc. Referring to FIG. 4, to program memory cell 402-C, a high voltage of for example 15 to 20 volts is applied to WL1. Vcc is applied to BSL control line and WL0 to couple BL0 to the drain terminal of memory cell 402-C. With BL0 grounded, the drain terminal of cell 402-C receives ground potential. Control line SSL remains at VSS and unselected word lines WL2–WL15 receive VCC. Thus, the cells are programmed serially in a NAND type structure by passing Vss to the selected cells as the pass (unselected) word lines are pulled up to pass Vss.

(Ex. 1001, '045 Patent, 7:26-40.)

'045 Patent Claim 1

1. An array of flash memory cells comprising:

- a plurality of columns of serially connected flash memory cells, each memory cell having a gate terminal;
- a plurality of bit lines respectively coupled to drain side of said plurality of columns of memory cells via a respective plurality of bit line select transistors, said plurality of bit line select transistors having gate terminals coupled to a bit line select control line;
- a plurality of word lines, each one coupling to a gate terminal of one memory cell in each of said plurality of columns to form rows of memory cells with common gate terminals; and
- a plurality of source select transistors respectively coupling a source side of said plurality of columns of memory cells to a logic low voltage, and having gate terminals coupled to a source select control line,

wherein, during programming:

- a logic high voltage is applied to said bit line select control line to turn on bit line select transistors,
- a logic low voltage is applied to source select control line to turn off source select transistors;
- a logic low voltage is applied to a selected bit line while a logic high voltage is applied to unselected bit lines, and
- a logic high voltage is applied to unselected word lines, while a boosted positive voltage is applied to a selected word line.

(Ex. 1001, '045 Patent, claim 1.)

'045 Patent Claim 4

4. A method of operating a flash memory device wherein programming memory cells is accomplished by the steps of:
applying a logic high voltage to a bit line select control line to turn on bit line select transistors,
applying a logic low voltage to a source select control line to turn off source select transistors;
applying a logic low voltage to a selected bit line while a logic high voltage is applied to unselected bit lines, and
applying a logic high voltage to unselected word lines, while a boosted positive voltage is applied to a selected word line.

(Ex. 1001, '045 Patent, claim 4.)

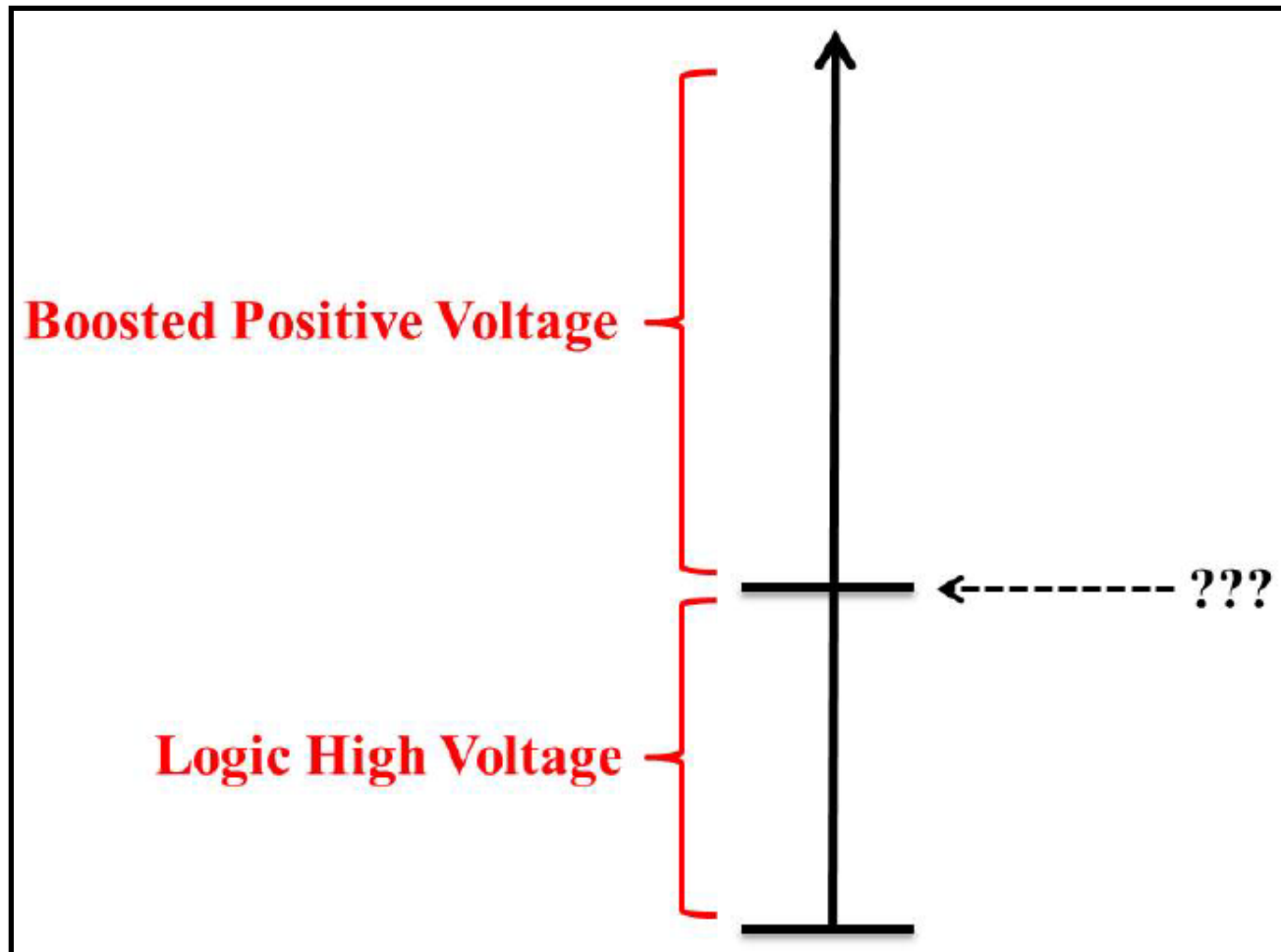
Board's Preliminary Construction for “Logic High Voltage”

2. “logic high voltage” (claims 1 and 4)

We agree with Petitioner that logic high voltage means “a positive voltage higher than logic low voltage, such as Vcc.” Pet. 10. The term “logic high voltage” is used only in the claims of the '045 patent. Petitioner's proposed construction is consistent with the specification that states voltage Vcc is applied to bit select control line (BSL), the unselected bit line, and the unselected word line during programming. *Id.* at 6:37-45; 7:26-40; Ex. 1006 ¶ 17. Thus, on this record, we are persuaded that “logic high voltage” is construed as a positive voltage higher than logic low voltage, such as Vcc.

(Paper 13, Decision, p. 8.)

Board's Preliminary Construction for "Logic High Voltage"



(Paper 20, PO Response, p. 11.)

Patent Owner's Construction for "Logic High Voltage"

ordinary skill in the art reading the '045 patent. One of ordinary skill in the art would understand that a "logic high voltage" would be less than or equal to the nominal value of the memory array's power supply, or what one of skill in the art would recognize as "Vcc." (See Morales Dec., ¶¶ 25-33 and 39; see Berg Dec., ¶¶ 27-32.) So a proper construction of "logic high voltage" is "a positive voltage higher than logic low voltage *and less than or equal to the nominal value for Vcc.*" (See *id.*)

(Paper 20, PO Response, p. 12.)

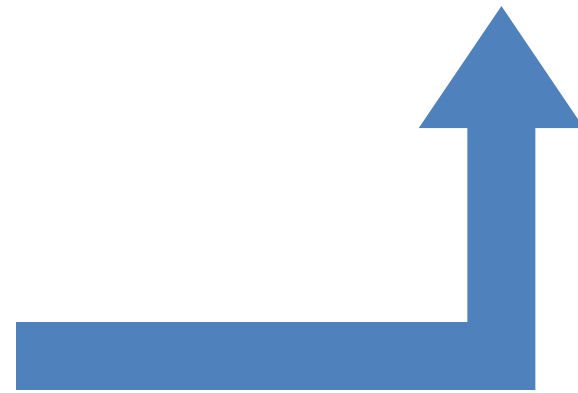
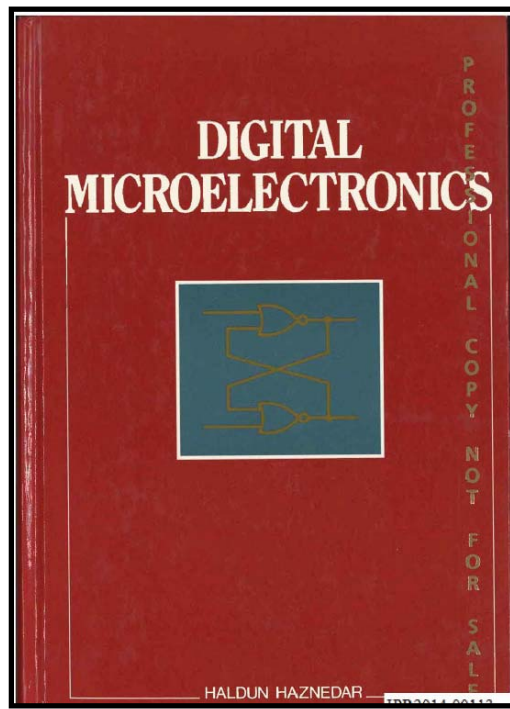
'045 Patent Specification Sets Upper Limit of “Logic High Voltage” at Vcc

TABLE I				
Control Line	Erase	Program	Read	Condition
BSL	Vcc	<u>Vcc</u>	Vcc	Selected
SSL	Vss	Vss	Vcc	Selected
BLO	Vcc	Vss	1.0–1.4V	Selected
BL1	Vss	<u>Vcc</u>	0.5V	Unselected
WL0	Vcc	<u>Vcc</u>	Vcc	Unselected
WL1	–12 to –15V	15–20V	Vss	Selected

(Ex. 1001, '045 Patent, col. 6. See *also* PO Response, p. 13.)

Extrinsic Evidence Supports Patent Owner's Construction for "Logic High Voltage"

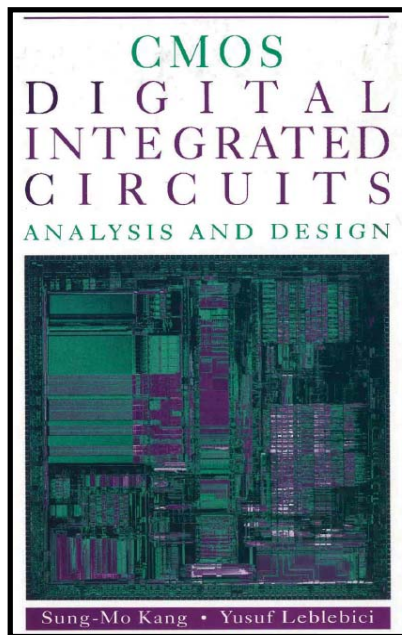
circuits. Typically, the *logical states* are described by two nominal voltage levels, the higher of which, corresponding to the power *supply* voltage, V_{CC} , represents **1** in *positive logic* while the *ground* (i.e., 0 V) represents **0**. However, as stated before,



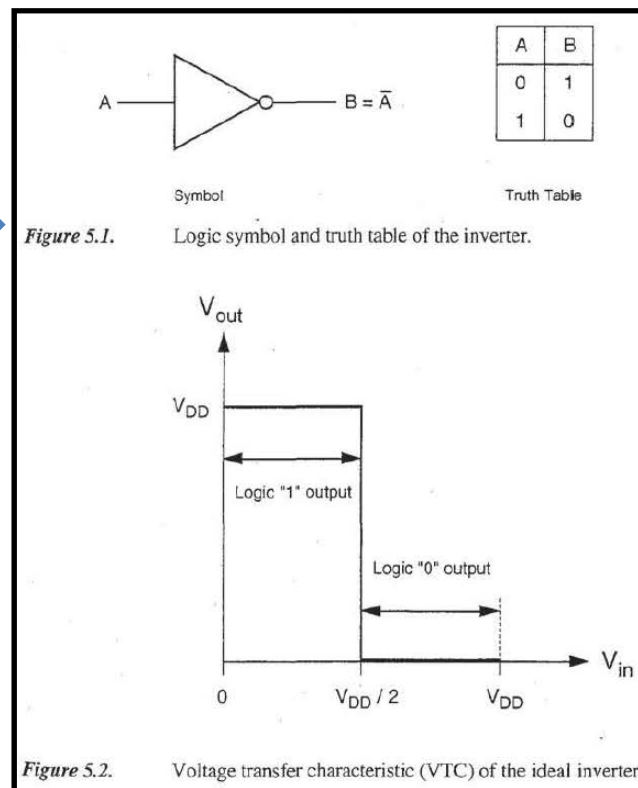
(Ex. 2013, 1991 Haznedar Textbook, p. 2 cited in Ex. 2001, Morales Dec., ¶ 29. See *also* Paper 20, PO Response, p. 12.)

Extrinsic Evidence Supports Patent Owner's Construction for "Logic High Voltage"

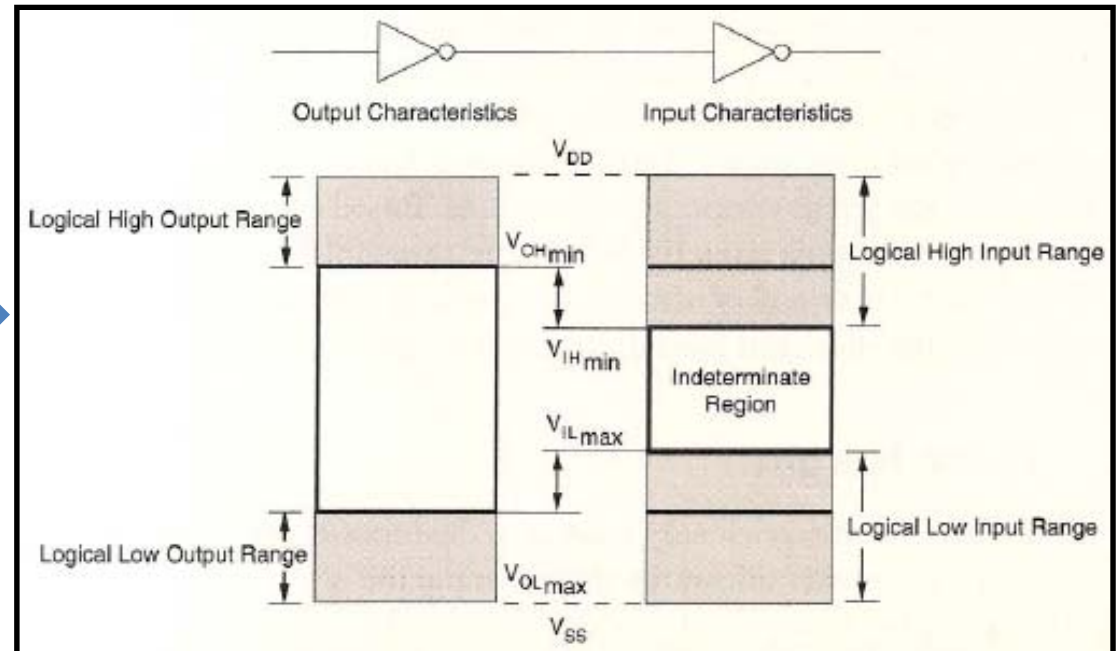
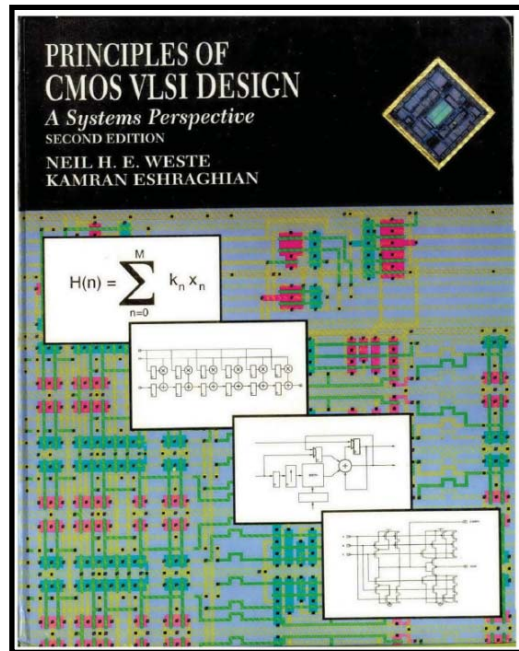
The logic symbol and the truth table of the ideal inverter are shown in Fig. 5.1. In MOS inverter circuits, both the input variable A and the output variable B are represented by node voltages, referenced to the ground potential. Using positive logic convention, the Boolean (or logic) value of "1" can be represented by a high voltage of V_{DD} , and the Boolean (or logic) value of "0" can be represented by a low voltage of 0. The DC voltage transfer characteristic (VTC) of the ideal inverter circuit is shown in Fig. 5.2.



(Ex. 2012, 1996 Kang Textbook, pp. 134-135 cited in Ex. 2001, Morales Dec., ¶ 29. See also Paper 20, PO Response, p. 12.)



Extrinsic Evidence Supports Patent Owner's Construction for "Logic High Voltage"



(Ex. 2005, 1993 Weste Textbook, p. 70 cited in Ex. 2002, Berg Dec., ¶ 39. See also Paper 20, PO Response, p. 13.)

V_{IHmin} = minimum HIGH input voltage
 V_{ILmax} = maximum LOW input voltage
 V_{OHmin} = minimum HIGH output voltage
 V_{OLmax} = maximum LOW output voltage.

'045 Patent Claim's "Logic High Voltage" Is Consistent with Extrinsic Evidence

Patent Owner's Expert, John E. Berg:

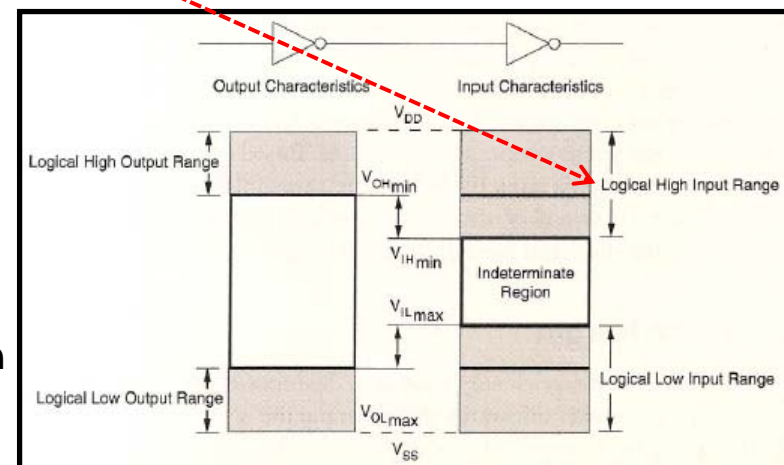
41. Similarly, this equivalency can be expressed in a table, which is shown below. Note the similarities in nomenclature (e.g., "logic high voltage" and logical high input voltage.) As Weste's book concerns itself with digital logic CMOS circuits, it can be ascertained that the '045 patent used terms that were consistent with the logic textbooks at the time

Table 1: Mapping Weste and the '045 terms

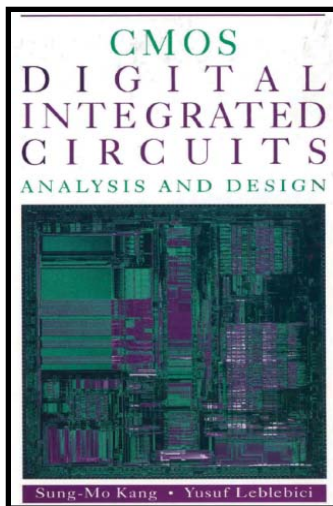
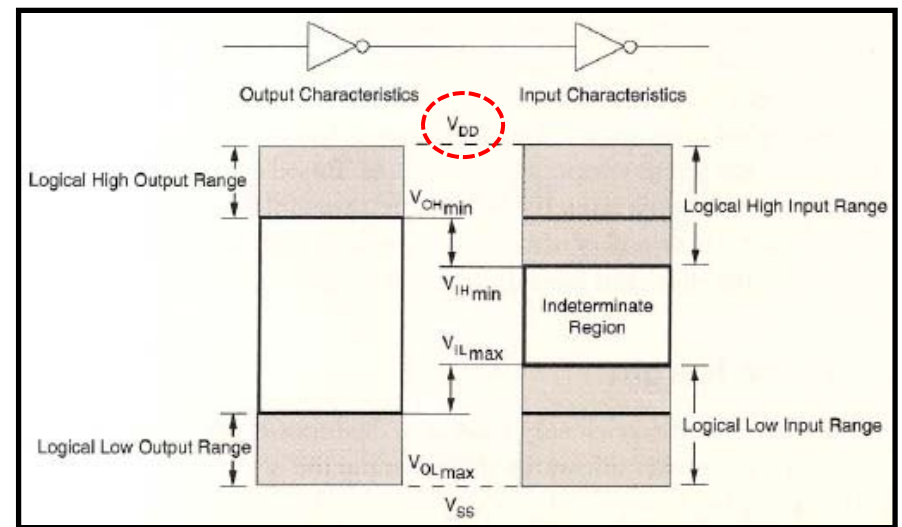
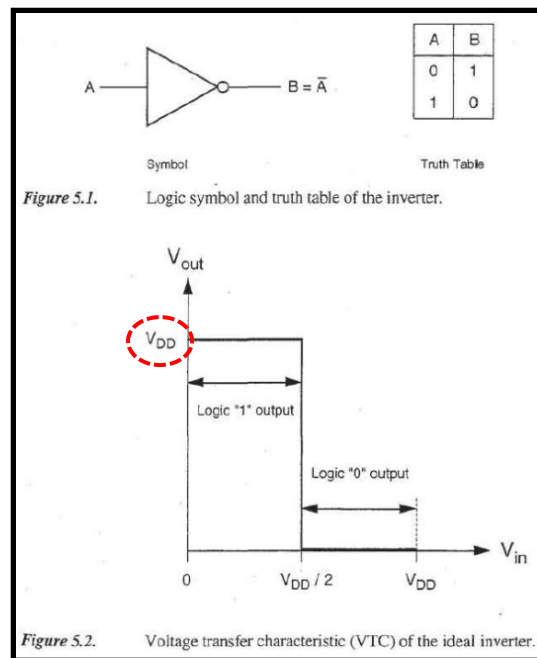
	'045 patent term	Weste term
Logic high power supply	Vcc	Vdd
Logic low power supply, Ground	Vss	Vss
Logic "1" voltage range	Logic High Voltage	Logical High Input Range
Logic "0" voltage range	Logic Low Voltage	Logical Low Input Range

(Ex. 2002, Berg Dec., ¶ 41. See also Paper 20, PO Response, p. 13.)

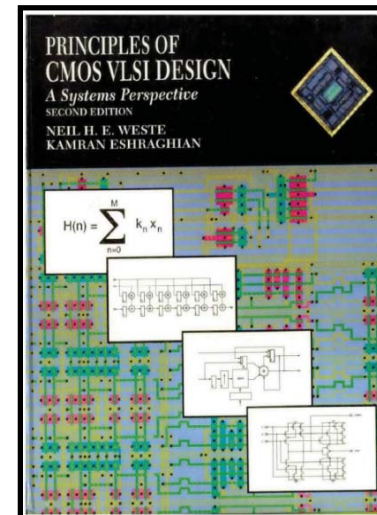
(Ex. 2005, 1993 Weste Textbook, p. 70 cited in Ex. 2002, Berg Dec., ¶ 39. See also Paper 20, PO Response, p. 13.)



Upper Limit of “Logic High Voltage” at V_{cc} Is Supported by Extrinsic Evidence

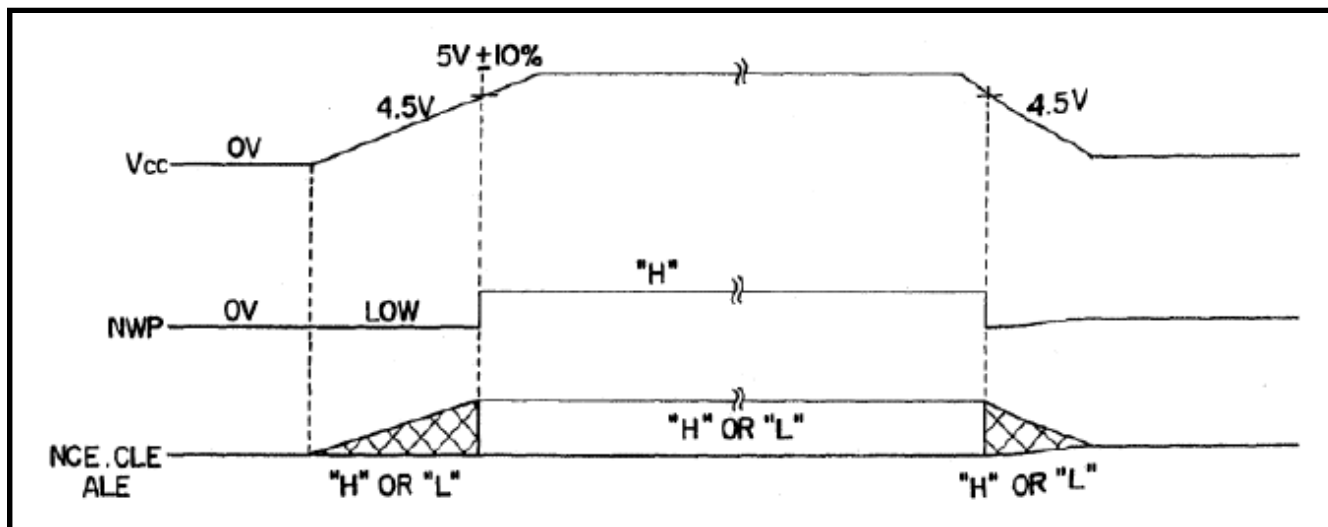


(Ex. 2012, 1996 Kang Textbook, p. 135 cited in Ex. 2001, Morales Dec., ¶ 29.)



(Ex. 2005, 1993 Weste Textbook, p. 70 cited in Ex. 2002, Berg Dec., ¶ 39.)

Upper Limit of “Logic High Voltage” at Vcc Is Supported by Nakai



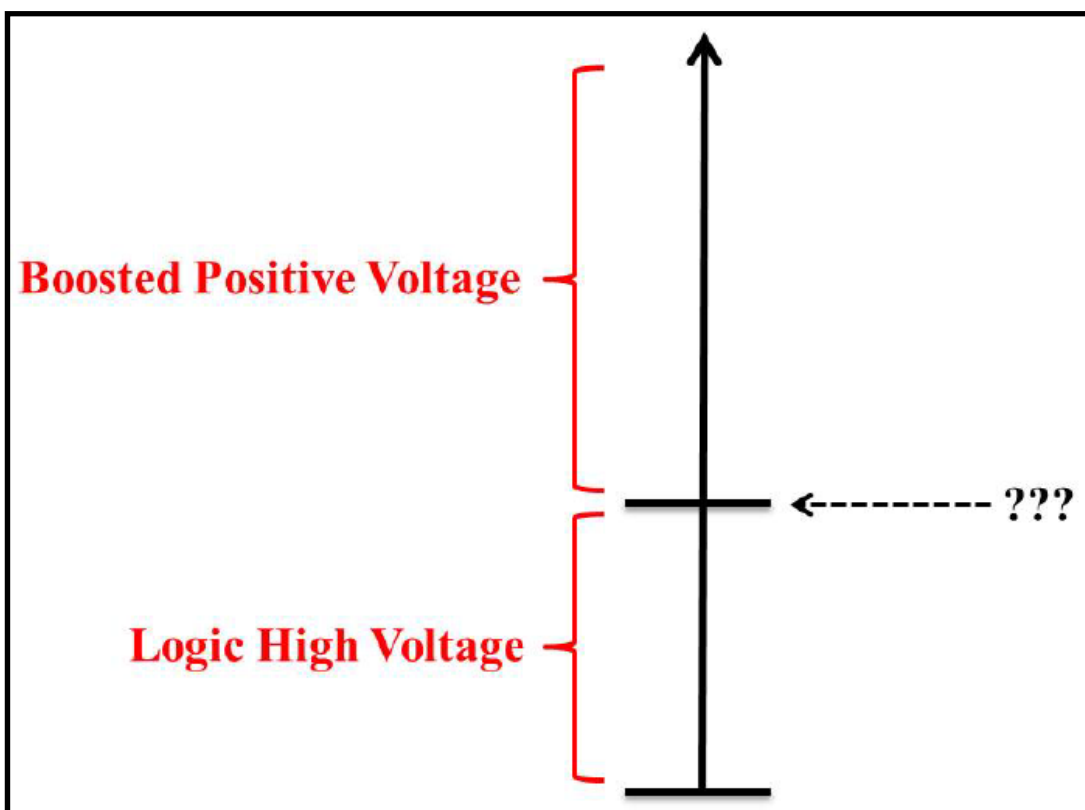
(Ex. 1005, Nakai, FIG. 20.)

Nakai's Vcc is its power-supply voltage and is the nominal voltage at which the logic circuits on Nakai's memory device produce a logic high voltage at their respective outputs. (See *id.*) Nakai's Vcc thus represents its “logic high voltage,” which is consistent with the construction proposed above. And voltages higher than the nominal power supply voltage Vcc are higher than a “logic high voltage.” (See *id.*, ¶ 34.) These other voltages are “boosted positive voltages.”

Board's Preliminary Construction for "Logic High Voltage" Does Not Clarify Claim Scope

during programming. *Id.* at 6:37-45; 7:26-40; Ex. 1006 ¶ 17. Thus, on this record, we are persuaded that "logic high voltage" is construed as a positive voltage higher than logic low voltage, such as V_{cc} .

(Paper 13, Decision, p. 8.)



(Paper 20, PO Response, p. 11.) 16

Board's Preliminary Construction for "Logic High Voltage" Does Not Clarify Claim Scope

Patent Owner's Expert, John E. Berg:

Logic High Voltage

27. The Board preliminarily construed "logic high voltage" as "a positive voltage higher than a logic low voltage, such as V_{cc} ." (Decision, p.8.) I do not agree with this construction. Standing alone, the Board's construction is imprecise because, it does not provide a clear demarcation between the range of "logic high voltage" and the range of the third recited voltage—a "boosted positive voltage."

28. A more precise construction would be to define the boundary between a "logic high voltage" and a "boosted positive voltage" as the nominal value of V_{cc} . That is, a "logic high voltage" would be greater than a logic low, and less than or equal to the nominal value of V_{cc} , i.e., the power supply to the flash memory chip.

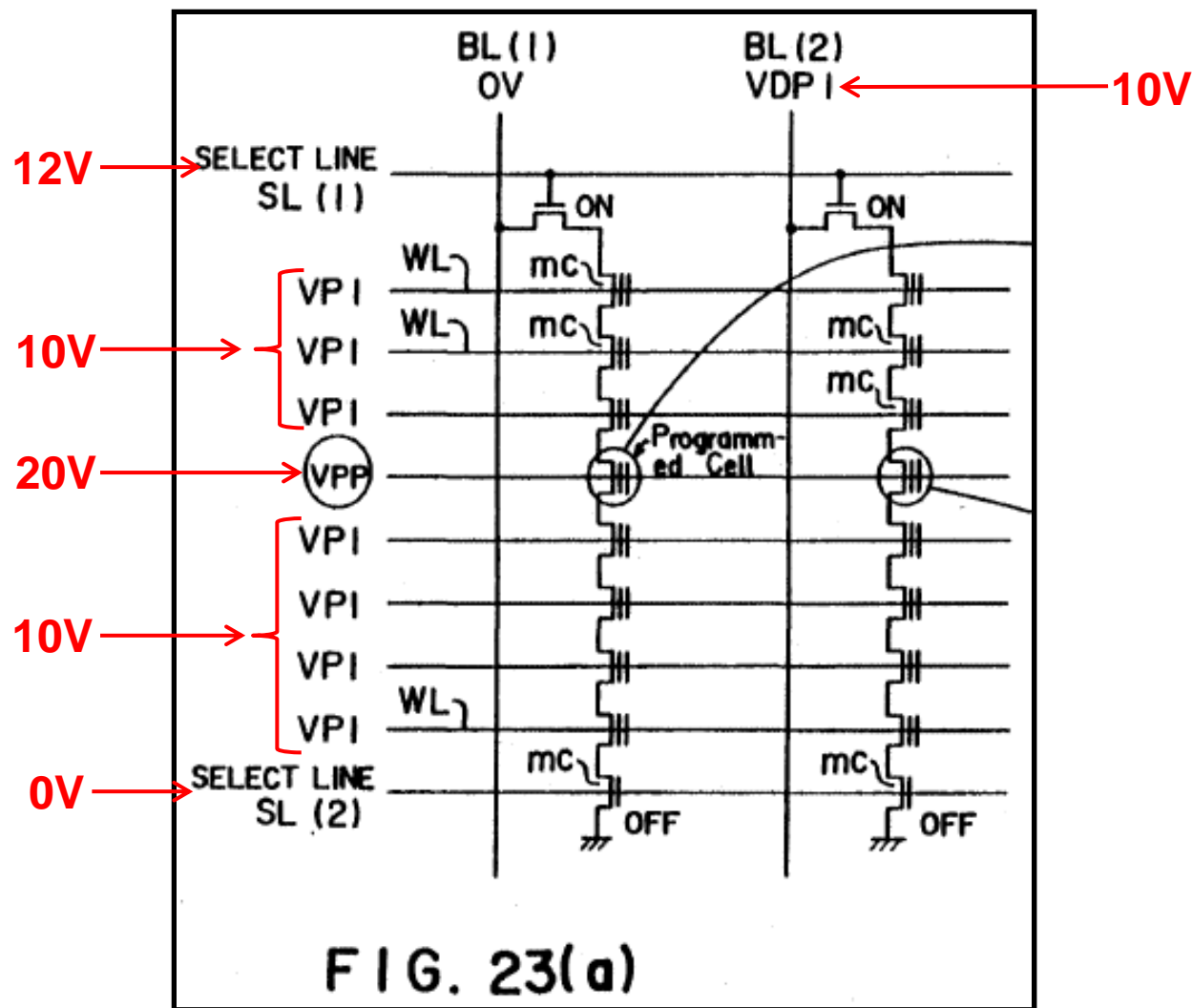
(Ex. 2002, Berg Dec., ¶¶ 27-28. See also Paper 20, PO Response, p. 12.)

Claimed Invention Confers Advantages over Nakai's Programming Scheme

C. Advantages of the Claimed Invention over Nakai's Programming Scheme

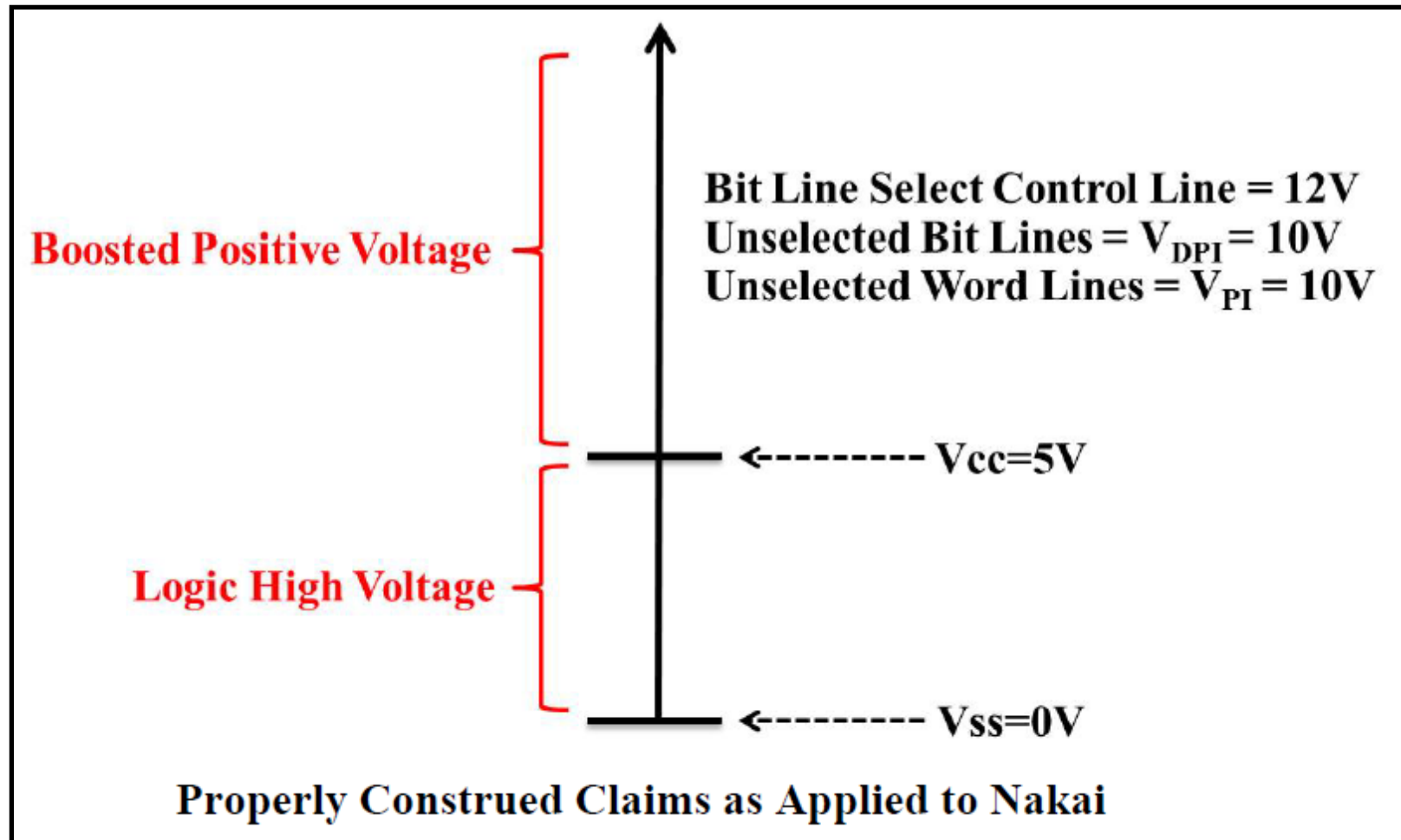
The difference between the two programming schemes is material. The '045 patent's programming scheme confers distinct advantages over Nakai's use of multiple boosted positive voltages. The advantages of avoiding Nakai's multiple boosted positive voltages include improved reliability of the memory array transistors and reduced power consumption. (*See* Ex. 2002, Berg Dec., ¶ 66.) And obviating the need for multiple different boosted positive voltages could also reduce the need for multiple charge pumps or other on-chip circuitry to boost voltages, which reduces overall chip footprint. (*See id.*) Each of these improvements is commercially important to flash memory manufacturers and their customers. (*See id.*, ¶¶ 45-54.)

Proper Construction for “Logic High Voltage” as Applied to Nakai



(Ex. 1005, Nakai, FIG. 23(a), annotated with voltages disclosed in Nakai, 1:46-2:9.)

Proper Construction for “Logic High Voltage” as Applied to Nakai



(Paper 20, PO Response, p. 20.)

Proper Construction for “Logic High Voltage” Is Consistent with Nakai

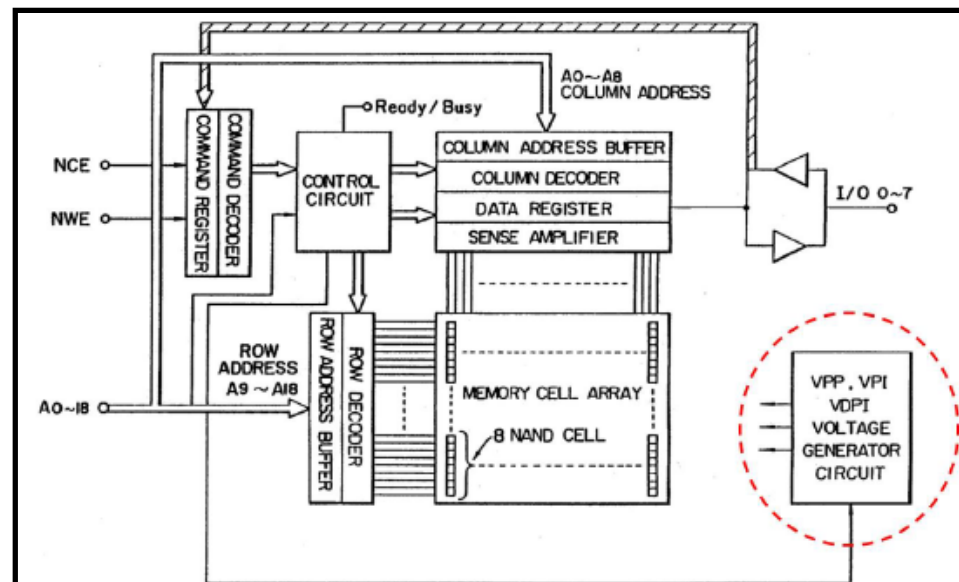


FIG. 26 of Nakai (Annotated)

As Nakai shows, V_{pp} , V_{PI} , and V_{DPI} are all on-chip generated voltages that are higher than Nakai's power supply V_{cc} —i.e., Nakai's logic high voltage. Such voltage generator circuits were well known during the timeframe of the Nakai patent. Since V_{cc} is the only identified power supply, one of ordinary skill in the art would understand that the voltage generator circuits of Nakai generate V_{pp} , V_{PI} , and V_{DPI} from V_{cc} . (See Ex. 2001, Morales Dec., ¶ 38; see Ex. 2002, Berg Dec., ¶¶ 45-54.)

Petitioner's Expert Did Not Consider the Value of Vcc in Nakai

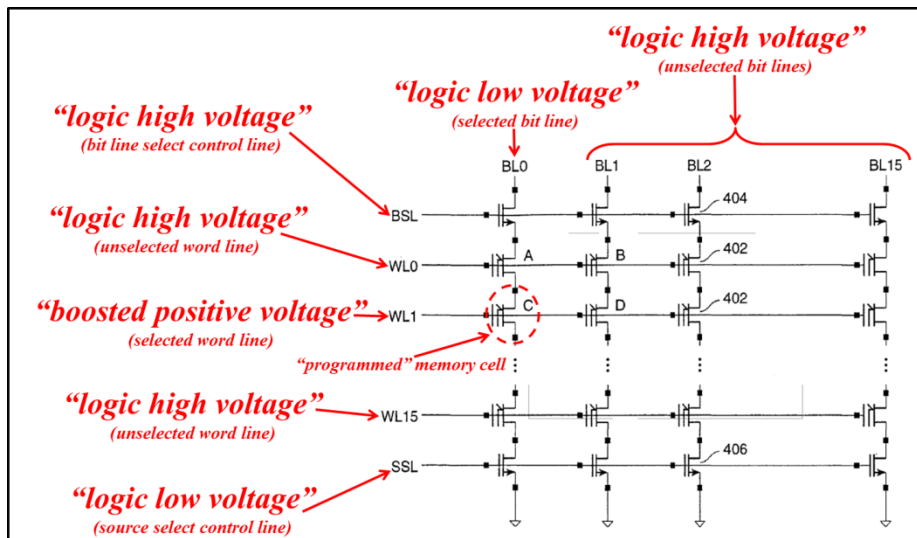
Deposition of Petitioner's Expert, Robert J. Murphy:

14 A No, it's not Vcc. Hold on. So my
15 recollection is that I don't recall Vcc being talked
16 about in Nakai, and I'm trying to see if there is a
17 location that I've missed or -- I don't see Vcc
18 specifically being quoted as what voltage it is.
19 And I don't recall reading that it was set at a
20 specific voltage. I'm sure it is. It just whether
21 the patentee put it in the spec or not.

(Ex. 2003, Murphy Depo. Transcript, p. 175, Ins. 14–21. See *also* Paper 20, PO Response, p. 21.)

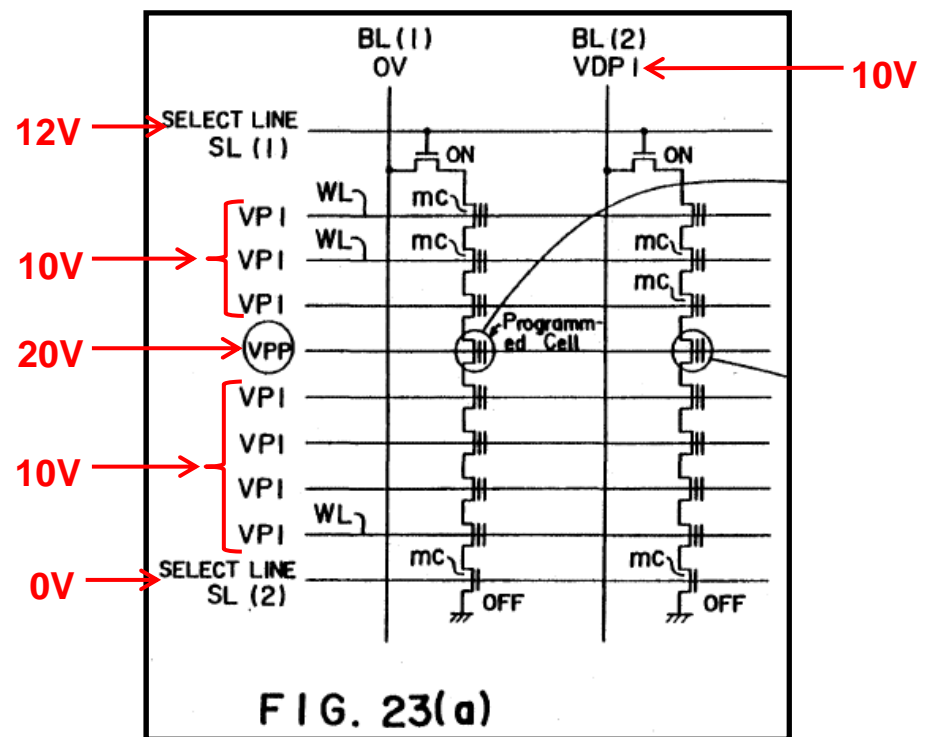
Nakai Does Not Anticipate

'045 Patent



(Paper 20, PO Response, p. 6.)

Nakai



(Ex. 1005, Nakai, FIG. 23(a), annotated with voltages disclosed in Nakai, 1:46-2:9.)

Nakai Does Not Anticipate

When Nakai's V_{CC} is taken into account, and the proper construction is applied to Nakai, it becomes clear that Nakai's V_{PI} (10V), V_{DPI} (10V) and 12V are all "boosted positive voltages" since they are positive voltages higher than Nakai's V_{CC} of 5V. Since claims 1 and 4 require a "logic high voltage" for the array elements shown above rather than a "boosted positive voltage," Nakai does not anticipate.⁷

(Paper 20, PO Response, pp. 21-22.)

CERTIFICATION OF SERVICE

The undersigned hereby certifies that the foregoing INTELLECTUAL
VENTURES I LLC'S DEMONSTRATIVE EXHIBITS was served electronically
via e-mail on November 5, 2014, in its entirety on the following:

Alan A. Limbach at **alan.limbach@dlapiper.com**

Gerald T. Sekimura at **gerald.sekimura@dlapiper.com**

CC: IV-Toshiba-DLA-Team@dlapiper.com

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Jon E. Wright/

Jon E. Wright
Registration No. 50,720
Attorney for Patent Owner

Date: November 5, 2014

1100 New York Avenue, N.W.
Washington, D.C. 20005
(202) 371-2600