UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TOSHIBA CORPORATION
Petitioner

v.

INTELLECTUAL VENTURES I LLC
Patent Owner

Case No. IPR2014-00113
Patent 6,058,045

PETITIONER TOSHIBA CORPORATION'S DEMONSTRATIVE EXHIBITS

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TOSHIBA

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Inter Partes Review of U.S. Patent No. 6,058,045 IPR2014-00113

Toshiba Corporation
Petitioner

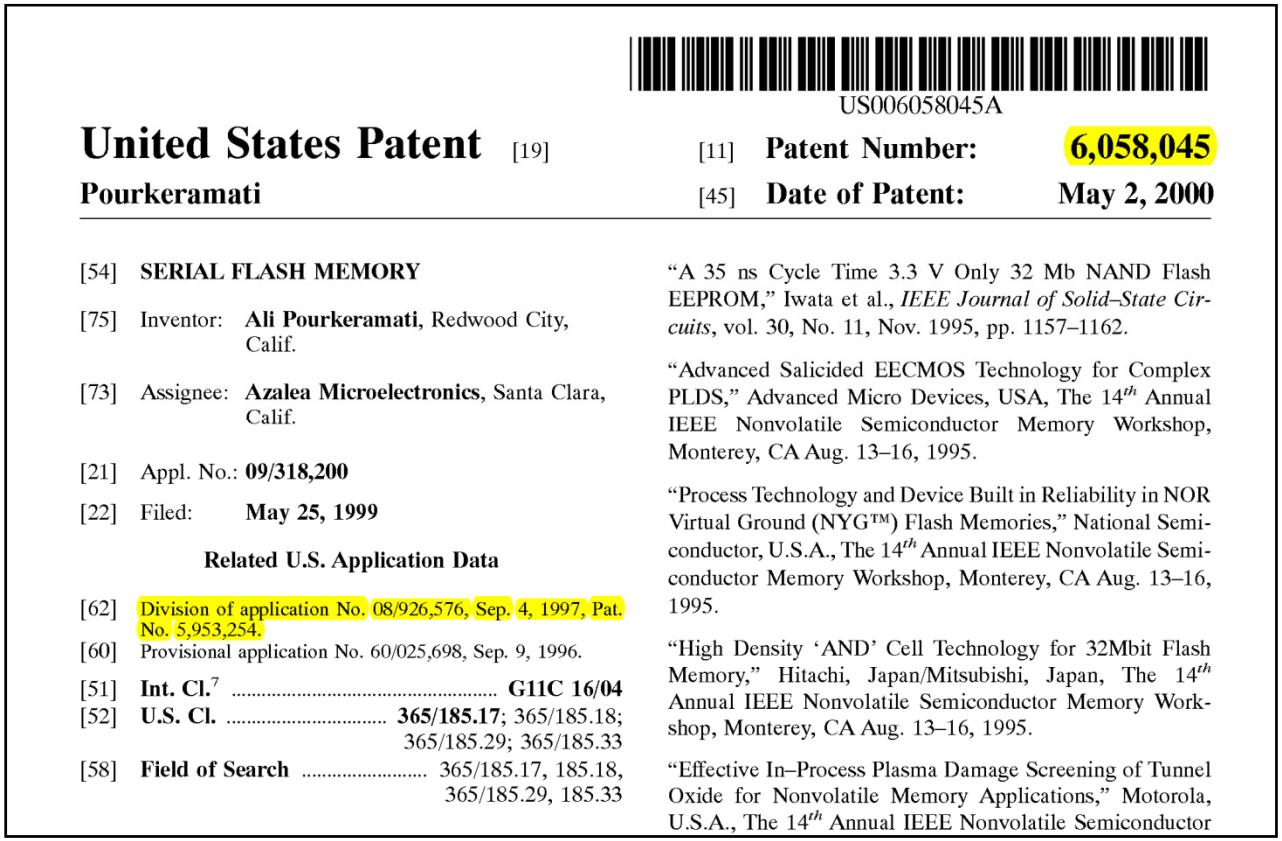
v.

Intellectual Ventures I LLC ("IV")
Patent Owner

Petitioner Toshiba Corporation's Demonstratives

Oral Hearing: November 6, 2014

IV's '045 Patent



US006058045A

United States Patent [19]

Pourkeramati

[11] **Patent Number: 6,058,045**

[45] **Date of Patent: May 2, 2000**

[54] **SERIAL FLASH MEMORY**

[75] Inventor: **Ali Pourkeramati**, Redwood City, Calif.

[73] Assignee: **Azalea Microelectronics**, Santa Clara, Calif.

[21] Appl. No.: **09/318,200**

[22] Filed: **May 25, 1999**

Related U.S. Application Data

[62] Division of application No. 08/926,576, Sep. 4, 1997, Pat. No. 5,953,254.

[60] Provisional application No. 60/025,698, Sep. 9, 1996.

[51] **Int. Cl.**[7] **G11C 16/04**

[52] **U.S. Cl.** **365/185.17**; 365/185.18; 365/185.29; 365/185.33

[58] **Field of Search** 365/185.17, 185.18, 365/185.29, 185.33

"A 35 ns Cycle Time 3.3 V Only 32 Mb NAND Flash EEPROM," Iwata et al., *IEEE Journal of Solid–State Circuits*, vol. 30, No. 11, Nov. 1995, pp. 1157–1162.

"Advanced Salicided EECMOS Technology for Complex PLDS," Advanced Micro Devices, USA, The 14th Annual IEEE Nonvolatile Semiconductor Memory Workshop, Monterey, CA Aug. 13–16, 1995.

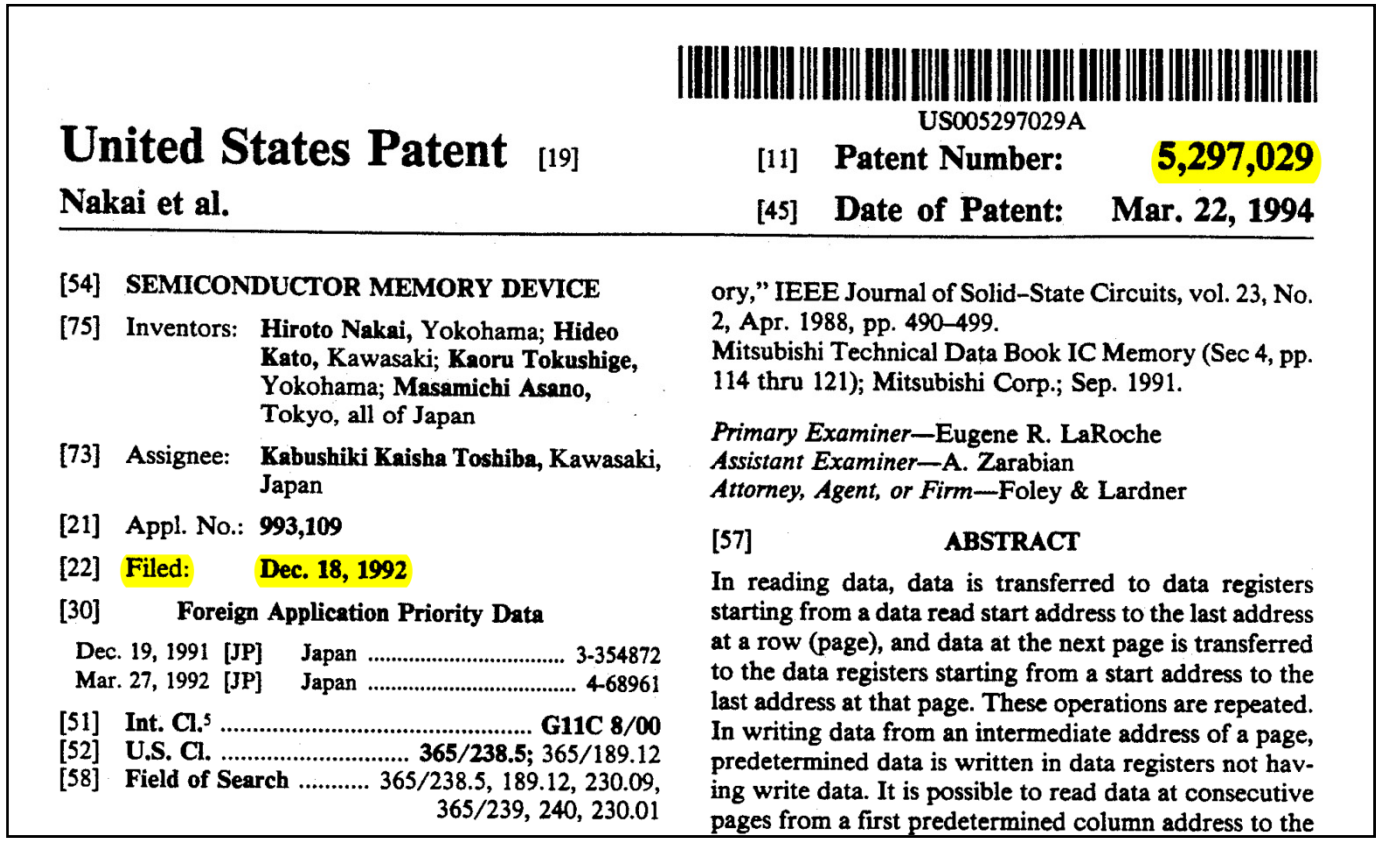
"Process Technology and Device Built in Reliability in NOR Virtual Ground (NYG™) Flash Memories," National Semiconductor, U.S.A., The 14th Annual IEEE Nonvolatile Semiconductor Memory Workshop, Monterey, CA Aug. 13–16, 1995.

"High Density 'AND' Cell Technology for 32Mbit Flash Memory," Hitachi, Japan/Mitsubishi, Japan, The 14th Annual IEEE Nonvolatile Semiconductor Memory Workshop, Monterey, CA Aug. 13–16, 1995.

"Effective In–Process Plasma Damage Screening of Tunnel Oxide for Nonvolatile Memory Applications," Motorola, U.S.A., The 14th Annual IEEE Nonvolatile Semiconductor

('045 patent, cover page - Exhibit 1001.)

Toshiba's '029 Patent - Nakai



US005297029A

United States Patent [19]

Nakai et al.

[11] **Patent Number: 5,297,029**

[45] **Date of Patent: Mar. 22, 1994**

[54] **SEMICONDUCTOR MEMORY DEVICE**

[75] Inventors: **Hiroto Nakai**, Yokohama; **Hideo Kato**, Kawasaki; **Kaoru Tokushige**, Yokohama; **Masamichi Asano**, Tokyo, all of Japan

[73] Assignee: **Kabushiki Kaisha Toshiba**, Kawasaki, Japan

[21] Appl. No.: **993,109**

[22] Filed: **Dec. 18, 1992**

[30] **Foreign Application Priority Data**

Dec. 19, 1991 [JP] Japan 3-354872
Mar. 27, 1992 [JP] Japan 4-68961

[51] **Int. Cl.**[5] **G11C 8/00**
[52] **U.S. Cl.** **365/238.5**; 365/189.12
[58] **Field of Search** 365/238.5, 189.12, 230.09, 365/239, 240, 230.01

ory," IEEE Journal of Solid-State Circuits, vol. 23, No. 2, Apr. 1988, pp. 490–499.
Mitsubishi Technical Data Book IC Memory (Sec 4, pp. 114 thru 121); Mitsubishi Corp.; Sep. 1991.

Primary Examiner—Eugene R. LaRoche
Assistant Examiner—A. Zarabian
Attorney, Agent, or Firm—Foley & Lardner

[57] **ABSTRACT**

In reading data, data is transferred to data registers starting from a data read start address to the last address at a row (page), and data at the next page is transferred to the data registers starting from a start address to the last address at that page. These operations are repeated. In writing data from an intermediate address of a page, predetermined data is written in data registers not having write data. It is possible to read data at consecutive pages from a first predetermined column address to the

(Nakai patent, cover page - Exhibit 1005.)

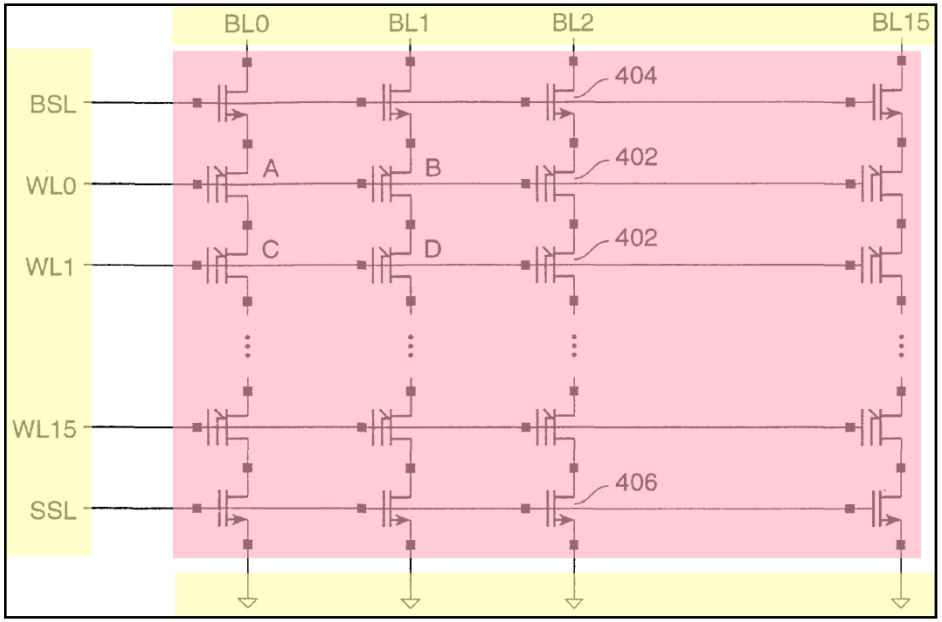
Adopted Claim Constructions

Claim Term	Petitioner's Proposed Constructions (Petition at 9-12.)
logic low voltage	a low voltage, such as ground or Vss
logic high voltage	a positive voltage higher than [the] logic low voltage, such as Vcc
boosted positive voltage	a positive voltage higher than [the] logic high voltage
selected bit line	the bit line connected to the column of memory cells containing the memory cell to be operated on
unselected bit lines	the bit lines connected to the columns of memory cells not containing the memory cell to be operated on
selected word line	the word line connected to the row of memory cells containing the memory cell to be operated on
unselected word lines	the word lines connected to the rows of memory cells not containing the memory cell to be operated on

The Board adopted Petitioner's proposed constructions (but without the word "the" underlined above.).

(Decision, at 7-9.)

Challenged claims cover (1) the array configuration and (2) applied program voltages



(Fig. 4, '045 patent - Exhibit 1001.)

4. A method of operating a flash memory device wherein programming memory cells is accomplished by the steps of:

applying a logic high voltage to a bit line select control line to turn on bit line select transistors,

applying a logic low voltage to a source select control line to turn off source select transistors;

applying a logic low voltage to a selected bit line while a logic high voltage is applied to unselected bit lines, and

applying a logic high voltage to unselected word lines, while a boosted positive voltage is applied to a selected word line.

(Claim 4, '045 patent - Exhibit 1001.)

(Reply at 1.)

1. An array of flash memory cells comprising:

a plurality of columns of serially connected flash memory cells, each memory cell having a gate terminal;

a plurality of bit lines respectively coupled to drain side of said plurality of columns of memory cells via a respective plurality of bit line select transistors, said plurality of bit line select transistors having gate terminals coupled to a bit line select control line;

a plurality of word lines, each one coupling to a gate terminal of one memory cell in each of said plurality of columns to from rows of memory cells with common gate terminals; and

a plurality of source select transistors respectively coupling a source side of said plurality of columns of memory cells to a logic low voltage, and having gate terminals coupled to a source select control line,

wherein, during programming:

a logic high voltage is applied to said bit line select control line to turn on bit line select transistors,

a logic low voltage is applied to source select control line to turn off source select transistors;

a logic low voltage is applied to a selected bit line while a logic high voltage is applied to unselected bit lines, and

a logic high voltage is applied to unselected word lines, while a boosted positive voltage is applied to a selected word line.

(Claim 1, '045 patent - Exhibit 1001.)

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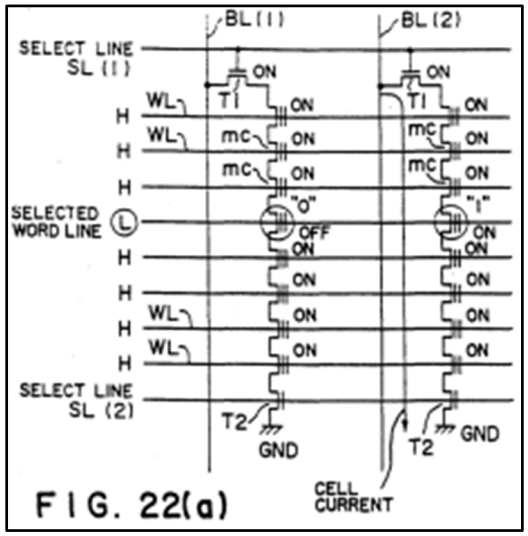
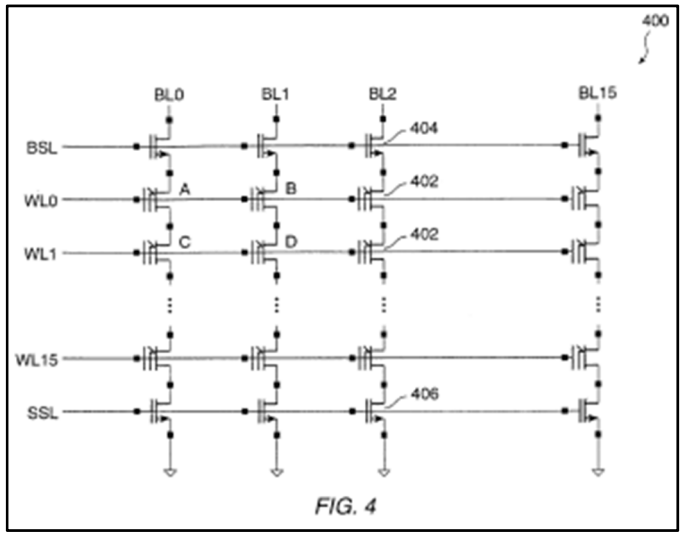
Undisputed: Nakai anticipates the claimed memory array configuration

Nakai anticipates the memory array configuration limitations under the Adopted Constructions. *(Petition at 13-14, 17-21 and 28-29.)*



(Fig. 22(a), Nakai patent- Exhibit 1005.)



(Fig. 4, '045 patent - Exhibit 1001.)

IV does not challenge the Adopted Constructions for the memory array configuration limitations, or argue they are not anticipated by Nakai.

(Reply at 1.)

Not Meaningfully Disputed: Nakai anticipates the claimed applied program voltages under the Adopted Constructions

Nakai anticipates the applied program voltage limitations under the Adopted Constructions. *(Petition at 15-16, 22-27 and 29.)*

IV's sole argument of validity under the Adopted Constructions is a single footnote:

> [7] Indeed, even if the Board does not alter its ambiguous preliminary claim construction, Nakai still does not anticipate. As shown, when the Board's construction is *actually applied* to Nakai and to the '045 patent, the upper boundary for "logic high voltage" becomes Vcc (instead of the indefinite "such as Vcc").

(Response at 22.)

Yet, there is no upper boundary of Vcc in the adopted construction of "logic high voltage":

Claim Term	Adopted Construction
logic high voltage	a positive voltage higher than logic low voltage, such as Vcc

(Decision at 7-8.)

NO meaningful dispute that Nakai anticipates the challenged claims under the Adopted Constructions.

(Reply at 2-3.)

Sole Contested Issue: Claim construction of "logic high voltage"

IV and its experts challenge only one of the Adopted Constructions:

Claim Term	"logic high voltage"
Adopted Construction	a positive voltage higher than logic low voltage, **such as Vcc.** *(Decision at 8.)*
IV and its experts	a positive voltage higher than logic low voltage **and less than or equal to the nominal value for Vcc.** *(Response at 7-15.)*

Sole issue in dispute: should the claims be effectively rewritten to add a numerical upper limit of Vcc to "logic high voltage" under the pretext of claim construction. (Reply at 1.)

This numerical upper limit is the only limitation argued by IV as distinguishing the claims over the Nakai prior art reference. (*Response at 15-22.*)

IV Never Applies The Requisite "Broadest Reasonable Construction" Standard

"A claim in an unexpired patent shall be given its broadest reasonable construction in light of the specification of the patent in which it appears." 37 CFR 42.100(b).

	Applied Claim Construction Standard	Citation
Petitioner and its expert	Broadest Reasonable Construction	*Petition at 8-13; Ex. 1006 at ¶16-20.*
Board	Broadest Reasonable Construction	*Decision at 7-9.*
IV and its experts	Clear Demarcation Principled and Precise Dividing Line Practical Dividing Line Reasonable and Principled Boundary More Precise Construction	*Response at 11, 17, 19-20.* *Response at 13, 17.* *Ex. 2001 at ¶31.* *Ex. 2001 at ¶39.* *Ex. 2002 at ¶28.*

(Reply at 6-8.)

IV and its experts do not challenge the Adopted Constructions, nor offer any constructions, under the requisite "broadest reasonable construction."

- IV and its experts apply narrower claim construction standards.
- IV and its experts never allege, let alone establish, any of their standards are the broadest reasonable construction standard.
- **There is no dispute in the record that the Adopted Constructions are appropriate under the "broadest reasonable construction" standard.**

(Reply at 6-8.)

Broadest Reasonable Construction of “logic high voltage”

The Petitioner, its expert, and the Board have set forth why the adopted construction for “logic high voltage” is the appropriate broadest reasonable construction:

- The term “logic high voltage” appears only in the claims and not in the specification.
- The construction is consistent with the exemplary voltages provided in the specification.
- One skilled in the art reviewing the ’045 patent would understand that “logic high voltage” is a voltage higher than logic low voltage, such as Vcc.
- The ’045 patent does not disclose ANY numerical limit on “logic high voltage.”

(Petition at 10; Ex. 1006 at ¶17; Decision at 8; Reply at 9.)

Adopted Construction of "logic high voltage" Appropriate Even Under IV's Claim Construction Standards

None of IV's arguments challenging the Adopted Construction of "logic high voltage" have any merit.
(Reply at 8-14.)

Adopted Constructions Dictate Where Voltages Begin And End

IV argues the Adopted Constructions only define the voltages relative to each other, which makes it "impossible to determine where one begins and the other ends." (Response at 10.)

Claim Term	Adopted Voltage Constructions
logic low voltage	a low voltage, such as ground or Vss
logic high voltage	a positive voltage ***higher than logic low voltage***, such as Vcc
boosted positive voltage	a positive voltage ***higher than logic high voltage***

(Decision at 7-8.)

Under the Adopted Constructions, logic low ends before logic high begins, and logic high ends before boosted positive begins. *(Reply at 9.)*

Adopted Constructions Dictate A Clear Demarcation

IV argues there is no clear demarcation between "logic high voltage" and "boosted positive voltage" if two or more voltages are applied to BSL, BL1 and WL0 during programming. *(Response at 11-12.)*

IV's argument misses the mark.

- If multiple different logic high voltages are applied, the challenged claims as properly construed merely require the boosted positive voltage to be greater than the logic high voltages (plural).
- IV admitted to the clear demarcation:

> voltages." Toshiba accomplishes this by defining the terms only relative to each other ("logic low" < "logic high" < "boosted positive"). But as a result, it is

(Response at 10.)

- IV's arbitrary numerical upper limit on "logic high voltage" does not solve its alleged problem, e.g. if all voltages are below Vcc.

(Reply at 9-10.)

IV's Proposed Numerical Upper Limit On "Logic High Voltage" Is Arbitrary

IV argues a numerical upper limit on "logic high voltage" is necessary for a clear demarcation between "logic high voltage" and "boosted positive voltage." *(Response at 11-12.)*

But, IV does not propose a similar numerical upper limit on "logic low voltage" for a clear demarcation between "logic low voltage" and "logic high voltage."

This glaring inconsistency shows IV's proposed construction under the pretext of "clear demarcation" is arbitrary and erroneous.

(Reply at 10.)

One Skilled In The Art Would Not Understand That "Logic High Voltage" Is Necessarily Equal To Or Less Than Vcc

IV argues that one of ordinary skill in the art would understand that a "logic high voltage" would be less than or equal to Vcc (the nominal value of the memory array's power supply). *(Response at 12.)*

To the contrary:

- The claims recite no numerical voltage limits.
  - Inventor could have included numerical voltage limits, and chose not to.
- No numerical voltage limits are disclosed in the specification, let alone Vcc.
- IV's construction directly contradicts the specification, as the '045 patent clearly contemplates "logic high voltage" exceeding Vcc:
  - Voltage of "about Vcc" is applied to BSL during erase, for which claims 2 and 5 recite applying "logic high voltage." *('045 patent, at 6:53-55.)*
  - Selected bit line during erase "can be as low as Vcc," for which claims 2 and 5 recite applying "logic high voltage." *('045 patent, at 6:60-65.)*

(Reply at 11-12.)

IV's Reliance On Memory's Power Supply Is Fatal To Its Construction

IV argues the Vcc numerical limitation is appropriate because of the memory array's nominal power supply. *(Response at 13.)*

IV's argument undermines its own proposed construction:

- Memory array's power supply is not recited in challenged claims.
- Memory array's power supply is not disclosed or described in specification.
- No claim limitations on source or sources of the claimed voltages.
- Mr. Berg admitted Vcc power supply is external to flash memory chip. *(Ex. 2002 at ¶¶ 22-23, 28, 49, 52-53.)*
- Scope of claim 1 would depend upon an unclaimed voltage, from an unclaimed power supply, that is separate from the claimed memory array device.

(Reply at 12-13.)

IV's Proposed Construction For "Logic High Voltage" Would Render Claim 1 Indefinite

IV's construction would render claim 1 indefinite.

Scope of claim 1 would depend on an unclaimed variable object: the external power supply that provides Vcc.

- There is no industry standard for Vcc.
- There is no industry standard for power supplies used to provide Vcc.
- One skilled in the art could not determine what is covered by claim 1.
  - Reference to externally supplied Vcc voltage (i.e. for which the memory chip is designed for) is akin to referring to the height of rider that the bicycle was designed for, which was held invalid.
    (Ex parte Brummer, 12 USPTQ2d 1653 (Bd. Pat. App. & Int. 1989.)

(Reply at 13.)

IV's Alleged Advantages Do Not Necessarily Result From Its Proposed Claim Construction

IV argues the claimed invention (under IV's proposed construction of "logic high voltage"), provides certain advantages. *(Response at 23.)*

Yet, IV's alleged advantages do not necessarily result from its construction of "logic high voltage," and they can be achieved under the Adopted Constructions.

- IV's Argument: Source and drain regions of the transistor "can have" the same diffusion construction.
  - Claims are not directed to memory cell components.
  - IV's construction does not require the same diffusion construction.
  - Adopted Constructions do not preclude the same diffusion construction.

- IV's Argument: Avoids on-chip charge pumps and other circuits.
  - Claims do not recite any such voltage sources or circuits.
  - IV's construction does not require the use of fewer charge pumps.
  - Adopted Constructions do not preclude the use of fewer charge pumps.

(Reply at 13-14.)

Experts

IV argues Petitioner's expert, Mr. Murphy, is not qualified to opine on "***NAND flash memory***." *(Response at 8-9.)*

- IV and its experts admitted the level of skill in the art for the '045 patent includes experience with "***flash memory***," not "***NAND flash memory***."
  (Reply at 3-4; Ex. 2001 at ¶17; Ex. 2002 at ¶19; Response at 8.)

IV argues that Mr. Murphy admitted lacking the requisite experience with "***flash memory***." *(Response at 9-10.)*

- IV's argument was disingenuous. IV failed to inform the Board of subsequent testimony that clarified the quoted answer was limited to ***stand-alone*** flash memory devices. Mr. Murphy testified that his experience more than met IV's definition of ordinary skill in the art of ***flash memory***.
  (Reply at 4; Ex. 2003 at 113:2-13; 114:11-117:6; 118:9-119:3; 20:18-22:17.)

Petitioner's expert applied the proper claim construction standard. IV's experts did not. *(Reply at 6-8.)*

IV's expert (Mr. Berg) proposed two conflicting constructions for "logic high voltage."
(Reply at 8; Ex. 2002 at ¶28 and ¶42.)

IV's Proposed Construction For "Logic High Voltage" Is An Improper Attempt To Amend The Claims

Inventor could have, but chose not to, limit the patent claims to devices using Vcc or lower for logic high voltages.

IV's proposed construction is an improper attempt to rewrite the claims without filing a motion to amend to save its patent over the Nakai reference.

Allowing IV to amend the claims under the pretext of claim construction would:

- wrongly deprive Petitioner of intervening rights.
- wrongly deprive Petitioner the opportunity to challenge the amended claims under new grounds of invalidity (i.e. obviousness over Nakai, additional prior art references, etc.) which is accorded with a motion to amend.

(Reply at 14-15.)

CERTIFICATE OF SERVICE

The undersigned certifies that a true copy of the foregoing **PETITIONER TOSHIBA CORPORATION'S DEMONSTRATIVE EXHIBITS** was served electronically via e-mail on November 5, 2014, in its entirety on the following:

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Dated: November 5, 2014

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