

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TOSHIBA CORPORATION,
Petitioner,

v.

INTELLECTUAL VENTURES, I, LLC,
Patent Owner.

Case No. IPR2014-00113
Patent No. 6,058,045

Held: November 6, 2014

Before KEVIN F. TURNER (via videoconference), TREVOR M. JEFFERSON, and DAVID C. McKONE (via videoconference),
Administrative Patent Judges.

The above-entitled matter came on for hearing on Thursday, November 6, 2014, commencing at 10:02 a.m., at the U.S. Patent and Trademark Office, 600 Dulany Street, Alexandria, Virginia.

Case No. IPR2014-00003 & IPR2014-005567
Patent 8,278,351

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P R O C E E D I N G S

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JUDGE JEFFERSON: Good morning. I'm Judge
Jefferson and with us remotely are Judges McKone and Turner.
We're here for IPR 2014-00113, Toshiba Corporation V
Intellectual Ventures I, LLC.
I'll ask each attorney to stand, starting with the Petitioner,
and make your appearances and state who is with you.
MR. LIMBACH: Good morning. My name is Alan
Limbach, I'm with DLA Piper, I represent the Petitioner, Toshiba; and
with me is -- go ahead.
MR. SINGH: Hi, my name is Harpreet Singh,
representing Petitioner with DLA Piper.
JUDGE JEFFERSON: Thank you.
MR. WRIGHT: Good morning, Your Honors.
Jon Wright from Stern, Kessler, Goldstein and Fox
representing the Patent Owner, Intellectual Ventures I.
With my at counsel's table is Christian Camarce, also
from Stern, Kessler, and back-up counsel that are also present are
Raymond Werner from the Stern Kessler firm, Andy Heinz from the
Desmarais firm and Donald Coulman from Intellectual Ventures.
Thank you.
JUDGE JEFFERSON: Thank you.

1 Obviously per our Order Paper 24, the proceedings will
2 be transcribed by a court reporter. Please speak up or into the
3 microphone.

4 We also remind you that we have two remote Judges and
5 any demonstratives or exhibits you refer to please refer to by page
6 number or other identifying marks so that we can then have a clear
7 record of what's being referred to and the Judges can follow your
8 presentations.

9 Each side will have 60 minutes to present their argument.
10 As Petitioner bears the burden of proof, we'll start with Petitioner.
11 You should let us know at the outset if you're going to reserve any
12 time for rebuttal.

13 The Patent Owner will have 60 minutes to respond to the
14 issues presented.

15 Again, I'll note for the remote panel members, they will
16 be, they should be mic'ed and able to hear everything that's going on.
17 If you have trouble, if you do have trouble hearing or we have trouble
18 hearing, we can repeat the questions we have for you.

19 On, I'm, my recollection is that there were no objections
20 made to demonstratives or evidence that were filed with the Court.

21 Just reminding you that there are no speaking objections
22 here. You have your time period to make any objections or -- I'm
23 sorry, make any statements on the record that you want to make
24 regarding evidence.

1 And we'll get started, if there are no questions from either
2 party.

3 And our Judges can hear everything okay?

4 JUDGE McKONE: I can hear, Judge Jefferson.

5 If I cannot hear somebody at the podium, I will let you
6 know. And you can hear me okay?

7 JUDGE JEFFERSON: Certainly.

8 Judge Turner?

9 JUDGE TURNER: Yes, I can hear. I can't hear anybody
10 until you talk into the microphone, but I'm looking forward to that.

11 JUDGE JEFFERSON: And I'll remind then, again,
12 please everyone talk into the microphone, including me. And of
13 course if our court reporter couldn't hear, she will let us know, as well.

14 We'll get started with Petitioner. Will you please let me
15 know how much time you're going to reserve and you can continue?

16 MR. LIMBACH: Thank you, your Honors.

17 Can you hear me remotely?

18 JUDGE JEFFERSON: Why don't you adjust the mic
19 straight so it looks a little more directional, straight at you.

20 MR. LIMBACH: Okay. Great, so again, my name is
21 Alan Limbach, for Petitioner, Toshiba, and I'll reserve 25 minutes for
22 rebuttal.

23 JUDGE JEFFERSON: Okay. You may begin.

24 MR. LIMBACH: Okay. Thank you.

1 So starting with, and I'll go by slide numbers, so if I
2 forget, just please remind me, but we'll dive right into slide 2.

3 So this IRP is about the '045 Patent, or what I'll be
4 referring to as the '045 Patent. It was filed in 1999 and claims priority
5 to a parent divisional -- or it's a divisional of a parent case that was
6 filed in 1997 claiming priority to a provisional in 1996.

7 The parent application covers the memory cells. There
8 was a restriction requirement in the parent case; and so this case just
9 covers how the memory cells are, flash memory cells are connected
10 together and how you apply the voltages.

11 Going to slide 3, this is the prior art that we'll be dealing
12 with today and what I refer to, you see this is a U.S. Patent 5,297,029,
13 what I'll be referring to as the Nakai reference. It is a Toshiba patent
14 and it was filed in 1992, approximately four years before the '045
15 Patent provisional application was filed.

16 Going to slide 3 -- 4, so in the Petitioner's petition we
17 offered seven claim constructions and three of those claim
18 constructions dealt with the voltages in the claim, in the asserted
19 claims -- or the challenged claims and four dealt with the array
20 configuration.

21 The Board adopted essentially the constructions that we
22 had proposed, minus the word the; and I don't think that that was
23 meant to signify anything that's relevant here today. So I'll be
24 referring to these as the adopted constructions.

1 Going to slide 5. So, the challenged claims have two
2 parts or aspects to them. The first is it sets forth the array
3 configuration of the memory array that's at issue or being covered by
4 the claim and the second is the applied voltages that are applied at the
5 various lines and in order to program a selected cell.

6 And those are highlighted on the slide.

7 Going to slide 6. Now what's undisputed in this case and
8 in this proceeding so far is the fact that Nakai anticipates the memory
9 array configuration aspects of these claims. We set forth in our
10 petition why those limitations are anticipated by Nakai.

11 I.V. never challenged the adopted constructions relating
12 to the array configuration and they don't argue that Nakai doesn't
13 anticipate those claim elements.

14 Going to slide 7, we also set forth in our petition why the,
15 under the adopted constructions, the applied program voltages are
16 anticipated by Nakai.

17 And the only argument that was ever introduced by I.V.
18 in its reply is a footnote that basically argued -- well I'll just read it, it
19 says, as shown, when the Board's construction is actually applied to
20 Nakai and the '045 Patent, the upper boundary for the logic high
21 voltage becomes Vcc. Well that's not the adopted construction. The
22 adopted construction is a positive voltage higher than logic low
23 voltage such as Vcc.

1 Here they're kind of wrapping in their proposed
2 construction, so to us we don't see that it's actually meaningfully
3 disputed that under the adopted constructions Nakai anticipates.

4 Going to slide 8. So the real issue here is claim
5 construction. I.V. and its experts challenge one of the adopted claim
6 constructions and only one, that's the, for logic high voltage.

7 Now everyone agrees that a logic high voltage is a
8 positive voltage higher than logic low voltage; and what's different is
9 that in I.V.'s proposed construction, they add an additional limitation,
10 and less than or equal to the nominal value of Vcc; and it's that
11 limitation that they're reading in to the claim language that is their sole
12 basis for why Nakai does not anticipate. If they can't read that
13 limitation in to the claim, it's essentially undisputed, the claims are
14 invalid over Nakai.

15 So the sole issue here is should we effectively re-write
16 the claims to add this numerical cap to the logic high voltage of Vcc.

17 Going to slide 9. Now 37 CFR 42.100(b) states, a claim
18 in an unexpired parent shall be given its broadest reasonable
19 construction in light of the specification of the patent in which it
20 appears. So that's the claim construction standard that we are all
21 operating under.

22 Now this slide summarizes the claim construction
23 standards argued or applied in this proceeding.

24 The Petitioner and its expert used broadest reasonable
25 construction. The Board used the broadest reasonable construction.

1 I.V. and its experts did not. They used other standards. They said,
2 well, clear demarcation or principled and precise dividing line,
3 practical dividing line, reasonable and principled boundary or a more
4 precise construction.

5 They don't challenge the adopted constructions under the
6 broadest reasonable construction standard. They don't identify the
7 standard and they never applied it.

8 They applied narrow constructions and they never try and
9 tie these constructions that they've argued to broadest reasonable.

10 So we don't believe that there's a dispute in the record in
11 this case on the issue of whether or not this -- the adopted construction
12 for logic high voltage is proper under the broadest reasonable
13 construction standard.

14 Going to slide 10. Now the Petitioner, its expert and the
15 Board all articulated why the adopted construction for logic high
16 voltage is appropriate.

17 The term logic high voltage appears only in the claims;
18 it's not in the specification. It's consistent with the exemplary voltages
19 provided in the specification. One skilled in the art viewing the '045
20 Patent would understand that logic high voltage is a voltage that's
21 higher than -- or is a voltage that's higher than logic low, such as Vcc.
22 There's nothing else in the specification that would provide anything
23 other than that.

1 JUDGE JEFFERSON: Counsel, has Petitioner presented
2 any testimony that supports the logic high voltage construction that
3 you proposed and the Board adopted in its preliminary decision?

4 MR. LIMBACH: Are you referring to an expert?

5 JUDGE JEFFERSON: Yes.

6 MR. LIMBACH: Yes. Our expert opined that this is the
7 proper construction and he applied the broadest reasonable
8 construction standard.

9 He identified the standard, he applied it and he concluded
10 this is the only reasonable construction under that standard.

11 JUDGE McKONE: So why isn't it just common sense
12 that the logic high is whatever is interpreted as a one, a logic one by
13 the remainder of the chip, as opposed to a logic zero?

14 MR. LIMBACH: When you go in to the patent -- we
15 looked for that, we looked for anything we could latch on to this, the
16 meaning of this other than what we proposed.

17 There is no logic device to tie that to; and the problem is
18 the logic high voltage is not applied to a logic device, it's applied to
19 things like word lines. Those are not logic devices, those are memory
20 cells.

21 And so, and the other problem is it says apply a logic
22 high voltage, a logic high voltage, a logic high voltage. So there's
23 more -- there can be more than one. In other words, they don't have to
24 be the same.

1 So if you're applying a voltage to a word line where
2 there's no logic device, we couldn't find any meaning for that.

3 JUDGE McKONE: Is there no ordinary meaning in the
4 context of memory devices where a logic high is 3.3 volts or 5 volts or
5 whatever is interpreted as a one by a memory cell?

6 MR. LIMBACH: Well, first of all, the specification
7 doesn't identify any such logic devices. Moreover, you could have
8 different logic devices on the same chip with different logic voltages.

9 So if, if we're going to tie the logic high to a logic device,
10 it has to be in the claims. It certainly has to be in the specification and
11 they don't identify that.

12 JUDGE TURNER: Counsel, with respect to claims 1
13 and 4, since the use of high voltage there is with respect to
14 programming, is there any other place in the spec that they can find
15 support other than column 7, let's say lines, it looks like 26 to 55?

16 MR. LIMBACH: I guess I didn't understand your
17 question.

18 JUDGE TURNER: The claims talk about, about logic
19 high voltage, but they talk about it with respect to 1 and 4. They only
20 talk about it during programming, and so the only part of the spec that
21 is really sort of specifically directed to the programming operation is
22 column 7 where it talks about programming operation. They have a
23 read operation.

24 So I would think if you, if you wanted support for what
25 that logic high voltage is, you'd have to find that support in those two

1 paragraphs in that column, or, or I'm sure Patent Owner will come up
2 and dispute that, but I guess I'm looking for your take on that.

3 MR. LIMBACH: So if you go to the specification, it
4 talks about the voltages, it gives exemplary voltages. It says you can
5 apply Vcc to the, say, the selected word line and then you go to the
6 claim and it says that's the logic high voltage, but there's nothing in
7 there that says it has to be Vcc.

8 And even I.V. admits it can be lower than Vcc. They
9 only give one value, they just say Vcc. They also use logic high
10 voltage to describe the erase operation, so it has to have the same
11 meaning and, again, it's not provided in the specification.

12 There's nothing that provides one of ordinary skill any
13 guidance as to anything other than they're just relative to each other.
14 There's no file history to rely on. The case was allowed without any
15 amendment or argument, so there's nothing that's provided in the
16 specification to provide you any guidance as to what these voltages
17 should be, other than the way that they are spelled forth in the adopted
18 constructions.

19 JUDGE TURNER: Okay.

20 MR. LIMBACH: One thing also to note is that the '045
21 Patent does not disclose any numerical limits on any of these voltages.
22 It does not say, oh, you can't have this particular voltage exceed X
23 value, which is important because that's the construction that's being
24 proffered by I.V.

1 So going to slide 11. Now, setting aside the fact that they
2 didn't apply the broadest reasonable construction, they set forth under
3 their standards many arguments as to why the logic high voltage
4 should be capped at Vcc. And even applying their arguments and
5 their standards, they don't have any merit, they don't make any sense,
6 and so I'll walk through those now.

7 Going to slide 12. Now first they, I.V. argues that the
8 adopted constructions only define the voltages relative to each other,
9 which is true. But they say well that makes it impossible to determine
10 where one begins and another ends, and that's simply not true.

11 The logic high is higher than the logic low and the
12 boosted positive is larger than the logic high. So, the logic low ends
13 before the logic high begins and the logic high ends before the
14 boosted positive begins. So you do know where one begins and
15 another one ends.

16 Going to slide 13. Now they say that there's no clear
17 demarcation between logic high voltage and boosted positive voltage
18 when you have more than one logic high voltage. And again, we don't
19 think that this argument has any merit to it.

20 If multiple different logic high voltages are applied, the
21 way that the claims are structured as they're properly construed, it just
22 simply means that the boosted positive has to be higher than the logic
23 high voltages, plural. There's nothing more in the claims or the
24 specification to provide otherwise.

1 And that's a clear demarcation. And, in fact, their own
2 papers admit that there's a clear demarcation because they actually set
3 forth the adopted constructions in an algebraic form and you can see
4 that they set it forth at logic low is less than logic high and logic high
5 is less than boosted positive. So there is a clear demarcation.

6 Now, they say well, no, we need to cap logic high at Vcc
7 to provide some type of a clear demarcation, but that, it doesn't work
8 that way. If you have a logic low -- I'm sorry, a logic high that's
9 below Vcc, that means that the boosted positive can be below Vcc, it
10 just needs to be higher than logic high. So the Vcc provides no value,
11 it doesn't mean anything.

12 Going to slide 14. Now the, a telltale indication of how
13 arbitrary this cap is is the fact that you have the same issue between
14 the difference between logic low and logic high, yet I.V. never
15 proffered a construction for capping logic low so you'd have that same
16 clear demarcation.

17 If they're so concerned about a clear demarcation
18 between logic high and boosted positive that's separate from simply
19 trying to save its patent over Nakai, then they would have offered a
20 construction for logic low and they didn't. So that shows you it's
21 arbitrary, it's erroneous, there's no merit to it.

22 JUDGE McKONE: Could it be that they just didn't need
23 to offer a construction of logic low because that wouldn't have
24 affected the outcome of the case?

1 MR. LIMBACH: It's possible, but I mean if they're
2 going to challenge the adopted constructions and they would say,
3 look, you need a clear demarcation between logic high and boosted,
4 don't you think that they would have at least said and of course the
5 same goes true for logic low.

6 I mean if we need that clear demarcation to apply this
7 patent, why not construe that as well. They didn't, they didn't provide
8 one.

9 I.V. argues that, one, and we're on slide 15 now, I.V.
10 argues that one of ordinary skill in the art would understand reading
11 the patent that the logic high is capped at Vcc, but there's nothing in
12 the -- there's nothing in the patent that suggests that.

13 The claims recite no numerical limits for any of the
14 voltages. If, if they wanted to cap logic high at Vcc, they could have
15 put that in the patent, they could have put that in the claims. They
16 chose not to.

17 Now, we all know that as, as this technology progresses,
18 voltages change, thresholds change and so it's a clear intent by the
19 inventor not to be tied to any specific voltage. He thought at the time,
20 because he didn't know about Nakai, that he had this broad concept of
21 how to apply programming voltages and now that they're faced with
22 Nakai, they're trying to reel back that scope, but that's not claim
23 construction, that's claim re-writing, that's claim amendment. We
24 don't think that's proper in the context of how they're doing it.

1 More importantly, there's no numerical limits even in the
2 specification. It nowhere describes that Vcc is an absolute limit for
3 logic high. So not only are they reading in a limitation in to the
4 claims, they're reading it from outside the patent.

5 Their construction also directly contradicts two
6 disclosure portions of the specification and they're cited on slide 15,
7 but it talks about the BSL line during erase and the BSL line that says
8 the voltage is about Vcc.

9 Well one of ordinary skill in the art when they hear about
10 Vcc, that means, well, it can be approximately, it can be a little below
11 or a little below -- above. Claim 2 and Claim 5 recite that the BSL
12 during erase is logic high. So the patent actually supports and
13 discloses that logic high can exceed Vcc.

14 The same is true for the bit line during the erase
15 operation where it says it can be as low as Vcc. Again, one of ordinary
16 skill reading that would say, oh, that means that it can be above Vcc
17 and, again, Claims 2 and 5 recite that that particular line is logic high.

18 So the patent actually --

19 JUDGE McKONE: I assume you would also oppose a
20 construction if we were to modify our construction to be about Vcc
21 rather than just below Vcc or -- I assume you would still oppose
22 around Vcc or about Vcc for logic high; is that correct?

23 MR. LIMBACH: Absolutely, because that, they, they
24 swung for the fences when they drafted these claims. They had the
25 control over how broad these claims would be and it's not our job to

1 try and narrow the claims in order to save the patent. If they wanted
2 to do that, they could have filed a motion to amend. They didn't.

3 They're trying to argue this is construction and this is not
4 the broadest reasonable construction. And, you know, if, if we didn't
5 have Nakai in front of us, why would we limit it to about Vcc, what
6 would be the reason to do that.

7 The only reason to limit it to Vcc is to save the patent
8 from invalidity and that's not claim construction, that's claim re-
9 drafting.

10 They could have put in dependent claims that limited it to
11 Vcc, but they didn't do that. And the problem is when we go to have
12 this patent asserted against us, they'll hit us with a nice broad claim on
13 infringement and then when we start showing prior art, they're circling
14 the fences and trying to narrow the claims.

15 That's not how it works. Either the claims are valid or
16 they're not valid. We're not here to try and save the patent over the
17 prior art -- well they are, but I'm not.

18 So I think that's all for slide 15. Give me just a second
19 here. So in slide 16 another argument they say is, well, limiting it to
20 Vcc is important because that's tied to the nominal power supply and
21 they give all sorts of reasons why it's really important to limit it to
22 Vcc, you don't want it to exceed, you get all these advantages and so
23 forth.

24 The problem is that the memory array power supply is
25 not recited in the claims. As a matter of fact, it's not even in the

1 specification. The memory array's power supply -- I'm sorry, the
2 claims don't include any limitations under the source of these
3 voltages. It doesn't say you have to get it from the Vcc or the primary
4 power supply source. You can get these voltages from anywhere,
5 according to the claim terms. There's no limitations on where these
6 voltages come.

7 As a matter of fact, Mr. Berg, their expert, testified that
8 Vcc power supply is typically an off-chip power source. So that
9 means that the scope of Claim 1 would depend upon an unclaimed
10 voltage from an unclaimed power supply that's external to the memory
11 array that's claimed in Claim 1.

12 And that kind of feeds in to slide 17. Their claim
13 construction actually renders Claim 1 indefinite. The scope of Claim
14 1 now depends upon an unclaimed variable object, this power supply,
15 this Vcc source. There's no industry standard for the value of Vcc.
16 Vcc typically refers to the power supply, the primary power supply's
17 voltage, wherever that power supply may be. It can be on chip, it can
18 be off chip.

19 There's also no industry standard for the power supply,
20 itself, where it is, what it is, what it does.

21 So here what you're doing is you're referencing
22 something that's externally applied and that's going to dictate the
23 scope of the claim.

24 So let me give you an example. Let's say that someone
25 makes a chip that reads on Claim 1. It has all of the architecture and

1 it's set to apply the voltages as specified in Claim 1. And it's got three
2 pins and it's got all its power pins on the side and one of them is Vcc,
3 one of them is logic low, one of them is logic high, one of them is
4 boosted positive; so all the voltages are coming in.

5 So, if you supply Vcc or lower to the logic high pin, that
6 would meet the claim and now we have infringement, according to
7 I.V.

8 But if suddenly I boost that voltage up to Vcc plus a
9 small number, all of a sudden the chip doesn't infringe? That can't be.

10 I have a chip here sitting here on the counter, does it
11 infringe or not? They can't tell me until I hook it up to the power
12 supply and then they'll look at the logic high voltage coming in and
13 then they'll make their determination.

14 So the scope of Claim 1 is indeterminable under their
15 construction. It gives no notice to the public what infringes and what
16 does not.

17 JUDGE McKONE: What about just construction of
18 logic high to be the chip power supply; why is that problematic?

19 MR. LIMBACH: The chip power supply is not part of
20 the array, it's not part of the chip.

21 So if I have a chip sitting here, the power supply is --
22 could be supplied by another manufacturer.

23 So I've got a chip and if I drop it in and the logic high
24 voltage that's supplied to it is above what they consider Vcc, then it
25 doesn't infringe. If it, if it --

1 JUDGE McKONE: They --

2 MR. LIMBACH: They meaning the person who drops
3 the chip in to the board that contains the power supply.

4 So you can't -- if you do that, if I've got a chip here, I
5 don't know if it infringes or not under their construction until I tie it to
6 a power supply.

7 That's not part of the claim language. It gives you, it's,
8 it's completely indefinite.

9 JUDGE TURNER: Let me ask a follow-up question real
10 quick. So if the claim actually recited Vcc, your position would be
11 that it's still indefinite?

12 MR. LIMBACH: If claim --

13 JUDGE TURNER: Let's say Claim 1 recited and said,
14 wherein, logic high is Vcc.

15 In theory, that could change, depending on what my
16 inputs to my chip are, so I think under your logic the claim would still
17 be indefinite, right?

18 MR. LIMBACH: I believe so. I believe so.

19 If I were drafting the claim, I would have set forth the
20 power supply, I would have defined it. I would have said there's a
21 voltage supplied by it. I would even have defined the fact that the
22 boosted positives may be derivative off of that. I would have set forth
23 where the power supply is to give guidance to those in the industry to
24 say, okay, now I know what you're talking about.

1 And, again, I would also put in the specification, oh, and
2 by the way, make logic high limited to Vcc because you get all these
3 advantages. None of that is taught. There's nothing in the
4 specification --

5 JUDGE TURNER: But if it was in the claim, it would
6 still be indefinite?

7 MR. LIMBACH: I would say --

8 JUDGE TURNER: And that's what I'm trying to get --

9 MR. LIMBACH: -- yeah, yeah.

10 JUDGE TURNER: Because there are a lot of claims, a
11 lot of claims to devices, having examined in this area, I can tell you
12 there are a lot that recite Vcc, so this is sort of, your argument
13 followed to its logical conclusion would be we've got an awful lot of
14 invalid patents out there because they recite Vcc which could be any
15 value, I guess.

16 Maybe I'm taking your argument to an absurd limit,
17 perhaps.

18 MR. LIMBACH: I'd have to look at the claims. I, I don't
19 know.

20 But if you're going to recite Vcc, you've got to set forth
21 in the claims what that is or in the specification and they didn't even
22 do that.

23 So, I don't know --

24 JUDGE TURNER: Okay.

25 MR. LIMBACH: -- I guess in the abstract --

1 JUDGE McKONE: So it is your position that because
2 the claims are not tied to specific numerical values, they're indefinite?

3 MR. LIMBACH: If you're going to tie it to a numerical
4 value such as Vcc, you have to identify the source of Vcc. Here they
5 don't, the claims don't identify that.

6 I don't know if I'm answering your question.

7 JUDGE TURNER: I, I think you are. I think I, I --
8 maybe we'll let you move along.

9 MR. LIMBACH: Okay.

10 JUDGE TURNER: So.

11 MR. LIMBACH: I mean it's a great hypothetical, but
12 they don't have that. They have an example of Vcc in the
13 specification, there's nothing in the claim that says Vcc.

14 I didn't -- that's an interesting question. If they had said
15 just Vcc in the claim language, it's certainly more definite, but I'd
16 have to think about that.

17 Back to slide 18. Now they say that, well, if you cap
18 logic high voltage, you have all these advantages that you get. Well,
19 none of the advantages that they espouse are even in the patent, they
20 don't even suggest it. And none of them necessarily result from their
21 construction.

22 They say, well you can have the source and drain regions
23 of the transistor, they can have the same construction, but these claims
24 are not directed to a specific memory cell, they cover all memory
25 cells.

1 Their construction does not require, does not necessarily
2 result in the same diffusion and the adopted constructions don't
3 preclude using the same diffusion.

4 Now they also argue, well, you can avoid all these on-
5 chip charge pumps and other circuits by limiting logic high to Vcc.
6 But the claims don't recite those circuits. There's no limitations on
7 where these voltages come from.

8 So their advantages, their construction does not
9 necessarily result or require future -- or charge pumps and the adopted
10 constructions don't preclude it.

11 Slide 19, I.V. challenged our expert's credentials. I won't
12 spend a whole lot of time on this other than to say they first argued
13 that he's not, he doesn't have the requisite experience in NAND flash
14 memory, yet both I.V. and their experts agreed that the art that's
15 applicable to one of ordinary skill in the art for the '045 Patent is flash
16 memory, not NAND flash memory.

17 And the second thing is they, they took a quotation
18 grossly out of context to say that he didn't even have the requisite
19 experience with flash memory. And so I just, I, we point you to the
20 testimony and you can decide for yourself whether that was a fair
21 criticism or not.

22 What's not disputed, though, is that the Petitioner's expert
23 is the one that applied the appropriate claim construction standard and
24 the I.V. experts did not. Like I said, they don't even use the term, they

1 don't even recognize that the standard exists because they didn't argue
2 it.

3 And it should be noted that, you know, Mr. Berg, again,
4 one of their experts, he actually proffered two different competing
5 constructions for logic high. Now, granted, he was talking about the
6 low end, but at one point he adopts I.V.'s construction, but then later
7 on he says oh, no, the low end of the scale is the trip value of a logic
8 circuit. So even he was inconsistent in his own declaration about
9 what their construction should be.

10 Slide --

11 JUDGE TURNER: Counsel, just real quick, if we
12 exclude Mr. Murphy's testimony, does anything change in this case?

13 That's what I wasn't quite sure of from the arguments
14 back and forth.

15 MR. LIMBACH: Not that I know of.

16 JUDGE TURNER: I mean it seems like the claim
17 construction remains the same, that Mr. Murphy is certainly
18 mentioned in the decision institute, but it doesn't seem like even if we
19 say he's not one of ordinary skill and we ignore his testimony that
20 anything really changes in the case, but --

21 MR. LIMBACH: Correct. They just were arguing that
22 not to give his testimony weight compared to their experts. I think
23 that was their only argument.

24 JUDGE TURNER: Okay.

25 MR. LIMBACH: But I agree, nothing changes.

1 So, the inventor had the opportunity if he wanted to to
2 add these limitations when they were prosecuting the original patent
3 and they, and he chose not to.

4 He didn't include -- he could have put it in the
5 specification, hey, you can limit it to Vcc, you can have all of these
6 advantages; none of that is there. Could have put it in the claims;
7 didn't do that. Could have described all these advantages; didn't do
8 that.

9 Now, I.V. had the opportunity to file a motion to amend.
10 If they wanted to put this limitation in, they could have done that. If
11 they were, if they wanted to amend the claim, which is what their
12 construction is doing, they are amending this claim, but they didn't do
13 that.

14 And there are reasons, there are litigation-driven reasons
15 why they didn't do that. That would have conferred upon Toshiba
16 intervening rights because now you have an amended claim that
17 would limit their damages. They didn't want to do that.

18 It would also, in this proceeding, it wrongly deprives us
19 of challenging the amended claim. If the claim is limited now to logic
20 high voltage capping at Vcc, we would have been given an
21 opportunity to go out and find new art or come up with alternate
22 theories of invalidity such as obviousness over Nakai and by doing it
23 this way, they've deprived us of that opportunity.

24 So procedurally it's wrong, as well. So we think the
25 adopted claim constructions are appropriate. We think that it's then,

1 it's undisputed that claims 1 and 4 are invalid over Nakai as
2 anticipated.

3 And that, I believe, is the end of my presentation, unless
4 you have any other questions.

5 JUDGE JEFFERSON: Counsel, I do have one question.
6 Trying to at least understand what I think the Patent Owner's partial
7 argument would be in response to this is that logic high is not being
8 redefined or amended, it's what one of ordinary skill in the art would
9 know from reading the spec alone and that there's a lot of citations to
10 extrinsic textbooks and books, micro electronics and CMOS circuits
11 that they say support the notion that Vcc is what everyone understands
12 the claims are limited to.

13 What's your response to that?

14 MR. LIMBACH: My response is, as Mr. Murphy
15 testified, that's not how one of ordinary skill would read this.

16 They would look at this and say they, they shot for the
17 moon, they, they thought that their invention was merely three
18 voltages positioned in the way they were with no caps. That was,
19 that's the natural read of this patent. And the fact that the patent
20 doesn't teach the fact that you'd want to cap it, any of these voltages in
21 any way, and the fact that in two places the patent says that it, logic
22 high can exceed Vcc.

23 If logic high was always, if, if it was clearly written so
24 one of ordinary skill in the art would look at that and say, oh, that's

1 capped at Vcc, then how come the patent twice says it can be above
2 Vcc.

3 That's not how one of ordinary skill would read it.

4 JUDGE JEFFERSON: Thank you.

5 MR. LIMBACH: Okay. Thank you.

6 JUDGE JEFFERSON: And you finished on time, so,
7 you have 25 minutes remaining.

8 MR. LIMBACH: Okay, great.

9 MR. WRIGHT: May it please the Board, Jon Wright,
10 again, on behalf of the Patent Owner, Intellectual Ventures I.

11 So, conventional flash memory devices required a
12 nominal power supply voltage and several higher voltages that were
13 used specifically for a programming operation. And early flash
14 memory devices received those voltages typically from external
15 sources.

16 One early innovation in the field of flash memory was to
17 eliminate the need for those multiple external voltages and to move
18 them on chip; and Nakai takes advantage of that innovation, but at the
19 cost of increased on-chip space and power consumption.

20 The '045 Patent moved the art a little bit further. And
21 what it allows is overcoming that problem in a flash memory array
22 that can be programmed with lower voltages than were typically used
23 in the prior art and specifically it allows the program inhibit portion of
24 a program operation to be achieved using the chip's nominal power

1 supply, Vcc. That is what one of ordinary skill in the art would
2 understand as being the logic high voltage.

3 So that we have a common understanding of how a flash
4 memory array is programmed, according to the claims, I'll turn to, first
5 to slide 2, which illustrates the claimed method for programming a
6 flash memory array.

7 So what we have on slide 2, of course, is an array of
8 floating gate transistors arranged in rows and columns and there are
9 three basic pathways to control an array of floating gate transistors.
10 On the drain side we have the bit lines along the top. On the source
11 side we have ground and a source select transistor and then going to
12 the control gates of these floating gate transistors, we have the word
13 lines.

14 So a cell in a flash memory array of course is
15 programmed by putting a high enough E field from the control gate of
16 the floating gate transistor across the channel to cause electrons to
17 tunnel in to a floating gate where they're stored. The cell is erased
18 with the opposite operation, you reverse the E field and push the
19 electrons off of the floating gate and a cell is read by sensing its
20 threshold voltage, which is different for a program cell than it is for an
21 erased cell.

22 And importantly, in the context of this discussion, the
23 high E fields required to operate a flash memory array also require
24 measures to protect neighboring, unselected cells. And during a

1 programming operation, these measures are referred to as program
2 inhibit measures, or sometimes shortened to P.I.

3 So for a flash memory cell, the programming operation
4 must select a cell to be programmed and it must protect unselected
5 cells.

6 As I've stated, the claimed flash memory array achieves
7 the protect function, the program inhibit function with a lower voltage
8 than is in the prior art and that lower voltage is the logic high voltage
9 that is applied to the unselected word lines, to the unselected bit lines
10 on the drain side and to the bit line select transistor.

11 JUDGE JEFFERSON: So, counsel, logic high voltage
12 doesn't appear in this specification, correct?

13 MR. WRIGHT: So, let me, let me turn to logic high
14 voltage and to Nakai.

15 JUDGE JEFFERSON: Well hold on, I mean, so it
16 doesn't, according to my question, it doesn't appear, those words don't
17 appear in the spec, correct?

18 MR. WRIGHT: It does in the sense that in the, the utility
19 application that was filed, and in the original patent utility application
20 that was filed, the patentee chose to use the term logic high voltage in
21 the originally-filed claims, which are part of the specification.

22 And one of ordinary skill in the art, and this is what
23 Toshiba did not mention during the entire course of its presentation, is
24 that claims are entitled to be read and, in fact, must be read according

1 to how one of ordinary skill in the art would understand those, those
2 claims.

3 So let's, let's think back to the time of invention and think
4 about, well, what would a patentee who wanted to use the Vcc, or the
5 nominal power supply for a memory device, what would be the best
6 way to claim that.

7 Well, would you use Vcc? Not necessarily, that's a, a
8 colloquial term. It refers to a collector voltage back when the
9 transistors were typically bipolar junction transistors.

10 Well would you use Vdd, which is the nominal power
11 supply voltage for a FET, typically, that refers to the drain voltage, or
12 would you use the power supply voltage. Well as I stated early on,
13 there were multiple power supply voltages going to a chip.

14 So one of ordinary skill in the art would have selected a
15 term that, that best gets to what the inventor was trying to achieve and
16 here that is the term logic high voltage.

17 And what the evidence --

18 JUDGE JEFFERSON: So --

19 JUDGE McKONE: You just told us that logic high
20 voltage could mean any of Vcc, Vdd power supply of the chip and
21 that the inventor did not want to limit the term that was used in the
22 claim because of all these possible technologies that the claim would
23 want to reach in the future; is that what I'm getting?

24 MR. WRIGHT: Well, what, the term logic high voltage
25 is linked to, intrinsically linked to Vcc. It is linked by Toshiba's own

1 expert, Mr. Murphy, who proposed a construction that said higher
2 than logic low voltage such as Vcc, and when you turn to both of the
3 Patent Owner's two experts and their declarations and the evidence
4 that they support, there is a link there.

5 And the issue I think for the Board to resolve, or one of
6 the key issues is how strong is that link between logic, the term logic
7 high voltage and Vcc, which one of ordinary skill in the art would
8 have understood to be the nominal power supply voltage for the chip.
9 And, Judge McKone, as you mentioned, for instance, a, a voltage that
10 would result in a logic one on a logic device.

11 JUDGE JEFFERSON: So back to my question, at least
12 in a different form, the written description does not use the term logic
13 high voltage in the '045 Patent; is that right?

14 MR. WRIGHT: It does not appear in the written
15 description supporting the claims. What does appear explicitly is Vcc.

16 JUDGE JEFFERSON: And at least in two of those
17 instances it says approximately Vcc or about Vcc, and it referenced at
18 least into the notion in the erase operation in column 6 of the patent; is
19 that right?

20 MR. WRIGHT: Of course, that's correct, in the context
21 of the erase, but the Patent Owner's construction, it's a nominal value
22 for Vcc. And I think in reality one of ordinary skill in the art would
23 recognize that we're never talking about precise voltages here. There
24 is always a nominal range for a voltage.

25 Nakai, itself, when you turn to Nakai --

1 JUDGE JEFFERSON: Well we'll get to Nakai --

2 MR. WRIGHT: Okay.

3 JUDGE JEFFERSON: -- but trying to get to your
4 construction, which says less than or equal to the nominal value for
5 Vcc.

6 MR. WRIGHT: Right.

7 JUDGE JEFFERSON: As part of the logic high
8 construction.

9 MR. WRIGHT: And the nominal, the nominal value
10 would necessarily have a range and --

11 JUDGE JEFFERSON: And we get to the word nominal
12 because we're tying that to the power supply for the particular flash
13 memory in question?

14 MR. WRIGHT: That's the one -- yes, yes. That's what
15 one of ordinary skill in the art would have understood.

16 And when you turn to the evidence in this case
17 supporting the Patent Owner's construction, we have two experts
18 whose qualifications are unchallenged and whom Toshiba chose not
19 to depose and challenge their testimony in that regard and who chose
20 not to submit any contradictory testimony in their reply.

21 What the evidence shows in this case, and I'm turning
22 now to slide 10 first in the context of Mr. Morales' declaration, it says
23 typically the logic states are described by two nominal voltage levels,
24 the higher of which corresponding to the power supply voltage, Vcc,
25 represents one in positive logic while the ground represents zero.

1 Mr. Morales also supported his declaration with another
2 textbook that said -- the Kang textbook and I've moved to slide 11
3 right now where it says using positive logic convention, the Boolean
4 logic value of one can be represented by a high voltage of Vdd.

5 Again, Vdd, Vcc, the nominal power supply voltage, one
6 of ordinary skill in the art understands those are synonymous,
7 synonymous terms.

8 Moving on to Mr. Berg's --

9 JUDGE McKONE: Well this doesn't say synonymous
10 here, this just says typically.

11 MR. WRIGHT: That supports our construction. That is
12 exactly what the goal is when you're looking to determine how one of
13 ordinary skill in the art would understand the term.

14 Absent some other unusual convention or absent some
15 other, something else contradicting that, one of ordinary skill in the art
16 would understand Vcc to be the logic high voltage.

17 And turning to Mr. Berg's declaration --

18 JUDGE McKONE: Why wasn't the term Vcc used in the
19 claims?

20 MR. WRIGHT: Well, again, if you --

21 JUDGE McKONE: If they're synonymous, why wasn't it
22 used in the claims? Why were different words chosen?

23 MR. WRIGHT: It is, Vcc is a term that was, that came
24 about as being the collector voltage which was the power supply for
25 logic devices using bipolar junction transistors.

1 Vdd, it evolved to Vdd which is, again, the drain side, the
2 power supply voltage for field effect transistors and in the future it
3 could have changed.

4 JUDGE McKONE: So these claims would not cover a
5 logic high voltage of Vdd; is that your position?

6 MR. WRIGHT: No, they, the term logic high voltage,
7 which is the term used in the claim, would be understood by ordinary,
8 one of ordinary skill in the art to be synonymous with either Vcc or
9 Vdd or the nominal power supply voltage because the term, if you,
10 that is the term that one of ordinary skill in the art would understand is
11 the term logic high voltage. It's a voltage that would, in a logic
12 device, result in a logic one and that changes with the technology as
13 Toshiba recognizes.

14 And what the evidence shows in this case, the weight of
15 the evidence, the preponderance of the evidence in this case shows
16 that one of ordinary skill in the art would understand the term logic
17 high voltage to be synonymous with Vcc, to be synonymous with
18 Vdd, to be what one of ordinary skill in the art would understand to be
19 the nominal voltage supply for, for a chip.

20 Nakai, itself, supports that construction.

21 JUDGE JEFFERSON: So before you get there, the, your
22 proposed construction is a positive voltage higher than logic low
23 voltage, and I'm quoting here, and less than or equal to the nominal
24 value for Vcc; am I hearing you say that what you really are saying is
25 less than or equal to the nominal value of the power supply of the chip

1 regardless of what it's called since your answer to Judge McKone was
2 it could be Vdd, it could be whatever the nominal value is?

3 MR. WRIGHT: Yes.

4 JUDGE JEFFERSON: So the proper construction here,
5 is it less than or equal to the nominal value for Vcc?

6 MR. WRIGHT: Yes, but because one of ordinary skill in
7 the art would -- I, what we were, what we were trying to achieve with
8 the claim construction -- the Board's preliminary construction is very,
9 very, very, very close, except that what Toshiba proposes is to
10 completely sever the link between the term logic high voltage and
11 Vcc. It says such as Vcc, but Toshiba wants you to ignore what one
12 of ordinary skill in the art would have understood is that it's
13 intrinsically linked to Vcc.

14 So in, in proposing a counter-construction, we're, we're,
15 we're moving it to make that, that link stronger and, in fact, that one of
16 ordinary skill in the art would understand the term logic high voltage
17 to be, to be capped at a nominal value for Vcc.

18 And it, and, in fact, the, even under the Board's
19 construction, preliminary construction, when you take that
20 construction and apply it to Nakai, you still don't, there's still no
21 anticipation. And that is explained and is a consistent theme running
22 through the Patent Owner's response. It doesn't exist solely in
23 footnote 7. Footnote 7 says as shown when you apply it, it's that.

24 So I certainly don't think that we ever relinquished or
25 meant to say that the Board needs, must adopt our construction.

1 Nakai still does not anticipate. And if I may turn to
2 Nakai now, or --

3 JUDGE McKONE: I have another question, though.

4 MR. WRIGHT: Yes, Your Honor.

5 JUDGE McKONE: If it was the patentee's intent here
6 not to limit itself to a particular technology and then, thus, didn't use
7 the terms Vcc or Vdd, why should we assume that the patentee
8 attempted to limit itself to the power supply of the chip, regardless of
9 what it was called, rather than other technology that might occur in
10 the future?

11 MR. WRIGHT: What -- so of course the patentee -- the
12 patents and the claims are, must be read according to one of ordinary
13 skill in the art. That's, that's undisputed.

14 And the patentee is entitled to use terms and did use a
15 term here that the patentee felt would convey to one of ordinary skill
16 in the art just, just that concept, that we can program, or at least for the
17 program inhibit portion of a programming operation, we can achieve
18 that with the logic high voltage. That is whatever the nominal power
19 supply is for the chip that you, that you would use to operate all the
20 logic devices on that chip.

21 But as Toshiba recognizes, we're not dealing with logic
22 devices here, we're dealing with a flash memory. And the beauty of
23 this invention, and I've put up slide 19, which is Nakai's method for
24 programming, the beauty of this invention is that you could use,
25 instead of these higher boosted program inhibit voltages, which is the

1 Vpi that is applied, the 10 volt Vpi that's applied to the unselected
2 word lines, the 10 volts, the Vdpi that's applied to the unselected bit
3 lines, and the even higher 12 volt is applied to the, to the bit select
4 line, instead of using these boosted positive voltages, we can achieve
5 the program inhibit portion of a programming operation on a flash
6 memory array using the logic high voltage for the chip, the nominal
7 power supply voltage for the chip, the voltage that causes a logic one
8 to, to be in a logic device.

9 JUDGE JEFFERSON: And where is that, support for
10 that found in the specification?

11 You say it's, in essence it's limited, the improvement is
12 that the select lines can be used only on the nominal power supply,
13 where is that found in this, where do you find support for that in the
14 spec?

15 MR. WRIGHT: Well the programming -- so the claim
16 set up the programming scheme for this flash memory array.

17 I've moved to slide, to slide 9 which has a table one and it
18 shows the programming scheme as being, having Vcc applied to the
19 unselected word lines, the unselected bit line and the bit line select
20 transistor.

21 And then, again, in the, the programming portion of the
22 specification that Judge Turner pointed to, it's using Vcc. And it
23 shows that there, that that, what one of ordinary skill in the art, what
24 the patentee, in fact, understood here was that when it used the term

1 logic high voltage in the, in the vernacular of 1996, that was, that was
2 Vcc.

3 Now it's supported additionally, and again, by the clear
4 weight of the evidence in this case, by the Patent Owner's two experts.

5 It's also supported by Nakai, itself.

6 So Nakai, and I'm turning to slide 15 right now, Nakai
7 has a Vcc and it is described as being five folds and it is described in
8 the context of a power on reset operation for Nakai's chip.

9 Now a power on reset operation is the operation that
10 allows a voltage supply, a nominal voltage supply going to the chip to
11 reach a, to ramp up and reach its nominal value, which here is 5 volts,
12 plus or minus 10 percent before the logic devices are allowed to begin
13 operating, otherwise you may get nonsensical results.

14 So Nakai specifically identifies its Vcc as being 5 volts,
15 its nominal power supply as 5 volts, plus or minus 10 percent.

16 Now --

17 JUDGE McKONE: So what is it called, this Vcc value,
18 do they call this Vcc value a logic high voltage?

19 MR. WRIGHT: It refers to it as, as Vcc and this
20 operation shows that that --

21 JUDGE McKONE: Is that a no to my question?

22 MR. WRIGHT: The term logic high voltage is not in
23 Nakai, if that was the question.

24 JUDGE McKONE: Okay.

25 MR. WRIGHT: So --

1 JUDGE McKONE: That was my question. Thank you.

2 MR. WRIGHT: So when you turn to, even under
3 Toshiba's construction and you say, and you apply that to Nakai and
4 say it's a, the logic high voltage is a voltage higher than the logic low
5 voltage, such as Vcc, if you apply that to Nakai, what you end up with
6 is Vcc being at 5 volts and the rest of the programming voltages for,
7 for Nakai, I'm turning to slide 20 now, but also, but also slide -- so
8 first slide 19, so Nakai is applying these boosted positive voltages,
9 these program inhibit voltages to the unselected word lines.

10 And those voltages, I'm turning now to slide 21, are
11 generated on chip in Nakai and they're shown, if you look at slide 21,
12 which is Figure 26 of Nakai, it has a Vpp, its programming voltage, its
13 boosted positive voltage and then these other boosted voltages that are
14 generated on chip from the voltage generator circuit of Vpi, a program
15 inhibit voltage, and Vdpi, the drain program inhibit voltage, those are
16 boosted on chip and what one of ordinary skill in the art would
17 understand is that they're boosted above Nakai's nominal power
18 supply voltage, Nakai's Vcc, Nakai's logic high voltage, which is 5
19 volts.

20 So it is unreasonable to take even the Board's
21 construction, which says logic high -- a voltage greater than logic low
22 voltage, such as Vcc, and when you apply that to Nakai, those 10 volts
23 and 12 volts are not voltages such as Vcc. The, the program inhibit
24 voltage is 10 volts, it's double Vcc. It's boosted above Vcc. And the
25 12 volts is boosted 2 volts beyond that.

1 JUDGE JEFFERSON: Let's, counsel, and in this patent,
2 in the '045 Patent, where do I find support for the fact that you can't
3 use boosted voltages above Vcc for your programming erase and other
4 operations?

5 MR. WRIGHT: Well the, the, what -- well, for one
6 thing, the claims say that unselected word lines receive logic high
7 voltage and the only embodiment that's described in the specification
8 is set forth in table one, which has Vcc as being that logic high
9 voltage that is applied to unselected word lines, unselected drain lines,
10 the bit line select transistor.

11 JUDGE JEFFERSON: So if I found a, so if I, if there
12 was some reference hypothetically in the spec that Vcc was whatever
13 your circuit uses for setting those lines, i.e., it's a range as long as it's
14 the, you're using the same voltages at those unselected bit lines or and
15 -- I believe the transistor select, as long as you're using the same one,
16 it doesn't matter what it is as long as it's whatever you're calling it, you
17 decide to do -- you call it the Vcc at that particular operation?

18 MR. WRIGHT: As long as it's the logic high voltage for
19 that particular device, which would be, which one of ordinary skill in
20 the art would understand as being Vcc or maybe it's Vdd, but,
21 whatever the nominal power supply voltage here, as in Nakai, 5 volts
22 for its power on reset operation.

23 JUDGE JEFFERSON: This might be imprecise, but, so
24 what I'm saying is why is it tied then to -- my next question would be
25 why is it tied to the power supply if the nominal power used for that

1 operation is Vcc plus 5, for example? Why isn't that then the standard
2 nominal voltage that we can then label Vcc again for the operation?

3 Why does it have to be tied to the nominal power supply
4 in the circuit, in part because there is no power supply discussed in the
5 specification, presumably, then whatever your NAND flash memory
6 is, uses for that operation is, as your power supply to Vcc is what it is,
7 if I boost it and call it Vcc plus 5, why wouldn't that suffice for those
8 claims?

9 MR. WRIGHT: So, so the '045 specification does
10 discuss the notion of Vcc being a, it does discuss power supply
11 voltages, and that's in column 2 at line, it looks like 13. It says that
12 the source terminal connects to the positive power supply voltage
13 typically 3 to 5 volts. It allows the source junction to be the same size
14 as the drain function.

15 We do give at least one example of what the power
16 supply voltage is there.

17 And, so I'm, maybe I'm not understanding the question.
18 It's kind of, it's fled from me again, I'm sorry.

19 JUDGE JEFFERSON: No, I think I'm asking it
20 imprecisely.

21 So I'm trying to get into the fact that you keep tying it to
22 the nominal power supply of the circuit and you admit that this power
23 supply is off chip, or at least it's not shown, certainly not claimed in
24 the claims and not discussed beyond this particular portion of the

1 specification; is that right, the power supply specifically for this
2 circuit?

3 MR. WRIGHT: That's right.

4 JUDGE JEFFERSON: So, when I get to the circuit, I'm
5 looking at the claims, whatever is used for programming erase or
6 whatever operations, it could be Vcc plus 5, I could presumably boost
7 it, but you're saying that the spec in this case prohibits us from doing
8 that, it has to be whatever is the nominal power supply for the circuit,
9 period. It's limited to that.

10 MR. WRIGHT: I think what the, what the proposed
11 construction that the Patent Owner is urging is that it is a nominal --
12 perhaps if I put the construction up, that might help us.

13 Can I have the, just the slide, Toshiba's slide that has the
14 two constructions. So --

15 JUDGE JEFFERSON: So we're looking at Toshiba slide
16 number?

17 MR. WRIGHT: This is Toshiba slide number 8, it has
18 both of the party's constructions on it.

19 So the Patent Owner's construction is a positive voltage
20 higher than logic low voltage and, again, what we're trying to achieve
21 there is a more defined -- a link between logic high voltage and Vcc,
22 again, what one of ordinary skill in the art would understand as Vcc,
23 synonymous with Vdd and the power supply voltages, make that link
24 stronger.

1 So it's the nominal value for Vcc is, is what we chose in
2 this proposed construction to make that link. The issue is does that
3 link, is that link meaningful or is that link meaningless.

4 Well the term logic high voltage, one of ordinary skill in
5 the art, as the evidence shows in this case, would understand that link
6 to be a strong link. You can't, you can't read out the term logic out of
7 high voltage. It's going to be the nominal voltage level that causes the
8 logic devices on that chip to work.

9 And that was the beauty of the invention, really.

10 JUDGE JEFFERSON: And then, so in this case, if I find
11 a circuit whose logic high voltage that causes the transistors on that
12 circuit to work Vcc plus 5, would that fall within the claims?

13 MR. WRIGHT: Would that fall into logic high voltage?

14 JUDGE JEFFERSON: Yes.

15 MR. WRIGHT: I think it might under that hypothetical.
16 I'd have to think about that a little bit, but I think it might. That's, that
17 is consistent with the term logic high voltage, at least.

18 So, so for Nakai to anticipate, anticipation requires
19 identity of invention. Nakai has to disclose an identical scheme for
20 managing a flash memory array during programming that, that's
21 disclosed and claimed.

22 Nakai does not use a logic high voltage on its unselected
23 word lines. Nakai does not use a logic high voltage on its bit select
24 line. Nakai does not use a logic high voltage on its unselected bit
25 lines.

1 This is where the two methods for programming crucially
2 diverge under either construction.

3 The boosted, the boosted voltages in Nakai, I'm putting
4 up right now slide 20, the program inhibit for the word lines, Vpi, the
5 program inhibit for the drain lines, Vdpi, and the bit select control line
6 at 12 volts, those are not voltages higher than Nakai's logic high
7 voltage such as Vcc. They're vastly different from that. They're
8 double Nakai's logic high voltage. They're double Nakai's Vcc,
9 double plus 2 volts in one instance.

10 So under either, either construction, that link cannot
11 reasonably be ignored, the link between logic high voltage and Vcc
12 and what one of ordinary skill in the art at the time would have
13 understood.

14 If you take the evidence in this case and put it on a set of
15 scales and you have one paragraph in Mr. Murphy's declaration -- let
16 me point out that Mr. Murphy did not appear to recognize, that Nakai
17 actually disclosed the value for Vcc as being 5 volts and that's in his
18 deposition testimony and that's also on slide 22.

19 If, if Mr. Murphy had recognized that Nakai actually had
20 a Vcc and it was set to 5 volts, he might have applied the Board's
21 preliminary construction differently or Toshiba's proposed
22 construction differently.

23 So under, under any construction, Nakai does not
24 disclose an identical method for programming a flash memory array.

1 A couple of additional points. Again, throughout
2 Toshiba's entire presentation Toshiba does not discuss and did not
3 even appear to recognize that we have to construe these terms as one
4 of ordinary skill in the art would understand these terms.

5 And, again, the weight of the evidence in this case, the
6 preponderance of the evidence in this case sits squarely in the Patent
7 Owner's favor.

8 Again, the Patent Owner was not swinging for the fences
9 when he chose the term logic high voltage. That's the term that best
10 represents what the Patent Owner was trying to achieve.

11 I can achieve the program inhibit operations with a lower
12 voltage. Well how am I going to describe that lower voltage; am I
13 going to pick a colloquial term that, you know, when you dig down
14 into it was confined to a particular technology, like Vcc or Vdd; no.

15 Am I going to pick a power supply voltage? Well, I
16 recognize that these chips, especially early on, had multiple power
17 supply voltages.

18 So the term that I choose to use, and, you know, looking
19 back, hindsight is 20/20. Maybe if the Patentee could have looked
20 forward to 2014 and peered in to this Courtroom, he might have done
21 it differently. But at that time it was reasonable for him to select a
22 term logic high voltage that the inventor felt would convey to one of
23 ordinary skill in the art that I'm using a lower voltage here on chips
24 that aren't even logic chips.

1 JUDGE McKONE: So it's your position that at the time
2 the, of the filing of the patent, chips could have multiple different
3 power supplies? Because that's what you just said, isn't it?

4 MR. WRIGHT: I think early on that was understood. I
5 think Mr. Berg explains this in his, in his declaration how one of the
6 steps forward --

7 JUDGE McKONE: Why do we now want to limit this to
8 one of those particular power supplies?

9 MR. WRIGHT: Well, because that's what the term logic
10 high voltage would convey to one of ordinary skill in the art.

11 The, the voltage for that chip that causes the logic
12 devices on that chip, again, we're not applying this in the flash
13 memory array to logic devices, we're applying it to word lines, to
14 floating gate transistors during the program inhibit portion of an
15 operation, but he's saying I can achieve that, I can achieve that with a
16 lower voltage. How am I going to convey that lower voltage; well,
17 I'm going to say it's the logic high voltage.

18 JUDGE JEFFERSON: Counsel, may I just, correct me if
19 I'm wrong, my understanding is that the quote I can achieve that with
20 a lower voltage, the support for that being capped at Vcc or lower is
21 found in the examples at the table one and the programming
22 discussion in column 7 --

23 MR. WRIGHT: Yes.

24 JUDGE JEFFERSON: -- of the '045 Patent using Vcc.

1 It doesn't say, there's nowhere else in the specification or
2 the written description, if I'm correct, that says I can achieve that
3 using a lower voltage because you don't need to use a higher voltage
4 than nominally Vcc?

5 MR. WRIGHT: That's what's in the intrinsic evidence.

6 The extrinsic evidence, which is a vital piece of the
7 evidence here and which is not inconsistent in any way with the patent
8 specification shows that one of ordinary skill in the art would have,
9 would have understood that to be, that the term logic high voltage to
10 be as described in the specification Vcc.

11 JUDGE JEFFERSON: While we're on at least the logic
12 high voltage being less than, am I just right in understanding that per
13 your construction that there is no lower bound on how low the voltage
14 logic high can be?

15 It says less than or equal to I believe in your construction,
16 proposed construction of Vcc, nominal value of Vcc?

17 MR. WRIGHT: To answer that question I'm also putting
18 up slide 12, which is the Weste textbook which Mr. Berg selects --
19 cites to.

20 So that is not a, a distinction that really is dispositive in
21 this case and it's not a distinction that the Patent Owner was focused
22 on in proposing a claim construction.

23 But when you look, for instance, at the Weste textbook,
24 we see that there is a, a range for the logical, the logical high input
25 range, the logic high voltage, there is a range there where you get a

1 logic one or a logic device. There is a range for logic low; and I think
2 one of ordinary skill in the art would understand that there's a range in
3 there where logic devices aren't -- are going to be in an indeterminant
4 state, or at least not work as designed.

5 So that range, however, is capped at the nominal power
6 supply voltage for that, for that chip and below.

7 So I think that forms the support for the Patent Owner's
8 construction and perhaps answers that, that question.

9 JUDGE JEFFERSON: And in, you said earlier when we
10 were talking about NAND flash devices which are not expressly, you
11 know, logic devices in the typical sense.

12 MR. WRIGHT: That's correct.

13 JUDGE JEFFERSON: Okay.

14 MR. WRIGHT: That's correct.

15 But in the, the beauty of this invention is that you can
16 achieve the program inhibit operation using a logic high voltage
17 instead of one that's boosted above that as Nakai does in its program
18 inhibit voltages.

19 JUDGE TURNER: Counsel, I think you spoke about the
20 fact that maybe the inventor didn't have the presence to understand
21 that maybe logic high voltage may cause this problem, but let me be
22 so bold to suggest that maybe Patent Owner has the ability, which
23 they haven't used, they could file a motion to amend and they could
24 take away this issue completely, so they could say instead of saying
25 logic high voltage, they could say power supply voltage, which you've

1 already sort of argued probably was written description support, so
2 why not amend and remove this confusion and take away this case
3 from us?

4 MR. WRIGHT: It's the Patent Owner's position that
5 there's no, there's no need to amend claims here.

6 The term logic high voltage, as the preponderance of the
7 evidence shows in this case, reasonably conveys to one of ordinary
8 skill in the art exactly what the Patent Owner meant.

9 JUDGE TURNER: And how are we, and I guess as a
10 follow-up question, how do we get to this extrinsic evidence?

11 Seems like Patent Owner has cited quite a bit of it, but
12 Phillips seems to instruct, you know, this panel that if we look at the
13 claim when we look at the specification and we really don't think
14 there's anything inconsistent and we say well here's what the claim
15 term means, we don't have to look at any extrinsic evidence if it's
16 clear, do we?

17 MR. WRIGHT: I don't think that's quite what Phillips
18 stand for. I think when Phillips, Phillips talks about different classes
19 of evidence that can be used for claim construction and of course the
20 strongest evidence is the intrinsic evidence.

21 But there is a class of evidence, extrinsic evidence that is
22 perfectly valid and can and should be used to help, to help the
23 adjudicator here determine how one of ordinary skill in the art would
24 have understood a claim.

1 And what Phillips warns us against with respect to
2 extrinsic evidence is that if the extrinsic evidence conflicts with or
3 contradicts the intrinsic evidence, that's forbidden. But that's not the
4 case here. There's nothing in Berg's testimony or Mr. Morales'
5 testimony, there's nothing in the three textbooks that is in any way
6 inconsistent with what is shown in the intrinsic evidence.

7 JUDGE TURNER: Okay. Other than the fact that
8 you're, and I'm, I am slightly confused because at one hand you're sort
9 of saying maybe we should have chosen a better term, logic high
10 voltage maybe is subject to maybe multiple interpretations, then on
11 the other hand you're sort of saying, well, really based on one of
12 ordinary skill in the art would have known at the time that this was
13 filed, it really only has one meaning.

14 So I'm, maybe it feels like a mixed message that you're
15 not giving me; maybe that's just how I'm hearing it.

16 MR. WRIGHT: Possibly. I'm not sure what the mixed
17 message, the mixed message is, Your Honor.

18 JUDGE TURNER: So what, what would logic high
19 voltage be understood in the context of the specifications?

20 It seems like it talks about what it can be, but it doesn't
21 limit it to that?

22 So it seems like our construction that it may be Vcc,
23 seems like that comports really quite well with what's in the
24 specification.

1 MR. WRIGHT: It may. The Patent Owner submits and
2 what the weight of the evidence shows is that it's a stronger link than
3 maybe Vcc, but again, even under that preliminary construction such
4 as Vcc, when you apply that to Nakai where Vcc is shown -- where
5 Nakai's logic high voltage, Nakai's Vcc is shown to be 5 volts, even
6 when you apply the Board's preliminary construction, those program
7 inhibit voltages of 10 volts and 12 volts are not voltages such as Vcc,
8 they're double Vcc or more than double Vcc.

9 JUDGE TURNER: I'll let you, I'll let you go on with
10 your presentation.

11 MR. WRIGHT: I'm nearing the end of my presentation,
12 Your Honor.

13 I wanted to see if there are other notes that I took with
14 respect to rebuttal.

15 It, it is the Patent Owner, one of Toshiba's themes is that
16 we're saying, we are ascribing a numerical value to Vcc that -- sorry, a
17 numerical value to logic high voltage; that is not the case, we've never
18 proposed a numerical value for that voltage. It is a, a range of
19 voltages around the nominal value for Vcc.

20 JUDGE JEFFERSON: But per your understanding as
21 supported by the spec and one of ordinary skill in the art, it can't be a
22 boosted nominal value?

23 MR. WRIGHT: It, a value that's boosted above the logic
24 high voltage would not be a logic high voltage.

1 Absent any further questions, Your Honor, I'll relinquish
2 the remainder of my time.

3 JUDGE TURNER: I don't have any more questions.

4 JUDGE McKONE: Nothing further from me.

5 MR. WRIGHT: Thank you.

6 JUDGE JEFFERSON: Thank you.

7 MR. LIMBACH: So I have a few comments on some of
8 the things that were said.

9 One thing that was not said is broadest reasonable
10 construction, they never used the words because they didn't apply it
11 and they're kind of dancing around it by saying well this is how one of
12 ordinary skill would read it, but they didn't say it because if they got
13 in to that argument, or if they made that point, they'd have to admit
14 whether or not they've applied it or not.

15 Now they're trying to tie logic high voltage to logic
16 device. They're saying that a logic high is a voltage that will operate a
17 logic device up to a one. Okay.

18 But if you look at their slide 20, and I'm, under their
19 construction they agree that the logic high voltage can be Vcc but can
20 go all the way down to just above logic low. In other words, it can go
21 right above the logic low.

22 So under their construction, they're trying to tie it to logic
23 devices, but that voltage would not be sufficient to operate a logic
24 device.

1 So their construction admits the fallacy, the construction
2 admits the fallacy of their argument. They can't tie it to a logic device
3 and then say but I'm just going to make a cap and it can be anything
4 lower all the way close to zero. Well that's not tied to a logic device,
5 that wouldn't operate a logic device.

6 The other fallacy is if you go slightly above Vcc, you'd
7 still operate the logic device.

8 Table 1 where it shows Vccs, those are examples. It
9 doesn't say these are all caps. It doesn't say these are all minimums.
10 It just says these are values, just a value.

11 And what's interesting is they don't say well we're going
12 to tie it to that value, we're going to say that the logic high is Vcc.
13 They admit it can go all the way down so there's a range. Table 1 is
14 not a list of caps. It's just a value that can be used.

15 And there's nothing in the specification that says that any
16 of those values are caps. As a matter of fact, twice the patent says the
17 opposite, it says it can be about Vcc, it suggests it can be higher. It
18 can be as low as Vcc, it's teaching that it can be higher.

19 Another point is they're saying well, no, we've got to lock
20 in this logic high voltage to Vcc, a voltage, it's a specific voltage, it's
21 got to be capped. If you look at the claim, it doesn't say a logic --
22 apply a logic voltage to this line and then apply the logic voltage to
23 this line and apply the, it says apply a logic voltage, apply a logic
24 voltage, apply a logic voltage. There is no one logic voltage.

1 They purposefully drafted the patent so that the voltages
2 didn't need to be the same, exactly the same. So there is no one logic
3 voltage here, and that's in the claim.

4 Now I think what I heard is he said, counsel for I.V. said,
5 well, logic high voltage can be Vcc, it can be Vdd or it can be the
6 nominal power supply voltage. I believe that's what he said and you
7 can go back and check the record.

8 That's not their construction. Their construction is a
9 nominal power supply for Vcc, but yet he says but Vdd is still
10 covered. Well that's not what their construction says.

11 The other thing is they're not tying logic high voltage to
12 Vcc. They're tying a cap for that voltage at Vcc. That's -- they're
13 disassociating, and as their slide 20 shows, it can be lower.

14 Now there was another point that, well, Mr. Murphy in
15 his, in his declaration and in his deposition didn't recognize Vcc, he
16 didn't -- in Nakai, he didn't even look at it. That's because back at that
17 point in the, in the proceeding they hadn't given us their construction.
18 We had no idea they were trying to put a cap on it.

19 So they're really kind of being unfair, they're saying well,
20 you know, Mr. Murphy didn't address our construction. He didn't
21 have it yet; so that was a little unfair.

22 They talk about the weight of the evidence. The weight
23 of the evidence is on their side. Well, the evidence here is the
24 broadest reasonable construction based on intrinsic evidence, that's
25 what we're arguing.

1 They're not using that construction standard and they're
2 relying solely on external evidence, extrinsic evidence. So the weight
3 of the evidence, and you rightfully pointed out, Your Honor, that, you
4 know, Phillips says, look, you look to the patent first and only if
5 there's an ambiguity can you even consider extrinsic evidence.

6 Now they said, well, but we've got this extrinsic evidence
7 and it doesn't contradict anything; it's completely consistent. That's
8 false. The patent twice says the logic high voltage can be higher than
9 Vcc. Their extrinsic evidence is not consistent with the intrinsic
10 evidence, it's contradictory.

11 JUDGE JEFFERSON: Counsel, I believe Patent Owner's
12 argument there was also that nominal in their claim construction, it
13 takes account of the fact it could be slightly higher or slightly lower
14 than Vcc, that the term nominal is used; and what's your response to
15 that?

16 MR. LIMBACH: How -- okay, so nominal, so now
17 they've got this little hedge and they're going to say that that somehow
18 subsumes about, somehow subsumes can be as low as; I don't think
19 so. I don't think that their construction for nominal gets it.

20 Now if you look at, if you go back to their slide number
21 12, they're relying on these, this external evidence on logic devices,
22 not memory cells, showing a logic high and the logic low.

23 Notice that there's a gap between them? There's a gap
24 between logic high and logic low. That's inconsistent with their
25 construction. Their construction is that logic high can go all the way

1 down to logic low, so their extrinsic evidence doesn't even support
2 their construction.

3 And lastly I'd like to go back to their slide number 20.
4 Now this is a slide that they have argued a lot about, it's in their
5 papers, it was argued on the screen. Let's just look, this is the way
6 that, this is all designed, you've got this demarcation, you've got Vcc
7 and even though there's nothing in the patent that says you can't go
8 above Vcc, they're saying it should be capped and then this is what
9 you get.

10 This figure is wrong. This is not how their construction
11 reads. Logic high voltage, the lower range, is accurately depicted. It
12 goes from just above logic low all the way up to Vcc under their
13 construction.

14 But boosted positive voltage is not defined in the adopted
15 construction, so they haven't challenged. It's not tied to Vcc, it's tied
16 to logic high voltage.

17 So if you pick a logic high voltage here that's, say, two
18 and a half volts, half of Vcc, that means the boosted positive voltage
19 can be down to just above logic high voltage. It can be half of Vcc.

20 So again, this Vcc number they're throwing in there is
21 completely arbitrary. There's a reason that they put a line there, it's to
22 try and save their patent over Nakai, but it, it's not tied to the patent.
23 It's not how one of ordinary skill in the art would read this patent.

1 And there's nothing in the patent that says that the
2 voltage in the table are caps. To the contrary, those are examples and
3 there's two instances where it says that you can be above it.

4 So we believe that the adopted constructions are as
5 precise as the patent allows and should be maintained.

6 Thank you.

7 JUDGE JEFFERSON: Before we let you go, were there
8 any questions from the panel?

9 JUDGE McKONE: I don't have any.

10 JUDGE TURNER: I don't have any.

11 JUDGE JEFFERSON: Thank you.

12 The case that -- we are adjourned. The case shall be
13 submitted. We're adjourned.

14 (Concluded at 11:37 a.m.)

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