

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TOSHIBA CORPORATION, TOSHIBA AMERICA, INC.,
TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC.,
and TOSHIBA AMERICA INFORMATION SYSTEMS, INC.,
Petitioner,

v.

INTELLECTUAL VENTURES I LLC,
Patent Owner.

Case IPR2014-00113
Patent 6,058,045

Before KEVIN F. TURNER, TREVOR M. JEFFERSON,
and DAVID C. McKONE, *Administrative Patent Judges*.

JEFFERSON, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

A. Background

Toshiba Corporation, Toshiba America, Inc., Toshiba America Electronic Components, Inc., and Toshiba America Information Systems, Inc. (collectively, “Petitioner”) filed a Petition (Paper 1, “Pet.”) to institute an *inter partes* review of claims 1 and 4 of U.S. Patent No. 6,058,045 (Ex. 1001, “the ’045 patent”). *See* 35 U.S.C. § 311. Intellectual Ventures I LLC (“Patent Owner”) filed a Preliminary Response (Paper 10, “Prelim. Resp.”). Pursuant to 35 U.S.C. § 314, in our Decision to Institute (Paper 13, “Dec.”) we instituted this proceeding as to claims 1 and 4 of the ’045 patent.

Patent Owner filed a Patent Owner Response (Paper 20, “PO Resp.”) and Petitioner filed a Reply to the Patent Owner Response (Paper 21, “Reply”). An oral hearing in this matter was held on November 6, 2014 (Paper 28, “Tr.”).

We have jurisdiction under 35 U.S.C. § 6(c). This is a final written decision under 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73 as to the patentability of the challenged claims. For the reasons that follow, Petitioner has demonstrated by a preponderance of the evidence that claims 1 and 4 of the ’045 patent are unpatentable.

B. Related Matters

Patent Owner has sued Petitioner for infringement of the ’045 patent in *Intellectual Ventures I LLC v. Toshiba Corp.*, No. 1:13-cv-00453 (D. Del.), filed on March 20, 2013. Pet. 1; Paper 7 (Patent Owner’s Mandatory Notices).

C. The '045 Patent

The '045 patent, titled “Serial Flash Memory,” issued on May 2, 2000, and claims the benefit of a provisional application dated September 9, 1996. Ex. 1001, at [45], [60], [62]. The '045 patent discloses a “scaleable flash memory cell structure and method of manufacture that improves data retention, increases capacitive coupling and speed of operation, and improves reliability.” *Id.* at 2:39–42. “The flash cell of the ['045 patent] permits implementation of arrays of flash memory cells that allow the designer to program and/or erase individual bytes of memory as well as blocks of memory.” *Id.* at 2:44–46. Figure 4 of the '045 patent, shown below, provides the exemplary memory array circuit disclosed.

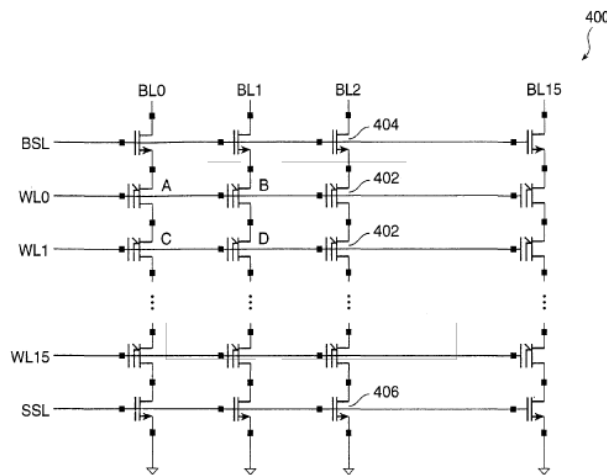


FIG. 4

Figure 4 depicts “a circuit schematic for an exemplary memory array made of flash cells.” *Id.* at 3:25–26. The disclosed memory array 400 in Figure 4 includes columns of serially connected flash memory cells located at the intersection of bit lines (BL0–BL15) and word lines (WL0–WL15). *Id.* at 6:22–28. Bit select control line (BSL) controls gate terminals of bit select

transistors 404, which couple bit lines to memory cells. *Id.* at 6:30–31. Source select control line (SSL) controls gate terminals for source select transistors 406, which couple ground to memory cells. *Id.* at 6:31–32.

Table 1 of the '045 patent, reproduced below, provides a biasing scheme that discloses voltages that are applied to lines of the array to perform program, read, or erase operations for selected or unselected portions of the array.

TABLE I				
Control Line	Erase	Program	Read	Condition
BSL	V _{cc}	V _{cc}	V _{cc}	Selected
SSL	V _{ss}	V _{ss}	V _{cc}	Selected
BLO	V _{cc}	V _{ss}	1.0–1.4V	Selected
BL1	V _{ss}	V _{cc}	0.5V	Unselected
WL0	V _{cc}	V _{cc}	V _{cc}	Unselected
WL1	–12 to –15V	15–20V	V _{ss}	Selected

Id. at 6:37–45. Table 1 provides an example of a biasing scheme for an individual cell, showing voltages applied to various control lines (i.e., V_{cc}, V_{ss}, etc.), and the desired function (erase, program, or read) for the selected or unselected portions of the array. *Id.* at 6:48–56.

D. Challenged Claims

Challenged claims 1 and 4 are reproduced below:

1. An array of flash memory cells comprising:
 - a plurality of columns of serially connected flash memory cells, each memory cell having a gate terminal;
 - a plurality of bit lines respectively coupled to drain side of said plurality of columns of memory cells via a respective plurality of bit line select transistors, said plurality of bit line

- select transistors having gate terminals coupled to a bit line select control line;
 - a plurality of word lines, each one coupling to a gate terminal of one memory cell in each of said plurality of columns to form rows of memory cells with common gate terminals; and
 - a plurality of source select transistors respectively coupling a source side of said plurality of columns of memory cells to a logic low voltage, and having gate terminals coupled to a source select control line,
- wherein, during programming:
- a logic high voltage is applied to said bit line select control line to turn on bit line select transistors,
 - a logic low voltage is applied to source select control line to turn off source select transistors;
 - a logic low voltage is applied to a selected bit line while a logic high voltage is applied to unselected bit lines, and
 - a logic high voltage is applied to unselected word lines, while a boosted positive voltage is applied to a selected word line.

4. A method of operating a flash memory device wherein programming memory cells is accomplished by the steps of:
 - applying a logic high voltage to a bit line select control line to turn on bit line select transistors,

applying a logic low voltage to a source select control line to turn off source select transistors;

applying a logic low voltage to a selected bit line while a logic high voltage is applied to unselected bit lines, and

applying a logic high voltage to unselected word lines, while a boosted positive voltage is applied to a selected word line.

E. The Asserted Ground

Petitioner contends that the challenged claims are unpatentable based on the following ground, upon which we instituted (Dec. 14; Pet. 13–29):

Reference	Basis	Claims Challenged
Nakai ¹	35 U.S.C. § 102(b)	1 and 4

II. ANALYSIS

A. Claim Construction

The Board interprets claims of an unexpired patent using the broadest reasonable construction in light of the specification of the patent in which they appear. *See* 37 C.F.R. § 42.100(b). Claim terms generally are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

¹ U.S. Patent No. 5,297,029, issued on Mar. 22, 1994 (filed on Dec. 18, 1992) (Ex. 1005, “Nakai”).

1. “logic high voltage” (claims 1 and 4)

Claims 1 and 4 recite “logic high voltage” as a claim limitation. We preliminarily construed “logic high voltage” as a positive voltage higher than logic low voltage, such as Vcc. Dec. 8.

Patent Owner contends that Petitioner’s proposed construction, which we agreed with for purposes of the Decision to Institute, is incorrect. PO Resp. 10–12. Patent Owner contends that, properly construed, “[o]ne of ordinary skill in the art would understand that a ‘logic high voltage’ would be less than or equal to the nominal value of the memory array’s power supply, or what one of skill in the art would recognize as ‘Vcc.’” PO Resp. 12 (citing Declaration of Louis J. Morales, Ex. 2001 ¶¶ 25–33, 39; Declaration of John E. Berg, Ex. 2002 ¶¶ 27–32.) Thus, Patent Owner argues, “a proper construction of ‘logic high voltage’ is ‘a positive voltage higher than logic low voltage **and less than or equal to the nominal value for Vcc.**” PO Resp. 12.

Patent Owner argues that Petitioner’s support for its proposed construction should be given little or no weight because Petitioner’s expert lacks NAND flash memory experience and is not a person of ordinary skill in the art. PO Resp. 10. In addition, Patent Owner contends that Petitioner’s proposed constructions, which define the terms relative to each other—“logic low voltage” < “logic high voltage” < “boosted positive voltage”—result in imprecise terms without clear demarcations between the various claimed voltages. PO Resp. 10–11 (citing Ex. 2002 ¶¶ 27–30).

Patent Owner supports its proposed construction by arguing that it was common in the art for “the memory devices disclosed in the ’045 patent (and also in Nakai) [to] have a nominal power supply that is referred to as

‘Vcc.’” PO Resp. 13 (citing Ex. 2001 ¶¶ 24–33, 39; Ex. 2002 ¶¶ 21–23). Patent Owner argues that because a boosted positive voltage is higher than nominal power supply voltage Vcc, the nominal power supply voltage provides “the only principled and precise dividing line between a logic high voltage, and the higher voltages that are boosted over Vcc.” *Id.* The only support Patent Owner cites from the ’045 patent is found in Table 1, which shows a “logic high voltage” that is not higher than power supply voltage Vcc. PO Resp. 13 (citing Ex. 1001, Table 1).

We disagree with Patent Owner’s contention that “logic high voltage” is limited by the nominal power supply voltage Vcc. Claims 1 and 4 recite voltages in relative terms to each other, using the terms “logic high voltage” and “logic low voltage” that do not appear in the written description of the ’045 patent and only appear in the claims. *See generally* Ex. 1001. Although Table 1 of the ’045 patent contains references to Vcc, neither the claims nor the specification indicate that the written description limits logic high voltage to Vcc.² Indeed, we do not find that the entries in Table 1 or any other portion of the ’045 patent written description show a clear intention to limit the scope of logic high voltage in claims 1 and 4 to Vcc.

² The Federal Circuit has stated that “while the specification [should be used] to interpret the meaning of a claim, courts must not import[] limitations from the specification into the claim.” *In re Trans Texas Holdings Corp.*, 498 F.3d 1290, 1299 (Fed. Cir. 2007) (alterations in original) (citations omitted). The scope of a claim is restricted to a disclosed embodiment only when “the patentee has demonstrated a clear intention to limit the claim scope using words or expressions of manifest exclusion or restriction.” *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004).

Patent Owner's proffered testimony that refers to the common understanding of Vcc as "the primary positive supply voltage to an IC" (Ex. 2001 ¶ 25) neither provides an explicit definition for the term "logic high voltage," nor expressly limits the term "logic high voltage" to Vcc. Accordingly, we disagree with Patent Owner's conclusion that the term "logic high voltage" is linked intrinsically to Vcc such that it should be capped by Vcc. *See* Tr. 30:24–25 ("the term logic high voltage is linked [] intrinsically to Vcc"), 35:13 ("intrinsically linked to Vcc").

We also agree with Petitioner (Reply 7–8) that Patent Owner's claim construction arguments and testimony overlook the requisite standard of the broadest reasonable construction in light of the specification of the patent (*see* 37 C.F.R. § 42.100(b)), in an attempt to narrow the construction of "logic high voltage" to be nominally equal to or lower than Vcc (PO Resp. 12; Ex. 2001 ¶ 32). The intrinsic evidence in the '045 patent does not support limiting the "logic high voltage" to Vcc, as it expressly states that programming voltages may vary. Ex. 1001, 6:53–55 (describing voltage as "about Vcc").

Claim terms generally are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *See In re Translogic Tech., Inc.*, 504 F.3d at 1257. We are unpersuaded, however, by Patent Owner's arguments (PO Resp. 12; Tr. 34:6–19) that seek to limit "logic high voltage" to unclaimed power supplies and their supply voltages that are neither disclosed in the specification nor recited in the claims.

We also are unpersuaded by Patent Owner's arguments that a construction of "logic high voltage" that is not limited to Vcc lacks a

practical dividing line or reasonable boundaries. PO Resp. 13; *see* Ex. 2001 ¶¶ 31, 39; Ex. 2002 ¶¶ 27, 28. Patent Owner has provided insufficient argument and evidence that a person of ordinary skill in the art would understand the term “logic high voltage” to be limited by Vcc in the context of the ’045 patent. For example, Patent Owner points to no industry standard for flash memory devices and power supplies, other than unsupported testimony of a common understanding regarding Vcc and nominal power supplies. Ex. 2001 ¶¶ 31, 39; Ex. 2002 ¶¶ 27, 28.

Patent Owner’s arguments that Petitioner’s expert lacks NAND flash memory experience and is not a person of ordinary skill in the art are also unavailing. PO Resp. 10. Patent Owner’s experts opined that a person of ordinary skill in the art would have at least 3 years of flash memory experience. Ex. 2001 ¶17; Ex. 2002 ¶ 19. We agree with Petitioner that its expert, Robert J. Murphy, has sufficient experience to meet the requirements of a person of ordinary skill in the art. Reply 4 (citing Deposition of Robert J. Murphy, Ex. 2003, 113:2–13, 114:11–117:6; 118:9–119:3). Indeed, we agree with Mr. Murphy’s declaration on the proposed construction of “logic high voltage” based on the specification of the ’045 patent. Ex. 1006 ¶ 17.

Finally, we find that Petitioner’s proposed construction is consistent with the specification that states that voltage Vcc is applied to bit select control line (BSL), the unselected bit line, and the unselected word line during programming. *See* Ex. 1001, 6:37–45, 7:26–40; Ex. 1006 ¶ 17. We

determine that the broadest reasonable construction of “logic high voltage” is a positive voltage higher than the logic low voltage, such as Vcc.³

2. Remaining Claim Terms

Patent Owner does not contest the claim constructions for the terms “logic low voltage” (claims 1 and 4); “boosted positive voltage” (claims 1 and 4); “selected bit line” and “unselected bit line” (claims 1 and 4); and “selected word line” and “unselected word line” (claims 1 and 4). In the Decision to Institute, we applied the broadest reasonable claim interpretation and interpreted the undisputed claim terms as follows (Dec. 7–9):

Claim Term	Construction
“logic low voltage”	“a low voltage, such as ground or Vss”
“boosted positive voltage.”	“a positive voltage higher than [the] logic high voltage” ⁴

³ Petitioner notes that the Board adopted Petitioner’s proposed construction for purposes of the Decision to Institute, but omitted the word “the” in the constructions for “logic high voltage” and “boosted positive voltage.” Reply 5; Dec. 7–9. As Patent Owner notes, the missing word (“the”) was not a “material change” to Petitioner’s proposed constructions. PO Resp. 7. In this Final Decision, our construction for “logic high voltage” inserts the word “the” into the construction, but does not alter our determination in our Decision to Institute or change our interpretation of the claim term.

⁴ As Patent Owner notes, the missing word (“the”) was not a “material change” to Petitioner’s proposed constructions, which we adopted in our Decision to Institute. PO Resp. 7; *see* Dec. 7–8. Our use of the word “the” in the construction for “boosted positive voltage” in this Final Decision does not alter our determination in our Decision to Institute or change our interpretation of the claim term.

Claim Term	Construction
“selected bit line”	“the bit line connected to the column of memory cells containing the memory cell to be operated on”
“unselected bit line”	“the bit line connected to the column of memory cells containing the memory cell to be operated on”
“selected word line”	“the word line connected to the row of memory cells containing the memory cell to be operated on”
“unselected word line”	“the word line connected to the row of memory cells containing the memory cell to be operated on”

After considering all of the evidence now before us, we maintain these constructions for purposes of this Decision.

B. Asserted Grounds of Unpatentability

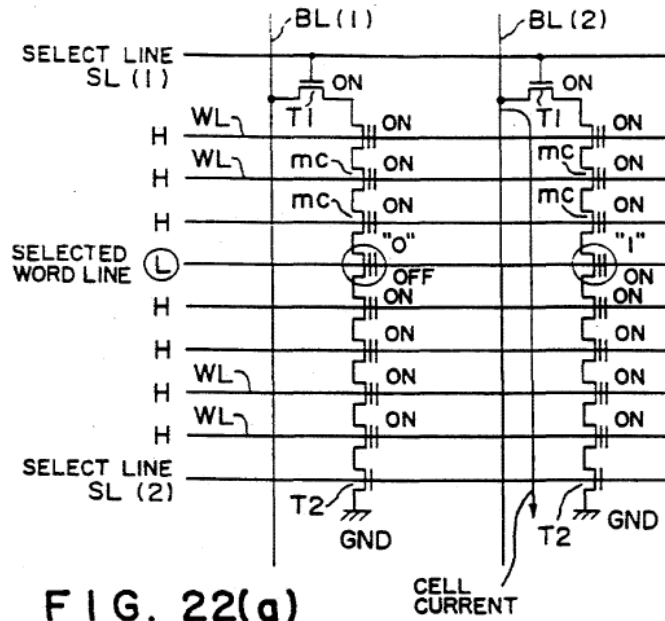
1. Anticipation by Nakai

Petitioner contends that Nakai anticipates claims 1 and 4. Pet. 13–16. Petitioner relies on the Declaration of Robert J. Murphy (Ex. 1006) (“Murphy Declaration”) and provides detailed claim charts showing the claim limitations and the corresponding disclosure in Nakai (Pet. 17–29). For the reasons set forth below, Petitioner has shown by a preponderance of the evidence that Nakai discloses each limitation of claims 1 and 4.

a. Nakai (Ex. 1005) Overview

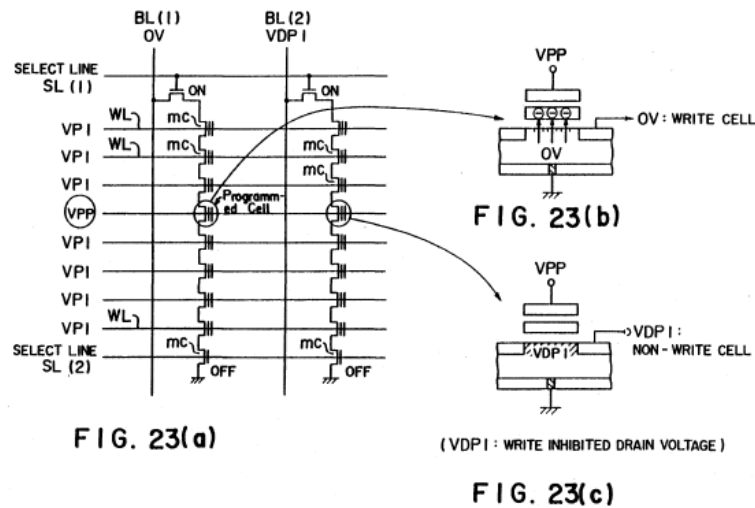
Nakai describes a semiconductor memory device that is a NAND type EEPROM arranged as an array. Ex. 1005, 1:20–26, Figs. 22(a), 25(a), 26. Nakai describes selecting a programmable memory cell within the array for read, write, and erase operations. *Id.* at 1:10–15, 1:46, 2:10. Figure 22(a),

shown below, illustrates the structure of the array memory cells. *Id.* at 1:20–23, 6:65–66.



“Fig[ure] 22(a) shows the structure of two NAND bundles each having eight memory cells MC of a floating gate structure and connected between a bit line and a source.” *Id.* at 1:2–23. Figure 22(a) shows select lines (SL), word lines (WL), bit lines (BL), and memory cells (MC). By setting select voltages to high or low levels at select lines and word lines, data in the selected memory cell can be read. *Id.* at 1:24–45.

Similarly, Figures 23(a)–(c), shown below, depict a write operation for the memory cells of Figure 22(a). *Id.* at 1:46–47, 6:67–68.



Figures 23(a)–(c) show a high voltage V_{pp} of about 20 V applied to a row to select a gate (Fig. 23(b) and (c) showing V_{PP}) and intermediate voltage V_{PI} of above 10 V applied to the remaining seven memory cells for unselected gates. *Id.* at 1:46–52. When the bit lines are set to specified voltages, write operations are performed at the selected write line (see Fig. 23(b) showing write cell at 0 V) and write operations are not performed at the non-write cells (see Fig. 23(c) showing non-write cell at V_{DP}).

Figure 25(a), reproduced below, shows the operation mode of a NAND structure semiconductor memory. *Id.* at 2:24–26.

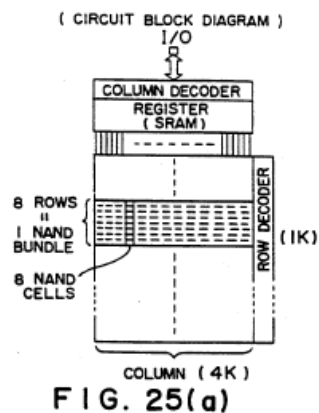


Figure 25(a) shows the semiconductor memory array laid out in bundles where “bit lines are laid out in the column direction, and 128 NAND bundles [equaling] 1024 word lines are laid out in the row direction.” *Id.* at 2:25–31.

b. Anticipation of Claims 1 and 4

We find that Nakai discloses the “flash memory” limitations of claims 1 and 4 (Pet 17 (citing Ex. 1006 ¶ 22)) and that Figure 4 of the ’045 patent and Figure 22(a) of Nakai are the same, showing an array configuration of gates or cells with select, bit, and word lines (Pet. 14). We also agree with Petitioner that the programming voltages described in Figure 23(a) of Nakai are the same selected and unselected lines and voltages recited in the “programming” limitations of claims 1 and 4. Pet. 14–15. We also agree with Petitioner that one of ordinary skill in the art would understand Nakai to disclose applying a logic low voltage to a selected bit line as recited in claims 1 and 4 (“a logic low voltage is applied to a selected bit line while a logic high voltage is applied to unselected bit lines”). Pet. 15, 16, 21, 23. Similarly, we find that Nakai discloses that “a logic high voltage is applied to unselected word lines, while a boosted positive voltage is applied to a selected word line” in the write operation described and shown in Figure 23(a). Pet. 27–28; Ex. 1005, 1:45–2:9.

Patent Owner’s primary argument is that under a proper construction of “logic high voltage” that is bounded as higher than logic low voltage and less than or equal to the nominal value for V_{cc} , Nakai fails to anticipate because it applies a programming scheme that uses “boosted positive voltage” where claims 1 and 4 require “logic high voltage.” PO Resp. 12 (providing proposed construction), 17 (applying construction to Nakai). Because we rejected Patent Owner’s limiting construction in Section II.A.1.,

we are not persuaded that Nakai fails to disclose a logic high voltage and a boosted positive voltage as recited in claims 1 and 4 and construed in Section II.A.1. Instead, under our construction for “logic high voltage,” which does not provide V_{cc} as an upper limit, we find that the programming voltages disclosed in Nakai (Ex. 1005 1:47–50, 1:53–57, 2:3, Fig. 23(a)) provide relative voltages that correspond to the claimed logic high voltage, logic low voltage, and boosted positive voltage. *See* Pet. 16 (table summarizing Nakai programming voltages).

We do not agree with Patent Owner’s arguments that the advantages of the ’045 patent’s programming scheme over the Nakai programming scheme is material to the application of “logic high voltage” as claimed to Nakai. PO Resp. 22. Patent Owner’s argument that ’045 patent programming scheme reduces the need for charge pumps or other the on-chip circuitry (PO Resp. 22–23) relies on features and functions that are beyond the scope of claims 1 and 4 and the written description that supports those claims. The ’045 patent claims do not recite, and the written description does not limit, the voltage sources used to provide the claimed voltages.

Although Patent Owner states in a footnote that Nakai would not anticipate the limitations of claims 1 and 4 even if the Board does not adopt Patent Owner’s proposed construction for “logic high voltage,” Patent Owner’s argument incorrectly assumes that the Board’s construction limits logic high voltage to V_{cc} . PO Resp. 22 n.7. Under the Board’s construction, V_{cc} is provided as an exemplary voltage and does not limit the upper boundary under the broadest reasonable interpretation of “logic high voltage” to V_{cc} .

In sum, we have considered the evidence and argument presented by Petitioner and Patent Owner. We are persuaded that Petitioner's evidence and argument show that Nakai anticipates the limitations of claims 1 and 4. Accordingly, we conclude that Petitioner has proven by a preponderance of the evidence that claims 1 and 4 are anticipated by Nakai.

III. CONCLUSION

Petitioner has demonstrated by a preponderance of the evidence that claims 1 and 4 of the '045 patent are unpatentable based on 35 U.S.C. § 102(b) as anticipated by Nakai.

IV. ORDER

For the reasons given, it is

ORDERED that, based on a preponderance of the evidence, claims 1 and 4 of U.S. Patent No. 6,058,045 are held unpatentable; and

FURTHER ORDERED, because this is a final written decision, the parties to this proceeding seeking judicial review of our Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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