

**FILED ON BEHALF OF TAIWAN SEMICONDUCTOR
MANUFACTURING COMPANY, LIMITED**

By: Steven H. Slater
Roger C. Knapp
Slater & Matsil, L.L.P.
17950 Preston Road, Suite 1000
Dallas, Texas 75252
Telephone: (972) 732-1001
Facsimile: (972) 732-9218

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

PETITION FOR *INTER PARTES* REVIEW

OF U.S. PATENT NO. 6,563,133 B1

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CERTIFICATE OF SERVICE ON PATENT OWNER PURSUANT TO 37
C.F.R. § 42.105(a)61

TABLE OF EXHIBITS

- TSMC1001: U.S. Patent No. 6,563,133 B1 to Tong Filed: August 9, 2000, Issued: May 13, 2003 (“133 Patent”)
- TSMC1002: File Wrapper of U.S. Patent No. 6,563,133 B1 to Tong, Application No. 09/635,272, filed August 9, 2000
- TSMC1003: Declaration of Dr. Richard A. Blanchard in Support of Petition for *Inter Partes* Review of U.S. Patent No. 6,563,133
- TSMC1004: Thomson Reuters Expert Witness Services Consultant Curriculum Vitae: Richard A. Blanchard, Ph.D.
- TSMC1005: U.S. Patent No. 6,534,381 to Cheung et al., Filed: January 4, 2000, Issued: March 18, 2003 (“Cheung”)
- TSMC1006: U.S. Patent No. 5,561,072 to Saito, Filed: November 21, 1994, Issued: October 1, 1996 (“Saito”)
- TSMC1007: Seiji Fujino et al., Silicon Wafer Direct Bonding through the Amorphous Layer, 34 Japanese J. Appl. Phys. 1322 (15 October 1995) (“Fujino”)
- TSMC1008: Shiyang Tian et al., A Detailed Physical Model for Ion Implant Induced Damage in Silicon, 45 (6) IEEE Transactions on Electron Devices 1226 (June 1998) (“Tian”)
- TSMC1009: RANDOM HOUSE WEBSTER’S COLLEGE DICTIONARY 884 (Random House, Inc. 2000) (1991)

Inter partes review under 35 U.S.C. § 311, and 37 C.F.R. Part 42, Subpart B is hereby requested for Claims 1-14 and 53-60 of U.S. Patent No. 6,563,133 B1 to Tong (“’133 Patent”). A copy of the ’133 Patent is attached as TSMC1001.

I. MANDATORY NOTICES (37 C.F.R. § 42.8)

A. Real Parties-in-Interest

This Petition is brought by Taiwan Semiconductor Manufacturing Company, Limited and TSMC North America Corporation (collectively “Petitioner”).

B. Related Matters

Petitioner is not aware of any judicial or administrative matter that would affect, or be affected, by a decision in this proceeding.

C. Lead and Backup Counsel

Lead Counsel:
Steven H. Slater
Reg. No. 35,361
Slater & Matsil, L.L.P.
17950 Preston Road
Suite 1000
Dallas, Texas 75252
Tel: (972) 732-1001
Fax: (972) 732-9218
Email: slater@slater-matsil.com

Back-up Counsel:
Roger C. Knapp
Reg. No. 46,836
Slater & Matsil, L.L.P.
17950 Preston Road
Suite 1000
Dallas, Texas 75252
Tel: (972) 732-1001
Fax: (972) 732-9218
Email: knapp@slater-matsil.com

D. Notice Information

Please address all correspondence to the Lead Counsel at the address provided in Section I.C above and to docketing@slater-matsil.com.

II. FEES (37 C.F.R. § 42.103)

The fee under 37 C.F.R. §§ 42.15(a), 42.103(a) for this Petition has been paid as part of the electronic submission of this Petition, and Petitioner authorizes any other fees that may be due in connection with this Petition to be charged to, or credit any overpayment to, Deposit Account No. 50-1065.

III. GROUNDS FOR STANDING (37 C.F.R. § 42.104(a))

Petitioner certifies that the '133 Patent is eligible for *inter partes* review. The '133 Patent issued on May 13, 2003, which is a patent that is not described in section 3(n)(1) of the Leahy-Smith America Invents Act under 37 C.F.R. § 42.102(a)(2), and the '133 Patent is not currently involved in a post-grant review proceeding. The '133 Patent is unexpired.

Petitioner certifies that Petitioner and their privies are not barred or estopped from requesting *inter partes* review of the '133 Patent challenging Claims 1-14 and 53-60 on the grounds identified in this Petition.

IV. IDENTIFICATION OF CHALLENGE (37 C.F.R. § 42.104(A)(1)-(2))

Petitioner requests institution of an *inter partes* review, and a determination of unpatentability, of Claims 1-14 and 53-60 over the prior art and bases below.

TABLE 1

| Exhibit No. | Description |
|--------------------|---|
| TSMC1005 | U.S. Patent No. 6,534,381 to Cheung et al., Filed: January 4, 2000, Issued: March 18, 2003 (“Cheung”), which is prior art under 35 U.S.C. § 102(e). Cheung was not previously before the Office |

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| | during prosecution of the '133 Patent. |
| TSMC1006 | U.S. Patent No. 5,561,072 to Saito, Filed: November 21, 1994, Issued: October 1, 1996 (“Saito”), which is prior art under 35 U.S.C. § 102(A). Saito was not previously before the Office during prosecution of the '133 Patent. |
| TSMC1007 | Seiji Fujino et al., <i>Silicon Wafer Direct Bonding through the Amorphous Layer</i> , 34 Japanese J. Appl. Phys. 1322 (15 October 1995) (“Fujino”), with is prior art under 35 U.S.C. § 102(A). The full disclosure of Fujino was not substantively addressed during prosecution of the '133 Patent. |
| TSMC1008 | Shiyang Tian et al., <i>A Detailed Physical Model for Ion Implant Induced Damage in Silicon</i> , 45 (6) IEEE Transactions on Electron Devices 1226 (June 1998) (“Tian”), which is prior art under 35 U.S.C. § 102(A). Tian was not previously before the Office during prosecution of the '133 Patent. |

TABLE 2

| Ground | Claims | Statutory Grounds and Prior Art Reference(s) |
|---------------|-----------------------------------|---|
| Ground 1 | 1-10, 12-14, 53-59 | Anticipated under 35 U.S.C. § 102(e) by or obvious under 35 U.S.C. § 103(a) over Cheung |
| Ground 2 | 1-14, 53-60 | Obvious under 35 U.S.C. § 103(a) over Cheung in view of Saito |
| Ground 3 | 1-14, 53-59 | Obvious under 35 U.S.C. § 103(a) over Cheung in view of Tian |
| Ground 4 | 1-14, 53-60 | Obvious under 35 U.S.C. § 103(a) over Cheung in view of Tian, and in further view of Saito |
| Ground 5 | 1-7, 9, 10, 12, 13, 53-56, 58, 59 | Anticipated under 35 U.S.C. § 102(A) by or obvious under 35 U.S.C. § 103(a) over Fujino |
| Ground 6 | 1-14, 53-56, 58-60 | Obvious under 35 U.S.C. § 103(a) over Fujino in view of Saito |
| Ground 7 | 1-13, 53-56, 58, 59 | Obvious under 35 U.S.C. § 103(a) over Fujino in view of Tian |
| Ground 8 | 1-14, 53-56, 58-60 | Obvious under 35 U.S.C. § 103(a) over Fujino in view of Tian, and in further view of Saito |
| Ground 9 | 2, 5, 54, 57 | Obvious under 35 U.S.C. § 103(a) over Fujino alone or in view of Saito and/or Tian, and in further view of Cheung |

V. CLAIM CONSTRUCTION (37 C.F.R. § 42.104(A)(3))

Pursuant to 37 C.F.R. § 42.100(b), the scope of the terms in the claims are to be given their broadest reasonable construction in light of the specification. Petitioner submits that such claim constructions do not necessarily correspond to the construction of claim terms under the legal standards that are mandated to be used by courts in litigation. *See, e.g.*, M.P.E.P. § 2686.04(IV). Hence, Petitioner submits that claim constructions discussed herein for the purposes of this Petition are not binding upon Petitioner in any litigation or other proceeding related to the '133 Patent. Petitioner expressly reserves the right to present differing constructions of the claims of the '133 Patent in litigation or other venue.

A brief discussion of the '133 Patent and its prosecution history is provided for context of the discussion of “nearly-amorphized layer” and “a few nm in thickness.” A copy of the prosecution history is attached as TSMC1002.

A. Overview of the '133 Patent

The '133 Patent relates to epitaxial-like bonding of wafer pairs at low temperature. *See* TSMC1001 at 1:8-9. A first wafer 200 is cleaned, such as using an RCA-1 solution. *See id.* at 5:57-6:3. The wafer 200 is immersed in an aqueous HF solution, such as 1% HF, to remove a native oxide layer, and subsequently exposed to a plasma or to ion implantation 201, preferably a boron-containing plasma (*e.g.*, B₂H₆ plasma) or ion (*e.g.*, BF₃ ion), argon plasma, or arsenic ion. *See*,

e.g., id. at 6:4-11, 34-36, 43-46; 8:22-26, 30-35, 55-58; 9:40-46; Figs. 1 (steps 101 and 102), 2A. The plasma or ion implantation 201 modifies the surface 202 and/or subsurface of the first wafer 200 to create defect areas and possibly a thin amorphous layer, as indicated by the thin layer at the surface 202, and when boron is used, may introduce boron into the substrate surface. *See, e.g., id.* at 6:7-16, 36-39. The amorphous layer is “about a few nm or more in thickness.” *Id.* at 6:42-43. The wafer is immersed in an aqueous HF solution, such as 1% HF, to remove a native or other oxide layer. *See id.* at 6:17-20, 48-49; Fig. 1 (step 103).

A second wafer 203 undergoes similar processing to have a plasma treated surface 204. *See id.* at 6:49-50. The wafers 200 and 203 are bonded with plasma treated surfaces 202 and 204 directly contacted to form a bonded structure at room temperature in atmosphere. *See id.* at 6:21-23, 49-52; Fig. 1 (step 104). The structure is annealed at low temperature. *See id.* at 6:25-26, 52-56; Fig. 1 (step 105). The temperature to anneal may be selected to recrystallize the amorphous layers, or a separate annealing procedure may be used to recrystallize the amorphous layers. *See id.* at 6:27-32.

In an example, an amorphous layer is formed with a thickness of 1650 Å (165 nm) and is recrystallized to have a thickness of 100 Å (10 nm). *See id.* at 9:50; 10:5-13; Figs. 10, 12.

B. Summary of Relevant Prosecution History

The '133 Patent was filed on August 9, 2000 as Application No. 09/635,272 with 58 claims. *See* TSMC1002 at 53-59. As relevant herein, claims 44, 92, and 103 during prosecution correspond to claims 1, 53, and 10, respectively, upon issuance. Unless indicated otherwise, claim numbers discussed in this subsection refer to the numbers during prosecution.

The U.S. Patent & Trademark Office (“the Office”) issued a first Office Action rejecting claim 44 as anticipated by U.S. Pat. No. 5,783,477 (“Kish”) and claim 44 as anticipated by U.S. Pat. No. 6,120,917 (“Eda”). *See id.* at 94-103.

In response to the first Office Action, the applicant amended claim 44 and added claim 103¹. *See id.* at 104-123. Claim 44 was amended as follows: “a first [amorphous] nearly-amorphized layer formed in said first surface” as well as a corresponding amendment for the second layer. *See id.* at 122. Claim 103 was added to recite “said first and second amorphous layers are each in the range of a few nm of thickness.” *See id.* at 115. The applicant argued in regards to Kish,

¹ Claims added in the amendment in response to the first Office Action after claim 100 were misnumbered by 1. *See, e.g.*, TSMC1002 at 126. Hence, claim 103 as referenced throughout prosecution was originally labeled as 104.

“There is no suggestion of any nearly-amorphized layers formed in a substrate. Kish simply [had] amorphous regions in a layer formed on the substrate.” *Id.* at 117. Similarly, the applicant argued, “There is no suggestion of any nearly amorphized layer in the surface of a substrate” in Eda. *Id.* at 118.

The Office then issued a second Office Action. *See id.* at 124-32. The Office rejected claim 103 as being indefinite; and claims 44 and 92 as anticipated by non-patent literature by Takagi et al. (“Takagi”); and claims 44 and 92 as obvious over Kish in view of U.S. Pat. No. 4,963,505 (“Fujii”). *See id.* at 125-30.

In response to the second Office Action, the applicant amended claims 44 and 92. *See id.* at 141-42. Claim 44 was amended as follows: “a first nearly-amorphized layer containing one of boron and arsenic formed [in] uniformly over said surface” as well as a corresponding amendment for the second layer and surface. *See id.* at 141. Claim 92 was amended as follows: “one first material amorphized substantially only in a first surface of said first material and containing one of boron and arsenic” as well as a corresponding amendment for the second material. *See id.* at 142.

In regards to the indefiniteness rejection, the applicant argued, “A ‘few’ is an easily understood value. One skilled in the art would not be confused by what constitutes, for example, a few nm.” *Id.* at 137. The applicant then stated:

Specifically, [Kish] discloses layer 95 formed on the semiconductor

layer and amorphous or polycrystalline regions 91 formed in a layer 95. Regions 91 are formed by selective patterning (see column 8, lines 18-32) and are useful to direct current flow through the bonded structure (see FIG. 9). . . . [O]ne skilled in the art would clearly not form regions 91 uniformly over the surface or over a substantial portion of the surface since the resulting large or complete non-ohmic contact would defeat the whole purpose of trying to form an ohmic contact.

There was some questions raised by Examiners Diaz and Lee over the terms like “substantial” and “uniform” regarding support in the specification and definiteness. The description clearly shows the treatment to produce the amorphized or nearly-amorphized surfaces, such as the non-limiting example of FIG. 2 where surface 202 extends over a substantial portion of the substrate. The support is clear. A term like “substantial” is very often used in this art recognizing that “substantially” is accurate as there may be some incompleteness or nonuniformity due to the realities of physical materials, or the presence of some structure or material on the surface preventing completeness or absoluteness. Terms like “substantial” as used in the claims are definite and convey the subject matter of the invention sought to be protected to one skilled in the art.

Id. at 137-138. The applicant again argued that Kish has “specific regions containing amorphous or polycrystalline material” rather than suggesting a nearly-amorphized layer. *See id.* at 138. The applicant cursorily stated that the claims as amended were patentable over Takagi. *See id.* at 139.

The Office issued a third Office Action rejecting claims 44 and 92 as obvious over Takagi in view of Fujii; and claims 44 and 92 as obvious over Takagi in view of U.S. Pat. No. 6,153,455 (“Yamazaki”). *See id.*, pp. 150-158.

In response to the third Office Action, the applicant characterized Takagi as teaching argon sputtering in a manner designed to clean a surface to promote bonding and further, that Takagi did not suggest a substitute for the argon beam. *See id.* at 162-163. The applicant stated that Fujii “describes an amorphous silicon layer 16 which may be formed by implanting ions such as silicon, arsenic, phosphorous” but argued that Fujii does not suggest “an amorphous layer in a bonded structure” since the “amorphous layer is intentionally thermally treated to form single-crystal and poly-crystal layers, and is not present in a bonded structure.” *Id.* at 163-164. Hence, the applicant concluded:

[T]here is no suggestion that the implantation to form the amorphous layer would be used for a surface cleaning operation and substitution for the Ar sputter etch of Takagi et al, nor is there any suggestion of an amorphous region or layer in a bonded device. The amorphous layer is specifically converted out of the amorphous state into a polycrystalline or single-crystalline state prior to any bonding. To the contrary, Fujii et al teaches away from using amorphous layers in a bonded structure.

Id. at 164. Similarly, the Applicant argued, “[T]here is no discussion [in Yamazaki] of forming an amorphous layer in a bonded structure, or any suggestion

that the ion implantation for the threshold voltage control would be substituted for an Ar sputter etch for cleaning the surface of the substrate. . . . [Yamazaki] also teaches away from amorphous layers remaining in the structure.” *Id.* at 164-165.

Subsequently, the Examiner allowed the application.

C. “**Nearly-amorphized layer**”

The term *nearly-amorphized layer* is completely absent from the specification of the ’133 Patent. The *nearly-amorphized layer* term was first introduced in a first amendment during prosecution. *See* TSMC1002 at 122. The applicant argued that the prior art did not teach an amorphous layer in arguing patentability of claim 1 (claim 44 during prosecution) and pointed out the import of some incompleteness or nonuniformity due to the realities of physical materials or the presence of some structure of material on the surface preventing completeness or absoluteness. *See, e.g., id.* at 163-165. Figure 2 in the ’133 Patent, which was cited as support for a nearly-amorphized layer, *see id.* at 164, teaches a surface 202 that is an amorphous layer, *see, e.g.,* TSMC1001 at 6:40-42. A plain meaning of “nearly” is “with close approximation.” TSMC1009 at 884. Hence, consistent with the broadest reasonable construction, arguments in the prosecution history, and support in the specification, Petitioner construes *nearly-amorphized layer* as a layer that at least closely approximates an amorphous layer. This construction includes, for example, an amorphous layer that allows for incompleteness of the

amorphizing due to realities of physical materials.

D. A few nm in thickness

The '133 Patent states, “The amorphous layer formed is about a few nm or more in thickness,” TSMC1001 at 6:42-43, and teaches in an embodiment forming “an amorphous layer with 1650 Å thick,” *see id.* at 9:48-50. The specification does not indicate whether this 1650 Å (165 nm) thickness is not “a few nm,” such as by stating that it is more than a few nm. Under the broadest reasonable construction consistent with the Specification, Petitioner asserts that *a few nm in thickness* at least encompasses 165 nm.

VI. UNPATENTABILITY OF CLAIMS 1-14 AND 53-60 AND SUPPORTING EVIDENCE (37 C.F.R. § 42.103(A)(4)-(5))

This Section applies each of the prior art references to Claims 1-14 and 53-60 to demonstrate a reasonable likelihood that at least one of Claims 1-14 and 53-60 is unpatentable. Petitioner submits a declaration of Dr. Richard A. Blanchard, attached hereto as TSMC1003, in support of this Petition. Accordingly, Petitioner asserts that there is a reasonable likelihood that at least one of Claims 1-14 and 53-60 is unpatentable.

GROUND 1: Claims 1-10, 12-14, and 53-59 are anticipated by or rendered obvious over Cheung.

| Claims | Cheung |
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| 1. A bonded structure, | Cheung discloses a “bonded structure.” <i>See, e.g.</i> , TSMC1005 at 2:18-20. |

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| <p>comprising:</p> | |
| <p>a first substrate having a first surface, a first nearly-amorphized layer containing one of boron and arsenic formed uniformly over said first surface; and</p> | <p>Cheung discloses an amorphous silicon layer 15 formed uniformly throughout an upper surface 19 of a substrate 10. <i>See, e.g., id.</i> at 3:49-50 (“Implant surface of first substrate to create a compliant layer (e.g., amorphous silicon layer)”); 5:52-6:14 (“The implantation process forms an ‘amorphous’ layer 15 of silicon overlying single crystal silicon material. . . . The amorphous silicon layer has a substantially planar upper surface 19, which also has amorphous characteristics.”); 8:16-18; Figs. 3, 4. Cheung describes forming the amorphous silicon layer 15 using an implant of a “silicon bearing particle” or other types of particles including “germanium or hydrogen.” <i>See, e.g., id.</i> at 5:65-66; 6:50-52. Since Cheung discloses an amorphous silicon layer 15, Cheung discloses a layer that at least closely approximates an amorphous layer, <i>i.e.</i>, a nearly-amorphized layer. <i>See, e.g., TSMC1003</i> at ¶ 30.</p> <p>Cheung discloses that the substrate 10 is doped with impurities including boron or arsenic. <i>See, e.g., TSMC1005</i> at 4:15-20. Thus, Cheung’s amorphous silicon layer 15 contains one of boron and arsenic. <i>See, e.g., TSMC1003</i> at ¶ 31.</p> |
| <p>a second substrate having a second surface, a second nearly-amorphized layer containing one of boron and arsenic formed uniformly over said second surface;</p> | <p>Cheung discloses forming an amorphous layer of silicon formed uniformly throughout a surface of a substrate 20. <i>See, e.g., TSMC1005</i> at 8:21-23, 32-65. Cheung describes forming an amorphous layer using implants of “a silicon bearing particle” or other types of particles including “germanium or hydrogen.” <i>See, e.g., id.</i> at 8:56-57; 5:65-66; 6:50-52. Since Cheung discloses an amorphous layer of silicon, Cheung discloses a layer that at least closely approximates an amorphous layer, <i>i.e.</i>, a nearly-amorphized layer. <i>See, e.g., TSMC1003</i> at ¶ 30.</p> <p>Cheung discloses that the substrate 20 is doped with impurities including boron or arsenic. <i>See, e.g., TSMC1005</i> at 5:4-7. Thus, Cheung’s amorphous layer of silicon contains one of boron and arsenic. <i>See also, e.g., TSMC1003</i> at ¶ 31.</p> |
| <p>said first surface</p> | <p>Cheung discloses bonding the surface of amorphous silicon</p> |

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| <p>being bonded to said second surface to form a bonded pair of substrates.</p> | <p>layer 15 of substrate 10 with the surface of amorphous layer of silicon of substrate 20. <i>See, e.g.</i>, TSMC1005 at 8:26-29, Col. 8:32-41 (“[T]he present invention provides a method for bonding substrates together using first and second compliant layers of amorphous silicon, for example, on the first substrate and second substrate, respectively.”); Fig. 8; <i>see also, e.g.</i>, TSMC1003 at ¶ 30.</p> |
| <p>2. A structure as recited in claim 1, comprising:</p> | <p>Cheung discloses the limitations of Claim 1.</p> |
| <p>one of said first and second substrates of said bonded pair having a third surface, said third surface having a nearly-amorphized layer;</p> | <p>Cheung describes bonding the substrates 10 and 20, as discussed above. <i>See, e.g.</i>, TSMC1005 at 8:10-41. Cheung teaches that the invention can be applied “for multi-layered integrated circuit devices, three-dimensional packaging of integrated semiconductor devices,” and more. <i>See, e.g., id.</i> at 1:17-21.</p> <p>Accordingly, it would have been obvious to a person having ordinary skill in the art at the time of the invention to form one of the first and second substrates having a third surface having a nearly-amorphized layer, to form a nearly-amorphized layer in a fourth surface of a third substrate, and to bond the third surface to the fourth surface as recited in Claim 2 to form multi-layered integrated circuit devices or a three-dimensional package as described in Cheung. <i>See also, e.g.</i>, TSMC1003 at ¶ 32.</p> |
| <p>a third substrate having a fourth surface, a fourth nearly-amorphized layer formed in said fourth surface; and</p> | <p>Moreover, “the mere duplication of parts has no patentable significance unless a new and unexpected result is produced.” <i>See, e.g., In re Harza</i>, 274 F.2d 669, 671 (C.C.P.A. 1960).²</p> |
| <p>said third surface bonded</p> | <p>Claim 2 requires nothing more than the duplication of the</p> |

² References to authorities are cited in first appearances of an issue and are not further referenced for similar issues, although such references should be inferred.

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| to said fourth surface. | parts recited in Claim 1, which does not produce any new and/or unexpected results for bonding nearly-amorphized layers of additional substrates. |
| 3. A structure as recited in claim 1, wherein said first and second substrates are selected from Si, InGaAs, InP, GaAs, Ge and SiC. | Cheung discloses the limitations of Claim 1. Cheung discloses that the substrates are “silicon,” “compound semiconductors and the like,” or “gallium arsenide [(GaAs)], gallium nitride (GaN), and others.” <i>See, e.g.</i> , TSMC1005 at 4:10-15, 25-27; 4:63-5:3; 9:52-53. |
| 4. A structure as recited in claim 1, wherein: | Cheung discloses the limitations of Claim 1. |
| said first and second substrates each comprises a silicon substrate; and | Cheung discloses that each of the substrates 10 and 20 are silicon. <i>See, e.g., id.</i> at 4:10-15; 4:66-5:3. |
| said first and second surfaces each comprises a silicon surface. | Cheung discloses that each of the surfaces of the amorphous silicon layer 15 of substrate 10 and amorphous layer of silicon of substrate 20 is a silicon surface. <i>See, e.g., id.</i> at 8:32-41, 62-65; 5:52-6:14. |
| 5. A structure as recited in claim 1, wherein: | Cheung discloses the limitations of Claim 1. |
| said first and second substrates comprise respective first and second semiconductor | Cheung discloses that the invention can be applied to “multi-layered integrated circuit devices, three-dimensional packaging of integrated semiconductor devices, photonic devices, piezoelectronic devices, microelectromechanical systems (“MEMS”), sensors, actuators, solar cells, flat panel displays (e.g., LCD, AMLCD), biological and biomedical devices, and the like.” <i>See, e.g., id.</i> at 1:17-24. |

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| devices. | |
| 6. A structure as recited in claim 1, wherein: | Cheung discloses the limitations of Claim 1. |
| said first surface comprises a first silicon surface exposed to a boron-containing plasma; and | The limitation “ <i>exposed to a boron-containing plasma</i> ” (emphasis added) is a product-by-process limitation, which only requires Petitioner to show a same structure. <i>See, e.g., Bonito Boats, Inc. v. Thunder Craft Boats, Inc.</i> , 489 U.S. 141, 159 (1989) (citing D. Chisum, CHISUM ON PATENTS § 8.05); <i>In re Thorpe</i> , 777 F.2d 695, 698 (Fed. Cir. 1985). |
| said second surface comprises a second silicon surface exposed to a boron-containing plasma. | To the extent that exposure to a boron-containing plasma requires the surfaces to resultantly contain boron, to which Petitioner does not concede, Cheung discloses that the surface 19 of the amorphous silicon layer 15 of substrate 10 and that the surface of the amorphous layer of silicon of substrate 20 each comprise a silicon surface and boron. <i>See, e.g., TSMC1005</i> at 4:12-20; 5:3-7; 6:9-14; 8:62-65; <i>see also TSMC1003</i> at ¶ 31. Hence, Cheung discloses a same structure. |
| 7. A structure as recited in claim 1, wherein: | Cheung discloses the limitations of Claim 1. |
| said first surface comprises a first silicon surface implanted with boron; and | The limitation “ <i>implanted with boron</i> ” (emphasis added) is a product-by-process limitation, which only requires Petitioner to show a same structure. |
| said second surface comprises a second silicon surface implanted with boron. | Cheung discloses that the surface 19 of the amorphous silicon layer 15 of substrate 10 and the surface of the amorphous layer of silicon of substrate 20 each comprise a silicon surface and boron. <i>See, e.g., TSMC1005</i> at 4:12-20; 5:3-7; 6:9-14; 8:62-65; <i>see also TSMC1003</i> at ¶ 31. Hence, Cheung discloses a same structure. |
| 8. A structure as recited in claim | Cheung discloses the limitations of Claim 1. |

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| 1, wherein: | |
| said first surface comprises a first silicon surface implanted with arsenic; and | The limitation “ <i>implanted with arsenic</i> ” (emphasis added) is a product-by-process limitation, which only requires Petitioner to show a same structure. |
| said second surface comprises a second silicon surface implanted with arsenic. | Cheung discloses that the surface 19 of the amorphous silicon layer 15 of substrate 10 and the surface of the amorphous layer of silicon of substrate 20 each comprise a silicon surface and arsenic. <i>See, e.g.</i> , TSMC1005 at 4:12-20; 5:3-7; 6:9-14; 8:62-65; <i>see also</i> TSMC1003 at ¶ 31. Hence, Cheung discloses a same structure. |
| 9. A structure as recited in claim 1, comprising: | Cheung discloses the limitations of Claim 1. |
| at least one of boron-boron and Si covalent bonds formed between said first and second substrates. | Cheung discloses a method for fabricating an “epi-like” substrate by bonding together a pair of substrates having amorphous surfaces. <i>See, e.g.</i> , TSMC1005 at 2:25-47. Cheung discloses steps to “strip” the surfaces of the substrates to the silicon surface. <i>See, e.g., id.</i> at 8:20, 26. The subsequent joining and annealing steps, <i>see, e.g., id.</i> at 8:27-29, form a bond between silicon atoms in the silicon surface, <i>see, e.g., id.</i> at 9:57 (“silicon-on-silicon” bond), which is a covalent bond since silicon-to-silicon bonding occurs by covalent bonding. <i>See, e.g.</i> , TSMC1003 at ¶ 33. Further, as understood by a person having ordinary skill in the art, an “epi-like” substrate denotes the formation of silicon covalent bonds across the bond interface for a pair of bonded substrates. <i>See, e.g., id.</i> |
| 10. A structure as recited in claim 1, wherein: | Cheung discloses the limitations of Claim 1. |
| said first and second amorphous | Cheung discloses forming an amorphous silicon layer with a “thickness ranging from about 10 nm to about 500 nm.” <i>See, e.g.</i> , TSMC1005 at 6:10-13. Hence, Cheung discloses a |

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| <p>layers are each in the range of a few nm in thickness.</p> | <p>thickness in the range of 165 nm, <i>i.e.</i>, a range of a few nm in thickness.</p> <p>Assuming for the sake of argument that Cheung’s disclosure does not anticipate the claim, Cheung’s range overlaps the range of a few nm in thickness, and therefore, Cheung renders Claim 10 <i>prima facie</i> obvious. <i>See, e.g., In re Wertheim</i>, 541 F.2d 257 (C.C.P.A. 1976); <i>In re Woodruff</i>, 919 F.2d 1575 (Fed. Cir. 1990).</p> <p>Even assuming further for the sake of argument that Cheung’s disclosure does not overlap, “it is not inventive to discover the optimum or workable ranges by routine experimentation.” <i>In re Aller</i>, 220 F.2d 454, 456 (C.C.P.A. 1955). The range of thickness of a few nm could be determined by a person having ordinary skill in the art at the time of the invention by routine experimentation. <i>See, e.g., TSMC1003</i> at ¶ 34.</p> |
| <p>12. A structure as recited in claim 1, wherein:</p> | <p>Cheung discloses the limitations of Claim 1.</p> |
| <p>said first surface comprises an amorphous boron-containing layer; and</p> | <p>Cheung discloses that the surface 19 of the amorphous silicon layer 15 comprises the amorphous silicon layer 15. <i>See, e.g., TSMC1005</i> at 3:49-50; 5:52-6:14; 8:15-18.</p> <p>Cheung discloses that the substrate 10 is doped with impurities including boron. <i>See, e.g., id.</i> at 4:15-20. Thus, Cheung’s amorphous silicon layer 15 contains boron. <i>See, e.g., TSMC1003</i> at ¶ 31.</p> |
| <p>said second surface comprises an amorphous boron-containing layer.</p> | <p>Cheung discloses that the surface of the amorphous layer of silicon comprises the amorphous layer. <i>See, e.g., TSMC1005</i> at 8:21-23, 32-65.</p> <p>Cheung discloses that the substrate 20 is doped with impurities including boron. <i>See, e.g., id.</i> at 5:4-7. Thus, Cheung’s amorphous layer of silicon contains boron. <i>See also, e.g., TSMC1003</i> at ¶ 31.</p> |

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| <p>13. A structure as recited in claim 1, wherein:</p> | <p>Cheung discloses the limitations of Claim 1.</p> |
| <p>said first surface comprises a surface exposed to a boron-containing plasma; and</p> | <p>The limitation “<i>exposed to a boron-containing plasma</i>” (emphasis added) is a product-by-process limitation, which only requires Petitioner to show a same structure.</p> <p>To the extent that exposure to a boron-containing plasma requires the surfaces to resultantly contain boron, to which Petitioner does not concede, Cheung discloses that the substrate 10 and the substrate 20 each are doped with impurities including boron. <i>See, e.g.</i>, TSMC1005 at 4:15-20; 5:4-7. Thus, Cheung’s surface 19 of the amorphous silicon layer 15 and surface of the amorphous layer of silicon each contain boron. <i>See, e.g.</i>, TSMC1003 at ¶ 31. Hence, Cheung teaches a same structure.</p> |
| <p>said second surface comprises a surface exposed to a boron-containing plasma.</p> | |
| <p>14. A structure as recited in claim 1, wherein:</p> | <p>Cheung discloses the limitations of Claim 1.</p> |
| <p>said first surface comprises a first surface exposed to an inert gas plasma; and</p> | <p>The limitation “<i>exposed to an inert gas plasma</i>” (emphasis added) is a product-by-process limitation, which only requires Petitioner to show a same structure.</p> <p>To the extent that exposure to an inert gas plasma requires a resultant change to the surfaces, to which Petitioner does not concede, Cheung discloses cleaning the surfaces of the substrates 10 and 20 using “a plasma cleaning process” using “non-reactive gases such as argon.” <i>See, e.g.</i>, TSMC1005 at 4:33, 43-44; 5:21, 29. Argon is an inert gas. <i>See, e.g.</i>, TSMC1003 at ¶ 35. Thus, Cheung discloses exposing the respective surface of the first and second substrates to an inert gas plasma.</p> |
| <p>said second surface comprises a second surface exposed to an inert gas plasma.</p> | |
| <p>53. A bonded structure, comprising:</p> | <p>Cheung discloses a “bonded structure.” <i>See, e.g.</i>, TSMC1005 at 2:18-20.</p> |

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| <p>a first substrate of substantially one first material amorphized substantially only in a first surface of said first material and containing one of boron and arsenic; and</p> | <p>Cheung discloses a substrate 10 of substantially one material, <i>e.g.</i>, silicon. <i>See, e.g., id.</i> at 4:12-14. The one material, <i>e.g.</i>, silicon, is amorphized, <i>e.g.</i>, amorphous silicon layer 15, substantially only in upper surface 19 of the material. <i>See, e.g., id.</i> at 3:49-50 (“Implant surface of first substrate to create a compliant layer (<i>e.g.</i>, amorphous silicon layer)”); 5:52-6:14 (“The implantation process forms an ‘amorphous’ layer 15 of silicon overlying single crystal silicon material. . . . The amorphous silicon layer has a substantially planar upper surface 19, which also has amorphous characteristics.”); 8:16-18; Figs. 3, 4; <i>see also, e.g.</i>, TSMC1003 at ¶ 36.</p> <p>Cheung discloses that the substrate 10 is doped with impurities including boron or arsenic. <i>See, e.g.</i>, TSMC1005 at 4:15-20; <i>see also, e.g.</i>, TSMC1003 at ¶ 37.</p> |
| <p>a second substrate of substantially one second material amorphized substantially only in a second surface of said second material and containing one of boron and arsenic;</p> | <p>Cheung discloses a substrate 20 of substantially one material, <i>e.g.</i>, silicon. <i>See, e.g.</i>, TSMC1005 at 4:66-5:1. The one material, <i>e.g.</i>, silicon, is amorphized, <i>e.g.</i>, amorphous layer of silicon, substantially only in a surface of the material. <i>See, e.g., id.</i> at 8:21-23, 32-65; <i>see also, e.g.</i>, TSMC1003 at ¶ 36.</p> <p>Cheung discloses that the substrate 20 is doped with impurities including boron or arsenic. <i>See, e.g.</i>, TSMC1005 at 5:4-7; <i>see also, e.g.</i>, TSMC1003 at ¶ 37.</p> |
| <p>said first surface being bonded to said second surface to form a bonded pair of substrates.</p> | <p>Cheung discloses bonding the surface of amorphous silicon layer 15 of substrate 10 with the surface of amorphous layer of silicon of substrate 20. <i>See, e.g.</i>, TSMC1005 at 8:26-29, Col. 8:32-41 (“[T]he present invention provides a method for bonding substrates together using first and second compliant layers of amorphous silicon, for example, on the first substrate and second substrate, respectively.”); Fig. 8; <i>see also, e.g.</i>, TSMC1003 at ¶ 36.</p> |
| <p>54. A structure</p> | <p>Cheung discloses the limitations of Claim 53.</p> |

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| <p>as recited in claim 53, comprising:</p> | |
| <p>one of said first and second substrates of said bonded pair being amorphized only in said first surface and in a third surface of said first material;</p> | <p>Cheung describes bonding the substrates 10 and 20, as discussed above. <i>See, e.g.</i>, TSMC1005 at 8:10-41. Cheung teaches that the invention can be applied “for multi-layered integrated circuit devices, three-dimensional packaging of integrated semiconductor devices,” and more. <i>See, e.g., id.</i> at 1:17-21.</p> <p>Accordingly, it would have been obvious to a person having ordinary skill in the art at the time of the invention to amorphize only the first surface and a third surface of the first material, amorphize another surface of a third material of a third substrate, and bond the surface of the third material to the third surface as recited in Claim 54 to form multi-layered integrated circuit devices or a three-dimensional package as described in Cheung. <i>See also, e.g.</i>, TSMC1003 at ¶ 38. (Petitioner notes “third surface” is used multiple times to refer to differing surfaces and that “said fourth surface” lacks a proper antecedent.)</p> |
| <p>a third substrate of substantially one third material amorphized only in a third surface of said third material; and</p> | <p>Moreover, “the mere duplication of parts has no patentable significance unless a new and unexpected result is produced.” Claim 54 requires nothing more than the duplication of the parts recited in Claim 53, which does not produce any new and/or unexpected results for bonding amorphized surfaces of additional substrates.</p> |
| <p>said third surface bonded to said fourth surface.</p> | |
| <p>55. A structure as recited in claim 53, wherein said first and second substrates are selected from Si, InGaAs, InP, GaAs, Ge and SiC.</p> | <p>Cheung discloses the limitations of Claim 53.</p> <p>Cheung discloses that the substrates are “silicon,” “compound semiconductors and the like,” or “gallium arsenide [(GaAs)], gallium nitride (GaN), and others.” <i>See, e.g.</i>, TSMC1005 at 4:10-15, 25-27; 4:63-5:3; 9:52-53.</p> |

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| <p>56. A structure as recited in claim 53, wherein:</p> | <p>Cheung discloses the limitations of Claim 53.</p> |
| <p>said first and second substrates each comprises a silicon substrate; and</p> | <p>Cheung discloses that each of the substrates 10 and 20 are silicon. <i>See, e.g., id.</i> at 4:10-15; 4:66-5:3.</p> |
| <p>said first and second surfaces each comprises a silicon surface.</p> | <p>Cheung discloses that each of the surfaces of the amorphous silicon layer 15 of substrate 10 and amorphous layer of silicon of substrate 20 is a silicon surface. <i>See, e.g., id.</i> at 8:32-41, 62-65; 5:52-6:14.</p> |
| <p>57. A structure as recited in claim 53, wherein:</p> | <p>Cheung discloses the limitations of Claim 53.</p> |
| <p>said first surface comprises a substantially planar surface of a first silicon layer formed on said first device; and</p> | <p>Cheung discloses the surface 19 of the amorphous silicon layer 15 is “a substantially planar upper surface.” <i>See, e.g., id.</i> at 6:12-14.</p> <p>Cheung discloses that the invention can be applied to “multi-layered integrated circuit devices, three-dimensional packaging of integrated semiconductor devices, photonic devices, piezoelectronic devices, microelectromechanical systems (‘MEMS’), sensors, actuators, solar cells, flat panel displays (e.g., LCD, AMLCD), biological and biomedical devices, and the like.” <i>See, e.g., id.</i> at 1:17-24. (Petitioner notes that “said first device” lacks a proper antecedent.)</p> |
| <p>said second surface comprises a substantially planar surface of a second</p> | <p>Cheung discloses forming a surface of an amorphous layer of silicon. <i>See, e.g., id.</i> at 8:21-23, 32-65. Cheung describes a corresponding amorphous silicon layer as having “a substantially planar upper surface.” <i>See, e.g., id.</i> at 6:12-14.</p> <p>Cheung discloses that the invention can be applied to “multi-</p> |

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| silicon layer formed on said second device. | layered integrated circuit devices, three-dimensional packaging of integrated semiconductor devices, photonic devices, piezoelectronic devices, microelectromechanical systems (“MEMS”), sensors, actuators, solar cells, flat panel displays (e.g., LCD, AMLCD), biological and biomedical devices, and the like.” <i>See, e.g., id.</i> at 1:17-24. (Petitioner notes that “said second device” lacks a proper antecedent.) |
| 58. A structure as recited in claim 53, wherein: | Cheung discloses the limitations of Claim 53. |
| said first surface comprises a surface exposed to a boron-containing plasma; and | The limitation “ <i>exposed</i> to a boron-containing plasma” (emphasis added) is a product-by-process limitation, which only requires Petitioner to show a same structure. To the extent that exposure to a boron-containing plasma requires the surfaces to resultantly contain boron, to which Petitioner does not concede, Cheung discloses that the surface 19 of the amorphous silicon layer 15 of substrate 10 and the surface of the amorphous layer of silicon of substrate 20 each comprise boron. <i>See, e.g.,</i> TSMC1005 at 4:12-20; 5:3-7; 6:9-14; 8:62-65; <i>see also</i> TSMC1003 at ¶ 37. Hence, Cheung discloses a same structure. |
| said second surface comprises a surface exposed to a boron-containing plasma. | |
| 59. A structure as recited in claim 53, wherein: | Cheung discloses the limitations of Claim 53. |
| said first surface comprises a surface implanted with one of boron and arsenic; and | The limitation “ <i>implanted</i> with one of boron and arsenic” (emphasis added) is a product-by-process limitation, which only requires Petitioner to show a same structure. Cheung discloses that the surface 19 of the amorphous silicon layer 15 of substrate 10 and the surface of the amorphous layer of silicon of substrate 20 each comprise boron or arsenic. <i>See, e.g.,</i> TSMC1005 at 4:12-20; 5:3-7; 6:9-14; 8:62-65; <i>see also</i> TSMC1003 at ¶ 37. Hence, Cheung discloses a same structure. |
| said second surface | |

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| comprises a surface implanted with one of boron and arsenic. | |
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Ground 2: Claims 1-14 and 53-60 are rendered obvious over Cheung in view of Saito.

A. Claims 1 and 53: As set forth in GROUND 1, *supra*, Cheung anticipates or renders obvious independent Claims 1 and 53. To the extent that Cheung may not teach nearly-amorphized layers or substrates “containing one of boron and arsenic,” as recited in Claims 1 and 53, respectively, it would have been obvious to a person having ordinary skill in the art at the time of the invention to implant Cheung’s substrates to form first and second “nearly-amorphized” layers (Claim 1) or to form first and second substrates (Claim 53) “containing one of boron and arsenic” using a plasma containing ions of silicon or germanium while simultaneously including ions of one of boron and arsenic as taught by Saito (*see, e.g.,* TSMC1006 at 2:40-59; 3:30-42) in order to dope Cheung’s surfaces with one of boron and arsenic for the formation of a device in the surfaces, such as taught by Cheung, *see* TSMC1005 at 1:19-24. *See also, e.g.,* TSMC1003 at ¶ 39.

B. Claims 2-10, 12-14, and 54-59: As set forth in GROUND 2(A), *supra*, Cheung in combination with Saito teaches the limitations of Claims 1 and 53. Further, as set forth in GROUND 1, *supra*, Cheung teaches the limitations of claims

2-10, 12-14, and 54-59, and hence, these claims are obvious over Cheung in view of Saito. To the extent that Cheung alone does not teach certain limitations of some of these dependent claims, further support is provided *infra* such that those claims are rendered obvious over Cheung and Saito.

C. Claims 6-9, 11-14, and 58-60:

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| 6. A structure as recited in claim 1, wherein: | As set forth in GROUNDS 1 and 2(A), <i>supra</i> , Cheung alone or in combination with Saito teaches the limitations of Claim 1. |
| said first surface comprises a first silicon surface exposed to a boron-containing plasma; and | It would have been obvious to a person having ordinary skill in the art at the time of the invention to expose Cheung's silicon surfaces of the respective substrates to a plasma containing ions of silicon or germanium while simultaneously including ions of boron as taught by Saito (<i>see, e.g.</i> , TSMC1006 at 2:40-59; 3:30-42) in order to dope Cheung's surfaces with boron for the formation of a device in the surfaces, such as taught by Cheung, <i>see</i> TSMC1005 at 1:19-24. <i>See also, e.g.</i> , TSMC1003 at ¶ 39. |
| said second surface comprises a second silicon surface exposed to a boron-containing plasma. | |
| 7. A structure as recited in claim 1, wherein: | As set forth in GROUNDS 1 and 2(A), <i>supra</i> , Cheung alone or in combination with Saito teaches the limitations of Claim 1. |
| said first surface comprises a first silicon surface implanted with boron; and | It would have been obvious to a person having ordinary skill in the art at the time of the invention to implant Cheung's silicon surfaces with boron as described in Saito (<i>see, e.g.</i> , TSMC1006 at 2:40-59; 3:30-42) in order to dope Cheung's surfaces with boron for the formation of a device in the surfaces, such as taught by Cheung, <i>see</i> TSMC1005 at 1:19-24. <i>See also, e.g.</i> , TSMC1003 at ¶ 39. |
| said second surface comprises a second silicon surface implanted with boron. | |
| 8. A structure as recited in claim 1, wherein: | As set forth in GROUNDS 1 and 2(A), <i>supra</i> , Cheung alone or in combination with Saito teaches the |

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| | limitations of Claim 1. |
| said first surface comprises a first silicon surface implanted with arsenic; and | It would have been obvious to a person having ordinary skill in the art at the time of the invention to implant Cheung's silicon surfaces with arsenic as described by Saito (<i>see, e.g.</i> , TSMC1006 at 2:40-59; 3:30-42) in order to dope Cheung's surfaces with arsenic for the formation of a device in the surfaces, such as taught by Cheung, <i>see</i> TSMC1005 at 1:19-24. <i>See, also, e.g.</i> , TSMC1003 at ¶ 39. |
| said second surface comprises a second silicon surface implanted with arsenic. | |
| 9. A structure as recited in claim 1, comprising: | As set forth in GROUNDS 1 and 2(A), <i>supra</i> , Cheung alone or in combination with Saito teaches the limitations of Claim 1. |
| at least one of boron-boron and Si covalent bonds formed between said first and second substrates. | <p>It would have been obvious to a person having ordinary skill in the art at the time of the invention to implant and/or expose Cheung's surfaces with boron as described by Saito (<i>see, e.g.</i>, TSMC1006 at 2:40-59; 3:30-42) in order to dope Cheung's surfaces for the formation of a device in the surfaces, such as taught by Cheung, <i>see</i> TSMC1005 at 1:19-24. <i>See, also, e.g.</i>, TSMC1003 at ¶ 39. With this plasma implant and/or exposure, Cheung's surfaces will have boron atoms. <i>See, e.g.</i>, TSMC1003 at ¶ 40.</p> <p>With Cheung's surfaces being exposed to a boron-containing plasma and having boron atoms thereon, Cheung's bonding process will undergo a same or similar process as described in the '133 Patent to achieve silicon covalent bonds and boron-boron bonds. Particularly, as in Cheung, the '133 Patent teaches that bonding boron treated silicon surfaces with boron atoms on the surfaces results in silicon covalent bonds and boron-boron bonds across the interface, even more at temperatures of 350-400°C. <i>See, e.g.</i>, TSMC1001 at 7:66-8:21. Accordingly, Cheung in combination with Saito will result in silicon covalent bonds and boron-boron bonds. <i>See, also, e.g.</i>, TSMC1003 at ¶ 40. Additionally, in</p> |

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| | <p>proceedings before the Office, where a reason to believe that a claimed limitation may be inherent in the prior art is shown, as is here, the burden shifts to the Patent Owner to provide evidence to the contrary. <i>See, e.g., Precision BioSciences, Inc. v. Institut Pasteur & Universite Pierre et Marie Curie</i>, No. 2011-012285, 2012 WL 1050572 at *3 (B.P.A.I. March 14, 2012); <i>Ice Ban Am., Inc. v. Patent of Sears Ecological Applications Co., LLC</i>, No. 2010-009574, 2010 WL 4913983 at *8 (B.P.A.I. Nov. 30, 2010).</p> |
| <p>11. A structure as recited in claim 1, wherein said first and second layers each comprise a few monolayers of boron.</p> | <p>As set forth in GROUNDS 1 and 2(A), <i>supra</i>, Cheung alone or in combination with Saito teaches the limitations of Claim 1. One skilled in the art would recognize that the energy and dose of B₂H₆ implants as described in Saito would lead to the formation of a few monolayers of boron in the surface of the substrates. <i>See, e.g., TSMC1003</i> at ¶ 41. It would have been obvious to a person having ordinary skill in the art at the time of the invention to implant Cheung’s surfaces with boron as described in Saito (<i>see, e.g., TSMC1006</i> at 2:40-59; 3:30-42), which would result in the formation of a few monolayers of boron in the layers, in order to dope Cheung’s surfaces with boron for the formation of a device in the surfaces, such as taught by Cheung, <i>see TSMC1005</i> at 1:19-24. <i>See also, e.g., TSMC1003</i> at ¶¶ 39, 41.</p> |
| <p>12. A structure as recited in claim 1, wherein:</p> | <p>As set forth in GROUNDS 1 and 2(A), <i>supra</i>, Cheung alone or in combination with Saito teaches the limitations of Claim 1.</p> |
| <p>said first surface comprises an amorphous boron-containing layer; and</p> | <p>It would have been obvious to a person having ordinary skill in the art at the time of the invention to implant Cheung’s surfaces with boron as described in Saito (<i>see, e.g., TSMC1006</i> at 2:40-59; 3:30-42) to form the surfaces to comprise an amorphous boron-containing layer in order to dope Cheung’s surfaces with boron for the formation of a device in the</p> |
| <p>said second surface comprises an amorphous boron-containing layer.</p> | |

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| | surfaces, such as taught by Cheung, <i>see</i> TSMC1005 at 1:19-24. <i>See also, e.g.</i> , TSMC1003 at ¶ 39. |
| 13. A structure as recited in claim 1, wherein: | As set forth in GROUNDS 1 and 2(A), <i>supra</i> , Cheung alone or in combination with Saito teaches the limitations of Claim 1. |
| said first surface comprises a surface exposed to a boron-containing plasma; and | It would have been obvious to a person having ordinary skill in the art at the time of the invention to expose Cheung's silicon surfaces of the respective substrates to a plasma containing ions of silicon or germanium while simultaneously including ions of boron as taught by Saito (<i>see, e.g.</i> , TSMC1006 at 2:40-59; 3:30-42) in order to dope Cheung's surfaces with boron for the formation of a device in the surfaces, such as taught by Cheung, <i>see</i> TSMC1005 at 1:19-24. <i>See also, e.g.</i> , TSMC1003 at ¶ 39. |
| said second surface comprises a surface exposed to a boron-containing plasma. | |
| 14. A structure as recited in claim 1, wherein: | As set forth in GROUNDS 1 and 2(A), <i>supra</i> , Cheung alone or in combination with Saito teaches the limitations of Claim 1. |
| said first surface comprises a first surface exposed to an inert gas plasma; and | Saito further describes that argon may be used as a carrier gas for the plasma ion implantation. <i>See, e.g.</i> , TSMC1006 at 4:26-27. A plasma containing silicon or germanium with a carrier gas such as argon may be formed in Saito's plasma chamber, which may be used to form Saito's amorphous regions. <i>See, e.g.</i> , TSMC1006 at 4:22-32; FIG. 1. It would have been obvious to a person having ordinary skill in the art at the time of the invention to use a plasma that contains silicon or germanium, as taught by both Cheung and Saito, and an inert gas such as argon for a carrier, as taught by Saito, in order to form Cheung's amorphous surfaces. <i>See, e.g.</i> , TSMC1003 at ¶¶ 35, 42. Using argon as a carrier gas to implant silicon or germanium is a simple substitution of one known technique for another known technique to obtain the predictable result of amorphizing a substrate. <i>See, e.g., KSR Intn'l Co. v. Teleflex Inc.</i> , 550 U.S. 398, 416 (2007). |
| said second surface comprises a second surface exposed to an inert gas plasma. | |

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| <p>58. A structure as recited in claim 53, wherein:</p> | <p>As set forth in GROUNDS 1 and 2(A), <i>supra</i>, Cheung alone or in combination with Saito teaches the limitations of Claim 53.</p> |
| <p>said first surface comprises a surface exposed to a boron-containing plasma; and</p> | <p>It would have been obvious to a person having ordinary skill in the art at the time of the invention to expose Cheung's silicon surfaces of the respective substrates to a plasma containing ions of silicon or germanium while simultaneously including ions of boron as taught by Saito (<i>see, e.g.</i>, TSMC1006 at 2:40-59; 3:30-42) in order to dope Cheung's surfaces with boron for the formation of a device in the surfaces, such as taught by Cheung, <i>see</i> TSMC1005 at 1:19-24. <i>See also, e.g.</i>, TSMC1003 at ¶ 39.</p> |
| <p>said second surface comprises a surface exposed to a boron-containing plasma.</p> | |
| <p>59. A structure as recited in claim 53, wherein:</p> | <p>As set forth in GROUNDS 1 and 2(A), <i>supra</i>, Cheung alone or in combination with Saito teaches the limitations of Claim 53.</p> |
| <p>said first surface comprises a surface implanted with one of boron and arsenic; and</p> | <p>It would have been obvious to a person having ordinary skill in the art at the time of the invention to implant Cheung's surfaces with one of boron and arsenic as described by Saito (<i>see, e.g.</i>, TSMC1006 at 2:40-59; 3:30-42) in order to dope Cheung's surfaces for the formation of a device in the surfaces, such as taught by Cheung, <i>see</i> TSMC1005 at 1:19-24. <i>See, also, e.g.</i>, TSMC1003 at ¶ 39.</p> |
| <p>said second surface comprises a surface implanted with one of boron and arsenic.</p> | |
| <p>60. A structure as recited in claim 59, comprising:</p> | <p>As set forth in GROUNDS 1, 2(B), and 2(C), <i>supra</i>, Cheung alone or in combination with Saito teaches the limitations of Claim 59.</p> |
| <p>boron-boron covalent bonds formed between said first and second substrates.</p> | <p>It would have been obvious to a person having ordinary skill in the art at the time of the invention to implant and/or expose Cheung's surfaces with boron as described by Saito (<i>see, e.g.</i>, TSMC1006 at 2:40-59; 3:30-42) in order to dope Cheung's surfaces for the formation of a device in the surfaces, such as taught by Cheung, <i>see</i> TSMC1005 at 1:19-24. <i>See, also, e.g.</i>, TSMC1003 at ¶ 39. With this plasma implant and/or exposure, Cheung's surfaces will have</p> |

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| | <p>boron atoms. <i>See, e.g.</i>, TSMC1003 at ¶ 40.</p> <p>With Cheung's surfaces being exposed to a boron-containing plasma and having boron atoms thereon, Cheung's bonding process will undergo a same or similar process as described in the '133 Patent to achieve boron-boron covalent bonds. Particularly, as in Cheung, the '133 Patent teaches that bonding boron treated silicon surfaces with boron atoms on the surfaces results in boron-boron covalent bonds across the interface, even more at temperatures of 350-400°C. <i>See, e.g.</i>, TSMC1001 at 7:66-8:21. Accordingly, Cheung in combination with Saito will result in boron-boron covalent bonds. <i>See, also, e.g.</i>, TSMC1003 at ¶ 40. Additionally, in proceedings before the Office, where a reason to believe that a claimed limitation may be inherent in the prior art is shown, as is here, the burden shifts to the Patent Owner to provide evidence to the contrary.</p> |
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GROUND 3: Claims 1-14 and 53-59 are rendered obvious over Cheung in view of Tian.

A. Claims 1 and 53: As set forth in GROUND 1, *supra*, Cheung anticipates or renders obvious independent Claims 1 and 53. To the extent that Cheung may not teach nearly-amorphized layers or substrates “containing one of boron and arsenic,” as recited in Claims 1 and 53, respectively, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the plasma ion implantation, as taught by Cheung, to include the boron or arsenic implantation, as taught or suggested by Tian (*see, e.g.*, TSMC1008 at Abstract, 1230), such that the amorphous layers contain one of boron and arsenic, to dope

Cheung's surfaces with one of boron and arsenic for the formation of a device in the surfaces, such as taught by Cheung, *see* TSMC1005 at 1:19-24. *See also, e.g.*, TSMC1003 at ¶ 43.

B. Claims 2-10, 12-14, and 54-59: As set forth in GROUND 3(A), *supra*, Cheung in combination with Tian teaches the limitations of Claims 1 and 53. Further, as set forth in GROUND 1, *supra*, Cheung teaches the limitations of claims 2-10, 12-14, and 54-59, and hence, these claims are obvious over Cheung in view of Tian. To the extent that Cheung alone does not teach certain limitations of some of these dependent claims, further support is provided *infra* such that those claims are rendered obvious over Cheung and Tian.

C. Claims 7, 8, 11, 12, and 59:

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| 7. A structure as recited in claim 1, wherein: | As set forth in GROUNDS 1 and 3(A), <i>supra</i> , Cheung alone or in combination with Tian teaches the limitations of Claim 1. |
| said first surface comprises a first silicon surface implanted with boron; and | It would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the plasma ion implantation, as taught by Cheung, to include the boron implantation, as taught or suggested by Tian (<i>see, e.g.</i> , TSMC1008 at Abstract, 1230), to dope Cheung's surfaces with boron for the formation of a device in the surfaces, such as taught by Cheung, <i>see</i> TSMC1005 at 1:19-24. <i>See also, e.g.</i> , TSMC1003 at ¶ 43. |
| said second surface comprises a second silicon surface implanted with boron. | |
| 8. A structure as recited in claim 1, wherein: | As set forth in GROUNDS 1 and 3(A), <i>supra</i> , Cheung alone or in combination with Tian teaches the limitations of Claim 1. |

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| <p>said first surface comprises a first silicon surface implanted with arsenic; and</p> | <p>It would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the plasma ion implantation, as taught by Cheung, to include the arsenic implantation, as taught or suggested by Tian (<i>see, e.g.</i>, TSMC1008 at Abstract, 1230), to dope Cheung’s surfaces with arsenic for the formation of a device in the surfaces, such as taught by Cheung, <i>see</i> TSMC1005 at 1:19-24. <i>See also, e.g.</i>, TSMC1003 at ¶ 43.</p> |
| <p>said second surface comprises a second silicon surface implanted with arsenic.</p> | |
| <p>11. A structure as recited in claim 1, wherein said first and second layers each comprise a few monolayers of boron.</p> | <p>As set forth in GROUNDS 1 and 3(A), <i>supra</i>, Cheung alone or in combination with Tian teaches the limitations of Claim 1. One of ordinary skill in the art would know that by controlling the dose and energy of a boron species in an ion shower or ion implantation, a region having a thickness of a few monolayers at or near the surface of the substrate would be boron rich. <i>See, e.g.</i>, TSMC1003 at ¶ 44. It would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the plasma ion implantation, as taught by Cheung, to include the boron implantation, as taught or suggested by Tian (<i>see, e.g.</i>, TSMC1008 at Abstract, 1230), which would result in the formation of a few monolayers of boron in the layers, to dope Cheung’s surfaces with boron for the formation of a device in the surfaces, such as taught by Cheung, <i>see</i> TSMC1005 at 1:19-24. <i>See also, e.g.</i>, TSMC1003 at ¶ 43.</p> |
| <p>12. A structure as recited in claim 1, wherein:</p> | <p>As set forth in GROUNDS 1 and 3(A), <i>supra</i>, Cheung alone or in combination with Tian teaches the limitations of Claim 1.</p> |
| <p>said first surface comprises an amorphous boron-containing layer; and</p> | <p>It would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the plasma ion implantation, as taught by Cheung, to include the boron implantation, as taught or suggested by Tian (<i>see, e.g.</i>, TSMC1008 at Abstract, 1230), such that Cheung’s surfaces comprise an amorphous boron-containing layer, to dope</p> |
| <p>said second surface comprises an amorphous boron-containing layer.</p> | |

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| | Cheung’s surfaces with boron for the formation of a device in the surfaces, <i>see</i> TSMC1005 at 1:19-24. <i>See also, e.g.</i> , TSMC1003 at ¶ 43. |
| 59. A structure as recited in claim 53, wherein: | As set forth in GROUNDS 1 and 3(A), <i>supra</i> , Cheung alone or in combination with Tian teaches the limitations of Claim 53. |
| said first surface comprises a surface implanted with one of boron and arsenic; and | It would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the plasma ion implantation, as taught by Cheung, to include the boron or arsenic implantation, as taught or suggested by Tian (<i>see, e.g.</i> , TSMC1008 at Abstract, 1230), to dope Cheung’s surfaces with one of boron and arsenic for the formation of a device in the surfaces, such as taught by Cheung, <i>see</i> TSMC1005 at 1:19-24. <i>See also, e.g.</i> , TSMC1003 at ¶ 43. |
| said second surface comprises a surface implanted with one of boron and arsenic. | |

Ground 4: Claims 1-14 and 53-60 are rendered obvious over Cheung in view of Tian, and in further view of Saito.

A. Claims 1 and 53: As set forth in GROUNDS 1 and 3(A), *supra*, Cheung anticipates or renders obvious or Cheung in combination with Tian renders obvious independent Claims 1 and 53. To the extent that Cheung alone or in combination with Tian may not teach nearly-amorphized layers or substrates “containing one of boron and arsenic,” as recited in Claims 1 and 53, respectively, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the implantation of silicon ions and boron or arsenic ions as described in Cheung and/or Tian to be a plasma ion implantation containing silicon ions and boron or arsenic ions as described in Saito (*see, e.g.*, TSMC1006 at 2:40-59; 3:30-

42) in order to dope boron or arsenic into surfaces for the formation of a device in the surfaces, such as taught by Cheung, *see* TSMC1005 at 1:19-24. *See also, e.g.*, TSMC1003 at ¶ 45.

B. Claims 2-14, and 54-59: As set forth in GROUND 4(A), *supra*, Cheung in combination with Tian and Saito teaches the limitations of Claims 1 and 53. Further, as set forth in GROUNDS 1 and 3, *supra*, Cheung alone or in combination with Tian teaches the limitations of claims 2-14, and 54-59, and hence, these claims are obvious over Cheung in view of Tian and Saito. To the extent that Cheung alone does not teach certain limitations of some of these dependent claims, further support is provided *infra* such that those claims are rendered obvious over Cheung, Tian, and Saito.

C. Claims 6, 9, 13, 14, 58, and 60:

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| 6. A structure as recited in claim 1, wherein: | As set forth in GROUNDS 1 and 4(A), <i>supra</i> , Cheung alone or in combination with Tian and Saito teaches the limitations of Claim 1. |
| said first surface comprises a first silicon surface exposed to a boron-containing plasma; and | It would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the implantation of silicon ions and boron ions as described in Cheung and/or Tian to use a plasma ion implantation containing silicon ions and boron ions as described in Saito (<i>see, e.g.</i> , TSMC1006 at 2:40-59; 3:30-42) in order to dope boron into surfaces for the formation of a device in the surfaces, such as taught by Cheung, <i>see</i> TSMC1005 at 1:19-24. <i>See also, e.g.</i> , TSMC1003 at ¶ 45. |
| said second surface comprises a second silicon surface exposed to a boron-containing plasma. | |

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| <p>9. A structure as recited in claim 1, comprising:</p> | <p>As set forth in GROUNDS 1 and 4(A), <i>supra</i>, Cheung alone or in combination with Tian and Saito teaches the limitations of Claim 1.</p> |
| <p>at least one of boron-boron and Si covalent bonds formed between said first and second substrates.</p> | <p>It would have been obvious to a person having ordinary skill in the art at the time of the invention to implant and/or expose Cheung's surfaces with boron as described by Saito (<i>see, e.g.</i>, TSMC1006 at 2:40-59; 3:30-42) in order to dope Cheung's surfaces for the formation of a device in the surfaces, such as taught by Cheung, <i>see</i> TSMC1005 at 1:19-24. <i>See, also, e.g.</i>, TSMC1003 at ¶ 45. With this plasma implant and/or exposure, Cheung's surfaces will have boron atoms. <i>See, e.g., id.</i> at ¶ 46.</p> <p>With Cheung's surfaces being exposed to a boron-containing plasma and having boron atoms thereon, Cheung's bonding process will undergo a same or similar process as described in the '133 Patent to achieve silicon covalent bonds and boron-boron bonds. Particularly, as in Cheung, the '133 Patent teaches that bonding boron treated silicon surfaces with boron atoms on the surfaces results in silicon covalent bonds and boron-boron bonds across the interface, even more at temperatures of 350-400°C. <i>See, e.g.</i>, TSMC1001 at 7:66-8:21. Accordingly, Cheung and Tian in combination with Saito will result in silicon covalent bonds and boron-boron bonds. <i>See, also, e.g.</i>, TSMC1003 at ¶ 46.</p> <p>Additionally, in proceedings before the Office, where a reason to believe that a claimed limitation may be inherent in the prior art is shown, as is here, the burden shifts to the Patent Owner to provide evidence to the contrary.</p> |
| <p>13. A structure as recited in claim 1, wherein:</p> | <p>As set forth in GROUNDS 1 and 4(A), <i>supra</i>, Cheung alone or in combination with Tian and Saito teaches the limitations of Claim 1.</p> |
| <p>said first surface</p> | <p>It would have been obvious to a person having</p> |

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| <p>comprises a surface exposed to a boron-containing plasma; and</p> | <p>ordinary skill in the art at the time of the invention to modify the implantation of silicon ions and boron ions as described in Cheung and/or Tian to use a plasma ion implantation containing silicon ions and boron ions as described in Saito (<i>see, e.g.,</i> TSMC1006 at 2:40-59; 3:30-42) in order to dope boron into surfaces for the formation of a device in the surfaces, such as taught by Cheung, <i>see</i> TSMC1005 at 1:19-24. <i>See also, e.g.,</i> TSMC1003 at ¶ 45.</p> |
| <p>said second surface comprises a surface exposed to a boron-containing plasma.</p> | |
| <p>14. A structure as recited in claim 1, wherein:</p> | <p>As set forth in GROUNDS 1 and 4(A), <i>supra</i>, Cheung alone or in combination with Tian and Saito teaches the limitations of Claim 1.</p> |
| <p>said first surface comprises a first surface exposed to an inert gas plasma; and</p> | <p>Saito further describes that argon may be used as a carrier gas for the plasma ion implantation. <i>See, e.g.,</i> TSMC1006 at 4:26-27. A plasma containing silicon or germanium with a carrier gas such as argon may be formed in Saito's plasma chamber, which may be used to form Saito's amorphous regions. <i>See, e.g.,</i> TSMC1006 at 4:22-32; FIG. 1. It would have been obvious to a person having ordinary skill in the art at the time of the invention to use a plasma that contains silicon or germanium, as taught by both Cheung and/or Tian, and an inert gas such as argon for a carrier, as taught by Saito, in order to form amorphous surfaces. <i>See, e.g.,</i> TSMC1003 at ¶¶ 35, 47. Using argon as a carrier gas to implant silicon or germanium is a simple substitution of one known technique for another known technique to obtain the predictable result of amorphizing a substrate.</p> |
| <p>said second surface comprises a second surface exposed to an inert gas plasma.</p> | |
| <p>58. A structure as recited in claim 53, wherein:</p> | <p>As set forth in GROUNDS 1 and 4(A), <i>supra</i>, Cheung alone or in combination with Tian and Saito teaches the limitations of Claim 53.</p> |
| <p>said first surface comprises a surface exposed to a boron-containing plasma; and</p> | <p>It would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the implantation of silicon ions and boron ions as described in Cheung and/or Tian to use a</p> |

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| <p>said second surface comprises a surface exposed to a boron-containing plasma.</p> | <p>plasma ion implantation containing silicon ions and boron ions as described in Saito (<i>see, e.g.</i>, TSMC1006 at 2:40-59; 3:30-42) in order to dope boron into surfaces for the formation of a device in the surfaces, such as taught by Cheung, <i>see</i> TSMC1005 at 1:19-24. <i>See also, e.g.</i>, TSMC1003 at ¶ 45.</p> |
| <p>60. A structure as recited in claim 59, comprising:</p> | <p>As set forth in GROUNDS 1, 3(B), 3(C), and 4(B), <i>supra</i>, Cheung alone or in combination with Tian and Saito teaches the limitations of Claim 59.</p> |
| <p>boron-boron covalent bonds formed between said first and second substrates.</p> | <p>It would have been obvious to a person having ordinary skill in the art at the time of the invention to implant and/or expose Cheung's surfaces with boron as described by Saito (<i>see, e.g.</i>, TSMC1006 at 2:40-59; 3:30-42) in order to dope Cheung's surfaces for the formation of a device in the surfaces, such as taught by Cheung, <i>see</i> TSMC1005 at 1:19-24. <i>See, also, e.g.</i>, TSMC1003 at ¶ 45. With this plasma implant and/or exposure, Cheung's surfaces will have boron atoms. <i>See, e.g., id.</i> at ¶ 46.</p> <p>With Cheung's surfaces being exposed to a boron-containing plasma and having boron atoms thereon, Cheung's bonding process will undergo a same or similar process as described in the '133 Patent to achieve boron-boron covalent bonds. Particularly, as in Cheung, the '133 Patent teaches that bonding boron treated silicon surfaces with boron atoms on the surfaces results in boron-boron covalent bonds across the interface, even more at temperatures of 350-400°C. <i>See, e.g.</i>, TSMC1001 at 7:66-8:21. Accordingly, Cheung and Tian in combination with Saito will result in boron-boron covalent bonds. <i>See, also, e.g.</i>, TSMC1003 at ¶ 46. Additionally, in proceedings before the Office, where a reason to believe that a claimed limitation may be inherent in the prior art is shown, as is here, the burden shifts to the Patent Owner to provide evidence to the contrary.</p> |

GROUND 5: Claims 1-7, 9, 10, 12, 13, 53-56, 58, and 59 are anticipated by or rendered obvious over Fujino.

| Claims | Fujino |
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| 1. A bonded structure, comprising: | Fujino discloses silicon wafer direct bonding. <i>See, e.g.</i> , TSMC1007 at Title. |
| a first substrate having a first surface, a first nearly-amorphized layer containing one of boron and arsenic formed uniformly over said first surface; and | Fujino discloses bonding “boron-doped, CZ-grown silicon wafers.” <i>See, e.g., id.</i> at 1322; <i>see also id.</i> at Fig. 1. Fujino describes that “[s]ilicon ions were implanted to make the silicon wafer surface amorphous,” and amorphous layers on wafers. <i>See, e.g., id.</i> Since Fujino discloses amorphous layers, Fujino discloses layers that each at least closely approximates an amorphous layer, <i>i.e.</i> , a nearly-amorphized layer. <i>See, e.g.</i> , TSMC1003 at ¶ 48. |
| a second substrate having a second surface, a second nearly-amorphized layer containing one of boron and arsenic formed uniformly over said second surface; | Fujino discloses that the wafers are each doped with boron. <i>See, e.g.</i> , TSMC1007 at 1322. Thus, Fujino’s amorphous layers each contain one of boron and arsenic. <i>See, e.g.</i> , TSMC1003 at ¶ 49. Fujino discloses eliminating a native oxide film from the surfaces of the wafers prior to bonding the amorphous surface layers, thus leaving the boron-doped silicon as the surface. <i>See, e.g.</i> , TSMC1007 at 1324. |
| said first surface being bonded to said second surface to form a bonded pair of substrates. | Fujino describes bonding the wafers having amorphous layers. <i>See, e.g., id.</i> at 1322 (The “wafers were bonded to each other under atmospheric pressure at room temperature.”), 1323 (describing results of bonding the “wafers with amorphous layer[s]”). |
| 2. A structure as recited in claim 1, comprising: | Fujino discloses the limitations of Claim 1. |
| one of said first and second substrates of said bonded pair | “[T]he mere duplication of parts has no patentable significance unless a new and unexpected result is produced.” Claim 2 requires nothing more than the |

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| <p>having a third surface, said third surface having a nearly-amorphized layer;</p> | <p>duplication of the parts recited in Claim 1, which does not produce any new and/or unexpected results for bonding nearly-amorphized layers of additional substrates.</p> |
| <p>a third substrate having a fourth surface, a fourth nearly-amorphized layer formed in said fourth surface; and</p> | |
| <p>said third surface bonded to said fourth surface.</p> | |
| <p>3. A structure as recited in claim 1, wherein said first and second substrates are selected from Si, InGaAs, InP, GaAs, Ge and SiC.</p> | <p>Fujino discloses the limitations of Claim 1. Fujino discloses that the wafers are silicon. <i>See, e.g.</i>, TSMC1007 at 1322.</p> |
| <p>4. A structure as recited in claim 1, wherein:</p> | <p>Fujino discloses the limitations of Claim 1.</p> |
| <p>said first and second substrates each comprises a silicon substrate; and</p> | <p>Fujino discloses that the wafers are silicon substrates. <i>See, e.g., id.</i> at 1322.</p> |
| <p>said first and second surfaces each comprises a silicon surface.</p> | <p>Fujino discloses eliminating a native oxide film from the surfaces of the wafers prior to bonding the amorphous surfaces. <i>See, e.g., id.</i> at 1324. Accordingly, each of the surfaces comprises a silicon surface.</p> |
| <p>5. A structure as recited in claim 1, wherein:</p> | <p>Fujino discloses the limitations of Claim 1.</p> |

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| <p>said first and second substrates comprise respective first and second semiconductor devices.</p> | <p>Fujino discloses that silicon wafer direct bonding can be used for “isolated vertical-DMOS and control circuits on a single chip.” <i>See, e.g., id.</i> at 1:17-24.</p> |
| <p>6. A structure as recited in claim 1, wherein:</p> | <p>Fujino discloses the limitations of Claim 1.</p> |
| <p>said first surface comprises a first silicon surface exposed to a boron-containing plasma; and</p> | <p>The limitation “<i>exposed</i> to a boron-containing plasma” (emphasis added) is a product-by-process limitation, which only requires Petitioner to show a same structure.</p> <p>To the extent that exposure to a boron-containing plasma requires the surfaces to resultantly contain boron, to which Petitioner does not concede, Fujino teaches that the surfaces each are silicon and comprise boron. <i>See, e.g.,</i> TSMC1007 at 1322, 1324; <i>see also</i> TSMC 1003 at ¶ 49. Fujino discloses eliminating a native oxide film from the surfaces of the wafers prior to bonding the amorphous surfaces. <i>See, e.g.,</i> TSMC1007 at 1324. Accordingly, each of the surfaces comprises a silicon surface. Hence, Fujino teaches a same structure.</p> |
| <p>said second surface comprises a second silicon surface exposed to a boron-containing plasma.</p> | |
| <p>7. A structure as recited in claim 1, wherein:</p> | <p>Fujino discloses the limitations of Claim 1.</p> |
| <p>said first surface comprises a first silicon surface implanted with boron; and</p> | <p>The limitation “<i>implanted</i> with boron” (emphasis added) is a product-by-process limitation, which only requires Petitioner to show a same structure.</p> <p>Fujino teaches that the surfaces each are silicon and comprise boron. <i>See, e.g.,</i> TSMC1007 at 1322, 1324; <i>see also</i> TSMC 1003 at ¶ 49. Fujino discloses eliminating a native oxide film from the surfaces of the wafers prior to bonding the amorphous surfaces. <i>See, e.g.,</i> TSMC1007 at 1324. Accordingly, each of the surfaces comprises a silicon surface. Hence, Fujino teaches a same structure.</p> |
| <p>said second surface comprises a second silicon surface implanted with boron.</p> | |

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| <p>9. A structure as recited in claim 1, comprising:</p> | <p>Fujino discloses the limitations of Claim 1.</p> |
| <p>at least one of boron-boron and Si covalent bonds formed between said first and second substrates.</p> | <p>Fujino discloses a method for “Silicon Wafer Direct Bonding.” <i>See, e.g.</i>, TSMC1007 at 1322. Fujino discloses “removal of contamination” and “surface treatment” steps on the silicon surfaces of the wafers. <i>See, e.g., id.</i> at Fig. 1; <i>see also id.</i> at 1324 (minimizing SiO layer by eliminating the native oxide). The subsequent contacting and annealing steps, <i>see, e.g., id.</i> at Fig. 1, form a bond between silicon atoms in the silicon surface, which is a covalent bond since silicon-to-silicon bonding occurs by covalent bonding. <i>See, e.g.</i>, TSMC1003 at ¶ 50.</p> |
| <p>10. A structure as recited in claim 1, wherein:</p> | <p>Fujino discloses the limitations of Claim 1.</p> |
| <p>said first and second amorphous layers are each in the range of a few nm in thickness.</p> | <p>Fujino discloses forming an amorphous silicon layer to a depth of 139 nm. <i>See, e.g.</i>, TSMC1007 at 1323. Hence, Fujino discloses a thickness in the range of 165 nm, <i>i.e.</i>, a range of a few nm in thickness.</p> <p>Assuming for the sake of argument that Fujino’s disclosure does not anticipate the claim, Fujino’s range overlaps the range of a few nm in thickness, and therefore, Fujino renders Claim 10 <i>prima facie</i> obvious.</p> <p>Even assuming further for the sake of argument that Fujino’s disclosure does not overlap, “it is not inventive to discover the optimum or workable ranges by routine experimentation.” Fujino teaches that “the thickness of the amorphous layer was varied by adjusting the acceleration energy.” <i>Id.</i> at 1322. The range of thickness of a few nm could be determined by a person having ordinary skill in the art at the time of the invention by routine experimentation. <i>See, e.g.</i>, TSMC1003 at ¶ 51.</p> |
| <p>12. A structure as</p> | <p>Fujino discloses the limitations of Claim 1.</p> |

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| <p>recited in claim 1, wherein:</p> | |
| <p>said first surface comprises an amorphous boron-containing layer; and</p> | <p>Fujino discloses surfaces of amorphous layers of silicon wafers. <i>See, e.g.</i>, TSMC1007 at 1322. Fujino discloses that the silicon wafers are boron-doped. <i>See, e.g., id.</i> Thus, Fujino’s amorphous layers contain boron. <i>See, e.g.</i>, TSMC1003 at ¶ 49. Fujino discloses eliminating a native oxide film from the surfaces of the wafers prior to bonding the amorphous surface layers, thus leaving the boron-doped silicon as the surface. <i>See, e.g.</i>, TSMC1007 at 1324.</p> |
| <p>said second surface comprises an amorphous boron-containing layer.</p> | |
| <p>13. A structure as recited in claim 1, wherein:</p> | <p>Fujino discloses the limitations of Claim 1.</p> |
| <p>said first surface comprises a surface exposed to a boron-containing plasma; and</p> | <p>The limitation “exposed to a boron-containing plasma” (emphasis added) is a product-by-process limitation, which only requires Petitioner to show a same structure.</p> <p>To the extent that exposure to a boron-containing plasma requires the surfaces to resultantly contain boron, to which Petitioner does not concede, Fujino discloses that the wafers each are boron-doped. <i>See, e.g.</i>, TSMC1007 at 1322. Thus, Fujino’s surfaces of the amorphous silicon layers each contain boron. <i>See, e.g.</i>, TSMC1003 at ¶ 49. Hence, Fujino teaches a same structure.</p> |
| <p>said second surface comprises a surface exposed to a boron-containing plasma.</p> | |
| <p>53. A bonded structure, comprising:</p> | <p>Fujino discloses silicon wafer direct bonding. <i>See, e.g.</i>, TSMC1007 at Title.</p> |
| <p>a first substrate of substantially one first material amorphized substantially only in a first surface of said first material and containing one of boron and arsenic; and</p> | <p>Fujino discloses bonding “boron-doped, CZ-grown silicon wafers.” <i>See, e.g., id.</i> at 1322. Fujino describes that “[s]ilicon ions were implanted to make the silicon wafer surface amorphous.” <i>See, e.g., id.</i></p> <p>Fujino discloses eliminating a native oxide film from the surfaces of the wafers prior to bonding the amorphous surface layers, thus leaving the boron-doped silicon as the surfaces. <i>See, e.g., id.</i> at 1324.</p> |

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| <p>a second substrate of substantially one second material amorphized substantially only in a second surface of said second material and containing one of boron and arsenic;</p> | <p>Thus, Fujino describes substrates each of substantially one material amorphized substantially only in a respective surface of the material and each containing one of boron and arsenic. <i>See, e.g.</i>, TSMC1003 at ¶¶ 52, 53.</p> |
| <p>said first surface being bonded to said second surface to form a bonded pair of substrates.</p> | <p>Fujino describes bonding the wafers having amorphized surface layers. <i>See, e.g.</i>, TSMC1007 at 1322 (The “wafers were bonded to each other under atmospheric pressure at room temperature.”), 1323 (describing results of bonding the “wafers with amorphous layer[s]”).</p> <p>Thus, Fujino describes bonding the first surface to the second surface to form a bonded pair of substrates. <i>See, e.g.</i>, TSMC1003 at ¶ 52.</p> |
| <p>54. A structure as recited in claim 53, comprising:</p> | <p>Fujino discloses the limitations of Claim 53.</p> |
| <p>one of said first and second substrates of said bonded pair being amorphized only in said first surface and in a third surface of said first material;</p> | <p>“[T]he mere duplication of parts has no patentable significance unless a new and unexpected result is produced.” Claim 54 requires nothing more than the duplication of the parts recited in Claim 53, which does not produce any new and/or unexpected results for bonding amorphized surfaces of additional substrates.</p> |
| <p>a third substrate of substantially one third material amorphized only in a third surface of said third material; and</p> | |
| <p>said third surface bonded to said fourth</p> | |

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| surface. | |
| 55. A structure as recited in claim 53, wherein said first and second substrates are selected from Si, InGaAs, InP, GaAs, Ge and SiC. | Fujino discloses the limitations of Claim 53. Fujino discloses that the first and second wafers are silicon. <i>See, e.g.</i> , TSMC1007 at 1322. |
| 56. A structure as recited in claim 53, wherein: | Fujino discloses the limitations of Claim 53. |
| said first and second substrates each comprises a silicon substrate; and | Fujino discloses that the wafers are silicon substrates. <i>See, e.g., id.</i> at 1322. |
| said first and second surfaces each comprises a silicon surface. | Fujino discloses eliminating a native oxide film from the surfaces of the wafers prior to bonding the amorphized surfaces. <i>See, e.g., id.</i> at 1324. Accordingly, each of the surfaces comprises a silicon surface. |
| 58. A structure as recited in claim 53, wherein: | Fujino discloses the limitations of Claim 53. |
| said first surface comprises a surface exposed to a boron-containing plasma; and | The limitation “ <i>exposed</i> to a boron-containing plasma” (emphasis added) is a product-by-process limitation, which only requires Petitioner to show a same structure. To the extent that exposure to a boron-containing plasma requires the surfaces to resultantly contain boron, to which Petitioner does not concede, Fujino teaches that the surfaces each comprise boron. <i>See, e.g.</i> , TSMC1007 at 1322; <i>see also</i> TSMC 1003 at ¶ 53. Hence, Fujino teaches a same structure. |
| said second surface comprises a surface exposed to a boron-containing plasma. | |
| 59. A structure as recited in claim 53, wherein: | Fujino describes the limitations of Claim 53. |

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| <p>said first surface comprises a surface implanted with one of boron and arsenic; and</p> | <p>The limitation “<i>implanted</i> with one of boron and arsenic” (emphasis added) is a product-by-process limitation, which only requires Petitioner to show a same structure.</p> |
| <p>said second surface comprises a surface implanted with one of boron and arsenic.</p> | <p>Fujino teaches that the surfaces each comprise boron. <i>See, e.g.</i>, TSMC1007 at 1322; <i>see also</i> TSMC 1003 at ¶ 53. Hence, Fujino teaches a same structure.</p> |

Ground 6: Claims 1-14, 53-56, and 58-60 are rendered obvious over Fujino in view of Saito.

A. Claims 1 and 53: As set forth in GROUND 5, *supra*, Fujino anticipates or renders obvious independent Claims 1 and 53. To the extent that Fujino may not teach nearly-amorphized layers or substrates “containing one of boron and arsenic,” as recited in Claims 1 and 53, respectively, it would have been obvious to a person having ordinary skill in the art at the time of the invention to implant Fujino’s substrates to form first and second “nearly-amorphized” layers (Claim 1) or to form first and second substrates (Claim 53) “containing one of boron and arsenic” using a plasma containing ions of silicon or germanium while simultaneously including ions of one of boron and arsenic as taught by Saito (*see, e.g.*, TSMC1006 at 2:40-59; 3:30-42) in order to dope Fujino’s surfaces with one of boron and arsenic for the formation of a device in the surfaces. *See also, e.g.*, TSMC1003 at ¶ 54.

B. Claims 2-7, 9, 10, 12, 13, 54-56, 58, and 59: As set forth in GROUND

6(A), *supra*, Fujino in combination with Saito teaches the limitations of Claims 1 and 53. Further, as set forth in GROUND 5, *supra*, Fujino teaches the limitations of claims 2-7, 9, 10, 12, 13, 54-56, 58, and 59, and hence, these claims are obvious over Fujino in view of Saito. To the extent that Fujino alone does not teach certain limitations of some of these dependent claims, further support is provided *infra* such that those claims are rendered obvious over Fujino and Saito

C. Claims 6-9, 11-14, and 58-60:

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| 6. A structure as recited in claim 1, wherein: | As set forth in GROUNDS 5 and 6(A), <i>supra</i> , Fujino alone or in combination with Saito teaches the limitations of Claim 1. |
| said first surface comprises a first silicon surface exposed to a boron-containing plasma; and | It would have been obvious to a person having ordinary skill in the art at the time of the invention to expose Fujino’s silicon surfaces of the wafers to a plasma containing ions of silicon while simultaneously including ions of boron as taught by Saito (<i>see, e.g.</i> , TSMC1006 at 2:40-59; 3:30-42) in order to dope Fujino’s surfaces with boron for the formation of a device in the surfaces. <i>See also, e.g.</i> , TSMC1003 at ¶ 54. |
| said second surface comprises a second silicon surface exposed to a boron-containing plasma. | |
| 7. A structure as recited in claim 1, wherein: | As set forth in GROUNDS 5 and 6(A), <i>supra</i> , Fujino alone or in combination with Saito teaches the limitations of Claim 1. |
| said first surface comprises a first silicon surface implanted with boron; and | It would have been obvious to a person having ordinary skill in the art at the time of the invention to implant Fujino’s silicon surfaces with boron as described in Saito (<i>see, e.g.</i> , TSMC1006 at 2:40-59; 3:30-42) in order to dope Fujino’s surfaces with boron for the formation of a device in the surfaces. <i>See also, e.g.</i> , TSMC1003 at ¶ 54. |
| said second surface comprises a second silicon surface implanted | |

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| with boron. | |
| 8. A structure as recited in claim 1, wherein: | As set forth in GROUNDS 5 and 6(A), <i>supra</i> , Fujino alone or in combination with Saito teaches the limitations of Claim 1. |
| said first surface comprises a first silicon surface implanted with arsenic; and | It would have been obvious to a person having ordinary skill in the art at the time of the invention to implant Fujino's silicon surfaces with arsenic as described by Saito (<i>see, e.g.</i> , TSMC1006 at 2:40-59; 3:30-42) in order to dope Fujino's surfaces with arsenic for the formation of a device in the surfaces. <i>See, also, e.g.</i> , TSMC1003 at ¶ 54. |
| said second surface comprises a second silicon surface implanted with arsenic. | |
| 9. A structure as recited in claim 1, comprising: | As set forth in GROUNDS 5 and 6(A), <i>supra</i> , Fujino alone or in combination with Saito teaches the limitations of Claim 1. |
| at least one of boron-boron and Si covalent bonds formed between said first and second substrates. | <p>It would have been obvious to a person having ordinary skill in the art at the time of the invention to implant and/or expose Fujino's surfaces with boron as described by Saito (<i>see, e.g.</i>, TSMC1006 at 2:40-59; 3:30-42) in order to dope Fujino's surfaces for the formation of a device in the surfaces. <i>See, also, e.g.</i>, TSMC1003 at ¶ 54. With this plasma implant and/or exposure, Fujino's surfaces will have boron atoms. <i>See, e.g.</i>, TSMC1003 at ¶ 55.</p> <p>With Fujino's surfaces being exposed to a boron-containing plasma and having boron atoms thereon, Fujino's bonding process will undergo a same or similar process as described in the '133 Patent to achieve silicon covalent bonds and boron-boron bonds. Particularly, as in Fujino, the '133 Patent teaches that bonding boron treated silicon surfaces with boron atoms on the surfaces results in silicon covalent bonds and boron-boron bonds across the interface, even more at temperatures of 350-400°C. <i>See, e.g.</i>, TSMC1001 at 7:66-8:21. Accordingly, Fujino in combination with Saito will result in silicon</p> |

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| | covalent bonds and boron-boron bonds. <i>See, also, e.g.</i> , TSMC1003 at ¶ 55. Additionally, in proceedings before the Office, where a reason to believe that a claimed limitation may be inherent in the prior art is shown, as is here, the burden shifts to the Patent Owner to provide evidence to the contrary. |
| 11. A structure as recited in claim 1, wherein said first and second layers each comprise a few monolayers of boron. | As set forth in GROUNDS 5 and 6(A), <i>supra</i> , Fujino alone or in combination with Saito teaches the limitations of Claim 1. One skilled in the art would recognize that the energy and dose of B ₂ H ₆ implants as described in Saito would lead to the formation of a few monolayers of boron in the surface of the substrates. <i>See, e.g.</i> , TSMC1003 at ¶ 56. It would have been obvious to a person having ordinary skill in the art at the time of the invention to implant Fujino's surfaces with boron as described in Saito (<i>see, e.g.</i> , TSMC1006 at 2:40-59; 3:30-42), which would result in the formation of a few monolayers of boron in the layers, in order to dope Fujino's surfaces with boron for the formation of a device in the surfaces. <i>See also, e.g.</i> , TSMC1003 at ¶¶ 54, 56. |
| 12. A structure as recited in claim 1, wherein: | As set forth in GROUNDS 5 and 6(A), <i>supra</i> , Fujino alone or in combination with Saito teaches the limitations of Claim 1. |
| said first surface comprises an amorphous boron-containing layer; and | It would have been obvious to a person having ordinary skill in the art at the time of the invention to implant Fujino's surfaces with boron as described in Saito (<i>see, e.g.</i> , TSMC1006 at 2:40-59; 3:30-42) to form the surfaces to comprise an amorphous boron-containing layer in order to dope Fujino's surfaces with boron for the formation of a device in the surfaces. <i>See also, e.g.</i> , TSMC1003 at ¶ 54. |
| said second surface comprises an amorphous boron-containing layer. | |
| 13. A structure as recited in claim 1, wherein: | As set forth in GROUNDS 5 and 6(A), <i>supra</i> , Fujino alone or in combination with Saito teaches the limitations of Claim 1. |
| said first surface comprises a surface | It would have been obvious to a person having ordinary skill in the art at the time of the invention to |

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| <p>exposed to a boron-containing plasma; and</p> | <p>expose Fujino's silicon surfaces of the wafers to a plasma containing ions of silicon while</p> |
| <p>said second surface comprises a surface exposed to a boron-containing plasma.</p> | <p>simultaneously including ions of boron as taught by Saito (<i>see, e.g.</i>, TSMC1006 at 2:40-59; 3:30-42) in order to dope Fujino's surfaces with boron for the formation of a device in the surfaces. <i>See also, e.g.</i>, TSMC1003 at ¶ 54.</p> |
| <p>14. A structure as recited in claim 1, wherein:</p> | <p>As set forth in GROUNDS 5 and 6(A), <i>supra</i>, Fujino alone or in combination with Saito teaches the limitations of Claim 1.</p> |
| <p>said first surface comprises a first surface exposed to an inert gas plasma; and</p> | <p>Saito further describes that argon in a plasma may be used as a carrier gas for the ion implantation. <i>See, e.g.</i>, TSMC1006 at 4:26-27. A plasma containing silicon with a carrier gas such as argon may be formed in Saito's plasma chamber, which may be used to form Saito's amorphous regions. <i>See, e.g.</i>, TSMC1006 at 4:22-32; FIG. 1. It would have been obvious to a person having ordinary skill in the art at the time of the invention to use a plasma, as taught by Saito, that contains silicon for an implantation, as taught by Fujino, and an inert gas such as argon for a carrier, as taught by Saito, in order to form Fujino's amorphous surfaces. <i>See, e.g.</i>, TSMC1003 at ¶¶ 35, 57. Using argon as a carrier gas to implant silicon is a simple substitution of one known technique for another known technique to obtain the predictable result of amorphizing a substrate.</p> |
| <p>said second surface comprises a second surface exposed to an inert gas plasma.</p> | |
| <p>58. A structure as recited in claim 53, wherein:</p> | <p>As set forth in GROUNDS 5 and 6(A), <i>supra</i>, Fujino alone or in combination with Saito teaches the limitations of Claim 53.</p> |
| <p>said first surface comprises a surface exposed to a boron-containing plasma; and</p> | <p>It would have been obvious to a person having ordinary skill in the art at the time of the invention to expose Fujino's surfaces to a plasma containing ions of silicon while simultaneously including ions of boron as taught by Saito (<i>see, e.g.</i>, TSMC1006 at 2:40-59; 3:30-42) in order to dope Fujino's surfaces with boron for the formation of a device in the</p> |
| <p>said second surface comprises a surface exposed to a boron-</p> | |

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| containing plasma. | surfaces. <i>See also, e.g.</i> , TSMC1003 at ¶ 54. |
| 59. A structure as recited in claim 53, wherein: | As set forth in GROUNDS 5 and 6(A), <i>supra</i> , Fujino alone or in combination with Saito teaches the limitations of Claim 53. |
| said first surface comprises a surface implanted with one of boron and arsenic; and | It would have been obvious to a person having ordinary skill in the art at the time of the invention to implant Fujino's surfaces using a plasma containing ions of silicon while simultaneously including ions of one of boron and arsenic as taught by Saito (<i>see, e.g.</i> , TSMC1006 at 2:40-59; 3:30-42) in order to dope Fujino's surfaces with one of boron and arsenic for the formation of a device in the surfaces. <i>See also, e.g.</i> , TSMC1003 at ¶ 54. |
| said second surface comprises a surface implanted with one of boron and arsenic. | |
| 60. A structure as recited in claim 59, comprising: | As set forth in GROUNDS 5, 6(B), and 6(C), <i>supra</i> , Fujino alone or in combination with Saito teaches the limitations of Claim 59. |
| boron-boron covalent bonds formed between said first and second substrates. | <p>It would have been obvious to a person having ordinary skill in the art at the time of the invention to implant and/or expose Fujino's surfaces with boron as described by Saito (<i>see, e.g.</i>, TSMC1006 at 2:40-59; 3:30-42) in order to dope Fujino's surfaces for the formation of a device in the surfaces. <i>See, also, e.g.</i>, TSMC1003 at ¶ 54. With this plasma implant and/or exposure, Fujino's surfaces will have boron atoms. <i>See, e.g., id.</i> at ¶ 55.</p> <p>With Fujino's surfaces being exposed to a boron-containing plasma and having boron atoms thereon, Fujino's bonding process will undergo a same or similar process as described in the '133 Patent to achieve boron-boron covalent bonds. Particularly, as in Fujino, the '133 Patent teaches that bonding boron treated silicon surfaces with boron atoms on the surfaces results in boron-boron covalent bonds across the interface, even more at temperatures of 350-400°C. <i>See, e.g.</i>, TSMC1001 at 7:66-8:21. Accordingly, Fujino in combination with Saito will</p> |

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| | result in boron-boron covalent bonds. <i>See, also, e.g.</i> , TSMC1003 at ¶ 55. Additionally, in proceedings before the Office, where a reason to believe that a claimed limitation may be inherent in the prior art is shown, as is here, the burden shifts to the Patent Owner to provide evidence to the contrary. |
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Ground 7: Claims 1-13, 53-56, 58, and 59 are rendered obvious over Fujino in view of Tian.

A. Claims 1 and 53: As set forth in GROUND 5, *supra*, Fujino anticipates or renders obvious Claims 1 and 53. To the extent that Fujino may not teach nearly-amorphized layers or substrates “containing one of boron and arsenic,” as recited in Claims 1 and 53, respectively, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the ion implantation, as taught by Fujino, to include boron or arsenic in the implantation, as taught or suggested by Tian (*see, e.g.*, TSMC1008 at Abstract, 1230), such that the amorphous layers contain one of boron and arsenic, to dope Fujino’s surfaces with one of boron and arsenic for the formation of a device. *See also, e.g.*, TSMC1003 at ¶ 58.

B. Claims 2-7, 9, 10, 12, 13, 54-56, 58, and 59: As set forth in GROUND 7(A), *supra*, Fujino in combination with Tian teaches the limitations of Claims 1 and 53. Further, as set forth in GROUND 5, *supra*, Fujino teaches the limitations of claims 2-7, 9, 10, 12, 13, 54-56, 58, and 59, and hence, these claims are obvious over Fujino in view of Tian. To the extent that Fujino alone does not teach certain

limitations of some of these dependent claims, further support is provided *infra* such that those claims are rendered obvious over Fujino and Tian.

C. Claims 7, 8, 11, 12, and 59:

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| 7. A structure as recited in claim 1, wherein: | As set forth in GROUNDS 5 and 7(A), <i>supra</i> , Fujino alone or in combination with Tian teaches the limitations of Claim 1. |
| said first surface comprises a first silicon surface implanted with boron; and | It would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the ion implantation, as taught by Fujino, to include the boron implantation, as taught or suggested by Tian (<i>see, e.g.</i> , TSMC1008 at Abstract, 1230), to dope Fujino’s surfaces with boron for the formation of a device in the surfaces. <i>See also, e.g.</i> , TSMC1003 at ¶ 58. |
| said second surface comprises a second silicon surface implanted with boron. | |
| 8. A structure as recited in claim 1, wherein: | As set forth in GROUNDS 5 and 7(A), <i>supra</i> , Fujino alone or in combination with Tian teaches the limitations of Claim 1. |
| said first surface comprises a first silicon surface implanted with arsenic; and | It would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the ion implantation, as taught by Fujino, to include the arsenic implantation, as taught or suggested by Tian (<i>see, e.g.</i> , TSMC1008 at Abstract, 1230), to dope Fujino’s surfaces with arsenic for the formation of a device in the surfaces. <i>See also, e.g.</i> , TSMC1003 at ¶ 58. |
| said second surface comprises a second silicon surface implanted with arsenic. | |
| 11. A structure as recited in claim 1, wherein said first and second layers each comprise a few monolayers of boron. | As set forth in GROUNDS 5 and 7(A), <i>supra</i> , Fujino alone or in combination with Tian teaches the limitations of Claim 1. One of ordinary skill in the art would know that by controlling the dose and energy of a boron species in an ion implantation, a region having a thickness of a few monolayers at or near the surface of the wafer would be boron rich. <i>See, e.g.</i> , TSMC1003 at ¶ 59. It would have been obvious to a |

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| | <p>person having ordinary skill in the art at the time of the invention to modify the ion implantation, as taught by Fujino, to include the boron implantation, as taught or suggested by Tian (<i>see, e.g.</i>, TSMC1008 at Abstract, 1230), which would result in the formation of a few monolayers of boron in the layers, to dope Fujino’s surfaces boron for the formation of a device in the surfaces. <i>See also, e.g.</i>, TSMC1003 at ¶ 58.</p> |
| <p>12. A structure as recited in claim 1, wherein:</p> | <p>As set forth in GROUNDS 5 and 7(A), <i>supra</i>, Fujino alone or in combination with Tian teaches the limitations of Claim 1.</p> |
| <p>said first surface comprises an amorphous boron-containing layer; and</p> | <p>It would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the ion implantation, as taught by Fujino, to include the boron implantation, as taught or suggested by Tian (<i>see, e.g.</i>, TSMC1008 at Abstract, 1230), such that Fujino’s surfaces comprise an amorphous boron-containing layer, to dope Fujino’s surfaces with boron for the formation of a device in the surfaces. <i>See also, e.g.</i>, TSMC1003 at ¶ 58.</p> |
| <p>said second surface comprises an amorphous boron-containing layer.</p> | |
| <p>59. A structure as recited in claim 53, wherein:</p> | <p>As set forth in GROUNDS 5 and 7(A), <i>supra</i>, Fujino alone or in combination with Tian teaches the limitations of Claim 53.</p> |
| <p>said first surface comprises a surface implanted with one of boron and arsenic; and</p> | <p>It would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the ion implantation, as taught by Fujino, to include boron or arsenic in the implantation, as taught or suggested by Tian (<i>see, e.g.</i>, TSMC1008 at Abstract, 1230), to dope Fujino’s surfaces with one of boron and arsenic for the formation of a device. <i>See also, e.g.</i>, TSMC1003 at ¶ 58.</p> |
| <p>said second surface comprises a surface implanted with one of boron and arsenic.</p> | |

Ground 8: Claims 1-14, 53-56, and 58-60 are rendered obvious over Fujino in view of Tian, and in further view of Saito.

A. Claims 1 and 53: As set forth in GROUNDS 5 AND 7(A), *supra*, Fujino

anticipates or renders obvious or Fujino in combination with Tian renders obvious independent Claims 1 and 53. To the extent that Fujino alone or in combination with Tian may not teach nearly-amorphized layers or substrates “containing one of boron and arsenic,” as recited in Claims 1 and 53, respectively, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the implantation of silicon ions and boron or arsenic ions as described in Fujino and/or Tian to be a plasma ion implantation containing silicon ions and boron or arsenic ions as described in Saito (*see, e.g.*, TSMC1006 at 2:40-59; 3:30-42) in order to dope one of boron and arsenic into surfaces for the formation of a device in the surfaces. *See also, e.g.*, TSMC1003 at ¶ 60.

B. Claims 2-13, 54-56, 58, and 59: As set forth in GROUND 8(A), *supra*, Fujino in combination with Tian and Saito teaches the limitations of Claims 1 and 53. Further, as set forth in GROUND 5 and 7, *supra*, Fujino alone or in combination with Tian teaches the limitations of claims 2-13, 54-56, 58, and 59, and hence, these claims are obvious over Fujino in view of Tian and Saito. To the extent that Fujino alone does not teach certain limitations of some of these dependent claims, further support is provided *infra* such that those claims are rendered obvious over Fujino, Tian, and Saito.

C. Claims 6, 9, 13, 14, 58, and 60:

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| 6. A structure as recited | As set forth in GROUNDS 5 and 8(A), <i>supra</i> , Fujino |
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| <p>in claim 1, wherein:</p> | <p>alone or in combination with Tian and Saito teaches the limitations of Claim 1.</p> |
| <p>said first surface comprises a first silicon surface exposed to a boron-containing plasma; and</p> | <p>It would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the implantation of silicon ions and boron ions as described in Fujino and/or Tian to use a plasma ion implantation containing silicon ions and boron ions as described in Saito (<i>see, e.g.</i>, TSMC1006 at 2:40-59; 3:30-42) in order to dope boron into surfaces for the formation of a device in the surfaces. <i>See also, e.g.</i>, TSMC1003 at ¶ 60.</p> |
| <p>said second surface comprises a second silicon surface exposed to a boron-containing plasma.</p> | |
| <p>9. A structure as recited in claim 1, comprising:</p> | <p>As set forth in GROUNDS 5 and 8(A), <i>supra</i>, Fujino alone or in combination with Tian and Saito teaches the limitations of Claim 1.</p> |
| <p>at least one of boron-boron and Si covalent bonds formed between said first and second substrates.</p> | <p>It would have been obvious to a person having ordinary skill in the art at the time of the invention to implant and/or expose Fujino's surfaces with boron as described by Saito (<i>see, e.g.</i>, TSMC1006 at 2:40-59; 3:30-42) in order to dope Fujino's surfaces for the formation of a device in the surfaces. <i>See, also, e.g.</i>, TSMC1003 at ¶ 60. With this plasma implant and/or exposure, Fujino's surfaces will have boron atoms. <i>See, e.g., id.</i> at ¶ 61.</p> <p>With Fujino's surfaces being exposed to a boron-containing plasma and having boron atoms thereon, Fujino's bonding process will undergo a same or similar process as described in the '133 Patent to achieve silicon covalent bonds and boron-boron bonds. Particularly, as in Fujino, the '133 Patent teaches that bonding boron treated silicon surfaces with boron atoms on the surfaces results in silicon covalent bonds and boron-boron bonds across the interface, even more at temperatures of 350-400°C. <i>See, e.g.</i>, TSMC1001 at 7:66-8:21. Accordingly, Fujino and Tian in combination with Saito will result</p> |

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| | <p>in silicon covalent bonds and boron-boron bonds. <i>See, also, e.g.</i>, TSMC1003 at ¶ 61. Additionally, in proceedings before the Office, where a reason to believe that a claimed limitation may be inherent in the prior art is shown, as is here, the burden shifts to the Patent Owner to provide evidence to the contrary.</p> |
| <p>13. A structure as recited in claim 1, wherein:</p> | <p>As set forth in GROUNDS 5 and 8(A), <i>supra</i>, Fujino alone or in combination with Tian and Saito teaches the limitations of Claim 1.</p> |
| <p>said first surface comprises a surface exposed to a boron-containing plasma; and</p> | <p>It would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the implantation of silicon ions and boron ions as described in Fujino and/or Tian to use a plasma ion implantation containing silicon ions and boron ions as described in Saito (<i>see, e.g.</i>, TSMC1006 at 2:40-59; 3:30-42) in order to dope boron into surfaces for the formation of a device in the surfaces. <i>See also, e.g.</i>, TSMC1003 at ¶ 60.</p> |
| <p>said second surface comprises a surface exposed to a boron-containing plasma.</p> | |
| <p>14. A structure as recited in claim 1, wherein:</p> | <p>As set forth in GROUNDS 5 and 8(A), <i>supra</i>, Fujino alone or in combination with Tian and Saito teaches the limitations of Claim 1.</p> |
| <p>said first surface comprises a first surface exposed to an inert gas plasma; and</p> | <p>Saito further describes that argon in a plasma may be used as a carrier gas for the ion implantation. <i>See, e.g.</i>, TSMC1006 at 4:26-27. A plasma containing silicon with a carrier gas such as argon may be formed in Saito's plasma chamber, which may be used to form Saito's amorphous regions. <i>See, e.g.</i>, TSMC1006 at 4:22-32; FIG. 1. It would have been obvious to a person having ordinary skill in the art at the time of the invention to use a plasma, as taught by Saito, that contains silicon for an implantation, as taught by Fujino, and an inert gas such as argon for a carrier, as taught by Saito, in order to form amorphous surfaces. <i>See, e.g.</i>, TSMC1003 at ¶¶ 35, 62. Using argon as a carrier gas to implant silicon is a simple substitution of one known technique for another known technique to obtain the predictable</p> |
| <p>said second surface comprises a second surface exposed to an inert gas plasma.</p> | |

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| | result of amorphizing a substrate. |
| 58. A structure as recited in claim 53, wherein: | As set forth in GROUNDS 5 and 8(A), <i>supra</i> , Fujino alone or in combination with Tian and Saito teaches the limitations of Claim 53. |
| said first surface comprises a surface exposed to a boron-containing plasma; and | It would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the implantation of silicon ions and boron ions as described in Fujino and/or Tian to use a plasma ion implantation containing silicon ions and boron ions as described in Saito (<i>see, e.g.</i> , TSMC1006 at 2:40-59; 3:30-42) in order to dope boron into surfaces for the formation of a device in the surfaces. <i>See also, e.g.</i> , TSMC1003 at ¶ 60. |
| said second surface comprises a surface exposed to a boron-containing plasma. | |
| 60. A structure as recited in claim 59, comprising: | As set forth in GROUNDS 5, 7(B), 7(C), and 8(B), <i>supra</i> , Fujino alone or in combination with Tian and Saito teaches the limitations of Claim 59. |
| boron-boron covalent bonds formed between said first and second substrates. | <p>It would have been obvious to a person having ordinary skill in the art at the time of the invention to implant and/or expose Fujino's surfaces with boron as described by Saito (<i>see, e.g.</i>, TSMC1006 at 2:40-59; 3:30-42) in order to dope Fujino's surfaces for the formation of a device in the surfaces. <i>See, also, e.g.</i>, TSMC1003 at ¶ 60. With this plasma implant and/or exposure, Fujino's surfaces will have boron atoms. <i>See, e.g., id.</i> at ¶ 61.</p> <p>With Fujino's surfaces being exposed to a boron-containing plasma and having boron atoms thereon, Fujino's bonding process will undergo a same or similar process as described in the '133 Patent to achieve and boron-boron covalent bonds. Particularly, as in Fujino, the '133 Patent teaches that bonding boron treated silicon surfaces with boron atoms on the surfaces results in boron-boron covalent bonds across the interface, even more at temperatures of 350-400°C. <i>See, e.g.</i>, TSMC1001 at 7:66-8:21. Accordingly, Fujino in combination with Saito will</p> |

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| | <p>result in boron-boron covalent bonds. <i>See, also, e.g.</i>, TSMC1003 at ¶ 61. Additionally, in proceedings before the Office, where a reason to believe that a claimed limitation may be inherent in the prior art is shown, as is here, the burden shifts to the Patent Owner to provide evidence to the contrary.</p> |
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Ground 9: Claims 2, 5, 54, and 57 are obvious over Fujino alone or in view of Saito and/or Tian, and in further view of Cheung.

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| <p>2. A structure as recited in claim 1, comprising:</p> | <p>As set forth in GROUNDS 5, 6(A), 7(A), and 8(A), <i>supra</i>, Fujino alone or in combination with Saito and/or Tian teaches the limitations of Claim 1.</p> |
| <p>one of said first and second substrates of said bonded pair having a third surface, said third surface having a nearly-amorphized layer;</p> | <p>Fujino describes bonding the wafers having amorphized surface layers. <i>See, e.g.</i>, TSMC1007 at 1322. Fujino describes bonding wafers to form power devices such as power transistors, isolated vertical-DMOS circuits and control circuits on a single chip. <i>See, e.g., id.</i> at 1322. Cheung describes bonding together amorphous surfaces of a pair of substrates. <i>See, e.g.</i>, TSMC1005 at 8:26-29, 32-36. Cheung describes bonding wafers to form “three-dimensional packaging of integrated semiconductor devices.” <i>See, e.g., id.</i> at 1:19-21.</p> |
| <p>a third substrate having a fourth surface, a fourth nearly-amorphized layer formed in said fourth surface; and</p> | <p>It would have been obvious to a person having ordinary skill in the art at the time of the invention to: form an amorphized third surface for one of the first and second substrates of Fujino; form an amorphized fourth surface region of a third substrate; and bond the third surface to the fourth surface to form a three-dimensional package as described in Cheung. <i>See also, e.g.</i>, TSMC1003 at ¶ 63.</p> |
| <p>said third surface bonded to said fourth surface.</p> | <p>As set forth in GROUNDS 5, 6(A), 7(A), and 8(A), <i>supra</i>, Fujino alone or in combination with Saito and/or Tian teaches the limitations of Claim 1.</p> |
| <p>5. A structure as recited in claim 1, wherein:</p> | <p>Fujino describes bonding the wafers having amorphized</p> |
| <p>said first and</p> | <p>Fujino describes bonding the wafers having amorphized</p> |

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| <p>second substrates comprise respective first and second semiconductor devices.</p> | <p>surface layers. <i>See, e.g.</i>, TSMC1007 at 1322. Fujino describes bonding wafers to form power devices such as power transistors, isolated vertical-DMOS circuits and control circuits on a single chip. <i>See, e.g., id.</i> at 1322. Cheung describes bonding together amorphous surfaces of a pair of substrates. <i>See, e.g.</i>, TSMC1005 at 8:26-29, 32-36. Cheung discloses that the invention can be applied to “multi-layered integrated circuit devices, three-dimensional packaging of integrated semiconductor devices, photonic devices, piezoelectronic devices, microelectromechanical systems (“MEMS”), sensors, actuators, solar cells, flat panel displays (e.g., LCD, AMLCD), biological and biomedical devices, and the like.” <i>See, e.g., id.</i> at 1:17-24.</p> <p>It would have been obvious to a person of ordinary skill in the art at the time of the invention to apply the devices taught by Cheung to the bonded wafers taught by Fujino since Fujino and Cheung both teach applications relating to bonding amorphous layers.</p> |
| <p>54. A structure as recited in claim 53, comprising:</p> | <p>As set forth in GROUNDS 5, 6(A), 7(A), and 8(A), <i>supra</i>, Fujino alone or in combination with Saito and/or Tian teaches the limitations of Claim 53.</p> |
| <p>one of said first and second substrates of said bonded pair being amorphized only in said first surface and in a third surface of said first material;</p> | <p>Fujino describes bonding the wafers having amorphized surface layers. <i>See, e.g.</i>, TSMC1007 at 1322. Fujino describes bonding wafers to form power devices such as power transistors, isolated vertical-DMOS circuits and control circuits on a single chip. <i>See, e.g., id.</i> at 1322. Cheung describes bonding together amorphous surfaces of a pair of substrates. <i>See, e.g.</i>, TSMC1005 at 8:26-29, 32-36. Cheung describes bonding wafers to form “three-dimensional packaging of integrated semiconductor devices.” <i>See, e.g., id.</i> at 1:19-21.</p> |
| <p>a third substrate of substantially one third material amorphized only in a third surface of said third material;</p> | <p>It would have been obvious to a person having ordinary skill in the art at the time of the invention to: form an amorphized third surface for one of the first and second substrates of Fujino; form an amorphized fourth surface</p> |

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| and | region of a third substrate; and bond the third surface to the fourth surface to form a three-dimensional package as described in Cheung. <i>See also, e.g.</i> , TSMC1003 at ¶ 63. (Petitioner notes that the “said fourth surface” as recited in Claim 54 lacks a proper antecedent basis.) |
| said third surface bonded to said fourth surface. | |
| 57. A structure as recited in claim 53, wherein: | As set forth in GROUNDS 5, 6(A), 7(A), and 8(A), <i>supra</i> , Fujino alone or in combination with Saito and/or Tian teaches the limitations of Claim 53. |
| said first surface comprises a substantially planar surface of a first silicon layer formed on said first device; and | Tian teaches that the surfaces are substantially planar surfaces of a silicon layer. <i>See, e.g.</i> , TSMC1007 at 1322 (Fig. 1). Also, Cheung teaches that the surfaces of the amorphous silicon layers are a substantially planar. <i>See, e.g.</i> , TSMC1005 at 6:12-14. Further, Cheung teaches that the bonding process can be applied to “multi-layered integrated circuit devices, three-dimensional packaging of integrated semiconductor devices, photonic devices, piezoelectronic devices, microelectro-mechanical systems (‘MEMS’), sensors, actuators, solar cells, flat panel displays (e.g., LCD, AMLCD), biological and biomedical devices, and the like.” <i>See, e.g., id.</i> at 1:17-24. It would have been obvious to a person of ordinary skill in the art at the time of the invention to have made the amorphous layers formed on devices for the various applications as taught by Cheung. |
| said second surface comprises a substantially planar surface of a second silicon layer formed on said second device. | |

VII. CONCLUSION

Claims 1-14 and 53-60 of the '133 Patent are not patentable over the prior art references discussed herein. The prior art references and their combinations present non-cumulative technological teachings not considered during the '133 Patent prosecution history, which alone or in combination teach or suggest each of the elements recited in each of Claims 1-14 and 53-60 of the '133 Patent. For at least these reasons, Petitioner has shown a reasonable likelihood that at least one of Claims 1-14 and 53-60 is unpatentable, and *inter partes* review of U.S. Patent No. 6,563,133 B1 is respectfully requested.

Respectfully submitted,

2013-11-1
Date

/Steven H. Slater/
Steven H. Slater
Reg. No. 35,361

Slater & Matsil, L.L.P.
17950 Preston Rd.
Suite 1000
Dallas, TX 75252
972-732-1001
972-732-9218 (fax)

**CERTIFICATE OF SERVICE ON PATENT OWNER PURSUANT
TO 37 C.F.R. § 42.105(a)**

The undersigned hereby certifies that the foregoing Petition for *inter partes* review of U.S. Patent No. 6,563,133 to Tong and the associated Exhibits TSMC1001-TSMC1009 were served by deposit in their entirety by EXPRESS MAIL on the attorney of record for the '133 Patent contemporaneous with the filing of the foregoing Petition on November 1, 2013:

Oblon, Spivak, McClelland Maier & Neustadt, L.L.P.
1940 Duke Street
Alexandria, VA 22314

Respectfully submitted,
SLATER & MATSIL, L.L.P.

2013-11-1
Date

/Steven H. Slater/
Steven H. Slater
Reg. No. 35,361

Slater & Matsil, L.L.P.
17950 Preston Rd.
Suite 1000
Dallas, TX 75252
972-732-1001
972-732-9218 (fax)