

FILE HISTORY

US 6,563,133

PATENT: 6,563,133

INVENTORS: Tong, Qin Yi

TITLE: Method of epitaxial-like wafer bonding at
low temperature and bonded structure

APPLICATION NO: US2000635272A


FILED: 09 AUG 2000

ISSUED: 13 MAY 2003

COMPILED: 03 OCT 2012

PATENT NUMBER

6563133



6563133

U.S. **UTILITY** Patent Application

O.I.P.E. <i>RAH 2</i>	PATENT DATE
SCANNED <i>PD²</i> Q.A. <i>CS</i>	MAY 13 2003

LOCATION NO 09/635272	CI	PRIOR 408	CLASS 201	SUBCLASS	ART UNIT 2825	EXAMINER DIAE
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Din-Yi Tong

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Method of epitaxial-like wafer bonding at low temperature and bonded structure

PTO-2040
12/99

ISSUING CLASSIFICATION											
ORIGINAL				CROSS REFERENCE(S)							
CLASS		SUBCLASS		CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)						
257		52		257	347'	618					
INTERNATIONAL CLASSIFICATION				438	455	974	482	485			
H	0	1	L	29/04							
H	0	1	L	21/30							

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<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg. <u>11</u>	Figs. Drwg. <u>28</u>	Print Fig. <u>2D</u>	Total Claims <u>60</u>	Print Claim for O.G. <u>1</u>
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	<u>José R. Díaz</u> (Assistant Examiner)			NOTICE OF ALLOWANCE MAILED <u>12-3-02</u>	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____ _____	<u>[Signature]</u> (Primary Examiner)			ISSUE FEE <u>225</u>	
				Amount Due <u>\$640.00</u>	
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	_____ (Legal Instruments Examiner)			ISSUE BATCH NUMBER _____	
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Form **PTO-436A**
(Rev. 6/99)

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TSMC1002
IPR of U.S. Pat. No. 6,563,133

METHOD OF EPITAXIAL-LIKE WAFER BONDING AT LOW TEMPERATURE AND BONDED STRUCTURE

Transaction History

Date	Transaction Description
08-09-2000	Initial Exam Team nn
09-01-2000	IFW Scan & PACR Auto Security Review
09-23-2000	Application Dispatched from OIPE
09-23-2000	Correspondence Address Change
10-05-2000	Case Docketed to Examiner in GAU
12-12-2000	Mail Restriction Requirement
12-12-2000	Restriction/Election Requirement
01-12-2001	Response to Election / Restriction Filed
01-16-2001	Information Disclosure Statement (IDS) Filed
01-16-2001	Information Disclosure Statement (IDS) Filed
01-19-2001	Information Disclosure Statement (IDS) Filed
01-19-2001	Information Disclosure Statement (IDS) Filed
01-23-2001	Date Forwarded to Examiner
01-26-2001	Information Disclosure Statement (IDS) Filed
01-26-2001	Information Disclosure Statement (IDS) Filed
02-13-2001	Case Docketed to Examiner in GAU
03-21-2001	Mail Non-Final Rejection
03-21-2001	Non-Final Rejection
06-21-2001	Response after Non-Final Action
06-27-2001	Date Forwarded to Examiner
09-14-2001	Final Rejection
09-17-2001	Mail Final Rejection (PTOL - 326)
12-07-2001	Amendment after Final Rejection
12-14-2001	Date Forwarded to Examiner
12-21-2001	Mail Advisory Action (PTOL - 303)
12-21-2001	Advisory Action (PTOL-303)
12-26-2001	Information Disclosure Statement (IDS) Filed
12-26-2001	Information Disclosure Statement (IDS) Filed
01-17-2002	Request for Continued Examination (RCE)
01-17-2002	Request for Extension of Time - Granted
01-17-2002	Workflow - Request for RCE - Begin
02-06-2002	Date Forwarded to Examiner
02-06-2002	Disposal for a RCE / CPA / R129
04-08-2002	Non-Final Rejection
04-10-2002	Mail Non-Final Rejection
09-10-2002	Response after Non-Final Action

09-10-2002	Request for Extension of Time - Granted
09-17-2002	Date Forwarded to Examiner
12-02-2002	Formal Drawings Required
12-02-2002	Notice of Allowance Data Verification Completed
12-02-2002	Case Docketed to Examiner in GAU
12-03-2002	Mail Notice of Allowance
12-03-2002	Mail Formal Drawings Required
01-13-2003	Dispatch to Publications
01-14-2003	Workflow - File Sent to Contractor
01-14-2003	Receipt into Pubs
02-19-2003	Issue Fee Payment Verified
02-19-2003	Workflow - Drawings Finished
02-19-2003	Workflow - Drawings Matched with File at Contractor
02-19-2003	Workflow - Drawings Received at Contractor
02-19-2003	Workflow - Drawings Sent to Contractor
02-19-2003	Issue Fee Payment Received
04-03-2003	Receipt into Pubs
04-04-2003	Application Is Considered Ready for Issue
04-08-2003	Receipt into Pubs
04-24-2003	Issue Notification Mailed
05-13-2003	Recordation of Patent Grant Mailed
05-13-2003	Patent Issue Date Used in PTA Calculation
12-17-2010	Statement Filed Indicating a Loss of Entitlement to Small Entity Status

PATENT APPLICATION



09635272



08/09/00

INITIALS ASD 8/23/00

CONTENTS

Date Received
(Incl. C. of M.)
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Date Received
(Incl. C. of M.)
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Date Mailed

1. Application 11 papers.		42.	
2. Restriction (30 days) 12/12/00		43.	
3. Election 1-12-01		44.	
4. IDS 1-19-01		45.	
5. IDS 1-26-01		46.	
3/1/01 6. Request (3 mos) 3/21/01 ^{ma}		47.	
7. IDS 1/16/01		48.	
8. Amdt A 6-21-01		49.	
9/14/01 9. Final 9/17/01 ^{ma}		50.	
10. Interview Summary 12/5/01		51.	
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13. IDS 12-26-01		54.	
14. Ex (1) 1-17-02		55.	
15. RCE 1-17-02		56.	
16. Request 4/10/02 ^{ma}		57.	
17. Eot (2 mos) 9/10/02		58.	
18. Amdt C 9/10/02		59.	
19. Allowance 12/03/02 ^{ma}		60.	
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POSITION	INITIALS	ID NO.	DATE
FEE DETERMINATION	<i>[Signature]</i>		05/17/02
O.I.P.E. CLASSIFIER	RSI		5/23/02
FORMALITY REVIEW	<i>[Signature]</i>	68608	9/23/2000
RESPONSE FORMALITY REVIEW			

INDEX OF CLAIMS

✓ Rejected N Non-elected
 = Allowed I Interference
 - (Through numeral) ... Canceled A Appeal
 + Restricted O Objected

Claim	Final	Original	Date
1	1	1	08/16/02
2	2	2	08/16/02
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150	150	150	08/16/02

If more than 150 claims or 10 actions
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SEARCHED

Class	Sub.	Date	Exmr.
438	455	3/13/01	P
Updated		9/10/01	P
438	456-459	9/10/01	P
Updated		4/8/02	P
438	455-459	4/2/02	P
↓	974		
↓	514		
↓	482		
438	485		
257	52		
	646		
↓	347		
↓	49		
257	629	12/2/02	P
257	618	12/2/02	P

INTERFERENCE SEARCHED

Class	Sub.	Date	Exmr.
438	455	12/2/02	P
↓	974		
↓	482		
438	485		
257	52		
↓	347	12/2/02	P
257	618	12/2/02	P

SEARCH NOTES (INCLUDING SEARCH STRATEGY)

	Date	Exmr.
Conferred w/ Sara Crane Text Search	3/13/01	P
1. East	3/13/01	P
a) 438/455 and amorph#6	3/14/01	P
b) "bond#4 adj substrates" and "amorph#4"		
Text Search		
1. East	9/10/01	P
Text Search		
East	4/8/02	P
Text Search		
East (amorphous or amorphized) and the classes/ subclasses disclosed in the "searched" box: 438/455-459, 974, 514 482, 485 257/52, 646, 347 49, 629, 618		



US006563133B1

(12) **United States Patent**
Tong

(10) **Patent No.: US 6,563,133 B1**
(45) **Date of Patent: May 13, 2003**

(54) **METHOD OF EPITAXIAL-LIKE WAFER BONDING AT LOW TEMPERATURE AND BONDED STRUCTURE**

(75) **Inventor: Qin-Yi Tong, Durham, NC (US)**

(73) **Assignee: Ziptronix, Inc., Research Triangle Park, NC (US)**

(*) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) **Appl. No.: 09/635,272**

(22) **Filed: Aug. 9, 2000**

(51) **Int. Cl.⁷ H01L 29/04; H01L 21/30**

(52) **U.S. Cl. 257/52; 257/347; 257/618; 438/455; 438/974; 438/482; 438/485**

(58) **Field of Search 438/455-459, 438/974, 514, 482, 485; 257/52, 646, 347, 49, 629, 618**

(56) **References Cited**

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6,143,628	A	*	11/2000	Sato et al.	438/455
6,153,445	A	*	11/2000	Yamazaki et al.	438/158
6,198,159	B1	*	3/2001	Hosoma et al.	257/643
6,246,068	B1		6/2001	Sato et al.	
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(List continued on next page.)

Primary Examiner—Eddie Lee

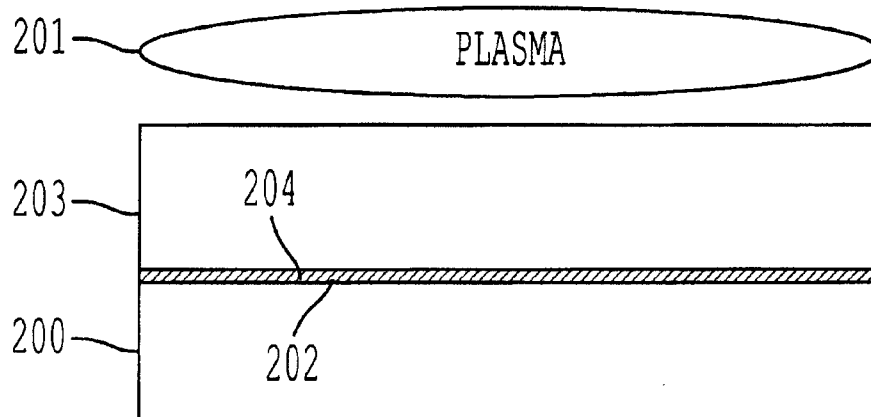
Assistant Examiner—José R. Díaz

(74) *Attorney, Agent, or Firm*—Oblon, Spivak, McClelland, Maier & Neustadt, P.C.

(57) **ABSTRACT**

A process for bonding oxide-free silicon substrate pairs and other substrates at low temperature. This process involves modifying the surface of the silicon wafers to create defect regions, for example by plasma-treating the surface to be bonded with a boron-containing plasmas such as a B₂H₆ plasma. The surface defect regions may also be created by ion implantation, preferably using boron. The surfaces may also be amorphized. The treated surfaces are placed together, thus forming an attached pair at room temperature in ambient air. The bonding energy reaches approximately 400 mJ/M² at room temperature, 900 mJ/M² at 150° C., and 1800 mJ/M² at 250° C. The bulk silicon fracture energy of 2500 mJ/m² was achieved after annealing at 350-400° C. The release of hydrogen from B-H complexes and the subsequent absorption of the hydrogen by the plasma induced modified layers on the bonding surfaces at low temperature is most likely responsible for the enhanced bonding energy.

60 Claims, 11 Drawing Sheets



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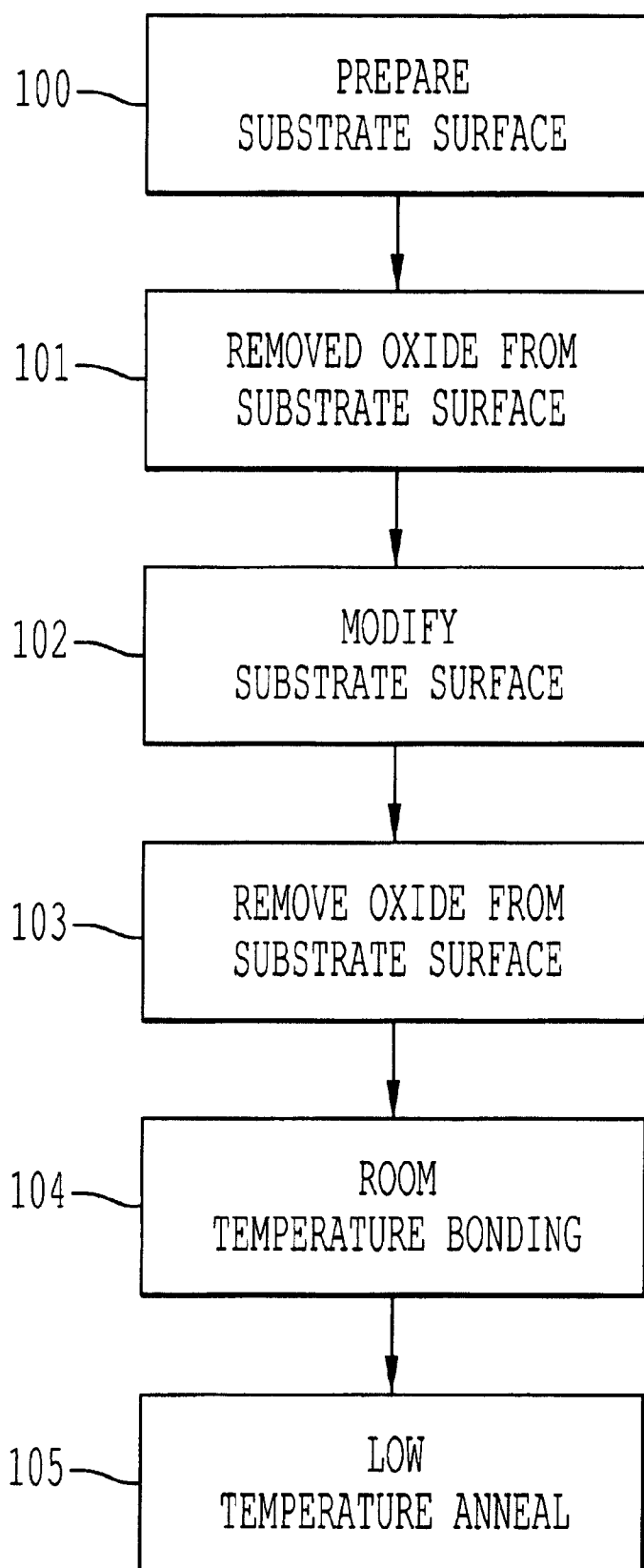
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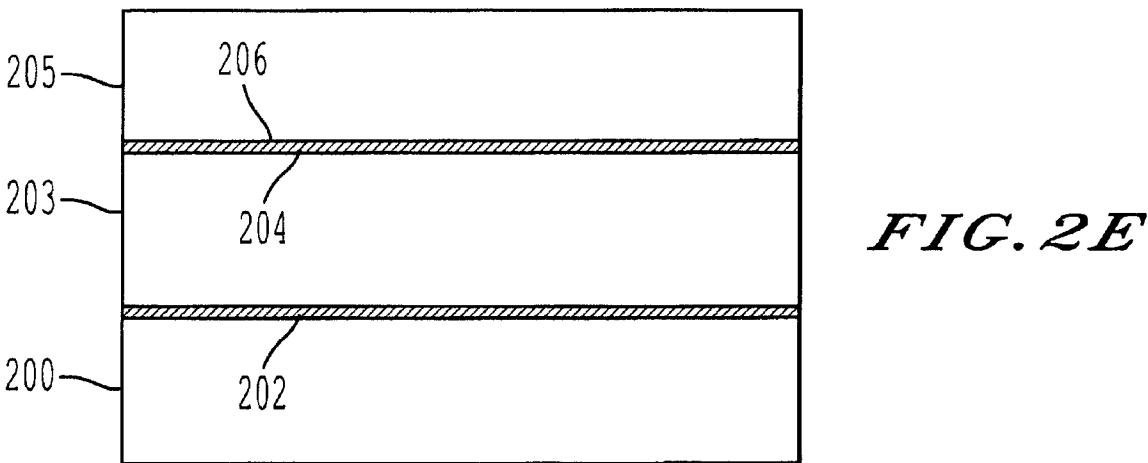
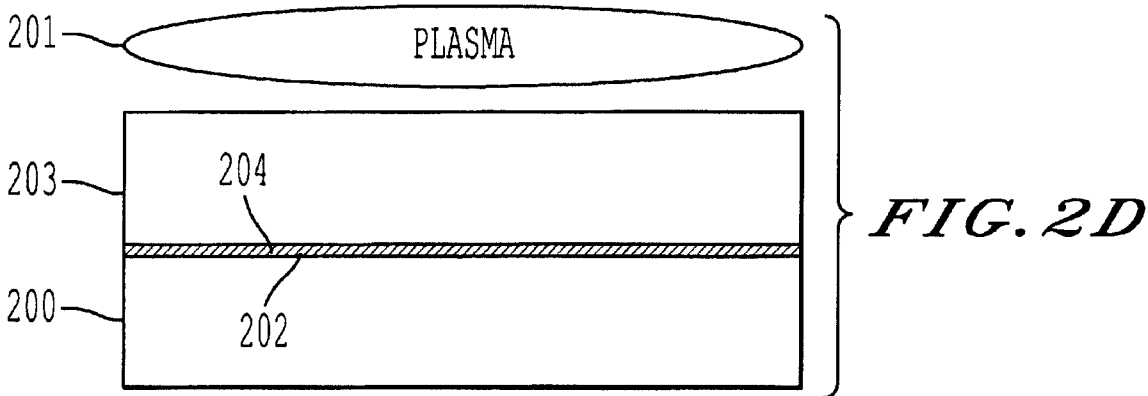
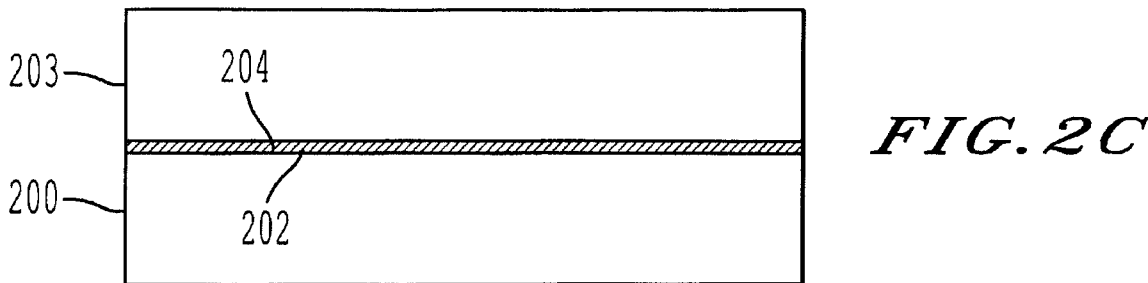
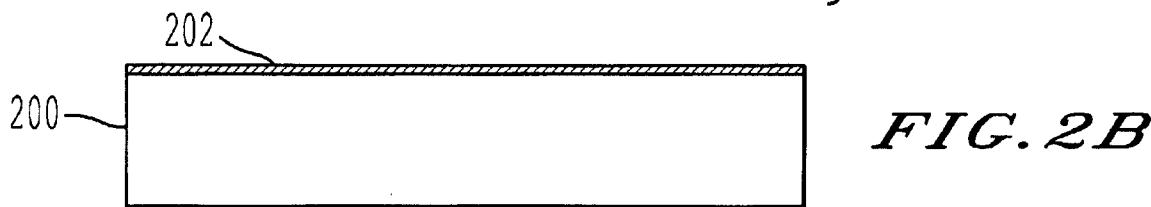
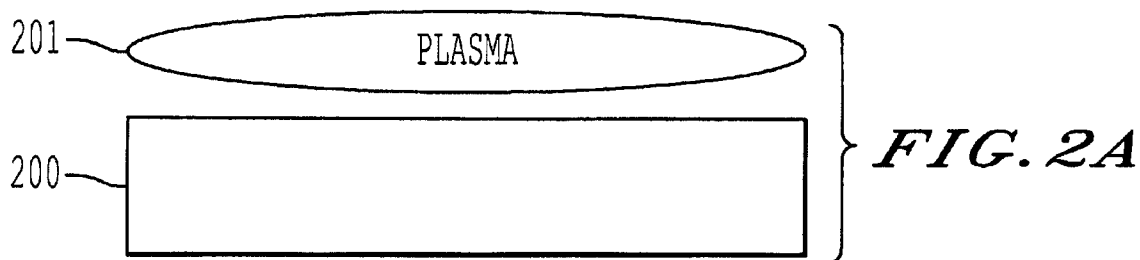
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*FIG. 1*



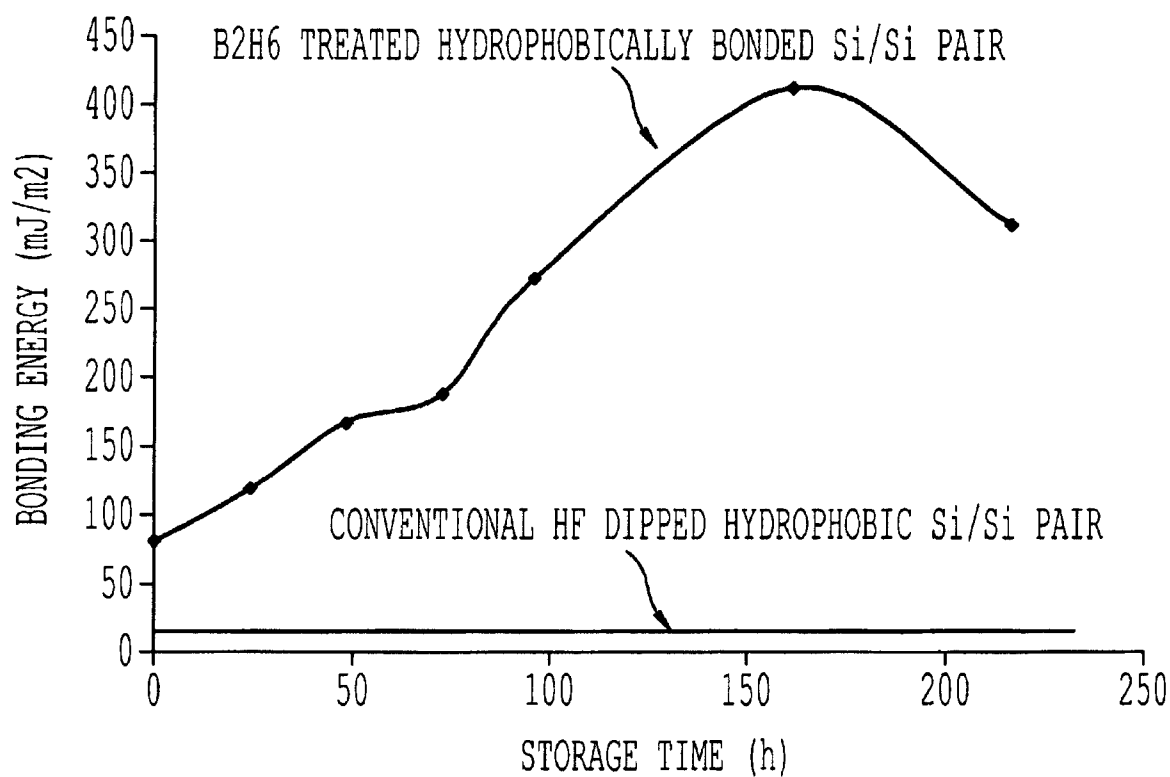


FIG. 3

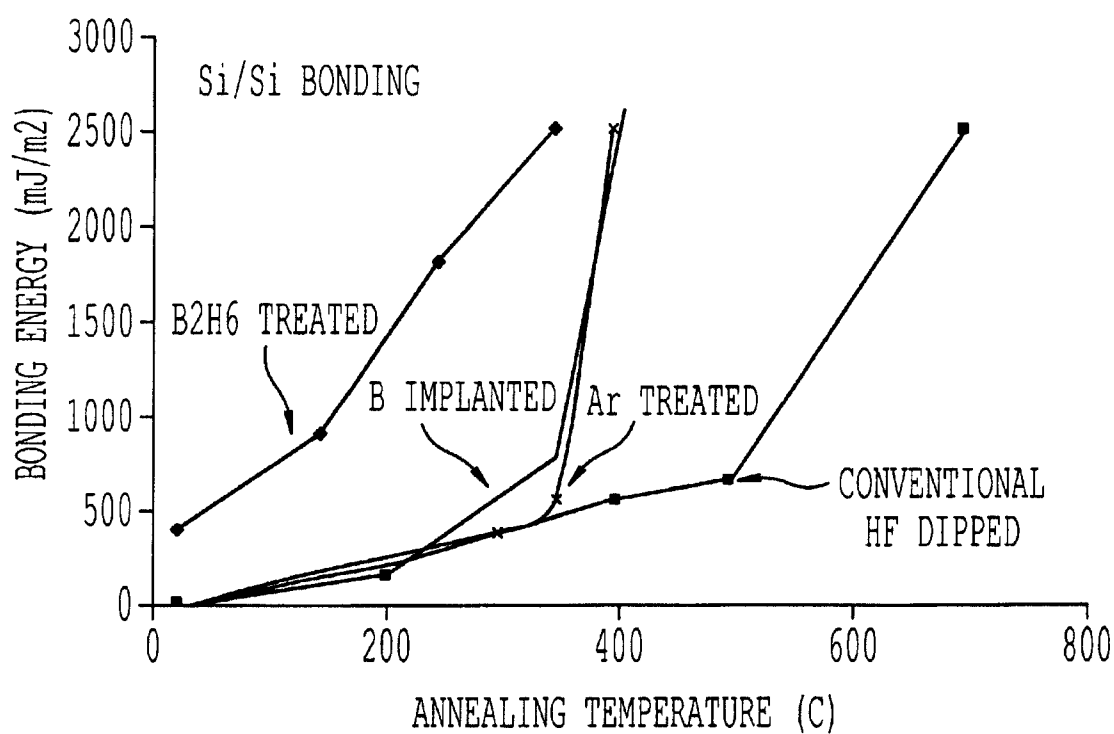


FIG. 4

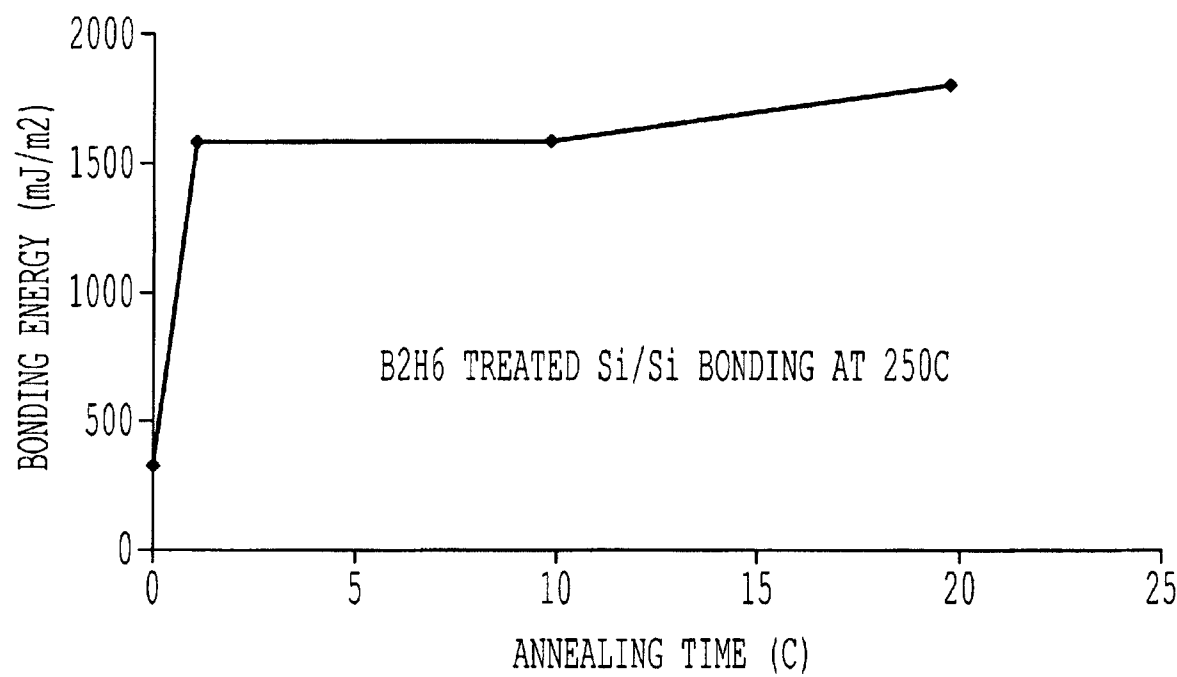


FIG. 5

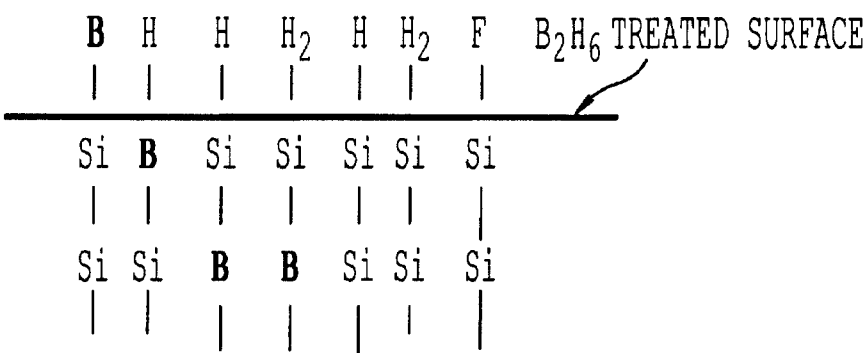
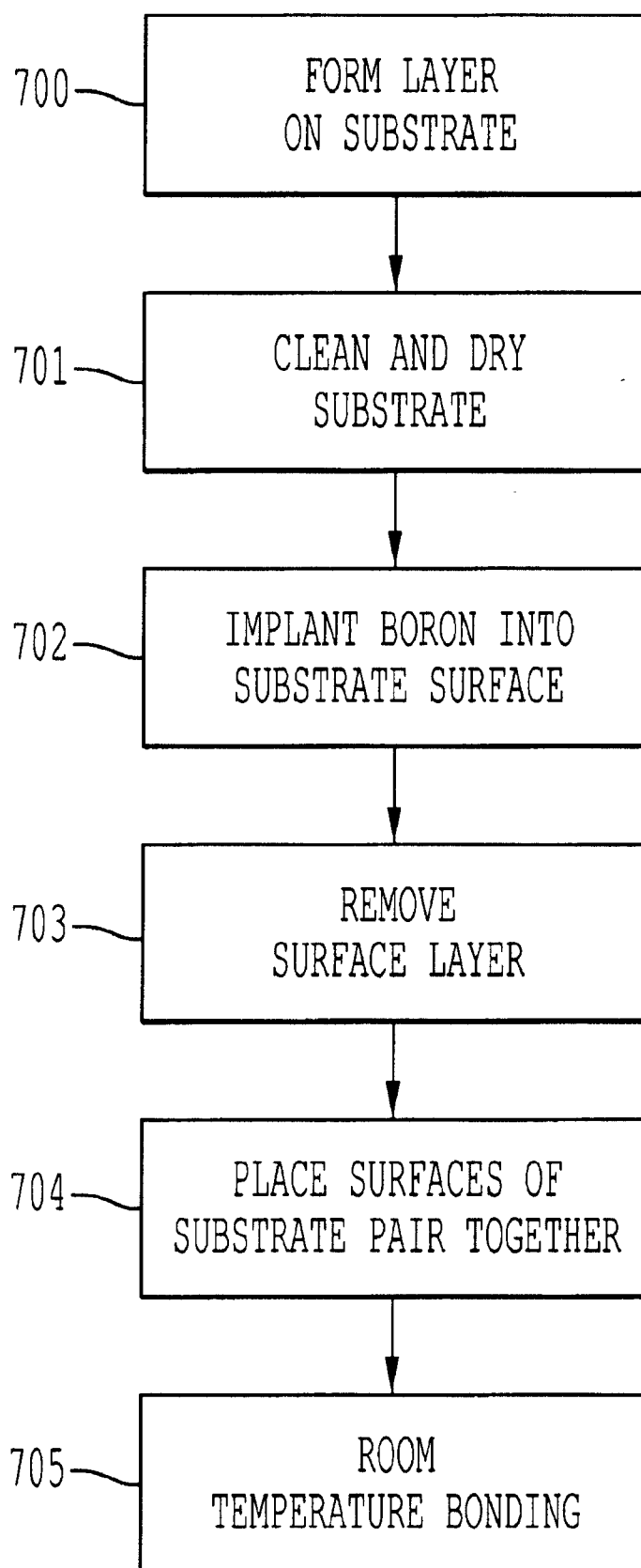


FIG. 6

*FIG. 7*

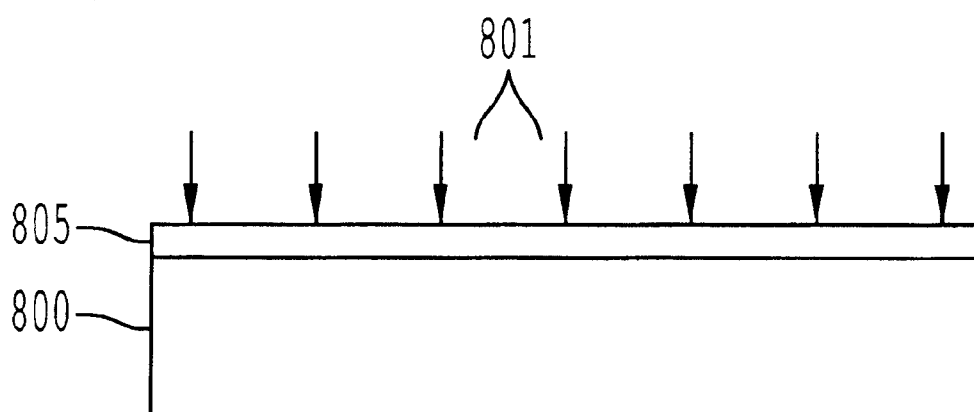


FIG. 8A

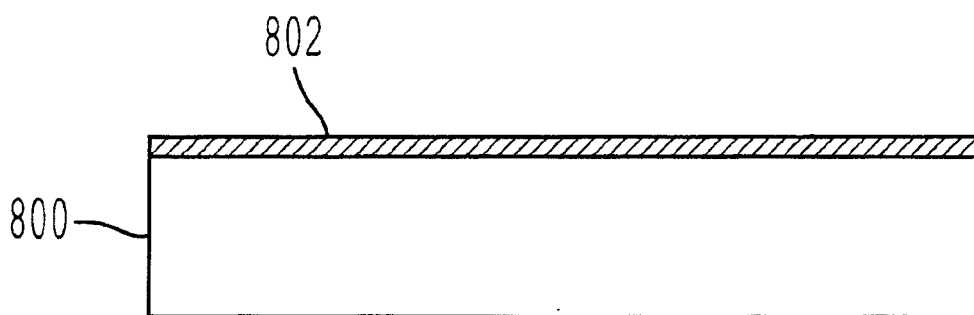


FIG. 8B

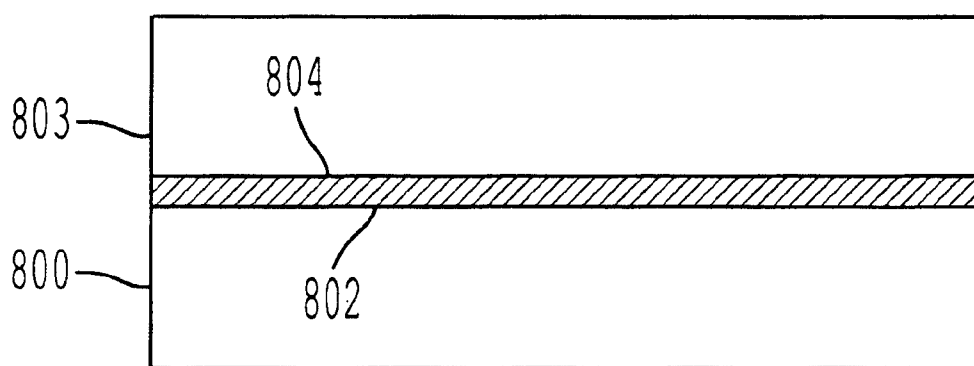


FIG. 8C

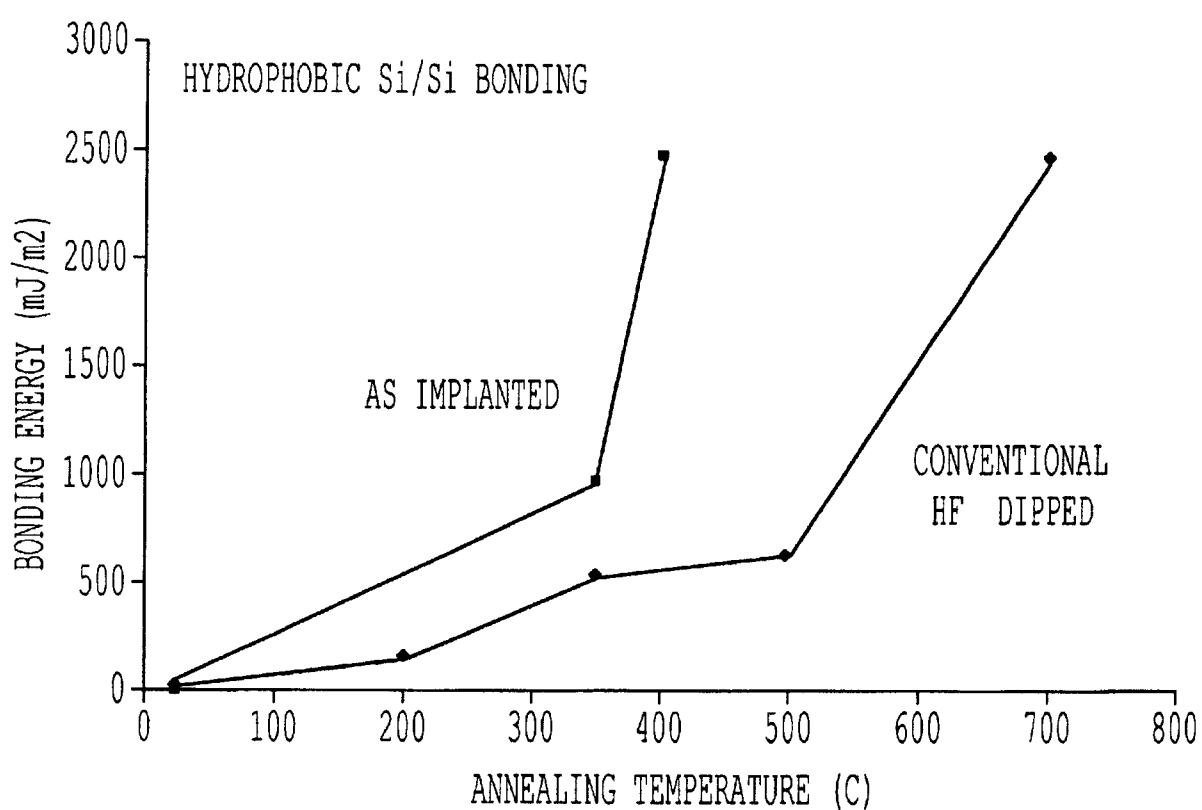


FIG. 9

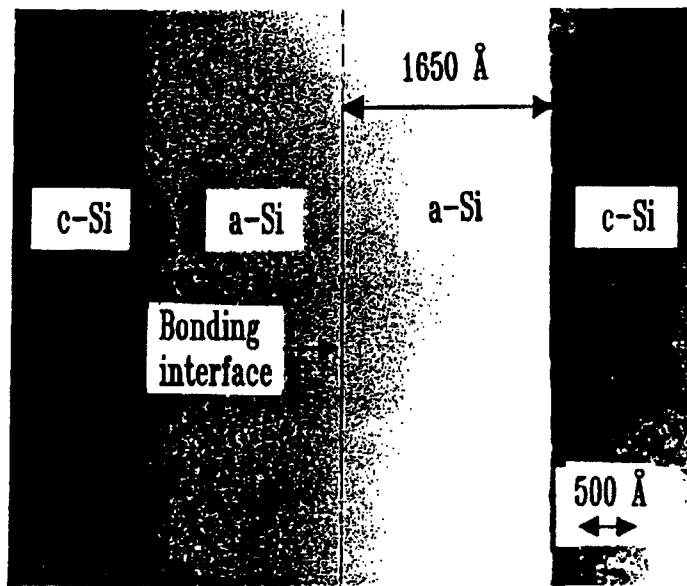


FIG. 10

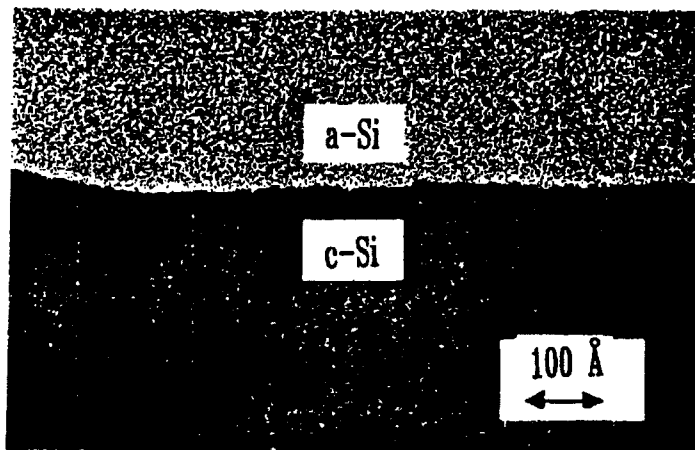


FIG. 11

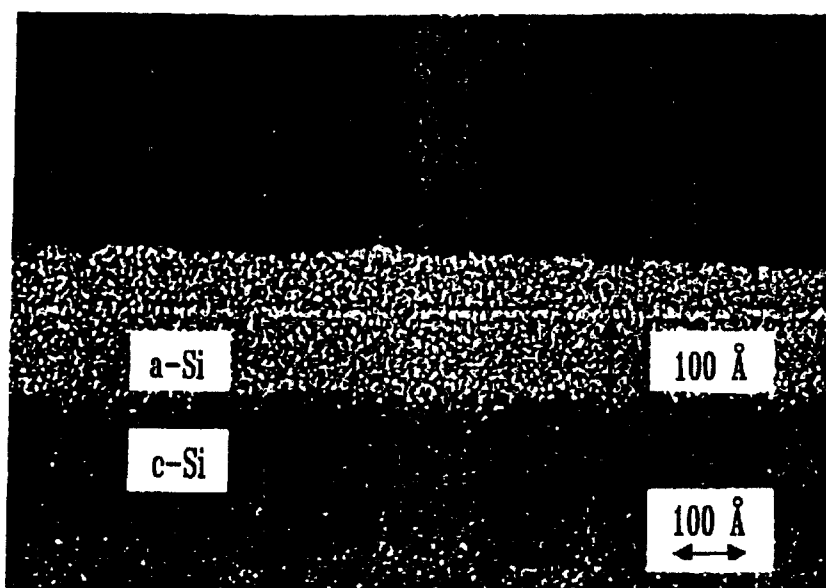


FIG. 12

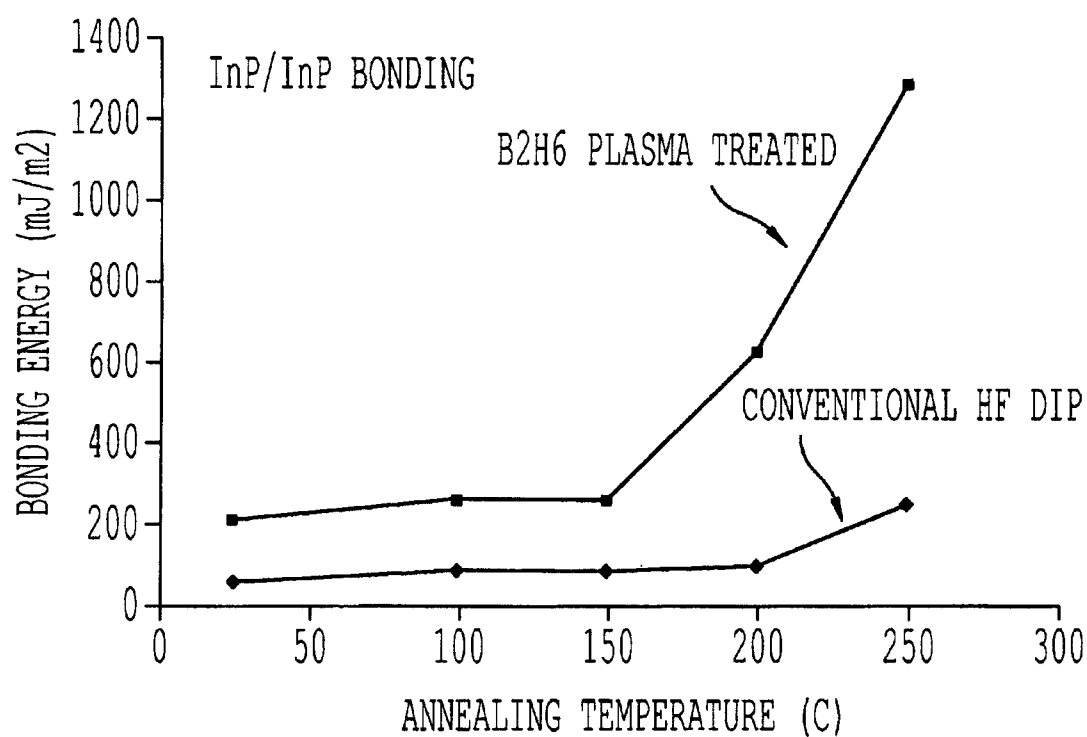


FIG. 13

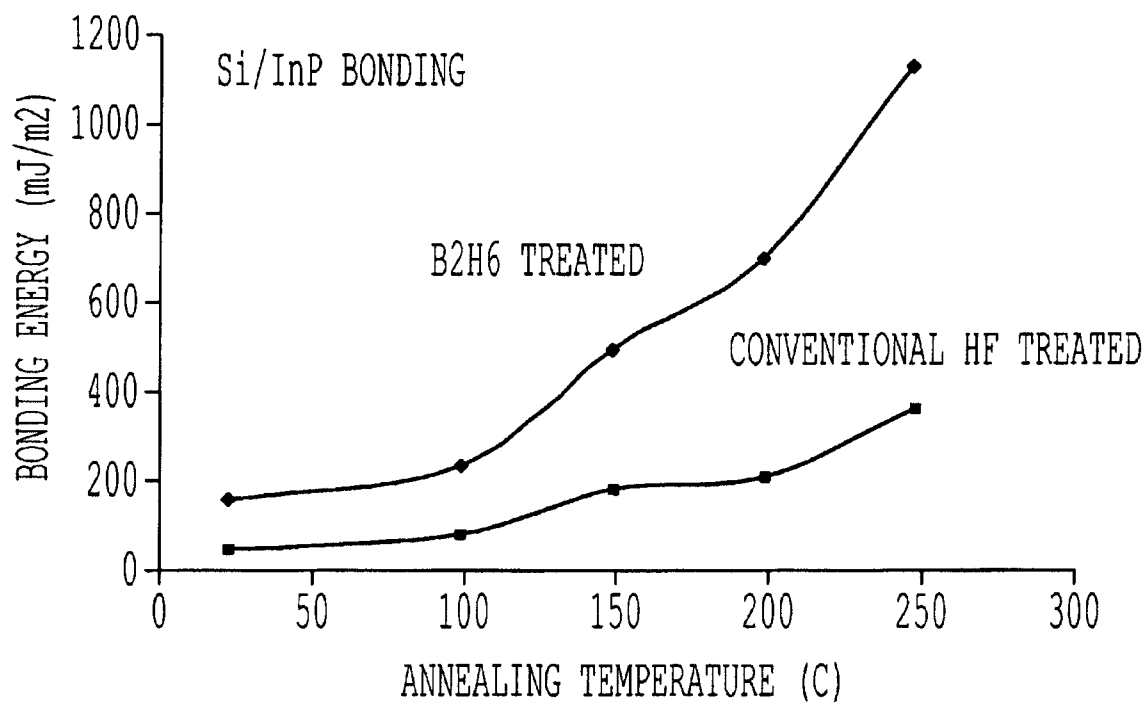


FIG. 14

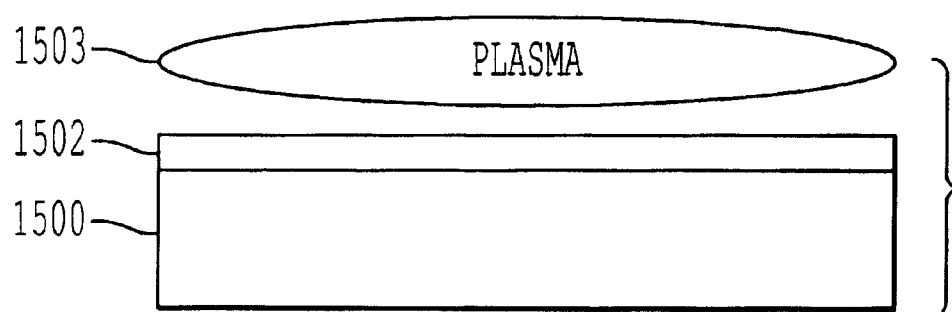


FIG. 15A

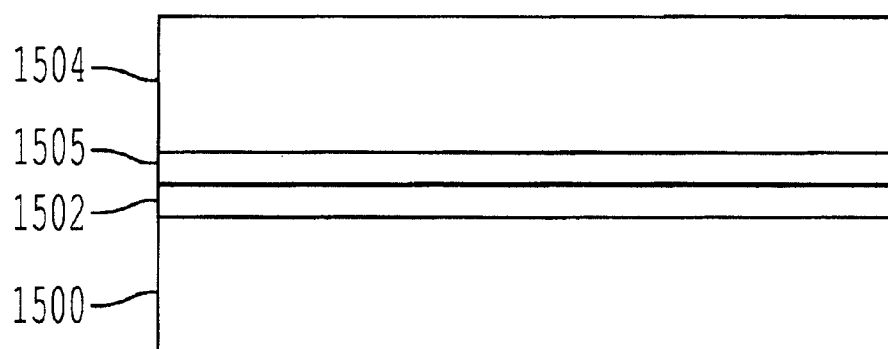


FIG. 15B

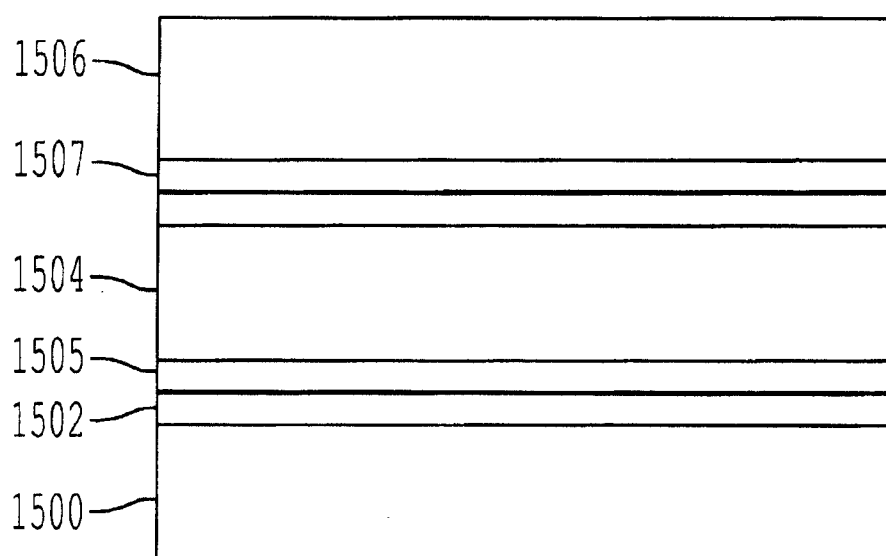
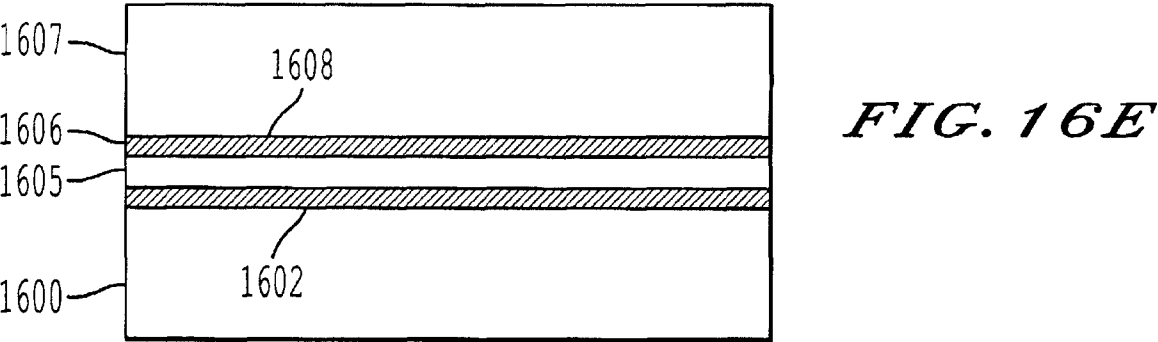
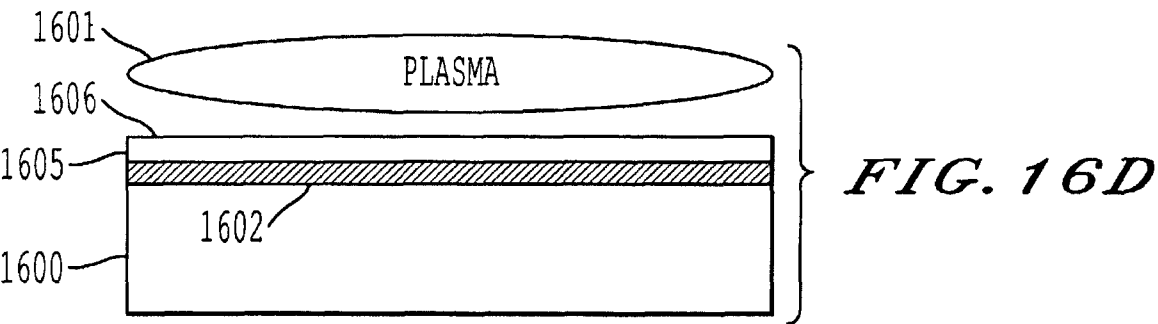
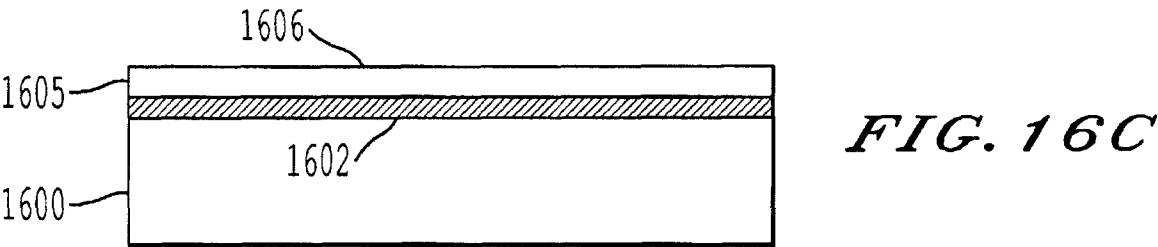
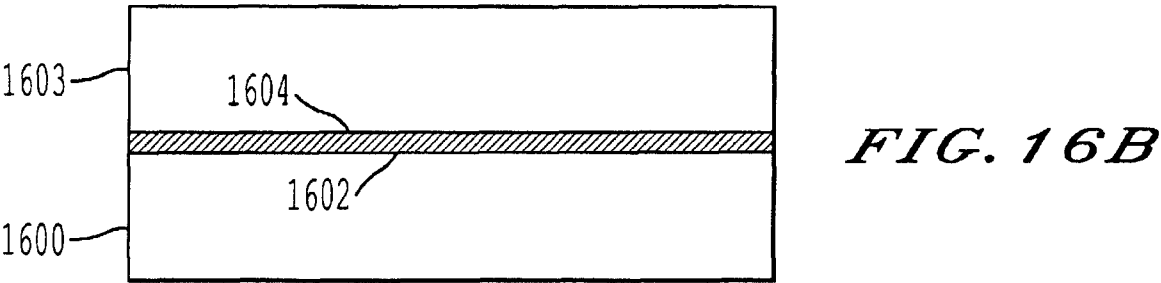
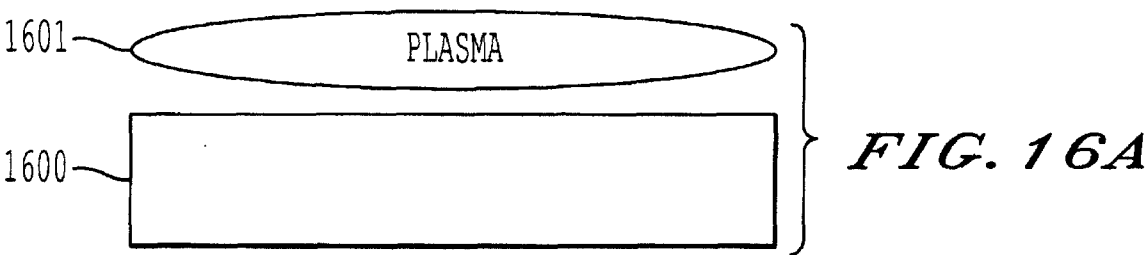


FIG. 15C



1

METHOD OF EPITAXIAL-LIKE WAFER BONDING AT LOW TEMPERATURE AND BONDED STRUCTURE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method of epitaxial-like bonding of wafer pairs at low temperature, and more particularly to a method of bonding in which the wafer surfaces are modified to create surface and subsurface defect areas, and possibly amorphized, by ion implantation or plasma, preferably by boron-containing ions or a plasma such as B_2H_6 .

2. Discussion of the Background

For many optoelectronic and electronic device applications, homo-epitaxial single crystalline layers consisting of same material with same crystalline orientation but different doping types or levels are necessary. For some device applications, active layers comprising single crystalline dissimilar materials are required. The active layers should be high crystallographic quality with interfaces that are thermally conductive and almost optical loss free. Conventional hetero-epitaxial growth techniques applied to these lattice mismatched active layers usually result in a large density of threading dislocations in the bulk of the layers. Bonding of single crystalline wafers of identical or dissimilar materials is an unique alternative approach to the epitaxial growth. Not only highly lattice-mismatched wafers can be bonded but also wafers with different crystalline orientations can be combined. Ideally, the mismatches of single crystalline bonding wafers are accommodated by dislocations (in lattice-mismatch case) or an amorphous layer (in orientation-mismatch case) localized at the bonding interface with no defects generated in the bulk area. This approach is termed epitaxial-like bonding. The epitaxial-like bonding can also be employed to prepare unique devices by integrating already processed device layers.

However, conventional epitaxial-like bonding is achieved by high temperature annealing. To bond wafers composed of thermally mismatched materials, severe and often damaging thermal stresses can be induced with high temperature annealing. Since thermal stresses can increase significantly with the size of dissimilar wafers, only small wafers currently can be epitaxially bonded at high temperatures. The high temperature annealing process can also produce unwanted changes to bonding materials and often prevents the bonding of processed device wafers. The bonding materials may decompose at high temperatures, even if the bonding wafers are thermally matched.

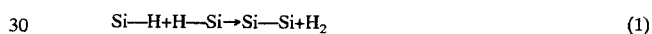
In order to epitaxially bond large wafers of dissimilar materials or processed wafers, an epitaxial-like bonding interface must be achieved at or near room temperature, or one wafer of the bonded pair must be thinned sufficiently before annealing to elevated temperatures. Although G öesele et al. in *Applied Physics Letters* 67, 3614 (1995) and Takagi et al. in *Applied Physics Letters* 74, 2387, 1999 reported room temperature epitaxial-like bonding of silicon wafers in ultrahigh vacuum, high temperature ($>600^\circ\text{C}$) pre-annealing in the former case or high external pressure ($>1\text{ MPa}$) in the latter case were required to achieve the bond that may introduce undesired effects to the bonding wafers.

Recently, M. Bruehl in *Electronics Letters* 31,1201 (1995) reported a promising generic thinning approach using a hydrogen-induced layer transfer method (so-called smart-cut method). In this approach, H atoms are implanted into a

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Si wafer to such concentration that a significant fraction of Si—Si bonds are broken creating a buried H-rich layer of micro-cracks susceptible to cleavage or fracture. By bonding the topmost oxide covered hydrophilic Si wafer surface to another substrate, a thin layer of the Si wafer can then be transferred by fracture of the H-rich region. However, this process requires that the bonding energy between the bonded wafers be higher than the fracture energy of the hydrogen-induced crack region at the layer transfer temperature. The layer transfer temperatures must be lower than the temperature beyond which hydrogen molecules in the material become mobile. For silicon, the temperature is about 500°C . (see Chu et al. in *Physics Review B*, 16, 3851 (1987)). The bonding energy of conventional HF dipped hydrophobic silicon wafer pairs is higher than the hydrogen-induced region only after annealing at temperatures higher than 600°C . Therefore, this process does not work for oxide-free hydrophobic silicon wafer bonding.

Typically, HF-dipped, hydrogen-terminated hydrophobic silicon wafers are used to realize epitaxial-like bonding after annealing at $>700^\circ\text{C}$. In order for bonded hydrophobic silicon wafer pairs to reach bulk fracture energy, Tong et al. in *Applied Physics Letters* 64, 625 (1994) reported that hydrogen (from HF-dip, mainly Si— H_2 and Si—H terminated hydrophobic silicon surfaces at the bonding interface) must be removed so that strong Si—Si epitaxial bonds across the mating surfaces can be formed. The reaction is illustrated in Equation (1).



The release of hydrogen from a stand-alone silicon wafer dipped in HF was demonstrated to start at about 367°C . from Si— H_2 and 447°C . from Si—H in an ultrahigh vacuum. Since hydrogen molecules become mobile in silicon only at temperatures higher than 500°C ., annealing at temperatures higher than 700°C . have been found necessary to completely deplete hydrogen from the bonding interface that results in a high bonding energy. Therefore, the smart-cut method for a layer transfer using conventional HF-dipped silicon wafer pairs is not possible because the bonding energy is too low at layer transfer temperatures that are lower than 500°C .

Based on above arguments, it becomes clear that the development of a low temperature epitaxial-like wafer bonding technology that is both cost-effective and manufacturable is essential for many advanced materials and device applications.

SUMMARY OF THE INVENTION

Accordingly, one object of this invention is to provide a wafer bonding method and bonded structure in which epitaxial-like bonding is achieved at near room temperature in ambient conditions without an external pressure.

Another object of this invention is to provide a wafer bonding method and bonded structure using bonding surfaces treated to obtain amorphized or partially amorphized surfaces by ion implantation or plasma, preferably by boron-containing ions or plasma.

These and other objects of the present invention are provided by a method for bonding first and second substrates including steps of preparing substantially oxide-free first and second surfaces of respective first and second substrates, creating a surface defect region in each of said first and second surfaces, and bonding said first and second surfaces. Creating the defective region may include plasma-treating the first and second surfaces of the first and second sub-

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strates with a plasma, and preferably a boron-containing plasma. The plasma-treating step may utilize a plasma in reactive ion etch (RIE) mode using B_2H_6 gas, and possibly a mixture of B_2H_6 , He, and Ar gases. Other gas plasmas, such as Ar may also be used.

As a result of the plasma-treating step, a thin amorphous layer may be formed in the first and second surfaces. A monolayer of boron may also be on said first and second surfaces and first and second surfaces may be doped with boron when a boron-containing plasma is used. Also, a few monolayers of boron are introduced into each of the first and second surfaces during said plasma-treating step.

After contacting, the substrates are maintained in contact, preferable under low vacuum but also in ambient air. A bonding energy of about 400 mJ/m² may be obtained at room temperature. Also, when the bonded pair of substrates is maintained at a temperature no more than about 250° C. after contacting, a bond strength of at least about 1500 mJ/m² may be obtained, and a bonding energy of about 2500 mJ/m² (bulk silicon fracture energy) may be obtained at 350° C. The method may also include step of annealing said bonded first and second surfaces at a temperature in the range of about 250–450° C., or at a temperature not exceeding about 350° C. A substantial portion of said amorphous layers in said first and second surfaces may be recrystallized, possibly in a separate annealing step.

The creating step may also include ion-implanting the first and second surfaces. As or B may be used to implant the surfaces. In the case of B, a surface layer is formed on the surface of the substrate and the energy of the implant is chosen to place the peak of the concentration profile at approximately the interface between the substrate surface and the surface layer. In the case of As, the surface is directly implanted and a thicker amorphous layer may be formed.

After contacting, the implanted substrates are maintained in contact, preferable under low vacuum but also in ambient air. The bonded pair may be heated at a temperature no more than about 400° C. The bonded pair of substrates may be maintained at a temperature no more than about 400° C. after contacting. A bonding energy of about 2500 mJ/m² (bulk silicon fracture energy) may be obtained.

To obtain the substantially oxide-free surfaces, the substrates may be immersed in a first etching solution, such as a hydrofluoric acid solution, before said plasma-treating step, and immersed in a second etching solution, such as a hydrofluoric acid solution, after said plasma-treating step. The substrates may be cleaned before immersing in the first etching solution, preferably using an RCA-1 solution.

The method may also include plasma treating an exposed surface of the bonded pair of substrates in a boron-containing plasma, and bonding a third wafer to said exposed surface.

The method may also include creating the defect region or amorphous layer in the surface of a silicon layer formed on a semiconductor device wafer. Two or more of the treated wafers may be bonded together.

The first and second substrates may be selected from Si, InGaAs, InP, GaAs, Ge, SiC and other semiconductors.

The objects of the invention may also be achieved by a method including amorphization of first and second surfaces of first and second silicon substrates by ion implantation or plasma, and contacting the first and second surfaces to form a bonded pair of substrates. The substrates may be immersed in a first hydrofluoric acid solution before said amorphization step, and immersed in a second hydrofluoric acid solution after said amorphization step by plasma. The sub-

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strates may be cleaned before immersing in the first hydrofluoric acid solution, preferably using an RCA-1 solution. The amorphization step may utilize arsenic (As) ion implantation or argon (Ar) RIE plasma.

After contacting, the substrates are maintained in contact, preferable under low vacuum but also in ambient air. The bonded pair may be heated at a temperature no more than about 400° C. The bonded pair of substrates may be maintained at a temperature no more than about 400° C. after contacting. A bonding energy of about 2500 mJ/m² (bulk silicon fracture energy) may be obtained. The bonded amorphous layers at the bonding interface can be completely recrystallized after annealing at 450° C.

The objects of the invention may also be achieved by a bonded structure having a first substrate having a first surface, a first amorphous layer formed in the first surface, and a second substrate having a second surface, a second amorphous layer formed in the second surface. The first surface is bonded to the second surface to form a bonded pair of substrates.

One of said first and second substrates of said bonded pair may have a third surface with an amorphous layer. A third substrate having a fourth surface, with a fourth amorphous layer formed in said fourth surface may be bonded to the bonded pair.

The first and second surfaces may comprise a surface exposed to boron-containing plasma. One of the first and second substrates of the bonded pair may have a planar surface exposed to boron-containing plasma bonded to a third surface of a third substrate exposed to boron-containing plasma. The first, second and third substrates may be selected from Si, InGaAs, InP, GaAs, Ge, SiC and other semiconductors.

The first and second substrates may comprise respective first and second semiconductor devices, the first surface may comprise a substantially planar surface of a first silicon layer formed on the first device, and the second surface may comprise a substantially planar surface of a second silicon layer formed on the second device.

The first surface may comprise a first silicon surface exposed to an inert gas plasma, and the second surface may comprise a second silicon surface exposed to an inert gas plasma.

The first surface may comprise a first silicon surface implanted with boron, and the second surface may comprise a second silicon surface implanted with boron.

The first surface may comprise a first silicon surface implanted with arsenic, and the second surface may comprise a second silicon surface implanted with arsenic.

The bonded structure according to the invention may include a first substrate having an amorphized first surface and containing boron and a second substrate having an amorphized second surface and containing boron, with the first surface being bonded to the second surface to form a bonded pair of substrates. The first and second substrates may be selected from Si, InGaAs, InP, GaAs, Ge, SiC and other semiconductors.

The first surface may comprise a first silicon surface exposed to a boron-containing plasma, and the second surface may comprise a second silicon surface exposed to a boron-containing plasma.

The first surface may comprises a first silicon surface implanted with boron, and the second surface may comprise a second silicon surface implanted with boron.

The bonded structure may also have a first substrate having a first surface implanted with boron, and a second

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substrate having a second surface implanted with boron. The first surface is bonded to said second surface to form a bonded pair of substrates. One of the first and second substrates of the bonded pair may have a planar surface implanted with boron. A third surface, implanted with boron, of a third substrate may be bonded to the planar surface. The first, second and third substrates may be selected from Si, InGaAs, InP, GaAs, Ge, SiC and other semiconductors.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete appreciation of the invention and many of the attendant advantages thereof will be readily obtained as the same becomes better understood by reference to the following detailed description when considered in connection with the accompanying drawings, wherein:

FIG. 1 is a flow chart illustrating method steps of the present invention;

FIGS. 2A-2E are sectional diagrams illustrating a first embodiment of the method according to the invention, and a bonded structure according to the invention;

FIG. 3 is graph depicting room temperature bonding energy as a function of storage time of bonded pairs of B_2H_6 treated hydrophobic silicon wafers;

FIG. 4 is a graph depicting bonding energy as a function of annealing temperature of B_2H_6 treated, boron-implanted treated, Ar plasma treated, and conventional hydrophobic (HF dipped only) silicon wafer pairs;

FIG. 5 is a graph depicting bonding energy as a function of annealing time at 250°C . for B_2H_6 treated wafer pairs;

FIG. 6 is a schematic of surface terminations on B_2H_6 plasma treated and HF dipped silicon wafers;

FIG. 7 is a flow chart showing a second embodiment of the method according to the present invention;

FIGS. 8A-8C are sectional diagrams illustrating a second embodiment of the method according to the invention, and a bonded structure according to the invention;

FIG. 9 is a graph depicting bonding energy as a function of annealing temperature;

FIG. 10 is an TEM (Transmission Electron Microscopy) image of an As-implanted amorphous-Si/amorphous-Si (a-Si/a-Si) bonding interface;

FIG. 11 is a HRTEM (High Resolution TEM) image of an As-implantation induced amorphous layer in a bonding wafer;

FIG. 12 is a HRTEM image for an As-implanted bonded pair after annealing;

FIG. 13 is a graph depicting bonding energy as a function of annealing temperature of B_2H_6 treated InP/InP wafer pairs;

FIG. 14 is a graph depicting bonding energy as a function of annealing temperature of B_2H_6 treated Si/InP wafer pairs;

FIGS. 15A-15C are diagrams of a forming a bonded structure according to the invention; and

FIGS. 16A-16E are diagrams of a forming a bonded structure according to the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to the drawings, wherein like reference numerals designate identical or corresponding parts throughout the several views, and more particularly to FIG. 1 thereof, FIG. 1 shows method steps of the present invention. In step 100, the substrates are cleaned using, for

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example, a wet RCA-1 ($H_2O+H_2O_2+NH_4OH$) solution. Other cleaning methods are possible, such as $H_2SO_4+H_2O_2$ or dry clean. Following the cleaning step using the RCA-1 solution, the substrates are immersed in step 101 in a hydrofluoric acid aqueous solution such as 1%HF solution to remove the surface thin native oxide layer. Upon removal from the hydrofluoric acid solution, the surfaces of the substrates are modified by creating surface and/or subsurface damage areas by ion implantation or plasma, preferably using boron-containing ions or boron-containing plasma, in step 102. By subsurface, it is meant at least the layer of atoms below the surface layer. The treatment may approach or reach amorphization to form a thin amorphous layer may be formed in the surface of the substrates. The surface treatment, when using boron, may introduce boron into the substrate surface.

Upon termination of the treatment, the substrates in step 103 are immersed in a dilute hydrofluoric acid aqueous solution such as 1%HF solution to remove the surface thin native oxide layer or any other oxide formed on the surface. Surfaces of the substrates which were treated in step 103 are placed together in step 104 at room temperature in atmosphere and form a room temperature bonded substrate pair. The attached substrate pair is preferably placed inside a low vacuum system, but may also be placed in ambient. The bonded pair is then annealed at low temperatures in step 105. The temperature may be selected to recrystallize the thin amorphous layers formed during the ion implantation or plasma treatment. Recrystallization may also be carried out in a separate annealing procedure. The wafer bonding method of the present invention achieves high bonding energy near room temperature.

FIGS. 2A-2E show sectional views of the first embodiment of the method according to the invention. In FIG. 2A, a substrate 200, after immersing in the aqueous HF solution, is exposed to a plasma 201. FIG. 2B illustrates wafer 200 after the plasma treatment. The plasma modifies the surface 202 of the wafer to create defect areas and possibly a thin amorphous layer. Subsurface (the layer adjacent the surface) defect areas may also be formed. Surface 202 is drawn with a heavier line to illustrate the defective area or amorphous layer formed by the plasma treatment. The amorphous layer formed is about a few nm or more in thickness. In a preferred case, the plasma is a boron-containing plasma and, most preferably, a B_2H_6 plasma. The position of the B in the surface structure will be described below in connection with FIG. 6.

The wafer is immersed in the aqueous HF solution as described above. Another wafer 203 having a similarly plasma treated surface 204 is placed in contact with wafer 200 with surfaces 202 and 204 directly contacted to form the bonded structure at room temperature in FIG. 2C. The bonded structure is annealed at a low temperature and is then ready for further processing, such as low-temperature annealing, substrate lapping, device formation, etc., or a combination of processes. The process may be continued by plasma-treating the exposed surface 205 of wafer 203 (FIG. 2D) and bonding it to another plasma-treated surface 207 of wafer 206 (FIG. 2E). Any number of substrates may be bonded together.

EXAMPLE

75 mm diameter, 1-10 ohm-cm, p-type Si (100) substrate wafers were used. The wafers were cleaned in a RCA-1 solution, dipped in a 1% hydrofluoric aqueous solution followed by treatment in B_2H_6 plasma for an appropriate

time period depending on the plasma system used. Appropriate plasma treatment times have ranged from 30 sec. to 5 min. The B_2H_6 plasma treatment consisted of a mixed gas of 20 sccm of 0.5% $B_2H_6/99.5\%He$ and 20 sccm Ar in an inductor coupled plasma (ICP) operating in a reactive ion etch mode with a RF power of 38 W at a pressure of ~5 mTorr. A ~100 V self-biased voltage was generated. This self-bias is the lowest possible self-bias for a stable plasma treatment in the plasma treatment system used herein. The wafers were then dipped in a diluted 1% HF solution to remove any oxide on the wafer surfaces. The wafers were then placed together without water rinse and bonded in air at room temperature.

The bonded wafer pair was stored in a low vacuum chamber at a vacuum level of about, for example, 700 Pa. The vacuum level is not critical. The bonding energy (specific surface energy) of the bonded pairs was determined by measuring the crack length introduced by inserting a razor blade into the bonding interface to partially separate the two wafers. FIG. 3 shows the room temperature bonding energies as a function of storage time for B_2H_6 plasma-treated hydrophobic bonded silicon wafers. Compared with a typical room temperature bonding energy of ~10–20 mJ/m² for conventional HF-dipped silicon wafer pairs, the bonding energy of ~400 mJ/m² for the B_2H_6 treated pairs is remarkably higher. A few interface bubbles were formed during low vacuum storage at room temperature, which supports the latter explanation that hydrogen released from the bonding interfaces is responsible for the increase of bonding energy at room temperature.

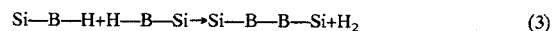
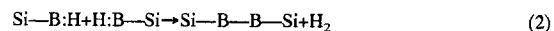
Bonding energy as a function of annealing temperature of B_2H_6 treated, boron-implanted treated, Ar plasma treated, and conventional hydrophobic (HF dipped only) silicon wafer pairs is shown in FIG. 4. It is important to note that for the B_2H_6 plasma treated samples, the bonding energy was ~900 mJ/m² at 150° C. and ~1800 mJ/m² at 250° C., and reaches the fracture energy of bulk silicon ~2500 mJ/m² at 350° C. For comparison, FIG. 4 also shows the bonding energy as a function of annealing temperature of conventional BF dipped silicon wafer pairs. TEM (Transmission Electron Microscopy) measurements have shown that the epitaxial bonding interface in the Si/Si bonded pairs was realized after 350° C. annealing.

A typical example of bonding energy as a function of annealing time at 250° C. is shown in FIG. 5. The bonding energy increases quickly with annealing time and is saturated after ~20 h annealing at 250° C. A few bubbles were generated during annealing indicating that the increase in bonding energy is associated with the release of hydrogen at the bonding interface.

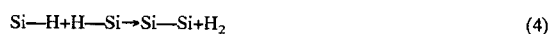
The B_2H_6 plasma treatment of present invention places boron not only on the surface but also in subsurface layers due to the self-bias voltage. After the HF dip, in addition to Si—H₂, Si—H and Si—F surface terminations, the B_2H_6 plasma-treated silicon surfaces will likely be terminated by Si—B:H from top surface boron atoms forming Si—B groups, by Si—B—H groups by boron at the first surface layer, and by Si—H and Si—H₂ groups that have subsurface boron atoms terminated to the silicon atoms, see FIG. 6. The bonding interface between the silicon wafer pair is most likely bridged by HF molecules resulting from the HF dip that can be removed by storage in low vacuum or in ambient at room temperature.

Since B—H complexes are very weakly polarized due to their similar electronegativity, the following reactions at the

bonding interface are likely responsible for the increase in bonding energy at room temperature:



The removal of hydrogen terminations on the boron atoms leads to a Si—B—B—Si bridging bond attaching one substrate to another. Moreover, as reported by Kim et al. in Applied Physics Letters 69, 3869 (1996), subsurface boron in the second layer weakens the surface Si—H bond. Hydrogen desorption from the bonding surfaces of B_2H_6 treated silicon wafers can take place at low temperatures resulting in a silicon covalent bond formation across the interface between the substrates as shown by the following reaction:



The boron-assisted reaction completely depletes hydrogen from the bonding interface at temperatures of 350–400° C. which is lower than a 700° C. temperature which is required for conventional HF dipped silicon substrate bonding, when no boron is present.

In a second embodiment, an inert gas plasma is used to create the defective area and thin amorphous layer. The third embodiment preferably uses an Ar-only plasma treatment to enhance the bonding energy at low temperatures, also shown in FIG. 4. Method steps for an Ar-only plasma treatment bonding process follow all the steps shown in FIG. 1. After cleaning in RCA1 solution (step 100), silicon wafers are dipped in 1%HF solution to remove the native oxide layer of any other oxide layer (step 101). The wafers are placed in the RIE plasma system and treated with Ar plasma in 30–100 mtorr for 15 seconds to 20 minutes. Ar plasma is generated by applying a RF power from 80–200 W at 13.56 MHz (step 102). The surface self-bias voltage is in the range of 200 V to 400 V. These Ar plasma treated wafers are dipped in 1%HF to remove any surface oxide layer (step 103) and bonded at room temperature in air (step 104). After storage in low vacuum for ~20 hrs (step 105), the bonded pairs are annealed. The bonding energy reaches the bulk silicon fracture energy (2500 mJ/m²) at 400° C. The bonding energy enhancement is likely due to that the amorphous layer formed by the Ar plasma treatment readily absorbs the hydrogen released from surface Si—H₂ and Si—H groups that takes place at about 300° C. The amorphous layer at the bonding interface may be recrystallized at low temperatures. Ar-only plasma treatment to enhance low temperature epitaxial-like bonding is especially attractive for applications that requires no monolayers of boron at the bonding interface.

A third embodiment of the present invention (shown in FIG. 7) is to use ion implantation to place boron onto the surfaces of bonding substrates. In step 700, the substrates are covered by a masking layer, preferably an oxide layer. The substrates are cleaned using, for example, a wet RCA-1 solution and dried. In step 701, surfaces of the substrates are implanted with boron using BF₃ as shown in step 702 to place the boron concentration peak at the oxide/silicon interface. As an example, forming an 800 Å thick thermal oxide on silicon wafers, boron implantation at an energy of 20 keV with a dose of $5 \times 10^{14}/\text{cm}^2$ places boron concentration peak of $6 \times 10^{19}/\text{cm}^2$ at the oxide/silicon interface. Employing a 6700 Å thick thermal oxide on silicon wafers, boron implantation at an energy of 180 keV with a dose of $5 \times 10^{14}/\text{cm}^2$ places boron concentration peak of $2.5 \times 10^{19}/\text{cm}^2$ at the oxide/silicon interface.

Following boron implantation, the substrates in step 703 are immersed in a dilute hydrofluoric acid solution to

remove the oxide layer. Surfaces of the substrates which were boron-implanted in step 702 are bonded at room temperature in step 704. The attached pair is preferably placed inside a low vacuum system and annealed in air at low temperature in step 705.

Boron implantation in bonding silicon wafers can achieve the bulk silicon fracture energy at $\sim 400^\circ\text{C}$. The bonding energy enhancement at room temperature seen with the boron plasma treated wafers is not achieved. Instead, a significant increase in bonding energy is seen at temperatures above than 300°C ., as shown in FIG. 4. It is likely that lower boron concentrations on the wafer surfaces for the boron implantation treatment in comparison to the plasma treatment case delays bonding enhancement until higher annealing temperatures are used.

Released hydrogen shown in equation (4) can build an internal pressure that offsets the bonding strength at the bonding interface. In order to alleviate the internal gas pressure, released hydrogen molecules need to be removed from the interface. The plasma or ion implantation treatment according to the invention induces a defective surface layer towards amorphization providing hydrogen trapping sites. Plasma or ion implantation treatments using other gases containing boron are expected to work as well.

FIGS. 8A–8C show cross sectional views of the third embodiment of the method. Ions 801 are implanted into a wafer 800 having a masking film 805, such as SiO_2 , formed on the surface, as shown in step 8A. The masking film 805 allows the energy of the implant to be adjusted so that the peak of the concentration distribution is at the surface of wafer 800. As shown in FIG. 8B, the wafer 800 has a modified surface 802 (shown with heavier line for illustrative purpose only) after removing the masking layer by immersing in an aqueous HF solution, in the case of layer 305 being SiO_2 . Another wafer 803 similarly treated with a modified surface 804 is placed in contact with wafer 800 at room temperature. The bonding of the two wafers is allowed to enhance with low-temperature annealing, as discussed above.

A fourth embodiment of the present invention is to use As (arsenic) ion implantation to silicon wafers to form an amorphous layer on the wafer surface. Method steps for an As ion implantation treatment bonding process follow the steps shown in FIG. 1. After cleaning, As ion implantation is performed at an energy of 180 keV with a dose of $9 \times 10^{14}/\text{cm}^2$. Any oxide layer is then removed prior to bonding. The As doping concentration peak of $8 \times 10^{19}/\text{cm}^3$ is located at 1150 Å from the silicon surface. Although this implantation induced a very low As doping on the wafer surface, an amorphous layer with 1650 Å thick was formed as confirmed both by a Monte Carlo simulation and TEM measurement (FIG. 10). The thickness of the amorphous layer can vary and is not limited to the value of this example. For instance, other ions may be implanted to create the amorphous layer. Arsenic is a dopant, and there are applications when it is desired not to dope the substrate so another ion, such as a non-doping ion like Ar, would be chosen.

After an HF dip to remove any oxide on the implanted surfaces, the wafers are bonded at room temperature in ambient conditions. After storage in low vacuum for ~ 20 h the bonded pairs are annealed in air. The bonding energy as a function of annealing temperature is shown in FIG. 9. The bonding energy reaches the bulk silicon fracture energy (2500 mJ/m^2) at 400°C . Bonded pairs of the As implanted silicon wafers that were annealed at 900°C . to fully recrystallize the amorphous layers before bonding have shown the same bonding energy of $\sim 400 \text{ mJ/m}^2$ as the conventional HF

dipped Si/Si pairs after 400°C . annealing. It is clear that as in the Ar plasma treatment case, the amorphous layers rather than As doping at the bonding interface play a key role in enhancing bonding energy at low temperatures.

FIGS. 10–12 show TEM images of the As-implanted substrates, and As-implanted bonded substrate pairs. In FIG. 10, a TEM image of bonding interface between the amorphous silicon layers (a-Si/a-Si) that were formed by As implantation is shown. FIG. 11 shows an HRTEM image of the interface between the amorphous silicon and the crystal silicon substrate (a-Si/c-Si). The amorphous layer is reduced to 100 Å in thickness after annealing for 24 hours at 450°C ., as shown in FIG. 12.

The above methods can be applied to other substrate combinations involving materials such as InP, GaAs, Ge, SiC, etc. Using the B_2H_6 plasma treatment process described in the first embodiment to InP/InP epitaxial-like wafer bonding, the bonding energy of the bonded InP/InP pairs reached the (100) InP bulk fracture energy of $\sim 600 \text{ mJ/m}^2$ after annealing at 200°C . for 24 h. FIG. 13 shows the bonding energy as a function of annealing temperature of the B_2H_6 treated InP/InP wafer pairs. For comparison, the bonding energy as a function of annealing temperature of conventional HF dipped InP/InP pairs is also shown.

The similar results were obtained for bonding a silicon wafer to an InP wafer. Using the B_2H_6 plasma treatment process described in the first embodiment to Si/InP epitaxial-like wafer bonding, the bonding energy of the bonded Si/InP pairs reached the (100) InP bulk fracture energy of $\sim 600 \text{ mJ/m}^2$ after annealing at 200°C . for 24 h. FIG. 14 shows the bonding energy as a function of annealing temperature of the B_2H_6 treated Si/InP wafer pairs. For comparison, the bonding energy as a function of annealing temperature of conventional HF dipped Si/InP pairs is also shown.

Two or more wafers having a silicon layer formed on the surface may also be bonded, as shown in FIGS. 15A–15C. Silicon layer 1502 of substrate 1500 is exposed to plasma 1503 in FIG. 15A. A similarly treated surface 1505 of wafer 1504 is placed in contact with surface 1502 and bonded (FIG. 15B). Surface 1505 may also be ion-implanted. The exposed surface of substrate 1504 may also be exposed to a plasma and bonded with treated surface 1507 of wafer 1506 to form a three-substrate bonded structure, as shown in FIG. 15C. These wafers may be processed wafers having devices and/or circuits formed therein with the silicon layer formed after device and/or circuit formation. The silicon layer should be planar, and may be planarized using techniques such as CMP. The silicon layer is treated using a plasma or ion-implantation, as discussed above. This structure preferably used the boron-containing plasma or boron implantation. Also, unique device structures such as double-sided power diodes, pin photodiodes and avalanche photodiodes may be realized. While the above embodiments are directed to substrates, it should be understood that a substrate may be of varying thickness. In other words, thin substrates may be bonded to other substrates, or bonded with two substrates to be between the substrates. A bonded substrate may also be thinned to a desired thickness by lapping or polishing, as discussed above. FIGS. 16A–16E illustrate this. The surface of substrate 1600 is exposed to plasma 1601 to form treated surface 1602 (FIGS. 16A and 16B). Surface 1602 has a surface defect region and may be amorphized. Another substrate 1603 with a treated surface 1604 is bonded to surface 1602 (FIG. 16B). In FIG. 16C, a portion of substrate 1603 is removed by lapping, polishing, etc. to leave portion 1605 with surface 1606. Surface 1606 may then be exposed to a plasma (FIG. 16D) and another wafer 1607 with treated

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surface 1608 may be bonded to surface 1606 (FIG. 16E). Unique structures where different materials of desired thicknesses may be bonded and formed according to the invention.

Some advantages of the wafer-bonding process of the present invention are that the process utilizes manufacturable steps which bond wafers at room temperature in ambient air and annealed at temperatures no higher than 450° C. to reach an epitaxial-like bond. Pre-annealing at elevated temperatures, external pressure, or high vacuum to achieve a high bonding energy are not required. The process uses common RIE plasma treatments or ion implantation that are economic, convenient and easy to implement.

In addition to the epitaxial-like wafer bonding for materials combination for preparing advanced devices such as pin and avalanche photodiodes, the process shown here can have applications in bonding unique device structures such as bonding back sides of two fully processed power devices to form double-sided power devices, can allow the device layer transfer onto carrier substrates with an epitaxial-like interface, and can be used to transfer device layers to more thermally conductive materials thus enhancing thermal management.

Numerous other modifications and variations of the present invention are possible in light of the above teachings. It is therefore to be understood that within the scope of the appended claims, the present invention may be practiced otherwise than as specifically described herein.

What is claimed as new and desired to be secured by Letters Patents of the United States is:

1. A bonded structure, comprising:
 - a first substrate having a first surface, a first nearly-amorphized layer containing one of boron and arsenic formed uniformly over said first surface; and
 - a second substrate having a second surface, a second nearly-amorphized layer containing one of boron and arsenic formed uniformly over said second surface;
 said first surface being bonded to said second surface to form a bonded pair of substrates.
2. A structure as recited in claim 1, comprising:
 - one of said first and second substrates of said bonded pair having a third surface, said third surface having a nearly-amorphized layer;
 - a third substrate having a fourth surface, a fourth nearly-amorphized layer formed in said fourth surface; and
 - said third surface bonded to said fourth surface.
3. A structure as recited in claim 1, wherein said first and second substrates are selected from Si, InGaAs, InP, GaAs, Ge and SiC.
4. A structure as recited in claim 1, wherein:
 - said first and second substrates each comprises a silicon substrate; and
 - said first and second surfaces each comprises a silicon surface.
5. A structure as recited in claim 1, wherein:
 - said first and second substrates comprise respective first and second semiconductor devices.
6. A structure as recited in claim 1, wherein:
 - said first surface comprises a first silicon surface exposed to a boron-containing plasma; and
 - said second surface comprises a second silicon surface exposed to a boron-containing plasma.
7. A structure as recited in claim 1, wherein:
 - said first surface comprises a first silicon surface implanted with boron; and

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said second surface comprises a second silicon surface implanted with boron.

8. A structure as recited in claim 1, wherein:

said first surface comprises a first silicon surface implanted with arsenic; and

said second surface comprises a second silicon surface implanted with arsenic.

9. A structure as recited in claim 1, comprising:

at least one of boron-boron and Si covalent bonds formed between said first and second substrates.

10. A structure as recited in claim 1, wherein:

said first and second amorphous layers are each in the range of a few nm in thickness.

11. A structure as recited in claim 1, wherein said first and second layers each comprise a few monolayers of boron.

12. A structure as recited in claim 1, wherein:

said first surface comprises an amorphous boron-containing layer; and

said second surface comprises an amorphous boron-containing layer.

13. A structure as recited in claim 1, wherein:

said first surface comprises a surface exposed to a boron-containing plasma; and

said second surface comprises a surface exposed to a boron-containing plasma.

14. A structure as recited in claim 1, wherein:

said first surface comprises a first surface exposed to an inert gas plasma; and

said second surface comprises a second surface exposed to an inert gas plasma.

15. A bonded structure, comprising:

a first substrate having a first surface, substantially all of said first surface being amorphized and containing boron;

a second substrate having a second surface, substantially all of said second surface being amorphized and containing boron; and

said first surface being bonded to said second surface to form a bonded pair of substrates.

16. A structure as recited in claim 15, wherein said first and second substrates are selected from Si, InGaAs, InP, GaAs, Ge, SiC.

17. A structure as recited in claim 15, wherein:

said first surface comprises a first silicon surface exposed to a boron-containing plasma; and

said second surface comprises a second silicon surface exposed to a boron-containing plasma.

18. A structure as recited in claim 15, wherein:

said first surface comprises a first silicon surface implanted with boron; and

said second surface comprises a second silicon surface implanted with boron.

19. A structure as recited in claim 15, comprising:

forming at least one of boron-boron and Si covalent bonds between said first and second substrates.

20. A structure as recited in claim 15, wherein:

said amorphized first and second surfaces are each in the range of a few nm in thickness.

21. A structure as recited in claim 15, wherein:

said amorphized first and second layers each comprises a few monolayers of boron.

22. A bonded structure, comprising:

a first substrate having a first surface, a first amorphous arsenic-containing layer formed in substantially all of said first surface; and

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a second substrate having a second surface, a second amorphous arsenic-containing layer formed in substantially all of said second surface;
 said first surface being bonded to said second surface to form a bonded pair of substrates.
 23. A structure as recited in claim 22, comprising:
 one of said first and second substrates of said bonded pair having a third surface, said third surface having an amorphous layer;
 a third substrate having a fourth surface, a fourth amorphous layer formed in said fourth surface; and
 said third surface bonded to said fourth surface.
 24. A structure as recited in claim 23, wherein:
 said third surface comprises an amorphous arsenic-containing layer; and
 said fourth surface comprises an amorphous arsenic-containing layer.
 25. A structure as recited in claim 22, wherein said first and second substrates are selected from Si, InGaAs, InP, GaAs, Ge and SiC.
 26. A structure as recited in claim 22, wherein:
 said first and second substrates each comprises a silicon substrate; and
 said first and second surfaces each comprises an arsenic-containing silicon surface.
 27. A structure as recited in claim 22, wherein:
 said first surface comprises a substantially planar surface of a first arsenic-containing silicon layer formed on said first substrate; and
 said second surface comprises a substantially planar surface of a second arsenic-containing silicon layer formed on said second substrate.
 28. A structure as recited in claim 22, wherein:
 said first surface comprises a first silicon surface implanted with arsenic; and
 said second surface comprises a second silicon surface implanted with arsenic.
 29. A structure as recited in claim 28, comprising:
 Si covalent bonds formed between said first and second substrates.
 30. A structure as recited in claim 22, comprising:
 said first and second surfaces being substantially oxide-free.
 31. A structure as recited in claim 22, wherein:
 said amorphized first and second surfaces are each in the range of a few nm in thickness.
 32. A structure as recited in claim 22, wherein:
 said amorphized first and second surfaces each comprises a few monolayers of arsenic.
 33. A bonded structure, comprising:
 a first substrate having a substantially oxide-free first surface, a substantial portion of said first surface being amorphized and containing one of boron and arsenic; and
 a second substrate having a substantially oxide-free second surface, a substantial portion of said first surface being amorphized and containing one of boron and arsenic;
 said first surface being bonded to said second surface to form a bonded pair of substrates.
 34. A structure as recited in claim 33, wherein:
 said first substrate comprises one material having said first surface; and
 said second substrate comprises one material having said second surface.

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35. A structure as recited in claim 33, comprising:
 one of said first and second substrates of said bonded pair having an amorphized substantially oxide-free third surface;
 a third substrate having an amorphized substantially oxide-free fourth surface; and
 said third surface bonded to said fourth surface.
 36. A structure as recited in claim 33, wherein said first and second substrates are selected from Si, InGaAs, InP, GaAs, Ge and SiC.
 37. A structure as recited in claim 33, wherein:
 said first and second substrates each comprises a silicon substrate; and
 said first and second surfaces each comprises an amorphized substantially oxide-free silicon surface.
 38. A structure as recited in claim 33, wherein:
 said first surface comprises a substantially planar surface of a first amorphous substantially oxide-free silicon layer formed on said first substrate; and
 said second surface comprises a substantially planar surface of a second amorphous substantially oxide-free silicon layer formed on said second substrate.
 39. A structure as recited in claim 33, wherein:
 said first surface comprises a surface exposed to a boron-containing plasma; and
 said second surface comprises a surface exposed to a boron-containing plasma.
 40. A structure as recited in claim 33, wherein:
 said first surface comprises an ion-implanted surface; and
 said second surface comprises an ion-implanted surface.
 41. A structure as recited in claim 33, wherein:
 said first surface comprises a surface ion-implanted with one of boron and arsenic; and
 said second surface comprises a surface ion-implanted with one of boron and arsenic.
 42. A structure as recited in claim 41, comprising:
 boron-boron formed between said first and second substrates.
 43. A bonded structure, comprising:
 a first substrate having a first surface with an amorphized first surface region extending only one to a few monolayers into said first substrate; and
 a second substrate having a second surface an amorphized second surface region extending only one to a few monolayers into said second substrate; and
 said first surface being bonded to said second surface to form a bonded pair of substrates.
 44. A structure as recited in claim 43, wherein:
 said amorphized first and second surface regions are each in the range of a few nm in thickness.
 45. A structure as recited in claim 43, wherein:
 said first and second surface regions each comprise at least one region extending over a substantial portion of a surface of said first and second substrates, respectively.
 46. A structure as recited in claim 43, comprising:
 one of said first and second substrates of said bonded pair having a third surface with an amorphized third surface region;
 a third substrate having a fourth surface with an amorphized fourth surface region; and
 said third surface bonded to said fourth surface.
 47. A structure as recited in claim 43, wherein said first and second substrates are selected from Si, InGaAs, InP, GaAs, Ge and SiC.

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48. A structure as recited in claim 43, wherein:
said first and second substrates each comprises a silicon
substrate; and
said first and second surfaces each comprises a silicon
surface. 5
49. A structure as recited in claim 43, wherein:
said first surface comprises a surface exposed to a boron-
containing plasma; and
said second surface comprises a surface exposed to a 10
boron-containing plasma.
50. A structure as recited in claim 43, wherein:
said first surface comprises an ion-implanted surface; and
said second surface comprises an ion-implanted surface.
51. A structure as recited in claim 43, wherein: 15
said first surface comprises a surface implanted with one
of boron and arsenic; and
said second surface comprises a second surface implanted
with one of boron and arsenic.
52. A structure as recited in claim 50, comprising: 20
boron-boron covalent bonds formed between said first and
second substrates.
53. A bonded structure, comprising:
a first substrate of substantially one first material amor- 25
phized substantially only in a first surface of said first
material and containing one of boron and arsenic; and
a second substrate of substantially one second material
amorphized substantially only in a second surface of
said second material and containing one of boron and 30
arsenic;
said first surface being bonded to said second surface to
form a bonded pair of substrates.
54. A structure as recited in claim 53, comprising: 35
one of said first and second substrates of said bonded pair
being amorphized only in said first surface and in a
third surface of said first material;

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- a third substrate of substantially one third material amor-
phized only in a third surface of said third material; and
said third surface bonded to said fourth surface.
55. A structure as recited in claim 53, wherein said first
and second substrates are selected from Si, InGaAs, InP,
GaAs, Ge and SiC.
56. A structure as recited in claim 53, wherein:
said first and second substrates each comprises a silicon
substrate; and
said first and second surfaces each comprises a silicon
surface.
57. A structure as recited in claim 53, wherein:
said first surface comprises a substantially planar surface
of a first silicon layer formed on said first device; and
said second surface comprises a substantially planar sur-
face of a second silicon layer formed on said second
device.
58. A structure as recited in claim 53, wherein:
said first surface comprises a surface exposed to a boron-
containing plasma; and
said second surface comprises a surface exposed to a
boron-containing plasma.
59. A structure as recited in claim 53, wherein:
said first surface comprises a surface implanted with one
of boron and arsenic; and
said second surface comprises a surface implanted with
one of boron and arsenic.
60. A structure as recited in claim 59, comprising:
boron-boron covalent bonds formed between said first and
second substrates.

* * * * *

Printed 03/13/2001

APPLICATION NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET
09/635,272	08/09/2000	257	2815	2025-0180-

APPLICANT
QIN-YI TONG, DURHAM, NORTH CAROLINA.

*CONTINUING DOMESTIC DATA*****
VERIFIED
Q *None*

371 (NAT'L STAGE) DATA*****
VERIFIED
Q *None*

FOREIGN APPLICATIONS***
VERIFIED
Q *None*

FOREIGN FILING LICENSE GRANTED 09/23/2000

SMALL ENTITY

Foreign priority claimed 35 USC 119 (a-d) conditions met	<input type="radio"/> yes <input checked="" type="radio"/> no <input type="radio"/> yes <input checked="" type="radio"/> no <input type="radio"/> Met after Allowance	STATE OR COUNTRY NC	SHEETS DRAWINGS 11	TOTAL CLAIMS 58	INDEPENDENT CLAIMS 4
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Verified and acknowledged *Q* *Q*
Examiner's Name Initials

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TITLE
METHOD OF EPITAXIAL-LIKE WAFER BONDING AT LOW TEMPERATURE AND BONDED STRUCTURE

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

1/18/2000 ASELLMAN 00000050 09635272

1 FC:201	345.00 OP
2 FC:203	342.00 OP
1 FC:202	39.00 OP

PTO-1556
(5/87)

*U.S. GPO: 1999-459-082/19144

JC803 U.S. PTO



08/09/00


JC873 U.S. PTO


09/635272



08/09/00

UTILITY PATENT APPLICATION TRANSMITTAL <small>(Only for new nonprovisional applications under 37 CFR 1.53(b))</small>	Attorney Docket No.	2025-0180-20
	First Inventor or Application Identifier	Qin-Yi TONG
	Title	A METHOD OF EPITAXIAL-LIKE WAFER BONDING AT LOW TEMPERATURE AND BONDED STRUCTURE

APPLICATION ELEMENTS <small>See MPEP chapter 600 concerning utility patent application contents</small>	ADDRESS TO: Assistant Commissioner for Patents Box Patent Application Washington, DC 20231
<p>1. <input checked="" type="checkbox"/> Fee Transmittal Form (e.g. PTO/SB/17) (Submit an original and a duplicate for fee processing)</p> <p>2. <input checked="" type="checkbox"/> Specification Total Pages 24</p> <p>3. <input checked="" type="checkbox"/> Drawing(s) (35 U.S.C. 113) (FORMALS) Total Sheets 11</p> <p>4. <input checked="" type="checkbox"/> Oath or Declaration Total Pages 2</p> <p>a. <input checked="" type="checkbox"/> Newly executed (original or copy)</p> <p>b. <input type="checkbox"/> Copy from a prior application (37 C.F.R. §1.63(d)) (for continuation/divisional with box 15 completed)</p> <p>i. <input type="checkbox"/> DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §1.63(d)(2) and 1.33(b).</p> <p>5. <input type="checkbox"/> Incorporation By Reference (usable if box 4B is checked) The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4B, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.</p>	ACCOMPANYING APPLICATION PARTS <p>6. <input type="checkbox"/> Assignment Papers (cover sheet & document(s))</p> <p>7. <input type="checkbox"/> 37 C.F.R. §3.73(b) Statement <input type="checkbox"/> Power of Attorney (when there is an assignee)</p> <p>8. <input type="checkbox"/> English Translation Document (if applicable)</p> <p>9. <input type="checkbox"/> Information Disclosure Statement (IDS)/PTO-1449 <input type="checkbox"/> Copies of IDS Citations</p> <p>10. <input type="checkbox"/> Preliminary Amendment</p> <p>11. <input checked="" type="checkbox"/> White Advance Serial No. Postcard</p> <p>12. <input checked="" type="checkbox"/> Small Entity Statement <input type="checkbox"/> Statement filed in prior application. Status still proper and desired.</p> <p>13. <input type="checkbox"/> Certified Copy of Priority Document(s) (if foreign priority is claimed)</p> <p>14. <input type="checkbox"/> Other:</p>
<p>15. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below:</p> <p><input type="checkbox"/> Continuation <input type="checkbox"/> Divisional <input type="checkbox"/> Continuation-in-part (CIP) of prior application no.: Prior application information: Examiner: Group Art Unit:</p>	
<p>16. Amend the specification by inserting before the first line the sentence:</p> <p><input type="checkbox"/> This application is a <input type="checkbox"/> Continuation <input type="checkbox"/> Division <input type="checkbox"/> Continuation-in-part (CIP) of application Serial No. Filed on</p> <p><input type="checkbox"/> This application claims priority of provisional application Serial No. Filed</p>	
<p>17. CORRESPONDENCE ADDRESS</p> <p> 22850 (703) 413-3000 FACSIMILE: (703) 413-2220</p>	

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Signature:		Date:	Aug 9, 2000
Name:	Carl E. Schlier	Registration No.:	34,426

TSMC1002

Docket No. 2025-0180-20

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR(S) Qin-Yi TONG
SERIAL NO: New Application
FILING DATE: Herewith

FOR: A METHOD OF EPITAXIAL-LIKE WAFER BONDING AT LOW TEMPERATURE AND BONDED
STRUCTURE

JC873 U.S. PTO
09/635272
08/09/00

FEE TRANSMITTAL

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

FOR	NUMBER FILED	NUMBER EXTRA	RATE	CALCULATIONS
TOTAL CLAIMS	58 - 20 =	38	× \$18 =	\$684.00
INDEPENDENT CLAIMS	4 - 3 =	1	× \$78 =	\$78.00
<input type="checkbox"/> MULTIPLE DEPENDENT CLAIMS (If applicable)			+ \$260 =	\$0.00
<input type="checkbox"/> LATE FILING OF DECLARATION			+ \$130 =	\$0.00
BASIC FEE				\$690.00
TOTAL OF ABOVE CALCULATIONS				\$1,452.00
<input checked="" type="checkbox"/> REDUCTION BY 50% FOR FILING BY SMALL ENTITY				\$-726.00
<input type="checkbox"/> FILING IN NON-ENGLISH LANGUAGE			+ \$130 =	\$0.00
<input type="checkbox"/> RECORDATION OF ASSIGNMENT			+ \$40 =	\$0.00
TOTAL				\$726.00

- ☐ Please charge Deposit Account No. 15-0030 in the amount of A duplicate copy of this sheet is enclosed.
- ☒ A check in the amount of \$726.00 to cover the filing fee is enclosed.
- ☒ The Commissioner is hereby authorized to charge any additional fees which may be required for the papers being filed herewith and for which no check is enclosed herewith, or credit any overpayment to Deposit Account No. 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully Submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

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Date: Aug 9, 2000



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Docket No. 2025-0180-20

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR(S) Qin-Yi TONG

SERIAL NO: New Application

FILING DATE: Herewith

FOR: A METHOD OF EPITAXIAL-LIKE WAFER BONDING AT LOW TEMPERATURE AND BONDED STRUCTURE

JCE73 U.S. PTO
09/635272
08/09/00

FEE TRANSMITTAL

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

FOR	NUMBER FILED	NUMBER EXTRA	RATE	CALCULATIONS
TOTAL CLAIMS	58 - 20 =	38	× \$18 =	\$684.00
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A duplicate copy of this sheet is enclosed.

Respectfully Submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

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Registration No. 34,426

Date: Aug 9, 2000



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2025-0180-20

TITLE OF THE INVENTION

A METHOD OF EPITAXIAL-LIKE WAFER BONDING
AT LOW TEMPERATURE AND BONDED STRUCTURE

BACKGROUND OF THE INVENTION

Field of the Invention:

The present invention relates to a method of epitaxial-like bonding of wafer pairs at low temperature, and more particularly to a method of bonding in which the wafer surfaces are modified to create surface and subsurface defect areas, and possibly amorphized, by ion implantation or plasma, preferably by boron-containing ions or a plasma such as B_2H_6 .

Discussion of the Background:

For many optoelectronic and electronic device applications, homo-epitaxial single crystalline layers consisting of same material with same crystalline orientation but different doping types or levels are necessary. For some device applications, active layers comprising single crystalline dissimilar materials are required. The active layers should be high crystallographic quality with interfaces that are thermally conductive and almost optical loss free. Conventional hetero-epitaxial growth techniques applied to these lattice mismatched active layers usually result in a large density of threading dislocations in the bulk of the layers. Bonding of single crystalline wafers of identical or dissimilar materials is a unique alternative approach to the epitaxial growth. Not only highly lattice-mismatched wafers can be bonded but also wafers with different crystalline orientations can be combined. Ideally, the mismatches of single crystalline bonding wafers are accommodated by dislocations (in lattice-mismatch case) or an amorphous layer (in orientation-mismatch case) localized at the bonding interface with no defects generated in the bulk area. This approach is termed epitaxial-like bonding. The epitaxial-like bonding can also be employed to prepare unique devices by integrating already processed device layers.

However, conventional epitaxial-like bonding is achieved by high temperature annealing. To bond wafers composed of thermally mismatched materials, severe and often damaging thermal stresses can be induced with high temperature annealing. Since thermal

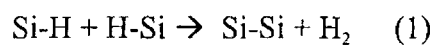
stresses can increase significantly with the size of dissimilar wafers, only small wafers currently can be epitaxially bonded at high temperatures. The high temperature annealing process can also produce unwanted changes to bonding materials and often prevents the bonding of processed device wafers. The bonding materials may decompose at high
5 temperatures, even if the bonding wafers are thermally matched.

In order to epitaxially bond large wafers of dissimilar materials or processed wafers, an epitaxial-like bonding interface must be achieved at or near room temperature, or one wafer of the bonded pair must be thinned sufficiently before annealing to elevated temperatures. Although Göesele et al. in Applied Physics Letters 67, 3614 (1995) and Takagi
10 et al in Applied Physics Letters 74, 2387, 1999 reported room temperature epitaxial-like bonding of silicon wafers in ultrahigh vacuum, high temperature ($>600^{\circ}\text{C}$) pre-annealing in the former case or high external pressure ($>1\text{ MPa}$) in the latter case were required to achieve the bond that may introduce undesired effects to the bonding wafers.

Recently, M. Bruel in Electronics Letters 31,1201 (1995) reported a promising generic
15 thinning approach using a hydrogen-induced layer transfer method (so-called smart-cut method). In this approach, H atoms are implanted into a Si wafer to such concentration that a significant fraction of Si-Si bonds are broken creating a buried H-rich layer of micro-cracks susceptible to cleavage or fracture. By bonding the topmost oxide covered hydrophilic Si wafer surface to another substrate, a thin layer of the Si wafer can then be transferred by
20 fracture of the H-rich region. However, this process requires that the bonding energy between the bonded wafers be higher than the fracture energy of the hydrogen-induced crack region at the layer transfer temperature. The layer transfer temperatures must be lower than the temperature beyond which hydrogen molecules in the material become mobile. For silicon, the temperature is about 500°C (see Chu et al in Physics Review B, 16, 3851 (1987)). The
25 bonding energy of conventional HF dipped hydrophobic silicon wafer pairs is higher than the hydrogen-induced region only after annealing at temperatures higher than 600°C . Therefore, this process does not work for oxide-free hydrophobic silicon wafer bonding.

Typically, HF-dipped, hydrogen-terminated hydrophobic silicon wafers are used to realize epitaxial-like bonding after annealing at $>700^{\circ}\text{C}$. In order for bonded hydrophobic
30 silicon wafer pairs to reach bulk fracture energy, Tong et al. in Applied Physics Letters 64, 625 (1994) reported that hydrogen (from HF-dip, mainly Si-H₂ and Si-H terminated

hydrophobic silicon surfaces at the bonding interface) must be removed so that strong Si-Si epitaxial bonds across the mating surfaces can be formed. The reaction is illustrated in Equation (1).



5 The release of hydrogen from a stand-alone silicon wafer dipped in HF was demonstrated to start at about 367°C from Si-H₂ and 447°C from Si-H in an ultrahigh vacuum. Since hydrogen molecules become mobile in silicon only at temperatures higher than 500°C, annealing at temperatures higher than 700°C have been found necessary to completely deplete hydrogen from the bonding interface that results in a high bonding energy. 10 Therefore, the smart-cut method for a layer transfer using conventional HF-dipped silicon wafer pairs is not possible because the bonding energy is too low at layer transfer temperatures that are lower than 500°C.

Based on above arguments, it becomes clear that the development of a low temperature epitaxial-like wafer bonding technology that is both cost-effective and 15 manufacturable is essential for many advanced materials and device applications.

SUMMARY OF THE INVENTION

Accordingly, one object of this invention is to provide a wafer bonding method and bonded structure in which epitaxial-like bonding is achieved at near room temperature in 20 ambient conditions without an external pressure.

Another object of this invention is to provide a wafer bonding method and bonded structure using bonding surfaces treated to obtain amorphized or partially amorphized surfaces by ion implantation or plasma, preferably by boron-containing ions or plasma.

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These and other objects of the present invention are provided by a method for bonding first and second substrates including steps of preparing substantially oxide-free first and second surfaces of respective first and second substrates, creating a surface defect region in each of said first and second surfaces, and bonding said first and second surfaces. Creating the defective region may include plasma-treating the first and second surfaces of the first and second substrates with a plasma, and preferably a boron-containing plasma. The plasma-treating step may utilize a plasma in reactive ion etch (RIE) mode using B₂H₆ gas, and 30

possibly a mixture of B_2H_6 , He, and Ar gases. Other gas plasmas, such as Ar may also be used.

As a result of the plasma-treating step, a thin amorphous layer may be formed in the first and second surfaces. A monolayer of boron may also be on said first and second surfaces and first and second surfaces may be doped with boron when a boron-containing plasma is used. Also, a few monolayers of boron are introduced into each of the first and second surfaces during said plasma-treating step.

After contacting, the substrates are maintained in contact, preferable under low vacuum but also in ambient air. A bonding energy of about 400 mJ/m^2 may be obtained at room temperature. Also, when the bonded pair of substrates is maintained at a temperature no more than about 250°C after contacting, a bond strength of at least about 1500 mJ/m^2 may be obtained, and a bonding energy of about 2500 mJ/m^2 (bulk silicon fracture energy) may be obtained at 350°C . The method may also include step of annealing said bonded first and second surfaces at a temperature in the range of about $250\text{-}450^\circ\text{C}$, or at a temperature not exceeding about 350°C . A substantial portion of said amorphous layers in said first and second surfaces may be recrystallized, possibly in a separate annealing step.

The creating step may also include ion-implanting the first and second surfaces. As or B may be used to implant the surfaces. In the case of B, a surface layer is formed on the surface of the substrate and the energy of the implant is chosen to place the peak of the concentration profile at approximately the interface between the substrate surface and the surface layer. In the case of As, the surface is directly implanted and a thicker amorphous layer may be formed.

After contacting, the implanted substrates are maintained in contact, preferable under low vacuum but also in ambient air. The bonded pair may be heated at a temperature no more than about 400°C . The bonded pair of substrates may be maintained at a temperature no more than about 400°C after contacting. A bonding energy of about 2500 mJ/m^2 (bulk silicon fracture energy) may be obtained.

To obtain the substantially oxide-free surfaces, the substrates may be immersed in a first etching solution, such as a hydrofluoric acid solution, before said plasma-treating step, and immersed in a second etching solution, such as a hydrofluoric acid solution, after said

plasma-treating step. The substrates may be cleaned before immersing in the first etching solution, preferably using an RCA-1 solution.

The method may also include plasma treating an exposed surface of the bonded pair of substrates in a boron-containing plasma, and bonding a third wafer to said exposed surface.

5 The method may also include creating the defect region or amorphous layer in the surface of a silicon layer formed on a semiconductor device wafer. Two or more of the treated wafers may be bonded together.

The first and second substrates may be selected from Si, InGaAs, InP, GaAs, Ge, SiC and other semiconductors.

10 The objects of the invention may also be achieved by a method including amorphization of first and second surfaces of first and second silicon substrates by ion implantation or plasma, and contacting the first and second surfaces to form a bonded pair of substrates. The substrates may be immersed in a first hydrofluoric acid solution before said amorphization step, and immersed in a second hydrofluoric acid solution after said
15 amorphization step by plasma. The substrates may be cleaned before immersing in the first hydrofluoric acid solution, preferably using an RCA-1 solution. The amorphization step may utilize arsenic (As) ion implantation or argon (Ar) RIE plasma.

20 After contacting, the substrates are maintained in contact, preferable under low vacuum but also in ambient air. The bonded pair may be heated at a temperature no more than about 400°C. The bonded pair of substrates may be maintained at a temperature no more than about 400°C after contacting. A bonding energy of about 2500 mJ/m² (bulk silicon fracture energy) may be obtained. The bonded amorphous layers at the bonding interface can be completely recrystallized after annealing at 450°C.

25 The objects of the invention may also be achieved by a bonded structure having a first substrate having a first surface, a first amorphous layer formed in the first surface, and a second substrate having a second surface, a second amorphous layer formed in the second surface. The first surface is bonded to the second surface to form a bonded pair of substrates.

30 One of said first and second substrates of said bonded pair may have a third surface with an amorphous layer. A third substrate having a fourth surface, with a fourth amorphous layer formed in said fourth surface may be bonded to the bonded pair.

The first and second surfaces may comprise a surface exposed to boron-containing plasma. One of the first and second substrates of the bonded pair may have a planar surface exposed to boron-containing plasma bonded to a third surface of a third substrate exposed to boron-containing plasma. The first, second and third substrates may be selected from Si, InGaAs, InP, GaAs, Ge, SiC and other semiconductors.

The first and second substrates may comprise respective first and second semiconductor devices, the first surface may comprise a substantially planar surface of a first silicon layer formed on the first device, and the second surface may comprise a substantially planar surface of a second silicon layer formed on the second device.

The first surface may comprise a first silicon surface exposed to an inert gas plasma, and the second surface may comprise a second silicon surface exposed to an inert gas plasma.

The first surface may comprise a first silicon surface implanted with boron, and the second surface may comprise a second silicon surface implanted with boron.

The first surface may comprise a first silicon surface implanted with arsenic, and the second surface may comprise a second silicon surface implanted with arsenic.

The bonded structure according to the invention may include a first substrate having an amorphized first surface and containing boron and a second substrate having an amorphized second surface and containing boron, with the first surface being bonded to the second surface to form a bonded pair of substrates. The first and second substrates may be selected from Si, InGaAs, InP, GaAs, Ge, SiC and other semiconductors.

The first surface may comprise a first silicon surface exposed to a boron-containing plasma, and the second surface may comprise a second silicon surface exposed to a boron-containing plasma.

The first surface may comprises a first silicon surface implanted with boron, and the second surface may comprise a second silicon surface implanted with boron.

The bonded structure may also have a first substrate having a first surface implanted with boron, and a second substrate having a second surface implanted with boron. The first surface is bonded to said second surface to form a bonded pair of substrates. One of the first and second substrates of the bonded pair may have a planar surface implanted with boron. A third surface, implanted with boron, of a third substrate may be bonded to the planar surface.

The first, second and third substrates may be selected from Si, InGaAs, InP, GaAs, Ge, SiC and other semiconductors.

BRIEF DESCRIPTION OF THE DRAWINGS

5 A more complete appreciation of the invention and many of the attendant advantages thereof will be readily obtained as the same becomes better understood by reference to the following detailed description when considered in connection with the accompanying drawings, wherein:

FIG. 1 is a flow chart illustrating method steps of the present invention;

10 FIGS. 2A-2E are sectional diagrams illustrating a first embodiment of the method according to the invention, and a bonded structure according to the invention;

FIG. 3 is graph depicting room temperature bonding energy as a function of storage time of bonded pairs of B_2H_6 treated hydrophobic silicon wafers;

15 FIG. 4 is a graph depicting bonding energy as a function of annealing temperature of B_2H_6 treated, boron-implanted treated, Ar plasma treated, and conventional hydrophobic (HF dipped only) silicon wafer pairs;

FIG. 5 is a graph depicting bonding energy as a function of annealing time at $250^\circ C$, for B_2H_6 treated wafer pairs;

20 FIG. 6 is a schematic of surface terminations on B_2H_6 plasma treated and HF dipped silicon wafers;

FIG. 7 is a flow chart showing a second embodiment of the method according to the present invention;

FIGS. 8A-8C are sectional diagrams illustrating a second embodiment of the method according to the invention, and a bonded structure according to the invention;

25 FIG. 9 is a graph depicting bonding energy as a function of annealing temperature;

FIG. 10 is an TEM (Transmission Electron Microscopy) image of an As-implanted amorphous-Si/amorphous-Si (a-Si/a-Si) bonding interface;

FIG. 11 is a HRTEM (High Resolution TEM) image of an As-implantation induced amorphous layer in a bonding wafer;

30 FIG. 12 is a HRTEM image for an As-implanted bonded pair after annealing;

FIG. 13 is a graph depicting bonding energy as a function of annealing temperature of B_2H_6 treated InP/InP wafer pairs;

FIG. 14 is a graph depicting bonding energy as a function of annealing temperature of B_2H_6 treated Si/InP wafer pairs;

FIGS. 15A-15C are diagrams of a forming a bonded structure according to the invention; and

FIGS. 16A-16E are diagrams of a forming a bonded structure according to the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to the drawings, wherein like reference numerals designate identical or corresponding parts throughout the several views, and more particularly to FIG. 1 thereof, FIG. 1 shows method steps of the present invention. In step 100, the substrates are cleaned using, for example, a wet RCA-1 ($H_2O+H_2O_2+NH_4OH$) solution. Other cleaning methods are possible, such as $H_2SO_4+H_2O_2$ or dry clean. Following the cleaning step using the RCA-1 solution, the substrates are immersed in step 101 in a hydrofluoric acid aqueous solution such as 1%HF solution to remove the surface thin native oxide layer. Upon removal from the hydrofluoric acid solution, the surfaces of the substrates are modified by creating surface and/or subsurface damage areas by ion implantation or plasma, preferably using boron-containing ions or boron-containing plasma, in step 102. By subsurface, it is meant at least the layer of atoms below the surface layer. The treatment may approach or reach amorphization to form a thin amorphous layer may be formed in the surface of the substrates. The surface treatment, when using boron, may introduce boron into the substrate surface.

Upon termination of the treatment, the substrates in step 103 are immersed in a dilute hydrofluoric acid aqueous solution such as 1%HF solution to remove the surface thin native oxide layer or any other oxide formed on the surface. Surfaces of the substrates which were treated in step 103 are placed together in step 104 at room temperature in atmosphere and form a room temperature bonded substrate pair. The attached substrate pair is preferably placed inside a low vacuum system, but may also be placed in ambient. The bonded pair is then annealed at low temperatures in step 105. The temperature may be selected to recrystallize the thin amorphous layers formed during the ion implantation or plasma

treatment. Recrystallization may also be carried out in a separate annealing procedure. The wafer bonding method of the present invention achieves high bonding energy near room temperature.

FIGS. 2A-2E show sectional views of the first embodiment of the method according to the invention. In FIG. 2A, a substrate 200, after immersing in the aqueous HF solution, is exposed to a plasma 201. FIG. 2B illustrates wafer 200 after the plasma treatment. The plasma modifies the surface 202 of the wafer to create defect areas and possibly a thin amorphous layer. Subsurface (the layer adjacent the surface) defect areas may also be formed. Surface 202 is drawn with a heavier line to illustrate the defective area or amorphous layer formed by the plasma treatment. The amorphous layer formed is about a few nm or more in thickness. In a preferred case, the plasma is a boron-containing plasma and, most preferably, a B_2H_6 plasma. The position of the B in the surface structure will be described below in connection with FIG. 6.

The wafer is immersed in the aqueous HF solution as described above. Another wafer 203 having a similarly plasma treated surface 204 is placed in contact with wafer 200 with surfaces 202 and 204 directly contacted to form the bonded structure at room temperature in FIG. 2C. The bonded structure is annealed at a low temperature and is then ready for further processing, such as low-temperature annealing, substrate lapping, device formation, etc., or a combination of processes. The process may be continued by plasma-treating the exposed surface 205 of wafer 203 (FIG. 2D) and bonding it to another plasma-treated surface 207 of wafer 206 (FIG. 2E). Any number of substrates may be bonded together.

EXAMPLE

75 mm diameter, 1-10 ohm-cm, p-type Si (100) substrate wafers were used. The wafers were cleaned in a RCA-1 solution, dipped in a 1% hydrofluoric aqueous solution followed by treatment in B_2H_6 plasma for an appropriate time period depending on the plasma system used. Appropriate plasma treatment times have ranged from 30 sec. to 5 min. The B_2H_6 plasma treatment consisted of a mixed gas of 20 sccm of 0.5% B_2H_6 /99.5% He and 20 sccm Ar in an inductor coupled plasma (ICP) operating in a reactive ion etch mode with a RF power of 38 W at a pressure of ~5 mTorr. A ~100 V self-biased voltage was generated. This self-bias is the lowest possible self-bias for a stable plasma treatment in the plasma treatment

system used herein. The wafers were then dipped in a diluted 1% HF solution to remove any oxide on the wafer surfaces. The wafers were then placed together without water rinse and bonded in air at room temperature.

The bonded wafer pair was stored in a low vacuum chamber at a vacuum level of about, for example, 700 Pa. The vacuum level is not critical. The bonding energy (specific surface energy) of the bonded pairs was determined by measuring the crack length introduced by inserting a razor blade into the bonding interface to partially separate the two wafers. FIG. 3 shows the room temperature bonding energies as a function of storage time for B_2H_6 plasma-treated hydrophobic bonded silicon wafers. Compared with a typical room temperature bonding energy of $\sim 10\text{--}20\text{ mJ/m}^2$ for conventional HF-dipped silicon wafer pairs, the bonding energy of $\sim 400\text{ mJ/m}^2$ for the B_2H_6 treated pairs is remarkably higher. A few interface bubbles were formed during low vacuum storage at room temperature, which supports the latter explanation that hydrogen released from the bonding interfaces is responsible for the increase of bonding energy at room temperature.

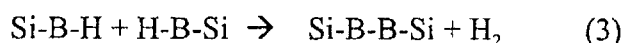
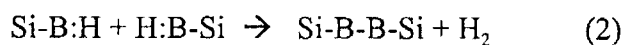
Bonding energy as a function of annealing temperature of B_2H_6 treated, boron-implanted treated, Ar plasma treated, and conventional hydrophobic (HF dipped only) silicon wafer pairs is shown in FIG. 4. It is important to note that for the B_2H_6 plasma treated samples, the bonding energy was $\sim 900\text{ mJ/m}^2$ at 150°C and $\sim 1800\text{ mJ/m}^2$ at 250°C , and reaches the fracture energy of bulk silicon $\sim 2500\text{ mJ/m}^2$ at 350°C . For comparison, FIG. 4 also shows the bonding energy as a function of annealing temperature of conventional HF dipped silicon wafer pairs. TEM (Transmission Electron Microscopy) measurements have shown that the epitaxial bonding interface in the Si/Si bonded pairs was realized after 350°C annealing.

A typical example of bonding energy as a function of annealing time at 250°C is shown in FIG. 5. The bonding energy increases quickly with annealing time and is saturated after $\sim 20\text{ h}$ annealing at 250°C . A few bubbles were generated during annealing indicating that the increase in bonding energy is associated with the release of hydrogen at the bonding interface.

The B_2H_6 plasma treatment of present invention places boron not only on the surface but also in subsurface layers due to the self-bias voltage. After the HF dip, in addition to Si- H_2 , Si-H and Si-F surface terminations, the B_2H_6 plasma-treated silicon surfaces will

likely be terminated by Si-B:H from top surface boron atoms forming Si-B groups, by Si-B-H groups by boron at the first surface layer, and by Si-H and Si-H₂ groups that have subsurface boron atoms terminated to the silicon atoms, see FIG. 6. The bonding interface between the silicon wafer pair is most likely bridged by HF molecules resulting from the HF dip that can be removed by storage in low vacuum or in ambient at room temperature.

Since B-H complexes are very weakly polarized due to their similar electronegativity, the following reactions at the bonding interface are likely responsible for the increase in bonding energy at room temperature:



The removal of hydrogen terminations on the boron atoms leads to a Si-B-B-Si bridging bond attaching one substrate to another. Moreover, as reported by Kim et al. in Applied Physics Letters 69, 3869 (1996), subsurface boron in the second layer weakens the surface Si-H bond. Hydrogen desorption from the bonding surfaces of B₂H₆ treated silicon wafers can take place at low temperatures resulting in a silicon covalent bond formation across the interface between the substrates as shown by the following reaction:



The boron-assisted reaction completely depletes hydrogen from the bonding interface at temperatures of 350-400°C which is lower than a 700°C temperature which is required for conventional HF dipped silicon substrate bonding, when no boron is present.

In a second embodiment, an inert gas plasma is used to create the defective area and thin amorphous layer. The third embodiment preferably uses an Ar-only plasma treatment to enhance the bonding energy at low temperatures, also shown in FIG. 4. Method steps for an Ar-only plasma treatment bonding process follow all the steps shown in FIG. 1. After cleaning in RCA1 solution (step 100), silicon wafers are dipped in 1%HF solution to remove the native oxide layer of any other oxide layer (step 101). The wafers are placed in the RIE plasma system and treated with Ar plasma in 30-100 mtorr for 15 seconds to 20 minutes. Ar plasma is generated by applying a RF power from 80-200 W at 13.56 MHz (step 102). The surface self-bias voltage is in the range of 200 V to 400 V. These Ar plasma treated wafers are dipped in 1%HF to remove any surface oxide layer (step 103) and bonded at room

temperature in air (step 104). After storage in low vacuum for ~20 hrs (step 105), the bonded pairs are annealed. The bonding energy reaches the bulk silicon fracture energy (2500 mJ/m²) at 400°C. The bonding energy enhancement is likely due to that the amorphous layer formed by the Ar plasma treatment readily absorbs the hydrogen released from surface Si-H₂ and Si-H groups that takes place at about 300°C. The amorphous layer at the bonding interface may be recrystallized at low temperatures. Ar-only plasma treatment to enhance low temperature epitaxial-like bonding is especially attractive for applications that requires no monolayers of boron at the bonding interface.

A third embodiment of the present invention (shown in FIG. 7) is to use ion implantation to place boron onto the surfaces of bonding substrates. In step 700, the substrates are covered by a masking layer, preferably an oxide layer. The substrates are cleaned using, for example, a wet RCA-1 solution and dried. in step 701. Surfaces of the substrates are implanted with boron using BF₃ as shown in step 702 to place the boron concentration peak at the oxide/silicon interface. As an example, forming an 800 Å thick thermal oxide on silicon wafers, boron implantation at an energy of 20 keV with a dose of 5x10¹⁴/cm² places boron concentration peak of 6x10¹⁹/cm² at the oxide/silicon interface. Employing a 6700 Å thick thermal oxide on silicon wafers, boron implantation at an energy of 180 keV with a dose of 5x10¹⁴/cm² places boron concentration peak of 2.5x10¹⁹/cm² at the oxide/silicon interface.

Following boron implantation, the substrates in step 703 are immersed in a dilute hydrofluoric acid solution to remove the oxide layer. Surfaces of the substrates which were boron-implanted in step 702 are bonded at room temperature in step 704. The attached pair is preferably placed inside a low vacuum system and annealed in air at low temperature in step 705.

Boron implantation in bonding silicon wafers can achieve the bulk silicon fracture energy at ~400°C. The bonding energy enhancement at room temperature seen with the boron plasma treated wafers is not achieved. Instead, a significant increase in bonding energy is seen at temperatures above than 300°C, as shown in FIG. 4. It is likely that lower boron concentrations on the wafer surfaces for the boron implantation treatment in comparison to the plasma treatment case delays bonding enhancement until higher annealing temperatures are used.

Released hydrogen shown in equation (4) can build an internal pressure that offsets the bonding strength at the bonding interface. In order to alleviate the internal gas pressure, released hydrogen molecules need to be removed from the interface. The plasma or ion implantation treatment according to the invention induces a defective surface layer towards amorphization providing hydrogen trapping sites. Plasma or ion implantation treatments using other gases containing boron are expected to work as well.

FIGS. 8A-8C show cross sectional views of the third embodiment of the method. Ions 801 are implanted into a wafer 800 having a masking film 805, such as SiO_2 , formed on the surface, as shown in step 8A. The masking film 805 allows the energy of the implant to be adjusted so that the peak of the concentration distribution is at the surface of wafer 800. As shown in FIG. 8B, the wafer 800 has a modified surface 802 (shown with heavier line for illustrative purpose only) after removing the masking layer by immersing in an aqueous HF solution, in the case of layer 305 being SiO_2 . Another wafer 803 similarly treated with a modified surface 804 is placed in contact with wafer 800 at room temperature. The bonding of the two wafers is allowed to enhance with low-temperature annealing, as discussed above.

A fourth embodiment of the present invention is to use As (arsenic) ion implantation to silicon wafers to form an amorphous layer on the wafer surface. Method steps for an As ion implantation treatment bonding process follow the steps shown in FIG. 1. After cleaning and removing any oxide layer, As ion implantation is performed at an energy of 180 keV with a dose of $9 \times 10^{14}/\text{cm}^2$. The As doping concentration peak of $8 \times 10^{19}/\text{cm}^3$ is located at $\sim 1150 \text{ \AA}$ from the silicon surface. Although this implantation induced a very low As doping on the wafer surface, an amorphous layer with 1650 \AA thick was formed as confirmed both by a Monte Carlo simulation and TEM measurement (FIG. 10). The thickness of the amorphous layer can vary and is not limited to the value of this example. For instance, other ions may be implanted to create the amorphous layer. Arsenic is a dopant, and there are applications when it is desired not to dope the substrate so another ion, such as a non-doping ion like Ar, would be chosen.

After an HF dip to remove any oxide on the implanted surfaces, the wafers are bonded at room temperature in ambient conditions. After storage in low vacuum for $\sim 20 \text{ h}$ the bonded pairs are annealed in air. The bonding energy as a function of annealing temperature is shown in Fig. 9. The bonding energy reaches the bulk silicon fracture energy (2500 mJ/m^2) at 400°C .

Bonded pairs of the As implanted silicon wafers that were annealed at 900°C to fully recrystallize the amorphous layers before bonding have shown the same bonding energy of ~400 mJ/m² as the conventional HF dipped Si/Si pairs after 400°C annealing. It is clear that as in the Ar plasma treatment case, the amorphous layers rather than As doping at the bonding interface play a key role in enhancing bonding energy at low temperatures.

FIGS. 10-12 show TEM images of the As-implanted substrates, and As-implanted bonded substrate pairs. In FIG. 10, a TEM image of bonding interface between the amorphous silicon layers (a-Si/a-Si) that were formed by As implantation is shown. FIG. 11 shows an HRTEM image of the interface between the amorphous silicon and the crystal silicon substrate (a-Si/c-Si). The amorphous layer is reduced to 100 Å in thickness after annealing for 24 hours at 450°C, as shown in FIG. 12.

The above methods can be applied to other substrate combinations involving materials such as InP, GaAs, Ge, SiC, etc. Using the B₂H₆ plasma treatment process described in the first embodiment to InP/InP epitaxial-like wafer bonding, the bonding energy of the bonded InP/InP pairs reached the (100) InP bulk fracture energy of ~ 600 mJ/m² after annealing at 200°C for 24 h. FIG. 13 shows the bonding energy as a function of annealing temperature of the B₂H₆ treated InP/InP wafer pairs. For comparison, the bonding energy as a function of annealing temperature of conventional HF dipped InP/InP pairs is also shown.

The similar results were obtained for bonding a silicon wafer to an InP wafer. Using the B₂H₆ plasma treatment process described in the first embodiment to Si/InP epitaxial-like wafer bonding, the bonding energy of the bonded Si/InP pairs reached the (100) InP bulk fracture energy of ~ 600 mJ/m² after annealing at 200°C for 24 h. FIG. 14 shows the bonding energy as a function of annealing temperature of the B₂H₆ treated Si/InP wafer pairs. For comparison, the bonding energy as a function of annealing temperature of conventional HF dipped Si/InP pairs is also shown

Two or more wafers having a silicon layer formed on the surface may also be bonded, as shown in FIGS. 15A - 15C. Silicon layer 1502 of substrate 1500 is exposed to plasma 1503 in FIG. 15A. A similarly treated surface 1505 of wafer 1504 is placed in contact with surface 1502 and bonded (FIG. 15B). Surface 1505 may also be ion-implanted. The exposed surface of substrate 1504 may also be exposed to a plasma and bonded with treated surface 1507 of wafer 1506 to form a three-substrate bonded structure, as shown in FIG. 15C. These

wafers may be processed wafers having devices and/or circuits formed therein with the silicon layer formed after device and/or circuit formation. The silicon layer should be planar, and may be planarized using techniques such as CMP. The silicon layer is treated using a plasma or ion-implantation, as discussed above. This structure preferably used the boron-containing plasma or boron implantation. Also, unique device structures such as double-sided power diodes, pin photodiodes and avalanche photodiodes may be realized. While the above embodiments are directed to substrates, it should be understood that a substrate may be of varying thickness. In other words, thin substrates may be bonded to other substrates, or bonded with two substrates to be between the substrates. A bonded substrate may also be thinned to a desired thickness by lapping or polishing, as discussed above. FIGS. 16A-16E illustrate this. The surface of substrate 1600 is exposed to plasma 1601 to form treated surface 1602 (FIGS. 16A and 16B). Surface 1602 has a surface defect region and may be amorphized. Another substrate 1603 with a treated surface 1604 is bonded to surface 1602 (FIG. 16B). In FIG. 16C, a portion of substrate 1603 is removed by lapping, polishing, etc. to leave portion 1605 with surface 1606. Surface 1606 may then be exposed to a plasma (FIG. 16D) and another wafer 1607 with treated surface 1608 may be bonded to surface 1606 (FIG. 16E). Unique structures where different materials of desired thicknesses may be bonded and formed according to the invention.

Some advantages of the wafer-bonding process of the present invention are that the process utilizes manufacturable steps which bond wafers at room temperature in ambient air and annealed at temperatures no higher than 450°C to reach an epitaxial-like bond. Pre-annealing at elevated temperatures, external pressure, or high vacuum to achieve a high bonding energy are not required. The process uses common RIE plasma treatments or ion implantation that are economic, convenient and easy to implement.

In addition to the epitaxial-like wafer bonding for materials combination for preparing advanced devices such as pin and avalanche photodiodes, the process shown here can have applications in bonding unique device structures such as bonding back sides of two fully processed power devices to form double-sided power devices, can allow the device layer transfer onto carrier substrates with an epitaxial-like interface, and can be used to transfer device layers to more thermally conductive materials thus enhancing thermal management.

Numerous other modifications and variations of the present invention are possible in light of the above teachings. It is therefore to be understood that within the scope of the appended claims, the present invention may be practiced otherwise than as specifically described herein.

WHAT IS CLAIMED AS NEW AND DESIRED TO BE SECURED BY LETTERS
PATENTS OF THE UNITED STATES IS:

1. A method for bonding first and second substrates, comprising:
5 preparing substantially oxide-free first and second surfaces of respective first and second substrates;
creating a surface defect region in each of said first and second surfaces; and
bonding said first and second surfaces.
- 10 2. A method as recited in claim 1, wherein said creating step comprises:
forming an amorphous layer about a few nm or more in thickness in each of said first and second surfaces.
3. A method as recited in claim 2, comprising:
forming said amorphous layer using one of ion implantation and plasma treatment.
- 15 4. A method as recited in claim 3, comprising:
forming said amorphous layer using As implantation.
5. A method as recited in claim 2, comprising:
forming said amorphous layer using a boron-containing plasma.
- 20 6. A method as recited in claim 5, comprising:
forming said amorphous layer using a B_2H_6 plasma.
7. A method as recited in claim 2, comprising:
forming said amorphous layer using an inert gas plasma.
8. A method as recited in claim 7, comprising:
forming said amorphous layer using an Ar plasma.
- 25 9. A method as recited in claim 2, comprising:
annealing said bonded first and second surfaces at a temperature in the range of about 250-450°C.
10. A method as recited in claim 9, comprising:
recrystallizing a substantial portion of said amorphous layers in said first and second surfaces.
- 30 11. A method as recited in claim 2, comprising:

annealing said bonded first and second surfaces at a temperature not exceeding about 350°C.

12. A method as recited in claim 1, wherein said creating step comprises: plasma treating said first and second surfaces using a boron-containing plasma.

13. A method as recited in claim 12, comprising: forming monolayers of boron on said first and second surfaces.

14. A method as recited in claim 12, comprising: doping said first and second surfaces with boron.

15. A method as recited in claim 1, comprising: bonding said first and second surfaces at room temperature.

16. A method as recited in claim 15, comprising: annealing said bonded first and second surfaces at a temperature in the range of about 250-450°C.

17. A method as recited in claim 1, comprising: forming said defect region using one of ion implantation and plasma treatment.

18. A method as recited in claim 1, comprising: forming said defect region using As implantation.

19. A method as recited in claim 1, comprising: forming said defect region using a boron-containing plasma.

20. A method as recited in claim 19, comprising: forming said defect region using a B₂H₆ plasma.

21. A method as recited in claim 1, comprising: forming said defect region using an inert gas plasma.

22. A method as recited in claim 21, comprising: forming said defect region using an Ar plasma.

23. A method as recited in claim 1, comprising: preparing substantially oxide-free first and second surfaces of respective first and second substrates made of one of Si, InP, SiC, Ge and GaAs.

24. A method as recited in claim 1, comprising: preparing a substantially oxide-free silicon substrate having said first surface; and

preparing a substantially oxide-free substrate made of one of InP, SiC, Ge and GaAs having said second surface.

25. A method as recited in claim 1, comprising:

forming a layer of a desired thickness said first surface;

5 ion implanting said first surface through said layer to create said surface defect region in said first substrate; and

creating said surface defect region in said second substrate using one of ion implantation and plasma treatment.

26. A method as recited in claim 1, comprising:

10 creating said surface defect region in said first substrate using plasma treatment; and creating said surface defect region in said second substrate using one of ion implantation and plasma treatment.

27. A method as recited in claim 1, comprising:

15 forming a silicon layer on a substrate containing a first active device as said first substrate; and

forming a silicon layer on a substrate containing a second active device as said second substrate.

28. A method as recited in claim 1, comprising:

20 immersing said first and second substrates in a first oxide etching solution before said creating step; and

immersing said first and second substrates in a second oxide etching solution after said creating step.

29. A method as recited in claim 28, comprising:

25 cleaning said first and second substrates before immersing said substrates in said first oxide etching solution.

30. A method as recited in claim 29, wherein said cleaning step comprises cleaning said first and second substrates in an RCA-1 solution.

31. A method as recited in claim 1, comprising:

30 forming at least one of boron-boron and Si covalent bonds between said first and second substrates.

32. A method as recited in claim 1, further comprising:

placing the bonded pair of substrates under vacuum.

33. A method as recited in claim 1, wherein said first and second substrates are selected from Si, InGaAs, InP, GaAs, Ge and SiC.

34. A method as recited in claim 1, comprising:

5 creating a surface defect region in an exposed surface of said bonded pair of substrates and in a third surface of a third wafer; and

bonding said third surface to said exposed surface.

35. A method as recited in claim 1, comprising:

maintaining said bonded pair at room temperature; and

10 obtaining a bond strength of at least about 400 mJ/m².

36. A method as recited in claim 1, comprising:

maintaining said bonded pair at a temperature no more than about 400°C; and

obtaining a bond strength of at least about 1500 mJ/m².

37. A method as recited in claim 36, comprising:

15 obtaining a bond strength of at least about 2500 mJ/m².

38. A method for bonding first and second substrates, comprising:

forming a surface layer on respective first and second surfaces each of said first and second substrates;

20 ion implanting an impurity into said first and second substrates with a peak concentration of said impurity located at approximately respective interfaces between said first and second surfaces and said surface layer;

removing said surface layer from each of said first and second substrates; and bonding said first and second surfaces.

39. A method as recited in claim 38, wherein said ion implanting step comprises:

25 forming a thin amorphous layer in each of said first and second surfaces.

40. A method as recited in claim 38, comprising:

forming said amorphous layer using B implantation.

41. A method as recited in claim 38, comprising:

annealing said bonded first and second surfaces at a temperature in the range of about 30 250-450°C.

42. A method as recited in claim 38, comprising:

recrystallizing a substantial portion of said amorphous layers in said first and second surfaces.

43. A method as recited in claim 38, comprising:
forming a surface defect region in each of said first and second surfaces.

5 *sub 4* 44. A bonded structure, comprising:
a first substrate having a first surface, a first amorphous layer formed in said first surface; and
a second substrate having a second surface, a second amorphous layer formed in said second surface;
10 said first surface being bonded to said second surface to form a bonded pair of substrates.

45. A structure as recited in claim 44, comprising:
one of said first and second substrates of said bonded pair having a third surface, said third surface having an amorphous layer;
15 a third substrate having a fourth surface, a fourth amorphous layer formed in said fourth surface; and
said third surface bonded to said fourth surface.

20 *3* 46. A structure as recited in claim 44, wherein said first and second substrates are selected from Si, InGaAs, InP, GaAs, Ge and SiC.

25 *4* 47. A structure as recited in claim 44, wherein:
said first and second substrates each comprises a silicon substrate; and
said first and second surfaces each comprises a silicon surface.

25 *sub 5* 48. A structure as recited in claim 44, wherein:
said first and second substrates comprise respective first and second semiconductor devices;
said first surface comprises a substantially planar surface of a first silicon layer formed on said first device; and
said second surface comprises a substantially planar surface of a second silicon layer formed on said second device.

30 *6* 49. A structure as recited in claim 44, wherein:

said first surface comprises a first silicon surface exposed to a boron-containing plasma; and

said second surface comprises a second silicon surface exposed to a boron-containing plasma.

5

50. A structure as recited in claim 44, wherein:

said first surface comprises a first silicon surface exposed to an inert gas plasma; and

said second surface comprises a second silicon surface exposed to an inert gas plasma.

7.

51. A structure as recited in claim 44, wherein:

said first surface comprises a first silicon surface implanted with boron; and

10

said second surface comprises a second silicon surface implanted with boron.

8.

52. A structure as recited in claim 44, wherein:

said first surface comprises a first silicon surface implanted with arsenic; and

said second surface comprises a second silicon surface implanted with arsenic.

9.

53. A structure as recited in claim 44, comprising:

15

at least one of boron-boron and Si covalent bonds formed between said first and

second substrates.

20
210667

54. A bonded structure, comprising:

a first substrate having an amorphized first surface and containing boron;

a second substrate having an amorphized second surface and containing boron; and

said first surface being bonded to said second surface to form a bonded pair of

substrates.

16.

55. A structure as recited in claim 54, wherein said first and second substrates are

selected from Si, InGaAs, InP, GaAs, Ge, SiC

17.

56. A structure as recited in claim 54, wherein:

25

said first surface comprises a first silicon surface exposed to a boron-containing

plasma; and

said second surface comprises a second silicon surface exposed to a boron-containing

plasma.

18.

57. A structure as recited in claim 54, wherein:

30

said first surface comprises a first silicon surface implanted with boron; and

said second surface comprises a second silicon surface implanted with boron.

ABSTRACT OF THE DISCLOSURE

A process for bonding oxide-free silicon substrate pairs and other substrates at low temperature. This process involves modifying the surface of the silicon wafers to create defect regions, for example by plasma-treating the surface to be bonded with a or boron-containing plasmas such as a B_2H_6 plasma. The surface defect regions may also be created by ion implantation, preferably using boron. The surfaces may also be amorphized. The treated surfaces are placed together, thus forming an attached pair at room temperature in ambient air. The bonding energy reaches approximately 400 mJ/m^2 at room temperature, 900 mJ/m^2 at 150°C , and 1800 mJ/m^2 at 250°C . The bulk silicon fracture energy of 2500 mJ/m^2 was achieved after annealing at $350\text{-}400^\circ\text{C}$. The release of hydrogen from B-H complexes and the subsequent absorption of the hydrogen by the plasma induced modified layers on the bonding surfaces at low temperature is most likely responsible for the enhanced bonding energy.

BEST COPY

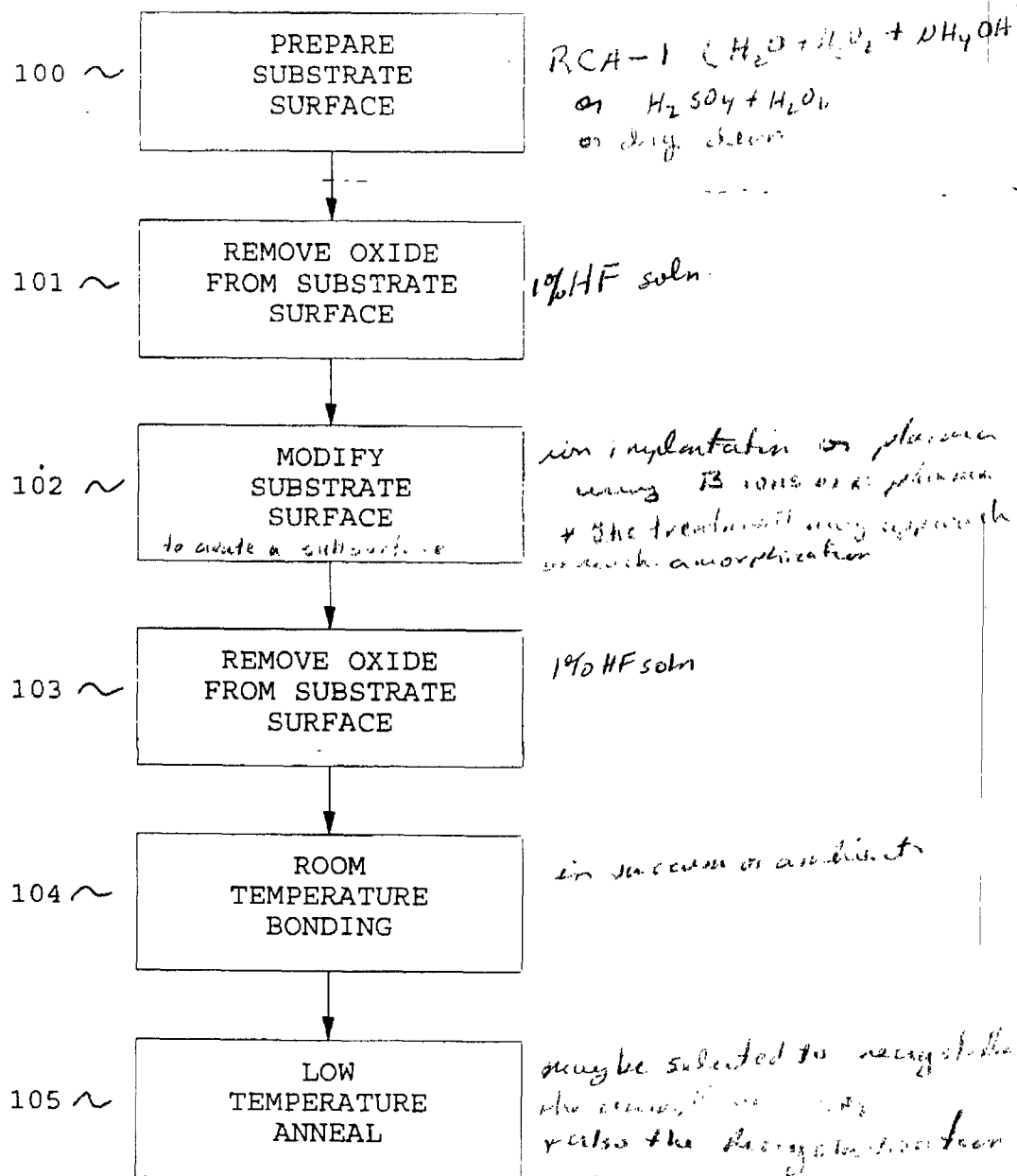


FIGURE 1

Conventional \Rightarrow epitaxial bonding

Page 2 \Rightarrow Smart-cut method \Rightarrow H atoms are implanted into a Si wafer
to break Si-Si bonds



annealing to release H atoms from Si and make Si-Si bond
at Temp $\uparrow 700^\circ C$

Problem: develop a low temp. smart-cut-like wafer bonding technique
($< 500^\circ C$)

PLASMA

to create defect
area and possible
amorphous. 200 ~

202 defective area or consumption tags

FIGURE 2A

"a few mm on
scale in thickness
112 ★

FIGURE 2B

200 ~

203 ~

204-

200 —

202 .

FIGURE 2C

201—

PLASMA

203 へ

204.

200 —

202

FIGURE 2D

205 ✓

206

203 ✓

204

200 ✓

FIGURE 2E

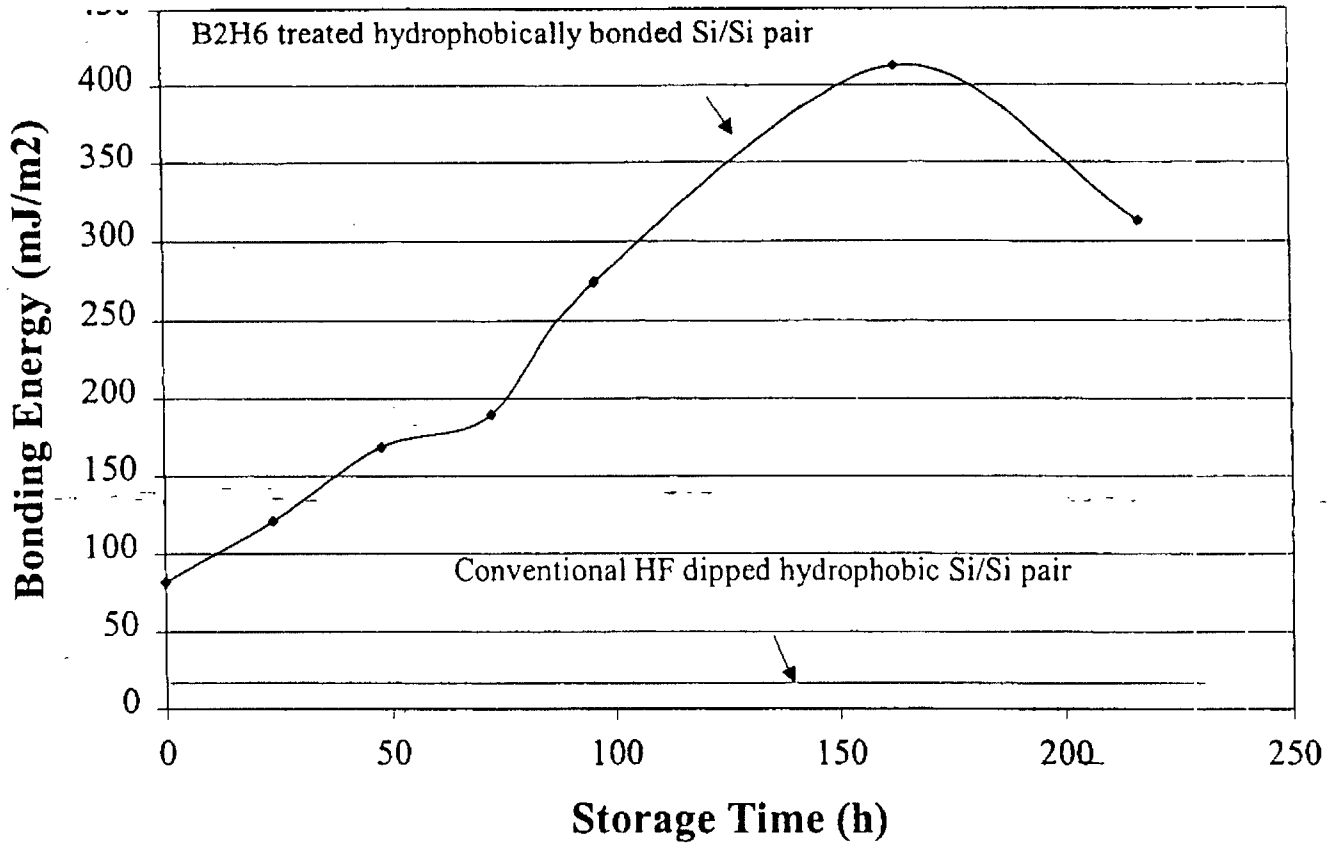


FIG. 3

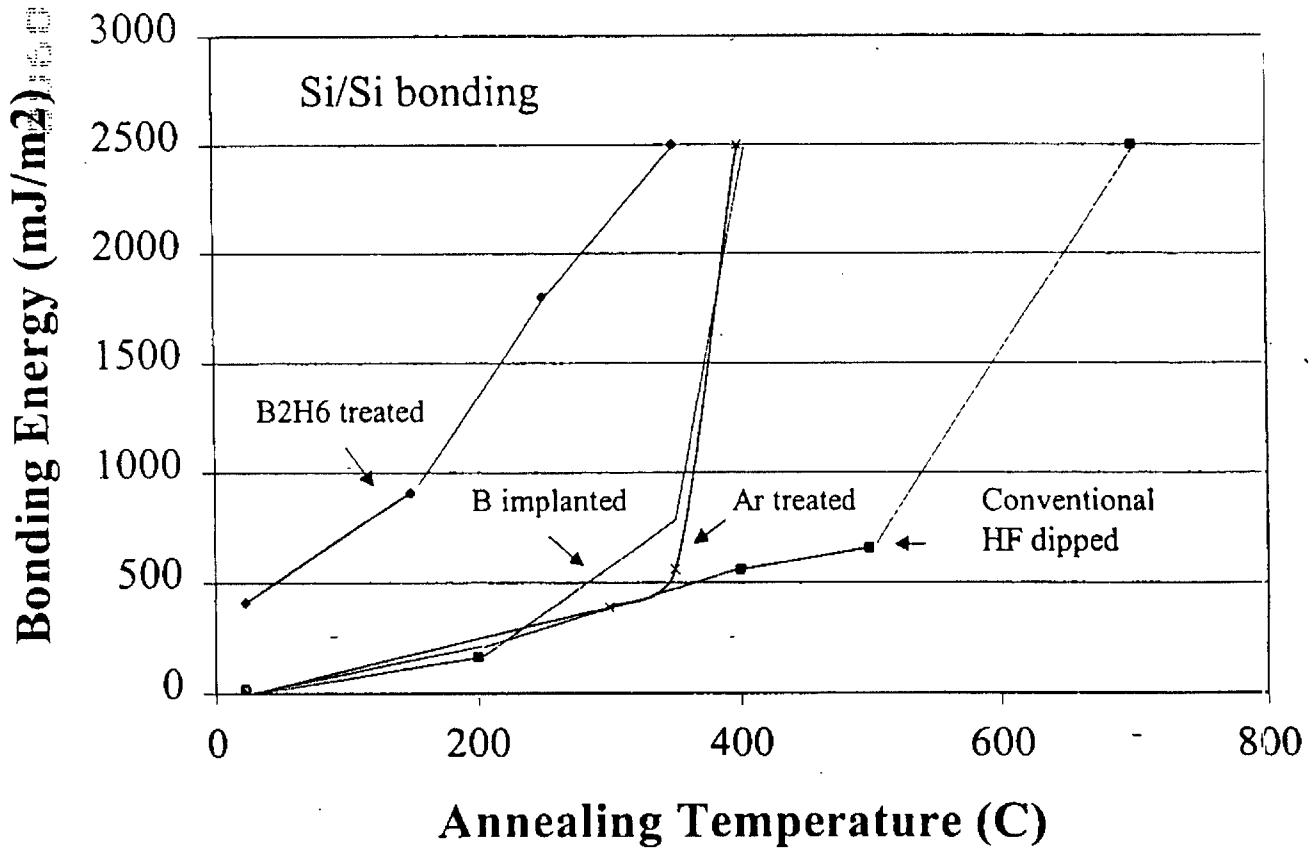


FIG. 4

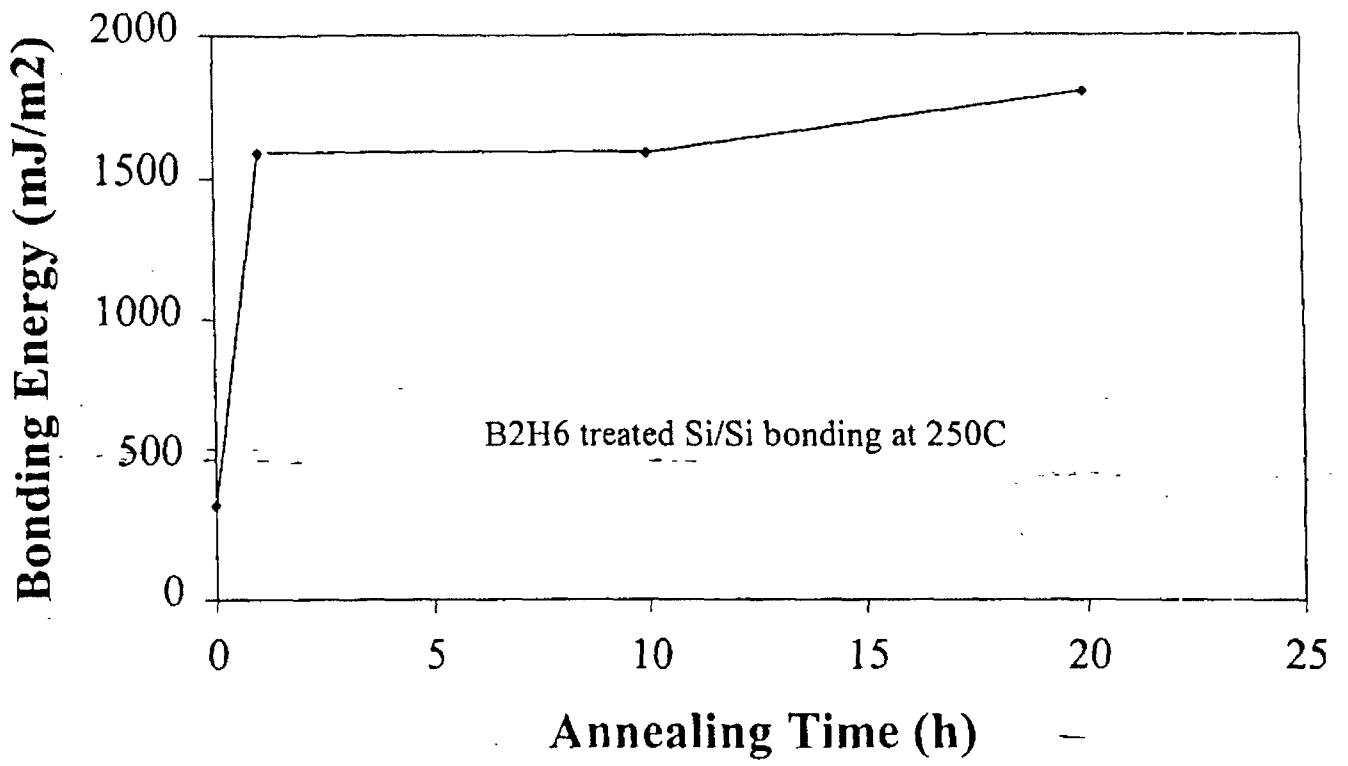


FIG. 5

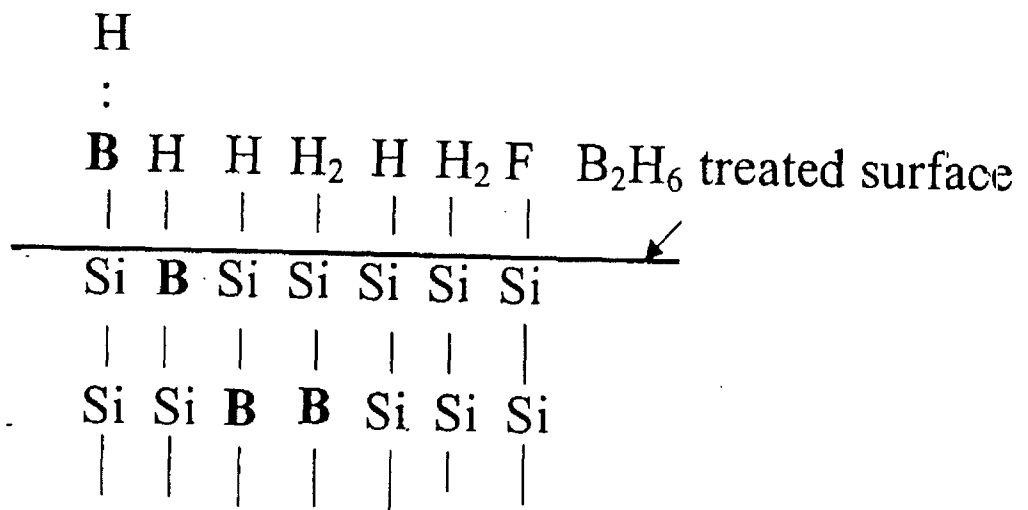


FIG. 6

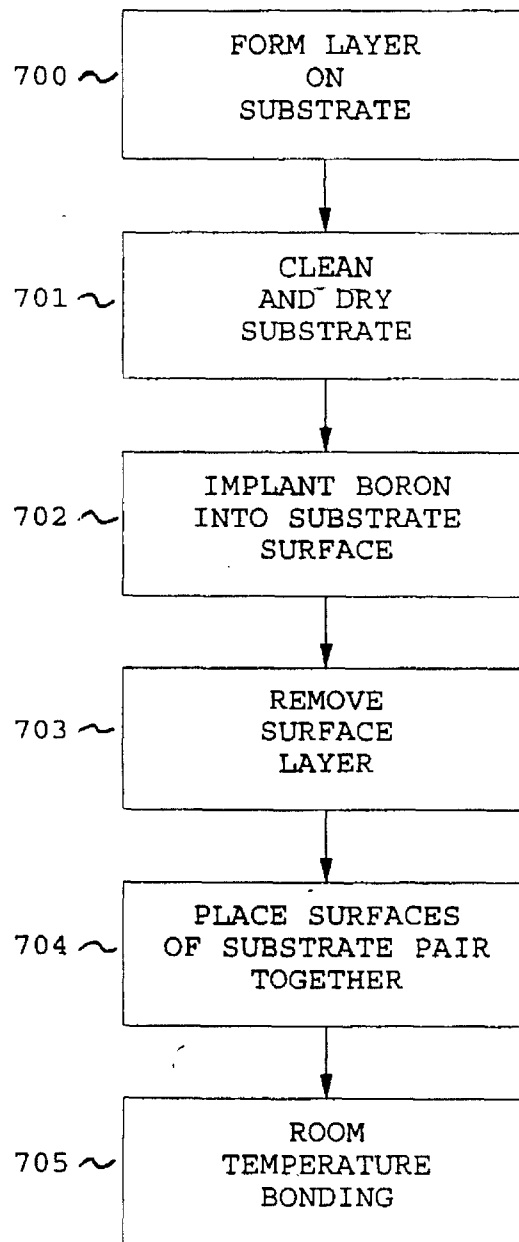


FIGURE 7

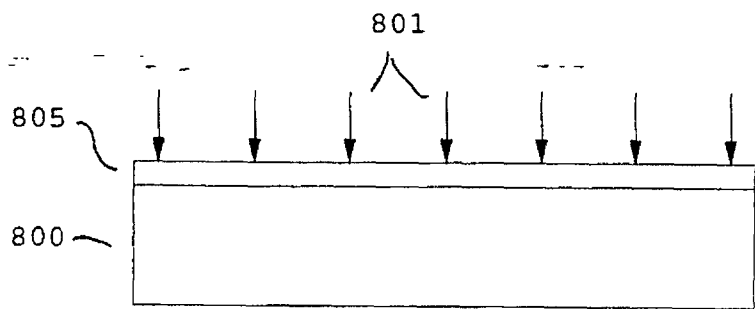


FIGURE 8A

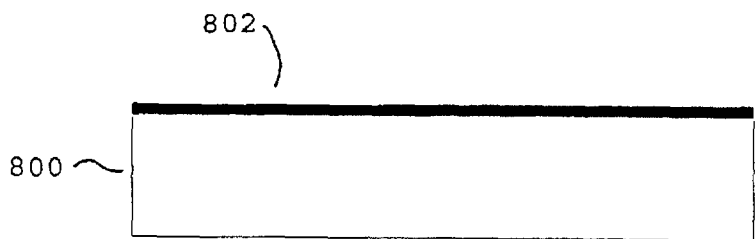


FIGURE 8B

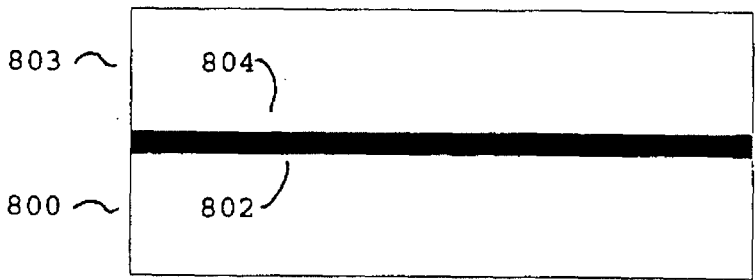


FIGURE 8C

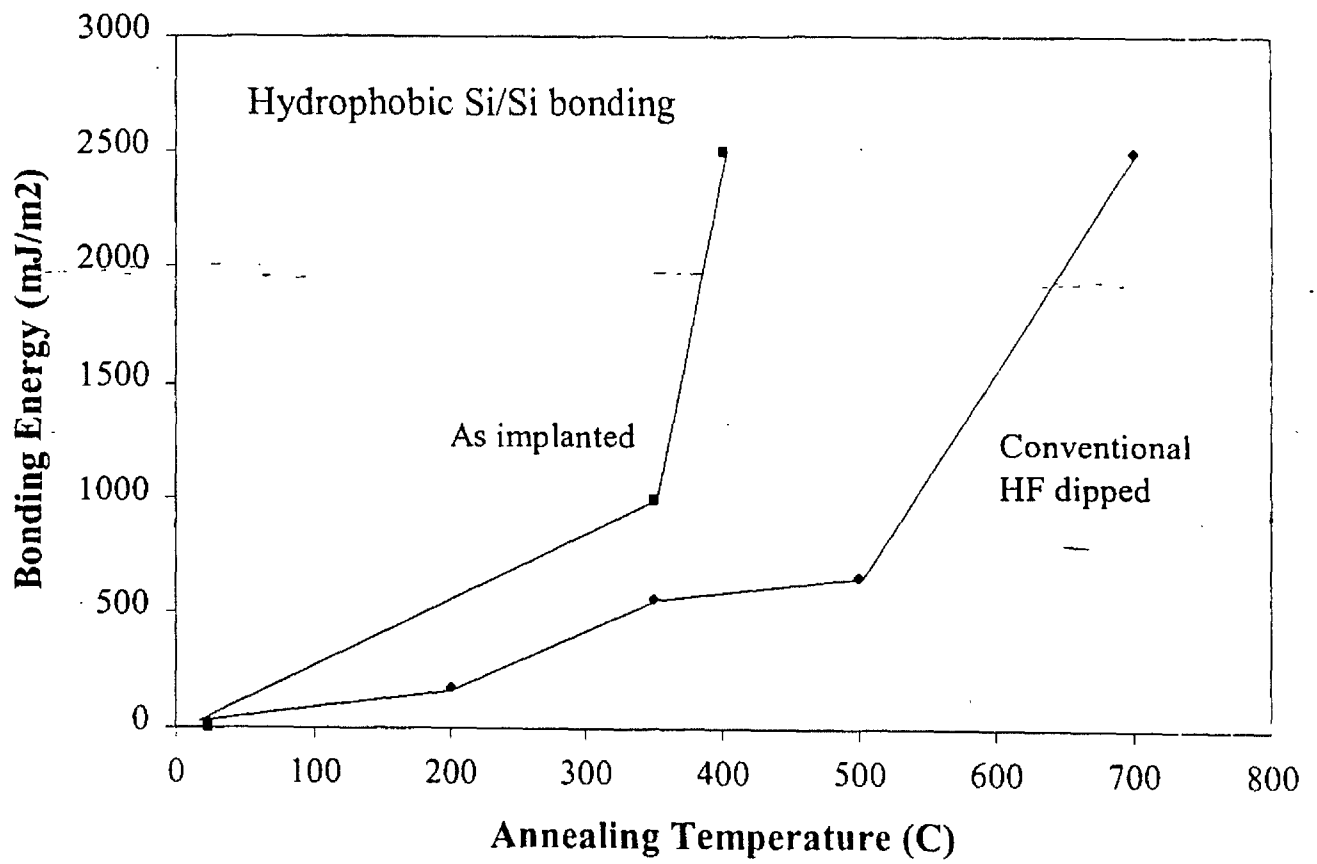


FIG. 9

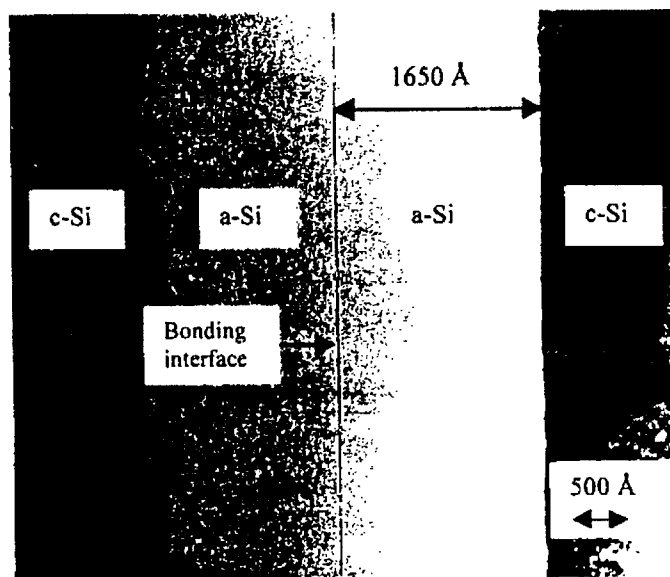


FIG. 10

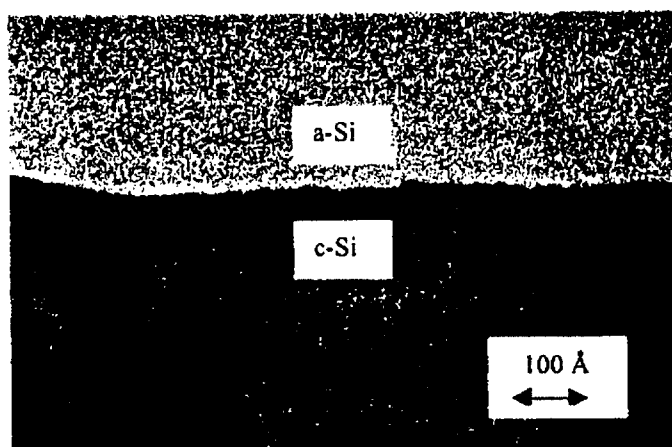


FIG. 11

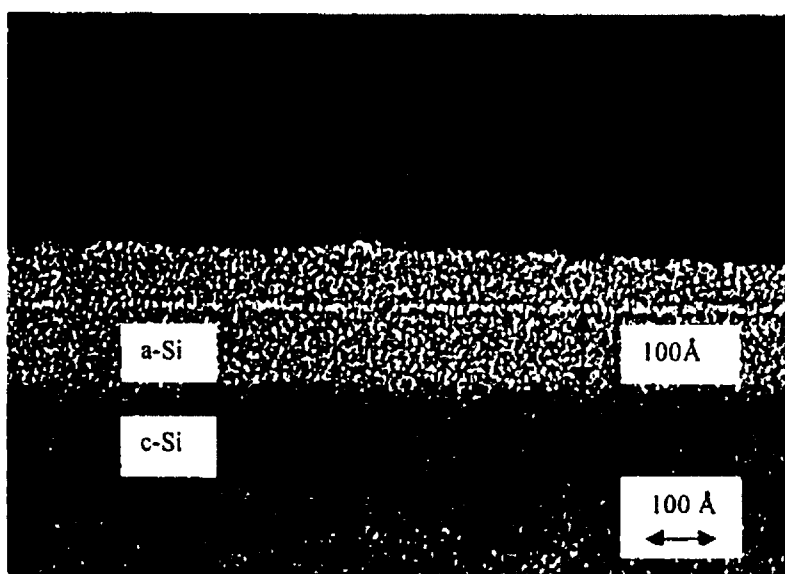


FIG. 12

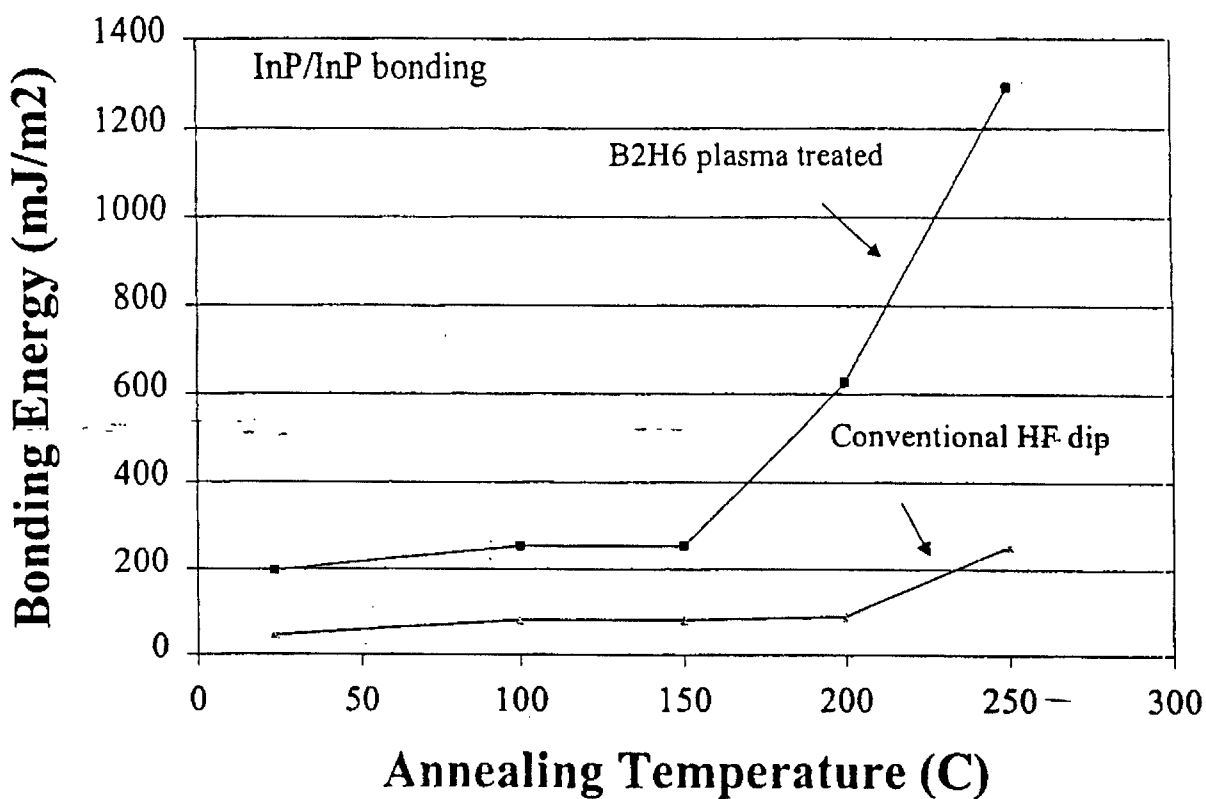


FIG. 13

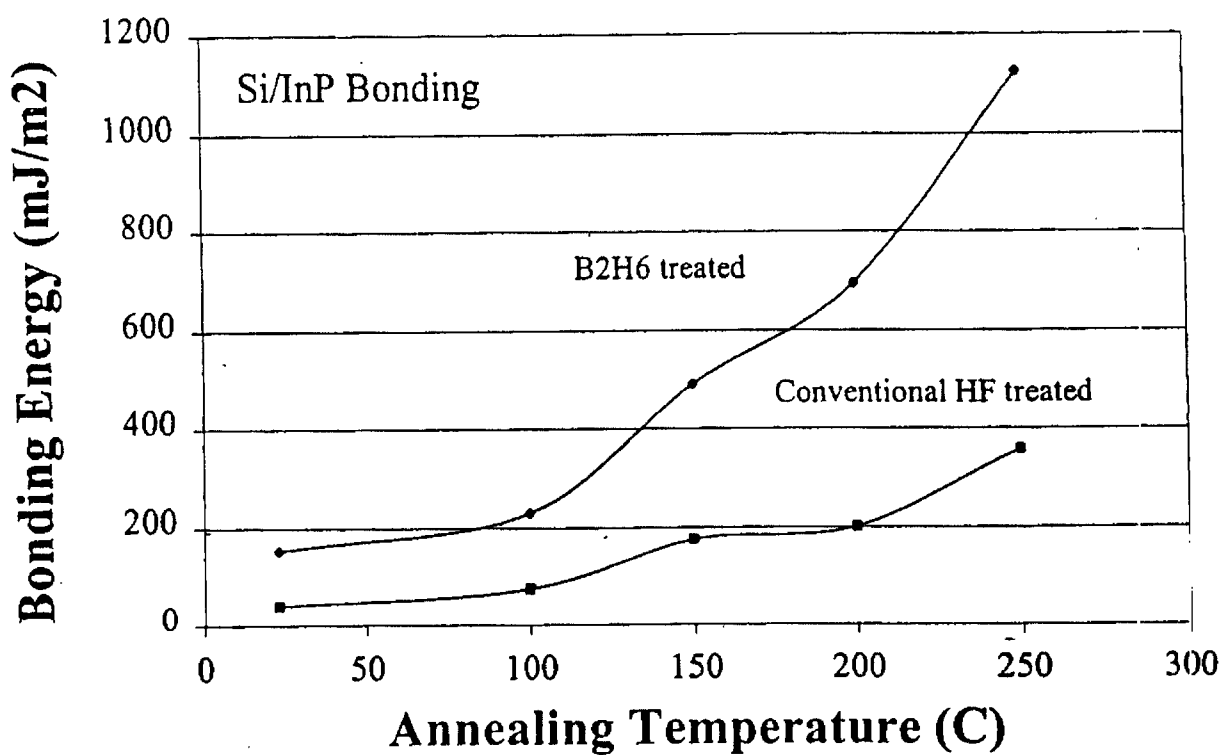


FIG. 14

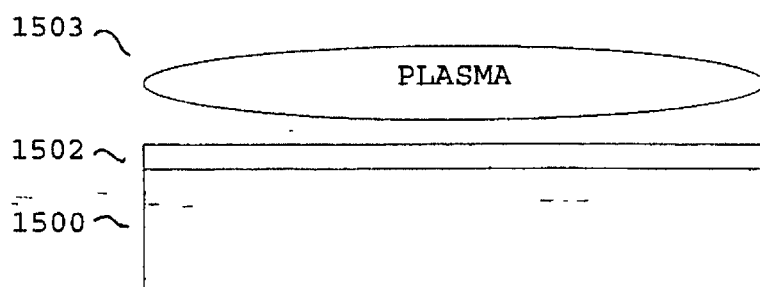


FIGURE 15A

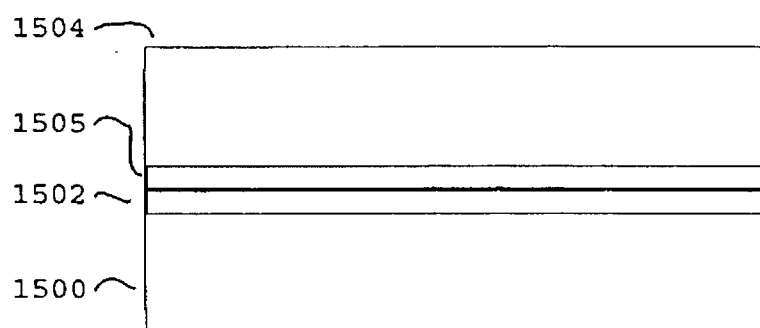


FIGURE 15B

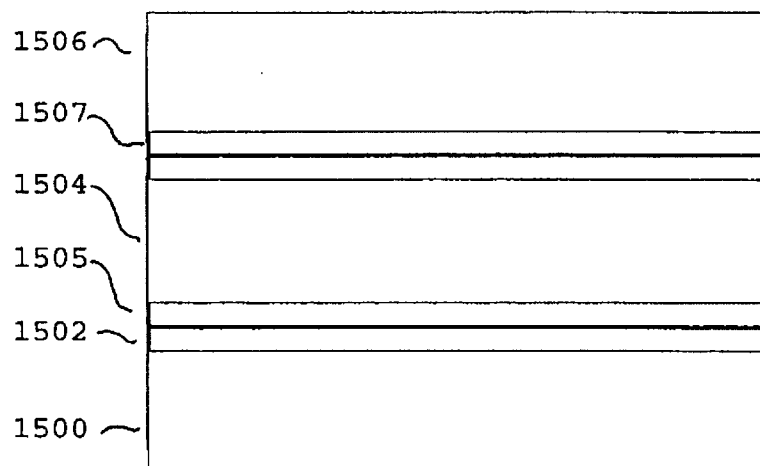


FIGURE 15C

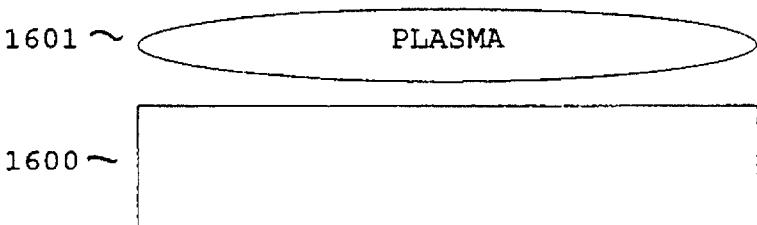


FIGURE 16A

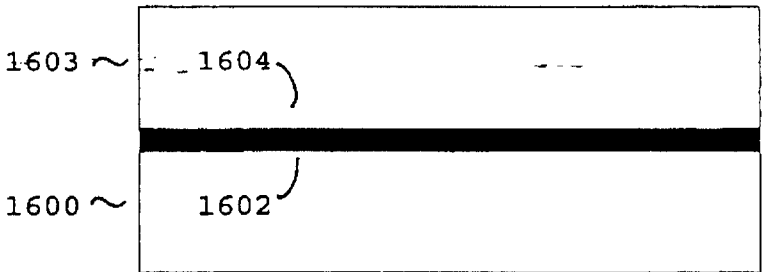


FIGURE 16B

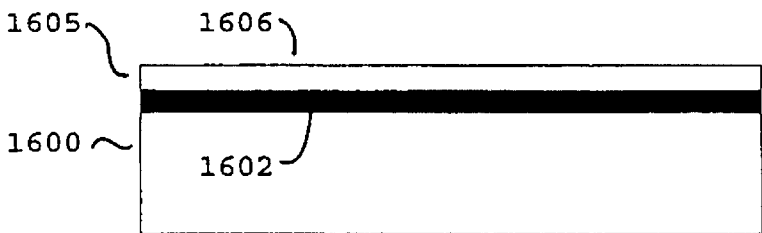


FIGURE 16C

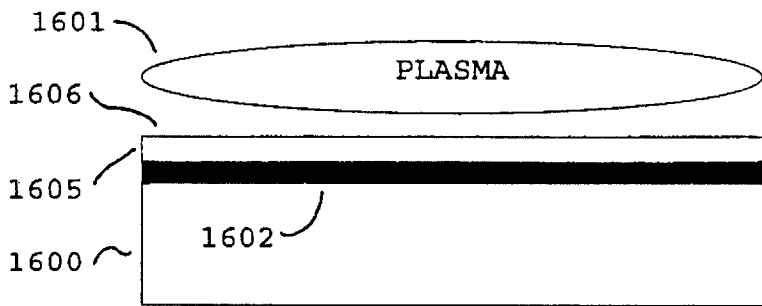


FIGURE 16D

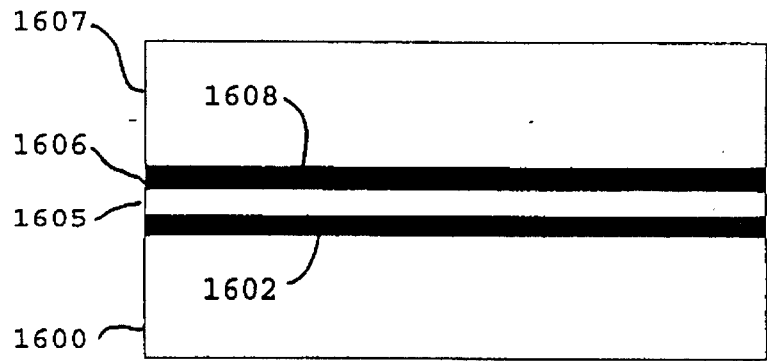


FIGURE 16E

Declaration, Power Of Attorney and Petition

Page 1 of X 2

WE (I) the undersigned inventor(s), hereby declare(s) that:

My residence, post office address and citizenship are as stated below next to my name,

We (I) believe that we are (I am) the original, first, and joint (sole) inventor(s) of the subject matter which is claimed and for which a patent is sought on the invention entitled

"A METHOD OF EPITAXIAL-LIKE WAFER BONDING AT LOW TEMPERATURE AND BONDED STRUCTURE"

the specification of which

- ☒ is attached hereto.
- ☐ was filed on _____ as
Application Serial No. _____
and amended on _____.
- ☐ was filed as PCT international application
Number _____
on _____,
and was amended under PCT Article 19
on _____ (if applicable).

We (I) hereby state that we (I) have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

We (I) acknowledge the duty to disclose information known to be material to the patentability of this application as defined in Section 1.56 of Title 37 Code of Federal Regulations.

We (I) hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed. Prior Foreign Application(s)

Application No.	Country	Day/Month/Year	Priority Claimed	
_____	_____	_____	<input type="checkbox"/> Yes	<input type="checkbox"/> No
_____	_____	_____	<input type="checkbox"/> Yes	<input type="checkbox"/> No
_____	_____	_____	<input type="checkbox"/> Yes	<input type="checkbox"/> No
_____	_____	_____	<input type="checkbox"/> Yes	<input type="checkbox"/> No

Attorney Docket No.: 20 180-20

Page 2 of 2
Declaration

We (I) hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below.

_____ (Application Number)	_____ (Filing Date)
_____ (Application Number)	_____ (Filing Date)

We (I) hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application.

Application Serial No.	Filing Date	Status (pending, patented, abandoned)
_____	_____	_____
_____	_____	_____
_____	_____	_____

And we (I) hereby appoint: Norman F. Oblon, Reg. No. 24,618; Marvin J. Spivak, Reg. No. 24,913; C. Irvin McClelland, Reg. No. 21,124; Gregory J. Maier, Reg. No. 25,599; Arthur L. Neustadt, Reg. No. 24,854; Richard D. Kelly, Reg. No. 27,757; James D. Hamilton, Reg. No. 28,421; Eckhard H. Kuesters, Reg. No. 28,870; Robert T. Pous, Reg. No. 29,099; Charles L. Gholz, Reg. No. 26,395; William E. Beaumont, Reg. No. 30,996; Jean-Paul Lavalleye, Reg. No. 31,451; Stephen G. Baxter, Reg. No. 32,884; Richard L. Treanor, Reg. No. 36,379; Steven P. Weihrouch, Reg. No. 32,829; John T. Goolkasian, Reg. No. 26,142; Richard L. Chinn, Reg. No. 34,305; Steven E. Lipman, Reg. No. 30,011; Carl E. Schlier, Reg. No. 34,426; James J. Kulbaski, Reg. No. 34,648; Richard A. Neifeld, Reg. No. 35,299; J. Derek Mason, Reg. No. 35,270; Surinder Sachar, Reg. No. 34,423; Christina M. Gadiano, Reg. No. 37,628; Jeffrey B. McIntyre, Reg. No. 36,867; William T. Enos, Reg. No. 33,128; Michael E. McCabe, Jr., Reg. No. 37,182; Bradley D. Lytle, Reg. No. 40,073; and Michael R. Casey, Reg. No. 40,294; our (my) attorneys, with full powers of substitution and revocation, to prosecute this application and to transact all business in the Patent Office connected therewith; and we (I) hereby request that all correspondence regarding this application be sent to the firm of OBLON, SPIVAK, McCLELLAND, MAIER & NEUSTADT, P.C., whose Post Office Address is: Fourth Floor, 1755 Jefferson Davis Highway, Arlington, Virginia 22202.

We (I) declare that all statements made herein of our (my) own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Qin-Yi TONG
NAME OF FIRST SOLE INVENTOR

Signature of Inventor

Date

Residence: 3511 Meadowrun Drive
Durham, North Carolina 27707

Citizen of: CHINA

Post Office Address: Same as above

AUG. 8. 2000 1:43PM

OB1 SPIVAK ET AL

NO. 1699 P. 2

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.

Applicant or Patentee: Qin-Yi TongSerial or Patent No.: New ApplicationAtty. Dkt. No.: 2025-0180-20Filed or issued: HerewithFor: "A METHOD OF EPITAXIAL-LIKE WAFER BONDING AT LOW TEMPERATURE AND BONDED STRUCTURE"**VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS
(37 CFR 1.9(f) and 1.27(d)) - NONPROFIT ORGANIZATION**

I hereby declare that I am an official empowered to act on behalf of the nonprofit organization identified below:

NAME OF ORGANIZATION RESEARCH TRIANGLE INSTITUTEADDRESS OF ORGANIZATION P.O. Box 12194, Research Triangle Park
North Carolina 27709

TYPE OF ORGANIZATION

☐ UNIVERSITY OR OTHER INSTITUTION OF HIGHER EDUCATION☐ TAX EXEMPT UNDER INTERNAL REVENUE SERVICE CODE (26 USC 501(a) and 501(c) (3))☒ NONPROFIT SCIENTIFIC OR EDUCATIONAL UNDER STATUTE OF STATE OF THE UNITED STATES OF AMERICA

(NAME OF STATE _____)

(CITATION OF STATUTE _____)

☐ WOULD QUALIFY AS TAX EXEMPT UNDER INTERNAL REVENUE SERVICE CODE (26 USC 501(a) and 501(c)(3)) IF LOCATED IN THE UNITED STATES OF AMERICA☐ WOULD QUALIFY AS NONPROFIT SCIENTIFIC OR EDUCATIONAL UNDER STATUTE OF STATE OF THE UNITED STATES OF AMERICA IF LOCATED IN THE UNITED STATES OF AMERICA

(NAME OF STATE _____)

(CITATION OF STATUTE _____)

I hereby declare that the nonprofit organization identified above qualifies as a nonprofit organization as defined in 37 CFR 1.9(e) for purposes of paying reduced fees under section 41(a) or (b) of Title 35, United States Code with regard to the invention entitled "A METHOD OF EPITAXIAL-LIKE WAFER BONDING AT LOW TEMPERATURE AND BONDED STRUCTURE"

by inventor(s) _____ described in _____

☒ the specification filed herewith☐ application serial no. _____, filed _____☐ patent no. _____, issued _____

I hereby declare that rights under contract or law have been conveyed to and remain with the nonprofit organization with regard to the above identified invention.

If the rights held by the nonprofit organization are not exclusive, each individual, concern or organization having rights to the invention is listed below and no rights to the invention are held by any person, other than the inventor, who could not qualify as a small business concern under 37 CFR 1.9(d) or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e). (NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27))

NAME _____

ADDRESS _____

☐ INDIVIDUAL ☐ SMALL BUSINESS CONCERN ☐ NONPROFIT ORGANIZATION

NAME _____

ADDRESS _____

☐ INDIVIDUAL ☐ SMALL BUSINESS CONCERN ☐ NONPROFIT ORGANIZATION

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements, and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF PERSON SIGNING David H. FaucetteTITLE IN ORGANIZATION Senior Patent & Licensing OfficerADDRESS OF PERSON SIGNING 3040 Cornwallis Road, P.O. Box 12194Research Triangle Park, North Carolina 27709SIGNATURE David H. Faucette DATE 8/9/00



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/635,272	08/09/00	TUNG	0 2025-0180-20

022850 MM01/1212
OBLON SPIVAK MCCLELLAND MAIER & NEUSTADT
FOURTH FLOOR
1755 JEFFERSON DAVIS HIGHWAY
ARLINGTON VA 22202

EXAMINER	
ZARNEKE, D	
ART UNIT	PAPER NUMBER
2812	2
DATE MAILED: 12/12/00	

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/635,272	TONG, QIN-YI	
	Examiner	Art Unit	
	David A. Zarneke	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☐ Responsive to communication(s) filed on _____.

2a) ☐ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-58 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☐ Claim(s) _____ is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☒ Claims 1-58 are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some * c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15) ☐ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other.

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Claims 1-43, drawn to a method, classified in class 438, subclass 455.
- II. Claims 44-58, drawn to a device, classified in class 257, subclass 1+.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the process as claimed can be used to make other and materially different product. For example, not all surface defect regions, as claimed in process claim 1, are amorphous, as claimed in product claim 44. Therefore, a non-amorphous surface defect region is possible.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

A telephone call was made to Carl Schlier on December 5, 2000 to request an oral election to the above restriction requirement, but did not result in an election being made.

Application/Control Number: 09/635,272
Art Unit: 2812


Page 3

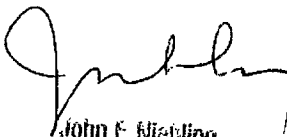
Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David A. Zarneke whose telephone number is (703)-305-3926. The examiner can normally be reached on M-Th (7:30-6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703)-308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are (703)-308-7722 for regular communications and (703)308-7721 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-308-0956.


David A. Zarneke
December 6, 2000


John F. Niebling
Supervisory Patent Examiner
Technology Center 2800

OBLON, SPIVAK, McCLELLAND, MAIER & NEUSTADT, P.C.

ATTORNEYS AT LAW

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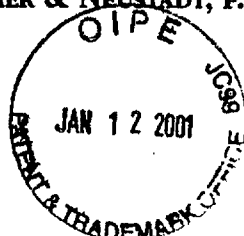
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PATENT, TRADEMARK AND COPYRIGHT LAW
AND RELATED FEDERAL AND ITC LITIGATION



Docket No.: 2025-0180-20

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

RE: Application Serial No.: 09/635,272

Applicants: Qin-Yi TONG

Filing Date: August 9, 2000

For: METHOD OF EPITAXIAL-LIKE WAFER BONDING

Group Art Unit: 2812

Examiner: ZARNEKE, D.

SIR:

Attached hereto for filing are the following papers:

Response to Restriction Requirement

Our check in the amount of \$0.00 is attached covering any required fees. In the event any variance exists between the amount enclosed and the Patent Office charges for filing the above-noted documents, including any fees required under 37 C.F.R. 1.136 for any necessary Extension of Time to make the filing of the attached documents timely, please charge or credit the difference to our Deposit Account No. 15-0030. Further, if these papers are not considered timely filed, then a petition is hereby made under 37 C.F.R. 1.136 for the necessary extension of time. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Carl E. Schlier

Eckhard H. Kuesters

Attorney of Record

Registration No. 28,870

Carl E. Schlier

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22850

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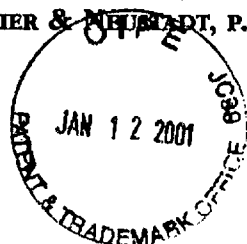
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PATENT, TRADEMARK AND COPYRIGHT LAW
AND RELATED FEDERAL AND ITC LITIGATION



Docket No.: 2025-0180-20

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

RE: Application Serial No.: 09/635,272

Applicants: Qin-Yi TONG

Filing Date: August 9, 2000

For: METHOD OF EPITAXIAL-LIKE WAFER BONDING . .

Group Art Unit: 2812

Examiner: ZARNEKE, D.

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* JAPANESE PATENT ATTORNEY
* REGISTERED PATENT AGENT

SIR:

Attached hereto for filing are the following papers:

Response to Restriction Requirement

Our check in the amount of \$0.00 is attached covering any required fees. In the event any variance exists between the amount enclosed and the Patent Office charges for filing the above-noted documents, including any fees required under 37 C.F.R. 1.136 for any necessary Extension of Time to make the filing of the attached documents timely, please charge or credit the difference to our Deposit Account No. 15-0030. Further, if these papers are not considered timely filed, then a petition is hereby made under 37 C.F.R. 1.136 for the necessary extension of time. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF:

QIN-YI TONG

SERIAL NO: 09/635,272

FILED: August 9, 2000

FOR: METHOD OF EPITAXIAL-LIKE
WAFER BONDING AT LOW
TEMPERATURE AND BONDED
STRUCTURE



:
: GROUP ART UNIT: 2812
:
: EXAMINER: ZARNEKE, D.

#3
1-19-01
C. B. Dan

RESPONSE TO RESTRICTION REQUIREMENT

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

In response to the restriction requirement of December 12, 2000, Applicant elects
with traverse, Group II, drawn to a device, corresponding to claims 44-58.

The proper criteria for restriction between distinct inventions is provided in MPEP
§803. The two criterion are (1) the inventions must be independent or distinct as claimed and
(2) there must be a *serious* burden on the examiner if restriction is not required.

Turning to the second criterion, if the search and examination of an entire application
can be made without a serious burden, the examiner *must* examine it on the merits, even
though it includes claims to independent or distinct inventions (MPEP §803 (emphasis
ours)).

Although the Office Action has identified separate classifications, making a *prima face* case
of a serious burden, it is respectfully submitted that there is no serious burden in searching
and examining the entire application.

Both the method claims and the structure claims are related to bonding. There
appears to be overlap in the search areas, facilitating a search of both the method and


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structure claims. The ability to do searching electronically also greatly simplifies the search process. Moreover, references in the semiconductor field often have descriptions of both a process and the structure made using the process. Finding and considering references for the process claims will likely lead to finding and considering references for the structure claims, as a matter of course.

There appears to be little, if any, extra effort in searching and examining claims 1-58 compared to searching and examining claims 44-58, even though the inventions of Groups I and II are distinct. It is therefore respectfully submitted that there is no *serious* burden on the examiner, and examination of claims 1-58 in this application is proper.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



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Attorney of Record
Registration No. 28,870

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Docket No 2025-0180-20

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Qin-Yi TONG

SERIAL NO: 09/635,272

FILED: August 9, 2000

FOR: A METHOD OF EPITAXIAL-LIKE WAFER BONDING AT LOW TEMPERATURE AND BONDED STRUCTURE

GAU: 2812

EXAMINER: ZARNEKE, D.

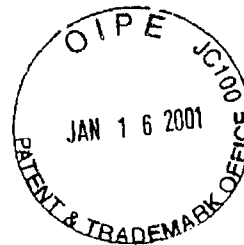
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INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Applicant(s) wish to disclose the following information.



REFERENCES

- ☒ The applicant(s) wish to make of record the references listed on the attached form PTO-1449. Copies of the listed references are attached, where required, as are either statements of relevancy or any readily available English translations of pertinent portions of any non-English language references.
- ☐ A check is attached in the amount required under 37 CFR §1.17(p).

RELATED CASES

- ☐ Attached is a list of applicant's pending application(s) or issued patent(s) which may be related to the present application. A copy of the patent(s) is attached along with PTO 1449.
- ☐ A check is attached in the amount required under 37 CFR §1.17(p).

CERTIFICATION

- ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.
- ☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

PETITION

- ☐ Applicant(s) hereby request consideration of the attached information. A check is attached in the amount of the Petition fee required under 37 CFR §1.17(i)(1).

DEPOSIT ACCOUNT

- ☒ Please charge any additional fees for the papers being filed herewith and for which no check is enclosed herewith, or credit any overpayment to deposit account number 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
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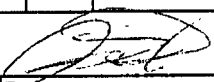
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Form PTO 1449 (Modified)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY DOCKET NO. 2025-0180-20		SERIAL NO. 09/635,272	
LIST OF REFERENCES CITED BY APPLICANT				APPLICANT Qin-Yi TONG		JAN 16 2001	
				FILING DATE August 9, 2000		GROUP 2812	
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
P	AA	5,877,070	03/02/99	U. M. GOESELE, et al.	438	458	
P	AB	5,915,167	06/22/99	Glenn J. LEEDY	438	108	
P	AC	5,354,695	10/11/94	Glenn J. LEEDY	438	411	
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P	AE	Q. Y. TONG, et al., Appl. Phys. Lett., Vol. 64, No. 5, Pages 625-627, "HYDROPHOBIC SILICON WAFER BONDING", January 31, 1994					
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Examiner					Date Considered		
[Signature]					9/12/01		

*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO 1449 (Modified)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY DOCKET NO. 2025-0180-20		SERIAL NO. 09/635,272	
LIST OF REFERENCES CITED BY APPLICANT				APPLICANT Qin-Yi TONG			
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OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)							
P	AU	L. RAYLEIGH, Proceedings of the Royal Society of London, Series A -- Mathematical and Physical Sciences, Vol. 156, Pages 326-349, "A STUDY OF GLASS SURFACES IN OPTICAL CONTACT", September 1, 1936					
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P	AX	Q.-Y. TONG, et al., 1999 IEEE International SOI Conference, Pages 104-105, "IOS---A NEW TYPE OF MATERIALS COMBINATION FOR SYSTEM-ON-A CHIP PREPARATION," October 1999.					
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P	BD	B.M. ARORA, et al., J. Vac. Sci. Technol. Vol. B5, No. 4, Pages 876-882, "REACTIVE ION-ETCHING-INDUCED DAMAGE IN SILICON USING SF ₆ GAS MIXTURES", Jul/Aug 1987					
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P	BK	J. BAGDAHN, et al., Proceedings of the Fourth International Symposium on Semiconductor Wafer Bonding: Science, Technology, and Applications, Proceedings Vol. 97-36, Pages 291-298, "CHARACTERISATION OF DIRECTLY BONDED SILICON WAFERS BY MEANS OF THE DOUBLE CANTILEVER CRACK OPENING METHOD", (no date)					
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P	BO	DARRELL HILL, et al., IEEE Microwave and Guided Wave Letters, Vol. 5, No. 11, Pages 373-375, "NOVEL HBT WITH REDUCED THERMAL IMPEDANCE", November 1995					
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Examiner				Date Considered 9/10/01			

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OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)							
QY	BU	Q-Y. TONG, et al., MRS Bulletin, Pages 40-44, "BEYOND "SMART-CUT®": RECENT ADVANCES IN LAYER TRANSFER FOR MATERIAL INTEGRATION", December 1998					
QY	BV	JAN HAISMA, Philips Journal of Research, Vol. 49, No. 1/2, Pages 165-170, "DIRECT BONDING IN PATENT LITERATURE", 1995					
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LIST OF REFERENCES CITED BY APPLICANT				APPLICANT Qin-Yi TONG		JAN 16 2001 2812	
				FILING DATE August 9, 2000			
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Docket No. 2025-0180-20

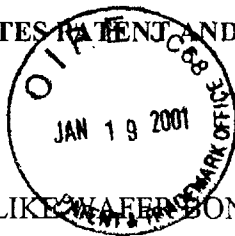
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Qin-Yi TONG

SERIAL NO: 09/635,272

FILED: August 9, 2000

FOR: A METHOD OF EPITAXIAL-LIKE WAFER BONDING AT LOW TEMPERATURE AND BONDED STRUCTURE



GAU: 2812

EXAMINER: ZARNEKE, D.

#4
S. Coates
1/26/01

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Applicant(s) wish to disclose the following information.

REFERENCES

- ☒ The applicant(s) wish to make of record the references listed on the attached form PTO-1449. Copies of the listed references are attached, where required, as are either statements of relevancy or any readily available English translations of pertinent portions of any non-English language references.
- ☐ A check is attached in the amount required under 37 CFR §1.17(p).

RELATED CASES

- ☐ Attached is a list of applicant's pending application(s) or issued patent(s) which may be related to the present application. A copy of the patent(s) is attached along with PTO 1449.
- ☐ A check is attached in the amount required under 37 CFR §1.17(p).

CERTIFICATION

- ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.
- ☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

PETITION

- ☐ Applicant(s) hereby request consideration of the attached information. A check is attached in the amount of the Petition fee required under 37 CFR §1.17(i)(1).

DEPOSIT ACCOUNT

- ☒ Please charge any additional fees for the papers being filed herewith and for which no check is enclosed herewith, or credit any overpayment to deposit account number 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
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U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

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LIST OF REFERENCES CITED BY APPLICANT

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U.S. PATENT DOCUMENTS

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	AA						
	AB						
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FOREIGN PATENT DOCUMENTS

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	AO					
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	AQ					
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	AT					
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	AV					

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	AW	Q.-Y. TONG, et al., Semiconductor Wafer Bonding Science and Technology, John Wiley & Sons, Inc., 1999
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	AZ	

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Other Prior Art

According to the information contained in form PTO-1449 or PTO-892, there are one or more other prior art/non-patent literature documents missing from the original file history record obtained from the United States Patent and Trademark Office. Upon your request we will attempt to obtain these documents from alternative resources. Please note that additional charges will apply for this service.

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	AS						
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)							
	AT	CIARLO, DINO R., Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology, and Applications, Proceedings Vol. 93-29, Pages 313-326, "HIGH - AND LOW - TEMPERATURE BONDING TECHNIQUES FOR MICROSTRUCTURES", May 1993					
	AU	ROSS, R.C., et al., Journal of Non-Crystalline Solids, Vol. 66, Pages 81-86, "PHYSICAL MICROSTRUCTURE IN DEVICE-QUALITY HYDROGENATED AMORPHOUS SILICON", 1984					
	AV	KO, W.H., et al., Micromachining and Micropackaging of Transducers, Pages 41-61, "BONDING TECHNIQUES FOR MICROSENSORS", 1985					
	AW	AUBERTON-HERVÉ, et al., Proceedings of the Eighth International Symposium on Silicon Materials Science and Technology, Silicon Materials Science and Technology, Vol. 2, Electrochemical Society Proceedings, Vol. 98-1, Pages 1341-1360, "SILICON ON INSULATOR WAFERS USING THE SMART CUT® TECHNOLOGY", 1998					
	AX	MITANI, KIYOSHI, Wafer Bonding: Studies of Interface Bubbles and Electrical Characterization, Department of Electrical Engineering, Duke University, 1991					
Examiner					Date Considered 3/14/01		
*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

BEST COPY



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
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Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/635,242	08/09/00	YIP, C	2000-033,042-20
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022846 MM02/0001
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EXAMINER

DIAG. 3
ART UNIT PAPER NUMBER

2000
DATE MAILED: 03/21/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.

09/635,272

Applicant(s)

TONG, QIN-YI

Examiner

José R. Díaz

Art Unit

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 January 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 44-58 is/are pending in the application.
- 4a) Of the above claim(s) 1-43 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 44-58 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

- 15) ☒ Notice of References Cited (PTO-892)
- 16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4,5.
- 18) ☐ Interview Summary (PTO-413) Paper No(s) _____.
- 19) ☐ Notice of Informal Patent Application (PTO-152)
- 20) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of claims 1-43 in Paper No. 3 is acknowledged. The traversal is on the ground(s) that there is no serious burden in searching and examining the entire application. This is not found persuasive because the restriction requirement sets forth in the MPEP do not take into account whether the Examiner searches in the paper or electronic files. Furthermore, since the Examiner has not indicated the full search area, Applicant's argument that this is not serious burden on the Examiner that "there appears to be overlap in the search areas, facilitating a search of both the method and structure claims" is not persuasive. Lastly, Applicant states the following "finding and considering references for the process claims will likely lead to finding and considering references for the structure claims, as a matter of course." If the Applicant states for the record that the method claims are not patentable distinct from the device claims, the restriction requirement would be withdrawn.

The requirement is still deemed proper and is therefore made FINAL.

Claim Objections

➤ Claims 54-58 are objected to under 37 CFR 1.75 as being a substantial duplicate of claims 44, 46, 49, 51 and 53. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 112

- The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

- Claims 48 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 48, it is not clear to the Examiner how the semiconductor devices are formed on the substrates. It is unclear whether the semiconductor devices are formed after the formation of the amorphous layers "in said substrate", as recited in claim 44, or before the formation of the amorphous layers (i.e. before the silicon layers are treated to form the amorphous layers, as disclosed on page 14, lines 26-31 and page 15, lines 1-5). Furthermore, it is not clear how the first and second silicon layers are related to the first and second amorphous layers.

Claim Rejections - 35 USC § 102

- The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

➤ Claims 44-46 and 54-55 are rejected under 35 U.S.C. 102(b) as being anticipated by Kish, Jr. et al. (US Patent No. 5,783,477).

Regarding claims 44 and 54, Kish, Jr. et al. teach a bonded structure (See Figures 1-9), comprising: a first substrate having a first surface (95), a first amorphous layer (91) formed in said first surface (See Figure 9); and a second substrate having a second surface (93), a second amorphous layer (91) formed in said second surface (See Figure 9); said first surface being bonded to said second surface to form a bonded pair substrates (See Figure 9). Furthermore, the claim 54 contains method of making characteristics (i.e. forming an amorphous layer by exposing the substrate to boron ambient) given no patentable weight in determining patentability of the final device structure. Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding claim 45, it would have been obvious to one having ordinary skill in the art at the time the invention was made to bond additional substrates to the bonded

structure since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8.

Regarding claims 46 and 55, Kish, Jr. et al. teach that the substrates comprise are selected from Si, InGaAs, InP, GaAs, Ge and SiC (see col. 3, lines 51-67).

➤ Claims 44, 47, 49-54, and 56-58 are rejected under 35 U.S.C. 102(e) as being anticipated by Eda (US Patent No. 6,120,917).

Regarding claims 44 and 54, Eda teaches a bonded structure (See Figures 1-22), comprising: a first substrate having a first surface (1), a first amorphous layer (8) formed in said first surface (See Figure 14); and a second substrate having a second surface (2) (See Figure 14), a second amorphous layer formed in said second surface (See col. 16, lines 55-59); said first surface being bonded to said second surface to form a bonded pair substrates (See Figure 14). Furthermore, the claim 54 contains method of making characteristics (i.e. forming an amorphous layer by exposing the substrate to boron ambient) given no patentable weight in determining patentability of the final device structure. Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious

product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding claim 47, Eda teaches that the first and second substrates each comprises a silicon substrate, and that the first and second surfaces each comprises a silicon surface (See Example 8, col. 16, lines 58-59, and col. 17, lines 37-53).

Regarding claims 49-52 and 56-57, Eda teaches forming amorphous layers (8) on said first and second silicon surfaces (See Figure 14, col. 16, lines 55-59, and col. 17, lines 37-53). Furthermore, the claims 49-52 contain method of making characteristics (i.e. forming an amorphous layer by exposing a silicon surface to a boron-containing plasma, to an inert gas plasma, to an implantation of boron, or to an implantation of arsenic) given no patentable weight in determining patentability of the final device structure. Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding claims 53 and 58, it is well known in the art that silicon materials are fully or partly bonded by covalent bonds, hence it is inherent that the amorphous silicon layers formed over the substrates, as disclosed by Eda, are bonded by covalent bonds.

Claim Rejections - 35 USC § 103

➤ The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

➤ Claim 48 rejected under 35 U.S.C. 103(a) as being unpatentable over Eda (US Patent No. 6,120,917) in view of Sato et al. (US Patent No. 6,143,628).

Eda, as stated supra, essentially discloses the claimed invention but fails to teach semiconductor devices formed on the substrates. Regarding claim 48, Sato et al. teach that it is well known in the art to form a semiconductor device over the amorphous layer prior bonding the substrates (See col. 15, lines 18-26). Sato et al. provide motivation to use such a semiconductor device in that it completes the integrated circuit (See col. 1, lines 5-14). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to have modified Eda to include forming a semiconductor device over the amorphous layer as taught by Sato et al. since such modification would result in a completed integrated circuit, as described in col. 1, lines 5-14 of Sato et al. Regarding the formation of an additional semiconductor device in the bonded structure, it would have been obvious to one having ordinary skill in the

Application/Control Number: 09/635,272
Art Unit: 2815

Page 8

art at the time the invention was made to form an additional semiconductor device in the bonded structure since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (703) 308-6078. The examiner can normally be reached on 8:00 - 5:00 Monday through Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.



EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

JRD
March 19, 2001

Notice of References Cited	Application/Control No. 09/635,272	Applicant(s)/Patent Under Reexamination TONS, QIN-YI	
	Examiner José R. Díaz	Art Unit 2815	Page 1 of 1

U.S. PATENT DOCUMENTS

* A-M	Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
A	US-5,783,477-	07-1998	Kish, Jr. et al.	438 455
B	US-6,143,628-	11-2000	Sato et al.	438 455
C	US-6,120,917-	09-2000	Eda	428 692
D	US- -			
E	US- -			
F	US- -			
G	US- -			
H	US- -			
I	US- -			
J	US- -			
K	US- -			
L	US- -			
M	US- -			

FOREIGN PATENT DOCUMENTS

* N-T	Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
N	- -				
O	- -				
P	- -				
Q	- -				
R	- -				
S	- -				
T	- -				

NON-PATENT DOCUMENTS

* U-X	Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
U	
V	
W	
X	

Docket No. 149840US-20

IN RE APPLICATION OF: Qin-Yi TONG

SERIAL NO: 09/635,272

FILED: August 9, 2000

FOR: METHOD OF EPITAXIAL-LIKE WATER BONDING AT LOW TEMPERATURE...



ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Transmitted herewith is an amendment in the above-identified application.

- ☐ No additional fee is required
- ☒ Small entity status of this application under 37 C.F.R. §1.9 and §1.27 is claimed.
- ☒ Additional documents filed herewith: Marked Up Copy

The Fee has been calculated as shown below:

CLAIMS	CLAIMS REMAINING		HIGHEST NUMBER PREVIOUSLY PAID	NO. EXTRA CLAIMS	RATE	CALCULATIONS	
TOTAL	66	MINUS	58	8	× \$18 =	\$144.00	
INDEPENDENT	6	MINUS	4	2	× \$80 =	\$160.00	
		<input type="checkbox"/>	MULTIPLE DEPENDENT CLAIMS		+ \$270 =	\$0.00	
		TOTAL OF ABOVE CALCULATIONS					\$304.00
		<input checked="" type="checkbox"/> Reduction by 50% for filing by Small Entity					\$-152.00
		<input type="checkbox"/> Recordation of Assignment				+ \$40 =	\$0.00
		TOTAL					\$152.00

- ☒ A check in the amount of **\$152.00** is attached.
- ☒ Please charge any additional Fees for the papers being filed herewith and for which no check is enclosed herewith, or credit any overpayment to deposit Account No. 15-0030. A duplicate copy of this sheet is enclosed.
- ☒ If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time may be charged to Deposit Account No. 15-0030. A duplicate copy of this sheet is enclosed.



22850

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2815
#

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149840US-20

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF:

QIN-YI TONG

SERIAL NO: 09/635,272

FILED: AUGUST 9, 2000

FOR: METHOD OF EPITAXIAL-LIKE
WATER BONDING AT LOW
TEMPERATURE AND
BONDED STRUCTURE

:

: EXAMINER: J. DIAZ

:

: GROUP ART UNIT: 2815

:

AMENDMENT

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Responsive to the Office Action dated March 21, 2001, please amend the above-identified application as follows:

IN THE SPECIFICATION

Please replace the paragraph on page 1, beginning at line 15 with the following:

A1 For many optoelectronic and electronic device applications, homo-epitaxial single crystalline layers consisting of same material with same crystalline orientation but different doping types or levels are necessary. For some device applications, active layers comprising single crystalline dissimilar materials are required. The active layers should be high crystallographic quality with interfaces that are thermally conductive and almost optical loss

cont. free. Conventional hetero-epitaxial growth techniques applied to these lattice mismatched active layers usually result in a large density of threading dislocations in the bulk of the layers. Bonding of single crystalline wafers of identical or dissimilar materials is an unique alternative approach to the epitaxial growth. Not only highly lattice-mismatched wafers can be bonded but also wafers with different crystalline orientations can be combined. Ideally, the mismatches of single crystalline bonding wafers are accommodated by dislocations (in lattice-mismatch case) or an amorphous layer (in orientation-mismatch case) localized at the bonding interface with no defects generated in the bulk area. This approach is termed epitaxial-like bonding. The epitaxial-like bonding can also be employed to prepare unique devices by integrating already processed device layers.

Please replace the paragraph on page 3, beginning at line 24 with the following:

These and other objects of the present invention are provided by a method for bonding first and second substrates including steps of preparing substantially oxide-free first and second surfaces of respective first and second substrates, creating a surface defect region in each of said first and second surfaces, and bonding said first and second surfaces.

A2 Creating the defective region may include plasma-treating the first and second surfaces of the first and second substrates with a plasma, and preferably a boron-containing plasma. The plasma-treating step may utilize a plasma in reactive ion etch (RIE) mode using B_2H_6 gas, and possibly a mixture of B_2H_6 , He, and Ar gases. Other gas plasmas, such as Ar may also be used.

Please replace the paragraph on page 13, beginning at line 14 with the following:

A3 A fourth embodiment of the present invention is to use As (arsenic) ion implantation

cont. A3 to silicon wafers to form an amorphous layer on the wafer surface. Method steps for an As ion implantation treatment bonding process follow the steps shown in FIG. 1. After cleaning, As ion implantation is performed at an energy of 180 keV with a dose of $9 \times 10^{14}/\text{cm}^2$. Any oxide layer is then removed prior to bonding. The As doping concentration peak of $8 \times 10^{19}/\text{cm}^3$ is located at $\sim 1150 \text{ \AA}$ from the silicon surface. Although this implantation induced a very low As doping on the wafer surface, an amorphous layer with 1650 \AA thick was formed as confirmed both by a Monte Carlo simulation and TEM measurement (FIG. 10). The thickness of the amorphous layer can vary and is not limited to the value of this example. For instance, other ions may be implanted to create the amorphous layer. Arsenic is a dopant, and there are applications when it is desired not to dope the substrate so another ion, such as a non-doping ion like Ar, would be chosen.

IN THE CLAIMS

Please cancel claims 1-43 without prejudice.

Please amend the claims as shown in the marked-up copy to read as follows:

94 sub B1 > 44. (Amended) A bonded structure, comprising:
a first substrate having a first surface, a first nearly-amorphized layer formed in said first surface; and
a second substrate having a second surface, a second nearly-amorphized layer formed in said second surface;
said first surface being bonded to said second surface to form a bonded pair of substrates.

2. 45. (Amended) A structure as recited in claim 44, comprising:

one of said first and second substrates of said bonded pair having a third surface, said third surface having a nearly-amorphized layer;

a third substrate having a fourth surface, a fourth nearly-amorphized layer formed in said fourth surface; and

said third surface bonded to said fourth surface.

5. 46. (Amended) A structure as recited in claim 44, wherein:

said first and second substrates comprise respective first and second semiconductor devices.

54. (Amended) A bonded structure, comprising:

a first substrate having an amorphized first surface, said first surface containing boron;

a second substrate having an amorphized second surface, said second surface containing boron; and

said first surface being bonded to said second surface to form a bonded pair of substrates.

Please add the following new claims:

59. (New) A bonded structure, comprising:

a first substrate having a first surface, a first amorphous arsenic-containing layer formed in said first surface; and

a second substrate having a second surface, a second amorphous arsenic-containing layer formed in said second surface;

said first surface being bonded to said second surface to form a bonded pair of substrates.

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60. (New) A structure as recited in claim 59, comprising:

one of said first and second substrates of said bonded pair having a third surface, said third surface having an amorphous layer;

a third substrate having a fourth surface, a fourth amorphous layer formed in said fourth surface; and

said third surface bonded to said fourth surface.

24.

61. (New) A structure as recited in claim 60, wherein:

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said third surface comprises an amorphous arsenic-containing layer; and

said fourth surface comprises an amorphous arsenic-containing layer.

25.

62. (New) A structure as recited in claim 59, wherein said first and second substrates are selected from Si, InGaAs, InP, GaAs, Ge and SiC.

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63. (New) A structure as recited in claim 59, wherein:

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said first and second substrates each comprises a silicon substrate; and

said first and second surfaces each comprises an arsenic-containing silicon surface.

64. (New) A structure as recited in claim 59, wherein:

sub
c1

said first surface comprises a substantially planar surface of a first arsenic-containing silicon layer formed on said first device; and

said second surface comprises a substantially planar surface of a second arsenic-containing silicon layer formed on said second device.

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65. (New) A structure as recited in claim 59, wherein:

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said first surface comprises a first silicon surface implanted with arsenic; and

said second surface comprises a second silicon surface implanted with arsenic.

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66. (New) A structure as recited in claim 65, comprising:

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Si covalent bonds formed between said first and second substrates.

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67. (New) A structure as recited in claim 59, comprising:

said first and second surfaces being substantially oxide-free.

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68. (New) A structure as recited in claim 59, wherein:

said amorphized first and second surfaces are each in the range of a few nm in

thickness.

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69. (New) A structure as recited in claim 59, wherein:

said amorphized first and second surfaces each comprises a few monolayers of

arsenic.

a7
sub 34

70. (New) A bonded structure, comprising:

a first substrate having an amorphized substantially oxide-free first surface; and

a second substrate having an amorphized substantially oxide-free second surface;

said first surface being bonded to said second surface to form a bonded pair of

substrates.

34.

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71. (New) A structure as recited in claim 70, wherein:

said first substrate comprises one material having said first surface; and

said second substrate comprises one material having said second surface.

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72. (New) A structure as recited in claim 70, comprising:

one of said first and second substrates of said bonded pair having an amorphized substantially oxide-free third surface;

a third substrate having an amorphized substantially oxide-free fourth surface; and

said third surface bonded to said fourth surface.

36.

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73. (New) A structure as recited in claim 70, wherein said first and second substrates

are selected from Si, InGaAs, InP, GaAs, Ge and SiC.

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74. (New) A structure as recited in claim 70, wherein:

said first and second substrates each comprises a silicon substrate; and

said first and second surfaces each comprises an amorphized substantially oxide-free silicon surface.

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75. (New) A structure as recited in claim 70, wherein:

said first surface comprises a substantially planar surface of a first amorphous substantially oxide-free silicon layer formed on said first device; and

said second surface comprises a substantially planar surface of a second amorphous substantially oxide-free silicon layer formed on said second device.

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76. (New) A structure as recited in claim 70, wherein:

said first surface comprises a surface exposed to a boron-containing plasma; and

said second surface comprises a surface exposed to a boron-containing plasma.

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77. (New) A structure as recited in claim 70, wherein:

said first surface comprises a surface exposed to an inert gas plasma; and

said second surface comprises a surface exposed to an inert gas plasma.

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78. (New) A structure as recited in claim 70, wherein:

said first surface comprises an ion-implanted surface; and

said second surface comprises an ion-implanted surface.

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79. (New) A structure as recited in claim 70, wherein:

said first surface comprises a surface ion-implanted with one of boron and arsenic;

and

said second surface comprises a surface ion-implanted with one of boron and arsenic.

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80. (New) A structure as recited in claim 70, comprising:

boron-boron formed between said first and second substrates.

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Q

43.

81. (New) A bonded structure, comprising:

a first substrate having a first surface with an amorphized first surface region extending only one to a few monolayers into said first substrate; and

a second substrate having a second surface an amorphized second surface region extending only one to a few monolayers into said second substrate; and

said first surface being bonded to said second surface to form a bonded pair of substrates.

44.

82. (New) A structure as recited in claim 81, wherein:

said amorphized first and second surface regions are each in the range of a few nm in thickness.

45.

83. (New) A structure as recited in claim 81, wherein:

said first and second surface regions each comprise at least one region extending over a substantial portion of a surface of said first and second substrates, respectively.

46.

84. (New) A structure as recited in claim 81, comprising:

one of said first and second substrates of said bonded pair having a third surface with an amorphized third surface region;

a third substrate having a fourth surface with an amorphized fourth surface region;

and

said third surface bonded to said fourth surface.

47.

85. (New) A structure as recited in claim 81, wherein said first and second substrates

are selected from Si, InGaAs, InP, GaAs, Ge and SiC.

48.

86. (New) A structure as recited in claim 81, wherein:

said first and second substrates each comprises a silicon substrate; and

said first and second surfaces each comprises a silicon surface.

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87. (New) A structure as recited in claim 81, wherein:

43

said first surface comprises a surface exposed to a boron-containing plasma; and
said second surface comprises a surface exposed to a boron-containing plasma.

88. (New) A structure as recited in claim 81, wherein:

said first surface comprises a surface exposed to an inert gas plasma; and
said second surface comprises a surface exposed to an inert gas plasma.

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89. (New) A structure as recited in claim 81, wherein:

43

said first surface comprises an ion-implanted surface; and
said second surface comprises an ion-implanted surface.

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90. (New) A structure as recited in claim 81, wherein:

43

said first surface comprises a surface implanted with one of boron and arsenic; and
said second surface comprises a second surface implanted with one of boron and

arsenic.

52

91. (New) A structure as recited in claim 81, comprising:

50

boron-boron covalent bonds formed between said first and second substrates.

92. (New) A bonded structure, comprising:

a first substrate of substantially one first material amorphized substantially only in a
first surface of said first material; and
a second substrate of substantially one second material amorphized substantially only
in a second surface of said second material;
said first surface being bonded to said second surface to form a bonded pair of
substrates.

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57. 93. (New) A structure as recited in claim 92, comprising:
one of said first and second substrates of said bonded pair being amorphized only in said first surface and in a third surface of said first material;
a third substrate of substantially one third material amorphized only in a third surface of said third material; and

said third surface bonded to said fourth surface.
55. 94. (New) A structure as recited in claim 92, wherein said first and second substrates are selected from Si, InGaAs, InP, GaAs, Ge and SiC;

56. 95. (New) A structure as recited in claim 92, wherein:
said first and second substrates each comprises a silicon substrate; and
said first and second surfaces each comprises a silicon surface.

61 57. 96. (New) A structure as recited in claim 92, wherein:
said first surface comprises a substantially planar surface of a first silicon layer formed on said first device; and
said second surface comprises a substantially planar surface of a second silicon layer formed on said second device.

58. 97. (New) A structure as recited in claim 92, wherein:
said first surface comprises a surface exposed to a boron-containing plasma; and
said second surface comprises a surface exposed to a boron-containing plasma.

98. (New) A structure as recited in claim 92, wherein:
said first surface comprises a surface exposed to an inert gas plasma; and
said second surface comprises a surface exposed to an inert gas plasma.

59.

99. (New) A structure as recited in claim 92, wherein:

said first surface comprises a surface implanted with one of boron and arsenic; and

said second surface comprises a surface implanted with one of boron and arsenic.

60.

100. (New) A structure as recited in claim 99, comprising:

boron-boron covalent bonds formed between said first and second substrates.

20.

102. (New) A structure as recited in claim 54, wherein:

said amorphized first and second surfaces are each in the range of a few nm in

thickness.

21.

103. (New) A structure as recited in claim 54, wherein:

said amorphized first and second layers each comprises a few monolayers of boron.

10.

104. (New) A structure as recited in claim 44, wherein:

said first and second amorphous layers are each in the range of a few nm in thickness.

11.

105. (New) A structure as recited in claim 44, wherein said first and second layers

each comprise a few monolayers of boron.

12.

106. (New) A structure as recited in claim 44, wherein:

said first surface comprises an amorphous boron-containing layer; and

said second surface comprises an amorphous boron-containing layer.

13.

107. (New) A structure as recited in claim 44, wherein:

said first surface comprises a surface exposed to a boron-containing plasma; and

said second surface comprises a surface exposed to a boron-containing plasma.

14.

108. (New) A structure as recited in claim 44, wherein:

said first surface comprises a first surface exposed to an inert gas plasma; and

said second surface comprises a second surface exposed to an inert gas plasma.

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109. (New) A structure as recited in claim 44, wherein:

said first surface comprises an ion-implanted surface; and

said second surface comprises an ion-implanted surface implanted.

REMARKS

Favorable reconsideration of this application is respectfully requested.

The specification has been amended to correct three minor typographical errors noted upon review of the application.

Claims 44-109 are now present in this application, claims 1-43 being canceled and claims 59-109 being added by way of the present amendment. Claims 54-58 stand objected to under 37 C.F.R. §1.75 as being substantially duplicate of respective claims 44, 46, 49, 51 and 53. Claim 48 stands rejected under 35 U.S.C. §112, second paragraph. Claims 44-46, 54 and 55 stand rejected under 35 U.S.C. §102(b) as anticipated by U.S. 5,783,477 (Kish, Jr. et al), claims 44, 47, 49-54 and 56-58 stand rejected under 35 U.S.C. §102(e) as anticipated by U.S. 6,120,917 (Eda), and claim 48 stands rejected under 35 U.S.C. §103(a) as unpatentable over Eda in view of U.S. 6,143,628 (Sato et al).

Regarding the objection under 37 C.F.R. §1.75, claim 44 recites first and second substrates having respective first and second surfaces, and first and second layers formed in the first and second surfaces, respectively. Claim 54 recites amorphized first and second surfaces each containing boron. Claim 44 does not mention boron, and thus the claims are clearly of different scope and cannot be considered duplicates of each other. Withdrawal of the objection under 37 C.F.R. §1.75 is respectfully requested.

Claim 48 was rejected since it was found unclear whether the devices are formed

before or after the formation of the amorphous layers, and being unclear as to how the first and second silicon layers are related to the first and second amorphous layers. First, it does not matter when the device are formed, as claim 48 goes to structure. The claim has been broadened by removing the silicon layer element, simultaneously rendering moot the §112 rejection.

① Does?
New matter
lay 15

Turning to the rejection over Kish, Jr. et al (hereafter "Kish"), the Office Action refers to element 95 as the first surface of a first substrate. However, reference numeral 95 refers to bonding layer 95 formed on the semiconductor layer. There is no suggestion of any nearly-amorphized layers formed in a substrate. Kish simply have amorphous regions in a layer formed on the substrate. There is therefore no suggestion of claim 44 and withdrawal of the rejection of claim 44 is respectfully requested.

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In claim 54, first and second substrates are recited each having an amorphized surface containing boron. The Office Action describes claim 54 as containing "method of making characteristics" referring to forming an amorphous layer by exposing the substrate to boron ambient. To the contrary, claim 54 recites simply structure and contains no method of making "characteristics" or any language that could lead to a determination that claim 54 is a "product-by-process" claim. Claim 54 recites a surface containing boron, and does not contain any language regarding how the boron comes to be in the amorphized first surface, or any steps in making the structure. A surface containing boron is clearly a structural element. As an example, a surface that does not contain boron is different in structure from one that contains boron. Claim 54 recites purely structure and its treatment as a product-by-process claim is improper.

In order to properly reject claim 54, the prior art must show first and second substrates each having an amorphized surface, the surfaces containing boron. The Office

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Action has not identified any reference having these elements. In other words, there has been no case of obviousness or anticipation set forth in the Office Action. The claim has simply been improperly treated as a method claim, while the claim recites no method elements, but only structure. Accordingly, allowance of claim 54 is in order.

Regarding the rejection over Eda, the Office Action refers to reference numeral 8 as a first amorphous layer formed in the first surface. Layer 8 is not an amorphous layer formed in the first surface but is rather, as described in column 12 in Example 8, an inorganic thin film formed on substrate 1. Claim 44 recites nearly amorphized layers formed in the surface of the substrates. Here, layer 8 is an inorganic film formed on substrate 1. There is no suggestion of any nearly amorphized layer in the surface of a substrate. There is only the teaching of an inorganic thin film formed on a substrate. Accordingly there is clearly no suggestion of claim 44 in Eda and withdrawal of this rejection is respectfully requested.

The same problems with the rejection of claim 54 over Kish noted above also apply to Eda. There is no suggestion of any structure having an amorphized layer containing boron in Eda. Treatment of the claim as a method or product-by-process claim is improper since claim 54 only recites structure, and further the Office Action has identified no prior art having the structure of claim 54. Accordingly, withdrawal of the rejection of claim 54 over Eda is also respectfully requested.

In the rejection of claim 48 over the combination of Eda and Sato et al (hereafter "Sato"), the Office Action refers to an layer 14 as an amorphous layer. The non-porous layer 14 is formed on layers 12 and 13. Claim 48 recites a nearly-amorphized layer formed in the substrate and there is no suggestion of such a layer in Sato. Clearly, Sato fails to disclose or suggest the structure of claim 48 and thus the rejection over the combination of Eda and Sato

also does not suggest the structure of claim 48. Accordingly, withdrawal of the rejection of claim 48 is also respectfully requested.

It is respectfully submitted that the present application is in condition for allowance and a favorable decision to that effect is respectfully requested.

Respectfully submitted,

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Marked-Up Copy

Serial No: __09/635,272__

Amendment Filed on:

____June 21, 2001____

IN THE SPECIFICATION

Please amend the paragraph on page 1, beginning at line 15 as follows:

--For many optoelectronic and electronic device applications, homo-epitaxial single crystalline layers consisting of same material with same crystalline orientation but different doping types or levels are necessary. For some device applications, active layers comprising single crystalline dissimilar materials are required. The active layers should be high crystallographic quality with interfaces that are thermally conductive and almost optical loss free. Conventional hetero-epitaxial growth techniques applied to these lattice mismatched active layers usually result in a large density of threading dislocations in the bulk of the layers. Bonding of single crystalline wafers of identical or dissimilar materials is an unique alternative approach to the epitaxial growth. Not only highly lattice-mismatched wafers can be bonded but also wafers with different crystalline orientations can be combined. Ideally, the mismatches of single crystalline bonding wafers are accommodated by dislocations (in lattice-mismatch case) or an amorphous layer (in orientation-mismatch case) localized at the bonding interface with no defects generated in the bulk area. This approach is termed [expitaxial-like] ~~epitaxial-like~~ bonding. The epitaxial-like bonding can also be employed to prepare unique devices by integrating already processed device layers.--

Please amend the paragraph on page 3, beginning at line 24 as follows:

--These and other objects of the present invention are provided by a method for bonding first and second substrates including steps of preparing substantially oxide-free first and second surfaces of respective first and second substrates, creating a surface defect region in each of said first and second surfaces, and bonding said first and second surfaces. Creating the defective region may include plasma-treating the first and second surfaces of the first and second substrates with a plasma, and preferably a boron-containing plasma. The plasma-treating step may utilize a plasma in reactive ion etch (RIE) mode using B_2H_6 gas, and possibly a mixture of B_2H_6 , He, and Ar gases. Other gas plasmas, such as [Armay] Ar may also be used.--

Please amend the paragraph on page 13, beginning at line 14 as follows:

--A fourth embodiment of the present invention is to use As [(arseniic)] (arsenic) ion implantation to silicon wafers to form an amorphous layer on the wafer surface. Method steps for an As ion implantation treatment bonding process follow the steps shown in FIG. 1. After cleaning [and removing any oxide layer], As ion implantation is performed at an energy of 180 keV with a dose of $9 \times 10^{14}/\text{cm}^2$. Any oxide layer then is removed prior to bonding. The As doping concentration peak of $8 \times 10^{19}/\text{cm}^3$ is located at $\sim 1150 \text{ \AA}$ from the silicon surface. Although this implantation induced a very low As doping on the wafer surface, an amorphous layer with 1650 \AA thick was formed as confirmed both by a Monte Carlo simulation and TEM measurement (FIG. 10). The thickness of the amorphous layer can vary and is not limited to the value of this example. For instance, other ions may be implanted to create the amorphous layer. Arsenic is a dopant, and there are applications when it is desired not to dope the substrate so another ion, such as a non-doping ion like Ar, would be chosen.--

IN THE CLAIMS

44. (Amended) A bonded structure, comprising:

a first substrate having a first surface, a first [amorphous] ~~nearly-amorphized~~ layer formed in said first surface; and

a second substrate having a second surface, a second [amorphous] ~~nearly-amorphized~~ layer formed in said second surface;

said first surface being bonded to said second surface to form a bonded pair of substrates.

45. (Amended) A structure as recited in claim 44, comprising:

one of said first and second substrates of said bonded pair having a third surface, said third surface having [an amorphous] a ~~nearly-amorphized~~ layer;

a third substrate having a fourth surface, a fourth [amorphous] ~~nearly-amorphized~~ layer formed in said fourth surface; and

said third surface bonded to said fourth surface.

48. (Amended) A structure as recited in claim 44, wherein:

said first and second substrates comprise respective first and second semiconductor devices[;

said first surface comprises a substantially planar surface of a first silicon layer formed on said first device; and

said second surface comprises a substantially planar surface of a second silicon layer formed on said second device].

54. (Amended) A bonded structure, comprising:

a first substrate having an amorphized first surface, [and] ~~said first surface~~ containing boron;

a second substrate having an amorphized second surface, [and] said second surface containing boron; and

said first surface being bonded to said second surface to form a bonded pair of substrates.



Transaction History Date 2001-09-17
Date information retrieved from USPTO Patent
Application Information Retrieval (PAIR)
system records at www.uspto.gov



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Patent and Trademark Office

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/038,277	08/09/00	TONG	0 2025-0180-20
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022850 MM91/0917
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EXAMINER

DIAG. 1	
ART UNIT	PAPER NUMBER

2815
DATE MAILED: 09/17/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.

09/635,272

Applicant(s)

TONG, QIN-YI

Examiner

José R. Díaz

Art Unit

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 June 2001.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 44-108 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 44-108 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) Z. 6) ☐ Other:

DETAILED ACTION

Claim Objections

➤ Claim 80 is objected to because of the following informalities: the phrase -- covalent bonds-- should be added between "boron-boron" and "formed between..." Appropriate correction is required.

➤ The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claims 102-109 been renumbered 101-108. ***Claim Rejections - 35***

USC § 112

➤ The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

➤ Claims 68, 82, 101, and 103 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear to the Examiner the range of thickness claimed by Applicant. Correction is required.

Claim Rejections - 35 USC § 102

➤ The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

➤ Claims 44, 47, 50, 70-71, 74-75, 77, 81-82, 86, 88, 92, 95-96, 103 and 107 are rejected under 35 U.S.C. 102(b) as being anticipated by Takagi et al. ("Transmission Electron Microscope Observations of Si/Si Interface Bonded at Room Temperature by Ar Beam Surface Activation", Jpn. J. Appl. Phys. Vol. 38, Part 1, No. 3A, pp. 1589-1594, March 1999).

Regarding claims 44, 47, 50, 70-71, 74-75, 77, 81-82, 86, 88, 92, 95-96, 103 and 107, Takagi et al. teach a bonded structure (see pages 1589-1594) comprising: a first substrate having a first surface, a first nearly-amorphized layer formed in said first surface; and a second substrate having a second surface, a second nearly-amorphized layer formed in said second surface; said first surface being bonded to said second surface to form a bonded pair of substrates (see Figure 2). Furthermore, Takagi et al. teach that nearly-amorphized layers are formed in substantially oxide-free surfaces (see Figure 2).

Claim Rejections - 35 USC § 103

➤ The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

➤ Claims 44-108 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kish, Jr. et al. (US Patent No. 5,783,477) in view of Fujii et al. (US Patent No. 4,963,505).

Regarding claims 44, 47-48, 53-54, 58-59, 63-64, 66, 68-69, 74, 80-83, 86, 91-92, 95-96, and 100-105, Kish, Jr. et al. teach a bonded structure (see columns 1-10) comprising: a first substrate having a first surface (95), a first amorphous layer (91) formed in said first surface; and a second substrate having a second surface (93), a second amorphous layer (91) formed in said second surface; said first surface being bonded to said second surface to form a bonded pair of substrates (see Figure 9). Furthermore, Kish, Jr. et al. teach that the amorphous layers are formed by ion implantation (see col. 8, lines 22-25). However, Kish, Jr. et al. do not teach the type of impurities used to form the amorphous layer during the ion implantation step. Fujii et al. teach that is well known in the art to form nearly-amorphized layers by implanting ions (i.e. boron or arsenic) in a polycrystalline silicon layer (see col. 8, lines 61-65). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Kish, Jr. et al. to include the limitation of forming the nearly-amorphized layer by implanting boron or arsenic in a substrate comprised of a polysilicon layer. The ordinary artisan would have been motivated to modify Kish, Jr. et al. in the manner described above for at least the purpose of providing a semiconductor device that can operate effectively without being influenced by variations of the electric potential in the substrate.

Regarding claims 46, 55, 62, 73, 85 and 94, Kish, Jr. et al. teach that the substrates are selected from Si, InGaAs, InP, GaAs, Ge and SiC (see col. 3, lines 51-67).

Regarding claims 67, 70-71 and 75, Kish, Jr. et al. teach that the first and second surfaces are substantially oxide-free (see Figure 9).

Regarding claims 45, 60-61, 72, 84, and 93, it would have been obvious to one having ordinary skill in the art at the time the invention was made to bond additional substrates to the bonded structure since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8.

Regarding claims 49-52, 56-57, 65, 76-79, 87-90, 97-99 and 106-108 the claim(s) contain method of making characteristics (i.e. "exposed to a boron-containing plasma", "exposed to an inert gas plasma", "implanted with boron", and "implanted with arsenic") given no patentable weight in determining patentability of the final device structure. Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in

"product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear.

Response to Arguments

➤ Applicant's arguments with respect to claims 44-108 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

➤ Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (703) 308-6078. The examiner can normally be reached on 8:00 - 5:00 Monday through Fridays.

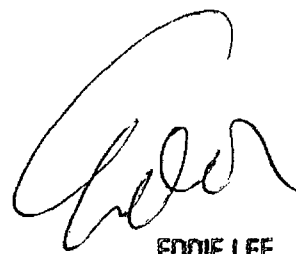
Application/Control Number: 09/635,272
Art Unit: 2815

Page 7

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JRD
September 10, 2001



EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Notice of References Cited	Application/Control No. 09/635,272	Applicant(s)/Patent Under Reexamination TONG, QIN-YI	
	Examiner José R. Díaz	Art Unit 2815	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number	Date	Name	Classification	
		Country Code-Number-Kind Code	MM-YYYY			
	A	US-4,963,505	10-1990	Fujii et al.	438	405
	B	US-				
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

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	N						
	O						
	P						
	Q						
	R						
	S						
	T						

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Interview Summary	Application No.	Applicant(s)	
	09/635,272	TONG, QIN-YI	
	Examiner	Art Unit	
	José R. Díaz	2815	

10
12/5/01

All participants (applicant, applicant's representative, PTO personnel):

- (1) José R. Díaz. (3) Carl Schlier.
 (2) Eddie Lee. (4) _____

Date of Interview: 05 December 2001.

Type: a) ☐ Telephonic b) ☐ Video Conference
 c) ☒ Personal [copy given to: 1) ☐ applicant 2) ☒ applicant's representative]

Exhibit shown or demonstration conducted: d) ☐ Yes e) ☒ No.
 If Yes, brief description: _____

Claim(s) discussed: 44-108.

Identification of prior art discussed: Takagi et al.; Kish, Jr. et al.; and Fujii et al.

Agreement with respect to the claims f) ☐ was reached. g) ☒ was not reached. h) ☐ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: Discussion focused on the outstanding grounds of rejection. Applicant argued the different between the structure of the references and the invention. Further, Applicant argued how the reference does not show a nearly amorphized layer.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

i) ☐ It is not necessary for applicant to provide a separate record of the substance of the interview/(if box is checked).

Unless the paragraph above has been checked, THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN ONE MONTH FROM THIS INTERVIEW DATE TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

Examiner Note: You must sign this form unless it is an Attachment to a signed Office action.

 Examiner's signature, if required

Docket No. 149840US-20
 IN RE APPLICATION OF: Qin-Yi TONG
 SERIAL NO: 09/635,272
 FILED: August 9, 2000
 FOR: A METHOD OF EPITAXIAL-LIKE WAFER BONDING AT LOW TEMPERATURE...

"RESPONSE UNDER 37 CFR 1.116-
 EXPEDITED PROCEDURE EXAMINING
 GROUP 2815"

ASSISTANT COMMISSIONER FOR PATENTS
 WASHINGTON, D.C. 20231

SIR:
 Transmitted herewith is an amendment in the above-identified application.

- ☒ No additional fee is required
- ☐ Small entity status of this application under 37 C.F.R. §1.9 and §1.27 is claimed.
- ☒ Additional documents filed herewith: Marked-Up Copy

The Fee has been calculated as shown below:

CLAIMS	CLAIMS REMAINING		HIGHEST NUMBER PREVIOUSLY PAID	NO. EXTRA CLAIMS	RATE	CALCULATIONS
TOTAL	61	MINUS	66	0	× \$18 =	\$0.00
INDEPENDENT	6	MINUS	6	0	× \$84 =	\$0.00
		<input type="checkbox"/> MULTIPLE DEPENDENT CLAIMS			+ \$280 =	\$0.00
		TOTAL OF ABOVE CALCULATIONS				\$0.00
		<input type="checkbox"/> Reduction by 50% for filing by Small Entity				\$0.00
		<input type="checkbox"/> Recordation of Assignment			+ \$40 =	\$0.00
		TOTAL				\$0.00

- ☐ A check in the amount of _____ is attached.
- ☒ Please charge any additional Fees for the papers being filed herewith and for which no check is enclosed herewith, or credit any overpayment to deposit Account No. 15-0030. A duplicate copy of this sheet is enclosed.
- ☒ If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time may be charged to Deposit Account No. 15-0030. A duplicate copy of this sheet is enclosed.



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 MAIER & NEUSTADT, P.C.

Carl E. Schlier

Eckhard H. Kuesters
 Registration No. 28,870

Carl E. Schlier
 Registration No. 34,426

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"RESF SE UNDER 37 CFR 1.116-
EXPEL...D PROCEDURE EXAMINING
GROUP 2815"

149840US-20

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF:

QIN-YI TONG

: EXAMINER: J. DIAZ

SERIAL NO: 09/635,272

FILED: AUGUST 9, 2000

: GROUP ART UNIT: 2815

FOR: METHOD OF EPITAXIAL-LIKE :
WATER BONDING AT LOW
TEMPERATURE AND
BONDED STRUCTURE

AMENDMENT UNDER 37 CFR §1.116

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Responsive to the Office Action dated September 17, 2001, please amend the above-identified application as follows:

IN THE CLAIMS

Please cancel claims 50, 77, 88, 98 and 108 without prejudice.

Please amend the claims as shown in the marked-up copy to read as follows:

1. 41. (Twice Amended) A bonded structure, comprising:
- a first substrate having a first surface, a first nearly-amorphized layer containing one of boron and arsenic formed uniformly over said first surface; and
 - a second substrate having a second surface, a second nearly-amorphized layer containing one of boron and arsenic formed uniformly over said second surface;

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B¹
said first surface being bonded to said second surface to form a bonded pair of substrates.

B²
15. ~~54~~. (Amended) A bonded structure, comprising:
a first substrate having a first surface, substantially all of said first surface being amorphized and containing boron;

a second substrate having a second surface, substantially all of said second surface being amorphized and containing boron; and

said first surface being bonded to said second surface to form a bonded pair of substrates.

B³
22. ~~54~~. (Amended) A bonded structure, comprising:
a first substrate having a first surface, a first amorphous arsenic-containing layer formed in substantially all of said first surface; and

a second substrate having a second surface, a second amorphous arsenic-containing layer formed in substantially all of said second surface;

said first surface being bonded to said second surface to form a bonded pair of substrates.

B⁴
33. ~~70~~. (Amended) A bonded structure, comprising:
a first substrate having a substantially oxide-free first surface, a substantial portion of said first surface being amorphized and containing one of boron and arsenic; and

a second substrate having a substantially oxide-free second surface, a substantial portion of said first surface being amorphized and containing one of boron and arsenic;

said first surface being bonded to said second surface to form a bonded pair of substrates.

B⁵
33. ~~91~~. (Amended) A bonded structure, comprising:

25
a first substrate of substantially one first material amorphized substantially only in a first surface of said first material and containing one of boron and arsenic; and

a second substrate of substantially one second material amorphized substantially only in a second surface of said second material and containing one of boron and arsenic;

said first surface being bonded to said second surface to form a bonded pair of substrates.

REMARKS

Favorable reconsideration of this application is respectfully requested.

Claims 44-49, 51-76, 78-87, 89-97 and 99-109 are now present in this application, claims 50, 77, 88, 98 and 108 being canceled by way of the present amendment. Claims 68, 82, 101 and 103 stand rejected under 35 U.S.C. §112, second paragraph. Claims 44, 47, 50, 70, 71, 74, 75, 77, 81, 82, 86, 88, 92, 95, 96, 103 and 107 stand rejected under 35 U.S.C. §102(b) as anticipated by Takagi et al. Claims 44-108 stand rejected over U.S. 5,783,477 (Kish, Jr. et al) in view of U.S. 4,963,505 (Fujii et al).

The §112 rejection is based on lack of definiteness regarding the recited range. The word "few" appears to be the source. A "few" is an easily understood value. One skilled in the art would not be confused by what constitutes, for example, a few nm. Withdrawal of this rejection is respectfully requested.

The Applicants greatly appreciate the interview with Examiner Diaz, and his supervisor Mr. Lee. During the interview the differences between the claimed invention and the prior art was discussed in detail. Specifically, Kish, Jr. et al (hereafter "Kish"), discloses layer 95 formed on the semiconductor layer and amorphous or polycrystalline regions 91 formed in a layer 95. Regions 91 are formed by selective patterning (see column 8, lines 18-

32) and are useful to direct current flow through the bonded structure (see FIG. 9). As pointed out in column 8, lines 25-32, the areas where regions 91 meet create non-ohmic contact regions. As the main purpose of Kish is to form an ohmic contact (see the Abstract, for example), one skilled in the art would clearly not form regions 91 uniformly over the surface or over a substantial portion of the surface since the resulting large or complete non-ohmic contact would defeat the whole purpose of trying to form an ohmic contact.

There was some questions raised by Examiners Diaz and Lee over the terms like “substantial” and “uniform” regarding support in the specification and definiteness. The description clearly shows the treatment to produce the amorphized or nearly-amorphized surfaces, such as the non-limiting example of FIG. 2 where surface 202 extends over a substantial portion of the substrate. The support is clear. A term like “substantial” is very often used in this art recognizing that “substantially” is accurate as there may be some incompleteness or nonuniformity due to the realities of physical materials, or the presence of some structure or material on the surface preventing completeness or absoluteness. Terms like “substantial” as used in the claims are definite and convey the subject matter of the invention sought to be protected to one skilled in the art.

Clearly, in Kish, there is no suggestion of any nearly-amorphized layer in claim 44, the amorphized surface of claim 54, the amorphous layer of claim 59, the amorphized surface of claim 70, or the surface of claim 92. Kish does not suggest the claimed surfaces but clearly only has specific regions containing amorphous or polycrystalline material to direct current flow.

The Fujii et al patent is only offered to teach implanting certain species. Even if this reference could be combined with Kish, only the same regions in Kish would result. The combination also does not suggest the claimed invention.

The pending claims as amended above were also not rejected over Takagi et al. The pending claims are patentable over Takagi et al.

Claim 81 recites the depth of the region to be a few nm, which has not been shown in any reference or is even discussed in the Office Action. The Office Action demonstrates that the burden of showing every element of claim 81 to be disclosed or suggested by the prior art has not been met. Thus, allowance of claim 81 is in order.

The present amendment is submitted under the provisions of 37 CFR §1.116 governing the entry of amendments after final rejection. As stated in MPEP §712.14, amendments placing an application in condition for allowance may be entered. The amendments above are believed to place the application in condition for allowance. Also, Examiners Diaz and Lee recognized that there were issues regarding the appropriateness of the rejections based upon the language of the claims pending before the issuance of this Office Action, such as claim 83 reciting a substantial portion and claim 81 reciting a depth of the regions. Closing examination at this point does not appear to be warranted.

It is respectfully submitted that the present application is in condition for allowance and a favorable decision to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Eckhard H. Kuesters
Registration No. 28,870
Carl E. Schlier
Registration No. 34,426
Attorneys of Record



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149840US-20

Marked-Up Copy
Serial No: 09/635,272
Amendment Filed

12-7-01

IN THE CLAIMS

44. (Twice Amended) A bonded structure, comprising:

a first substrate having a first surface, a first nearly-amorphized layer containing one of boron and arsenic formed [in] uniformly over said first surface; and

a second substrate having a second surface, a second nearly-amorphized layer containing one of boron and arsenic formed [in] uniformly over said second surface;

said first surface being bonded to said second surface to form a bonded pair of substrates.

54. (Amended) A bonded structure, comprising:

a first substrate having [an amorphized] a first surface, substantially all of said first surface being amorphized and containing boron;

a second substrate having [an amorphized] a second surface, substantially all of said second surface being amorphized and containing boron; and

said first surface being bonded to said second surface to form a bonded pair of substrates.

59. (Amended) A bonded structure, comprising:

a first substrate having a first surface, a first amorphous arsenic-containing layer formed in substantially all of said first surface; and

a second substrate having a second surface, a second amorphous arsenic-containing layer formed in substantially all of said second surface;

said first surface being bonded to said second surface to form a bonded pair of substrates.

70. (Amended) A bonded structure, comprising:

a first substrate having [an amorphized] a substantially oxide-free first surface, a substantial portion of said first surface being amorphized and containing one of boron and arsenic; and

a second substrate having [an amorphized] a substantially oxide-free second surface, a substantial portion of said first surface being amorphized and containing one of boron and arsenic;

said first surface being bonded to said second surface to form a bonded pair of substrates.

92. (Amended) A bonded structure, comprising:

a first substrate of substantially one first material amorphized substantially only in a first surface of said first material and containing one of boron and arsenic; and

a second substrate of substantially one second material amorphized substantially only in a second surface of said second material and containing one of boron and arsenic;

said first surface being bonded to said second surface to form a bonded pair of substrates.



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14

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/635,272	08/09/2000	Qin-Yi Tong	2025-0180-20	5012

22850 7590 12/21/2001

OBLON SPIVAK MCCLELLAND MAIER & NEUSTADT PC
FOURTH FLOOR
1755 JEFFERSON DAVIS HIGHWAY
ARLINGTON, VA 22202

EXAMINER

DIAZ, JOSE R

ART UNIT	PAPER NUMBER
----------	--------------

2815

DATE MAILED: 12/21/2001

12

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Application No. 09/635,272	Applicant(s) TONG, QIN-YI	
	Examiner José R. Díaz	Art Unit 2815	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 07 December 2001 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

- a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
- b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection. ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.
2. ☒ The proposed amendment(s) will not be entered because:
- (a) ☒ they raise new issues that would require further consideration and/or search (see NOTE below);
 - (b) ☐ they raise the issue of new matter (see Note below);
 - (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
 - (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: See Continuation Sheet.

3. ☐ Applicant's reply has overcome the following rejection(s): _____.
4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
5. ☐ The a) ☐ affidavit, b) ☐ exhibit, or c) ☐ request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____.
6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.
7. ☒ For purposes of Appeal, the proposed amendment(s) a) ☒ will not be entered or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

The status of the claim(s) is (or will be) as follows:


Claim(s) allowed: _____.

Claim(s) objected to: _____.

Claim(s) rejected: 44-108.

Claim(s) withdrawn from consideration: _____.

8. ☐ The proposed drawing correction filed on _____ is a) ☐ approved or b) ☐ disapproved by the Examiner.
9. ☐ Note the attached Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
10. ☐ Other: _____


 EDDIE LEE
 SUPERVISORY PATENT EXAMINER
 TECHNOLOGY CENTER 2800

Continuation Sheet (PTO-303)
09/635,272

Application No.

Continuation of 2. NOTE: The limitation regarding the amorphized substrate in the claimed device, as presented in the amendment, sets forth subject matter which was not considered in the finally rejected claim and hence presents new issues which require further consideration and/or search.

Docket No. 149840US20



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Qin-Yi TONG

SERIAL NO: 09/635,272

GAU: 2815

FILED: August 9, 2000

EXAMINER: DIAZ, J.

FOR: A METHOD OF EPITAXIAL-LIKE WAFER BONDING AT LOW TEMPERATURE AND BONDED STRUCTURE

✓ 28/159
#13 IDS
1-8-02
Ratko

INFORMATION DISCLOSURE/RELATED CASE STATEMENT UNDER 37 CFR 1.97

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Applicant(s) wish to disclose the following information.

REFERENCES

- The applicant(s) wish to make of record the references cited in the attached PCT International Search Report listed on the attached form PTO-1449. Copies of the listed references are attached, where required, as are either statements of relevancy or any readily available English translations of pertinent portions of any non-English language references.
- A check is attached in the amount required under 37 CFR §1.17(p).

RELATED CASES

- ☐ Attached is a list of applicant's pending application(s) or issued patent(s) which may be related to the present application. A copy of the patent(s), together with a copy of the claims and drawings of the pending application(s) is attached along with PTO 1449.
- ☐ A check is attached in the amount required under 37 CFR §1.17(p).

CERTIFICATION

- Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.
- ☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

- Please charge any additional fees for the papers being filed herewith and for which no check is enclosed here with, or credit any overpayment to deposit account number 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Eckhard H. Kuesters
Registration No. 28,870

Carl E. Schlier
Registration No. 34,426

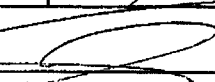
James D. Hamilton
Registration No. 28,421



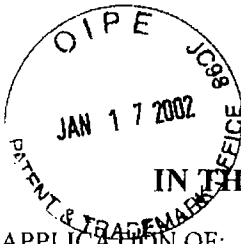
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(OSMMN 10/98)

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Form PTO 1449 (Modified)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY DOCKET NO. 149840US20		SERIAL NO. 09/635,272	
LIST OF REFERENCES CITED BY APPLICANT DEC 26 2001				APPLICANT Qin-Yi TONG			
				FILING DATE August 9, 2000		GROUP 2815	
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA	5,783,477	7/21/98	Kish, Jr. et al.			
	AB	4,963,505	10/16/90	Fujii et al.			
	AC	6,246,068	6/12/01	Sato et al.			
	AD	6,255,731	7/3/01	Ohmi et al.			
	AE	6,143,628	11/7/00	Sato et al.			
	AF	6,120,917	9/19/00	Eda			
	AG						
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	AN						
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES NO		
	AO						
	AP						
	AQ						
	AR						
	AS						
	AT						
	AU						
	AV						
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)							
	AW						
	AX						
	AY						
	AZ						
Examiner: 					Date Considered: 4/8/02		

*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



Docket No.: C149840US-20

RCE/281
A

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Qin-Yi TONG

GAU: 2815

SERIAL NO: 09/635,272

EXAMINER: Jose DIAZ

#15/PCE
2/6/2
Gurles

FILED: August 9, 2000

FOR: A METHOD OF EPITAXIAL-LIKE WAFER BONDING...

REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

This is a request for Continued Examination (RCE) under 37 C.F.R. §1.114 of the above-identified application.

Submission required under 37 C.F.R. §1.114

Previously Submitted:

- ☒ Consider the amendment(s)/reply under 37 C.F.R. §1.116 previously filed on December 7, 2001
- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on

Enclosed:

- ☐ Amendment/Reply
- ☐ Information Disclosure Statement (IDS)
- ☐ Other:

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FEES	RATE	CALCULATIONS
<input type="checkbox"/> Suspension of action on the above-identified application is requested under 37 C.F.R. §1.103(c) for a period of months.	\$130.00	\$0.00
<input checked="" type="checkbox"/> RCE Fee required under 37 C.F.R. §1.17(e)	\$740.00	\$740.00
<input checked="" type="checkbox"/> A ONE MONTH EXTENSION OF TIME IS REQUESTED		\$110.00
TOTAL OF ABOVE CALCULATIONS:		\$850.00
<input checked="" type="checkbox"/> REDUCTION BY 50% FOR FILING AS SMALL ENTITY		\$-425.00
TOTAL:		\$425.00

☐ A check in the amount of \$0.00 is enclosed

☒ Please charge any additional Fees for the papers being filed herewith and for which no check is enclosed herewith, or credit any overpayment to Deposit Account No. 15-0030. A duplicate copy of this sheet is enclosed.

☒ If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 CFR 1.136, and any additional fees required under 37 CFR 1.136 for any necessary extension of time may be charged to Deposit Account No. 15-0030. A duplicate of this sheet is enclosed.

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Respectfully Submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

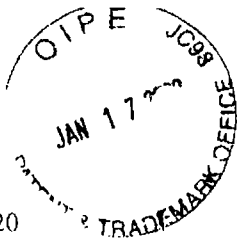
Eckhard H. Kuesters

Registration No. 28,870

Carl E. Schlier

Registration No. 34,426

TSMC1002



Docket No. 149840US-20

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Qin-Yi TONG

GAU: 2815

SERIAL NO: 09/635,272

EXAMINER: J. DIAZ

FILED: August 9, 2000

FOR: A METHOD OF EPITAXIAL-LIKE WAFER BONDING

REQUEST FOR EXTENSION OF TIME
UNDER 37 C.F.R. 1.136

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

It is hereby requested that a one month extension of time be granted to **January 17, 2002** for

- ☐ filing a response to the Official Action dated:
- ☐ responding to the requirements in the Notice of Allowability dated:
- ☐ filing the Formal Drawings. The Issue Fee due has been timely filed.
- ☐ responding to the Notice to File Missing Parts of Application dated:
- ☒ filing an RCE. A timely response to the final rejection, due December 17, 2001 has been filed.
- ☐ filing an Appeal Brief. A Notice of Appeal was filed on:
- ☒ Applicant claims small entity status. See 37 CFR 1.27. Therefore, the fee amount shown below is reduced by one half.

The required fee of \$55.00 is enclosed herewith by check and any further charges may be made against the Attorney of Record's Deposit Account No. **15-0030**. A duplicate copy of this sheet is enclosed.

Respectfully Submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Eckhard H. Kuesters
Registration No. 28,870

Carl E. Schlier
Registration No. 34,426



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/635,272	08/09/2000	Qin-Yi Tong	2025-0180-20	5012

22850 7590 04/10/2002

OBLON SPIVAK MCCLELLAND MAIER & NEUSTADT PC
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1755 JEFFERSON DAVIS HIGHWAY
ARLINGTON, VA 22202

EXAMINER

DIAZ, JOSE R

ART UNIT	PAPER NUMBER
----------	--------------

2815

DATE MAILED: 04/10/2002

16

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/635,272	TONG, QIN-YI	
	Examiner	Art Unit	
	José R. Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 January 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 44-49, 51-76, 78-87, 89-97 and 99-107 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 44-49, 51-76, 78-87, 89-97 and 99-107 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No.'s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>13</u> . | 6) <input type="checkbox"/> Other: |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

➤ A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on December 7, 2001 has been entered.

Claim Rejections - 35 USC § 112

➤ The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

➤ Claims 64 and 75 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 64-65 recite the limitation "said first device". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

➤ The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

➤ Claims 81-83 and 85-86 rejected under 35 U.S.C. 102(b) as being anticipated by Kish, Jr et al. (US Patent No. 5,783,477).

Regarding claims 81-83, Kish, Jr. et al. teach a bonded structure (see columns 1-10) comprising: a first substrate having a first surface (95), a first amorphous layer (91) formed in said first surface; and a second substrate having a second surface (93), a second amorphous layer (91) formed in said second surface; said first surface being bonded to said second surface to form a bonded pair of substrates (see Figure 9). Furthermore, Kish, Jr. et al. teach that the amorphous layers are formed by ion implantation (see col. 8, lines 22-25).

Regarding claims 85-86, Kish, Jr. et al. teach that the substrates are selected from Si, InGaAs, InP, GaAs, Ge and SiC (see col. 3, lines 51-67).

Claim Rejections - 35 USC § 103

➤ The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

➤ Claims 44-48, 52, 59-75, 78-79, 81-86, 89-90, 92-96, 99-101, 103-104, and 107 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takagi et al. ("Transmission Electron Microscope Observations of Si/Si Interface Bonded at Room Temperature by Ar Beam Surface Activation", Jpn. J. Appl. Phys. Vol. 38, Part 1, No. 3A, pp. 1589-1594, March 1999) in view of Fujii et al. (US Patent No. 4,963,505).

Regarding claims 44 and 52, 59, 61, 64-71, 75, 78-79, 81-83, 89-90, 92, 99-101, 103-104, and 107, Takagi et al. teach a bonded structure (see pages 1589-1594) comprising: a first substrate having a first surface, a first nearly-amorphized layer formed in said first surface; and a second substrate having a second surface, a second nearly-amorphized layer formed in said second surface; said first surface being bonded to said second surface to form a bonded pair of substrates (see Figs. 2-3 and "Discussion" on pages 1591-1593). Furthermore, Takagi et al. teach that nearly-amorphized layers are formed in substantially oxide-free surfaces (see Figure 2). However, Takagi et al. fails to teach first and second nearly-amorphized layers containing one of boron and arsenic. Fujii et al. teach that is well known in the art to form nearly-amorphized layers by implanting ions (i.e. arsenic) in a polycrystalline silicon layer (see col. 8, lines 61-65). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Takagi et al. to include the limitation of incorporating arsenic ions in a surface of a substrate such that a nearly-amorphized layer is created in the substrate. The ordinary artisan would have been motivated to modify Takagi et al. in the manner described above for at least the purpose of providing a semiconductor device that can operate effectively without being influenced by variations of the electric potential in the substrate.

Regarding claims 45, 60, 72, 84, and 93, the combination Takagi et al. in view of Fujii et al. discloses the claimed invention except for the duplication of part in which an additional nearly-amorphized substrate is bonded to a previous bonded structure. It

would have been obvious to one having ordinary skill in the art at the time the invention was made to bond additional nearly-amorphized substrates since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8.

Regarding claims 46-47, 62-63, 73-74, 85-86, and 94-96, Takagi et al. teach that the substrates are formed of Si (see pages 1589-1593).

Regarding claims 48, Takagi et al. teach that the first and second substrates comprise respective first and second semiconductor devices (see Introduction and Experimental on pages 1589-1590).

➤ Claims 44-49, 51-76, 78-87, 89-97, and 99-107 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takagi et al. ("Transmission Electron Microscope Observations of Si/Si Interface Bonded at Room Temperature by Ar Beam Surface Activation", *Jpn. J. Appl. Phys.* Vol. 38, Part 1, No. 3A, pp. 1589-1594, March 1999) in view of Yamazaki et al. (US Patent No. 6,153,455).

Regarding claims 44 and 49, 51-54, 56-59, 61, 64-71, 75-76, 78-83, 87, 89-92, 97, and 99-107, Takagi et al. teach a bonded structure (see pages 1589-1594) comprising: a first substrate having a first surface, a first nearly-amorphized layer formed in said first surface; and a second substrate having a second surface, a second nearly-amorphized layer formed in said second surface; said first surface being bonded to said second surface to form a bonded pair of substrates (see Figs. 2-3 and "Discussion" on pages 1591-1593). Furthermore, Takagi et al. teach that nearly-amorphized layers are formed in substantially oxide-free surfaces (see Figure 2).

However, Takagi et al. fails to teach first and second nearly-amorphized layers containing one of boron and arsenic. Yamazaki et al. teach that is well known in the art to form nearly-amorphized layers by adding B ions by ion implantation or plasma doping in the silicon layer (see col. 3, lines 45-50 and col. 10, lines 6-10). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Yamazaki et al. to include the limitation of incorporating boron ions in a surface of a substrate such that a nearly-amorphized layer is created in the substrate. The ordinary artisan would have been motivated to modify Yamazaki et al. in the manner described above for at least the purpose of providing a semiconductor device that can operate effectively without being influenced by variations of the electric potential in the substrate.

Regarding claims 45, 60, 72, 84, and 93, the combination Takagi et al. in view of Yamazaki et al. discloses the claimed invention except for the duplication of part in which an additional nearly-amorphized substrate is bonded to a previous bonded structure. It would have been obvious to one having ordinary skill in the art at the time the invention was made to bond additional nearly-amorphized substrates since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8.

Regarding claims 46-47, 55, 62-63, 73-74, 85-86, and 94-96, Takagi et al. teach that the substrates are formed of Si (see pages 1589-1593).

Application/Control Number: 09/635,272
Art Unit: 2815

Page 7

Regarding claims 48, Takagi et al. teach that the first and second substrates comprise respective first and second semiconductor devices (see Introduction and Experimental on pages 1589-1590).

Response to Arguments

➤ Applicant's arguments with respect to claims 44-49, 51-76, 78-87, 89-97, 99-107 have been considered but are moot in view of the new ground(s) of rejection.

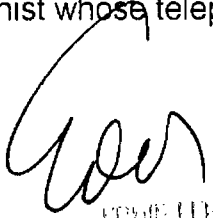
Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (703) 308-6078. The examiner can normally be reached on 9:00 - 5:00 Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 746-3891 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 303-0956.

JRD
April 8, 2002

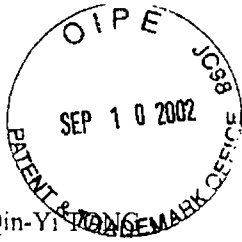

EDDIE C. LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1800

Notice of References Cited	Application/Control No. 09/635,272	Applicant(s)/Patent Under Reexamination TONG, QIN-YI	
	Examiner José R. Díaz	Art Unit 2815	Page 1 of 1

U.S. PATENT DOCUMENTS					
*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,153,445	11-2000	Yamazaki et al.	439/158
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS					
*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name Classification
	N				
	O				
	P				
	Q				
	R				
	S				
	T				

NON-PATENT DOCUMENTS		
*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	



2815
48

Docket No. 149840US20
IN RE APPLICATION OF: Qin-Yi TONG
SERIAL NO: 09/635,272
RCE FILED: January 17, 2002
FOR: A METHOD OF EPITAXIAL-LIKE WAFER BONDING AT LOW TEMPERATURE

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:
Transmitted herewith is an amendment in the above-identified application.

- ☐ No additional fee is required
☒ Small entity status of this application under 37 C.F.R. §1.9 and §1.27 is claimed.
☒ Additional documents filed herewith: Marked-Up Copy, Request for Extension of Time (2 Months)

The Fee has been calculated as shown below:

CLAIMS	CLAIMS REMAINING		HIGHEST NUMBER PREVIOUSLY PAID	NO. EXTRA CLAIMS	RATE	CALCULATIONS
TOTAL	61	MINUS	61	0	x \$18 =	\$0.00
INDEPENDENT	6	MINUS	6	0	x \$84 =	\$0.00
		<input type="checkbox"/> MULTIPLE DEPENDENT CLAIMS			+ \$280 =	\$0.00
		TOTAL OF ABOVE CALCULATIONS				\$0.00
		<input checked="" type="checkbox"/> Reduction by 50% for filing by Small Entity				\$0.00
		<input type="checkbox"/> Recordation of Assignment			+ \$40 =	\$0.00
		TOTAL				\$0.00

- ☒ A check in the amount of **\$200.00** is attached.
☒ Please charge any additional Fees for the papers being filed herewith and for which no check is enclosed herewith, or credit any overpayment to deposit Account No. 15-0030. A duplicate copy of this sheet is enclosed.
☒ If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time may be charged to Deposit Account No. 15-0030. A duplicate copy of this sheet is enclosed.



22850

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Carl E. Schlier

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Registration No. 28,870
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Registration No. 34,426

TECHNICAL
REVIEW
10/10/02



149840US-20

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF:

QIN-YI TONG

: EXAMINER: J. DIAZ

SERIAL NO: 09/635,272

:

RCE FILED: JANUARY 17, 2002

: GROUP ART UNIT: 2815

FOR: METHOD OF EPITAXIAL-LIKE :
WATER BONDING AT LOW
TEMPERATURE AND
BONDED STRUCTURE

#18/Amended
A round
9/17/02

AMENDMENT

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Responsive to the Office Action dated April 10, 2002, please amend the
above-identified application as follows:

IN THE CLAIMS

Please amend the claims as shown in the marked-up copy to read as follows:

27. 64. (Amended) A structure as recited in claim 59, wherein:

said first surface comprises a substantially planar surface of a first arsenic-containing
silicon layer formed on said first substrate; and

said second surface comprises a substantially planar surface of a second arsenic-
containing silicon layer formed on said second substrate.

38. 75. (Amended) A structure as recited in claim 70, wherein:

C2
Cust
said first surface comprises a substantially planar surface of a first amorphous
substantially oxide-free silicon layer formed on said first substrate; and

said second surface comprises a substantially planar surface of a second amorphous
substantially oxide-free silicon layer formed on said second substrate.

REMARKS

Favorable reconsideration of this application is respectfully requested.

Claims 44-109 are present in this application. Claims 64 and 75 stand rejected under 35 U.S.C. §112, second paragraph. Claims 81-83, 85 and 86 stand rejected under 35 U.S.C. §102(b) as anticipated by U.S. 5,783,477 (Kish, Jr. et al). Under 35 U.S.C. §103(a), claims 44-48, 52, 59-75, 78, 79, 81-86, 89, 90, 92-96, 99-101, 103, 104 and 107 stand rejected over the article by Takagi et al in view of U.S. 4,963,505 (Fujii et al), and claims 44-49, 51-76, 78, 87, 89-97 and 99-107 stand rejected over Takagi et al in view of U.S. 6,153,455 (Yamazaki et al).

Claims 64 and 75 have been amended to provide clear antecedent basis, correcting an formal error. Withdrawal of the §112 rejection is respectfully requested.

In the §102 rejection over Kish, Jr. et al (hereafter "Kish"), the Office Action describes Kish as having two substrates bonded together with amorphous "layers" 91 formed in the surface of each substrate. However, the Office Action fails to point out how Kish discloses a substrate with an amorphous region "extending only one to a few monolayers" into each of the first and second substrates as recited in each of claims 81-83, 85 and 86. In order to reject a claim under §102, a reference *must* disclose *every* element of a claim. Without any assertion in the Office Action (or any explanation at all) how Kish discloses an amorphous region extending only a few monolayers into the first and second substrates, the rejection

must be withdrawn. Moreover, Kish teach that amorphous elements 91 are formed by laser annealing or by ion implantation, both of which would likely produce an element 91 extending deeper than one to a few monolayers into the surface. Figure 9 also establishes that Kish teaches that elements 91 will be deeper than a few monolayers. As there is no disclosure of every element of claims 81-83, 85 and 86 in Kish, withdrawal of the §102 rejection of claims 81-83, 85 and 86 is required, and is respectfully requested.

Before addressing the §103(a) rejections, the Applicant would like to provide the following brief discussion. In the claims rejected under §103(a), the surface of a substrate contains an amorphous or nearly amorphized layer containing B or As. In one non-limiting example, B is present in an amorphous surface layer. The bonding energy is enhanced at low temperatures, producing a strong bond between substrates. B may also promote the removal of H from the bonding surfaces, also enhancing the bonding strength at low temperature.

Turning now to the §103(a) rejections, the Takagi et al. article describes the observations of silicon-silicon interface bonding utilizing Ar beam sputter etching. As described on page 1589, an Ar beam applied to the surface, sputter-etching the surface. Using an Ar beam "removes contamination on the specimen surface." *Id.* Instead if the surface is treated using wet chemicals (HNO_3 , $\text{H}_2\text{SO}_4 + \text{H}_2\text{O}_2$, etc.), a thin oxide or sub-oxide layer may be formed at the bonding interface. *Id.* In another wet treatment (HF), small amount impurities are formed on the surface, such as hydrocarbons which produce a rough surface and small precipitates. *Id.* Clearly, the Ar sputtering in Takagi et al. is designed to clean the surface to promote bonding. Importantly, Takagi et al. suggests no other type of ion beam etching to clean the surface to facilitate bonding. Only Ar is mentioned. There is also no suggestion that another type of beam would be a suitable substitute for the Ar beam.

The Office Action looks to two other references to provide a suggestion for using As

or B implantation as a substitute for the Ar sputter etch of Takagi et al in a bonded structure. However, there is no mention of cleaning substrate surfaces using As or B implantations in these two references, nor is there any mention of the As or B implantation being a substitute for Ar sputter etching. The purpose of the As and B implantations is not to clean the surface, but is to form active regions in a semiconductor device or as a precursor for forming polycrystalline or single crystalline films. To support the arguments in the Office Action, identification of a suggestion that As or B implantation is a substitute for Ar sputter etch, or a suggestion of amorphous layers formed by the As or B implants in a bonded structure is needed. There is no such suggestions in either reference, which will be discussed in more detail below.

The Office Action points to column 8, lines 61-65 of Fujii et al. This portion describes an amorphous silicon layer 16 which may be formed by implanting ions such as silicon, arsenic, phosphorous. Layer 16 is formed on substrate 1 and oxide film 2.

Layer 16 is then subjected to a thermal treatment at a temperature of 500-1100°C, to form a solid phase epitaxial growth layer (column 8, lines 32-40). The portion 16a is reduced to a single crystal silicon and the portion 16b covering the oxide film 2 is reduced to polycrystalline silicon. When this structure is bonded, as shown in Fig. 1(e), the amorphous silicon layer 16 is no longer present. Instead the single crystal layer 16a and the polycrystalline layer 16b are present.

Fujii et al does teach one skilled in the art to form an amorphous layer as a precursor for forming a film having a combination single-crystal and polycrystalline component. Fujii et al also teaches that the amorphous layer may be produced by forming a polycrystalline layer and implanting the polycrystalline layer. However, there is no suggestion of an amorphous layer in a bonded structure. The amorphous layer is intentionally thermally treated to form

single-crystal and poly-crystal layers, and is not present in a bonded structure.

Moreover, there is no suggestion that the implantation to form the amorphous layer would be used for a surface cleaning operation and substitution for the Ar sputter etch of Takagi et al, nor is there any suggestion of an amorphous region or layer in a bonded device. The amorphous layer is specifically converted out of the amorphous state into a poly-crystalline or single-crystalline state prior to any bonding. To the contrary, Fujii et al teaches away from using amorphous layers in a bonded structure.

The Office Action has simply pointed to the idea of forming an amorphous layer on top of a silicon substrate through the use of the ion implantation. This teaching falls short of suggesting to one skilled in the art, when armed with the teachings of Takagi et al, to use As or B implantation instead of the Ar sputter etch. Nothing in either reference suggests that the implantation would be used for Ar sputter etch, or implantation would be a suitable substitute. Accordingly, the §103(a) rejection over Takagi et al combined with Fujii et al must be withdrawn.

In Yamazaki et al, an amorphous layer 102 is formed on a quartz substrate 101 by low pressure CVD or plasma CVD. Diborane is introduced into the film forming gas to dope amorphous silicon film 102. Subsequently, amorphous silicon film 102 is crystallized, and transistor formation steps are carried out including ion implantation to form source and drain regions. The Office Action mentions the ion implantation for threshold voltage control in column 3, lines 45-50. However, there is no discussion of forming an amorphous layer in a bonded structure, or any suggestion that the ion implantation for the threshold voltage control would be substituted for an Ar sputter etch for cleaning the surface of the substrate. Importantly, the amorphous silicon film again is intentionally re-crystallized since the purpose here is to form a transistor device. Yamazaki et al also teaches away from

amorphous layers remaining in the structure.

The Office Action also mentions column 10, lines 6-10 of Yamazaki et al. These lines discuss introducing boron by using diborane in forming an amorphous silicon film. These lines also mention the amorphous silicon film may be doped by ion implantation. However, there is no suggestion of forming an amorphous layer for a bonded structure. As mentioned above the amorphous silicon film is re-crystallized to form transistor devices. These lines also make no suggestion of using ion implantation for an Ar sputter etch in Takagi et al.

Nothing in Yamazaki et al. mentions any connection with forming an amorphous layer for a bonded structure, or any type of process which would be used to clean a surface of a substrate by ion implantation. There is clearly no suggestion that forming an amorphous layer and re-crystallizing it, or the teaching of threshold voltage control by implantation would suggest to one skilled in the art to substitute ion implantation for the argon sputter etch of Takagi et al.

There is no suggestion in Yamazaki et al. of an amorphous layer formed by ion implantation that would be used in the structure taught by Takagi et al. Without such a suggestion the combination is defective, and the §103(a) rejection over Takagi et al. and Yamazaki et al. must be withdrawn.

It is respectfully submitted that the present application is in condition for allowance and a favorable decision to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Eckhard H. Kuesters
Registration No. 28,870

Carl E. Schlier
Registration No. 34,426
Attorneys of Record



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149840US-20

<p>Marked-Up Copy Serial No: 09/635,272 Amendment Filed on: September 10, 2002</p>

Please amend the claims as follows:

IN THE CLAIMS

64. (Amended) A structure as recited in claim 59, wherein:

said first surface comprises a substantially planar surface of a first arsenic-containing silicon layer formed on said first [device] substrate; and

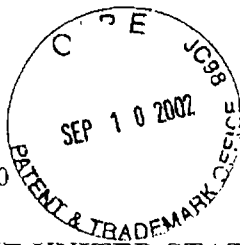
said second surface comprises a substantially planar surface of a second arsenic-containing silicon layer formed on said second [device] substrate.

75. (Amended) A structure as recited in claim 70, wherein:

said first surface comprises a substantially planar surface of a first amorphous substantially oxide-free silicon layer formed on said first [device] substrate; and

said second surface comprises a substantially planar surface of a second amorphous substantially oxide-free silicon layer formed on said second [device] substrate.

Docket No. 149840US20



#137/Ext 17
(2 mos)
A. R. Diaz
9/17/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Qin-Yi TONG

GAU: 2815

SERIAL NO: 09/635,272

EXAMINER: Jose R. DIAZ

RCE FILED: January 17, 2002

FOR: A METHOD OF EPITAXIAL-LIKE WAFER BONDING AT LOW TEMPERATURE

REQUEST FOR EXTENSION OF TIME
UNDER 37 C.F.R. 1.136

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

It is hereby requested that a **two** month extension of time be granted to September 10, 2002 for

- ☒ filing a response to the Official Action dated: April 10, 2002
- ☐ responding to the requirements in the Notice of Allowability dated:
- ☐ filing the Formal Drawings. The Issue Fee due has been timely filed.
- ☐ responding to the Notice to File Missing Parts of Application dated:
- ☐ filing a Notice of Appeal. A timely response to the final rejection, due has been filed.
- ☐ filing an Appeal Brief. A Notice of Appeal was filed on:
- ☒ Applicant claims small entity status. See 37 CFR 1.27. Therefore, the fee amount shown below is reduced by one-half.

The required fee of \$200.00 is enclosed herewith by check and any further charges may be made against the Attorney of Record's Deposit Account No. 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully Submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Carl E. Schlier

Eckhard H. Kuesters

Registration No. 28,870

Carl E. Schlier

Registration No. 34,426



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Tel. (703) 413-3000
Fax. (703) 413-2220
(OSMMN 10/01)
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Notice of Allowability

Application No.

09/635,272

Examiner

José R Díaz

Applicant(s)

TONG, QIN-YI

Art Unit

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 9/10/02.
2. ☒ The allowed claim(s) is/are 44-49, 51-76, 78-87, 89-97 and 99-107.
3. ☐ The drawings filed on _____ are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
- * Certified copies not received: _____.
5. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 - (a) ☐ The translation of the foreign language provisional application has been received.
6. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

7. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
8. ☒ CORRECTED DRAWINGS must be submitted.
 - (a) ☒ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☒ hereto or 2) ☐ to Paper No. _____.
 - (b) ☐ including changes required by the proposed drawing correction filed _____, which has been approved by the Examiner.
 - (c) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No. _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the top margin (not the back) of each sheet. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

9. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|---|
| 1 <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 2 <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3 <input checked="" type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 4 <input type="checkbox"/> Interview Summary (PTO-413), Paper No. _____ |
| 5 <input type="checkbox"/> Information Disclosure Statements (PTO-1449), Paper No. _____ | 6 <input type="checkbox"/> Examiner's Amendment/Comment |
| 7 <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit of Biological Material | 8 <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance |
| | 9 <input type="checkbox"/> Other |

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance: Applicant's arguments filed in Paper No. 18 are persuasive. For instance, the prior art fails to teach, disclose, or suggest, either alone or in combination, a structure comprising a first substrate having a first nearly-amorphized region containing one of boron and arsenic formed on a first surface of said first substrate and/or extending only one to a few monolayers into said first substrate; a second substrate having a second nearly-amorphized region containing one of boron and arsenic formed on a second surface of said second substrate and/or extending only one to a few monolayers into said second substrate; and said first surface being bonded to said second surface to form a bonded pair of substrates.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R Díaz whose telephone number is (703) 308-6078. The examiner can normally be reached on 9:00-5:00 Monday, Tuesday, Thursday and Friday.

Application/Control Number: 09/635,272
Art Unit: 2815

Page 3

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 746-3891 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JRD
December 1, 2002

A handwritten signature in black ink, appearing to be 'JRD', is located in the middle right section of the page.

Notice of References Cited

Application/Control No.

09/635,272

Applicant(s)/Patent Under

Reexamination

TONG, QIN-YI

Examiner

José R Díaz

Art Unit

2815

Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,198,159 B1	03-2001	Hosoma et al.	257/643
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)

Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

NOTICE OF DRAFTSPERSON'S
PATENT DRAWING REVIEWThe drawing(s) filed (insert date) 08/09/00:A. ☐ approved by the Draftsperson under 37 CFR 1.84 or 1.152.B. ☒ objected to by the Draftsperson under 37 CFR 1.84 or 1.152 for the reasons indicated below. The Examiner will require submission of new, corrected drawings when necessary. Corrected drawing must be submitted according to the instructions on the back of this notice.1. DRAWINGS. 37 CFR 1.84(a): Acceptable categories of drawings:
Black ink. Color.☐ Color drawings are not acceptable until petition is granted.

Fig(s) _____

☐ Pencil and non black ink not permitted. Fig(s) _____

2. PHOTOGRAPHS. 37 CFR 1.84(b)

☐ 1 full-tone set is required. Fig(s) _____☐ Photographs may not be mounted. 37 CFR 1.84(c)☐ Poor quality (half-tone). Fig(s) _____

3. TYPE OF PAPER. 37 CFR 1.84(e)

☐ Paper not flexible, strong, white, and durable.

Fig(s) _____

☐ Erasures, alterations, overwritings, interlineations, folds, copy machine marks not accepted. Fig(s) _____☐ Mylar, velum paper is not acceptable (too thin).

Fig(s) _____

4. SIZE OF PAPER. 37 CFR 1.84(f): Acceptable sizes:

☐ 21.0 cm by 29.7 cm (DIN size A4)☐ 21.6 cm by 27.9 cm (8 1/2 x 11 inches)☐ All drawing sheets not the same size.

Sheet(s) _____

☐ Drawings sheets not an acceptable size. Fig(s) _____

5. MARGINS. 37 CFR 1.84(g): Acceptable margins:

Top 2.5 cm Left 2.5cm Right 1.5 cm Bottom 1.0 cm

SIZE: A4 Size

Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm

SIZE: 8 1/2 x 11

Margins not acceptable. Fig(s) 2A, 3-5, 9, 13☒ Top (T) ☒ Left (L)☐ Right (R) ☐ Bottom (B)

6. VIEWS. 37 CFR 1.84(h)

REMINDER: Specification may require revision to correspond to drawing changes.

Partial views. 37 CFR 1.84(h)(2)

☐ Brackets needed to show figure as one entity.

Fig(s) _____

☐ Views not labeled separately or properly.

Fig(s) _____

☐ Enlarged view not labeled separately or properly.

Fig(s) _____

7. SECTIONAL VIEWS. 37 CFR 1.84 (h)(3)

☐ Hatching not indicated for sectional portions of an object.

Fig(s) _____

☐ Sectional designation should be noted with Arabic or

Roman numbers. Fig(s) _____

8. ARRANGEMENT OF VIEWS. 37 CFR 1.84(i)

☐ Words do not appear on a horizontal, left-to-right fashion when page is either upright or turned so that the top becomes the right side, except for graphs. Fig(s) _____

9. SCALE. 37 CFR 1.84(k)

☐ Scale not large enough to show mechanism without crowding when drawing is reduced in size to two-thirds in reproduction.

Fig(s) _____

10. CHARACTER OF LINES, NUMBERS, & LETTERS.

37 CFR 1.84(i)

☒ Lines, numbers & letters not uniformly thick and well defined, clean, durable, and black (poor line quality).Fig(s) 3-6, 9, 14

11. SHADING. 37 CFR 1.84(m)

☐ Solid black areas pale. Fig(s) _____☐ Solid black shading not permitted. Fig(s) _____☐ Shade lines, pale, rough and blurred. Fig(s) _____

12. NUMBERS, LETTERS, & REFERENCE CHARACTERS.

37 CFR 1.84(p)

☐ Numbers and reference characters not plain and legible.

Fig(s) _____

☐ Figure legends are poor. Fig(s) _____☐ Numbers and reference characters not oriented in the same direction as the view. 37 CFR 1.84(p)(1)

Fig(s) _____

☐ English alphabet not used. 37 CFR 1.84(p)(2)

Fig(s) _____

☐ Numbers, letters and reference characters must be at least .32 cm (1/8 inch) in height. 37 CFR 1.84(p)(3)

Fig(s) _____

13. LEAD LINES. 37 CFR 1.84(q)

☐ Lead lines cross each other. Fig(s) _____☐ Lead lines missing. Fig(s) _____

14. NUMBERING OF SHEETS OF DRAWINGS. 37 CFR 1.84(r)

☐ Sheets not numbered consecutively, and in Arabic numerals beginning with number 1. Sheet(s) _____

15. NUMBERING OF VIEWS. 37 CFR 1.84(u)

☐ Views not numbered consecutively, and in Arabic numerals, beginning with number 1. Fig(s) _____

16. CORRECTIONS. 37 CFR 1.84(w)

☐ Corrections not made from prior PTO-948 dated _____

17. DESIGN DRAWINGS. 37 CFR 1.152

☐ Surface shading shown not appropriate. Fig(s) _____☐ Solid black shading not used for color contrast.

Fig(s) _____

COMMENTS

REVIEWER Draftsman: Son Lam DATE 12/02/02 TELEPHONE NO. _____

(703)308-0366

ATTACHMENT TO PAPER NO. 19



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

22850 7590 12/03/2002
OBLON SPIVAK MCCLELLAND MAIER & NEUSTADT
PC
FOURTH FLOOR
1755 JEFFERSON DAVIS HIGHWAY
ARLINGTON, VA 22202

EXAMINER	
DIAZ, JOSE R	
ART UNIT	CLASS-SUBCLASS
2815	257-052030

DATE MAILED: 12/03/2002

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/635,272	08/09/2000	Qin-Yi Tong	2025-0180-20	5012

TITLE OF INVENTION: METHOD OF EPITAXIAL-LIKE WAFER BONDING AT LOW TEMPERATURE AND BONDED STRUCTURE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$640	\$0	\$640	01/03/2003

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. **PROSECUTION ON THE MERITS IS CLOSED.** THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN **THREE MONTHS** FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. **THIS STATUTORY PERIOD CANNOT BE EXTENDED.** SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

- A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.
- B. If the status is changed, pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above and notify the United States Patent and Trademark Office of the change in status, or

If the SMALL ENTITY is shown as NO:

- A. Pay TOTAL FEE(S) DUE shown above, or
- B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check the box below and enclose the PUBLICATION FEE and 1/2 the ISSUE FEE shown above.
- ☐ Applicant claims SMALL ENTITY status.
See 37 CFR 1.27.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Box ISSUE FEE**
Commissioner for Patents
Washington, D.C. 20231
Fax **(703)746-4000**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)			Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.
22850	7590	12/03/2002	
OBLON SPIVAK MCCLELLAND MAIER & NEUSTADT PC FOURTH FLOOR 1755 JEFFERSON DAVIS HIGHWAY ARLINGTON, VA 22202			

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above, or being facsimile transmitted to the USPTO, on the date indicated below.

	(Depositor's name)
	(Signature)
	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/635,272	08/09/2000	Qin-Yi Tong	2025-0180-20	5012

TITLE OF INVENTION: METHOD OF EPITAXIAL-LIKE WAFER BONDING AT LOW TEMPERATURE AND BONDED STRUCTURE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$640	\$0	\$640	03/03/2003

EXAMINER	ART UNIT	CLASS-SUBCLASS
DIAZ, JOSE R	2815	257-052000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363). <input type="checkbox"/> Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached. <input type="checkbox"/> "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.	2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 1 _____ 2 _____ 3 _____
---	--

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the USPTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE _____ (B) RESIDENCE: (CITY and STATE OR COUNTRY) _____

Please check the appropriate assignee category or categories (will not be printed on the patent) ☐ individual ☐ corporation or other private group entity ☐ government

4a. The following fee(s) are enclosed: <input type="checkbox"/> Issue Fee <input type="checkbox"/> Publication Fee <input type="checkbox"/> Advance Order - # of Copies _____	4b. Payment of Fee(s): <input type="checkbox"/> A check in the amount of the fee(s) is enclosed. <input type="checkbox"/> Payment by credit card. Form PTO-2038 is attached. <input type="checkbox"/> The Commissioner is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).
--	--

Commissioner for Patents is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.

(Authorized Signature) _____	(Date) _____
<p>NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.</p> <p>This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Washington, DC 20231.</p> <p>Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.</p>	

TRANSMIT THIS FORM WITH FEE(S)



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/635,272	08/09/2000	Qin-Yi Tong	2025-0180-20	5012
22850	7590	12/03/2002	EXAMINER	
OBLON SPIVAK MCCLELLAND MAIER & NEUSTADT PC FOURTH FLOOR 1755 JEFFERSON DAVIS HIGHWAY ARLINGTON, VA 22202			DIAZ, JOSE R	
			ART UNIT	PAPER NUMBER
			2815	
DATE MAILED: 12/03/2002				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The patent term adjustment to date is 0 days. If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the term adjustment will be 0 days.

If a continued prosecution application (CPA) was filed in the above-identified application, the filing date that determines patent term adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) system. (<http://pair.uspto.gov>)

Any questions regarding the patent term extension or adjustment determination should be directed to the Office of Patent Legal Administration at (703)305-1383.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/635,272	08/09/2000	Qin-Yi Tong	2025-0180-20	5012
22850	7590	12/03/2002	EXAMINER	
OBLON SPIVAK MCCLELLAND MAIER & NEUSTADT PC FOURTH FLOOR 1755 JEFFERSON DAVIS HIGHWAY ARLINGTON, VA 22202 UNITED STATES			DIAZ, JOSE R	
			ART UNIT	PAPER NUMBER
			2815	
DATE MAILED: 12/03/2002				

Notice of Possible Fee Increase on October 1, 2002

If a reply to a "Notice of Allowance and Fee(s) Due" is filed in the Office on or after October 1, 2002, then the amount due may be higher than that set forth in the "Notice of Allowance and Fee(s) Due" since there may be an increase in fees effective on October 1, 2002. See Revision of Patent and Trademark Fees for Fiscal Year 2003; Notice of Proposed Rulemaking, 67 Fed. Reg. 30634, 30636 (May 7, 2002). Although a change to the amount of the publication fee is not currently proposed for October 2002, if the issue fee or publication fee is to be paid on or after October 1, 2002, applicant should check the USPTO web site for the current fees before submitting the payment. The USPTO Internet address for the fee schedule is: <http://www.uspto.gov/main/howtofees.htm>.

If the issue fee paid is the amount shown on the "Notice of Allowance and Fee(s) Due," but not the correct amount in view of any fee increase, a "Notice to Pay Balance of Issue Fee" will be mailed to applicant. In order to avoid processing delays associated with mailing of a "Notice to Pay Balance of Issue Fee," if the response to the Notice of Allowance and Fee(s) due form is to be filed on or after October 1, 2002 (or mailed with a certificate of mailing on or after October 1, 2002), the issue fee paid should be the fee that is required at the time the fee is paid. If the issue fee was previously paid, and the response to the "Notice of Allowance and Fee(s) Due" includes a request to apply a previously-paid issue fee to the issue fee now due, then the difference between the issue fee amount at the time the response is filed and the previously paid issue fee should be paid. See Manual of Patent Examining Procedure, Section 1308.01 (Eighth Edition, August 2001).

Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

Transaction History Date 2003-02-19

Date information retrieved from USPTO Patent
Application Information Retrieval (PAIR)
system records at www.uspto.gov

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Box ISSUE FEE
Commissioner for Patents
Washington, D.C. 20231
Fax (703)746-4000

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

22850 7590 12/03/2002

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/635,272	08/09/2000	Qin-Yi Tong	149840US20	5012

TITLE OF INVENTION: METHOD OF EPITAXIAL-LIKE WAFER BONDING AT LOW TEMPERATURE AND BONDED STRUCTURE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$640 650	\$0	\$640 650	3/03/2003

EXAMINER	ART UNIT	CLASS-SUBCLASS
DIAZ, JOSE R	2815	257-052000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

- OBLON, SPIVAK,
- MCCLELLAND, MAIER
- & NEUSTADT, P.C.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the USPTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

ZIPTRONIX, INC.

Research Triangle Park, NORTH CAROLINA

Please check the appropriate assignee category or categories (will not be printed on the patent) ☐ individual ☒ corporation or other private group entity ☐ government

4a. The following fee(s) are enclosed:

- ☒ Issue Fee
- ☐ Publication Fee
- ☐ Advance Order - # of Copies -0-

4b. Payment of Fee(s):

- ☒ A check in the amount of the fee(s) is enclosed.
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Commissioner for Patents is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.

(Authorized Signature)

(Date)

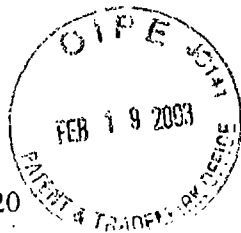
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This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Washington, DC 20231.

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TRANSMIT THIS FORM WITH FEE(S)

149840US20



20 Kern

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF:

Qin-Yi TONG

SERIAL NO.: 09/635,272

FILED: August 9, 2000

FOR: METHOD OF EPITAXIAL-LIKE
WAFER BONDING AT LOW
TEMPERATURE AND BONDED
STRUCTURE

:

: GROUP: 2815

: DATE ALLOWED: December 3, 2002

: EXAMINER: Diaz, J.R.

:

LETTER TO THE OFFICIAL DRAFTSMAN

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Any corrections required by the Chief Draftsman or drawing amendments approved by the Examiner have been incorporated into the copies of the Formal Drawings submitted herewith. It is requested that the enclosed 11 sheets of Formal Drawings be entered to replace the drawings previously filed in this application.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870

Joseph A. Scafetta, Jr.
Registration No. 26,803



22850

Customer Number 22850
Tel. (703) 413-3000
Fax. (703) 413-2220
(OSMMN 10/01)

MJS/jrs

I:\USER\JRSM\DRAWINGS\COVER LETTERS\149840.DOC

6563133

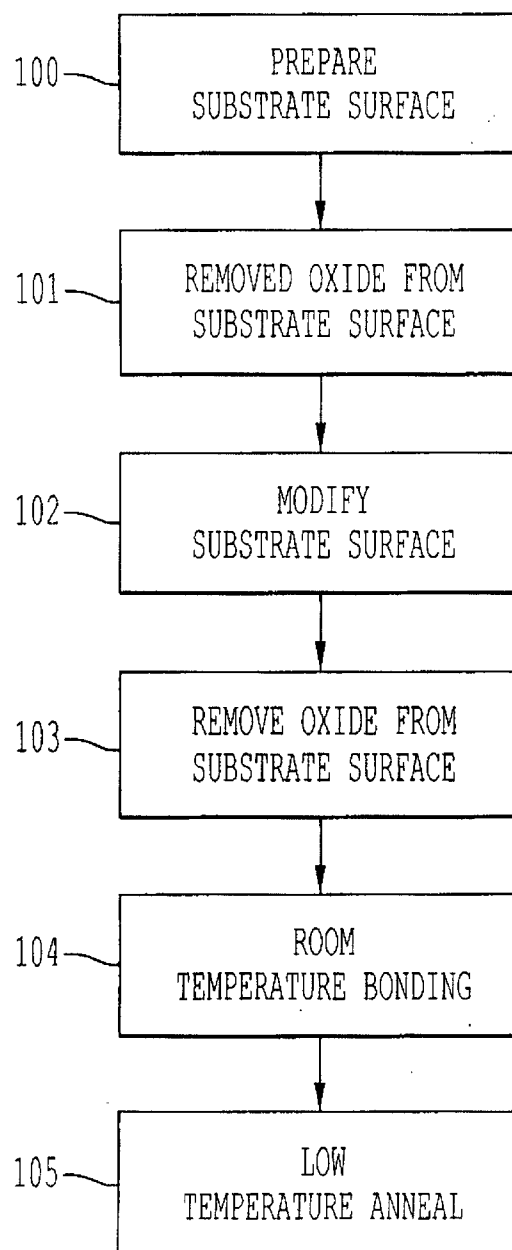
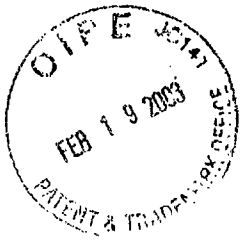
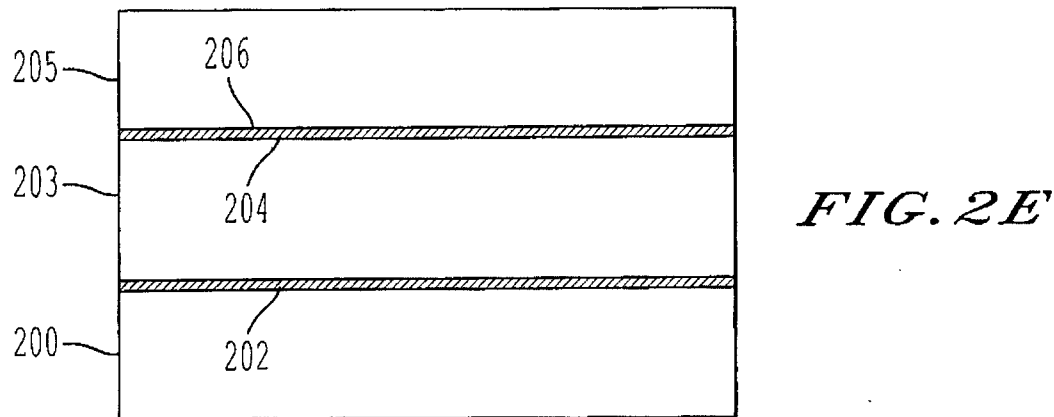
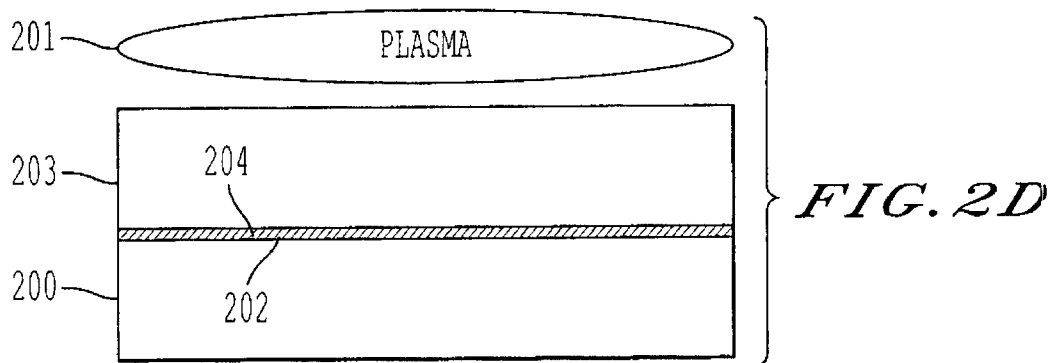
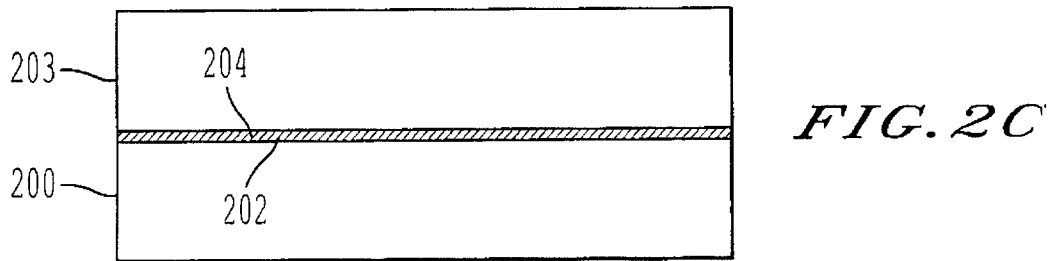
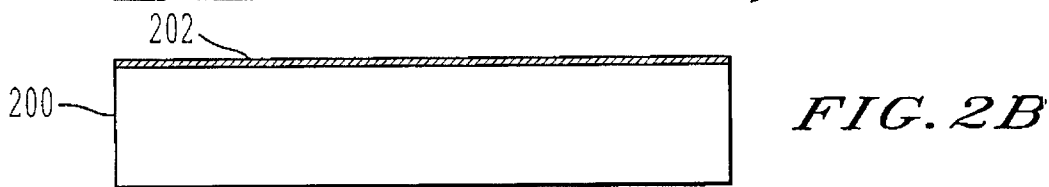
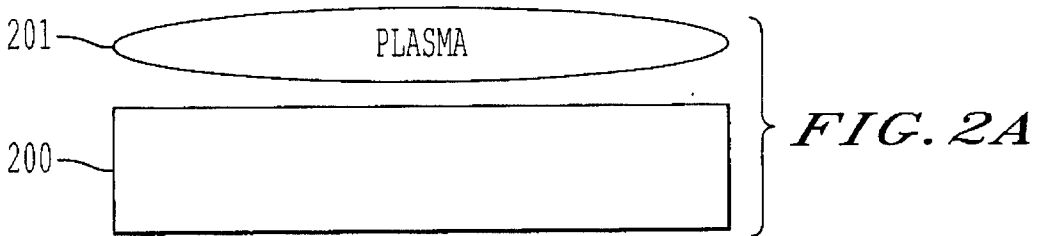


FIG. 1



SERIAL NO: 09/635,272
NV: Qin-Yi TONG
DOCKET #149840US20
SHEET 2 OF 11





SERIAL NO: 09/635,272
INV: Qin-Yi TONG
DOCKET #149840US20
SHEET 3 OF 11

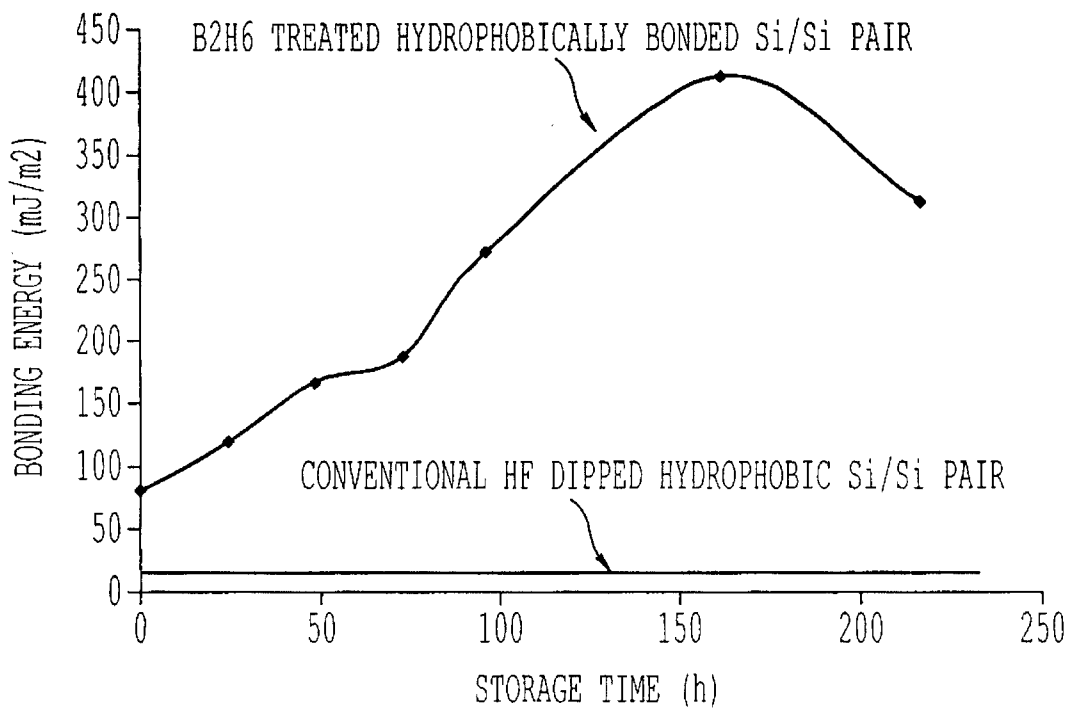


FIG. 3

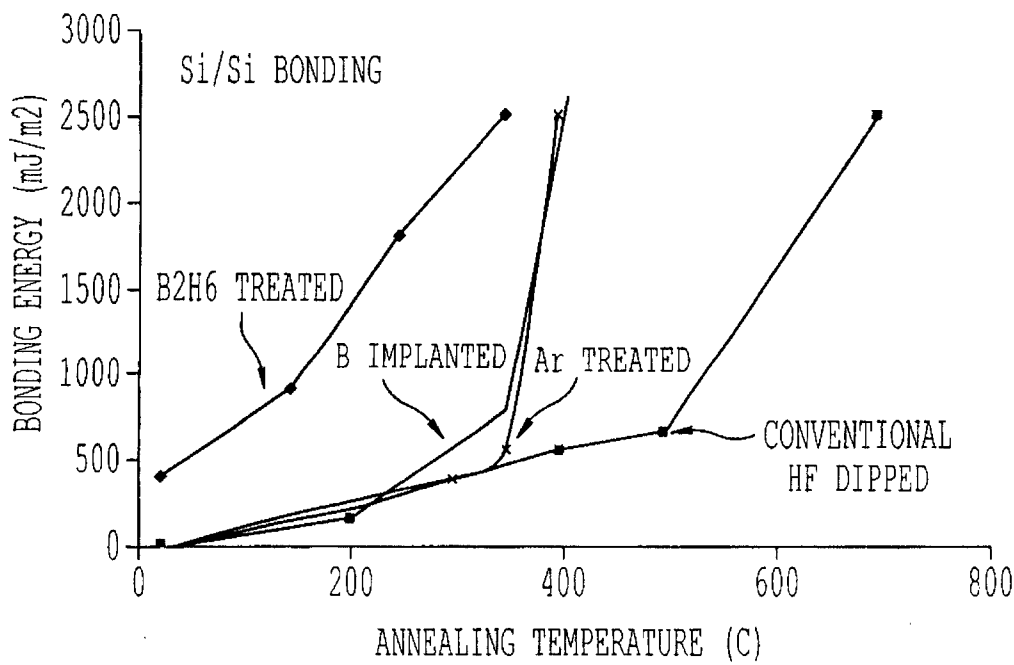


FIG. 4



SERIAL NO: 09/635,272
V: Qin-Yi TONG
DOCKET #149840US20
SHEET 4 OF 11

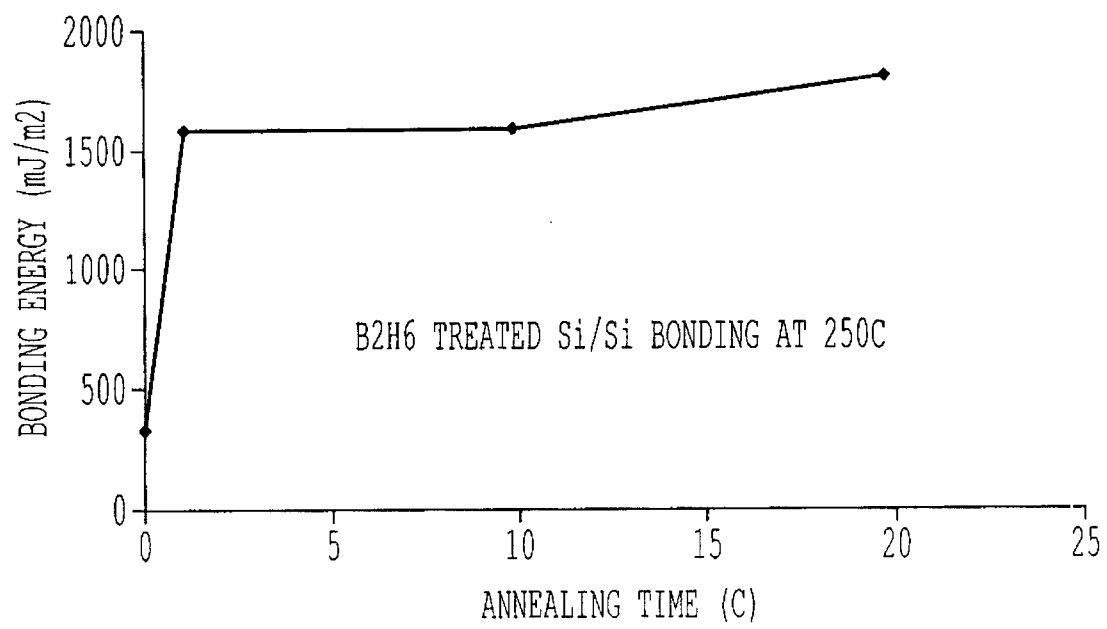


FIG. 5

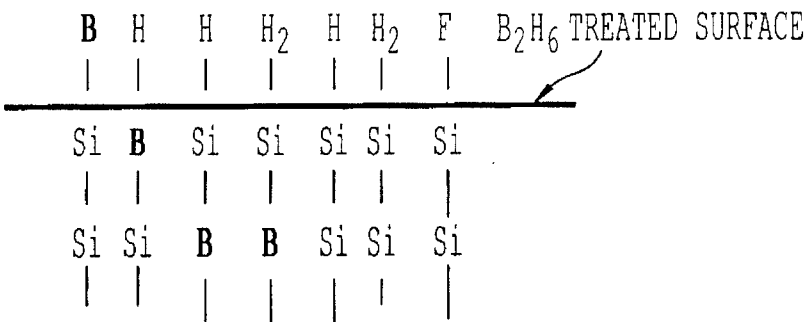


FIG. 6



SERIAL NO: 09/635,272
I' Qin-Yi TONG
L SET #149840US20
SHEET 5 OF 11

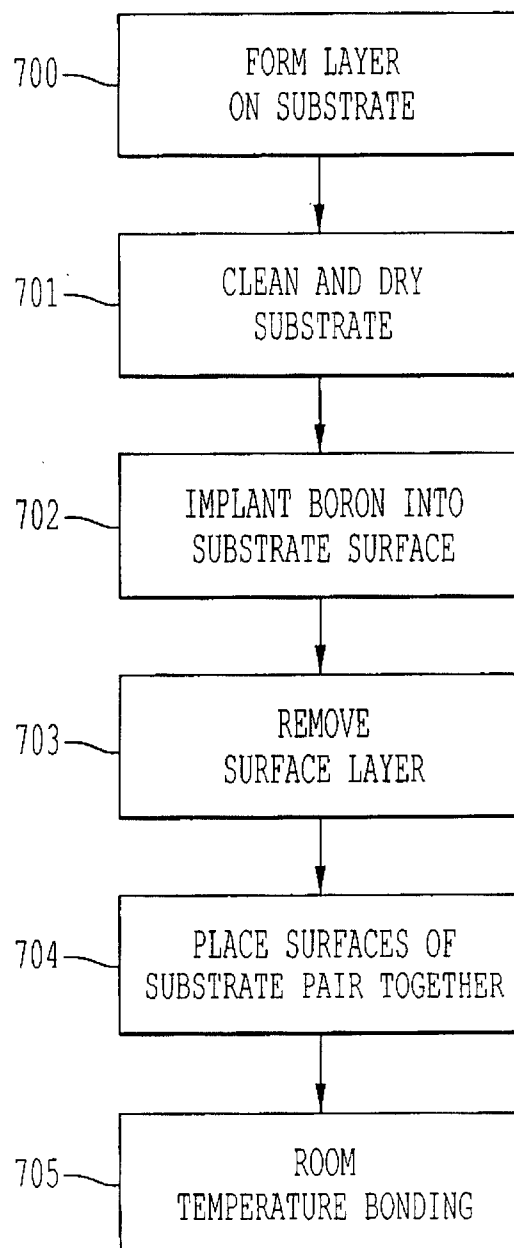


FIG. 7



SERIAL NO: 09/635,272
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DOCKET #149840US20
SHEET 6 OF 11

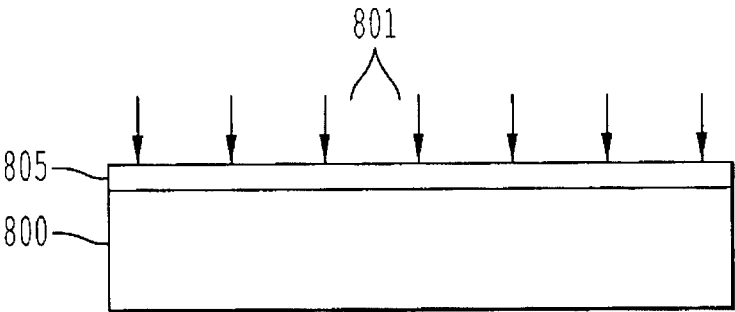


FIG. 8A

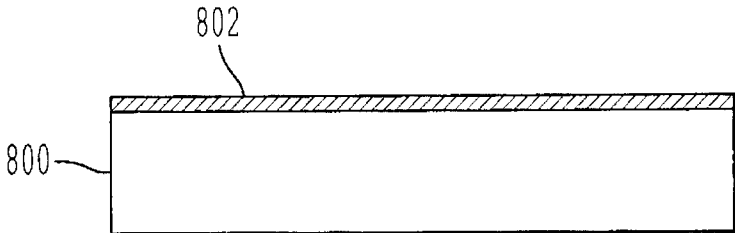


FIG. 8B

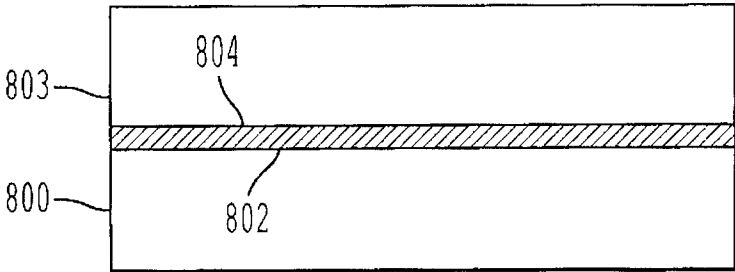
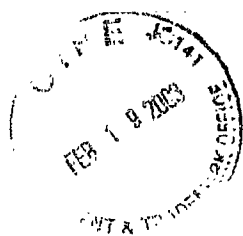


FIG. 8C



SERIAL NO: 09/635,272
V: Qin-Yi TONG
JACKET #149840US20
SHEET 7 OF 11

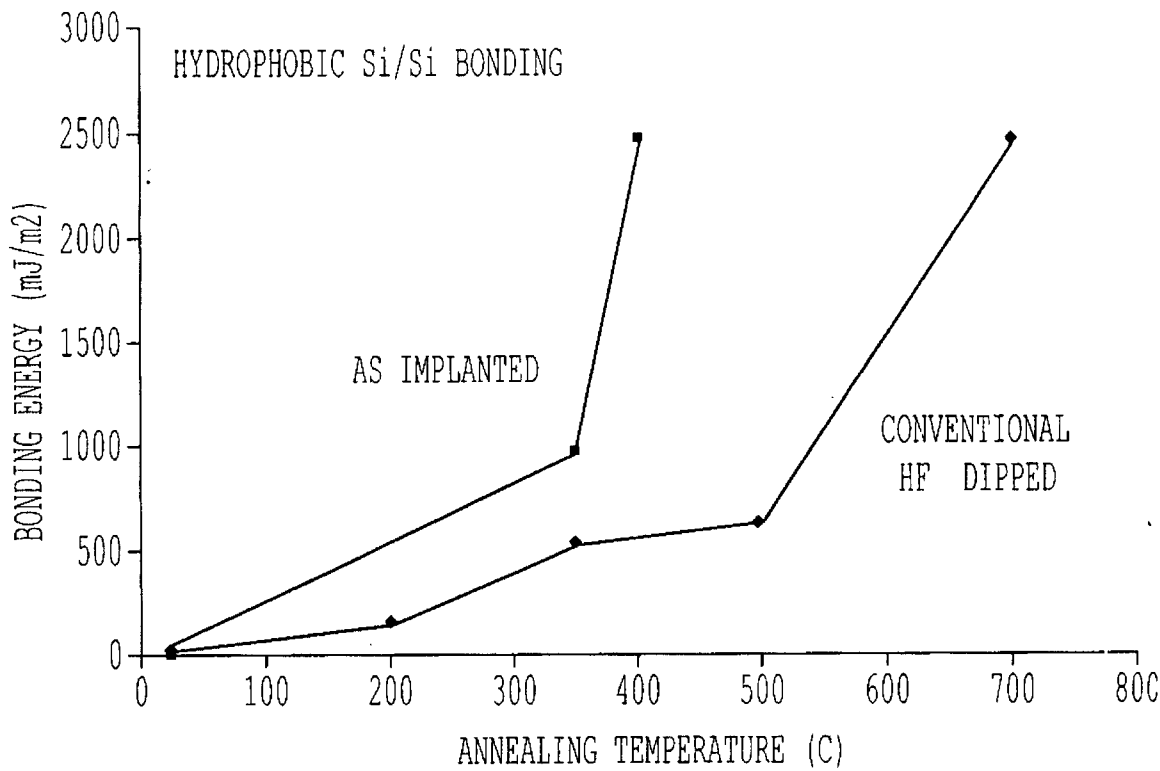


FIG. 9



SERIAL NO: 09/635,272
INVENTOR: QIN-YI TONG
DOCKET #149840US20
SHEET 8 OF 11

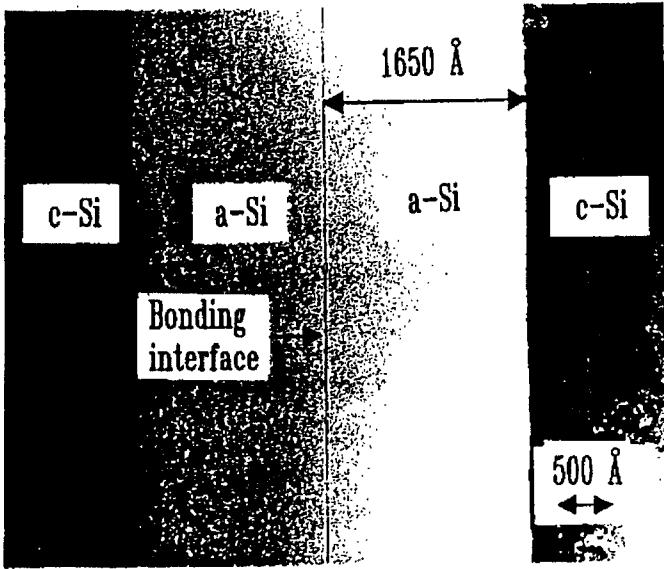


FIG. 10

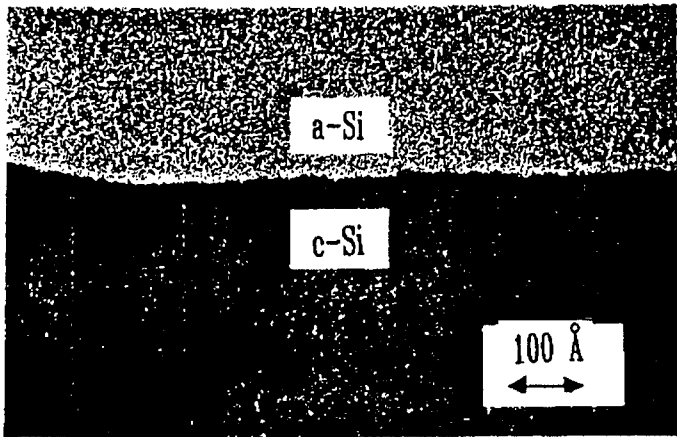


FIG. 11

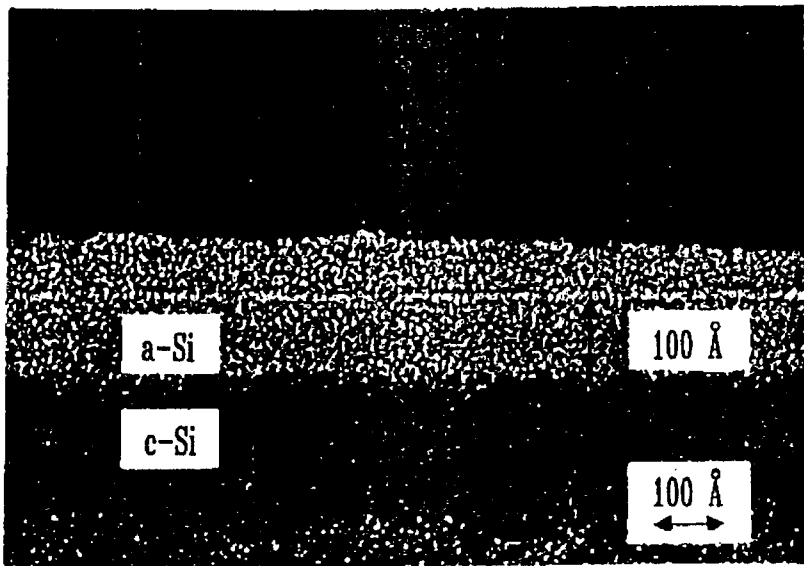


FIG. 12



SERIAL NO: 09/635,272
V: Qin-Yi TONG
DOCKET #149840US20
SHEET 9 OF 11

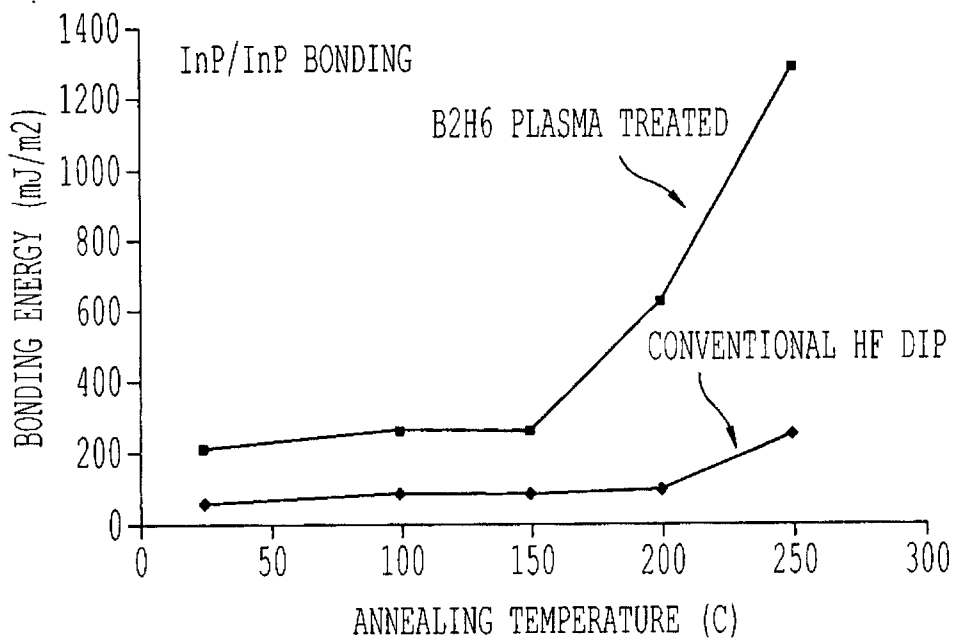


FIG. 13

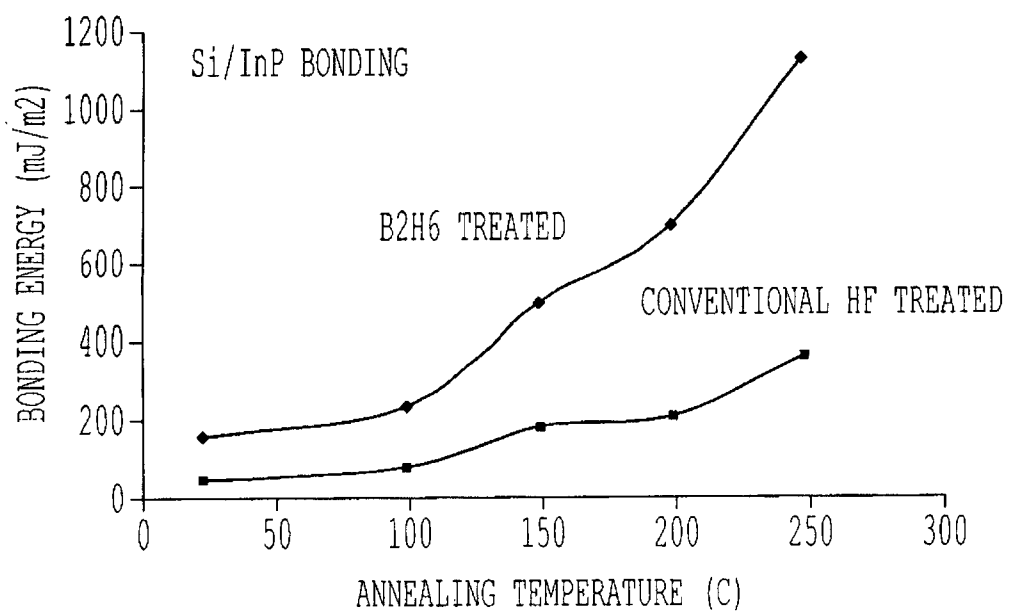


FIG. 14



SERIAL NO: 09/635,272
Inventor: Qin-Yi TONG
PUBLICATION NO: 2003/0149840US20
SHEET 10 OF 11

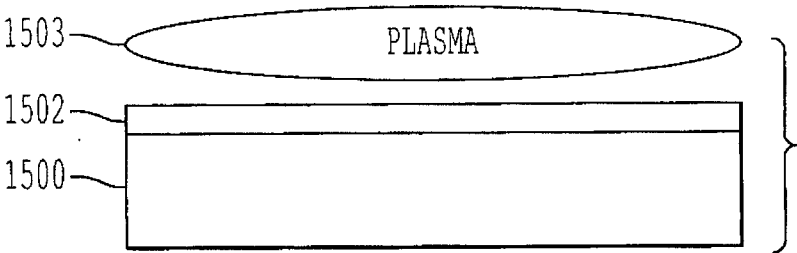


FIG. 15A

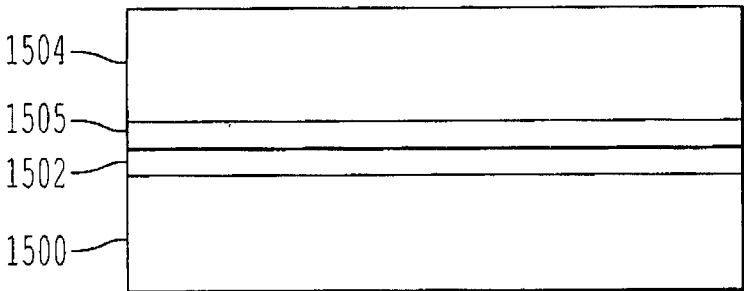


FIG. 15B

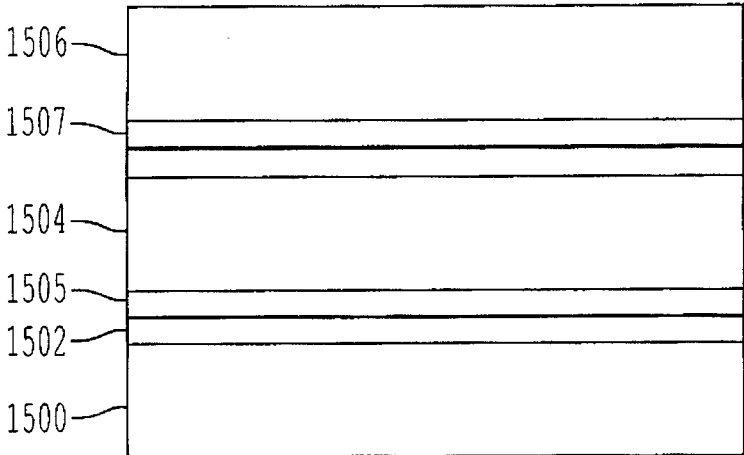
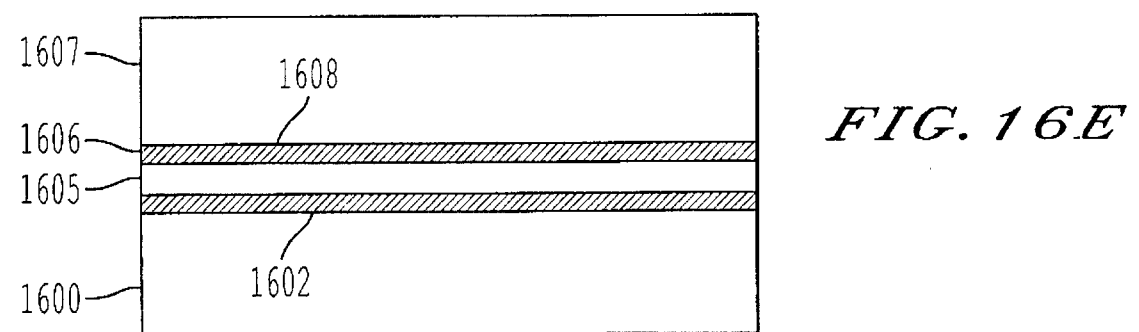
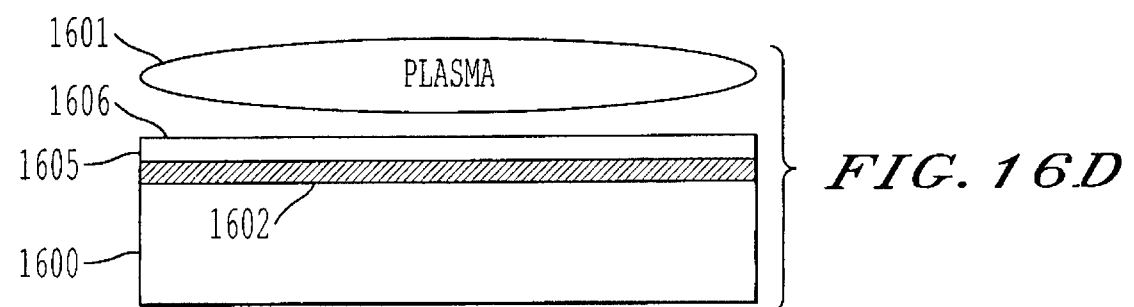
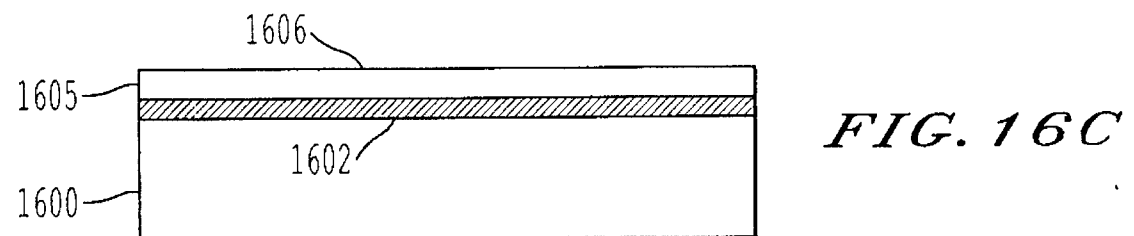
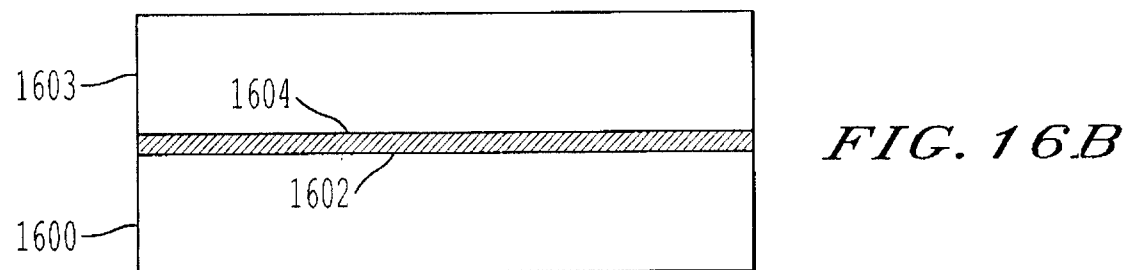
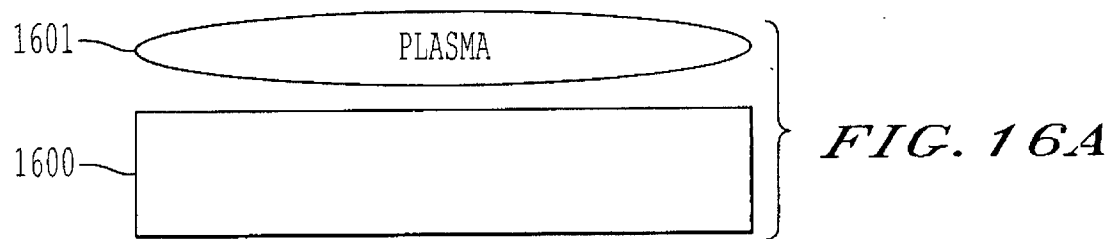


FIG. 15C



PATENT APPLICATION FEE DETERMINATION RECORD

Effective October 1, 2001

Application or Docket Number

CLAIMS AS FILED - PART I

(Column 1) (Column 2)

TOTAL CLAIMS		
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	minus 20=	*
INDEPENDENT CLAIMS	minus 3 =	*
MULTIPLE DEPENDENT CLAIM PRESENT <input type="checkbox"/>		

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

(Column 1) (Column 2) (Column 3)

AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	* 51	Minus ** 66	=
Independent	* 6	Minus *** 6	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <input type="checkbox"/>			

SMALL ENTITY TYPE ☐ OR

OTHER THAN SMALL ENTITY

RATE	FEE	RATE	FEE
BASIC FEE	370.00	BASIC FEE	740.00
X\$ 9=		X\$18=	
X42=		X84=	
+140=		+280=	
TOTAL		TOTAL	

SMALL ENTITY OR

OTHER THAN SMALL ENTITY

RATE	ADDITIONAL FEE	RATE	ADDITIONAL FEE
X\$ 9=		X\$18=	
X42=		X84=	
+140=		+280=	
TOTAL ADDIT. FEE		TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE	RATE	ADDITIONAL FEE
X\$ 9=		X\$18=	
X42=		X84=	
+140=		+280=	
TOTAL ADDIT. FEE		TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE	RATE	ADDITIONAL FEE
X\$ 9=		X\$18=	
X42=		X84=	
+140=		+280=	
TOTAL ADDIT. FEE		TOTAL ADDIT. FEE	

AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	* 51	Minus ** 66	=
Independent	* 6	Minus *** 6	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <input type="checkbox"/>			

AMENDMENT C	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus **	=
Independent	*	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <input type="checkbox"/>			

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."

***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

PATENT APPLICATION FEE DETERMINATION RECORD
Effective December 29, 1999

Application or Docket Number

09 635272

CLAIMS AS FILED - PART I

(Column 1)

(Column 2)

FOR	NUMBER FILED	NUMBER EXTRA
BASIC FEE		
TOTAL CLAIMS	58 minus 20 =	38
INDEPENDENT CLAIMS	4 minus 3 =	1
MULTIPLE DEPENDENT CLAIM PRESENT		

SMALL ENTITY
TYPE ☐

OR OTHER THAN
SMALL ENTITY

RATE	FEE		RATE	FEE
	345.00	OR		690.00
X\$ 9=	342	OR	X\$18=	648
X39=	39	OR	X78=	08
+130=		OR	+260=	
TOTAL	726	OR	TOTAL	

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

(Column 1)

(Column 2)

(Column 3)

AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	66	Minus	58	= 8
Independent	6	Minus	4	= 2
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

SMALL ENTITY

OR OTHER THAN
SMALL ENTITY

RATE	ADDI- TIONAL FEE		RATE	ADDI- TIONAL FEE
X\$ 9=	72.60	OR	X\$18=	
X39=	80.00	OR	X78=	
+130=		OR	+260=	
TOTAL ADDIT. FEE	152	OR	TOTAL ADDIT. FEE	

(Column 1)

(Column 2)

(Column 3)

AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

RATE	ADDI- TIONAL FEE		RATE	ADDI- TIONAL FEE
X\$ 9=		OR	X\$18=	
X39=		OR	X78=	
+130=		OR	+260=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

(Column 1)

(Column 2)

(Column 3)

AMENDMENT C	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

RATE	ADDI- TIONAL FEE		RATE	ADDI- TIONAL FEE
X\$ 9=		OR	X\$18=	
X39=		OR	X78=	
+130=		OR	+260=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."

***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

MPI Family Report (Family Bibliographic and Legal Status)

In the MPI Family report, all publication stages are collapsed into a single record, based on identical application data. The bibliographic information displayed in the collapsed record is taken from the latest publication.

Report Created Date: 2012-10-03

Name of Report:

Number of Families: 1

Comments:

Table of Contents

1.	US6563133B1	20030513	ZIPTRONIX INC	US	
	Method of epitaxial-like wafer bonding at low temperature and bonded structure				5



Family1

6 records in the family, collapsed to 5 records.

AU8060201A 20020218

[no drawing available]

(ENG) A method of epitaxial-like wafer bonding at low temperature and bonded structure

Assignee: ZIPTRONIX

Inventor(s): TONG QIN-YI

Application No: AU 8060201 D

Filing Date: 20010809

Issue/Publication Date: 20020218

Abstract: (ENG) A process for bonding oxide-free silicon substrate pairs and other substrates at low temperature. This process involves modifying the surface of the silicon wafers to create defect regions, for example by plasma-treating the surface to be bonded with a or boron-containing plasmas such as a B₂H₆ plasma. The surface defect regions may also be created by ion implantation, preferably using boron. The surfaces may also be amorphized. The treated surfaces are placed together, thus forming an attached pair at room temperature in ambient air. The bonding energy reaches approximately 400 mJ/m² at room temperature, 900 mJ/m² at 150° C., and 1800 mJ/m² at 250° C. The bulk silicon fracture energy of 2500 mJ/m² was achieved after annealing at 350-400° C. The release of hydrogen from B-H complexes and the subsequent absorption of the hydrogen by the plasma induced modified layers on the bonding surfaces at low temperature is most likely responsible for the enhanced bonding energy.

Priority Data: US 63527200 20000809 A Y; US 0122591 20010809 W W N;

IPC (International Class): H01L021302; H01L02118; H01L021306

ECLA (European Class): H01L02102F2D; H01L02118B2; H01L021306

Legal Status: There is no Legal Status information available for this patent

TW556251B 20031001

(ENG) a method of epitaxial-like wafer bonding at low temperature and bonded structure

Assignee: ZIPTRONIX INCUS

[no drawing available]

Inventor(s): TONG QIN-YI CN

Application No: TW 90119343 A

Filing Date: 20010808

Issue/Publication Date: 20031001

Abstract: (ENG) A process for bonding oxide-free silicon substrate pairs and other substrates at low temperature. This process involves modifying the surface of the silicon wafers to create defect regions, for example by plasma-treating the surface to be bonded with a or boron-containing plasmas such as a B2H6 plasma. The surface defect regions may also be created by ion implantation, preferably using boron. The surfaces may also be amorphized. The treated surfaces are placed together, thus forming an attached pair at room temperature in ambient air. The bonding energy reaches approximately 400 mJ/M<2> at room temperature, 900 mJ/M<2> at 150 DEG C, and 1800 mJ/M<2> at 250 DEG C. The bulk silicon fracture energy of 2500 mJ/m<2> was achieved after annealing at 350-400 DEG C. The release of hydrogen from B-H complexes and the subsequent absorption of the hydrogen by the plasma induced modified layers on the bonding surfaces at low temperature is most likely responsible for the enhanced bonding energy.

Priority Data: US 63527200 20000809 A Y;

IPC (International Class): H01L021302; H01L02118; H01L021306

ECLA (European Class): H01L02102F2D; H01L02118B2; H01L021306

Legal Status:

Date	+/-	Code	Description
20040205	(+)	GD4A	ISSUE OF PATENT CERTIFICATE FOR GRANTED INVENTION PATENT



WO2002013247A1 20020214

(ENG) A METHOD OF EPITAXIAL-LIKE WAFER BONDING AT LOW TEMPERATURE AND BONDED STRUCTURE

Assignee: ZIPTRONIX US

Inventor(s): TONG QIN-YI

Application No: US 0122591 W

Filing Date: 20010809

Issue/Publication Date: 20020214

Abstract: (ENG) A process for bonding oxide-free silicon substrate pairs and other substrates at low temperature. This process involves modifying the surface of the silicon wafers (200, 203) to create defect regions (202, 204), for example by plasma-treating the surface to be bonded with boron-containing plasmas such as a B₂H₆ plasma (201). The surface defect regions may also be amorphized (202, 204). The treated surfaces are placed together, thus forming an attached pair at room temperature in ambient air. The bonding energy reaches approximately 400 mJ/m² at room temperature, 900mJ/m² at 150 DEG C, and 1800 mJ/m² at 250 DEG C. The bulk silicon fracture energy of 2500 mJ/m² was achieved after annealing at 350-400 DEG C. The release of hydrogen from B-H complexes and the subsequent absorption of the hydrogen by the plasma induced modified layers on the bonding surfaces at low temperature is most likely responsible for the enhanced bonding energy.

Priority Data: US 63527200 20000809 A Y;

IPC (International Class): H01L021302; H01L02118; H01L021306

ECLA (European Class): H01L02102F2D; H01L02118B2; H01L021306

Designated Countries:

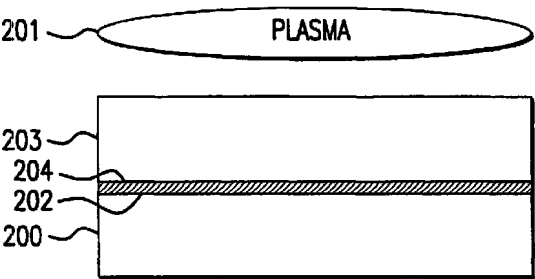
----Designated States: (national) AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW ::: (ARIPO) AP GH GM KE LS MW MZ SD SL SZ TZ UG ZW
----Regional Treaties: (EAPO) EA AM AZ BY KG KZ MD RU TJ TM
----EPO Extension States: (EPO) EP AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
----Elected States (PCT): (OAPI) OA BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG

Publication Language: ENG

Filing Language: ENG

Legal Status:

Date	+/-	Code	Description
20020214	(+)	AK	DESIGNATED STATES Kind code of corresponding patent document: A1; List of designated states: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW;
20020214	(+)	AL	DESIGNATED COUNTRIES FOR REGIONAL PATENTS Kind code of corresponding patent document: A1; List of designated states: GH GM KE LS MW MZ SD SL SZ TZ UG ZW AM AZ



			BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG;
20020410	()	121	EP: THE EPO HAS BEEN INFORMED BY WIPO THAT EP WAS DESIGNATED IN THIS APPLICATION
20030618	()	REG	REFERENCE TO NATIONAL CODE Corresponding country code for PRS Code (EP REG): DE; Corresponding EP Code 1 for PRS Code (EP REG): 8642;
20031022	(-)	122	EP: PCT APP. NOT ENT. EUROP. PHASE
20050607	()	NENP	NON-ENTRY INTO THE NATIONAL PHASE IN: Corresponding country code for PRS Code (EP REG): JP;

US7332410B2 20080219
US2003141502A1 20030731

(ENG) Method of epitaxial-like wafer bonding at low temperature and bonded structure

Assignee: ZIPTRONIX INC US

Inventor(s): TONG QIN-YI US

Application No: US 35814103 A

Filing Date: 20030205

Issue/Publication Date: 20080219

Abstract: (ENG) A process for bonding oxide-free silicon substrate pairs and other substrates at low temperature. This process involves modifying the surface of the silicon wafers to create defect regions, for example by plasma-treating the surface to be bonded with a or boron-containing plasmas such as a B₂H₆-plasma. The surface defect regions may also be created by ion implantation, preferably using boron. The surfaces may also be amorphized. The treated surfaces are placed together, thus forming an attached pair at room temperature in ambient air. The bonding energy reaches approximately 400 mJ/m² at room temperature, 900 mJ/m² at 150° C., and 1800 mJ/m² at 250° C. The bulk silicon fracture energy of 2500 mJ/m² was achieved after annealing at 350-400° C. The release of hydrogen from B-H complexes and the subsequent absorption of the hydrogen by the plasma induced modified layers on the bonding surfaces at low temperature is most likely responsible for the enhanced bonding energy.

Priority Data: US 35814103 20030205 A N; US 63527200 20000809 A 3 Y;

Related Application(s): 10/358141 20030205 20030141502 20030731 US; 09/635272 20000809 6563133 US

IPC (International Class): H01L02148; H01L021302; H01L02118; H01L021306

ECLA (European Class): H01L02102F2D; H01L02118B2; H01L021306

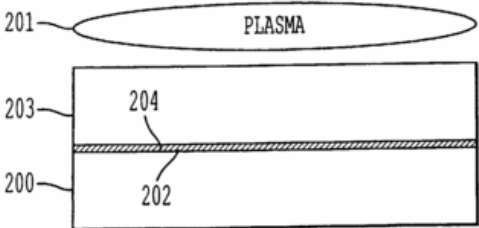
US Class: 438455; 257E21088; 257E21122; 257E21214; 257E21215; 257E21228; 438482; 438513; 438514

Publication Language: ENG

Filing Language: ENG

Agent(s): Oblon, Spivak, McClelland, Maier & Neustadt, P.C.

Examiner Primary: Parker, Kenneth



Examiner Assistant: Diaz, José R.

Legal Status:

Date	+/-	Code	Description
20081104	0	CC	

US6563133B1 20030513

(ENG) Method of epitaxial-like wafer bonding at low temperature and bonded structure

Assignee: ZIPTRONIX INC US

Inventor(s): TONG QIN-YI US

Application No: US 63527200 A

Filing Date: 20000809

Issue/Publication Date: 20030513

Abstract: (ENG) A process for bonding oxide-free silicon substrate pairs and other substrates at low temperature. This process involves modifying the surface of the silicon wafers to create defect regions, for example by plasma-treating the surface to be bonded with a or boron-containing plasmas such as a B2H6 plasma. The surface defect regions may also be created by ion implantation, preferably using boron. The surfaces may also be amorphized. The treated surfaces are placed together, thus forming an attached pair at room temperature in ambient air. The bonding energy reaches approximately 400 mJ/M2 at room temperature, 900 mJ/M2 at 150° C., and 1800 mJ/M2 at 250° C. The bulk silicon fracture energy of 2500 mJ/m2 was achieved after annealing at 350-400° C. The release of hydrogen from B-H complexes and the subsequent absorption of the hydrogen by the plasma induced modified layers on the bonding surfaces at low temperature is most likely responsible for the enhanced bonding energy.

Priority Data: US 63527200 20000809 A Y;

IPC (International Class): H01L021302; H01L02118; H01L021306

ECLA (European Class): H01L02102F2D; H01L02118B2; H01L021306

US Class: 257052; 257347; 257618; 257E21088; 257E21214; 257E21215; 257E21228; 438455; 438482; 438485; 438974

Agent(s): Oblon, Spivak, McClelland, Maier & Neustadt, P.C.

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Examiner Primary: Lee, Eddie

Examiner Assistant: Díaz, José R.

Assignments Reported to USPTO:

Reel/Frame: 11265/0856 **Date Signed:** 20000808 **Date Recorded:** 20001024

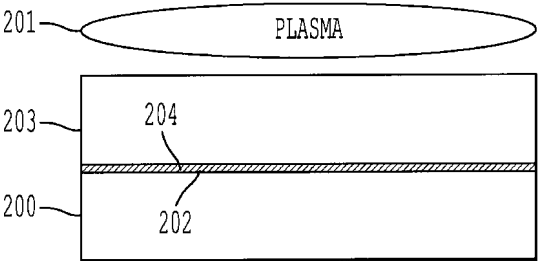
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Assignor: TONG, QIN-YI

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Brief: ASSIGNMENT OF ASSIGNORSINTEREST (SEE DOCUMENT FOR DETAILS).

Reel/Frame: 12002/0970 **Date Signed:** 20001026 **Date Recorded:** 20010725



Assignee: ZIPTRONIX, INC. RESEARCH TRIANGLE PARK NORTH CAROLINA

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Brief: ASSIGNMENT OF ASSIGNORSINTEREST (SEE DOCUMENT FOR DETAILS).

Legal Status:			
Date	+/-	Code	Description
20001024	()	AS	ASSIGNMENT New owner name: RESEARCH TRIANGLE INSTITUTE 3040 CORNWALLIS ROAD R; : ASSIGNMENT OF ASSIGNORS INTEREST;ASSIGNOR:TONG, QIN-YI;REEL/FRAME:011265/0856; Effective date: 20000808;
20001024	()	AS	New owner name: RESEARCH TRIANGLE INSTITUTE, NORTH CAROLINA; : ASSIGNMENT OF ASSIGNORS INTEREST;ASSIGNOR:TONG, QIN-YI;REEL/FRAME:011265/0856; Effective date: 20000808;
20001024	()	AS	New owner name: RESEARCH TRIANGLE INSTITUTE 3040 CORNWALLIS ROAD R; : ASSIGNMENT OF ASSIGNORS INTEREST;ASSIGNOR:TONG, QIN-YI;REEL/FRAME:011265/0856; Effective date: 20000808;
20010725	()	AS	ASSIGNMENT New owner name: ZIPTRONIX, INC. RESEARCH TRIANGLE PARK NORTH CAROL; : ASSIGNMENT OF ASSIGNORS INTEREST;ASSIGNOR:RESEARCH TRIANGLE INSTITUTE;REEL/FRAME:012002/0970; Effective date: 20001026;
20010725	()	AS	ASSIGNMENT New owner name: ZIPTRONIX, INC.RESEARCH TRIANGLE PARK, NORTH CAROL; : ASSIGNMENT OF ASSIGNORS INTEREST;ASSIGNOR:RESEARCH TRIANGLE INSTITUTE /AR;REEL/FRAME:012002/0970; Effective date: 20001026;
20010725	()	AS	New owner name: ZIPTRONIX, INC., NORTH CAROLINA; : ASSIGNMENT OF ASSIGNORS INTEREST;ASSIGNOR:RESEARCH TRIANGLE INSTITUTE;REEL/FRAME:012002/0970; Effective date: 20001026;
20010725	()	AS	New owner name: ZIPTRONIX, INC. RESEARCH TRIANGLE PARK NORTH CAROL; : ASSIGNMENT OF ASSIGNORS INTEREST;ASSIGNOR:RESEARCH TRIANGLE INSTITUTE;REEL/FRAME:012002/0970; Effective date: 20001026;
20010725	()	AS	New owner name: ZIPTRONIX, INC.RESEARCH TRIANGLE PARK, NORTH CAROL; : ASSIGNMENT OF ASSIGNORS INTEREST;ASSIGNOR:RESEARCH TRIANGLE INSTITUTE /AR;REEL/FRAME:012002/0970; Effective date: 20001026;
20061011	()	FPAY	Year of fee payment: 4;
20101216	()	FPAY	Year of fee payment: 8;
20101216	()	SULP	Year of fee payment: 7;

USPTO Maintenance Report					
Patent Bibliographic Data				10/03/2012 06:32 AM	
Patent Number:	6563133		Application Number:	09635272	
Issue Date:	05/13/2003		Filing Date:	08/09/2000	
Title:	METHOD OF EPITAXIAL-LIKE WAFER BONDING AT LOW TEMPERATURE AND BONDED STRUCTURE				
Status:	12th year fee window opens: 05/13/2014			Entity:	LARGE
Window Opens:	N/A	Surcharge Date:	N/A	Expiration:	N/A
Fee Amt Due:	Window not open	Surchg Amt Due:	Window not open	Total Amt Due:	Window not open
Fee Code:	1553	MAINTENANCE FEE DUE AT 11.5 YEARS			
Surcharge Fee Code:					
Most recent events (up to 7):	12/17/2010 12/17/2010 12/16/2010 12/16/2010 10/11/2006	Pat Hldr no Longer Claims Small Ent Stat Refund - Payment of Maintenance Fee, 8th Yr, Small Entity. 7.5 yr surcharge - late pmt w/in 6 mo, Large Entity. Payment of Maintenance Fee, 8th Year, Large Entity. Payment of Maintenance Fee, 4th Yr, Small Entity. --- End of Maintenance History ---			
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