

**Declaration of Dr. Richard A. Blanchard in Support of Petition
for *Inter Partes* Review of U.S. Patent No. 6,563,133**

Mail Stop: Inter Partes Review

Attn: Patent Trial and Appeal Board

Commissioner for Patents

PO Box 1450

Alexandria, VA 22313-1450

Commissioner:

I, Richard A. Blanchard, declare as follows:

1. I have been retained on behalf of Taiwan Semiconductor Manufacturing Company, Limited and TSMC North America Corporation (collectively “TSMC”) for the above-captioned *inter partes review* proceeding. I understand that this proceeding involves U.S. Patent No. 6,563,133 (hereinafter the “‘133 Patent”).
2. I have been asked to provide my technical review, analysis, insights and opinions regarding the above-noted references that form the basis for the grounds for unpatentability set forth in the Petition for *inter partes* review of the ‘133 Patent.
3. In my judgment, as an expert in the field of semiconductor manufacturing and semiconductor materials since at least 1977, I am qualified to provide an opinion as to what a person of ordinary skill in the art would have understood, known or concluded at the time that the patent-at-issue was filed.

I. Qualifications

4. I am a consultant for Thomson Reuters Expert Witness Services (previously known as Silicon Valley Expert Witness Group), a consulting company specializing in expert witness litigation support and technology consulting. I also provide technical consulting services to the semiconductor and electronics industry through Blanchard Associates.

5. My academic credentials include both a Bachelor of Science Degree in Electrical Engineering (BSEE) and a Master of Science Degree in Electrical Engineering (MSEE) from the Massachusetts Institute of Technology in 1968 and 1970, respectively. I subsequently obtained a Ph. D. in Electrical Engineering in 1982 from Stanford University.

6. My professional background and technical qualifications are stated above and are also reflected in my *Curriculum Vitae*, which is attached as TSMC1004. I am being compensated at a rate of \$275.00 per hour, with reimbursement for actual expenses, for my work related to this petition for *Inter Partes* Review. My compensation is not dependent on and in no way affects the substance of my statements in this declaration.

7. I have worked or consulted for more than 40 years as an Electrical Engineer. My primary focus has been the development, manufacture, operation and use of devices and integrated circuits, the assembly of these devices and integrated

circuits, products that use them, and their failures. My employment history following my graduation from MIT began at Fairchild Semiconductor in 1970. At Fairchild, my responsibilities included circuit and device design, process development and product engineering in the Linear Integrated Circuits Department.

8. In 1974, I joined Foothill College as an Associate Professor in the Engineering & Technology Division. My responsibilities included developing a program in Semiconductor Technology as well as teaching other courses in the division. While at Foothill College, I co-founded two companies, Cognition and Supertex, and later joined Supertex as a Vice President in 1978. At Supertex, I designed and developed discrete DMOS (double-diffused metal oxide semiconductor) transistors as well as integrated circuits that contained DMOS transistors. At Supertex, I also supervised the in-house assembly area, which included responsibility for the semiconductor manufacturing processes.

9. I left Supertex to join Siliconix in 1982, where I soon became Vice President of Engineering, with the responsibility for directing all of the company's product design and development. At Siliconix, I directed and contributed to the development of both discrete transistors and integrated circuits, including aspects of their assembly.

10. In 1987, I joined IXYS Corporation as a Senior Vice President with the responsibility for organizing an integrated circuits department. At IXYS, I developed integrated circuits that contained DMOS transistors or that interfaced to DMOS devices. My responsibilities included the design, the assembly, and the testing of these integrated circuits.

11. These duties continued until 1991, when I left IXYS to set up Blanchard Associates, a consulting firm specializing in semiconductor technology, including intellectual property. Soon thereafter, I was invited to join Failure Analysis Associates, which I did in late 1991. At Failure Analysis Associates, I investigated failures in electrical and electronic systems in addition to performing design and development consulting. Some of this work included the investigation of semiconductor material properties.

12. I left Failure Analysis in 1998 to join IP Managers, which later merged with the Silicon Valley Expert Witness Group, now known as Thomson Reuters Expert Witness Services (“Thomson Reuters”). At Thomson Reuters, I work with companies on patent and trade secret matters. I also consult for a number of semiconductor companies, working with them to develop products and intellectual property, or assisting them in other technical areas through Blanchard Associates. I am a member of a number of professional societies, including the Institute of Electrical and Electronic Engineers, the International Microelectronics and

Packaging Society, the American Vacuum Society, the Electronic Device Failure Analysis Society, and the Electrostatic Discharge Society.

II. My understanding of anticipation and obviousness

13. It is my understanding that a claimed invention is unpatentable if the claimed invention is anticipated by a single prior art reference. To anticipate a claim, the prior art reference must disclose each and every element as set forth in the claim, either expressly or by an inherent description. I understand that an element is inherent in a prior art reference if the subject matter is necessarily present in the prior art reference. I understand that evidence outside of the prior art reference may be examined to determine whether an element is necessarily present in the prior art reference. If a claim covers several alternatives, the claim is anticipated if any of the structures or composition within the scope of that claim is known in the prior art.

14. It is my understanding that a claimed invention is unpatentable if the differences between the invention and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. It is my understanding that “obviousness” is a question of law based on underlying factual issues including the content of the prior art and the level of skill in the art.

15. In considering whether the claims of the patent are obvious, I have been asked to consider (a) the level of ordinary skill in the art at the time of the claimed invention, (b) the scope and content of the prior art, (c) any differences between the prior art and the claims of the patent-in-suit, and (d) any “objective indicia” related to obviousness, including commercial success, long-felt but unresolved need, failure of others, copying, praise by others, unexpected results, and simultaneous invention by others.

16. I understand that for a single reference or a combination of references to make the claimed invention obvious, a person of ordinary skill in the art at the time of the invention must have been able to arrive at the claimed invention by modifying, altering or combining the applied references.

17. I also understand that when considering the obviousness of a patent claim, one should consider whether a teaching, suggestion or motivation to combine the references in the same manner as claimed exists so as to avoid impermissibly applying hindsight when considering the prior art. I understand this test should not be rigidly applied, but that the test can be important to avoid such hindsight. I understand that identifying a teaching, motivation, or suggestion in a prior art reference is not required to prove obviousness. I understand that teachings, suggestions, and motivations may also be found within the knowledge of a person

of ordinary skill, including inferences and creative steps that such a person would employ.

18. It is my understanding that the date of invention is generally presumed to be the filing date of an application for a patent, until proven to be an earlier date by the Patent Owner. If the patent claims priority to a prior application, it is my understanding that the patent may receive the benefit of the earlier filing date only if the earlier-filed application contains disclosure sufficient to support the claims of the patent, as issued.

III. Factual Understandings

19. I understand the presumed date of the invention is the filing date of the '133 Patent, which is August 9, 2000. I understand that the '133 Patent does not claim priority to an earlier application. Unless indicated otherwise, analyses relating to the time of the invention are with respect to this August 9, 2000 date.

20. A person of ordinary skill in the art as of August 9, 2000 would have a M.S. in Electrical Engineering, Materials Science, Solid State Electronics, or similar, and would also have at least 2 years' experience, or the equivalent through an advanced degree or similar, involving semiconductor processing and/or wafer bonding. Unless indicated otherwise, analyses stated herein are with reference to what a person of ordinary skill in the art would understand and know.

IV. Evidence and References Considered

21. I have reviewed, considered, and am familiar with the following references:

U.S. Patent No. 6,563,133 to Tong, Filed: August 9, 2000, Issued: May 13, 2003 (“ ‘133 Patent”).
U.S. Patent No. 6,534,381 to Cheung et al., Filed: January 4, 2000, Issued: March 18, 2003 (“Cheung”).
U.S. Patent No. 5,561,072 to Saito, Filed: November 21, 1994, Issued: October 1, 1996 (“Saito”).
Seiji Fujino et al., <i>Silicon Wafer Direct Bonding through the Amorphous Layer</i> , 34 Japanese J. Appl. Phys. 1322 (15 October 1995) (“Fujino”).
Shiyang Tian et al., <i>A Detailed Physical Model for Ion Implant Induced Damage in Silicon</i> , 45 (6) IEEE Transactions on Electron Devices 1226 (June 1998) (“Tian”).

22. I understand that each of Cheung, Saito, Fujino, and Tian qualify as prior art to the ‘133 Patent.

V. Background of the ‘133 Patent

23. The ‘133 Patent describes methods for bonding silicon layers at low temperatures. An example of this process is to plasma-treat the surfaces to be bonded with a boron containing plasma such as a B₂H₆ plasma. See, e.g., ‘133 Patent at Abstract. Such techniques were well known in the art at the time of the invention.

24. FIGS. 2A-2E of the '133 Patent illustrate that a dosage of boron and/or arsenic ions can create a uniform layer that constitutes a compliant or, as otherwise described, amorphous layer, on the top surface of the wafer.

25. Approaches described in the '133 Patent, in particular those claimed, were well known in the art at the time of the invention. Methods of increasing the density of integrated circuits, as dictated by Moore's law, have progressed to the point that bonding of wafers at low temperatures has become increasingly important.

26. Uses of the technology of the '133 Patent, as described at Col. 10:35–11:4 and FIGS. 15 and 16 of the '133 Patent, as well as in related patents and literature known in the art at the time of the invention are focused on providing a solution to the needs of very dense 3D integrated circuits. Related patents and literature known in the art at the time of the invention provide methods to directly bond semiconductor materials together at low temperatures without intervening insulating layers. This process represents a step beyond bonding individual semiconductor structures having insulating layers between them and being connected with conductive metal paths. The methods described in the '133 Patent were practiced in the art at the time of the invention.

27. Currently, technologies used to increase chip complexity are being accomplished with ever smaller feature sizes using semiconductor layers separated

by insulators connected in 3D stacks with conductive interconnect layers bridging between the isolated layers. The '133 and related patents and literature known in the art at the time of the invention provide 3D structures that can be bonded and interconnected at low temperatures.

VI. Applied Constructions

28. I understand the construction of “nearly-amorphized layer” to be a layer that at least closely approximates an amorphous layer.

29. I understand the construction of “a few nm in thickness” encompasses at least 165 nm (1650 Å).

VII. Application of the Cheung Reference

30. Cheung at Col. 3:49-50 describes implanting a surface of a first substrate to create a compliant layer (e.g., amorphous silicon layer). Cheung uses the terms “compliant layer” and “amorphous layer” interchangeably. Cheung at Col. 5:66 describes forming an amorphous layer using an implant of a “silicon bearing particle.” Cheung at Col. 6:52 describes that other types of particles including “germanium or hydrogen” may also be used to form an amorphous layer. Cheung at Col. 8:15–18, Col. 8:32–36 and FIG. 3 describes a first silicon substrate having an amorphous layer formed uniformly over a surface. Cheung at Col. 8:21–23, Col. 8:32–36 describes using the same process to form a second amorphous layer

for a second substrate. Since Cheung describes first and second amorphous layers, Cheung describes layers that at least closely approximate respective amorphous layers, *i.e.*, “nearly-amorphized layer[s].” Cheung at Col. 8:26–29, Col. 8:32–36 describes bonding the substrates together using the first and second amorphous layers.

31. Cheung at Col. 4:15–20 and Col. 5:4–7 describes substrates doped with impurities including boron or arsenic. A person having ordinary skill in the art would understand that the doping with boron or arsenic can be performed during the formation of the crystal that results in the wafer or by ion implantation. Under either circumstance, a distribution of boron or arsenic will be present throughout the wafer, including Cheung’s amorphous layers. Further, boron or arsenic will also be present at the surface of the wafer, *e.g.*, the surface of the amorphous layer, based on this distribution. Thus, Cheung describes a first amorphous layer, *e.g.*, a first nearly-amorphized layer, of a first substrate that contains one of boron and arsenic bonded to a second amorphous layer, *e.g.*, a second nearly-amorphized layer, of a second substrate that contains one of boron and arsenic. Specifically, when the wafer is boron doped, the wafer, amorphous layer, and surface of the amorphous layer will contain boron. Specifically, when the wafer is arsenic doped, the wafer, amorphous layer, and surface of the amorphous layer will contain arsenic.

32. Cheung describes bonding wafers to form “multi-layered integrated circuit devices [and] three-dimensional packaging of integrated semiconductor devices.” *See, e.g.*, Col. 1:17–21. It would have been obvious to a person having ordinary skill in the art at the time of the invention to use Cheung’s teachings to bond an amorphous layer, e.g., a nearly-amorphized layer, of an additional substrate to another amorphous layer, e.g., a nearly-amorphized layer, of one of the bonded first and second substrates in order to form a multi-layered integrated circuit device or a 3D package as described in Cheung.

33. Cheung at Col. 8:10–65 describes embodiments for bonding first and second amorphous layers for respective first and second substrates, which may be silicon. This process sequence includes the steps of “cleaning” each of the wafer surfaces followed by “stripping” each of the wafer surfaces. This sequence of steps is included to remove any contaminants from each of the wafer surfaces prior to bonding the two wafers together. In the instance in which both wafers are silicon, the goal of the wafer “stripping” step is to remove, for example, a native oxide layer and any contaminants. Then, during the “joining” step (Step 9) and the bonding step (Step 10), the bond that is formed is between silicon atoms present on each wafer surface, and the resulting bond is covalent, since silicon-to-silicon bonding occurs by covalent bonding. Further, Cheung describes the resulting bonded wafers as silicon-on-silicon at Col. 9:55–57. Claim 19 of Cheung further

describes the formation of a silicon-on-silicon wafer and Claim 23 describes a method of forming “silicon-on-silicon epi-like substrates.” For Cheung’s bonded substrates to be “epi-like,” the bond between the silicon atoms at the location of the wafer-to-wafer bond interface must be the same as the bonds in the bulk of the silicon substrates themselves, which are silicon covalent bonds. Thus, Cheung describes the formation of silicon covalent bonds between the first and second substrates.

34. Using normal methods of experimentation, a person of ordinary skill in the art at the time of the invention could form amorphous layers in the range of a few nm in thickness as recited in Claim 10 for bonding amorphous layers. This thickness range would have been chosen to allow for the partial recrystallization of the amorphous layers following the bonding of the amorphous layers described in Cheung. Cheung at Col. 6:10–15 describes forming an amorphous layer over a surface that is about 10nm to about 500nm in thickness, which includes a thickness of 165 nm. Cheung describes a low temperature anneal to further bond substrates together. *See, e.g.*, Col. 8:29–30. The low temperature anneal may recrystallize a portion of the amorphous silicon material. *See, e.g.*, Col. 7:57–59. Thus, starting with an amorphous layer having a thickness of up to 500nm, a person having ordinary skill in the art at the time of the invention could select an anneal as taught

or suggested by Cheung to reduce the thickness of the amorphous layer to a few nm in thickness as recited in Claim 10.

35. Argon is element 18 on the periodic table of elements. Argon is an inert gas.

36. Cheung at Col. 3:49-50 describes implanting a surface of a first substrate to create a compliant layer (e.g., amorphous silicon layer). Cheung uses the terms “compliant layer” and “amorphous layer” interchangeably. Cheung at Col. 5:66 describes forming an amorphous layer using an implant of a “silicon bearing particle.” Cheung at Col. 6:52 describes that other types of particles including “germanium or hydrogen” can also be used to form an amorphous layer. Cheung at Col. 8:15–18, Col. 8:32–36 and FIG. 3 describes a first substrate having an amorphized layer formed substantially only in a first surface. Cheung at Col. 8:21-23, Col. 8:32–36 describes using the same process to form a second amorphized layer substantially only in a second surface of a second substrate. Cheung at Col. 8:26–29, Col. 8:32–36 describes bonding the substrates together using the first and second amorphous layers.

37. Cheung at Col. 4:15–20 and Col. 5:4–7 describes substrates doped with impurities including boron or arsenic. A person having ordinary skill in the art would understand that the doping with boron or arsenic can be performed during the formation of the crystal that results in the wafer or by ion implantation. Under either circumstance, a distribution of boron or arsenic will be present throughout

the wafer, including Cheung's amorphous layers. Further, boron or arsenic will also be present at the surface of the wafer, e.g., the surface of the amorphous layer, based on this distribution. Thus, Cheung describes a first substrate that contains one of boron and arsenic bonded to a second substrate that contains one of boron and arsenic. Specifically, when the wafer is boron doped, the wafer, amorphous layer, and surface of the amorphous layer will contain boron. Specifically, when the wafer is arsenic doped, the wafer, amorphous layer, and surface of the amorphous layer will contain arsenic.

38. Cheung describes bonding wafers to form “multi-layered integrated circuit devices [and] three-dimensional packaging of integrated semiconductor devices.” *See, e.g.*, Col. 1:17–21. It would have been obvious to a person having ordinary skill in the art at the time of the invention to use Cheung's teachings to bond a surface of an additional substrate that is amorphized substantially only in its surface to another surface of one of the bonded first and second substrates, the surface being amorphized substantially only therein in order to form a multi-layered integrated circuit device or a 3D package as described in Cheung.

VIII. Cheung in view of Saito

39. Cheung and Saito both describe forming amorphous layers on substrates using plasma ion implants of silicon. *See, e.g.*, Cheung at Col. 2:35–40, Col. 5:63–

66, Col. 6:2–6, Col. 6:50–53, Col. 8:10–55; See, e.g., Saito at Col. 2:40–59; 3:32–37. Cheung at Col. 1:16–23 describes that substrates may be bonded together to form integrated circuit devices, 3D IC devices, etc. Cheung at Col. 5:4–7 describes that substrates doped with impurities such as, for example, boron, arsenic and/or phosphorus, may be bonded together. Saito at Col. 2:46–59 describes that a surface of a substrate may be made amorphous and doped simultaneously using plasma ion implants of silicon and an impurity, such as boron, arsenic and/or phosphorus. Using the teachings of Cheung and Saito, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the plasma ion implantation of silicon discussed in Cheung for the formation of amorphous layers, *e.g.*, nearly-amorphized layers and/or materials amorphized substantially only in a respective surface, in substrates by simultaneously including one of boron and arsenic in the plasma ion implantations as described by Saito, such that the amorphous layers contain one of boron and arsenic, to dope the surfaces of the substrates with one of boron and arsenic for the formation of a device in the surfaces. Further, it would have been obvious to use boron in the plasma ion implantations to form a P-type doped region in the surfaces of the substrates for a device. Also, it would have been obvious to use arsenic in the plasma ion implantations to form an N-type doped region in the surfaces of the substrates for a device.

40. Cheung and Saito both describe forming amorphous layers on substrates using plasma ion implants of silicon. See, e.g., Cheung at Col. 2:35–40, Col. 5:63–66, Col. 6:2–6, Col. 8:10–55; See, e.g., Saito at Col. Col. 2:40–59; 3:30–43. Cheung at Col. 5:4–7 describes that substrates doped with impurities such as, for example, boron may be bonded together. Saito at Col. 2:46–59, Col. 3:30–43 describes that a surface of a substrate may be made amorphous and simultaneously doped using plasma ion implants of silicon and an impurity, such as boron. Cheung at Col. 2:18–23 describes low-temperature bonding of amorphous layers and at Col. 9:38 describes a low-temperature anneal of 550° C. When boron is used in the plasma ion implantation of the silicon substrate, as discussed above, boron will be at the surface of the silicon substrate. Thus, when the boron-doped silicon substrates are bonded, boron-boron and silicon covalent bonds form between the bonded substrates.

41. Cheung and Saito each describe one or more techniques for introducing atoms, which include boron or another species, into the surface of a substrate. Cheung describes using an “ion shower” or “plasma immersion ion implantation” at Col. 5:63–64. Saito describes doping a substrate using a plasma containing ions of phosphorus, boron or arsenic. One of ordinary skill in the art would know that by controlling the dose and energy of a boron species in an ion shower or ion

implantation, a region having a thickness of a few monolayers at or near the surface of the substrate would be boron rich.

42. Cheung and Saito both describe forming amorphous layers on substrates using plasma ion implants of silicon. See, e.g., Cheung at Col. 2:35–40, Col. 5:63–66, Col. 6:2–6, Col. 6:50–53, Col. 8:10–55; See, e.g., Saito at Col. 3:30–43. Saito at Col. 4:26–27 and FIG. 1 describes that argon may be used as a carrier gas for the plasma ion implants. In addition, it was well known by persons having ordinary skill in the art at the time of the invention that inert plasma gasses such as argon or helium could be used as carrier gasses during plasma ion implantation. It would have been obvious to a person having ordinary skill in the art at the time of the invention to use an inert gas plasma, such as the argon described in Saito, as a carrier gas during the plasma ion implantation of silicon described in Cheung for the formation of Cheung’s first and second amorphous layers since using such an inert gas plasma as a carrier was common in plasma ion implantation techniques. This, in turn, would expose Cheung’s first and second surfaces to an inert gas plasma.

IX. Cheung in view of Tian

43. Cheung describes forming amorphous layers on substrates using ion implants of silicon. See, e.g., Cheung at Col. 5:63–66. Cheung at Col. 1:16–23

describes that substrates may be bonded together to form integrated circuit devices, 3D IC devices, etc. Cheung at Col. 5:4–7 describes that substrates doped with impurities such as, for example, boron, arsenic and/or phosphorus, may be bonded together. Tian describes processes for forming doped amorphous layers by implanting ions of arsenic or boron into single-crystal silicon. See, e.g., Abstract, pp. 1226, 1230. It would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the plasma ion implantation of silicon discussed in Cheung in the formation of amorphous layers, *e.g.*, nearly-amorphized layers and/or materials amorphized substantially only in a respective surface, in substrates by simultaneously including one of boron and arsenic in the ion implantation, as taught or suggested by Tian, such that the amorphous layers contain one of boron and arsenic, to dope the surfaces of the substrates with one of boron and arsenic for the formation of a device in the surfaces. Further, it would have been obvious to use boron in the plasma ion implantations to form a P-type doped region in the surfaces of the substrates for a device. Also, it would have been obvious to use arsenic in the plasma ion implantations to form an N-type doped region in the surfaces of the substrates for a device.

44. Cheung and Tian each describe one or more techniques for introducing atoms, which include boron or another species, into the surface of a substrate. Cheung describes using an “ion shower” or “plasma immersion ion implantation”

at Col. 5:63–64. Tian describes doping a substrate using an ion implantation of phosphorus, boron or arsenic. One of ordinary skill in the art would know that by controlling the dose and energy of a boron species in an ion shower or ion implantation, a region having a thickness of a few monolayers at or near the surface of the substrate would be boron rich.

X. Cheung in view of Tian and in further view of Saito

45. Cheung and Saito both describe forming amorphous layers on substrates using implants of silicon. See, e.g., Cheung at Col. 5:66; Saito at Col. 3:32–37. Cheung at Col. 1:16–23 describes that substrates may be bonded together to form integrated circuit devices, 3D IC devices, etc. Cheung at Col. 5:4–7 describes that substrates doped with impurities such as, for example, boron, arsenic and/or phosphorus, may be bonded together. Saito at Col. 2:46–59 describes that a surface of a substrate may be made amorphous and doped simultaneously using plasma ion implants of silicon and an impurity, such as boron, arsenic and/or phosphorus. Tian describes processes for forming doped amorphous layers by implanting arsenic or boron into single-crystal silicon. See, e.g., Abstract, pp. 1226, 1230. It would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the ion implantation, as taught or suggested by Cheung and/or Tian, to be a plasma ion implantation with silicon ions and

boron or arsenic ions, as taught or suggested by Saito, to dope the surfaces of the substrates with one of boron and arsenic for the formation of a device in the surfaces. Further, it would have been obvious to use boron in the plasma ion implantations to form a P-type doped region in the surfaces of the substrates for a device. Also, it would have been obvious to use arsenic in the plasma ion implantations to form an N-type doped region in the surfaces of the substrates for a device.

46. Cheung and Saito both describe forming amorphous layers on substrates using plasma ion implants of silicon. See, e.g., Cheung at Col. 2:35–40, Col. 5:63–66, Col. 6:2–6, Col. 8:10–55; See, e.g., Saito at Col. Col. 2:40–59; 3:30–43. Cheung at Col. 5:4–7 describes that substrates doped with impurities such as, for example, boron may be bonded together. Saito at Col. 2:46–59, Col. 3:30–43 describes that a surface of a substrate may be made amorphous and simultaneously doped using plasma ion implants of silicon and an impurity, such as boron. Tian describes processes for forming doped amorphous layers by implanting arsenic or boron into single-crystal silicon. See, e.g., Abstract, pp. 1226, 1230. Cheung at Col. 2:18–23 describes low-temperature bonding of amorphous layers and at Col. 9:38 describes a low-temperature anneal of 550° C. When boron is used in the plasma ion implantation of the silicon substrate, as discussed above, boron will be at the surface of the silicon substrate. Thus, when the boron-doped silicon

substrates are bonded, boron-boron and silicon covalent bonds form between the bonded substrates.

47. Cheung and Saito both describe forming amorphous layers on substrates using plasma ion implants of silicon. See, e.g., Cheung at Col. 2:35–40, Col. 5:63–66, Col. 6:2–6, Col. 6:50–53, Col. 8:10–55; See, e.g., Saito at Col. 3:30–43. Saito at Col. 4:26–27 and FIG. 1 describes that argon may be used as a carrier gas for the plasma ion implants. Tian describes processes for forming doped amorphous layers by implanting arsenic or boron into single-crystal silicon. See, e.g., Abstract, pp. 1226, 1230. In addition, it was well known by persons having ordinary skill in the art at the time of the invention that inert plasma gasses such as argon or helium could be used as carrier gasses during plasma ion implantation. It would have been obvious to a person having ordinary skill in the art at the time of the invention to use an inert gas plasma, such as the argon described in Saito, as a carrier gas during the plasma ion implantation of silicon described in Cheung and/or Tian for the formation of first and second amorphous layers since using such an inert gas plasma as a carrier was common in plasma ion implantation techniques. This, in turn, would expose the first and second surfaces to an inert gas plasma.

XI. Application of the Fujino Reference

48. Fujino at page 1322 describes bonding silicon wafers having amorphous surfaces formed thereon. Fujino describes implanting silicon ions into boron-doped CZ-grown silicon wafers to form the amorphous layers. See, e.g., at page 1322. Since Fujino describes amorphous layers, Fujino describes layers that at least closely approximate respective amorphous layers, *i.e.*, “nearly-amorphized layer[s].” Fujino at 1322-1323 describes bonding the substrates together using the amorphous layers.

49. Fujino at page 1322 describes boron-doped CZ-grown silicon wafers. A person having ordinary skill in the art would understand that the doping with boron can be performed during the formation of the crystal that results in the wafer or by ion implantation. Under either circumstance, a distribution of boron will be present throughout the wafer, including Fujino’s amorphous layers. Further, boron will also be present at the surface of the wafer, e.g., the surface of the amorphous layer, based on this distribution. Thus, Fujino describes a first amorphous layer, e.g., a first nearly-amorphized layer, of a wafer that contains one of boron and arsenic bonded to a second amorphous layer, e.g., a second nearly-amorphized layer, of a wafer that contains one of boron and arsenic. Specifically, when the wafer is boron doped, the wafer, amorphous layer, and surface of the amorphous layer will contain boron.

50. Fujino at page 1322 describes embodiments for bonding amorphous layers for respective wafers, which are silicon. This process sequence includes the steps of “Removal of contamination” followed by “Surface treatment” for each of the wafer surfaces. This sequence of steps is included to remove any contaminants from each of the wafer surfaces prior to bonding the two wafers together. Further, Fujino at page 1324 teaches the elimination of a native oxide. Then, during the “Wafer contact” and “Annealing” steps, the bond that is formed is between silicon atoms present on each wafer surface, and the resulting bond is covalent, since silicon-to-silicon bonding occurs by covalent bonding. Thus, Fujino describes the formation of silicon covalent bonds between the wafers.

51. Using normal methods of experimentation, a person of ordinary skill in the art at the time of the invention could form amorphous layers in the range of a few nm in thickness as recited in Claim 10 for bonding amorphous layers. Fujino at page 1323 describes forming an amorphous layer over a surface that is to a depth of 139 nm, which is within a thickness of 165 nm. Fujino at page 1322 describes varying the thickness of the amorphous layer by adjusting the acceleration energy of the implant. Thus, based on these descriptions, a person having ordinary skill in the art at the time of the invention could select a thickness of the amorphous layer as taught or suggested by Fujino by adjusting the acceleration energy of the implant to achieve a few nm in thickness as recited in Claim 10.

52. Fujino at page 1322 describes implanting silicon ions into boron-doped CZ-grown silicon wafers to form the amorphous layers. Fujino at page 1322 describes a first substrate having an amorphized layer formed substantially only in a first surface. Fujino at page 1322 describes using the same process to form a second amorphized layer substantially only in a second surface of a second substrate. Fujino at page 1322 describes bonding the substrates together using the first and second amorphous layers.

53. Fujino at page 1322 describes boron-doped silicon wafers. A person having ordinary skill in the art would understand that the doping with boron can be performed during the formation of the crystal that results in the wafer or by ion implantation. Under either circumstance, a distribution of boron will be present throughout the wafer, including Fujino's amorphous layers. Further, boron will also be present at the surface of the wafer, e.g., the surface of the amorphous layer, based on this distribution. Thus, Fujino describes a first substrate that contains one of boron and arsenic bonded to a second substrate that contains one of boron and arsenic. Specifically, when the wafer is boron doped, the wafer, amorphous layer, and surface of the amorphous layer will contain boron.

XII. Fujino in view of Saito

54. Fujino and Saito both describe forming amorphous layers using implants of silicon. See, e.g., Fujino at p. 1322; Saito at Col. 3:32–37. Fujino at page 1322 describes bonding wafers to form power devices such as power transistors, isolated vertical-DMOS circuits and control circuits on a single chip. Fujino at page 1322 describes bonding together boron doped wafers. Saito at Col. 2:46–59 describes that a surface of a substrate may be made amorphous and doped simultaneously using plasma ion implants of silicon and an impurity, such as boron, arsenic and/or phosphorus. It would have been obvious to a person having ordinary skill in the art at the time of the invention to implant Fujino’s wafers to form the amorphous layers using a plasma containing silicon or germanium ions and boron or arsenic ions, as described in Saito, such that the amorphous layers contain one of boron and arsenic, in order to dope surfaces with one of boron and arsenic for the formation of a device in the surfaces. Further, it would have been obvious to use boron in the plasma ion implantations to form a P-type doped region in the surfaces of the substrates for a device. Also, it would have been obvious to use arsenic in the plasma ion implantations to form an N-type doped region in the surfaces of the substrates for a device.

55. Fujino and Saito both describe forming amorphous layers using implants of silicon. See, e.g., Fujino at p. 1322; Saito at Col. 3:32–37. Fujino at page 1322

describes bonding wafers to form power devices such as power transistors, isolated vertical-DMOS circuits and control circuits on a single chip. Fujino at page 1322 describes bonding together boron doped wafers. Saito at Col. 2:46–59, Col. 3:30–43 describes that a surface of a substrate may be made amorphous and simultaneously doped using plasma ion implants of silicon and an impurity, such as boron. Fujino in Figure 1 describes bonding of amorphous layers at room temperature and then describes an anneal of 600° C. When boron is used in the plasma ion implantation of the silicon substrate, as discussed above, boron will be at the surface of the silicon substrate. Thus, when the boron-doped silicon substrates are bonded, boron-boron and silicon covalent bonds form between the bonded substrates.

56. Fujino and Saito both describe forming amorphous layers using implants of silicon. See, e.g., Fujino at p. 1322; Saito at Col. 3:32–37. Saito describes doping a substrate using a plasma containing ions of phosphorus, boron or arsenic. One of ordinary skill in the art would know that by controlling the dose and energy of a boron species in an ion shower or ion implantation, a region having a thickness of a few monolayers at or near the surface of the substrate would be boron rich.

57. Fujino and Saito both describe forming amorphous layers using implants of silicon. See, e.g., Fujino at p. 1322; Saito at Col. 3:32–37. Saito at Col. 4:26–27 and FIG. 1 describes that argon may be used as a carrier gas for the plasma ion

implants. In addition, it was well known by persons having ordinary skill in the art at the time of the invention that inert plasma gasses such as argon or helium could be used as carrier gasses during plasma ion implantation. It would have been obvious to a person having ordinary skill in the art at the time of the invention to use an inert gas plasma, such as the argon described in Saito, as a carrier gas during the plasma ion implantation of silicon described in Fujino for the formation of Fujino's first and second amorphous layers since using such an inert gas plasma as a carrier was common in plasma ion implantation techniques. This, in turn, would expose Fujino's first and second surfaces to an inert gas plasma.

XIII. Fujino in view Tian

58. Fujino describes forming amorphous layers using implants of silicon. See, e.g., Fujino at p. 1322. Fujino at page 1322 describes bonding wafers to form power devices such as power transistors, isolated vertical-DMOS circuits and control circuits on a single chip. Fujino at page 1322 describes bonding together boron doped wafers. Tian describes processes for forming doped amorphous layers by implanting arsenic or boron into single-crystal silicon. See, e.g., Abstract, pp. 1226, 1230. It would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the ion implantation of silicon, as taught by Fujino, in the formation of amorphous layers, *e.g.*, nearly-amorphized

layers and/or materials amorphized substantially only in a respective surface, in wafers to include boron or arsenic in the ion implantation, as taught or suggested by Tian, such that the amorphous layers contain one of boron and arsenic, to dope these surfaces of substrates with one of boron and arsenic for the formation of a device in the surfaces. Further, it would have been obvious to use boron in the plasma ion implantations to form a P-type doped region in the surfaces of the substrates for a device. Also, it would have been obvious to use arsenic in the plasma ion implantations to form an N-type doped region in the surfaces of the substrates for a device.

59. Fujino describes forming amorphous layers using implants of silicon. See, e.g., Fujino at p. 1322. Tian describes processes for forming doped amorphous layers by implanting arsenic or boron ions into single-crystal silicon. See, e.g., Abstract, pp. 1226, 1230. One of ordinary skill in the art would know that by controlling the dose and energy of a boron species in an ion shower or ion implantation, a region having a thickness of a few monolayers at or near the surface of the substrate would be boron rich.

XIV. Fujino in view of Tian and in further view of Saito

60. Fujino and Saito both describe forming amorphous layers using implants of silicon. See, e.g., Fujino at p. 1322; Saito at Col. 3:32–37. Fujino at page 1322

describes bonding wafers to form power devices such as power transistors, isolated vertical-DMOS circuits and control circuits on a single chip. Fujino at page 1322 describes bonding together boron doped wafers. Saito at Col. 2:46–59 describes that a surface of a substrate may be made amorphous and doped simultaneously using plasma ion implants of silicon and an impurity, such as boron, arsenic and/or phosphorus. Tian describes processes for forming doped amorphous layers by implanting arsenic or boron into single-crystal silicon. See, e.g., Abstract, pp. 1226, 1230. It would have been obvious to persons having ordinary skill in the art at the time of the invention to modify the ion implantation, as taught or suggested by Fujino and/or Tian, to be a plasma ion implantation with silicon ions and boron or arsenic ions, as taught or suggested by Saito, to dope the surfaces of the substrates with one of boron and arsenic for the formation of a device in the surfaces. Further, it would have been obvious to use boron in the plasma ion implantations to form a P-type doped region in the surfaces of the substrates for a device. Also, it would have been obvious to use arsenic in the plasma ion implantations to form an N-type doped region in the surfaces of the substrates for a device.

61. Fujino and Saito both describe forming amorphous layers using implants of silicon. See, e.g., Fujino at p. 1322; Saito at Col. 3:32–37. Fujino at page 1322 describes bonding wafers to form power devices such as power transistors, isolated

vertical-DMOS circuits and control circuits on a single chip. Fujino at page 1322 describes bonding together boron doped wafers. Saito at Col. 2:46–59, Col. 3:30–43 describes that a surface of a substrate may be made amorphous and simultaneously doped using plasma ion implants of silicon and an impurity, such as boron. Tian describes processes for forming doped amorphous layers by implanting arsenic or boron into single-crystal silicon. See, e.g., Abstract, pp. 1226, 1230. Fujino in Figure 1 describes bonding of amorphous layers at room temperature and then describes an anneal of 600° C. When boron is used in the plasma ion implantation of the silicon substrate, as discussed above, boron will be at the surface of the silicon substrate. Thus, when the boron-doped silicon substrates are bonded, boron-boron and silicon covalent bonds form between the bonded substrates.

62. Fujino and Saito both describe forming amorphous layers using implants of silicon. See, e.g., Fujino at p. 1322; Saito at Col. 3:32–37. Tian describes processes for forming doped amorphous layers by implanting arsenic or boron into single-crystal silicon. See, e.g., Abstract, pp. 1226, 1230. Saito at Col. 4:26–27 and FIG. 1 describes that argon may be used in a plasma as a carrier gas for the ion implants. In addition, it was well known by persons having ordinary skill in the art at the time of the invention that inert plasma gasses such as argon or helium could be used as carrier gasses during plasma ion implantation. It would have been

obvious to a person having ordinary skill in the art at the time of the invention to use an inert gas plasma, such as the argon described in Saito, as a carrier gas during the ion implantation of silicon described in Fujino and/or Tian for the formation of first and second amorphous layers since using such an inert gas plasma as a carrier was common in plasma ion implantation techniques. This, in turn, would expose the first and second surfaces to an inert gas plasma.

XV. Fujino alone or in view of Saito and/or Tian, and in further view of Cheung

63. Fujino at page 1322 describes bonding silicon wafers having amorphous surfaces formed thereon. Fujino at page 1322 describes bonding wafers to form power devices such as power transistors, isolated vertical-DMOS circuits and control circuits on a single chip. Cheung describes bonding wafers having amorphous surfaces formed thereon in order to form “three-dimensional packaging of integrated semiconductor devices.” See, e.g., Col. 1:19–21; Col. 8:10–48. It would have been obvious to a person having ordinary skill in the art at the time of the invention to use Cheung’s teachings to bond an additional substrate being amorphized substantially only in its surface to another amorphized layer of one of the bonded first and second substrates in order to form a 3D integrated semiconductor device having power transistors, isolated vertical-DMOS circuits and control circuit chips on a single chip as described by Fujino.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made herein on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine, or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed this 1st day of Nov., 2013 at Santa Clara County, CA.

Richard A. Blanchard

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