

**Thomson Reuters Expert Witness Services
Consultant Curriculum Vitae**

Richard A. Blanchard, Ph.D.

Expertise

- MOS and Bipolar Device Technology
 - Semiconductor Device Physics
 - Microchip Fabrication & Analysis
 - Electronic Systems
 - Electrical & Electronic Failures
 - ESD & EOS Failures
 - Assembly & Packages
 - CMOS, DMOS & BiCMOS Technology
 - Power IC's & Power Electronics
 - Printed Circuit Board Manufacturing
 - Printable Electronics, including LEDs
 - Semiconductor Process & Control
 - Patents & Trade Secrets
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Professional Summary

Dr. Blanchard has over 40 years of combined industry, research, academic, and consulting experience. His research covers semiconductor device and electronics design, semiconductor device physics, semiconductor manufacturing processes and equipment, failure analysis, and reverse engineering of semiconductor devices and electronic circuits. Dr. Blanchard is a named inventor on more than 160 issued U.S. patents. As a result, he has been involved in numerous patent and trade secret litigation matters including a number of ITC proceedings. He has also authored or co-authored books and articles dealing with semiconductor design, process development, and failure analysis.

Employment History

From: 1991, **Blanchard Associates**
2008-
To: Present Mountain View, CA
Position: *2008-Present: Industry Consultant and Expert Witness*
Blanchard Associates specializes in working with both start-ups and established companies in the development of new products as well as intellectual property. His projects have included the development of improved low voltage and high voltage MOS-gated devices and the development of printable electronics such as LEDs and discrete transistors. This work has included the identification of patentable material and work to protect this material. He is also an Exclusive Expert for SVEWG.

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- From: 1998 **Silicon Valley Expert Witness Group, Inc.**
To: 2007 Mountain View, CA
Position: *Exclusive Expert and Consultant*
Silicon Valley Expert Witness Group, Inc. (SVEWG) is a high technology, "Silicon Valley" consulting company specializing in expert witness litigation support and technology consulting. SVEWG has an extensive roster of world-class technology experts used in the defense and promotion of intellectual property rights and other litigation disputes. SVEWG Principals offer extensive in-house technology, legal and business expertise and have direct access to senior litigation and technology consultants worldwide.
- From: 1991 **Failure Analysis Associates, Inc. (Now named "Exponent")**
To: 1998 Menlo Park, CA
Position: *Principal Engineer & Division Manager*
Responsible for the Electrical/Electronic Division of Failure Analysis Associates providing consulting services to the electrical and electronics industry. Specific duties include:
- Semiconductor devices. Failure analysis and reverse engineering of solid-state electronic components and circuits. Semiconductor processing and semiconductor process equipment. Semiconductor manufacturing and process control.
 - Failure analysis of electric and electronic systems, subsystems, and components, including causes of electrical fires
 - Reliability modeling and lifetime prediction of electrical and electronic systems and subsystems
 - Automotive electronics. Design of discrete devices and integrated circuits
 - Power Electronics. Power MOS and Smart Power Technologies
- From: 1987 **IXYS Corporation**
To: 1991 San Jose, CA
Position: *Senior Vice President*
Responsible for the development of IC products. Established an in-house CAD capability. Recruited an IC design team and coordinated the definition and development of IXYS ICs. Identified, qualified and monitored the IC foundries that manufactured these circuits. Set up testing capability at IXYS. Coordinated assembly on IC's. Worked on various MOSFET and IGBT device, test, and assembly problems.

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From: 1982 **Siliconix, Inc.**
To: 1987 Santa Clara, CA
Position: *Vice President, Engineering*
Other titles held at Siliconix, Inc. were Engineering Manager (1982-1983) and Director (1983-1984). Responsible for the development of advanced process technology and the design of both discrete devices (JFETs, lateral and vertical DMOS transistors) and integrated circuits (low and high voltage CMOS, D/CMOS and bipolar-JFET). Personally responsible for many key innovations and inventions in power MOS and D/CMOS IC technology and their assembly and test requirements. He submitted approximately 20 patent disclosures while employed at Siliconix, Inc. He holds the two key "trench FET" patents, of which he is the sole inventor.

From: 1976 **Supertex, Inc.**
To: 1982 Sunnyvale, CA
Position: *Founder and Vice President, MOS Power Products*
Responsible for investigation of new semiconductor devices and new technologies. In charge of Power MOS device research, design and development. His work lead to the design and development of both the discrete power MOS device family and the high voltage IC (HVIC) family sold by Supertex, Inc. Responsible for an in-house assembly area as well as engineering aspects of power MOS and HVIC testing.

From: 1976 **Cognition, Inc.**
To: 1978 Mountain View, CA
Position: *Founder and Consulting Engineer*
Responsible for developing the process technology for fabricating monolithic silicon pressure sensors. A process line was established for the manufacture of piezoresistive pressure sensors, including the precision etching of thin silicon diaphragms.

From: 1974 **Foothill College**
To: 1978 Los Altos Hills, CA
Position: *Associate Professor, Assistant Division Chairman, Engineering & Technology Division*
Accomplishments included developing the curriculum for the Semiconductor Technology Program, and establishing a small processing facility for teaching students the fundamentals of semiconductor technology. Supervised approximately 60 instructors in the evening and off-campus programs.

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From: 1974 **Independent Consultant**
To: 1976 Los Altos Hills, CA
Duties: Consultant to the semiconductor industry, including court appointed
“Special Master” in the Fairchild Semiconductor Corporation v.
National Semiconductor Corporation Isoplanar patent suit.

From: 1970 **Fairchild Semiconductor**
To: 1974 Mountain View, CA
Position: *Senior Engineer, Department Manager*
Responsible for the fabrication of the integrated circuits in the
Polaroid SX-70 camera. Technologies directly related to this work
include standard bipolar technology, bipolar- MOS technology,
silicon gate technology and flip-chip assembly technology.

Deposition and Trial Testimony (Past Five Years)

Anthony Bookhamer, Lena J. Tyron, Charles Thomas Martin, Jr., and Carl Disilvestro v.
Sunbeam Products, Inc., United States District Court, Northern District of California, Civil
Action No. 09-CV-06027 EMC (DMR).

Kentucky Farm Bureau Mutual Insurance Company v. Sunbeam Products, Inc., United States
District Court, Western District of Kentucky, Paducah Division, Civil Action No. 5:11-CV-
0098-R. (R, D)

Osram v. LG Electronics, United States International Trade Commission, Washington, DC, In
the matter of Certain light-Emitting Diodes and Products Containing the Same, Investigation
No. 337-TA-784. (D, R, T)

Thomas Post; Debra Ferguson, Bobbie Haskett, Michael Post, Laura Zedaker, and Margie
Zervos v. Sunbeam Products, Inc., United States District Court, Eastern District of California,
Case No. 2:11-CV-00792-JAM-CMK. (R, D)

Osram v. LG Electronics/Samsung, United States International Trade Commission,
Washington, DC, in the matter of Certain Light-Emitting Diodes and Products Containing the
Same, Investigation No. 337-TA-785. (D, R, Tutorial)

Nationwide Mutual Insurance Company v. Mack Wallbed Systems, in the Superior Court of the
State of California, County of Sonoma, Case No. SCV-247147. (D, T)

Richtek v. uPI, et al., In the matter of Certain DC-DC Controllers and Products Containing
Them, International Trade Commission, Washington, DC, Case No. 337-TA-698. (D, R, T)

Quality Investment Properties Santa Clara, Inc. v. Serrano Electric, Inc. and Peterson Power
Systems, Inc., and Serrano Electric, Inc. (Cross-Claimant) v. Peterson Power Systems, Inc.
(Cross-Defendant), United States District Court, Case No. 5:09-CV-05376LHK. (D, R)

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Michael J. Anderson and Deborah M. Anderson v. Sunbeam Products, Inc., Supreme Court of the State of New York County of Oswego, Case No. 08-2230. (D, R)

Security Mutual Insurance, et al. v. Sunbeam Products, Inc. et al., United States District Court Northern District of New York, Civil Action No.: 5:09-CV-0460. (D, R)

Coorstek, Inc. v. Steven F. Reiber and Mary L. Reiber, United States District Court, District of Colorado, Case No. 08-CV-01133-KMT-CBS. (D, R, Tutorial)

Nationwide Mutual Fire Insurance Company, as subrogee of Mildred Harrop v. Sunbeam Products, Inc., United States District Court, District of Rhode Island, C.A. No. 09-509/S. (D, R)

Kay A. Reed and Charlie Wear, Trust Administrators for the Vornado Liquidating Trust v. Tyco Electronics Corporation, Global Wire Technologies of Indiana, Inc. GWT Investments, Inc. and Unicable, Inc., Superior Court of California, Case No. CGC-05-441279. (D, T)

Jeffery Quist, as Trustee for the heirs and next of kin of Jerald Quist, Deceased, and Virginia Quist v. Sunbeam Products, Inc., d/b/a Jarden Consumer Solutions. (D, R)

Barbara Kay and James Kay v. Sunbeam Products, Inc., United States District Court, Western District of Missouri, Central Division, Case No. 2:09CV-4065-NKL. (D, R, T)

Tessera, Inc. v. United Test and Assembly Center, LTD and UTAC America, Inc., Superior Court of California, County of Alameda, Case No. RG08410327. (D)

Sun Yen v. Volkswagen Group of America, Inc., Superior Court of California, County of Alameda, Case No. RG08416335. (D)

LG Display Co., Ltd. v. Chi Mei Optoelectronics Corporation, AU Optronics Corporation, AU Optronics Corporation of America: Tatung Company, Tatung Company of America, Inc. and Viewsonic Corporation, United States District Court, District of Delaware, Civil Action No. 06-726 (JJF). (D, R)

Safeco Insurance Company of Illinois v. BSH Home Appliances Corporation and Chun Yuen Ng, Superior Court of California, County of San Francisco, Case No. 060-08-471246. (D)

Olivia Evans, et al. v. G3 Energy, LLC, et al., Alameda County Superior Court Case No.: VG-05-218563. (D)

State Farm Fire and Casualty Co., as Subrogee of Benjamin Parr and June Parr, and Benjamin Parr and June Parr, Individually v. Sunbeam Products, Inc., United States District Court, Central District, Peoria Division, Case No. 1:06-CV-01208. (D, R, T)

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Safeco Insurance v. Eaton Electrical, Inc., et al., Marin Superior Court, Case No. 60820. (D)

Quantum Research Group v. Apple Computer Company, Inc., Cypress Semiconductor Corp., Cypress Microsystems, and Fingerworks, Inc., Unites States District of Maryland, Civil Action No. 1:05-CV-03408-WMN. (D, R)

Nathan J. Sheridan v. Fladeboe Volkswagen, Inc., Volkswagen of America, Inc., Superior Court of the State of California for the County of Orange, Case No. 06CC09510. (D, T)

Underlined Party Indicates Provided: Deposition (D), Report (R), or Testimony in Court (T)

Patents

| <u>Patent Number</u> | <u>Date Issued</u> | <u>Title</u> |
|----------------------|--------------------|---|
| 8,330,213 | 12/11/2010 | Power Semiconductor Devices, Methods, and Structures with Embedded Dielectric Layers Containing Permanent Charges |
| 8,330,217 | 12/11/2010 | Devices, Methods, and Systems with MOS-Gated Trench-to-Trench Lateral, Current Flow |
| 8,133,768 | 03/13/2012 | Method of Manufacturing a Light Emitting Photovoltaic or Other Electronic Apparatus and System |
| 8,049,271 | 11/01/2011 | Power Semiconductor Device Having a Voltage Sustaining Layer with a Terraced Trench Formation of Floating Islands |
| 7,989,293 | 08/02/2011 | Trench Device Structure and Fabrication |
| 7,825,492 | 11/02/2010 | Isolated Vertical Power Device Structure with Both N-Doped and P-Doped Trenches |
| 7,745,885 | 06/29/2010 | High Voltage Power MOSFET Having Low On-Resistance |
| 7,736,976 | 06/15/2010 | Method for Fabricating a Power Semiconductor Device Having a Voltage Sustaining Layer with a Terraced Trench Facilitating Formation of Floating Islands |
| 7,705,397 | 04/27/2010 | Devices, Methods, and Systems with MOS-Gated Trench-to-Trench Lateral Current Flow |
| 7,704,842 | 04/27/2010 | Lateral High-Voltage Transistor with Vertically-Extended Voltage-Equalized Drift Region |
| 7,586,165 | 09/08/2009 | Microelectromechanical Systems (MEMS) Device Including a Superlattice |
| 7,586,148 | 09/08/2009 | Power Semiconductor Device Having a Voltage Sustaining Region that Includes Doped Columns Formed by Terraced Trenches |
| 7,557,394 | 07/07/2009 | High-Voltage Transistor Fabrication with Trench Etching Technique |
| 7,544,544 | 06/09/2009 | Low Capacitance Two-Terminal Barrier Controlled TVS Diodes |
| 7,535,041 | 05/19/2009 | Method for Making a Semiconductor Device Including Regions of Band-Engineered Semiconductor Superlattice to Reduce Device-On Resistance |
| 7,531,850 | 05/12/2009 | Semiconductor Device Including a Memory Cell with a Negative |

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| 7,531,829 | 05/12/2009 | Differential Resistance (NDR) Device Semiconductor Device Including Regions of Band-Engineered Semiconductor Superlattice to Reduce Device-On Resistance |
| 7,504,305 | 03/17/2009 | Technique for Forming the Deep Doped Regions in Superjunction Devices |
| 7,473,966 | 01/06/2009 | Oxide-Bypassed Lateral High Voltage Structures and Methods |
| 7,442,584 | 10/28/2008 | Isolated Vertical Power Device Structure with Both N-Doped and P- Doped Trenches |
| 7,411,249 | 08/12/2008 | Lateral High-Voltage Transistor with Vertically-Extended Voltage- Equalized Drift Region |
| 7,397,097 | 07/08/2008 | Integrated Released Beam Layer Structure Fabricated in Trenches and Manufacturing Method Thereof |
| 7,339,252 | 03/04/2008 | Semiconductor Having Thick Dielectric Regions |
| 7,304,347 | 12/04/2007 | Method for Fabricating a Power Semiconductor Device Having a Voltage Sustaining Layer with a Terraced Trench Facilitating Formation of Floating Islands |
| 7,244,970 | 07/17/2007 | Low Capacitance Two-Terminal Barrier Controlled TVS Diodes |
| 7,224,027 | 05/29/2007 | High Voltage Power MOSFET Having a Voltage Sustaining Region that Includes Doped Columns Formed by Trench Etching and Diffusion from Regions of Oppositely Doped Polysilicon |
| 7,202,494 | 04/10/2007 | FinFET Including a Superlattice |
| 7,199,427 | 04/03/2007 | DMOS Device with a Programmable Threshold Voltage |
| 7,138,289 | 11/21/2006 | Technique for Fabricating Multilayer Color Sensing Photodetectors |
| 7,094,621 | 08/22/2006 | Fabrication on Diaphragms and "Floating" Regions of Single Crystal Semiconductor for MEMS Devices |
| 7,091,552 | 08/15/2006 | High Voltage Power MOSFET Having a Voltage Sustaining Region that Includes Doped Columns Formed by Trench Etching and Ion Implantation |
| 7,084,455 | 08/01/2006 | Power Semiconductor Device Having a Voltage Sustaining Region that Includes Terraced Trench with Continuous Doped Columns Formed in an Epitaxial Layer |
| 7,067,376 | 06/27/2006 | High Voltage power MOSFET Having Low On-Resistance |
| 7,061,072 | 06/13/2006 | Integrated Circuit Inductors Using Driven Shields |
| 7,023,069 | 04/04/2006 | Method for Forming Thick Dielectric Regions Using Etched Trenches |
| 7,019,360 | 03/28/2006 | High Voltage Power MOSFET Having a Voltage Sustaining Region that Includes Doped Columns Formed by Trench Etching Using an Etchant Gas that is also a Doping Source |
| 7,015,104 | 03/21/2006 | Technique for Forming the Deep Doped Columns in Superjunction |
| 6,992,350 | 01/31/2006 | High Voltage Power MOSFET Having Low On-Resistance |
| 6,949,432 | 09/27/2005 | Trench DMOS Transistor Structure Having a Low Resistance Path to a Drain Contact Located on an Upper Surface |
| 6,921,938 | 07/26/2005 | Double Diffused Field Effect Transistor Having Reduced On- Resistance |

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| 6,906,529 | 06/14/2005 | Capacitive Sensor Device With Electrically Configurable Pixels |
| 6,882,573 | 04/19/2005 | DMOS Device with a Programmable Threshold Voltage |
| 6,861,337 | 03/01/2005 | Method for Using a Surface Geometry for a MOS-Gated Device in the Manufacture of Dice Having Different Sizes |
| 6,812,526 | 11/02/2004 | Trench DMOS Transistor Structure Having a Low Resistance Path to a Drain Contact Located on an Upper Surface |
| 6,812,056 | 11/02/2004 | Technique for Fabricating MEMS Devices Having Diaphragms of "Floating" Regions of Single Crystal Material |
| 6,794,251 | 09/21/2004 | Method of Making a Power Semiconductor Device |
| 6,790,745 | 09/14/2004 | Fabrication of Dielectrically Isolated Regions of Silicon in a Substrate |
| 6,777,745 | 08/17/2004 | Symmetric Trench MOSFET Device and Method of Making Same |
| 6,750,523 | 06/15/2004 | Photodiode Stacks for Photovoltaic Relays and the Method of Manufacturing the Same |
| 6,750,104 | 06/15/2004 | High Voltage Power MOSFET Having a Voltage Sustaining Region that Includes Doped Columns Formed by Trench Etching Using an Etchant Gas that is also a Doping Source |
| 6,734,495 | 05/11/2004 | Two Terminal Programmable MOS-Gated Current Source |
| 6,730,963 | 05/04/2004 | Minimum Sized Cellular MOS-Gated Device Geometry |
| 6,724,044 | 04/20/2004 | MOSFET Device Having Geometry that Permits Frequent Body Contact |
| 6,724,039 | 04/20/2004 | Semiconductor Device Having a Schottky Diode |
| 6,713,351 | 03/30/2004 | Double Diffused Field Effect Transistor Having Reduced On-Resistance |
| 6,710,414 | 03/23/2004 | Surface Geometry for a MOS-Gated Device that Allows the Manufacture of Dice Having Different Sizes |
| 6,710,400 | 03/23/2004 | Method for Fabricating a High Voltage Power MOSFET Having a Voltage Sustaining Region that Includes Doped Columns Formed by Rapid Diffusion |
| 6,689,662 | 02/10/2004 | Method of Forming a High Voltage Power MOSFET Having Low On-Resistance |
| 6,686,244 | 02/03/2004 | Power Semiconductor Device Having a Voltage Sustaining Region that Includes Doped Columns Formed with a Single Ion Implantation Step |
| 6,660,571 | 12/09/2003 | High Voltage Power MOSFET Having Low On-Resistance |
| 6,656,797 | 12/02/2003 | High Voltage Power MOSFET Having a Voltage Sustaining Region that Includes Doped Columns Formed by Trench Etching and Ion Implantation |
| 6,649,477 | 11/18/2003 | Method for Fabricating a Power Semiconductor Device Having a Voltage Sustaining Layer with a Terraced Trench Facilitating Formation of Floating Islands |
| 6,627,949 | 09/30/2003 | High Voltage Power MOSFET Having Low On-Resistance |
| 6,624,494 | 09/23/2003 | Method for Fabricating a Power Semiconductor Device Having a Floating Island Voltage Sustaining Layer |
| 6,621,107 | 09/16/2003 | Trench DMOS Transistor with Embedded Trench Schottky Rectifier |

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| 6,593,619 | 07/15/2003 | High Voltage Power MOSFET Having Low On-Resistance |
| 6,593,174 | 07/15/2003 | Field Effect Transistor Having Dielectrically Isolated Sources and Drains and Method for Making Same |
| 6,576,516 | 06/10/2003 | High Voltage Power MOSFET Having a Voltage Sustaining Region that Includes Doped Columns Formed by Trench Etching and Diffusion from Regions of Oppositely Doped Polysilicon |
| 6,566,201 | 05/20/2003 | Method for Fabricating a High Voltage Power MOSFET Having a Voltage Sustaining Region that Includes Doped Columns Formed by Rapid Diffusion |
| 6,538,279 | 03/25/2003 | High-Side Switch with Depletion-Mode Device |
| 6,492,663 | 12/10/2002 | Universal Source Geometry for MOS-Gated Power Devices |
| 6,479,352 | 11/12/2002 | Method of Fabricating High Voltage Power MOSFET Having Low On-Resistance |
| 6,472,709 | 10/29/2002 | Trench DMOS Transistor Structure Having a Low Resistance Path to a Drain Contact Located on an Upper Surface |
| 6,468,866 | 10/22/2002 | Single Feature Size MOS Technology Power Device |
| 6,465,304 | 10/15/2002 | Method for Fabricating a Power Semiconductor Device Having a Floating Island Voltage Sustaining Layer |
| 6,432,775 | 08/13/2002 | Trench DMOS Transistor Structure Having a Low Resistance Path to a Drain Contact Located on an Upper Surface |
| 6,420,764 | 07/16/2002 | Field Effect Transistor (sic. Transistor) Having Dielectrically Isolated Sources and Drains and Methods for Making Same |
| 6,403,427 | 06/11/2002 | Field Effect Transistor Having Dielectrically Isolated Sources and Drains and Method for Making Same |
| 6,399,961 | 06/04/2002 | Field Effect Transistor Having Dielectrically Isolated Sources and Drains and Method for Making Same |
| 6,369,426 | 04/09/2002 | Transistor with Integrated Photodetector for Conductivity Modulation |
| 6,368,918 | 04/09/2002 | Method of Fabricating Nan (sic. an) Embedded Flash EEPROM with a Tunnel Oxide Grown on a Textured Substrate |
| 6,331,794 | 12/18/2001 | Phase Leg with Depletion-Mode Device |
| 6,316,336 | 11/13/2001 | Method for Forming Buried Layers with Top-Side Contacts and the Resulting Structure |
| 6,291,845 | 09/18/2001 | Fully-Dielectric-Isolated FET Technology |
| 6,272,050 | 08/07/2001 | Method and Apparatus for Providing an Embedded Flash-EEPROM Technology |
| 6,239,752 | 05/29/2001 | Semiconductor Chip Package that is also an Antenna |
| 6,225,662 | 05/01/2001 | Semiconductor Structure with Heavily Doped Buried Breakdown Region |
| 6,215,170 | 04/10/2001 | Structure for Single Conductor Acting as Ground and Capacitor Plate Electrode Using Reduced Area |
| 6,198,114 | 03/06/2001 | Field Effect Transistor Having Dielectrically Isolated Sources and Drains and Method for Making Same |
| 6,069,385 | 05/30/2000 | Trench MOS-Gated Device |

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| 6,064,109 | 05/16/2000 | Ballast Resistance for Producing Varied Emitter Current Flow Along the Emitter's Injecting Edge |
| 6,046,473 | 04/04/2000 | Structure and Process for Reducing the On-Resistance of MOS-Gated Power Devices |
| 6,011,298 | 01/04/2000 | High Voltage Termination with Buried Field-Shaping Region |
| 5,985,721 | 11/16/1999 | Single Feature Size MOS Technology Power Device |
| 5,981,998 | 11/09/1999 | Single Feature Size MOS Technology Power Device |
| 5,981,318 | 11/09/1999 | Fully-Dielectric-Isolated FET Technology |
| 5,960,277 | 09/28/1999 | Method of Making a Merged Device with Aligned Trench FET and Buried Emitter Patterns |
| 5,897,355 | 05/27/1999 | Method of Manufacturing Insulated Gate Semiconductor Device to Improve Ruggedness |
| 5,869,371 | 02/09/1999 | Structure and Process for Reducing the On-Resistance of MOS-gated Power Devices |
| 5,856,696 | 01/05/1999 | Field Effect Transistor Having Dielectrically Isolated Sources and Drains |
| 5,821,136 | 10/13/1998 | Inverted Field-Effect Device with Polycrystalline Silicon/Germanium Channel |
| 5,801,396 | 09/01/1998 | Inverted Field-Effect Device with Polycrystalline Silicon/Germanium Channel |
| 5,798,549 | 08/25/1998 | Conductive Layer Overlaid Self-Aligned MOS-Gated Semiconductor Devices |
| 5,773,328 | 06/30/1998 | Method Of Making A Fully-Dielectric-Isolated FET |
| 5,756,386 | 05/26/1998 | Method of Making Trench MOS-Gated Device with A Minimum Number of Masks |
| 5,710,443 | 01/20/1998 | Merged Device with Aligned Trench FET and Buried Emitter Patterns |
| 5,708,289 | 01/13/1998 | Pad Protection Diode Structure |
| 5,701,023 | 12/23/1997 | Insulated Gate Semiconductor Device Typically Having Subsurface-Peaked Portion of Body Region for Improved Ruggedness |
| 5,691,555 | 11/25/1997 | Integrated Structure Current Sensing Resistor For Power Devices Particularly For Overload Self-Protected Power MOS Devices |
| 5,668,025 | 09/16/1997 | Method of Making a FET with Dielectrically Isolated Sources and Drains |
| 5,663,079 | 09/02/1997 | Method of Making Increased Density MOS-Gated Semiconductor Devices |
| 5,648,670 | 07/15/1997 | Trench MOS-Gated Device with a Minimum Number of Masks |
| 5,640,037 | 06/17/1997 | Cell with Self-Aligned Contacts |
| 5,637,889 | 06/10/1997 | Composite Power Transistor Structures Using Semiconductor Materials With Different Bandgaps |
| 5,591,655 | 01/07/1997 | Process for Manufacturing a Vertical Switched-Emitter Structure with Improved Lateral Isolation |
| 5,589,415 | 12/31/1996 | Method for Forming a Semiconductor Structure with Self-Aligned Contacts |

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| 5,576,245 | 11/19/1996 | Method of Making Vertical Current Flow Field Effect Transistor |
| 5,574,301 | 11/12/1996 | Vertical Switched-Emitter Structure with Improved Lateral Isolation |
| 5,528,063 | 06/18/1996 | Conductive-Overlaid Self-Aligned MOS-Gated Semiconductor Devices |
| 5,485,027 | 01/16/1996 | Isolated DMOS IC Technology |
| 5,298,781 | 03/29/1994 | Vertical Current Flow Field Effect Transistor with Thick Insulator Over Non-Channel Areas |
| 5,237,481 | 08/17/1993 | Temperature Sensing Device for Use in a Power Transistor |
| 5,218,228 | 06/08/1993 | High Voltage MOS Transistors with Reduced Parasitic Current Gain |
| 5,164,325 | 11/17/1992 | Method of Making a Vertical Current Flow Field Effect Transistor |
| 5,156,989 | 10/20/1992 | Complementary, (sic) Isolated DMOS IC Technology |
| 5,132,235 | 07/21/1992 | Method for Fabricating a High Voltage MOS Transistor |
| 5,034,785 | 07/23/1991 | Planar Vertical Channel DMOS Structure |
| 4,983,535 | 01/08/1991 | Vertical DMOS Transistor Fabrication Process |
| 4,978,631 | 12/18/1990 | Current Source with a Process Selectable Temperature Coefficient |
| 4,958,204 | 09/18/1990 | Junction Field-Effect Transistor with a Novel Gate |
| 4,956,700 | 09/11/1990 | Integrated Circuit with High Power, Vertical Output Transistor Capability |
| 4,952,992 | 08/28/1990 | Method and Apparatus for Improving the On-Voltage Characteristics of a Semiconductor Device |
| 4,929,991 | 05/29/1990 | Rugged Lateral DMOS Transistor Structure |
| 4,920,388 | 04/24/1990 | Power Transistor with Integrated Gate Resistor |
| 4,916,509 | 04/10/1990 | Method for Obtaining Low Interconnect Resistance on a Grooved Surface and the Resulting Structure |
| 4,914,058 | 04/03/1990 | Grooved DMOS Process with Varying Gate Dielectric Thickness |
| 4,896,196 | 01/23/1990 | Vertical DMOS Power Transistor with an Integral Operating Condition Sensor |
| 4,893,160 | 01/09/1990 | Method for Increasing the Performance of Trenched Devices and the Resulting Structure |
| 4,868,537 | 09/19/1989 | Doped SiO ₂ Resistor and Method of Forming Same |
| 4,851,366 | 07/25/1989 | Method for Providing Dielectrically Isolated Circuit |
| 4,845,051 | 07/04/1989 | Buried Gate JFET |
| 4,835,586 | 05/30/1989 | Dual-Gate High Density FET |
| 4,827,324 | 05/02/1989 | Implantation of Ions into an Insulating Layer to Increase Planar PN Junction Breakdown Voltage |
| 4,824,795 | 04/25/1989 | Method for Obtaining Regions of Dielectrically Isolated Single Crystal Silicon |
| 4,816,882 | 03/28/1989 | Power MOS Transistor with Equipotential Ring |
| 4,799,100 | 01/17/1989 | Method and Apparatus for Increasing Breakdown of a Planar Junction |
| 4,798,810 | 01/17/1989 | Method for Manufacturing a Power MOS Transistor |
| 4,794,436 | 12/27/1988 | High Voltage Drifted-Drain MOS Transistor |
| 4,791,462 | 12/13/1988 | Dense Vertical J-MOS Transistor |
| 4,774,196 | 09/27/1988 | Method of Bonding Semiconductor Wafers |

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| | | |
|-----------|------------|---|
| 4,767,722 | 08/30/1988 | Method for Making Planar Vertical Channel DMOS Structures |
| 4,759,836 | 07/26/1988 | Ion Implantation of Thin Film CrSi ₂ and SiC Resistors |
| 4,707,909 | 11/24/1987 | Manufacture of Trimmable High Value Polycrystalline Silicon Resistors |
| 4,682,405 | 07/28/1987 | Methods for Forming Lateral and Vertical DMOS Transistors |
| 4,402,003 | 08/30/1983 | Composite MOS/Bipolar Power Device |
| 4,398,339 | 08/16/1983 | Fabrication Method for High Power MOS Device |
| 4,393,391 | 07/12/1983 | Power MOS Transistor With a Plurality of Longitudinal Grooves to Increase Channel Conducting Area |
| 4,345,265 | 08/17/1982 | MOS Power Transistor with Improved High-Voltage Capability |
| 4,344,081 | 08/10/1982 | Combined DMOS and a Vertical Bipolar Transistor Device and Fabrication Method Therefor (sic) |
| 4,145,703 | 03/20/1979 | High Power MOS Device and Fabrication Method Therefor (sic) |

Education

| <u>Year</u> | <u>University</u> | <u>Degree</u> |
|-------------|---------------------|-------------------------------|
| 1982 | Stanford University | Ph.D., Electrical Engineering |
| 1970 | M.I.T. | MSEE |
| 1968 | M.I.T. | BSEE |

Publications – Books

Blanchard, R. A., Burgess, David, “Wafer Failure Analysis for Yield Enhancement,” *Accelerated Analysis*, 2000.

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Professional Associations and Achievements

- Senior Member, Institute of Electrical and Electronics Engineers
- Member, Electronic Device Failure Analysis Society
- Member, International Microelectronics & Packaging Society
- Member, American Vacuum Society
- Member, National Fire Protection Association
- Court Appointed Special Master

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