

## Silicon Wafer Direct Bonding through the Amorphous Layer

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We found that excess water molecules and hydrocarbons, existing in the bonding interface and thought to cause voids, were absorbed in the damaged area of the amorphous layer formed on the surface of the wafer upon direct bonding of silicon wafers, thus making it possible to suppress void formation with relatively low heat-treatment temperature of 600°C for 3 h.

**KEYWORDS:** silicon wafer direct bonding, ion implantation, amorphous layer, void, water molecule

### 1. Introduction

Over the last few years, silicon wafer direct bonding techniques have been drawing attention as a method of fabricating power devices and silicon on insulator (SOI) devices. With regard to power devices, silicon wafer direct bonding techniques have several advantages: they enable formation of a thick and high-resistance layer on a low-resistance substrate thereby making it suitable for fabrication of power transistors with high breakdown voltage,<sup>1)</sup> isolated vertical-DMOS and control circuits on a single chip.<sup>2–4)</sup> However, there are many problems yet to be solved. Among them, heat-treatment temperature during bonding is high. In general, 1000°C or higher heat-treatment temperature is reported to be required to produce strong and void-free bonding.<sup>5–7)</sup> The diffusion of impurities from the low-resistance substrate to the high-resistance layer may occur during heat treatment. This diffusion of impurities restricts the device structure design, as well as increasing the ON-resistance of power devices.

As far as reduction of heat-treatment temperature during bonding is concerned, it has been reported that forming a 1  $\mu\text{m}$  thermal oxide film on the silicon wafer eliminates the development of voids even during heat treatment at approximately 200°C.<sup>8,9)</sup> This may be attributed to the fact that excess water molecules present on the bonding interface are absorbed into the thermal oxide film. However, for the devices considered in this paper, the above method cannot be applied because the thick oxide film obstructs current flowing across the bonded interface. Therefore, we proposed another method in which an amorphous layer, rather than a thick oxide film, is formed. Then the excess water molecules are absorbed into the amorphous layer during heat treatment.

### 2. Experimental

The bonding procedure of this experiment is shown in Fig. 1. Six-inch-diameter,  $\langle 100 \rangle$ -oriented, boron-doped, CZ-grown silicon wafers were used. The resistivity of the wafers was 3–5  $\Omega \cdot \text{cm}$ ; the concentration of oxygen was  $1.0 \times 10^{18}$  atoms/cm<sup>3</sup>. These wafers are commercially available. Silicon ions were implanted to make the silicon wafer surface amorphous. In the experiment, the thickness of the amorphous layer was varied by adjusting the acceleration energy between 60 to

180 keV at  $5 \times 10^{15}$  dose/cm<sup>3</sup>. Mitani *et al.*<sup>10)</sup> have already reported that hydrocarbons adhering to the wafer surface are a cause of voids. With this in mind, we conducted the cleaning process shown in Fig. 1 to remove contamination and hydrocarbons on the wafer surface. The cleaning methods each consist of the steps: SC-1 cleaning (a mixture of  $\text{NH}_4\text{OH}$ ,  $\text{H}_2\text{O}_2$  and  $\text{H}_2\text{O}$ ), etching by HF solution, SC-2 cleaning (a mixture of  $\text{HCl}$ ,  $\text{H}_2\text{O}_2$  and  $\text{H}_2\text{O}$ ), and etching by HF solution. Subsequently, to form the native oxide film on wafer surfaces, wafers were dipped into a mixture of  $\text{H}_2\text{SO}_4$  and  $\text{H}_2\text{O}_2$  ( $\text{H}_2\text{SO}_4\text{:H}_2\text{O}_2=4\text{:}1$ ) at  $85 \pm 5^\circ\text{C}$  for 3 min. Furthermore, these wafers were rinsed in deionized water for 30 min and spin-dried at 1800 rpm for 3 min in dry  $\text{N}_2$ . As a result of the above-mentioned processes, the wafers became covered in a native oxide film with 0.63 nm thickness, which was measured using X-ray photoelectron spectroscopy (XPS). Then these wafers were bonded to each other under atmospheric pressure at room temperature immediately after the above treatment. The angle of rotational mismatch when these

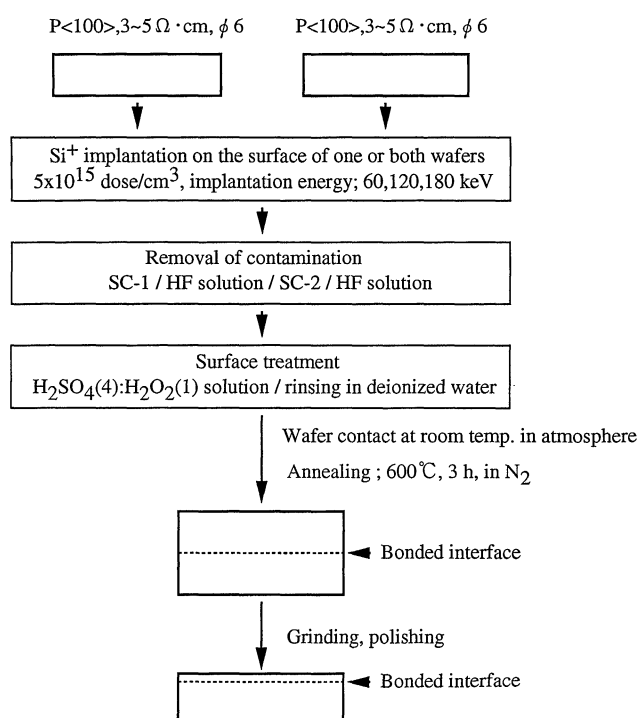


Fig. 1. Bonding procedure of this experiment.

wafers were bonded was minimized to be less than 0.5 degree. The bonded wafer was annealed at 600°C for 3 h in N<sub>2</sub>.

In order to evaluate the thickness of the amorphous layer after silicon ion implantation, the spreading resistance method was used with beveled surfaces. The bonded interface structure of the bonded wafer, in terms of voids and formation of amorphous SiO<sub>x</sub> layer,<sup>11)</sup> was evaluated by Makyou<sup>12)</sup> and TEM, respectively. When the voids were observed at the bonded interface by Makyou, one side of the bonded wafer was ground and mirror-polished, and the thickness from the mirror-polished surface to the bonded interface was 2–3 μm.

### 3. Results and Discussion

The spreading resistance near the wafer surface after silicon ion implantation at 60, 120, and 180 keV acceleration energy is shown in Fig. 2. The thickness of

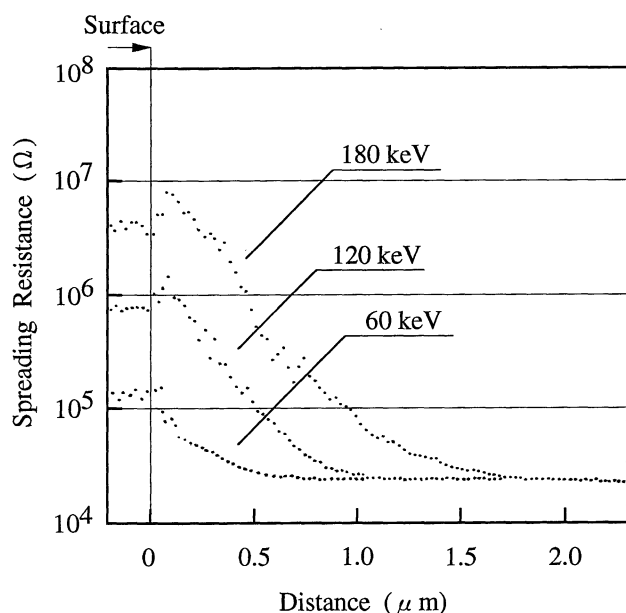


Fig. 2. Spreading resistance near the wafer surface after silicon ion implantation.

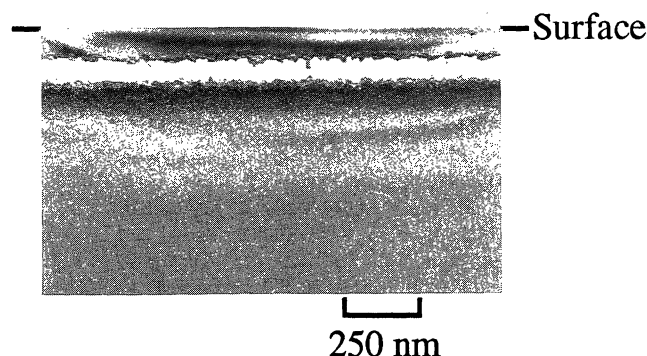


Fig. 3. Cross-sectional TEM image after silicon ion implantation (acceleration energy; 120 keV).

the amorphous layer was defined as the depth at which the spreading resistance equaled the constant resistance in the deep section of the wafer, then the thicknesses of the amorphous layers produced at 60, 120, and 180 keV acceleration energy became 0.6, 1.0, and 1.7 μm, respectively. The cross-sectional TEM image of wafer surface after implantation at 120 keV acceleration energy is shown in Fig. 3. The 75-nm-wide amorphous region was observed at about 139 nm depth, which is the projected range of silicon ion implantation. A high-resolution TEM image showed that the damaged region had many crystal defects in the upper and lower parts of the amorphous region. These results suggest that many crystal defects are distributed in the amorphous layer defined by the spreading resistance, and that the thickness of the amorphous layer depends on the acceleration energy.

Figure 4 shows the Makyou topographs obtained after bonding between wafers with no amorphous layer, wafers with amorphous layer, and wafer with no amorphous layer and wafer with amorphous layer. Despite eliminating hydrocarbons, thought to cause voids, through the previously mentioned cleaning process, we found that many voids were observed at the bonded interface between the wafers without any amorphous layer. It was found that in the bonded interface between the wafer with no amorphous layer and wafer with amorphous layer, the void formation was suppressed for amorphous layers produced at 180 keV acceleration energy while suppression was not so effective for amorphous layers produced at 60 and 120 keV acceleration energy. In the case of bonding between wafers involving an amorphous layer, the void formation was significantly suppressed for amorphous layers produced at more than 120 keV acceleration energy. These results show that the amorphous layer suppresses the void formation in silicon wafer direct bonding at low temperature.

Figure 5 shows the cross-sectional TEM lattice image near the bonded interface between wafers with an amorphous layer produced at 120 keV acceleration energy. A SiO<sub>x</sub> 2–3 nm thick layer was observed at the bonded interface. As mentioned above, the wafer surface had a native oxide film 0.63 nm thick just before the bonding. It is thought that the 2–3-nm-thick SiO<sub>x</sub> layer was formed by absorbing the excess water molecules. It is assumed that the damaged area on the upper amorphous layer played an important role in absorbing the excess water molecules and hydrocarbons existing on the bonded interface. As a result, void formation was suppressed by annealing at a relatively low temperature of 600°C.

The amorphous layer formed by silicon ion implantation recrystallized when heated (600°C, 3 h) during the bonding process, and the presence of crystal defects was confirmed by TEM observation. It is expected that crystal defects can be eliminated by heat treatment at high temperatures (around 1000°C) when fabricating devices using the bonded wafers.

The devices considered in this paper are left with a 2–3-nm-thick SiO<sub>x</sub> layer in the bonded interface, which

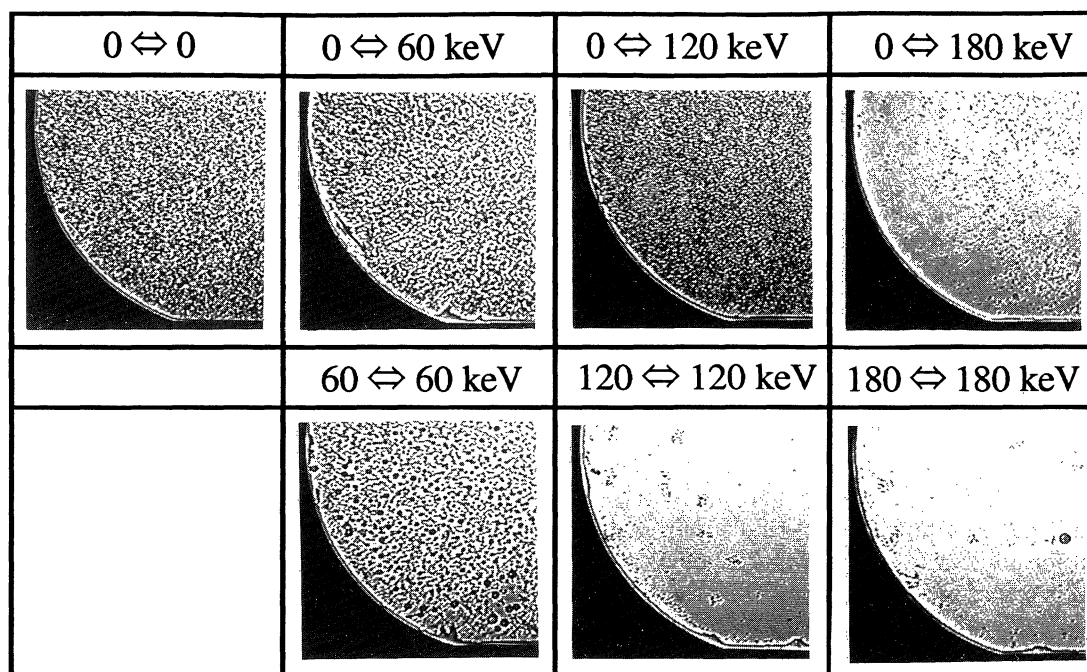


Fig. 4. Makyo topographs of bonded wafers (acceleration energy; 60, 120, 180 keV, 0 means without silicon ion implantation).

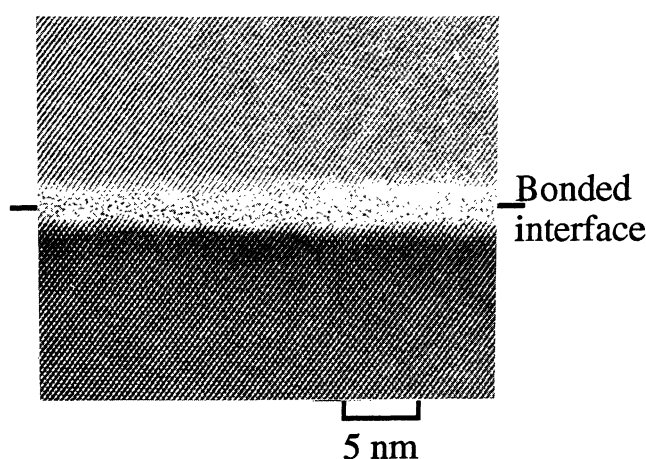


Fig. 5. Cross-sectional TEM lattice image near the bonded interface (acceleration energy; 120 $\leftrightarrow$ 120 keV).

is expected to degrade electrical performance. However, as reported by Himi *et al.*<sup>13)</sup> and Ishigami *et al.*,<sup>11)</sup> this SiO<sub>x</sub> layer can be minimized by eliminating or maximally thinning the native oxide formed on the wafer surface before bonding. The electrical resistance in the bonded interface can possibly be reduced by diffusing the wafer impurities through the bonded interface, during high-temperature heat treatment (around 1000°C) to fabricate the devices.

#### 4. Conclusions

In this paper, we showed that if an amorphous layer was formed on the wafer surface before a silicon wafer was bonded directly, then during the annealing process excess water molecules and hydrocarbons were ab-

sorbed from the bonding interface into the damaged region on the amorphous layer, and void formation was suppressed by annealing at a relatively low temperature of 600°C.

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