UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.
And
TSMC NORTH AMERICA CORPORATION
Petitioner

v.

ZIPTRONIX
Patent Owner

Case IPR2014-00114
Patent 6,563,133

Filing Date of This Paper: November 27, 2013

Before Administrative Patent Judge Kevin F. Turner
(Cathy Underwood, Trial Paralegal)

CORRECTED

PETITION FOR *INTER PARTES* REVIEW

OF U.S. PATENT NO. 6,563,133 B1

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TABLE OF EXHIBITS

Initiation of an *inter partes* review under 35 U.S.C. § 311, and 37 C.F.R. Part 42, Subpart B is hereby requested for Claims 1-14 and 53-60 of U.S. Patent No. 6,563,133 B1 to Tong ("'133 Patent") and a final determination that Claims 1-14 and 53-60 are unpatentable on one or more of the bases identified herein is requested. A copy of the '133 Patent is attached as TSMC1001.

I. MANDATORY NOTICES

A. Real Parties-in-Interest and Related Matters

This Petition is brought by Taiwan Semiconductor Manufacturing Company, Limited and TSMC North America Corporation (collectively "Petitioner").

Petitioner is not aware of any judicial or administrative matter that would affect, or be affected by, a decision in this proceeding.

B. Lead and Backup Counsel and Notice Information

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II. GROUNDS FOR STANDING

Petitioner certifies that the '133 Patent is eligible for *inter partes* review. Petitioner further certifies that Petitioner and their privies are not barred or estopped from requesting *inter partes* review of the '133 Patent challenging Claims 1-14 and 53-60 on the grounds identified in this Petition.

III. PRIOR ART RELIED UPON

Petitioner requests institution of an *inter partes* review, and a determination of unpatentability, of Claims 1-14 and 53-60 over the prior art and bases below.

- TSMC1005: U.S. Patent No. 6,534,381 to Cheung et al. ("Cheung").
- TSMC1006: U.S. Patent No. 5,561,072 to Saito ("Saito").
- TSMC1007: S. Fujino et al., *Silicon Wafer Direct Bonding through the Amorphous Layer*, 34 Japanese J. Appl. Phys. 1322 (15 October 1995) ("Fujino").
- TSMC1008: S. Tian et al., *A Detailed Physical Model for Ion Implant Induced Damage in Silicon*, 45 (6) IEEE Transactions on Electron Devices 1226 (June 1998) ("Tian").

Saito, Tian, and Fujino are prior art under 35 U.S.C. § 102(b), and Cheung is prior art under 35 U.S.C. § 102(e). None of Cheung, Saito, and Tian were previously before the Office during prosecution of the '133 Patent. The full disclosure of Fujino was not substantively addressed during prosecution of the '133 Patent.

IV. CLAIM CONSTRUCTION (37 C.F.R. § 42.104(A)(3))

Pursuant to 37 C.F.R. § 42.100(b), the terms in the claims are to be given their broadest reasonable construction in light of the specification. Such claim constructions may differ under the legal standards mandated to be used by courts in litigation. *See* M.P.E.P. § 2686.04(IV). Hence, Petitioner submits that these claim constructions are not binding upon Petitioner in any litigation or other proceeding.

A. Overview of the '133 Patent

The '133 Patent relates to bonding of wafer pairs. *See* TSMC1001 at 1:8-9. A first wafer 200 is cleaned. *See id.* at 5:57-6:3. The wafer 200 is immersed in an aqueous HF solution to remove a native oxide layer, and subsequently exposed to a plasma or to ion implantation 201, preferably a boron-containing plasma or ion, argon plasma, or arsenic ion. *See id.* at 6:4-11, 34-36, 43-46; 8:22-26, 30-35, 55-58; 9:40-46; Figs. 1 (steps 101 and 102), 2A. The plasma or ion implantation 201 modifies the surface 202 and/or subsurface of the first wafer 200 to create defect areas and possibly a thin amorphous layer, as indicated by the thin layer at the surface 202, and when boron is used, may introduce boron into the substrate surface. *See id.* at 6:7-16, 36-39. The amorphous layer is "about a few nm or more in thickness." *Id.* at 6:42-43. The wafer is immersed in an aqueous HF solution to remove a native or other oxide layer. *See id.* at 6:17-20, 48-49; Fig. 1 (step 103).

A second wafer 203 undergoes similar processing to have a plasma treated surface 204. *See id.* at 6:49-50. The plasma treated surfaces 202, 204 are directly

contacted to form a bonded structure at room temperature. *See id.* at 6:21-23, 49-52; Fig. 1 (step 104). The structure is annealed at low temperature. *See id.* at 6:25-26, 52-56; Fig. 1 (step 105). The temperature to anneal may be selected to recrystallize the amorphous layers, or a separate annealing procedure may be used to recrystallize the amorphous layers. *See id.* at 6:27-32.

B. Summary of Relevant Prosecution History

The '133 Patent was filed on August 9, 2000 with 58 claims. *See* TSMC1002 at 53-59. As relevant herein, claims 44, 92, and 103 during prosecution correspond to claims 1, 53, and 10, respectively, upon issuance. Unless indicated otherwise, claim numbers discussed in this subsection refer to the numbers during prosecution. The prosecution history is attached as TSMC1002.

A first Office Action rejected claim 44 as anticipated by U.S. Pat. No. 5,783,477 ("Kish") and claim 44 as anticipated by U.S. Pat. No. 6,120,917 ("Eda"). *See id.* at 94-103. Applicant amended claim 44 and added claim 103. *See id.* at 104-123. (Claims added in the amendment in response to the first Office Action after claim 100 were misnumbered by 1. *See* TSMC1002 at 126. Hence, claim 103 as referenced throughout prosecution was originally labeled as 104.) Claim 44 was amended: "a first [amorphous] nearly-amorphized layer formed in said first surface" as well as a corresponding amendment for the second layer. *See id.* at 122. Claim 103 was added to recite "said first and second amorphous layers

are each in the range of a few nm of thickness." *See id.* at 115. The applicant argued in regards to Kish, "There is no suggestion of any nearly-amorphized layers formed in a substrate. Kish simply [had] amorphous regions in a layer formed on the substrate." *Id.* at 117. Similarly, the applicant argued, "There is no suggestion of any nearly amorphized layer in the surface of a substrate" in Eda. *Id.* at 118.

A second Office Action rejected claim 103 as being indefinite; claims 44 and 92 as anticipated by Takagi et al. ("Takagi"); and claims 44 and 92 as obvious over Kish in view of U.S. Pat. No. 4,963,505 ("Fujii"). *See id.* at 124-32. In response the applicant amended claim 44 as follows: "a first nearly-amorphized layer containing one of boron and arsenic formed [in] uniformly over said surface." *See id.* at 141. Claim 92 was amended: "one first material amorphized substantially only in a first surface of said first material and containing one of boron and arsenic." *See id.* at 142.

In regards to the indefiniteness rejection, the applicant argued, "A 'few' is an easily understood value. One skilled in the art would not be confused by what constitutes, for example, a few nm." *Id.* at 137. The applicant then stated:

> Specifically, [Kish] discloses layer 95 formed on the semiconductor layer and amorphous or polycrystalline regions 91 formed in a layer 95. Regions 91 are formed by selective patterning (see column 8, lines 18-32) and are useful to direct current flow through the bonded structure (see FIG. 9). . . . [O]ne skilled in the art would clearly not

> form regions 91 uniformly over the surface or over a substantial portion of the surface since the resulting large or complete non-ohmic contact would defeat the whole purpose of trying to form an ohmic contact.
>
> There was some questions raised by Examiners Diaz and Lee over the terms like "substantial" and "uniform" regarding support in the specification and definiteness. The description clearly shows the treatment to produce the amorphized or nearly-amorphized surfaces, such as the non-limiting example of FIG. 2 where surface 202 extends over a substantial portion of the substrate. The support is clear. A term like "substantial" is very often used in this art recognizing that "substantially" is accurate as there may be some incompleteness or nonuniformity due to the realities of physical materials, or the presence of some structure or material on the surface preventing completeness or absoluteness. Terms like "substantial" as used in the claims are definite and convey the subject matter of the invention sought to be protected to one skilled in the art.

Id. at 137-138. The applicant again argued that Kish has "specific regions containing amorphous or polycrystalline material" rather than suggesting a nearly-amorphized layer. *See id*. at 138.

A third Office Action rejected claims 44 and 92 as obvious over Takagi in view of Fujii; and claims 44 and 92 as obvious over Takagi in view of U.S. Pat. No. 6,153,455 ("Yamazaki"). *See id.*, pp. 150-158. In response, applicant stated Fujii "describes an amorphous silicon layer 16 which may be formed by

implanting ions such as silicon, arsenic, phosphorous" but argued that Fujii does not suggest "an amorphous layer in a bonded structure" since the "amorphous layer is intentionally thermally treated to form single-crystal and poly-crystal layers, and is not present in a bonded structure." *Id.* at 163-164. Applicant concluded:

> [T]here is no suggestion that the implantation to form the amorphous layer would be used for a surface cleaning operation and substitution for the Ar sputter etch of Takagi et al, nor is there any suggestion of an amorphous region or layer in a bonded device. The amorphous layer is specifically converted out of the amorphous state into a poly-crystalline or single-crystalline state prior to any bonding. To the contrary, Fujii et al teaches away from using amorphous layers in a bonded structure.

Id. at 164.

C. "Nearly-amorphized layer"

The term ***nearly-amorphized layer*** is completely absent from the specification of the '133 Patent. The ***nearly-amorphized layer*** term was first introduced in a first amendment during prosecution. *See* TSMC1002 at 122. The applicant argued that the prior art did not teach an amorphous layer in arguing patentability of claim 1 (claim 44 during prosecution) and pointed out the import of some incompleteness or nonuniformity due to the realities of physical materials or the presence of some structure of material on the surface preventing completeness or absoluteness. *See id.* at 163-165. Figure 2 in the '133 Patent, which was cited as

support for a nearly-amorphized layer, *see id.* at 164, teaches a surface 202 that is an amorphous layer, *see* TSMC1001 at 6:40-42. A plain meaning of "nearly" is "with close approximation." TSMC1009 at 884. Hence, consistent with the broadest reasonable construction, arguments in the prosecution history, and support in the specification, Petitioner construes ***nearly-amorphized layer*** as a layer that at least closely approximates an amorphous layer, which construction allows for incompleteness of the amorphizing due to realities of physical materials.

D. A few nm in thickness

The '133 Patent states, "The amorphous layer formed is about a few nm or more in thickness," TSMC1001 at 6:42-43, and teaches in an embodiment forming "an amorphous layer with 1650 Å thick," *see id.* at 9:48-50. Under the broadest reasonable construction consistent with the Specification, Petitioner asserts that ***a few nm in thickness*** at least encompasses 165nm (1650 Å).

V. UNPATENTABILITY OF CLAIMS 1-14 AND 53-60 AND SUPPORTING EVIDENCE

Petitioner asserts that there is a reasonable likelihood that Claims 1-14 and 53-60 are unpatentable as discussed in this section, which is supported by a declaration of Dr. Richard A. Blanchard, attached hereto as TSMC1003.

Ground 1: Claims 1-10, 12-14, and 53-59 are anticipated under 35 U.S.C. § 102(e) by Chueng or rendered obvious under 35 U.S.C. § 103(a) over Cheung.

A. Claim 1 ***A bonded structure, comprising:***

Cheung discloses a "bonded structure." *See* TSMC1005 at 2:18-20.

a first substrate having a first surface, a first nearly-amorphized layer containing one of boron and arsenic formed uniformly over said first surface; and

Cheung discloses an amorphous silicon layer 15 formed uniformly throughout an upper surface 19 of a substrate 10. *See id.* at 3:49-50 ("Implant surface of first substrate to create a compliant layer (e.g., amorphous silicon layer)"); 5:52-6:14 ("The implantation process forms an 'amorphous' layer 15 of silicon overlying single crystal silicon material. . . . The amorphous silicon layer has a substantially planar upper surface 19, which also has amorphous characteristics."); 8:16-18; Figs. 3, 4. Cheung describes forming the amorphous silicon layer 15 using an implant of a "silicon bearing particle" or other types of particles. *See id.* at 5:65-66; 6:50-52. Since Cheung discloses an amorphous silicon layer 15, Cheung discloses a layer that at least closely approximates an amorphous layer, *i.e.*, a nearly-amorphized layer. *See* TSMC1003 at ¶ 30.

Cheung discloses that the substrate 10 is doped with impurities including boron or arsenic. *See* TSMC1005 at 4:15-20. Thus, Cheung's amorphous silicon layer 15 contains one of boron and arsenic. *See* TSMC1003 at ¶ 31.

a second substrate having a second surface, a second nearly-amorphized layer containing one of boron and arsenic formed uniformly over said second

surface;

Cheung discloses forming an amorphous layer of silicon formed uniformly throughout a surface of a substrate 20. *See* TSMC1005 at 8:21-23, 32-65. Cheung describes forming an amorphous layer using implants of "a silicon bearing particle" or other types of particles including "germanium or hydrogen." *See id.* at 8:56-57; 5:65-66; 6:50-52. Since Cheung discloses an amorphous layer of silicon, Cheung discloses a layer that at least closely approximates an amorphous layer, *i.e.*, a nearly-amorphized layer. *See* TSMC1003 at ¶ 30.

Cheung discloses that the substrate 20 is doped with impurities including boron or arsenic. *See* TSMC1005 at 5:4-7. Thus, Cheung's amorphous layer of silicon contains one of boron and arsenic. *See* TSMC1003 at ¶ 31.

said first surface being bonded to said second surface to form a bonded pair of substrates.

Cheung discloses bonding the surface of amorphous silicon layer 15 of substrate 10 with the surface of amorphous layer of silicon of substrate 20. *See* TSMC1005 at 8:26-29, Col. 8:32-41 ("[T]he present invention provides a method for bonding substrates together using first and second compliant layers of amorphous silicon, for example, on the first substrate and second substrate, respectively."); Fig. 8; *see also* TSMC1003 at ¶ 30.

B. Claims 2-10 and 12-14: Claims 2-10 and 12-14 are dependent on Claim

1, which as set forth in GROUND 1(A) Cheung teaches the limitations of Claim 1.

Claim 2 recites: "one of said first and second substrates of said bonded pair having a third surface, said third surface having a nearly-amorphized layer; a third substrate having a fourth surface, a fourth nearly-amorphized layer formed in said fourth surface; and said third surface bonded to said fourth surface."

Cheung describes bonding the substrates 10 and 20, as discussed above. *See* TSMC1005 at 8:10-41. Cheung teaches that the invention can be applied "for multi-layered integrated circuit devices, three-dimensional packaging of integrated semiconductor devices," and more. *See id.* at 1:17-21.

Accordingly, it would have been obvious to a person of ordinary skill in the art at the time of the invention ("a POSITA") to form one of the first and second substrates having a third surface having a nearly-amorphized layer, to form a nearly-amorphized layer in a fourth surface of a third substrate, and to bond the third surface to the fourth surface as recited in Claim 2 to form integrated circuit devices or a three-dimensional package as described in Cheung. S*ee also* TSMC1003 at ¶ 32.

Moreover, "the mere duplication of parts has no patentable significance unless a new and unexpected result is produced." *See In re Harza*, 274 F.2d 669, 671 (C.C.P.A. 1960). (References to authorities are cited in first appearances of an issue and are not further referenced for similar issues, although such references

should be inferred.) Claim 2 requires nothing more than the duplication of the parts recited in Claim 1, which does not produce any new and/or unexpected results for bonding nearly-amorphized layers of additional substrates.

Claim 3 recites "wherein said first and second substrates are selected from Si, InGaAs, InP, GaAs, Ge and SiC." Cheung discloses that the substrates are "silicon," "compound semiconductors and the like," or "gallium arsenide [(GaAs)], gallium nitride (GaN), and others." *See* TSMC1005 at 4:10-15, 25-27; 9:52-53.

Claim 4 recites "wherein: said first and second substrates each comprises a silicon substrate; and said first and second surfaces each comprises a silicon surface." Cheung discloses that each of the substrates 10 and 20 are silicon. *See id.* at 4:10-15; 4:66-5:3. Cheung further discloses that each of the surfaces of the amorphous silicon layer 15 of substrate 10 and amorphous layer of silicon of substrate 20 is a silicon surface. *See id.* at 8:32-41, 62-65; 5:52-6:14.

Claim 5 recites "wherein: said first and second substrates comprise respective first and second semiconductor devices." Cheung discloses that the invention can be applied to "multi-layered integrated circuit devices, three-dimensional packaging of integrated semiconductor devices, photonic devices, piezoelectronic devices, microelectromechanical systems ('MEMS'), sensors, actuators, solar cells, flat panel displays (e.g., LCD, AMLCD), biological and biomedical devices, and the like." *See id.* at 1:17-24.

Claim 6 recites "wherein: said first surface comprises a first silicon surface exposed to a boron-containing plasma; and said second surface comprises a second silicon surface exposed to a boron-containing plasma." The limitation "*exposed* to a boron-containing plasma" (emphasis added) is a product-by-process limitation, which only requires Petitioner to show a same structure.

To the extent that exposure to a boron-containing plasma requires the surfaces to resultantly contain boron, to which Petitioner does not concede, Cheung discloses that the surface 19 of the amorphous silicon layer 15 of substrate 10 and that the surface of the amorphous layer of silicon of substrate 20 each comprise a silicon surface and boron. *See* TSMC1005 at 4:12-20; 5:3-7; 6:9-14; 8:62-65; *see also* TSMC1003 at ¶ 31. Hence, Cheung discloses a same structure.

Claim 7 recites that each of the first surface and the second surface comprises a "silicon surface implanted with boron." The limitation "*implanted* with boron" (emphasis added) is a product-by-process limitation, which only requires Petitioner to show a same structure. Cheung discloses that the surface 19 of the amorphous silicon layer 15 of substrate 10 and the surface of the amorphous layer of silicon of substrate 20 each comprise a silicon surface and boron. *See* TSMC1005 at 4:12-20; 5:3-7; 6:9-14; 8:62-65; *see also* TSMC1003 at ¶ 31. Hence, Cheung discloses a same structure.

Claim 8 recites that each of the first second surfaces comprises a "silicon

surface implanted with arsenic." The limitation "*implanted* with arsenic" (emphasis added) is a product-by-process limitation, which only requires Petitioner to show a same structure. Cheung discloses that the surface 19 of the amorphous silicon layer 15 of substrate 10 and the surface of the amorphous layer of silicon of substrate 20 each comprise a silicon surface and arsenic. *See* TSMC1005 at 4:12-20; 5:3-7; 6:9-14; 8:62-65; *see also* TSMC1003 at ¶ 31. Hence, Cheung discloses a same structure.

Claim 9 recites "at least one of boron-boron and Si covalent bonds formed between said first and second substrates." Cheung discloses a method for fabricating an "epi-like" substrate by bonding together a pair of substrates having amorphous surfaces. *See* TSMC1005 at 2:25-47. Cheung discloses steps to "strip" the surfaces of the substrates to the silicon surface. *See id.* at 8:20, 26. The subsequent joining and annealing steps, *see id.* at 8:27-29, form a bond between silicon atoms in the silicon surface, *see id.* at 9:57 ("silicon-on-silicon" bond), which is a covalent bond since silicon-to-silicon bonding occurs by covalent bonding. *See* TSMC1003 at ¶ 33. Further, as understood by a POSITA, an "epi-like" substrate denotes the formation of silicon covalent bonds across the bond interface for a pair of bonded substrates. *See id.*

Claim 10 recites "wherein: said first and second amorphous layers are each in the range of a few nm in thickness." Cheung discloses forming an amorphous

silicon layer with a "thickness ranging from about 10 nm to about 500 nm." *See* TSMC1005 at 6:10-13. Hence, Cheung discloses a thickness in the range of 165 nm, *i.e.*, a range of a few nm in thickness.

Assuming for the sake of argument that Cheung's disclosure does not anticipate the claim, Cheung's range overlaps the range of a few nm in thickness, and therefore, renders Claim 10 *prima facie* obvious. *See, e.g.*, *In re Wertheim*, 541 F.2d 257 (C.C.P.A. 1976); *In re Woodruff*, 919 F.2d 1575 (Fed. Cir. 1990).

Even assuming further for the sake of argument that Cheung's disclosure does not overlap, "it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller*, 220 F.2d 454, 456 (C.C.P.A. 1955). The range of thickness of a few nm could be determined by a POSITA by routine experimentation. *See* TSMC1003 at ¶ 34.

Claim 12 recites that each of the first and second surfaces comprise "an amorphous boron-containing layer." Cheung discloses that surfaces of the first and second substrate 10, 20 are implanted to create compliant layers (e.g., amorphous silicon layers). *See* TSMC1005 at 5:52-6:14; 8:15−23. Cheung discloses that the substrates 10, 20 are doped with impurities including boron. *See id.* at 4:15-20. Thus, Cheung's amorphous silicon layer 15 contains boron. *See* TSMC1003 at ¶ 31.

Claim 13 recites that each of the first surface and the second surface

"comprises a surface exposed to a boron-containing plasma." The limitation "*exposed* to a boron-containing plasma" (emphasis added) is a product-by-process limitation, which only requires Petitioner to show a same structure.

To the extent that exposure to a boron-containing plasma requires the surfaces to resultantly contain boron, to which Petitioner does not concede, Cheung discloses that the substrate 10 and the substrate 20 each are doped with impurities including boron. *See* TSMC1005 at 4:15-20; 5:4-7. Thus, Cheung's surface 19 of the amorphous silicon layer 15 and surface of the amorphous layer of silicon each contain boron. *See* TSMC1003 at ¶ 31. Hence, Cheung teaches a same structure.

Claim 14 recites that each of the first surface and the second surface comprises a "surface exposed to an inert gas plasma." The limitation "*exposed* to an inert gas plasma" (emphasis added) is a product-by-process limitation, which only requires Petitioner to show a same structure.

To the extent that exposure to an inert gas plasma requires a resultant change to the surfaces, to which Petitioner does not concede, Cheung discloses cleaning the surfaces of the substrates 10 and 20 using "a plasma cleaning process" using "non-reactive gases such as argon." *See* TSMC1005 at 4:33, 43-44; 5:21, 29. Argon is an inert gas. *See* TSMC1003 at ¶ 35. Thus, Cheung discloses exposing the respective surface of the first and second substrates to an inert gas plasma.

C. Claim 53: ***A bonded structure, comprising:***

Cheung discloses a "bonded structure." *See* TSMC1005 at 2:18-20.

a first substrate of substantially one first material amorphized substantially only in a first surface of said first material and containing one of boron and arsenic; and

Cheung discloses a substrate 10 of substantially one material, e.g., silicon. *See id.* at 4:12-14. The one material, *e.g.*, silicon, is amorphized, *e.g.*, amorphous silicon layer 15, substantially only in upper surface 19 of the material. *See id.* at 3:49-50 ("Implant surface of first substrate to create a compliant layer (e.g., amorphous silicon layer)"); 5:52-6:14 ("The implantation process forms an 'amorphous' layer 15 of silicon overlying single crystal silicon material. . . . The amorphous silicon layer has a substantially planar upper surface 19, which also has amorphous characteristics."); 8:16-18; Figs. 3, 4; *see also* TSMC1003 at ¶ 36.

Cheung discloses that the substrate 10 is doped with impurities including boron or arsenic. *See* TSMC1005 at 4:15-20; *see also* TSMC1003 at ¶ 37.

a second substrate of substantially one second material amorphized substantially only in a second surface of said second material and containing one of boron and arsenic;

Cheung discloses a substrate 20 of substantially one material, *e.g.*, silicon. *See* TSMC1005 at 4:66-5:1. The one material, *e.g.*, silicon, is amorphized, *e.g.*, amorphous layer of silicon, substantially only in a surface of the material. *See id.* at

8:21-23, 32-65; *see also* TSMC1003 at ¶ 36.

Cheung discloses that the substrate 20 is doped with impurities including boron or arsenic. *See* TSMC1005 at 5:4-7; *see also* TSMC1003 at ¶ 37.

said first surface being bonded to said second surface to form a bonded pair of substrates.

Cheung discloses bonding the surface of amorphous silicon layer 15 of substrate 10 with the surface of amorphous layer of silicon of substrate 20. *See* TSMC1005 at 8:26-29, Col. 8:32-41 ("[T]he present invention provides a method for bonding substrates together using first and second compliant layers of amorphous silicon, for example, on the first substrate and second substrate, respectively."); Fig. 8; *see also* TSMC1003 at ¶ 36.

D. Claims 54-59: Claims 54-59 are dependent on Claim 53, which as set forth in GROUND 1(C), Cheung teaches the limitations of Claim 53.

Claim 54 recites: "one of said first and second substrates of said bonded pair being amorphized only in said first surface and in a third surface of said first material; a third substrate of substantially one third material amorphized only in a third surface of said third material; and said third surface bonded to said fourth surface." Cheung describes bonding the substrates 10 and 20, as discussed above. *See* TSMC1005 at 8:10-41. Cheung teaches that the invention can be applied "for multi-layered integrated circuit devices, three-dimensional packaging of integrated

semiconductor devices," and more. *See id.* at 1:17-21.

Accordingly, it would have been obvious to a POSITA to amorphize only the first surface and a third surface of the first material, amorphize another surface of a third material of a third substrate, and bond the surface of the third material to the third surface as recited in Claim 54 to form multi-layered integrated circuit devices or a three-dimensional package as described in Cheung. *See also* TSMC1003 at ¶ 38. (Petitioner notes "third surface" is used multiple times to refer to differing surfaces and that "said fourth surface" lacks a proper antecedent.)

Moreover, "the mere duplication of parts has no patentable significance unless a new and unexpected result is produced." Claim 54 requires nothing more than the duplication of the parts recited in Claim 53, which does not produce any new and/or unexpected results.

Claim 55 recites "wherein said first and second substrates are selected from Si, InGaAs, InP, GaAs, Ge and SiC." Cheung discloses that the substrates are "silicon," "compound semiconductors and the like," or "gallium arsenide [(GaAs)], gallium nitride (GaN), and others." *See* TSMC1005 at 4:10-15, 25-27; 9:52-53.

Claim 56 recites wherein "said first and second substrates each comprises a silicon substrate; and said first and second surfaces each comprises a silicon surface." Cheung discloses that each of the substrates 10 and 20 are silicon. *See id.* at 4:10-15; 4:66-5:3. Cheung discloses that each of the surfaces of the amorphous

silicon layer 15 of substrate 10 and amorphous layer of silicon of substrate 20 is a silicon surface. *See id.* at 8:32-41, 62-65; 5:52-6:14.

Claim 57 recites said first surface comprises a substantially planar surface of a first silicon layer formed on said first device." Cheung discloses the surface 19 of the amorphous silicon layer 15 is "a substantially planar upper surface." *See id.* at 6:12-14. Cheung further discloses that the invention can be applied to "multi-layered integrated circuit devices, three-dimensional packaging of integrated semiconductor devices, photonic devices, piezoelectronic devices, microelectromechanical systems ('MEMS'), sensors, actuators, solar cells, flat panel displays (e.g., LCD, AMLCD), biological and biomedical devices, and the like." *See id.* at 1:17-24. (Petitioner notes that "said first device" lacks a proper antecedent.)

Claim 57 further recites "said second surface comprises a substantially planar surface of a second silicon layer formed on said second device." Cheung discloses forming a surface of an amorphous layer of silicon. *See id.* at 8:21-23, 32-65. Cheung describes a corresponding amorphous silicon layer as having "a substantially planar upper surface." *See id.* at 6:12-14. Cheung further discloses that the invention can be applied to "multi-layered integrated circuit devices, three-dimensional packaging of integrated semiconductor devices, photonic devices, piezoelectronic devices, microelectromechanical systems ('MEMS'), sensors,

actuators, solar cells, flat panel displays (e.g., LCD, AMLCD), biological and biomedical devices, and the like." *See id.* at 1:17-24. (Petitioner notes that "said second device" lacks a proper antecedent.)

Claim 58 recites that each of the first surface and the second surface "comprises a surface exposed to a boron-containing plasma." The limitation "*exposed* to a boron-containing plasma" (emphasis added) is a product-by-process limitation, which only requires Petitioner to show a same structure.

To the extent that exposure to a boron-containing plasma requires the surfaces to resultantly contain boron, to which Petitioner does not concede, Cheung discloses that the surface 19 of the amorphous silicon layer 15 of substrate 10 and the surface of the amorphous layer of silicon of substrate 20 each comprise boron. *See* TSMC1005 at 4:12-20; 5:3-7; 6:9-14; 8:62-65; *see also* TSMC1003 at ¶ 37. Hence, Cheung discloses a same structure.

Claim 59 recites that each of the first surface and the second surface "comprises a surface implanted with one of boron and arsenic." The limitation "*implanted* with one of boron and arsenic" (emphasis added) is a product-by-process limitation, which only requires Petitioner to show a same structure.

Cheung discloses that the surface 19 of the amorphous silicon layer 15 of substrate 10 and the surface of the amorphous layer of silicon of substrate 20 each comprise boron or arsenic. *See* TSMC1005 at 4:12-20; 5:3-7; 6:9-14; 8:62-65; *see*

also TSMC1003 at ¶ 37. Hence, Cheung discloses a same structure.

Ground 2: Claims 1-14 and 53-60 are obvious under 35 U.S.C. § 103(a) over Cheung in view of Saito.

A. Claims 1 and 53: As set forth in GROUND 1 Cheung anticipates or renders obvious independent Claims 1 and 53. To the extent that Cheung may not teach nearly-amorphized layers or substrates "containing one of boron and arsenic," as recited in Claims 1 and 53, respectively, it would have been obvious to a POSITA to implant Cheung's substrates to form first and second "nearly-amorphized" layers (Claim 1) or to form first and second substrates (Claim 53) "containing one of boron and arsenic" using a plasma containing ions of silicon or germanium while simultaneously including ions of one of boron and arsenic as taught by Saito (*see* TSMC1006 at 2:40-59; 3:30-42) in order to dope Cheung's surfaces with one of boron and arsenic for the formation of a device in the surfaces, such as taught by Cheung, *see* TSMC1005 at 1:19-24. *See also* TSMC1003 at ¶ 39.

B. Claims 2-10, 12-14, and 54-59: As set forth in GROUND 2(A) Cheung in combination with Saito teaches the limitations of Claims 1 and 53. Further, as set forth in GROUND 1 Cheung teaches the limitations of claims 2-10, 12-14, and 54-59, and hence, these claims are obvious over Cheung in view of Saito.

C. Claims 6-9 and 11-14: Claims 6-9 and 11-14 are dependent on Claim 1, which as set forth in GROUNDS 1 and 2(A) Cheung alone or in combination with

Saito teaches the limitations of Claim 1.

Claim 6 recites that each of the first and second surface are "exposed to a boron-containing plasma." It would have been obvious to a POSITA to expose Cheung's silicon surfaces of the respective substrates to a plasma containing ions of silicon or germanium while simultaneously including ions of boron as taught by Saito (*see* TSMC1006 at 2:40-59; 3:30-42) in order to dope Cheung's surfaces with boron for the formation of a device in the surfaces, such as taught by Cheung, *see* TSMC1005 at 1:19-24. *See also* TSMC1003 at ¶ 39.

Claim 7 recites that the first and second surface are silicon surfaces "implanted with boron." It would have been obvious to a POSITA to implant Cheung's silicon surfaces with boron as described in Saito (*see* TSMC1006 at 2:40-59; 3:30-42) in order to dope Cheung's surfaces with boron for the formation of a device in the surfaces, such as taught by Cheung, *see* TSMC1005 at 1:19-24. *See also* TSMC1003 at ¶ 39.

Claim 8 recites that the first and second surface are silicon surfaces "implanted with arsenic." It would have been obvious to a POSITA to implant Cheung's silicon surfaces with arsenic as described by Saito (*see* TSMC1006 at 2:40-59; 3:30-42) in order to dope Cheung's surfaces with arsenic for the formation of a device in the surfaces, such as taught by Cheung, *see* TSMC1005 at 1:19-24. *See, also* TSMC1003 at ¶ 39.

Claim 9 recites that "at least one of boron-boron and Si covalent bonds" are formed between the first and second substrates. It would have been obvious to a POSITA to implant/expose Cheung's surfaces with boron as described by Saito (*see* TSMC1006 at 2:40-59; 3:30-42) in order to dope Cheung's surfaces for the formation of a device in the surfaces, such as taught by Cheung, *see* TSMC1005 at 1:19-24. *See, also* TSMC1003 at ¶ 39. With this plasma implant/exposure, Cheung's surfaces will have boron atoms. *See* TSMC1003 at ¶ 40.

With Cheung's surfaces being exposed to a boron-containing plasma and having boron atoms thereon, Cheung's bonding process will undergo a same or similar process as described in the '133 Patent to achieve silicon covalent bonds and boron-boron bonds. Particularly, as in Cheung, the '133 Patent teaches that bonding boron treated silicon surfaces with boron atoms on the surfaces results in silicon covalent bonds and boron-boron bonds across the interface, even more at temperatures of 350-400°C. *See* TSMC1001 at 7:66-8:21. Accordingly, Cheung in combination with Saito will result in silicon covalent bonds and boron-boron bonds. *See, also* TSMC1003 at ¶ 40. Additionally, where a reason to believe that a claimed limitation may be inherent in the prior art is shown, as is here, the burden shifts to the Patent Owner to provide evidence to the contrary. *See, e.g.*, *Precision BioSciences, Inc. v. Institut Pasteur & Universite Pierre et Marie Curie*, No. 2011-012285, 2012 WL 1050572 at *3 (B.P.A.I. March 14, 2012); *Ice Ban Am., Inc. v.*

Patent of Sears Ecological Applications Co., LLC, No. 2010-009574, 2010 WL 4913983 at *8 (B.P.A.I. Nov. 30, 2010).

Claim 11 recites that the first and second layers "each comprise a few monolayers of boron." A POSITA would recognize that the energy and dose of B_2H_6 implants as described in Saito would lead to the formation of a few monolayers of boron in the surface of the substrates. *See* TSMC1003 at ¶ 41. It would have been obvious to a POSITA to implant Cheung's surfaces with boron as described in Saito (*see* TSMC1006 at 2:40-59; 3:30-42), which would result in the formation of a few monolayers of boron in the layers, in order to dope Cheung's surfaces with boron for the formation of a device in the surfaces, such as taught by Cheung, *see* TSMC1005 at 1:19-24. *See also* TSMC1003 at ¶¶ 39, 41.

Claim 12 recites that each of the first and second surfaces comprise "an amorphous boron-containing layer." It would have been obvious to a POSITA to implant Cheung's surfaces with boron as described in Saito (*see* TSMC1006 at 2:40-59; 3:30-42) to form the surfaces to comprise an amorphous boron-containing layer in order to dope Cheung's surfaces with boron for the formation of a device in the surfaces, such as taught by Cheung, *see* TSMC1005 at 1:19-24. *See also* TSMC1003 at ¶ 39.

Claim 13 recites that each of the first and second surfaces is "exposed to a boron-containing plasma." It would have been obvious to a POSITA to expose

Cheung's silicon surfaces of the respective substrates to a plasma containing ions of silicon or germanium while simultaneously including ions of boron as taught by Saito (*see* TSMC1006 at 2:40-59; 3:30-42) in order to dope Cheung's surfaces with boron for the formation of a device in the surfaces, such as taught by Cheung, *see* TSMC1005 at 1:19-24. *See also* TSMC1003 at ¶ 39.

Claim 14 recites that each of the first and second surfaces comprises a surface "exposed to an inert gas plasma." Saito further describes that argon may be used as a carrier gas for the plasma ion implantation. *See* TSMC1006 at 4:26-27. A plasma containing silicon or germanium with a carrier gas such as argon may be formed in Saito's plasma chamber, which may be used to form Saito's amorphous regions. *See* TSMC1006 at 4:22-32; FIG. 1. It would have been obvious to a POSITA to use a plasma that contains silicon or germanium, as taught by both Cheung and Saito, and an inert gas such as argon for a carrier, as taught by Saito, in order to form Cheung's amorphous surfaces. *See* TSMC1003 at ¶¶ 35, 42. Using argon as a carrier gas to implant silicon or germanium is a simple substitution of one known technique for another known technique to obtain the predictable result of amorphizing a substrate. *See, e.g.*, *KSR Intn'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007).

D. Claims 58-60: Claims 58-60 are dependent on Claim 53, which as set forth in GROUNDS 1 and 2(A) Cheung alone or in combination with Saito teaches.

Claim 58 recites that each of the first and second surfaces comprises "a surface exposed to a boron-containing plasma." It would have been obvious to a POSITA to expose Cheung's silicon surfaces of the respective substrates to a plasma containing ions of silicon or germanium while simultaneously including ions of boron as taught by Saito (*see* TSMC1006 at 2:40-59; 3:30-42) in order to dope Cheung's surfaces with boron for the formation of a device in the surfaces, such as taught by Cheung, *see* TSMC1005 at 1:19-24. *See also* TSMC1003 at ¶ 39.

Claim 59 recites that each of the first and second surfaces comprises "a surface implanted with one of boron and arsenic." It would have been obvious to a POSITA to implant Cheung's surfaces with one of boron and arsenic as described by Saito (*see* TSMC1006 at 2:40-59; 3:30-42) in order to dope Cheung's surfaces for the formation of a device in the surfaces, such as taught by Cheung, *see* TSMC1005 at 1:19-24. *See, also* TSMC1003 at ¶ 39.

Claim 60 depends from Claim 59 and recites "boron-boron covalent bonds formed between" the first and second substrates. It would have been obvious to a POSITA to implant and/or expose Cheung's surfaces with boron as described by Saito (*see* TSMC1006 at 2:40-59; 3:30-42) in order to dope Cheung's surfaces for the formation of a device in the surfaces, such as taught by Cheung, *see* TSMC1005 at 1:19-24. *See, also* TSMC1003 at ¶ 39. With this plasma implant and/or exposure, Cheung's surfaces will have boron atoms. *See* TSMC1003 at ¶

40.

With Cheung's surfaces being exposed to a boron-containing plasma and having boron atoms thereon, Cheung's bonding process will undergo a same or similar process as described in the '133 Patent to achieve boron-boron covalent bonds. Particularly, as in Cheung, the '133 Patent teaches that bonding boron treated silicon surfaces with boron atoms on the surfaces results in boron-boron covalent bonds across the interface, even more at temperatures of 350-400°C. *See* TSMC1001 at 7:66-8:21. Accordingly, Cheung in combination with Saito will result in boron-boron covalent bonds. *See, also* TSMC1003 at ¶ 40. Additionally, in proceedings before the Office, where a reason to believe that a claimed limitation may be inherent in the prior art is shown, as is here, the burden shifts to the Patent Owner to provide evidence to the contrary.

GROUND 3: Claims 1-14 and 53-59 are obvious under 35 U.S.C. § 103(a) over Cheung in view of Tian.

A. Claims 1 and 53: As set forth in GROUND 1 Cheung anticipates or renders obvious Claims 1 and 53. To the extent that Cheung may not teach nearly-amorphized layers or substrates "containing one of boron and arsenic," as recited in Claims 1 and 53, respectively, it would have been obvious to a POSITA to modify the plasma ion implantation, as taught by Cheung, to include the boron or arsenic implantation, as taught or suggested by Tian (*see* TSMC1008 at Abstract, 1230), such that the amorphous layers contain one of boron and arsenic, to dope

Cheung's surfaces with one of boron and arsenic for the formation of a device in the surfaces, such as taught by Cheung, *see* TSMC1005 at 1:19-24. *See also* TSMC1003 at ¶ 43.

B. Claims 2-10, 12-14, and 54-59: As set forth in GROUND 3(A) Cheung in combination with Tian teaches the limitations of Claims 1 and 53. Further, as set forth in GROUND 1 Cheung teaches the limitations of claims 2-10, 12-14, and 54-59, and hence, these claims are obvious over Cheung in view of Tian.

C. Claims 7, 8, 11, and 12: Claim 7, 8, 11, and 12 are dependent on Claim 1, which as set forth in GROUNDS 1 and 3(A) Cheung alone or in combination with Tian teaches the limitations of Claim 1.

Claim 7 recites that the first and second surface are silicon surfaces "implanted with boron." It would have been obvious to a POSITA to modify the plasma ion implantation, as taught by Cheung, to include the boron implantation, as taught or suggested by Tian (*see* TSMC1008 at Abstract, 1230), to dope Cheung's surfaces with boron for the formation of a device in the surfaces, such as taught by Cheung, *see* TSMC1005 at 1:19-24. *See also* TSMC1003 at ¶ 43.

Claim 8 recites that the first and second surface are silicon surfaces "implanted with arsenic." It would have been obvious to a POSITA to modify the plasma ion implantation, as taught by Cheung, to include the arsenic implantation, as taught or suggested by Tian (*see* TSMC1008 at Abstract, 1230), to dope

Cheung's surfaces with arsenic for the formation of a device in the surfaces, such as taught by Cheung, *see* TSMC1005 at 1:19-24. *See also* TSMC1003 at ¶ 43.

Claim 11 recites that the first and second layers "each comprise a few monolayers of boron." A POSITA would know that by controlling the dose and energy of a boron species in an ion shower or ion implantation, a region having a thickness of a few monolayers at or near the surface of the substrate would be boron rich. *See* TSMC1003 at ¶ 44. It would have been obvious to a POSITA to modify the plasma ion implantation, as taught by Cheung, to include the boron implantation, as taught or suggested by Tian (*see* TSMC1008 at Abstract, 1230), which would result in the formation of a few monolayers of boron in the layers, to dope Cheung's surfaces with boron for the formation of a device in the surfaces, such as taught by Cheung, *see* TSMC1005 at 1:19-24. *See also* TSMC1003 at ¶ 43.

Claim 12 recites that each of the first and second surfaces comprise "an amorphous boron-containing layer." It would have been obvious to a POSITA to modify the plasma ion implantation, as taught by Cheung, to include the boron implantation, as taught or suggested by Tian (*see* TSMC1008 at Abstract, 1230), such that Cheung's surfaces comprise an amorphous boron-containing layer, to dope Cheung's surfaces with boron for the formation of a device in the surfaces, *see* TSMC1005 at 1:19-24. *See also* TSMC1003 at ¶ 43.

D. Claim 59: Claim 59 is dependent on Claim 53, which as set forth in

GROUNDS 1 and 3(A) Cheung alone or in combination with Tian teaches the limitations of Claim 53. Claim 59 further recites that each of the first and second surfaces comprises "a surface implanted with one of boron and arsenic." It would have been obvious to a POSITA to modify the plasma ion implantation, as taught by Cheung, to include the boron or arsenic implantation, as taught or suggested by Tian (*see* TSMC1008 at Abstract, 1230), to dope Cheung's surfaces with one of boron and arsenic for the formation of a device in the surfaces, such as taught by Cheung, *see* TSMC1005 at 1:19-24. *See also* TSMC1003 at ¶ 43.

Ground 4: Claims 1-14 and 53-60 are obvious under 35 U.S.C. § 103(a) over Cheung in view of Tian and Saito.

A. Claims 1 and 53: As set forth in GROUNDS 1 and 3(A) Cheung anticipates or renders obvious or Cheung in combination with Tian renders obvious independent Claims 1 and 53. To the extent that Cheung alone or in combination with Tian may not teach nearly-amorphized layers or substrates "containing one of boron and arsenic," as recited in Claims 1 and 53, respectively, it would have been obvious to a POSITA to modify the implantation of silicon ions and boron or arsenic ions as described in Cheung and/or Tian to be a plasma ion implantation containing silicon ions and boron or arsenic ions as described in Saito (*see* TSMC1006 at 2:40-59; 3:30-42) in order to dope boron or arsenic into surfaces for the formation of a device in the surfaces, such as taught by Cheung, *see* TSMC1005 at 1:19-24. *See also* TSMC1003 at ¶ 45.

B. Claims 2-14 and 54-59: As set forth in GROUND 4(A) Cheung in combination with Tian and Saito teaches the limitations of Claims 1 and 53. Further, as set forth in GROUNDS 1 and 3 Cheung alone or in combination with Tian teaches the limitations of claims 2-14 and 54-59, and hence, these claims are obvious over Cheung in view of Tian and Saito.

C. Claims 6, 9, 13, and 14: Claim 6, 9, 13, and 14 are dependent on Claim 1, which as set forth in GROUNDS 1 and 4(A) Cheung alone or in combination Tian and Saito teaches the limitations of Claim 1.

Claim 6 recites that the first and second surface are "exposed to a boron-containing plasma." It would have been obvious to a POSITA to modify the implantation of silicon ions and boron ions as described in Cheung and/or Tian to use a plasma ion implantation containing silicon ions and boron ions as described in Saito (*see* TSMC1006 at 2:40-59; 3:30-42) in order to dope boron into surfaces for the formation of a device in the surfaces, such as taught by Cheung, *see* TSMC1005 at 1:19-24. *See also* TSMC1003 at ¶ 45.

Claim 9 recites that "at least one of boron-boron and Si covalent bonds" are formed between the first and second substrates. It would have been obvious to a POSITA to implant and/or expose Cheung's surfaces with boron as described by Saito (*see* TSMC1006 at 2:40-59; 3:30-42) in order to dope Cheung's surfaces for the formation of a device in the surfaces, such as taught by Cheung, *see*

TSMC1005 at 1:19-24. *See, also* TSMC1003 at ¶ 45. With this plasma implant and/or exposure, Cheung's surfaces will have boron atoms. *See id.* at ¶ 46.

With Cheung's surfaces being exposed to a boron-containing plasma and having boron atoms thereon, Cheung's bonding process will undergo a same or similar process as described in the '133 Patent to achieve silicon covalent bonds and boron-boron bonds. Particularly, as in Cheung, the '133 Patent teaches that bonding boron treated silicon surfaces with boron atoms on the surfaces results in silicon covalent bonds and boron-boron bonds across the interface, even more at temperatures of 350-400°C. *See* TSMC1001 at 7:66-8:21. Accordingly, Cheung and Tian in combination with Saito will result in silicon covalent bonds and boron-boron bonds. *See, also* TSMC1003 at ¶ 46. Additionally, in proceedings before the Office, where a reason to believe that a claimed limitation may be inherent in the prior art is shown, as is here, the burden shifts to the Patent Owner to provide evidence to the contrary.

Claim 13 recites that each of the first and second surfaces is "exposed to a boron-containing plasma." It would have been obvious to a POSITA to modify the implantation of silicon ions and boron ions as described in Cheung and/or Tian to use a plasma ion implantation containing silicon ions and boron ions as described in Saito (*see* TSMC1006 at 2:40-59; 3:30-42) in order to dope boron into surfaces for the formation of a device in the surfaces, such as taught by Cheung, *see*

TSMC1005 at 1:19-24. *See also* TSMC1003 at ¶ 45.

Claim 14 recites that each of the first and second surfaces comprises a surface "exposed to an inert gas plasma." Saito further describes that argon may be used as a carrier gas for the plasma ion implantation. *See* TSMC1006 at 4:26-27. A plasma containing silicon or germanium with a carrier gas such as argon may be formed in Saito's plasma chamber, which may be used to form Saito's amorphous regions. *See* TSMC1006 at 4:22-32; FIG. 1. It would have been obvious to a POSITA to use a plasma that contains silicon or germanium, as taught by both Cheung and/or Tian, and an inert gas such as argon for a carrier, as taught by Saito, in order to form amorphous surfaces. *See* TSMC1003 at ¶¶ 35, 47. Using argon as a carrier gas to implant silicon or germanium is a simple substitution of one known technique for another known technique to obtain the predictable result of amorphizing a substrate.

D. Claim 58: Claim 58 is dependent on Claim 53, which as set forth in GROUNDS 1 and 4(A) Cheung alone or in combination with Tian and Saito teaches the limitations of Claim 53. Claim 58 recites that each of the first and second surfaces comprises "a surface exposed to a boron-containing plasma." It would have been obvious to a POSITA to modify the implantation of silicon ions and boron ions as described in Cheung and/or Tian to use a plasma ion implantation containing silicon ions and boron ions as described in Saito (*see* TSMC1006 at

2:40-59; 3:30-42) in order to dope boron into surfaces for the formation of a device in the surfaces, such as taught by Cheung, *see* TSMC1005 at 1:19-24. *See also* TSMC1003 at ¶ 45.

E. Claim 60: Claim 60 is dependent upon Claim 59, which is dependent on Claim 53. As set forth in GROUNDS 1 and 4(A)-(B) Cheung alone or in combination with Tian and Saito teaches the limitations of Claims 53 and 59. Claim 60 recites "boron-boron covalent bonds formed between" the first and second substrates. It would have been obvious to a POSITA to implant and/or expose Cheung's surfaces with boron as described by Saito (*see* TSMC1006 at 2:40-59; 3:30-42) in order to dope Cheung's surfaces for the formation of a device in the surfaces, such as taught by Cheung, *see* TSMC1005 at 1:19-24. *See, also* TSMC1003 at ¶ 45. With this plasma implant and/or exposure, Cheung's surfaces will have boron atoms. *See id.* at ¶ 46.

With Cheung's surfaces being exposed to a boron-containing plasma and having boron atoms thereon, Cheung's bonding process will undergo a same or similar process as described in the '133 Patent to achieve boron-boron covalent bonds. Particularly, as in Cheung, the '133 Patent teaches that bonding boron treated silicon surfaces with boron atoms on the surfaces results in boron-boron covalent bonds across the interface, even more at temperatures of 350-400°C. *See* TSMC1001 at 7:66-8:21. Accordingly, Cheung and Tian in combination with Saito

will result in boron-boron covalent bonds. *See, also* TSMC1003 at ¶ 46. Additionally, in proceedings before the Office, where a reason to believe that a claimed limitation may be inherent in the prior art is shown, as is here, the burden shifts to the Patent Owner to provide evidence to the contrary.

GROUND 5: Claims 1-7, 9, 10, 12, 13, 53-56, 58, and 59 are anticipated under 35 U.S.C. § 102(b) by or obvious under 35 U.S.C. § 103(a) over Fujino.

A. Claim 1: ***A bonded structure, comprising:***

Fujino discloses silicon wafer direct bonding. *See* TSMC1007 at Title.

a first substrate having a first surface, a first nearly-amorphized layer containing one of boron and arsenic formed uniformly over said first surface; and

a second substrate having a second surface, a second nearly-amorphized layer containing one of boron and arsenic formed uniformly over said second surface;

Fujino discloses bonding "boron-doped, CZ-grown silicon wafers." *See id.* at 1322; *see also id.* at Fig. 1. Fujino describes that "[s]ilicon ions were implanted to make the silicon wafer surface amorphous," and amorphous layers on wafers. *See id*. Since Fujino discloses amorphous layers, Fujino discloses layers that each at least closely approximates an amorphous layer, *i.e.*, a nearly-amorphized layer. *See* TSMC1003 at ¶ 48.

Fujino discloses that the wafers are each doped with boron. *See* TSMC1007 at 1322. Thus, Fujino's amorphous layers each contain one of boron and arsenic. *See* TSMC1003 at ¶ 49.

Fujino discloses eliminating a native oxide film from the surfaces of the wafers prior to bonding the amorphous surface layers, thus leaving the boron-doped silicon as the surface. *See* TSMC1007 at 1324.

said first surface being bonded to said second surface to form a bonded pair of substrates.

Fujino describes bonding the wafers having amorphous layers. *See id.* at 1322 (The "wafers were bonded to each other under atmospheric pressure at room temperature."), 1323 (describing results of bonding the "wafers with amorphous layer[s]").

B. Claims 2-7, 9, 10, 12, and 13: Claims 2-7, 9, 10, 12, and 13 are dependent on Claim 1, which as set forth in GROUND 5(A) Fujino discloses or renders obvious the limitations of Claim 1.

Claim 2 recites: "one of said first and second substrates of said bonded pair having a third surface, said third surface having a nearly-amorphized layer; a third substrate having a fourth surface, a fourth nearly-amorphized layer formed in said fourth surface; and said third surface bonded to said fourth surface."

"[T]he mere duplication of parts has no patentable significance unless a new

and unexpected result is produced." Claim 2 requires nothing more than the duplication of the parts recited in Claim 1, which does not produce any new and/or unexpected results for bonding nearly-amorphized layers of additional substrates.

Claim 3 recites "wherein said first and second substrates are selected from Si, InGaAs, InP, GaAs, Ge and SiC." Fujino discloses that the wafers are silicon. *See* TSMC1007 at 1322.

Claim 4 recites "wherein: said first and second substrates each comprises a silicon substrate; and said first and second surfaces each comprises a silicon surface." Fujino discloses that the wafers are silicon substrates. *See id.* at 1322. Fujino further discloses eliminating a native oxide film from the surfaces of the wafers prior to bonding the amorphous surfaces. *See id.* at 1324. Accordingly, each of the surfaces comprises a silicon surface.

Claim 5 recites "wherein: said first and second substrates comprise respective first and second semiconductor devices." Fujino discloses that silicon wafer direct bonding can be used for "isolated vertical-DMOS and control circuits on a single chip." *See id.* at 1:17-24.

Claim 6 recites "wherein: said first surface comprises a first silicon surface exposed to a boron-containing plasma; and said second surface comprises a second silicon surface exposed to a boron-containing plasma." The limitation "*exposed* to a boron-containing plasma" (emphasis added) is a product-by-process limitation,

which only requires Petitioner to show a same structure.

To the extent that exposure to a boron-containing plasma requires the surfaces to resultantly contain boron, to which Petitioner does not concede, Fujino teaches that the surfaces each are silicon and comprise boron. *See* TSMC1007 at 1322, 1324; *see also* TSMC 1003 at ¶ 49. Fujino discloses eliminating a native oxide film from the surfaces of the wafers prior to bonding the amorphous surfaces. *See* TSMC1007 at 1324. Accordingly, each of the surfaces comprises a silicon surface. Hence, Fujino teaches a same structure.

Claim 7 recites that each of the first surface and the second surface comprises a "silicon surface implanted with boron." The limitation "*implanted* with boron" (emphasis added) is a product-by-process limitation, which only requires Petitioner to show a same structure.

Fujino teaches that the surfaces each are silicon and comprise boron. *See* TSMC1007 at 1322, 1324; *see also* TSMC 1003 at ¶ 49. Fujino discloses eliminating a native oxide film from the surfaces of the wafers prior to bonding the amorphous surfaces. *See* TSMC1007 at 1324. Accordingly, each of the surfaces comprises a silicon surface. Hence, Fujino teaches a same structure.

Claim 9 recites "at least one of boron-boron and Si covalent bonds formed between said first and second substrates." Fujino discloses a method for "Silicon Wafer Direct Bonding." *See* TSMC1007 at 1322. Fujino discloses "removal of

contamination" and "surface treatment" steps on the silicon surfaces of the wafers. *See id.* at Fig. 1; *see also id.* at 1324 (minimizing SiO layer by eliminating the native oxide). The subsequent contacting and annealing steps, *see id.* at Fig. 1, form a bond between silicon atoms in the silicon surface, which includes a silicon-to-silicon covalent bond. *See* TSMC1003 at ¶ 50.

Claim 10 recites "wherein: said first and second amorphous layers are each in the range of a few nm in thickness." Fujino discloses forming an amorphous silicon layer to a depth of 139 nm. *See* TSMC1007 at 1323. Hence, Fujino discloses a thickness in the range of 165 nm, *i.e.*, a range of a few nm in thickness.

Assuming for the sake of argument that Fujino's disclosure does not anticipate the claim, Fujino's range overlaps the range of a few nm in thickness, and therefore, Fujino renders Claim 10 *prima facie* obvious.

Even assuming further for the sake of argument that Fujino's disclosure does not overlap, "it is not inventive to discover the optimum or workable ranges by routine experimentation." Fujino teaches that "the thickness of the amorphous layer was varied by adjusting the acceleration energy." *Id.* at 1322.The range of thickness of a few nm could be determined by a POSITA by routine experimentation. *See* TSMC1003 at ¶ 51.

Claim 12 recites "said first surface comprises an amorphous boron-containing layer." Fujino discloses surfaces of amorphous layers of silicon wafers.

See TSMC1007 at 1322. Fujino discloses that the silicon wafers are boron-doped. *See id.* Thus, Fujino's amorphous layers contain boron. *See* TSMC1003 at ¶ 49. Fujino discloses eliminating a native oxide film from the surfaces of the wafers prior to bonding the amorphous surface layers, thus leaving the boron-doped silicon as the surface. *See* TSMC1007 at 1324.

Claim 13 recites that each of the first surface and the second surface "comprises a surface exposed to a boron-containing plasma." The limitation "exposed to a boron-containing plasma" (emphasis added) is a product-by-process limitation, which only requires Petitioner to show a same structure.

To the extent that exposure to a boron-containing plasma requires the surfaces to resultantly contain boron, to which Petitioner does not concede, Fujino discloses that the wafers each are boron-doped. *See* TSMC1007 at 1322. Thus, Fujino's surfaces of the amorphous silicon layers each contain boron. *See* TSMC1003 at ¶ 49. Hence, Fujino teaches a same structure.

C. Claim 53: ***A bonded structure, comprising:***

Fujino discloses silicon wafer direct bonding. *See* TSMC1007 at Title.

a first substrate of substantially one first material amorphized substantially only in a first surface of said first material and containing one of boron and arsenic; and

a second substrate of substantially one second material amorphized

substantially only in a second surface of said second material and containing one of boron and arsenic;

Fujino discloses bonding "boron-doped, CZ-grown silicon wafers." *See id.* at 1322. Fujino describes that "[s]ilicon ions were implanted to make the silicon wafer surface amorphous." *See id*.

Fujino discloses eliminating a native oxide film from the surfaces of the wafers prior to bonding the amorphous surface layers, thus leaving the boron-doped silicon as the surfaces. *See id.* at 1324.

Thus, Fujino describes substrates each of substantially one material amorphized substantially only in a respective surface of the material and each containing one of boron and arsenic. *See* TSMC1003 at ¶¶ 52, 53.

said first surface being bonded to said second surface to form a bonded pair of substrates.

Fujino describes bonding the wafers having amorphized surface layers. *See* TSMC1007 at 1322 (The "wafers were bonded to each other under atmospheric pressure at room temperature."), 1323 (describing results of bonding the "wafers with amorphous layer[s]"). Thus, Fujino describes bonding the first surface to the second surface to form a bonded pair of substrates. *See* TSMC1003 at ¶ 52.

D. Claims 54-56, 58, and 59: Claims 54-56, 58, and 59 are dependent on Claim 53, which as set forth in GROUND 5(C) Cheung teaches.

Claim 54 recites: "one of said first and second substrates of said bonded pair being amorphized only in said first surface and in a third surface of said first material; a third substrate of substantially one third material amorphized only in a third surface of said third material; and said third surface bonded to said fourth surface." "[T]he mere duplication of parts has no patentable significance unless a new and unexpected result is produced." Claim 54 requires nothing more than the duplication of the parts recited in Claim 53, which does not produce any new and/or unexpected results for bonding amorphized surfaces of additional substrates.

Claim 55 recites "wherein said first and second substrates are selected from Si, InGaAs, InP, GaAs, Ge and SiC." Fujino discloses that the first and second wafers are silicon. *See* TSMC1007 at 1322.

Claim 56 recites wherein "said first and second substrates each comprises a silicon substrate; and said first and second surfaces each comprises a silicon surface." Fujino discloses that the wafers are silicon substrates. *See id.* at 1322. Fujino discloses eliminating a native oxide film from the surfaces of the wafers prior to bonding the amorphized surfaces. *See id.* at 1324. Accordingly, each of the surfaces comprises a silicon surface.

Claim 58 recites that each of the first surface and the second surface "comprises a surface exposed to a boron-containing plasma." The limitation

"*exposed* to a boron-containing plasma" (emphasis added) is a product-by-process limitation, which only requires Petitioner to show a same structure.

To the extent that exposure to a boron-containing plasma requires the surfaces to resultantly contain boron, to which Petitioner does not concede, Fujino teaches that the surfaces each comprise boron. *See* TSMC1007 at 1322; *see also* TSMC 1003 at ¶ 53. Hence, Fujino teaches a same structure.

Claim 59 recites that each of the first surface and the second surface "comprises a surface implanted with one of boron and arsenic." The limitation "*implanted* with one of boron and arsenic" (emphasis added) is a product-by-process limitation, which only requires Petitioner to show a same structure.

Fujino teaches that the surfaces each comprise boron. *See* TSMC1007 at 1322; *see also* TSMC 1003 at ¶ 53. Hence, Fujino teaches a same structure.

Ground 6: Claims 1-14, 53-56, and 58-60 are obvious under 35 U.S.C. § 103(a) over Fujino in view of Saito.

A. Claims 1 and 53: As set forth in GROUND 5 Fujino anticipates or renders obvious Claims 1 and 53. To the extent that Fujino may not teach nearly-amorphized layers or substrates "containing one of boron and arsenic," as recited in Claims 1 and 53, respectively, it would have been obvious to a POSITA to implant Fujino's substrates to form first and second "nearly-amorphized" layers (Claim 1) or to form first and second substrates (Claim 53) "containing one of boron and arsenic" using a plasma containing ions of silicon or germanium while

simultaneously including ions of one of boron and arsenic as taught by Saito (*see* TSMC1006 at 2:40-59; 3:30-42) in order to dope Fujino's surfaces with one of boron and arsenic for the formation of a device. *See also* TSMC1003 at ¶ 54.

B. Claims 2-7, 9, 10, 12, 13, 54-56, 58, and 59: As set forth in GROUND 6(A) Fujino in combination with Saito teaches the limitations of Claims 1 and 53. Further, as set forth in GROUND 5 Fujino teaches the limitations of claims 2-7, 9, 10, 12, 13, 54-56, 58, and 59, and hence, these claims are obvious over Fujino in view of Saito.

C. Claims 6-9 and 11-14: Claim 6-9 and 11-14 are dependent on Claim 1, which as set forth in GROUNDS 5 and 6(A) Fujino alone or in combination with Saito teaches the limitations of Claim 1.

Claim 6 recites that the first and second surface are "exposed to a boron-containing plasma." It would have been obvious to a POSITA to expose Fujino's silicon surfaces of the wafers to a plasma containing ions of silicon while simultaneously including ions of boron as taught by Saito (*see* TSMC1006 at 2:40-59; 3:30-42) in order to dope Fujino's surfaces with boron for the formation of a device in the surfaces. *See also* TSMC1003 at ¶ 54.

Claim 7 recites that the first and second surface are silicon surfaces "implanted with boron." It would have been obvious to a POSITA to implant Fujino's silicon surfaces with boron as described in Saito (*see* TSMC1006 at 2:40-

59; 3:30-42) in order to dope Fujino's surfaces with boron for the formation of a device in the surfaces. *See also* TSMC1003 at ¶ 54.

Claim 8 recites that the first and second surface are silicon surfaces "implanted with arsenic." It would have been obvious to a POSITA to implant Fujino's silicon surfaces with arsenic as described by Saito (*see* TSMC1006 at 2:40-59; 3:30-42) in order to dope Fujino's surfaces with arsenic for the formation of a device in the surfaces. *See, also* TSMC1003 at ¶ 54.

Claim 9 recites that "at least one of boron-boron and Si covalent bonds" are formed between the first and second substrates. It would have been obvious to a POSITA to implant/expose Fujino's surfaces with boron as described by Saito (*see* TSMC1006 at 2:40-59; 3:30-42) in order to dope Fujino's surfaces for the formation of a device. *See* TSMC1003 at ¶ 54. With this plasma implant/exposure, Fujino's surfaces will have boron atoms. *See* TSMC1003 at ¶ 55.

With Fujino's surfaces being exposed to a boron-containing plasma and having boron atoms thereon, Fujino's bonding process will undergo a same or similar process as described in the '133 Patent to achieve silicon covalent bonds and boron-boron bonds. Particularly, as in Fujino, the '133 Patent teaches that bonding boron treated silicon surfaces with boron atoms on the surfaces results in silicon covalent bonds and boron-boron bonds across the interface, even more at temperatures of 350-400°C. *See* TSMC1001 at 7:66-8:21. Accordingly, Fujino in

combination with Saito will result in silicon covalent bonds and boron-boron bonds. *See, also* TSMC1003 at ¶ 55. Additionally, where a reason to believe that a claimed limitation may be inherent in the prior art is shown, as is here, the burden shifts to the Patent Owner to provide evidence to the contrary.

Claim 11 recites that the first and second layers "each comprise a few monolayers of boron." One skilled in the art would recognize that the energy and dose of B_2H_6 implants as described in Saito would lead to the formation of a few monolayers of boron in the surface of the substrates. *See* TSMC1003 at ¶ 56. It would have been obvious to a POSITA to implant Fujino's surfaces with boron as described in Saito (*see* TSMC1006 at 2:40-59; 3:30-42), which would result in the formation of a few monolayers of boron in the layers, in order to dope Fujino's surfaces with boron for the formation of a device in the surfaces. *See also* TSMC1003 at ¶¶ 54, 56.

Claim 12 recites that each of the first and second surfaces comprise "an amorphous boron-containing layer." It would have been obvious to a POSITA to implant Fujino's surfaces with boron as described in Saito (*see* TSMC1006 at 2:40-59; 3:30-42) to form the surfaces to comprise an amorphous boron-containing layer in order to dope Fujino's surfaces with boron for the formation of a device in the surfaces. *See also* TSMC1003 at ¶ 54.

Claim 13 recites that each of the first and second surfaces is "exposed to a

boron-containing plasma." It would have been obvious to a POSITA to expose Fujino's silicon surfaces of the wafers to a plasma containing ions of silicon while simultaneously including ions of boron as taught by Saito (*see* TSMC1006 at 2:40-59; 3:30-42) in order to dope Fujino's surfaces with boron for the formation of a device in the surfaces. *See also* TSMC1003 at ¶ 54.

Claim 14 recites that each of the first and second surfaces comprises a surface "exposed to an inert gas plasma." Saito further describes that argon in a plasma may be used as a carrier gas for the ion implantation. *See* TSMC1006 at 4:26-27. A plasma containing silicon with a carrier gas such as argon may be formed in Saito's plasma chamber, which may be used to form Saito's amorphous regions. *See* TSMC1006 at 4:22-32; FIG. 1. It would have been obvious to a POSITA to use a plasma, as taught by Saito, that contains silicon for an implantation, as taught by Fujino, and an inert gas such as argon for a carrier, as taught by Saito, in order to form Fujino's amorphous surfaces. *See* TSMC1003 at ¶¶ 35, 57. Using argon as a carrier gas to implant silicon is a simple substitution of one known technique for another known technique to obtain the predictable result of amorphizing a substrate.

D. Claims 58-60: Claim 58-60 are dependent on Claim 53, which as set forth in GROUNDS 5 and 6(A) Fujino alone or in combination with Saito teaches.

Claim 58 recites that each of the first and second surfaces comprises "a

surface exposed to a boron-containing plasma." It would have been obvious to a POSITA to expose Fujino's surfaces to a plasma containing ions of silicon while simultaneously including ions of boron as taught by Saito (*see* TSMC1006 at 2:40-59; 3:30-42) in order to dope Fujino's surfaces with boron for the formation of a device in the surfaces. *See also* TSMC1003 at ¶ 54.

Claim 59 recites that each of the first and second surfaces comprises "a surface implanted with one of boron and arsenic." It would have been obvious to a POSITA to implant Fujino's surfaces using a plasma containing ions of silicon while simultaneously including ions of one of boron and arsenic as taught by Saito (*see* TSMC1006 at 2:40-59; 3:30-42) in order to dope Fujino's surfaces with one of boron and arsenic for the formation of a device. *See also* TSMC1003 at ¶ 54.

Claim 60 depends from Claim 59 (see above) and recites "boron-boron covalent bonds formed between" the first and second substrates. It would have been obvious to a POSITA to implant and/or expose Fujino's surfaces with boron as described by Saito (*see* TSMC1006 at 2:40-59; 3:30-42) in order to dope Fujino's surfaces for the formation of a device in the surfaces. *See, also* TSMC1003 at ¶ 54. With this plasma implant and/or exposure, Fujino's surfaces will have boron atoms. *See id.* at ¶ 55.

With Fujino's surfaces being exposed to a boron-containing plasma and having boron atoms thereon, Fujino's bonding process will undergo a same or

similar process as described in the '133 Patent to achieve boron-boron covalent bonds. Particularly, as in Fujino, the '133 Patent teaches that bonding boron treated silicon surfaces with boron atoms on the surfaces results in boron-boron covalent bonds across the interface, even more at temperatures of 350-400°C. *See* TSMC1001 at 7:66-8:21. Accordingly, Fujino in combination with Saito will result in boron-boron covalent bonds. *See, also* TSMC1003 at ¶ 55. Additionally, in proceedings before the Office, where a reason to believe that a claimed limitation may be inherent in the prior art is shown, as is here, the burden shifts to the Patent Owner to provide evidence to the contrary.

Ground 7: Claims 1-13, 53-56, 58, and 59 are obvious under 35 U.S.C. § 103(a) over Fujino in view of Tian.

A. Claims 1 and 53: As set forth in GROUND 5 Fujino anticipates or renders obvious Claims 1 and 53. To the extent that Fujino may not teach nearly-amorphized layers or substrates "containing one of boron and arsenic," as recited in Claims 1 and 53, respectively, it would have been obvious to a POSITA to modify the ion implantation, as taught by Fujino, to include boron or arsenic in the implantation, as taught or suggested by Tian (*see* TSMC1008 at Abstract, 1230), such that the amorphous layers contain one of boron and arsenic, to dope Fujino's surfaces with one of boron and arsenic for the formation of a device. *See also* TSMC1003 at ¶ 58.

B. Claims 2-7, 9, 10, 12, 13, 54-56, 58, and 59: As set forth in GROUND

7(A) Fujino in combination with Tian teaches the limitations of Claims 1 and 53. Further, as set forth in GROUND 5 Fujino teaches the limitations of claims 2-7, 9, 10, 12, 13, 54-56, 58, and 59, and hence, these claims are obvious over Fujino in view of Tian.

C. Claims 7, 8, 11, and 12: Claims 7, 8, 11, and 12 are dependent on Claim 1, which as set forth in GROUNDS 5 and 7(A) Fujino alone or in combination with Tian teaches the limitations of Claim 1.

Claim 7 recites that the first and second surface are silicon surfaces "implanted with boron." It would have been obvious to a POSITA to modify the ion implantation, as taught by Fujino, to include the boron implantation, as taught or suggested by Tian (*see* TSMC1008 at Abstract, 1230), to dope Fujino's surfaces with boron for the formation of a device. *See also* TSMC1003 at ¶ 58.

Claim 8 recites that the first and second surface are silicon surfaces "implanted with arsenic." It would have been obvious to a POSITA to modify the ion implantation, as taught by Fujino, to include the arsenic implantation, as taught or suggested by Tian (*see* TSMC1008 at Abstract, 1230), to dope Fujino's surfaces with arsenic for the formation of a device. *See also* TSMC1003 at ¶ 58.

Claim 11 recites that the first and second layers "each comprise a few monolayers of boron." A POSITA would know that by controlling the dose and energy of a boron species in an ion implantation, a region having a thickness of a

few monolayers at or near the surface of the wafer would be boron rich. *See* TSMC1003 at ¶ 59. It would have been obvious to a POSITA to modify the ion implantation, as taught by Fujino, to include the boron implantation, as taught or suggested by Tian (*see* TSMC1008 at Abstract, 1230), which would result in the formation of a few monolayers of boron in the layers, to dope Fujino's surfaces boron for the formation of a device in the surfaces. *See also* TSMC1003 at ¶ 58.

Claim 12 recites that each of the first and second surfaces comprise "an amorphous boron-containing layer." It would have been obvious to a POSITA to modify the ion implantation, as taught by Fujino, to include the boron implantat, as taught or suggested by Tian (*see* TSMC1008 at Abstract, 1230), such that Fujino's surfaces comprise an amorphous boron-containing layer, to dope Fujino's surfaces with boron for the formation of a device. *See also* TSMC1003 at ¶ 58.

D. Claim 59: Claim 59 is dependent on Claim 53, which as set forth in GROUNDS 5 and 7(A) Fujino alone or in combination with Tian teaches the limitations of Claim 53. Claim 59 recites that each of the first and second surfaces comprises "a surface implanted with one of boron and arsenic."

It would have been obvious to a POSITA to modify the ion implant, as taught by Fujino, to include boron or arsenic in the implant, as taught or suggested by Tian (*see* TSMC1008 at Abstract, 1230), to dope Fujino's surfaces with one of boron and arsenic for the formation of a device. *See also* TSMC1003 at ¶ 58.

Ground 8: Claims 1-14, 53-56, and 58-60 are obvious under 35 U.S.C. § 103(a) over Fujino in view of Tian and Saito.

A. Claims 1 and 53: As set forth in GROUNDS 5 AND 7(A) Fujino anticipates or renders obvious or Fujino in combination with Tian renders obvious independent Claims 1 and 53. To the extent that Fujino alone or in combination with Tian may not teach nearly-amorphized layers or substrates "containing one of boron and arsenic," as recited in Claims 1 and 53, respectively, it would have been obvious to a POSITA to modify the implantation of silicon ions and boron or arsenic ions as described in Fujino and/or Tian to be a plasma ion implantation containing silicon ions and boron or arsenic ions as described in Saito (*see* TSMC1006 at 2:40-59; 3:30-42) in order to dope one of boron and arsenic into surfaces for the formation of a device in the surfaces. *See also* TSMC1003 at ¶ 60.

B. Claims 2-13, 54-56, 58, and 59: As set forth in GROUND 8(A) Fujino in combination with Tian and Saito teaches the limitations of Claims 1 and 53. Further, as set forth in GROUND 5 and 7 Fujino alone or in combination with Tian teaches the limitations of claims 2-13, 54-56, 58, and 59, and hence, these claims are obvious over Fujino in view of Tian and Saito.

C. Claims 6, 9, 13, and 14: Claims 6, 9, 13, and 14 are dependent on Claim 1, which as set forth in GROUNDS 5 and 8(A) Fujino alone or in combination with Tian and Saito teaches the limitations of Claim 1.

Claim 6 recites that the first and second surface are "exposed to a boron-

containing plasma." It would have been obvious to a POSITA to modify the implantation of silicon ions and boron ions as described in Fujino and/or Tian to use a plasma ion implantation containing silicon ions and boron ions as described in Saito (*see* TSMC1006 at 2:40-59; 3:30-42) in order to dope boron into surfaces for the formation of a device in the surfaces. *See also* TSMC1003 at ¶ 60.

Claim 9 recites that "at least one of boron-boron and Si covalent bonds" are formed between the first and second substrates. It would have been obvious to a POSITA to implant/expose Fujino's surfaces with boron as described by Saito (*see* TSMC1006 at 2:40-59; 3:30-42) in order to dope Fujino's surfaces for the formation of a device in the surfaces. *See, also* TSMC1003 at ¶ 60. With this plasma implant/exposure, Fujino's surfaces will have boron atoms. *See id.* at ¶ 61.

With Fujino's surfaces being exposed to a boron-containing plasma and having boron atoms thereon, Fujino's bonding process will undergo a same or similar process as described in the '133 Patent to achieve silicon covalent bonds and boron-boron bonds. Particularly, as in Fujino, the '133 Patent teaches that bonding boron treated silicon surfaces with boron atoms on the surfaces results in silicon covalent bonds and boron-boron bonds across the interface, even more at temperatures of 350-400°C. *See* TSMC1001 at 7:66-8:21. Accordingly, Fujino and Tian in combination with Saito will result in silicon covalent bonds and boron-boron bonds. *See, also* TSMC1003 at ¶ 61. Additionally, where a reason to believe

that a claimed limitation may be inherent in the prior art is shown, as is here, the burden shifts to the Patent Owner to provide evidence to the contrary.

Claim 13 recites that each of the first and second surfaces is "exposed to a boron-containing plasma." It would have been obvious to a POSITA to modify the implantation of silicon ions and boron ions as described in Fujino and/or Tian to use a plasma ion implantation containing silicon ions and boron ions as described in Saito (*see* TSMC1006 at 2:40-59; 3:30-42) in order to dope boron into surfaces for the formation of a device in the surfaces. *See also* TSMC1003 at ¶ 60.

Claim 14 recites that each of the first and second surfaces comprises a surface "exposed to an inert gas plasma." Saito further describes that argon in a plasma may be used as a carrier gas for the ion implantation. *See* TSMC1006 at 4:26-27. A plasma containing silicon with a carrier gas such as argon may be formed in Saito's plasma chamber, which may be used to form Saito's amorphous regions. *See* TSMC1006 at 4:22-32; FIG. 1. It would have been obvious to a POSITA to use a plasma, as taught by Saito, that contains silicon for an implantation, as taught by Fujino, and an inert gas such as argon for a carrier, as taught by Saito, in order to form amorphous surfaces. *See* TSMC1003 at ¶¶ 35, 62. Using argon as a carrier gas to implant silicon is a simple substitution of one known technique for another known technique to obtain the predictable result of amorphizing a substrate.

D. Claim 58: Claim 58 is dependent on Claim 53, which as set forth in GROUNDS 5 and 8(A) Fujino alone or in combination with Tian and Saito teaches the limitations of Claim 53. Claim 58 recites that each of the first and second surfaces comprises "a surface exposed to a boron-containing plasma." It would have been obvious to a POSITA to modify the implant of silicon ions and boron ions as described in Fujino and/or Tian to use a plasma ion implant containing silicon ions and boron ions as described in Saito (*see* TSMC1006 at 2:40-59; 3:30-42) in order to dope boron into surfaces for the formation of a device. *See also* TSMC1003 at ¶ 60.

E. Claim 60: Claim 60 is dependent upon Claim 59, which is dependent on Claim 53. As set forth in GROUNDS 1 and 4(A)-(B) Cheung alone or in combination with Tian and Saito teaches the limitations of Claims 53 and 59. Claim 60 recites "boron-boron covalent bonds formed between" the first and second substrates. It would have been obvious to a POSITA to implant and/or expose Fujino's surfaces with boron as described by Saito (*see* TSMC1006 at 2:40-59; 3:30-42) in order to dope Fujino's surfaces for the formation of a device in the surfaces. *See, also* TSMC1003 at ¶ 60. With this plasma implant and/or exposure, Fujino's surfaces will have boron atoms. *See id.* at ¶ 61.

With Fujino's surfaces being exposed to a boron-containing plasma and having boron atoms thereon, Fujino's bonding process will undergo a same or

similar process as described in the '133 Patent to achieve and boron-boron covalent bonds. Particularly, as in Fujino, the '133 Patent teaches that bonding boron treated silicon surfaces with boron atoms on the surfaces results in boron-boron covalent bonds across the interface, even more at temperatures of 350-400°C. *See* TSMC1001 at 7:66-8:21. Accordingly, Fujino in combination with Saito will result in boron-boron covalent bonds. *See, also* TSMC1003 at ¶ 61. Additionally, in proceedings before the Office, where a reason to believe that a claimed limitation may be inherent in the prior art is shown, as is here, the burden shifts to the Patent Owner to provide evidence to the contrary.

Ground 9: Claims 2, 5, 54, and 57 are obvious under 35 U.S.C. § 103(a) over Fujino alone or in view of Saito and/or Tian, and in further view of Cheung.

A. Claims 2 and 5: Claims 2 and 5 are dependent on Claim 1, which as set forth in GROUNDS 5, 6(A), 7(A), and 8(A) Fujino alone or in combination with Saito and/or Tian teaches the limitations of Claim 1.

Claim 2 recites a structure having a third substrate having a surface with a nearly-amorphized layer bonded to one of the first and second substrates. Fujino describes bonding the wafers having amorphized surface layers. *See* TSMC1007 at 1322. Fujino describes bonding wafers to form power devices such as power transistors, isolated vertical-DMOS circuits and control circuits on a single chip. *See id.* at 1322. Cheung describes bonding together amorphous surfaces. *See*

TSMC1005 at 8:26-29, 32-36. Cheung describes bonding wafers to form "three-dimensional packaging of integrated semiconductor devices." *See id.* at 1:19-21.

It would have been obvious to a POSITA to: form an amorphized third surface for one of the first and second substrates of Fujino; form an amorphized fourth surface region of a third substrate; and bond the third surface to the fourth surface to form a three-dimensional package as described in Cheung. *See also* TSMC1003 at ¶ 63.

Claim 5 recites that the first and second substrates "comprise respective first and second semiconductor devices." Fujino describes bonding the wafers having amorphized surface layers. *See* TSMC1007 at 1322. Fujino describes bonding wafers to form power devices such as power transistors, isolated vertical-DMOS circuits and control circuits on a single chip. *See id.* at 1322. Cheung describes bonding together amorphous surfaces of a pair of substrates. *See* TSMC1005 at 8:26-29, 32-36. Cheung discloses that the invention can be applied to "multi-layered integrated circuit devices, three-dimensional packaging of integrated semiconductor devices, photonic devices, piezoelectronic devices, microelectromechanical systems ('MEMS'), sensors, actuators, solar cells, flat panel displays (e.g., LCD, AMLCD), biological and biomedical devices, and the like." *See id.* at 1:17-24.

It would have been obvious to a POSITA to apply the devices taught by

Cheung to form a three-dimensional package as described in Cheung. *See also* TSMC1003 at ¶ 63.

B. Claims 54 and 57: Claims 54 and 57 are dependent on Claim 53, which as set forth in GROUNDS 5, 6(A), 7(A), and 8(A) Fujino alone or in combination with Saito and/or Tian teaches the limitations of Claim 53.

Claim 54 recites a third substrate of "substantially one third material amorphized only in a third surface of said third material" and that the third surface is bonded to "said fourth surface." Fujino describes bonding the wafers having amorphized surface layers. *See* TSMC1007 at 1322. Fujino describes bonding wafers to form power devices such as power transistors, isolated vertical-DMOS circuits and control circuits on a single chip. *See id.* at 1322. Cheung describes bonding together amorphous surfaces of a pair of substrates. *See* TSMC1005 at 8:26-29, 32-36. Cheung describes bonding wafers to form "three-dimensional packaging of integrated semiconductor devices." *See id.* at 1:19-21.

It would have been obvious to a POSITA to: form an amorphized third surface for one of the first and second substrates of Fujino; form an amorphized fourth surface region of a third substrate; and bond the third surface to the fourth surface to form a three-dimensional package as described in Cheung. *See also* TSMC1003 at ¶ 63. (Petitioner notes that the "said fourth surface" as recited in Claim 54 lacks a proper antecedent basis.)

Claim 57 recites that the first surface "comprises a substantially planar surface of a first silicon layer formed on said first device" and that the second surface "comprises a substantially planar surface of a second silicon layer formed on said second device." Tian teaches that the surfaces are substantially planar surfaces of a silicon layer. *See* TSMC1007 at 1322 (Fig. 1). Also, Cheung teaches that the surfaces of the amorphous silicon layers are a substantially planar. *See* TSMC1005 at 6:12-14. Further, Cheung teaches that the bonding process can be applied to "multi-layered integrated circuit devices, three-dimensional packaging of integrated semiconductor devices, photonic devices, piezoelectronic devices, microelectro-mechanical systems ('MEMS'), sensors, actuators, solar cells, flat panel displays (e.g., LCD, AMLCD), biological and biomedical devices, and the like." *See id.* at 1:17-24. It would have been obvious to a POSITA to have made amorphous layers formed on devices for various applications as taught by Cheung.

VI. CONCLUSION

For at least those reasons discussed above, Petitioner has shown a reasonable likelihood that at least one of Claims 1-14 and 53-60 is unpatentable, and *inter partes* review of U.S. Patent No. 6,563,133 B1 is respectfully requested. Petitioner authorizes any other fees to be charged to Deposit Account No. 50-1065.

Respectfully submitted,

2013-11-27 /Steven H. Slater/
Date Steven H. Slater, Reg. No. 35,361

CERTIFICATE OF SERVICE ON PATENT OWNER PURSUANT TO 37 C.F.R. § 42.105(a)

The undersigned hereby certifies that the foregoing CORRECTED PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 6,563,133 was served in its entirety by electronic service on the counsel of record for the Patent Owner at the email addresses listed below contemporaneous with the filing of the foregoing Corrected Petition on November 27, 2013:

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