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Paper 14
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LIMITED and
TSMC NORTH AMERICA CORPORATION
Petitioner

v.

ZIPTRONIX
Patent Owner

Case IPR2014-00114
Patent 6,563,133 B1

Before KEVIN F. TURNER, JAMES B. ARPIN, and JAMES A. TARTAL, *Administrative Patent Judges*.

TURNER, *Administrative Patent Judge*

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Taiwan Semiconductor Manufacturing Company, Limited and TSMC North America Corporation (collectively, "TSMC") filed a corrected petition (Paper 12, "Pet.") requesting *inter partes* review of claims 1-14 and 53-60 of U.S. Patent No. 6,563,133 B1 ("the '133 Patent"). Patent Owner, Ziptronix, Inc., timely filed mandatory notices pursuant to 37 C.F.R. § 42.8(a)(2), but did not file a preliminary response. We have jurisdiction under 35 U.S.C. § 314.

The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides:

> THRESHOLD --The Director may not authorize an inter partes review to be instituted unless the Director determines that the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.

We conclude that the information presented in the petition demonstrates that there is a reasonable likelihood that TSMC will prevail in challenging claims 1-14 and 53-60 as unpatentable under 35 U.S.C. § 103. Pursuant to 35 U.S.C. § 314, we hereby authorize an *inter partes* review to be instituted as to claims 1-14 and 53-60 of the '133 Patent.

A. Related Matters

TSMC indicates that there are no judicial or administrative matters pending related to the ’133 Patent. Pet. 1.

B. The ’133 Patent (Ex. 1001)

The ’133 Patent relates to low temperature bonding of substrates through the use of defect regions on the surface, where those regions also can be amorphized. Ex. 1001, Abstr. The treated surfaces are placed together, forming an attached pair at room temperature in ambient air. *Id*. The defect regions may be formed by plasma treating the surface or through ion implantation. *Id*. at 6:33-61.

C. Challenged Claims

Independent claims 1 and 53, as well as dependent claims 2-14 and 54-60, are challenged by TSMC in its Petition. Claim 1 is illustrative and is reproduced below:

> 1. A bonded structure, comprising:
>
> a first substrate having a first surface, a first nearly-amorphized layer containing one of boron and arsenic formed uniformly over said first surface; and
>
> a second substrate having a second surface, a second nearly-amorphized layer containing one of boron and arsenic formed uniformly over said second surface;
>
> said first surface being bonded to said second surface to form a bonded pair of substrates.

D. Prior Art Relied Upon

TSMC relies upon the following prior art references:

Cheung	US 6,534,381 B2	Mar. 18, 2003	(Ex. 1005)
Saito	US 5,561,072	Oct. 1, 1996	(Ex. 1006)

Seiji Fujino et al., *Silicon Wafer Direct Bonding through the Amorphous Layer*, 34 Japanese J. Appl. Phys. 1322 (15 October 1995) (Ex. 1007)(hereinafter "Fujino").

Shiyang Tian et al., *A Detailed Physical Model for Ion Implant Induced Damage in Silicon*, 45 (6) IEEE Transactions on Electron Devices 1226 (June 1998) (Ex. 1008)(hereinafter "Tian").

E. Alleged Grounds of Unpatentability

TSMC asserts the following grounds of unpatentability:[1]

Basis	**References**	**Claim(s)**
§ 102	Cheung	1-10, 12-14, and 53-59
§ 103	Cheung and Saito	1-14 and 53-60
§ 103	Cheung and Tian	1-14 and 53-59
§ 103	Cheung, Tian, and Saito	1-14 and 53-60

[1] TSMC asserts in their alleged grounds of unpatentability under anticipation based on Cheung or Fujino that each cited reference anticipates or renders obvious particular claims. TSMC, however, provides the necessary analysis for obviousness only with respect to claim 2 (Pet. 11), claim 10 (Pet. 15, 40), and claim 54 (Pet. 54). Accordingly, we interpret TSMC's ground for the remaining claims challenged based only on Cheung or Fujino to be limited to only 35 U.S.C. § 102.

§ 102	Fujino	1-7, 9, 10, 12, 13, 53-56, 58, and 59
§ 103	Fujino and Saito	1-14, 53-56, and 58-60
§ 103	Fujino and Tian	1-13, 53-56, 58, and 59
§ 103	Fujino, Tian, and Saito	1-14, 53-56, and 58-60
§ 103	Fujino, Tian, Saito, and Cheung	2, 5, 54, and 57

II. ANALYSIS

A. Claim Construction

As a first step in our analysis for determining whether to institute a trial, we determine the meaning of the claims. In an *inter partes* review, claim terms in an unexpired patent are given their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b). Under the broadest reasonable construction standard, claims are to be given their broadest reasonable interpretation consistent with the specification, and the claim language should be read in light of the specification, as it would be interpreted by one of ordinary skill in the art. *In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004). This means that the words of the claim are given their plain meaning unless the plain meaning is inconsistent with the specification. *In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989). In this regard, an inventor is entitled to be his or her own lexicographer of patent claim terms by providing a definition of the term in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

TSMC notes that the claim term "nearly-amorphized layer," recited in claim 1, is not discussed or defined in the specification of the '133 Patent (Pet. 7), and argues that the plain meaning of "nearly" is "with close approximation" (Pet. 8). Based on this, TSMC argues that a "nearly-amorphized layer" should be construed as "a layer that at least closely approximates an amorphous layer." *Id*. We are persuaded that this is the broadest reasonable construction in light of the specification of the claim term, based on the instant record, and apply that construction in the analysis below.

Claim 10 recites, in part, that "said first and second amorphous layers are each in the range of a few nm in thickness." TSMC notes that the specification of the '133 Patent teaches in an embodiment the formation of an amorphous layer with 1650 Å thickness, and argues that, under the broadest reasonable construction, "**a few nm in thickness**" at least encompasses 165 nm. *Id*. However, we are not persuaded that the plain meaning of "a few nm in thickness" should be interpreted to cover such a thickness. Claim 10 is a dependent claim, and we are persuaded that there is support in the specification (Ex. 1001, 6:43-44), such that a few nm need not encompass 165 nm. Given the plain and ordinary meaning of "few,"[2] we are persuaded that "a few nm in thickness" means a small number of nanometers in thickness.

[2] Merriam-Webster Dictionary defines "few" as "consisting of or amounting to only a small number." http://www.merriam-webster.com/dictionary/few (last visited Apr. 23, 2014).

B. Principles of Law

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc*., 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966).

The level of ordinary skill in the art is reflected by the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001); *In re GPAC Inc*., 57 F.3d 1573, 1579 (Fed. Cir. 1995); *In re Oelrich*, 579 F.2d 86, 91 (CCPA 1978).

C. Anticipation by Cheung

TSMC asserts that claims 1-10, 12-14, and 53-59 of the '133 Patent are anticipated under 35 U.S.C. § 102 by Cheung. Pet. 8-22. Cheung is directed to a method for fabricating multi-layered substrates, whereby a compliant layer is formed on a face of a first substrate, and is joined to a face of a second substrate having a surface non-uniformity. Ex. 1005, Abstr. Cheung details that the compliant layer can be an amorphous silicon layer that is substantially planar. *Id*. at 3:49-51; Fig. 5. We are persuaded, on the present record, that the disclosed amorphous silicon layer would be "a layer

that at least closely approximates an amorphous layer," as claimed. Pet. 9-10. In one embodiment, the second substrate also can have a compliant layer formed thereon, which is used to form joining of the substrates. Ex. 1005, 8:21-29.

TSMC also argues that Cheung discloses that its substrate may be doped or undoped, with disclosed dopants of arsenic and boron. *Id*. at 4:15-20; Pet. 9. Based on this, TSMC states that Cheung's amorphous silicon layer contains a dopant of boron or arsenic, and cites to the declaration of Dr. Blanchard in support. Pet. 9. Dr. Blanchard testifies such doping can occur during wafer formation or by ion implantation, and that amorphous layers on the surface also will contain dopants, i.e., boron or arsenic. Ex. 1003 ¶ 31. We are not persuaded, however, that the amorphous layers in Cheung must contain the dopants, as required by independent claims 1 and 53.

As discussed in Saito, the doping concentration varies based on the energy and the ions employed. Ex. 1006, 1:34-41. Unlike Saito, Cheung does not provide any conditions for such ion implantation, which Dr. Blanchard testifies may be one of the processes of formation of the doped substrates. Ex. 1003 ¶ 31. The concentration of arsenic or boron atoms can vary based on distances from the surface, as discussed in Tian. Ex. 1008, figs. 1, 2, 4; 1231-1233. Without more disclosure in Cheung, we are persuaded that, although it may be likely that the amorphized surfaces of the substrates in Cheung contain boron or arsenic, it has not been shown that Cheung's bonded substrates *must* contain such layers. "'Inherency . . . may not be established by probabilities or possibilities. The mere fact that a

certain thing may result from a given set of circumstances is not sufficient.'" *Bettcher Indus., Inc. v. Bunzl USA, Inc.*, 661 F.3d 629, 639-40 (Fed. Cir. 2011) (quoting *In re Oelrich*, 666 F.2d 578, 581 (CCPA 1981)). As such, we are not persuaded that Cheung anticipates the subject matter of claims 1 and 53, or claims dependent thereon.

For the foregoing reasons, we are not persuaded that there is a reasonable likelihood that TSMC would prevail on its assertion that claims 1-10, 12-14, and 53-59 of the '133 Patent are anticipated by Cheung.

D. Obviousness over Cheung and Saito

TSMC asserts that claims 1-14 and 53-60 of the '133 Patent are obvious under 35 U.S.C. § 103 over Cheung and Saito. Pet. 8-22. As discussed above, we are not persuaded that Cheung anticipates the subject matter of claims 1 and 53, but we are persuaded that it is likely that, in view of the teachings of Saito, the amorphized surfaces of Cheung may be modified to contain boron or arsenic.

TSMC acknowledges that "Cheung may not teach . . . substrates 'containing one of boron and arsenic,' as recited in Claims 1 and 53." Pet. 22. TSMC argues, however, that it would have been obvious to a person of ordinary skill in the art to implant Cheung's substrates with boron or arsenic using a plasma containing ions as taught by Saito. *Id*. We agree that Saito discloses the implantation of ions of an impurity, including boron and arsenic, into a surface region of a semiconductor substrate through the use of a plasma. Ex 1006, 2:46-52. We also are persuaded, on the present record, that one of ordinary skill in the art would have reason to dope the substrate

surfaces of Cheung, using the methods of Saito, prior to the creation of the amorphous layers and the bonding of the substrates, so that the amorphous layers contain one of arsenic and boron. Based on this, and the discussion of Cheung provided above, we are persuaded that TSMC has shown a reasonable likelihood it would prevail in showing that Cheung, in combination with Saito, renders the subject matter of claims 1 and 53 obvious.

With respect to claims 2-5, 10, and 54-57, TSMC argues that Cheung discloses that the invention can be applied for multi-layered integrated circuit devices, and that it would have been obvious to form a bonded structure with three substrates, per the disclosed methods. Pet. 11, 18-19; Ex. 1005, 1:17-21. TSMC also argues that Cheung discloses that its substrates can be silicon or compound semiconductors, and that Cheung discloses that its bonding can be accomplished to achieve multilayered integrated circuit devices. Pet. 12, 19-21; Ex. 1005, 4:10-15, 25-27. TSMC also argues that Cheung discloses that the amorphous silicon layer can have a thickness ranging from about 10 nm to about 500 nm. Pet. 14-15; Ex. 1005, 6:10-13. TSMC has shown, based on the further disclosures of Cheung, that there is a reasonable likelihood it would prevail in showing the subject matter of claims 2-5, 10, and 54-57 would have been obvious over Cheung and Saito.

With respect to claims 6-8, 12-14, 58, and 59, TSMC argues that it would have been obvious to expose the substrates of Cheung to a plasma containing ions of silicon and boron or arsenic, as well as implant boron into the substrates by the same method, as taught by Saito. Pet. 23, 27; Ex. 1006,

2:40-59; 3:30-42. With respect to claims 9 and 60, TSMC argues that with Cheung's substrate surface having boron atoms, the bonding process between the substrates would undergo the same or a similar process, as described in the '133 Patent, resulting in silicon covalent bonds and boron-boron bonds across the interface. Pet. 24, 27-28. With respect to claim 11, TSMC argues that a person of ordinary skill in the art would recognize that plasma implantations of Saito would lead to the formation of a few monolayers of boron on the surface of the substrates. *Id*. at 25. Based on the arguments of TSMC, we are persuaded on the present record that TSMC has demonstrated a reasonable likelihood that it would prevail in showing that Cheung, in combination with Saito, renders the subject matter of claims 6-9, 11-14, and 58-60 obvious.

For the foregoing reasons, we are persuaded that there is a reasonable likelihood that TSMC will prevail in demonstrating that claims 1-14 and 53-60 of the '133 Patent are unpatentable over the combination of Cheung and Saito.

E. Anticipation by Fujino

TSMC asserts that claims 1-7, 9, 10, 12, 13, 53-56, 58, and 59 of the '133 Patent are anticipated by Fujino. Pet. 36-44. Fujino discloses the direct bonding of silicon wafers through the use of amorphous layers. Ex. 1007, Abstr. Fujino details that silicon ions are implanted to make the silicon wafer surface amorphous, and that those surfaces are used to bond the wafers together. *Id*. at 1322. We are persuaded that, on the present record, the disclosed amorphous silicon layer would be "a layer that at least

closely approximates an amorphous layer," as claimed. TSMC argues that Fujino discloses that a native oxide film is eliminated from the surfaces of the wafers, "leaving the boron-doped silicon as the surface." Pet. 37. Although TSMC is correct that Fujino discloses the use of boron-doped, CZ-grown silicon wafers (Pet. 36), TSMC identifies no express or inherent disclosure in Fujino that the formed *amorphized* surfaces contain boron, or some other dopant.

Similar to the analysis of the ground alleging anticipation by Cheung above, we are persuaded that Fujino also fails to detail that the *amorphous* silicon wafer surface must contain the dopants found in the grown silicon wafers. Thus, although we are persuaded that it may be likely that the amorphized surfaces of Fujino's substrate surfaces contain boron or arsenic, it is not certain that Fujino's bonding of substrates *must* include amorphous layers containing boron or arsenic. As such, we are not persuaded that Fujino anticipates the subject matter of claims 1 and 53, or claims dependent thereon.

For the foregoing reasons, we are not persuaded that there is a reasonable likelihood that TSMC would prevail in demonstrating that claims 1-7, 9, 10, 12, 13, 53-56, 58, and 59 of the '133 Patent are anticipated by Fujino.

F. Obviousness over Fujino and Saito

TSMC asserts that claims 1-14, 53-56, and 58-60 of the '133 Patent are obvious under 35 U.S.C. § 103 over Fujino and Saito. Pet. 44-50. As discussed above, we are not persuaded that Fujino anticipates the subject

matter of claims 1 and 53, but we are persuaded that it is likely that the amorphized surfaces of Fujino contain boron or arsenic.

TSMC acknowledges that "Fujino may not teach . . . substrates 'containing one of boron and arsenic,' as recited in Claims 1 and 53." Pet. 44. TSMC argues, however, that it would have been obvious to a person of ordinary skill in the art to implant Fujino's substrates with boron or arsenic using a plasma containing ions as taught by Saito. *Id*. at 44-45. We agree that Saito discloses the implantation of ions of an impurity, including boron and arsenic, into a surface region of a semiconductor substrate through the use of a plasma. Ex 1006, 2:46-52. We also are persuaded, on the present record, that one of ordinary skill in the art would have reason to dope the substrate surfaces of Fujino, using the methods of Saito, prior to the creation of the amorphous layers and the bonding of the substrates, so that the amorphous layers contain one of arsenic and boron. Based on this, and the discussion of Fujino provided above, we are persuaded that Petitioner has shown a reasonable likelihood that it would prevail in demonstrating that Fujino, in combination with Saito, renders the subject matter of claims 1 and 53 obvious.

With respect to claims 2, 3, 54, and 55, TSMC argues that the duplication of the parts does not produce any new or unexpected results, and that it would have been obvious to form a bonded structure with three substrates, per the methods disclosed in Fujino. Pet. 37-38, 43. With respect to claims 4, 5, and 56, TSMC also argues that Fujino discloses that its substrates can be silicon, and that Fujino discloses that its bonding can be applied to isolated vertical-DMOS and control circuits on a single chip. Pet.

38, 43; Ex. 1007, 1322. With respect to claim 10, TSMC also argues that Fujino discloses that the thickness of the amorphous silicon layer can be varied by adjusting the acceleration energy, and that determining a proper range could be determined by routine experimentation. Pet. 40; Ex. 1007, 1322. TSMC has shown, based on the further disclosures of Fujino, that there is a reasonable likelihood it would prevail in showing the subject matter of claims 2-5, 10, and 54-56 would have been obvious over Fujino and Saito.

With respect to claims 6-8, 12-14, 58, and 59, TSMC argues that it would have been obvious to expose the substrates of Fujino to a plasma containing ions of silicon and boron or arsenic, as well as implant boron into the substrates by the same method, as taught by Saito. Pet. 45-46, 47-49; Ex. 1006, 2:40-59; 3:30-42. With respect to claims 9 and 60, TSMC argues that with Fujino's substrate surface having boron atoms, the bonding process between the substrates would undergo a same or similar process as described in the '133 Patent, resulting in silicon covalent bonds and boron-boron bonds across the interface. Pet. 46-47, 49-50. With respect to claim 11, TSMC argues that a person of ordinary skill in the art would recognize that plasma implantations of Saito would lead to the formation of a few monolayers of boron on the surface of the substrates. *Id*. at 47. Based on the arguments of TSMC, we are persuaded that TSMC has demonstrated a reasonable likelihood it would prevail in showing that Fujino, in combination with Saito, renders the subject matter of claims 6-9, 11-14, and 58-60 obvious.

For the foregoing reasons, we are persuaded that there is a reasonable likelihood that TSMC will prevail in demonstrating that claims 1-14, 53-56, and 58-60 of the '133 Patent are unpatentable over the combination of Fujino and Saito.

G. Remaining Grounds of Unpatentability

TSMC also contends that claims 1-14 and 53-60 also are unpatentable under 35 U.S.C. § 103 based on additional combinations of Cheung, Fujino, Tian, and/or Saito, as well as over Cheung or Fujino, taken alone. Pet. 11, 15, 28-36, 40, 44-52, 54, 57-60. Nevertheless, TSMC does not argue that any of these grounds is superior to the grounds upon which we are instituting *inter partes* review and, therefore, we conclude that those grounds of unpatentability are redundant to the grounds of unpatentability on which we initiate an *inter parties* review. We note that the proper focus of a redundancy designation is on whether TSMC articulates a meaningful distinction in terms of relative strengths and weaknesses with respect to the application of the prior art disclosures to one or more claim limitations. *See Liberty Mutual Ins. Co. v. Progressive Casualty Inc. Co.*, CBM2012-00003, Paper 7, 2 (PTAB, Oct. 25, 2012). In this case, the petition does not create any distinctions between grounds. Simply proposing different grounds of unpatentability based on different methods and systems does not distinguish meaningfully the applied prior art references. Accordingly, we exercise our discretion and do not authorize an *inter partes* review on the remaining grounds of unpatentability asserted by TSMC against claims 1-14 and 53-60 of the '133 Patent. *See* 37 C.F.R. § 42.108(a).

III. CONCLUSION

For the foregoing reasons, we determine that the information presented in the petition shows that there is a reasonable likelihood that TSMC would prevail in challenging claims 1-14 and 53-60 of the '133 Patent. Accordingly, the petition is *granted* on the grounds as discussed above.

At this stage in the proceeding, no final determination with respect to the patentability of the challenged claims has been made.

IV. ORDER

For the foregoing reasons, it is

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review is hereby instituted as to claims 1-14 and 53-60 of the '133 Patent for the following grounds of unpatentability:

A. Claims 1-14 and 53-60 as unpatentable under 35 U.S.C. § 103(a) over Cheung and Saito; and

B. Claims 1-14, 53-56, and 58-60 as unpatentable under 35 U.S.C. § 103(a) over Fujino and Saito.

FURTHER ORDERED that no other grounds of unpatentability are authorized for this *inter partes* review;

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial. The trial will commence on the entry date of this decision.

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