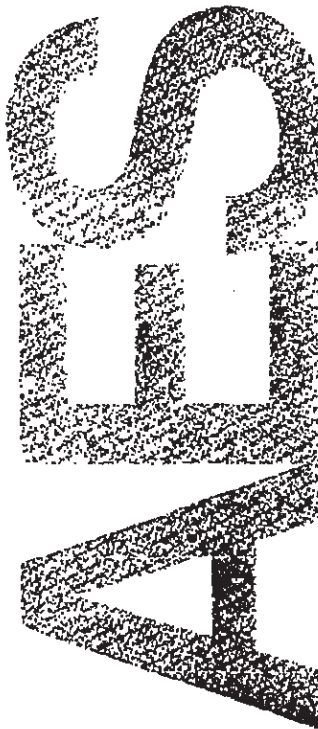
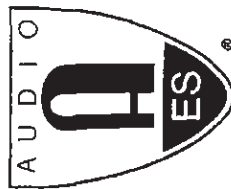


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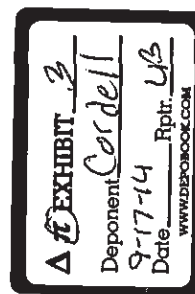


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A MOSFET Power Amplifier with Error Correction

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0. ABSTRACT

Power MOSFETs are emerging as the device of choice for high-quality power amplifiers because of their speed, reduced need for protection and falling cost. A low-distortion power amplifier design is presented which includes output stage error correction to reduce the effect of transconductance droop in the crossover region and thus allow operation at more efficient bias levels.

1. INTRODUCTION

The rapid evolution of power MOSFETs during the last few years has brought them to the point where they are now very attractive for use in audio amplifier power output stages. Important improvements which have been made include increased voltage, current and dissipation ratings, reduced "on" resistance, availability of complementary pairs and greatly reduced cost. Although a 75-watt MOSFET is still more expensive than a 150-watt bipolar transistor, the premium is small when considered relative to total amplifier cost and improved performance.

The purpose of this paper is to demonstrate the level of performance achievable with current technology and illustrate practical circuit techniques for achieving this performance.

Power MOSFETs have several fundamental advantages over bipolar power transistors, most notably speed and freedom from secondary breakdown. The latter provides higher "usable" power dissipation, improved reliability, and freedom from safe-area limiter circuits which can misbehave and cause audible degradation. MOSFETs also have some disadvantages in comparison with bipolar transistors. These include higher turn-on voltage drive requirements and smaller transconductance at low current levels. The former tends to contradict generalizations which have been made to the effect that drive circuits for power MOSFETs are less expensive, at least for the reliable source-follower configuration. The latter results in transconductance droop in the crossover region if bias currents are not fairly high. Such transconductance droop can result in crossover distortion.

In this paper we will present a high-performance amplifier design which utilizes the advantages of the power MOSFET while dealing with the drawbacks of the device. Although not taken to an extreme, the underlying philosophy of the design is that small-signal silicon is inexpensive, i.e., that the overwhelming portion of expense in a power amplifier is in items like the power transformer, filter capacitors, power transistors, heat sinks, chassis and related hardware. Thus, in order to take full advantage of the performance achievable with the MOSFET output stage, a very high quality front-end and driver are provided. The driver, operating from regulated boosted supplies, is capable of providing high voltage and current swings to the power MOSFETs with good headroom. Output stage transconductance droop is dealt with by employing a simple but very effective output stage error correction technique proposed by Hawksford.¹ The resulting design achieves a 20-kHz THD figure of less than 0.0015 percent at an idle bias of only 150 mA.

2. MOSFET VS. BIPOLAR OUTPUT STAGES

Design of MOSFET power amplifiers is quite straightforward and conventional as long as differences between MOSFETs and bipolar transistors are understood. Figure 1 shows the drain and gate transfer characteristics typical of the devices used in this project (International Rectifier types IRF-132 and IRF-9130).² The important point to see here is that

these enhancement devices require about 3 volts of forward gate bias to begin to turn on (e.g., gate threshold voltage, V_t) and may require as much as 8 volts to conduct high currents (10 amperes). While the required bias voltage is thus higher than for bipolar transistors, it can still be generated by the traditional V_{BE} multiplier circuit. However, because the MOSFET's negative temperature coefficient of transconductance tends to provide inherent thermal bias stability, the V_{BE} multiplier transistor or associated reference diode should not be mounted on the heat sink.

If the popular source-follower output stage configuration is used, the substantial gate drive voltage required for high currents means that the driver stage should be provided with a "boosted" power supply voltage greater than that of the main high-current supply in order to take full advantage of the voltage swing available from the latter. The current requirements for the boosted supply are small, and it can be regulated at little additional expense, thus reducing hum, crosstalk and modulation distortion. Several high-quality bipolar power amplifiers also use boosted driver supplies, some regulated.

While bipolar transistors are regularly placed in parallel with small individual emitter ballast resistors, the paralleling issue is not as straightforward for power MOSFETs, at least in linear applications. It has been said that the negative temperature coefficients of transconductance and "on" resistance of MOSFETs act to suppress current hogging by one transistor, thus permitting easy paralleling of MOSFETs without ballast resistors. This appears to be true for hard-switching applications where the paralleled devices are all fully turned-on together (i.e., channels fully enhanced by forward gate voltage) so that current and dissipation imbalances are only a result of mismatched on resistance. However, the issue is more complex for linear, and especially low-distortion, applications because the operating region of interest is not the fully turned-on region, but rather the linear region wherein drain current at a specified gate voltage is important. Specifically, recognizing that the gate threshold voltage specification for these devices is 2-4 volts, an examination of the gate transfer characteristics of Figure 1 indicates that a very serious current imbalance can exist unless gate threshold voltages among paralleled devices are reasonably matched. It is also apparent that reasonable temperature differentials will not adequately reduce the imbalance. Because of the size of the worst-case threshold voltage differentials possible, source ballast resistors are not a reasonable approach to achieving balance. It thus appears that for high quality audio applications where paralleled devices are necessary, both threshold voltage and transconductance of paralleled devices should be matched. Threshold matching that guarantees that all devices are on to some extent in the quiescent bias state, and transconductance matching to within 20% is probably adequate.

Modern complementary MOSFETs, with maximum "on" resistances of only about 0.3 ohms, are just about as efficient as bipolar transistors in terms of voltage dropped from supply rail to load in output stages. However, they typically require a higher operating current to achieve a given transconductance. This characteristic is illustrated in Figure 2. The device transconductance in a source-follower or emitter-follower output stage is important because it determines the small signal voltage drop through the stage as a function of current. This is especially important in Class-AB stages where it is desirable that the sum of the effective transconductances of both halves be high and be constant with current so as to avoid crossover distortion. It can be seen from Figure 2 that approaching this condition with power MOSFETs requires fairly substantial bias current (as a rough starting point, that current where transconductance is one-half its high-current asymptotic value), on the order of a few hundred milliamperes.

In contrast, bipolar power transistors are typically biased at a much lower current, but this is not entirely advantageous. A typical bipolar output stage will often be biased approximately where the dynamic emitter resistance of the output devices ($1/g_m$) at crossover is equal to the associated ballast resistance as a compromise in achieving approximately constant total output stage transconductance as a function of current. This is done because both halves are "on" and contribute transconductance in the crossover region while only one half

contributes transconductance at currents well outside the crossover region. This usually results in bias currents of less than 100 mA per output transistor, sometimes as low as 20 mA. This small amount of bias current compared to several amperes of signal current being handled can sometimes result in unexpected temporary bias inadequacy, resulting in crossover distortion, because a small change in circuit parameters (about 50 mV) can cause the bias current to go almost to zero. This can happen as a result of the time delay in the intentional thermal feedback loop created by placing the bias generator transistor on the heat sink. After a high dissipation interval ends, the amplifier may find itself temporarily underbiased because the power transistor junctions cooled down faster than the bias transistor. Bipolar output stages can be operated in an overbiased mode, but the penalty can be dangerously reduced thermal stability if larger heat sinks are not used, or increased crossover distortion if larger ballast resistors are used. No such feedback loop is necessary for thermal stability of MOSFET output stages and their higher bias is less likely to disappear under transient thermal conditions. Compared to bipolar designs, Class-AB MOSFET power output stages also tend to have a wider Class-A region of operation and a smoother transition to the Class-B region of operation.

Although power MOSFETs require virtually no drive current at low frequencies, their substantial input capacitance means that drive circuits with forward and reverse drive capabilities similar to those employed with bipolar transistors should be used for wideband, high slew-rate circuits for demanding audio applications. Although the gate-source capacitance can be on the order of 1000 pF, this capacitance is effectively "bootstrapped" in a source follower output stage, typically reducing its effect by about an order of magnitude. The smaller gate-drain capacitance, about 100 pF, is also present. A 100 V/ μ s slope with an effective capacitance of 200 pF thus requires a 20 mA current capability from each driver.

Power MOSFETs tend to be inherently faster than bipolars, partly because there are no minority carrier effects. Their speed is primarily limited by the ability of the drive circuitry to charge the internal gate electrode capacitance. The wider bandwidth, reduced excess phase and reduced variation of device speed with voltage and current tend to allow greater high-frequency negative feedback with greater stability. The higher switching speed also tends to reduce dynamic crossover distortion. However, power MOSFETs do have a tendency to very high frequency parasitic oscillations in real-world circuits. This appears to be a result of the natural high speed of the device combined with the substantial drain-source capacitance (300 pF) typical of these devices, making formation of a Colpitts oscillator easy if inductance is present in the gate circuit. This often necessitates the use of a small resistor in series with the gate. In combination with the device input capacitance, this resistor (typically about 100 ohms) can create an additional pole which tends to reduce the high-frequency improvement over bipolar transistors. The MOSFET's higher switching speed also greatly reduces the flow of Class-AB common-mode current at high frequencies which poses such a destructive threat to many bipolar designs.

Perhaps one of the most important advantages of power MOSFETs for audio use is their freedom from secondary breakdown which results in a large safe operating area (SOA). A highly simplified explanation of secondary breakdown in bipolar transistors is that it results from localized current hogging which in turn results from localized thermal "hot spots." Transistor current at a given base-emitter voltage has a very strong positive temperature coefficient. Thus, a "hot spot" carries more current and gets even hotter as a result. This regenerative process, once started, can be very rapid and unforgiving. It can persist even after the external voltage and current conditions re-enter the safe operating area, leading to destruction. The relationships in a power MOSFET are in contrast *degenerative* in nature because hotter regions exhibit reduced transconductance and thus tend to conduct less of the total current. This tends to equalize the temperature across the chip. The safe area of a MOSFET is thus primarily governed by simple thermal considerations of how much energy (product of power and time) is required to raise the temperature of the hottest point on the chip (which will not be much different than the average temperature of the whole chip) to a

dangerous point.

Figure 3 shows a comparison of safe operating area for a power MOSFET and a typical bipolar power transistor. Notice that there are no steep secondary breakdown SOA slopes at high voltages for the MOSFET - it is essentially limited by simple power dissipation over its full voltage range. This is also true for short-term dissipation well in excess of rated continuous dissipation, where thermal time constants govern the allowable excess dissipation. For example, a 25-ampere peak with 100 volts across the MOSFET can be handled for 10 microseconds. Figure 3 illustrates that "usable" dissipation (SOA at higher voltages) for a MOSFET may be equal to that of a bipolar power transistor of substantially higher rated power dissipation. Safe operating area at high voltages is particularly important when difficult reactive loads are being driven. In many power amplifiers the use of multiple paralleled output devices is for reasons of increased safe operating area rather than simple thermal considerations. Finally, freedom from secondary breakdown means freedom from complex safe-area limiter circuits, some of which are notorious for their misbehavior.

Figure 4 illustrates a simple 50-watt MOSFET power amplifier design. It is notably similar to what a simple bipolar power amplifier design would look like. Transistors Q1 and Q2 comprise the input differential amplifier whose output is converted to a single-ended current by current mirror Q3, 4. This current feeds the common-emitter pre-driver Q5 which is provided with a constant-current load. Capacitor C1 provides Miller-effect feedback compensation and establishes a stable gain-crossover frequency of approximately 2 MHz. Transistor Q6 is connected in a conventional V_{be} multiplier circuit to provide adjustable bias (nominally about 8V) for the output stage. Emitter-follower drivers Q7 and Q8 provide a low-impedance drive for the gates of power MOSFETs Q9 and Q10. The drivers isolate the high-impedance pre-driver collector circuit from the nonlinear input capacitance of the MOSFETs and provide adequate charge and discharge current for the MOSFET gate circuits. The boosted supplies for all circuits prior to the output stage enable the drive circuitry to provide adequate gate voltage to fully turn-on the MOSFETs while maintaining margin against saturation. Zener diodes D1-D4 protect the MOSFETs from excessive gate-source voltages of either polarity.

3. INPUT AND DRIVER CIRCUITS

As would be the case with a bipolar design as well, many improvements can be made to the "front-end" of the simplified amplifier of Figure 4 in order to provide higher performance and take full advantage of the capability of the MOSFET output stage. Although substantially adding to the complexity of the schematic in appearance, such improvements primarily involve only small-signal, low-voltage transistors and inexpensive passive components, and thus contribute only a small percentage increase to total amplifier cost.

The front-end for the amplifier to be discussed here is shown in in Figure 5. The input stage is a differential JFET-bipolar cascode with a constant current bias supply. The cascode allows the use of a low-noise dual JFET, achieving a referred input noise of less than $6 \text{ nV}/\sqrt{\text{Hz}}$. It also provides good common-mode and power supply rejection, necessary because negative feedback is not very effective in reducing power supply and common-mode impairments introduced at the input stage. The degenerated JFET input stage can handle fairly large open-loop input signals with relatively low distortion, making the amplifier relatively immune to transient intermodulation distortion (TIM) and RFI effects.

The input stage is loaded by current sources (Q6, Q7) to provide high open-loop gain at low frequencies. Emitter followers Q8 and Q9 isolate the input stage from second-stage (pre-driver) loading effects and produce a combined common-mode feedback to properly bias Q6 and Q7. This also provides additional common-mode rejection by reducing the common-mode impedance seen by the collectors of the input stage. Limiter diodes D2 and D3 prevent excessive signal swings at the collectors of Q4 and Q5 when the amplifier is clipping.

The complementary pre-driver stage consists of a differential cascode (Q10-13) loaded with a Darlington-cascode current mirror (Q14-17) to provide a single-ended drive for the output stage. The cascode achieves high speed by eliminating Miller effect and allowing the use of fast low voltage transistors in the common-emitter differential amplifier. Elimination of Miller effect is also important in reducing high-frequency distortion resulting from nonlinear collector-base junction capacitance. The cascode configuration also improves low-frequency linearity and power supply rejection by reducing Early effect. The complementary pre-driver structure, made possible by the current mirror, greatly reduces second-order distortion.

Transistors Q18 and Q19 provide regulated bias for the cascode bases and emitter-follower collectors. Adequate current is available so that these voltages remain stable even under clipping conditions. Diodes D4-D7 prevent the cascodes from saturating when the amplifier clips. Zener diode D8 provides for two identical drive signals offset by 22 volts to allow for biasing and error correction in the output stage.

Overall negative feedback connections and frequency compensation are also shown in Figure 5. R11 and R12 set the closed-loop gain at approximately 20. The resistance of this divider was chosen to be fairly low to avoid noise and maintain good high-frequency characteristics. As a result, current flow and dissipation is not insignificant (100 mW in R12 at 50-watt operating level). To avoid thermally-induced distortion at low frequencies, these resistors should be over-sized metal-film types, 1-watt and 2-watt respectively.

Feedback compensation is provided by C4 and R13 which implement rolloff feedback from the output of the pre-driver to the inverting amplifier input, establishing a stable gain crossover frequency of about 2 MHz. Providing compensation by feedback to the input stage tends to allow improved slew rate and reduced power supply coupling; the latter because both ends of the network are ground-referenced (in contrast to the Miller-effect compensation of Figure 4). Elements C3 and R14 act to stabilize the loop formed by C4 and R13. This front-end design enables the amplifier to achieve a slew rate in excess of 300 V/ μ s.

4. OUTPUT STAGE AND ERROR CORRECTION

In virtually any well-designed power amplifier the output stage ultimately limits performance. It is here where both high voltages and large current swings are present, necessitating larger, more rugged devices which tend to be slower and less linear over their required operating range. The performance-limiting nature of the output stage is especially true in Class-B and -AB designs, where the signals being handled by each "half" have highly nonlinear "half-wave-rectified" waveforms and where crossover distortion is easily generated. In contrast, it is not difficult or prohibitively expensive to design front-end circuitry of exceptional linearity.

Overall negative feedback greatly improves amplifier performance (including dynamic distortions such as transient intermodulation distortion), but it becomes progressively less effective as the frequency or speed of the errors being corrected increases. High-frequency crossover notch distortion is a good example. For this reason, several high-performance amplifier designs now employ feedforward error correction in addition to conventional negative feedback. However, some of these designs can be complex and expensive. The philosophy of this design is based on the observation that only the output stage needs extra error correction and that such local error correction can be less complex and more effective.

While the power MOSFET has many advantages, it was pointed out in Section 2 that the lower transconductance of the MOSFET will result in considerable crossover distortion unless rather high bias currents are chosen. Figure 6 illustrates this effect by showing the individual and summed transconductances of both halves of a Class-AB MOSFET output stage as a function of net output current. At a bias current of 150 mA and a load of 8 ohms, this transconductance variation can result in open-loop output stage harmonic distortion on the order of one percent, as pictured in Figures 7a and 7b. Mismatches in the transconductance

characteristics of the top and bottom output devices also contribute to the distortion of Figure 7. Again, while bipolar transistor transconductance is high enough and consistent enough that it is relatively unimportant in an emitter follower stage, MOSFET transconductance is smaller and less consistent, making it a significant parameter in source-follower stages.

Figure 8 illustrates an error correction technique described by Hawksford which is well-suited to this application.¹ Here the output stage, being a source follower, is modeled as having exactly unity gain with an error voltage $e(x)$ added. This error represents any departure from unity gain, whether it is a linear departure due to less than unity gain, a distortion due to transconductance nonlinearity, or injected errors like power supply ripple. A differential amplifier, represented by summer S2, merely subtracts the output from the input of the power stage to arrive at $e(x)$. This error signal is then added to the input of the power stage by summer S1 to provide that distorted input which is required for an undistorted output. Note that this is an error cancellation technique like feedforward as opposed to an error reduction technique like negative feedback. This technique is in a sense like the dual of feedforward. It is less expensive because the point of summation is a low-power internal amplifier node. It is less critical of component tolerances and frequency response matching because less circuitry is enclosed and that circuitry is simple. Feedforward tends to become less effective at very high frequencies because the required phase and amplitude matching for error cancellation becomes progressively more difficult to maintain. The technique of Figure 8 also tends to become less effective at very high frequencies because, being a feedback loop (albeit not a traditional negative feedback loop), it requires some amount of compensation for stability, detracting from the phase and amplitude matching.

A schematic of the MOSFET power amplifier's output stage and error correction circuit is shown in Figure 9. The error correction circuit is a slightly modified version of one illustrated in Reference 1. Emitter followers Q20 and Q21 isolate the high-impedance pre-driver output nodes from the output stage and provide a low-impedance signal for the error correction summation process. Double emitter followers Q24, Q26 and Q25, Q27 provide a high-current drive capability for the MOSFET gates and isolate the error correction summing nodes from the MOSFET gate loads. Note that Q24 and Q25 can be fast, inexpensive small-signal transistors. Transistors Q22 and Q23 and resistors R38-R45 comprise the differential amplifier for summer S2 of Figure 8. The output current of these transistors is summed with the input signal (summer S1 of Figure 8) by means of R34 and R35. For error correction, the top and bottom halves (Q22, Q23) work independently to produce identical correction signals. Input signals offset by ± 11 volts, as supplied by the pre-driver circuit, provide d.c. operating voltage for these circuits. These offset voltages must be adequate to allow for the maximum bias plus V_{GS} signal swing required by the MOSFETs. Transistors Q22 and Q23, in conjunction with R32 and R33, control the d.c. voltage drop across R34 and R35. They thus set the bias for the MOSFETs by means of a V_{be} - referenced feedback loop which also includes Q24, Q25, Q26 and Q27. Resistors R38 and R39 control the loop gain of the bias loops and improve stability. Overall frequency compensation of the error correction and bias loops is provided by R36, R37, C6, C7 and C10.

Figures 7c and 7d show open-loop distortion of the output stage with error correction to be less than 0.1%, illustrating an improvement of better than an order of magnitude, even at 20 kHz. This was achieved with 5% tolerance resistors. While use of closer-tolerance resistors would improve the correction at lower frequencies, where it is unnecessary, their use would make a smaller improvement at 20 kHz because performance there is beginning to be limited by the speed of the error correction loop. Sensitivity of 20-kHz THD to tolerance in the error correction circuit has been measured to be approximately 0.0002% per percent in the closed-loop amplifier. For ultimate performance, a pot can be placed between the junctions of R38, R39 and R44, R45.

The output stage is completed by C8, C9 and R50-53 for control of parasitic oscillations and D11-D14 for protection of the MOSFET gates from excessive drive voltages.

As mentioned in Section 2, power MOSFETs are considerably more prone to high-frequency parasitic oscillations than bipolar power transistors because of their inherent high-speed nature and because of their substantial drain-source capacitance, making it easy to form an efficient Colpitts oscillator structure with inductance in the gate circuit. The amount of series gate resistance required for suppression of parasitic oscillations grows in proportion to the amount of inductance in the gate circuit. For high-speed output stage operation it is therefore important to minimize this inductance. Although not employed in Figure 9, this can be done especially well by shielding the gate leads back to the driver transistors, grounding the shield to the local bypass ground at each end. Then only a 10-ohm series resistor at the driver end and a ferrite bead at the gate end are necessary.

5. PERFORMANCE

This amplifier employs substantial amounts of negative feedback (40 dB at 20 kHz), and 20-kHz total harmonic distortion (THD) was the primary performance metric used in the design process. In recent years several new forms of distortion have been described, sometimes in the belief that they were caused by large amounts of negative feedback and that traditional measures of distortion (e.g., harmonic and intermodulation) would be ineffective in detecting them. Some of these beliefs have been shown to be unfounded.⁴⁻¹⁰ Nevertheless, it was decided to include some of these newer measures of distortion in the performance evaluation.

In spite of the error correction, which improves performance by more than an order of magnitude, transconductance variation in the output stage is still the dominant source of distortion in this amplifier. For this reason, output stage bias current continues to influence performance and tradeoffs can be made. The measurements presented here were made at a bias current of 150 mA, resulting in a quiescent output stage power dissipation of 11 watts for the 50-watt amplifier. It should also be noted that the transconductance characteristics of the N- and P- channel output devices were not matched.

A word about measurement technique is in order. In many cases the distortions being measured were below those levels measurable by conventional equipment and techniques. In order to add dynamic range to that provided by the equipment employed, a distortion magnifier circuit was utilized. This circuit scales the output level of the noninverting amplifier under test down to that of the input, subtracts the two, re-introduces 11 percent of the scaled-down amplifier output signal, and finally multiplies the result by 9 for presentation to the measuring equipment. The net effect is to provide unity gain for the fundamental and a gain of ten to distortion products generated by the amplifier under test. Amplitude and phase balance adjustments were incorporated into the output signal path prior to the subtraction to achieve a fundamental null of greater than 60 dB to frequencies beyond 20 kHz. The excellent noise and distortion performance of the 5534-type operational amplifiers employed make this approach effective. For example, a sensitive THD analyzer¹¹ with a 20-kHz measurement floor of about 0.001 percent was employed in combination with this distortion magnifier to achieve a residual of about 0.0003 percent at 20 kHz, primarily limited by noise of the power amplifier under test. The distortion output of the analyzer was then observed with both an oscilloscope and a spectrum analyzer. The latter further improves the measurement floor in most cases. Most of the other distortion tests employed a similar arrangement. Due to an oscilloscope calibration error, all vertical deflections in the photographs are 6.4 percent low.

Figures 10 and 11 show total harmonic distortion as a function of frequency and power. Dashed portions of the curves indicate that distortion is below the residual of the measuring system. Figure 12 shows the appearance of the 20-kHz full-power harmonic distortion products without and with output stage error correction. Figure 13 illustrates a virtually unmeasurable level of SMPTE* intermodulation distortion (60 & 6000 Hz, 4:1).

Dynamic intermodulation distortion (DIM), a test for measurement of transient intermodulation distortion (TIM), is shown in Figure 14.¹² In this test a 3.18-kHz squarewave and a 15-kHz sine wave are mixed 4:1 and passed through the amplifier. A spectrum analyzer is used to measure the in-band intermodulation components. Performance is shown for both 30-kHz and 100-kHz first-order low-pass filtering of the squarewave source (DIM-30 and DIM-100). As predicted by the good 20-kHz THD performance and high slew rate of this amplifier, both DIM-30 and DIM-100 distortion levels are very low; in fact, the former is unmeasurable.

Interface intermodulation distortion (IIM)⁹ is measured by applying 1000 Hz to the amplifier under test and 60 Hz to a test amplifier, each of which drives opposite ends of an 8-ohm load resistor. A spectrum analyzer is then used to measure distortion products at the output of the amplifier under test. Both amplifiers are operated at half the rated power of the amplifier under test and distortion products are referred to the 1-kHz level at the output of the amplifier under test. For this test the spectrum analyzer was preceded by a modified version of the distortion magnifier to produce a magnification of 100. IIM was unmeasurable, at less than 0.0001 percent.

Phase intermodulation distortion (PIM) is shown in Figure 15.¹⁰ PIM is measured in the same way as SMPTE-IM, except that phase modulation of the carrier is measured instead of amplitude modulation. The phase modulation is then expressed in time (e.g., rms nanoseconds).

Damping factor (DF) as a function of frequency is shown in Figure 16, and is extremely high. It is high for three reasons: 1) the power MOSFETS present very light loading to the drivers, producing a low open-loop output impedance essentially equal to the inverse of their transconductance; 2) the error correction circuit tends to drive this open-loop output impedance to zero; 3) substantial overall negative feedback further reduces the output impedance by an amount approximating the feedback factor (40 dB at 20 kHz).

Although the need for this much damping factor is doubtful, the importance of DF on frequency response and coloration has sometimes been underestimated. This is explained by the fact that most speaker systems are designed assuming they will be driven by a pure voltage source (sometimes, it seems, with limitless current capability as well!). For example, the impedance of a nominal 4-ohm system may dip to 2.5 ohms and rise to over 50 ohms at various points across the frequency band due to driver and crossover resonances. A typical bipolar amplifier may have a damping factor of 100 (perhaps less at high frequencies), resulting in frequency response deviations on the order of 0.3 dB with such a load. Coloration due to low DF may also partly explain audible differences among vacuum-tube and low-feedback designs.

Figure 17 illustrates small-signal and full-power 20-kHz squarewaves into an 8-ohm load. Figure 18 shows small-signal and full-power 20-kHz squarewaves into a reactive load consisting of 1-ohm and 1 μ F in series. In the full-power case the squarewave has been bandlimited to 200 kHz by a first-order low-pass filter. Figure 19 shows 500 kHz small-signal squarewaves into an 8-ohm resistive load and a reactive load consisting of 1-ohm and 1- μ F in series. It also shows a full-power 500 kHz squarewave into an 8-ohm load. Few bipolar amplifiers would survive this test.

Table 1 summarizes overall performance of the amplifier.

* Society of Motion Picture and Television Engineers.

6. CONCLUSION

Power MOSFETs are capable of exceptional performance when used in combination with good drive circuitry and simple error correction circuitry. Their ability to operate without complex and unreliable safe-area limiting circuitry makes them especially useful for demanding audio applications. Compared with bipolar transistors, the major disadvantage of MOSFETs (and source of distortion) seems to be the lower transconductance, but this can be dealt with effectively by means of a simple error correction circuit. Although a MOSFET power amplifier can still be expected to cost a little more, the improved characteristics seem to justify the small premium in applications where performance is important.

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TABLE 1

POWER OUTPUT ($R_L = 8\Omega$)	50W
TOTAL HARMONIC DISTORTION (20 - 20 kHz)	<0.001%
SMPTE IM DISTORTION	0.00013%
DYNAMIC INTERMODULATION DISTORTION (DIM-30)	<0.006%*
(DIM-100)	0.014%
INTERFACE INTERMODULATION DISTORTION (IIM)	0.0001%
PHASE INTERMODULATION DISTORTION (PIM)	<0.1 ns
SLEW RATE	>300 V/ μ s
RISETIME	100 ns
DAMPING FACTOR (20 - 20 kHz)	>5000
S/N ('A' WTD, re 1 WATT)	108 dB
* BELOW MEASUREMENT FLOOR	

TABLE 1: Summary of MOSFET power amplifier performance.

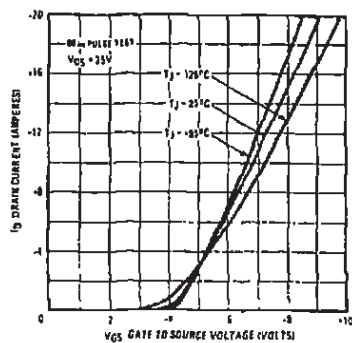
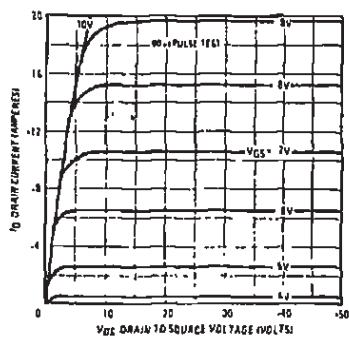
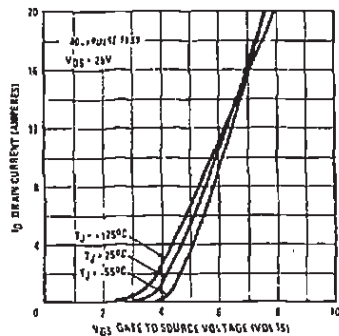
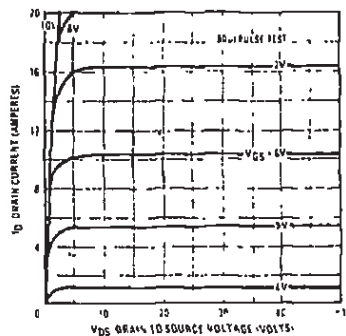


FIGURE 1: Drain and gate characteristics for power MOSFET types IRF-132 (a&b) and IRF-9130 (c&d).

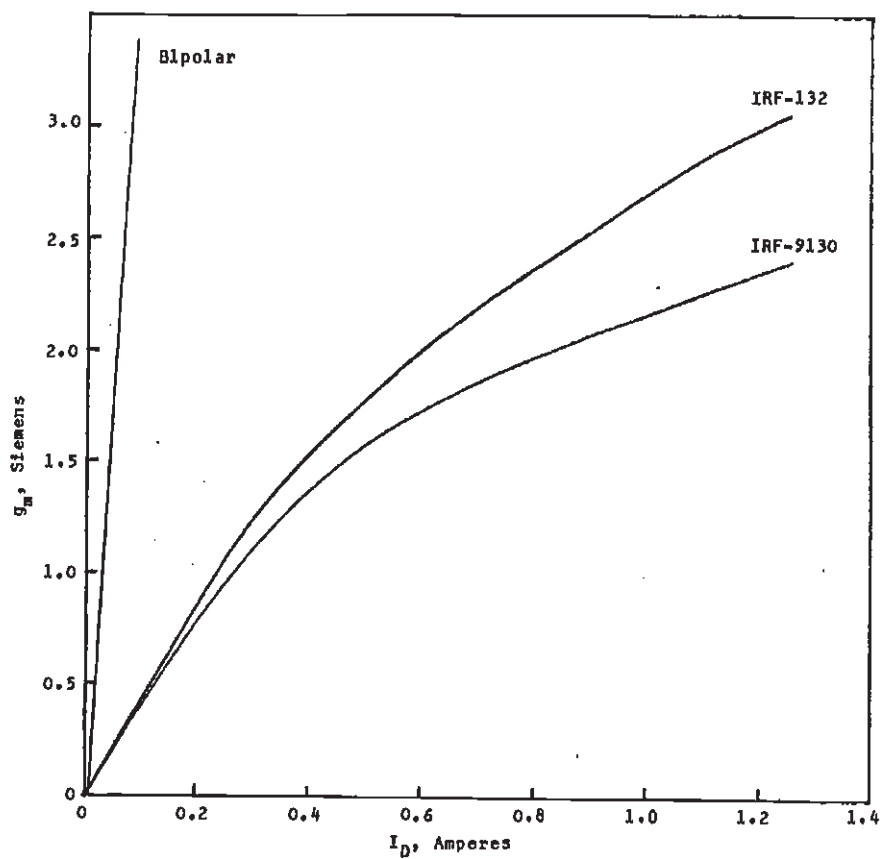


FIGURE 2: Power MOSFET transconductance versus drain current. For comparison, note much greater ratio of transconductance to operating current typical of bipolar transistors.

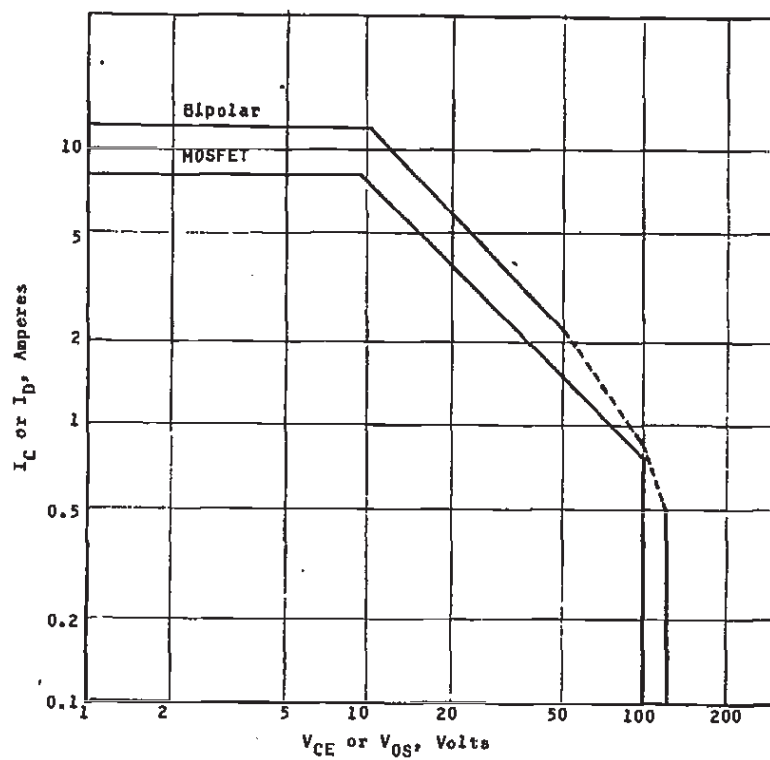


FIGURE 3: Safe operating area (SOA) comparison of a power MOSFET (IRF-9130) and a bipolar ring-emitter transistor (2SA-1072). Rated power dissipations are 75W and 120W, respectively.

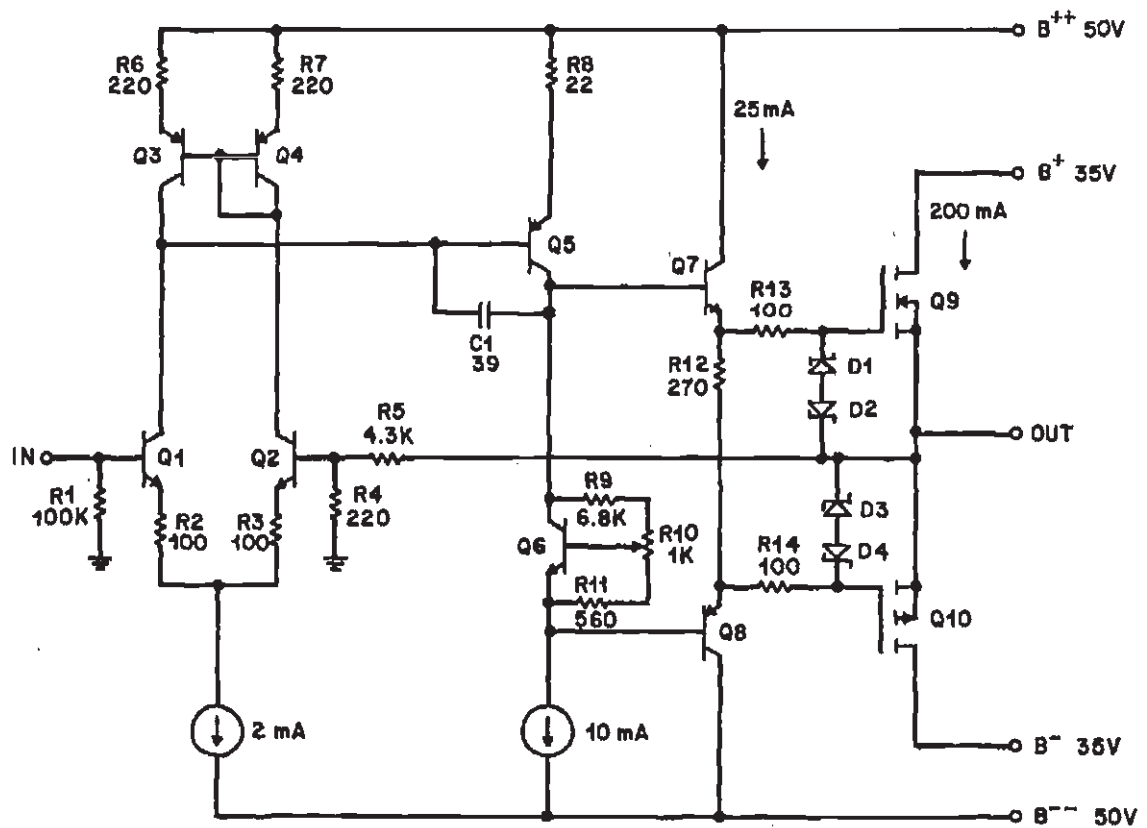
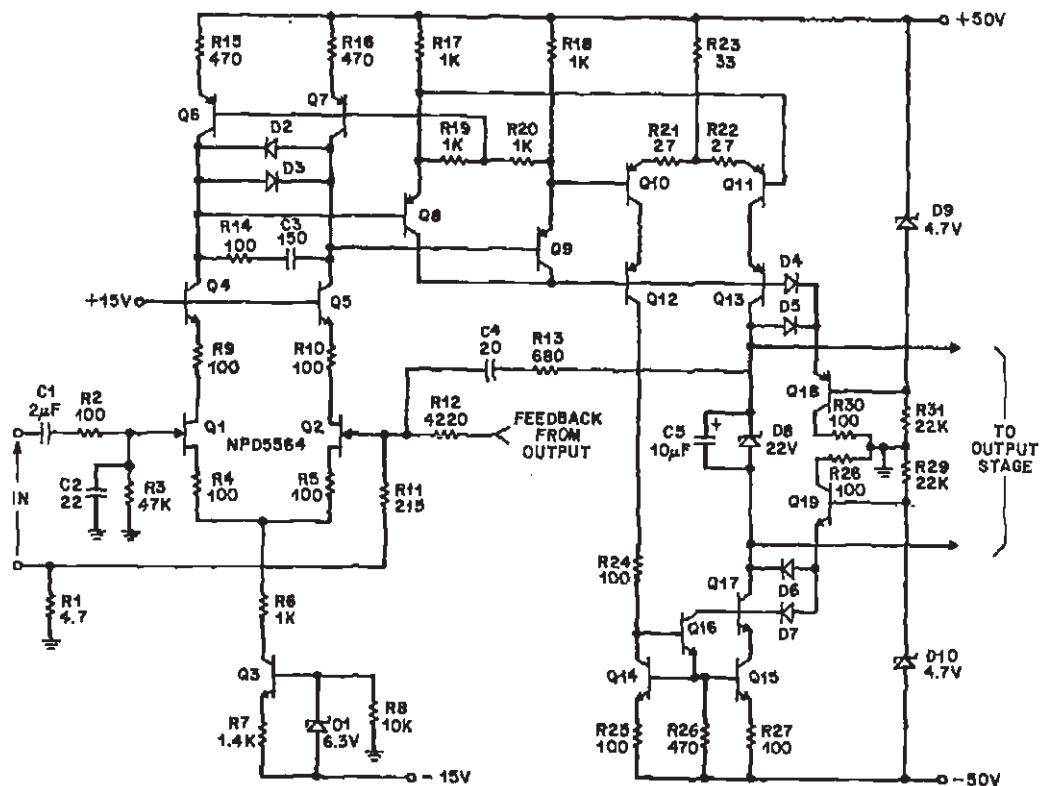


FIGURE 4: A simple MOSFET power amplifier. Note use of boosted power supplies to satisfy MOSFET gate drive requirements.



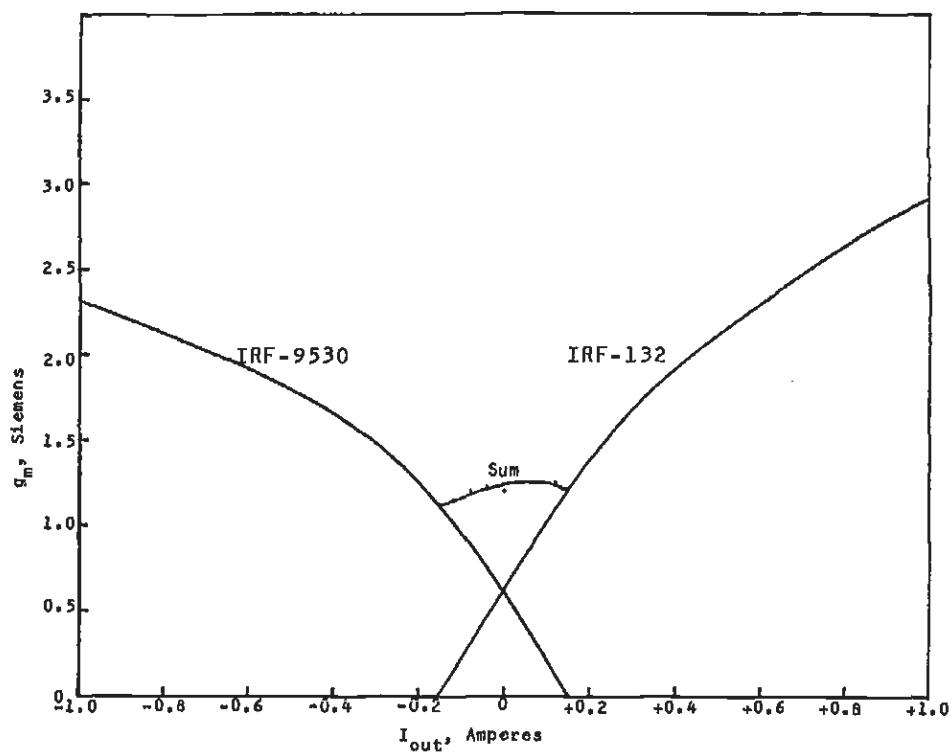


FIGURE 6: Output stage transconductance versus output current for a bias current of 150 mA. Reduced total transconductance in central region can cause crossover distortion.

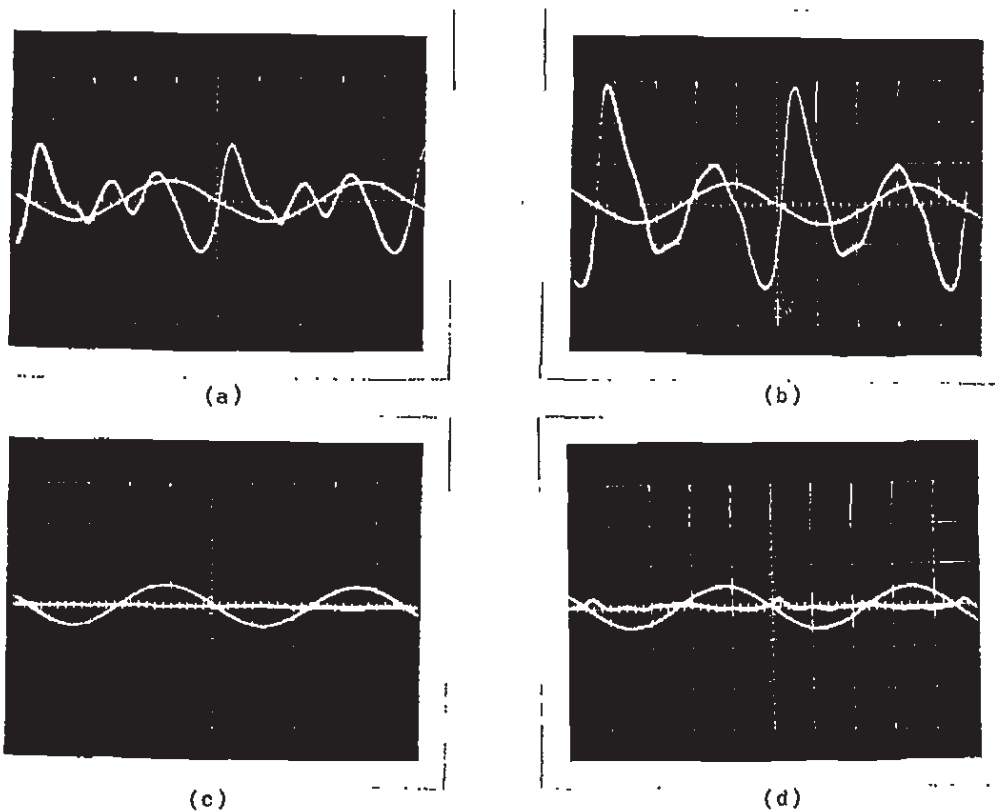


FIGURE 7: Output stage open-loop distortion (THD).
a) 1 kHz, no error correction; b) 20 kHz, no error
correction; c) 1 kHz, with error correction; d)
20 kHz, with error correction. Vertical distortion
scale 0.5%/div. All measurements at full-power (50W).

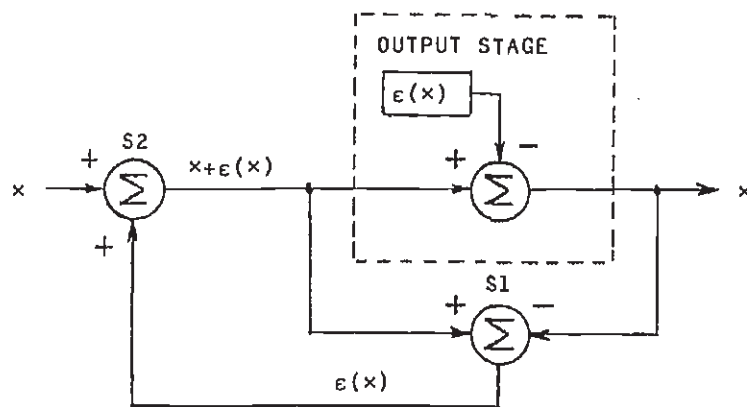


FIGURE 8: Output stage error correction technique.

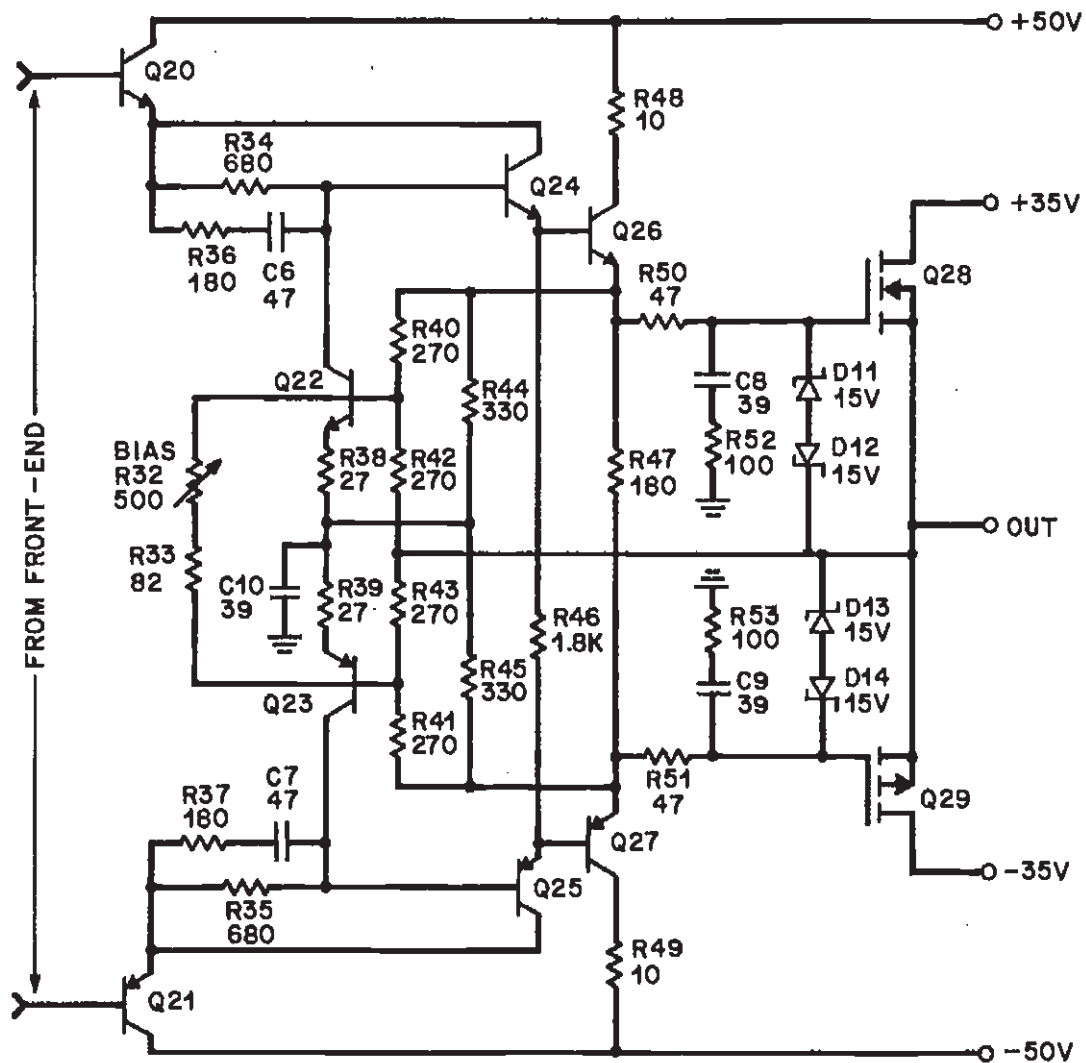


FIGURE 9: MOSFET power amplifier output stage. Q22 and Q23 provide error correction signals.

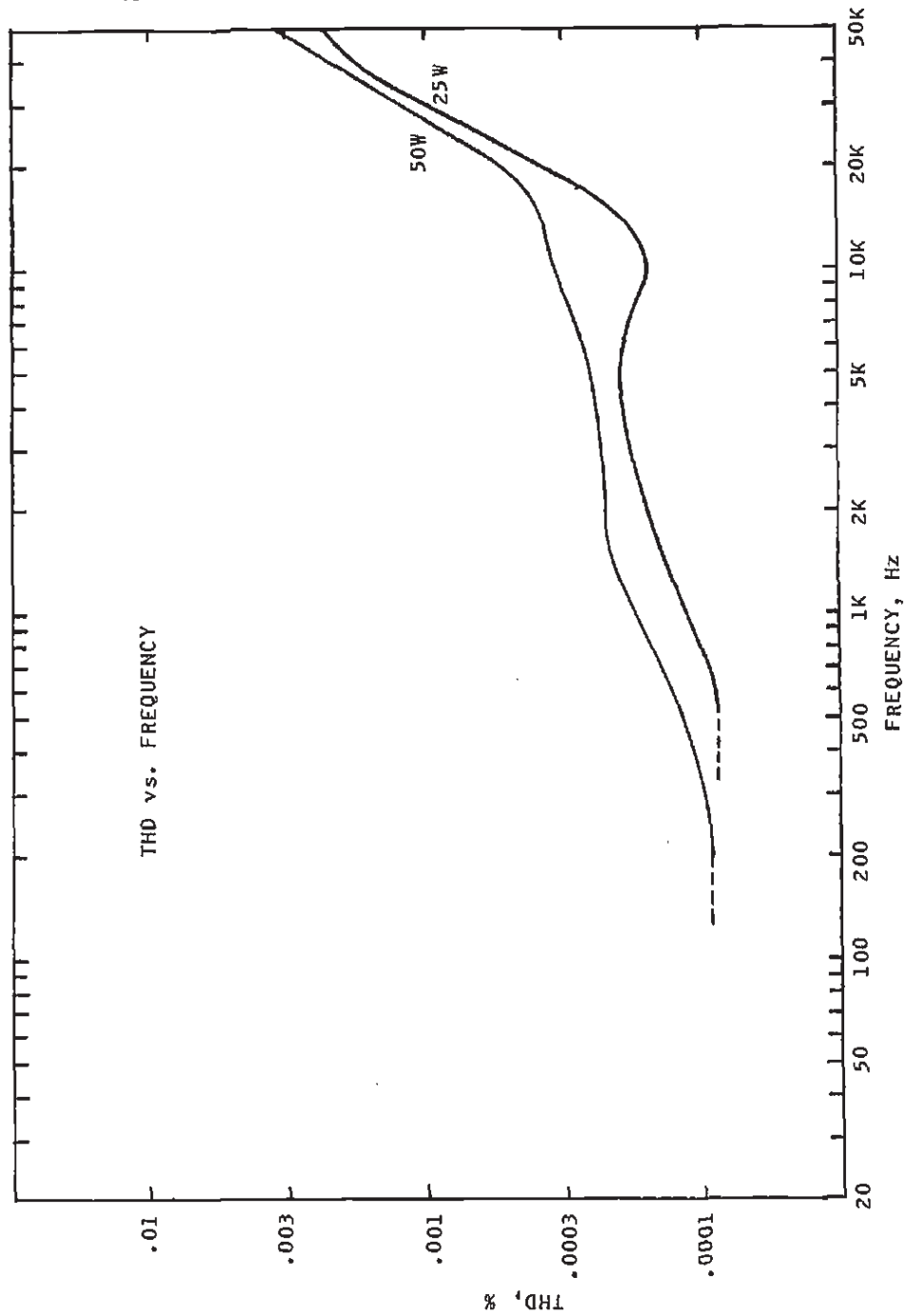


FIGURE 10: Total harmonic distortion (THD) as a function of frequency.

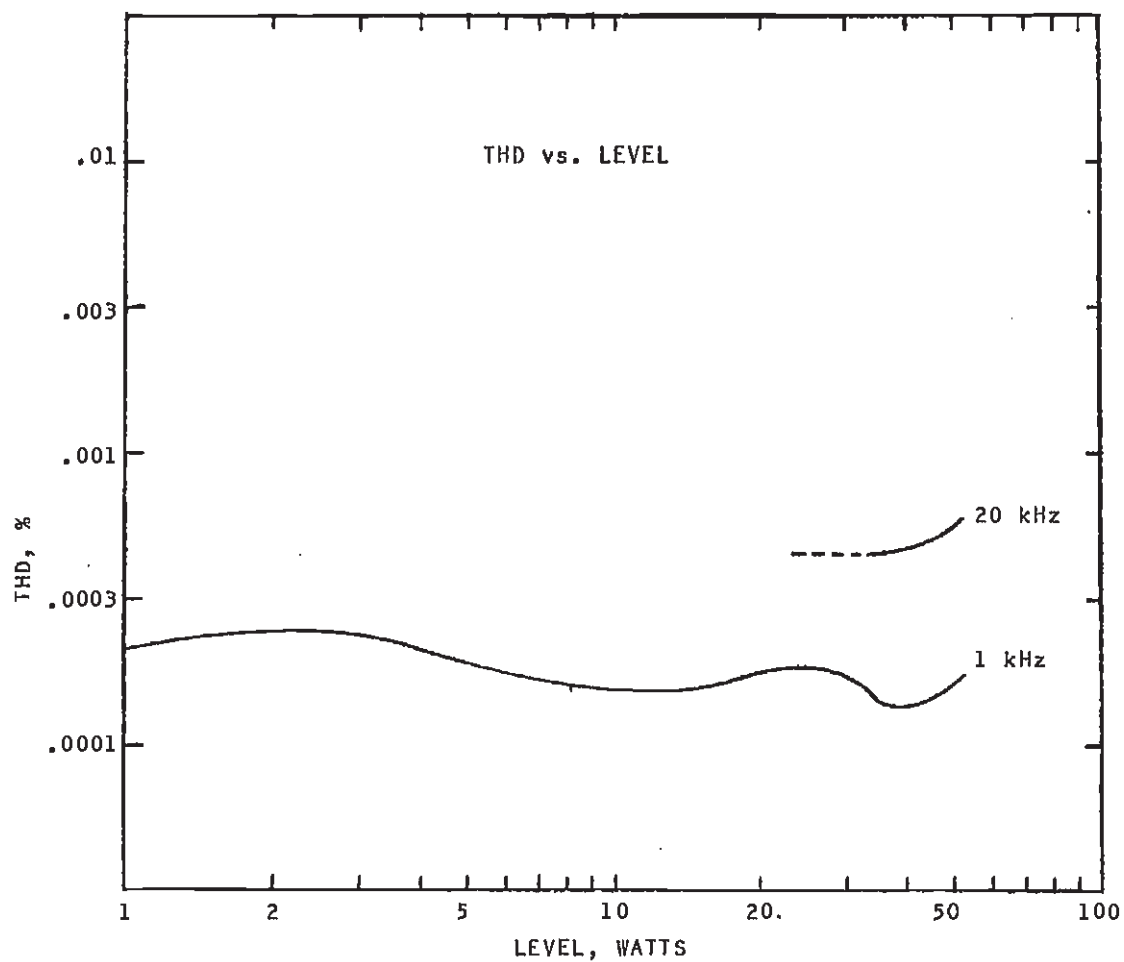
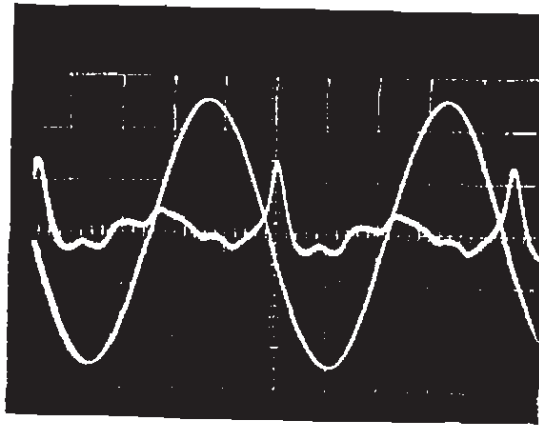
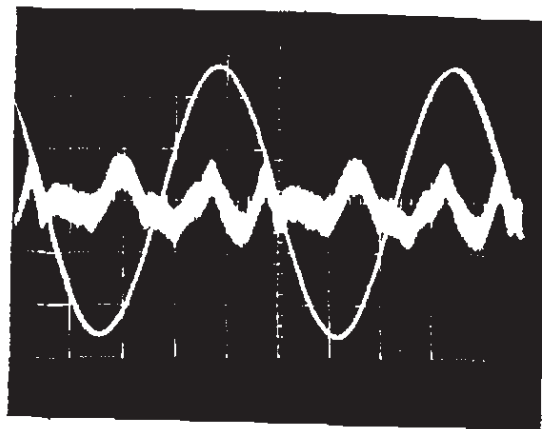


FIGURE 11: Total harmonic distortion as a function of level.



(a)



(b)

FIGURE 12: 20-kHz total harmonic distortion (THD) products at full power (50W). a) without error correction (THD analyzer reads .02%); b) with error correction (THD analyzer reads .0006%).

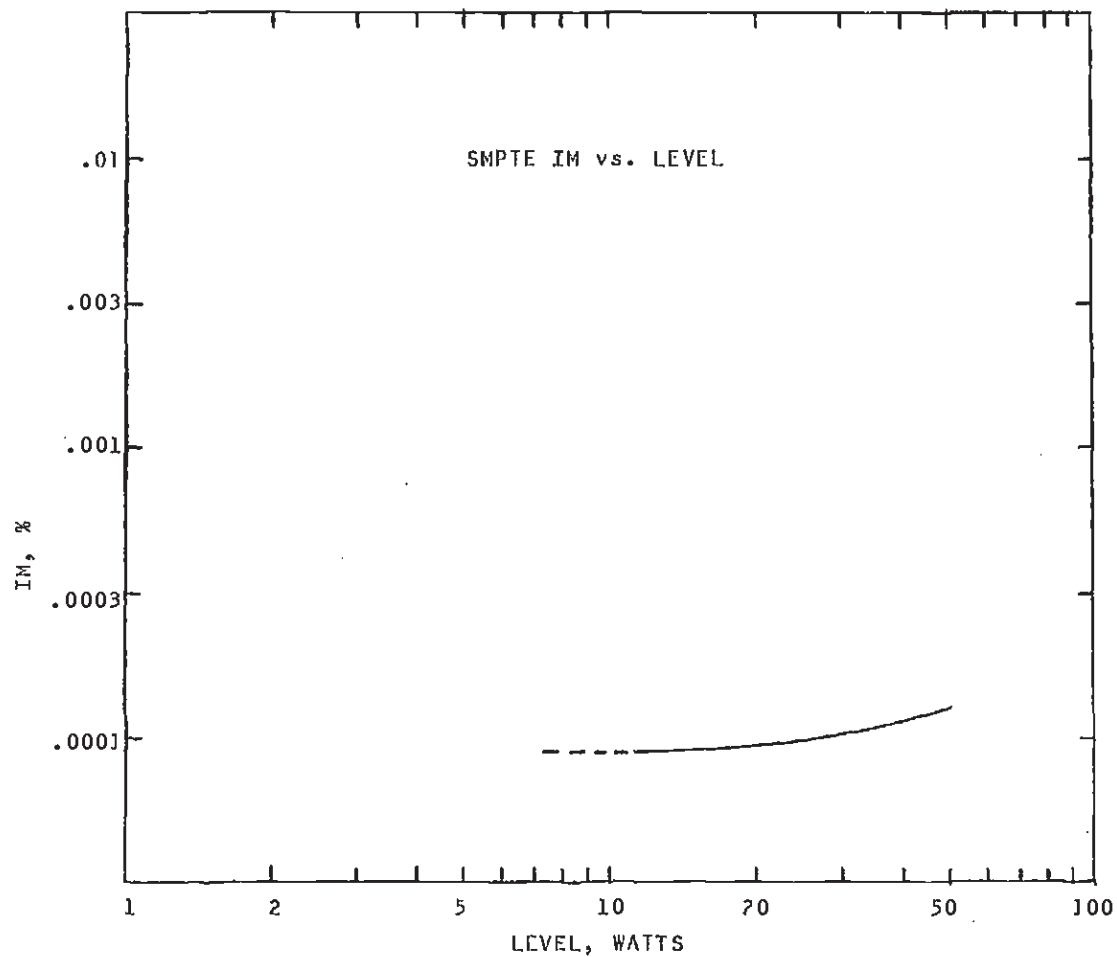


FIGURE 13: SMPTE intermodulation distortion (60 & 6000 Hz, 4:1) as a function of level.

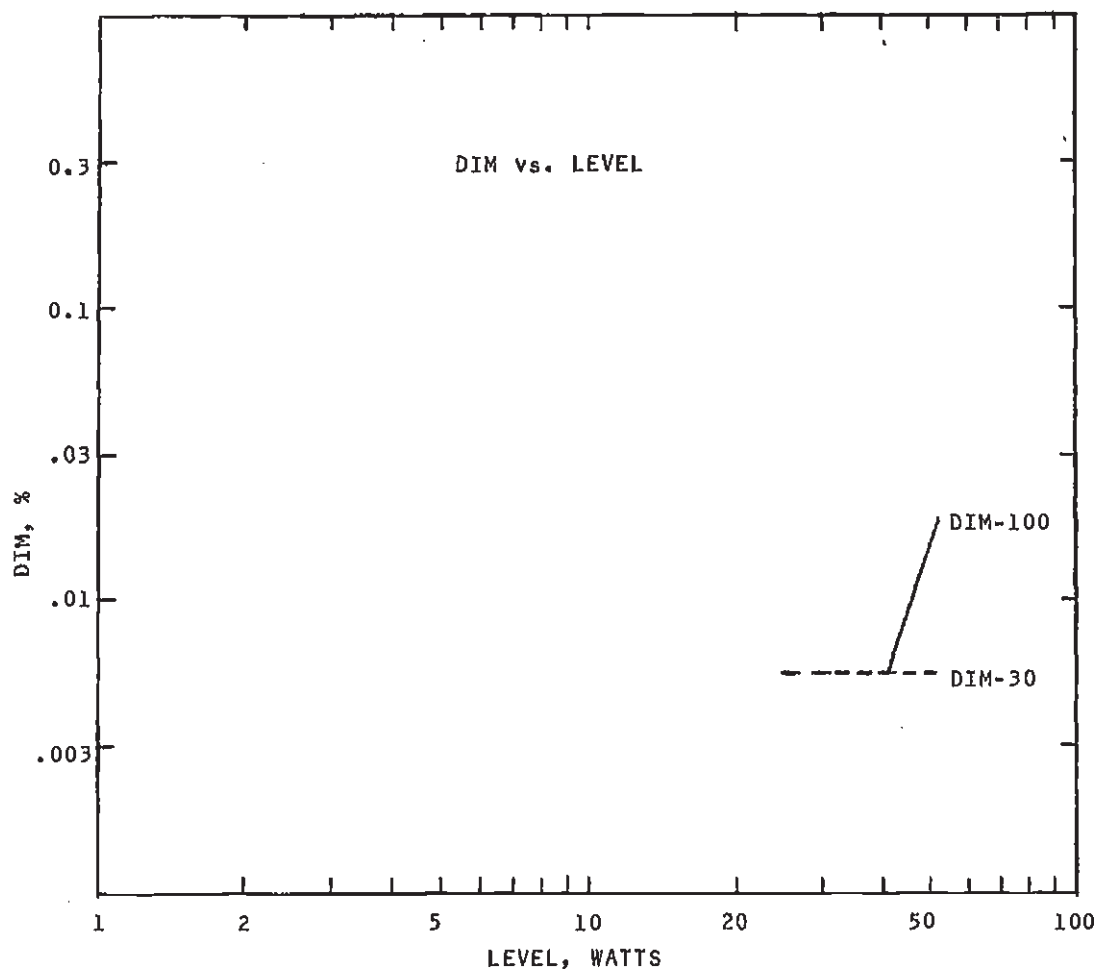


FIGURE 14: Dynamic intermodulation distortion (DIM-30 and DIM-100) as a function of level.

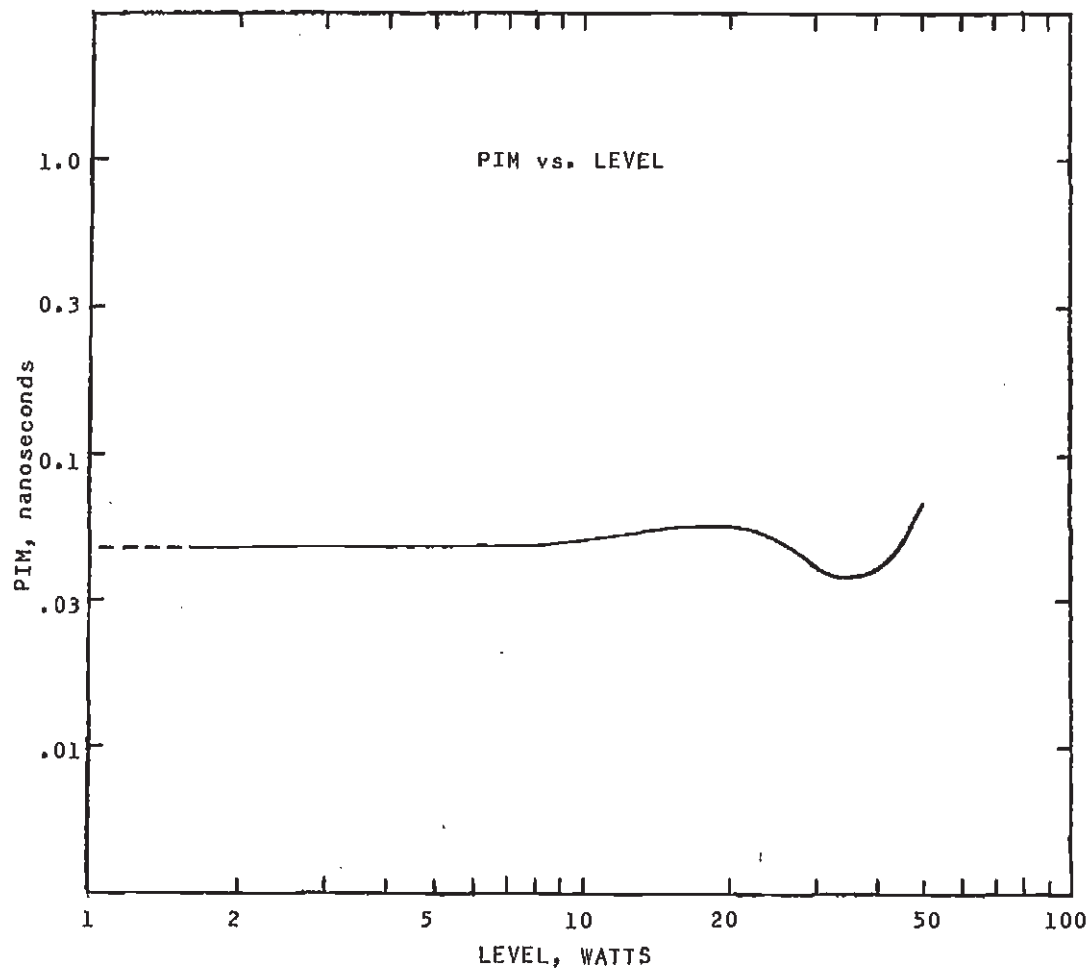


FIGURE 15: Phase intermodulation distortion (PIM) as a function of level. Note that phase modulation is expressed in rms nanoseconds.

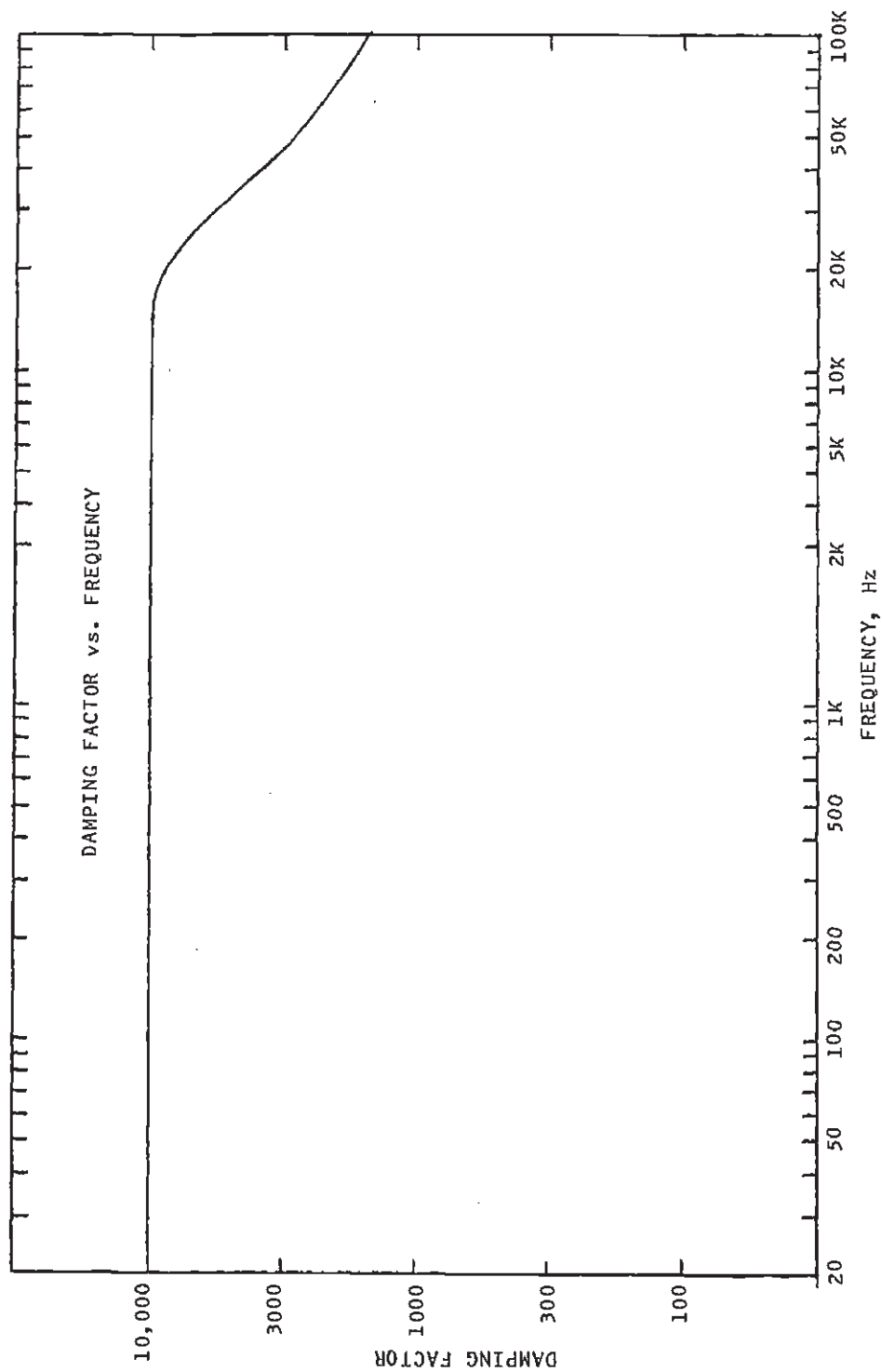
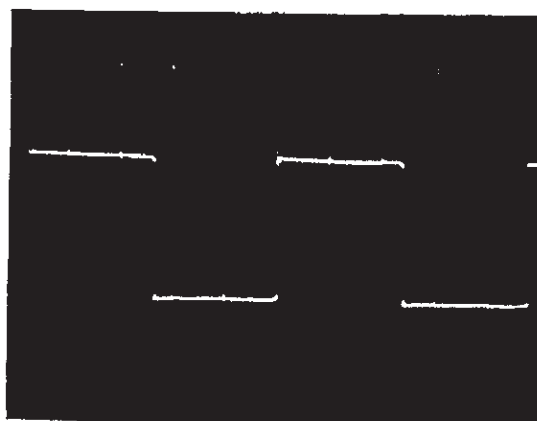
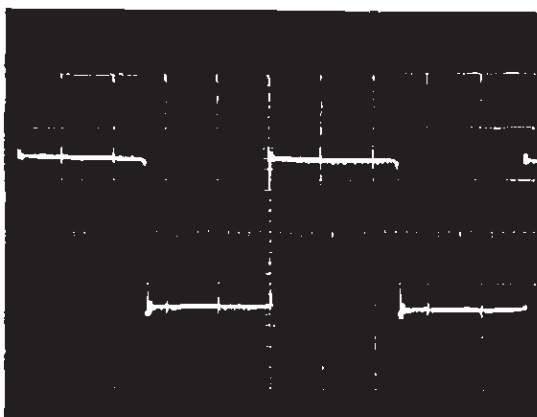


FIGURE 16: Damping factor as a function of frequency.

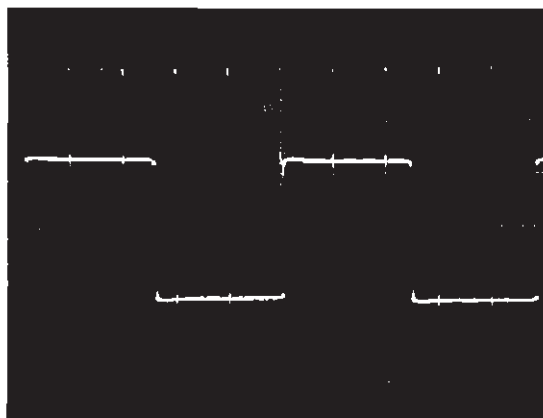


(a)

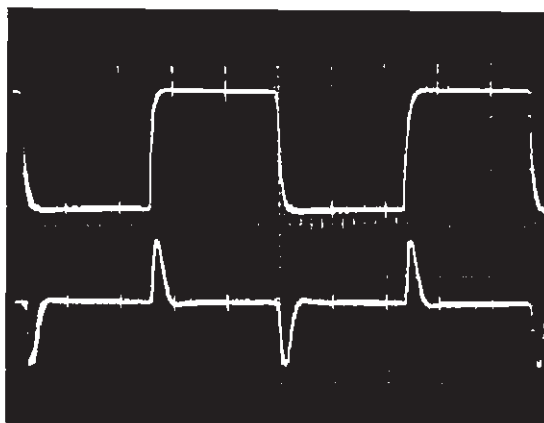


(b)

FIGURE 17: 20-kHz squarewave into an 8-ohm load.
a) small-signal (1V/div); b) full-power (20V/div).



(a)



(b)

FIGURE 18: 20-kHz squarewave into a 1-ohm resistor in series with a 1- μ F capacitor. a) small-signal (1V/div). b) full-power (20V/div), input bandlimited to 200 kHz. Bottom trace is output current (20A/div).

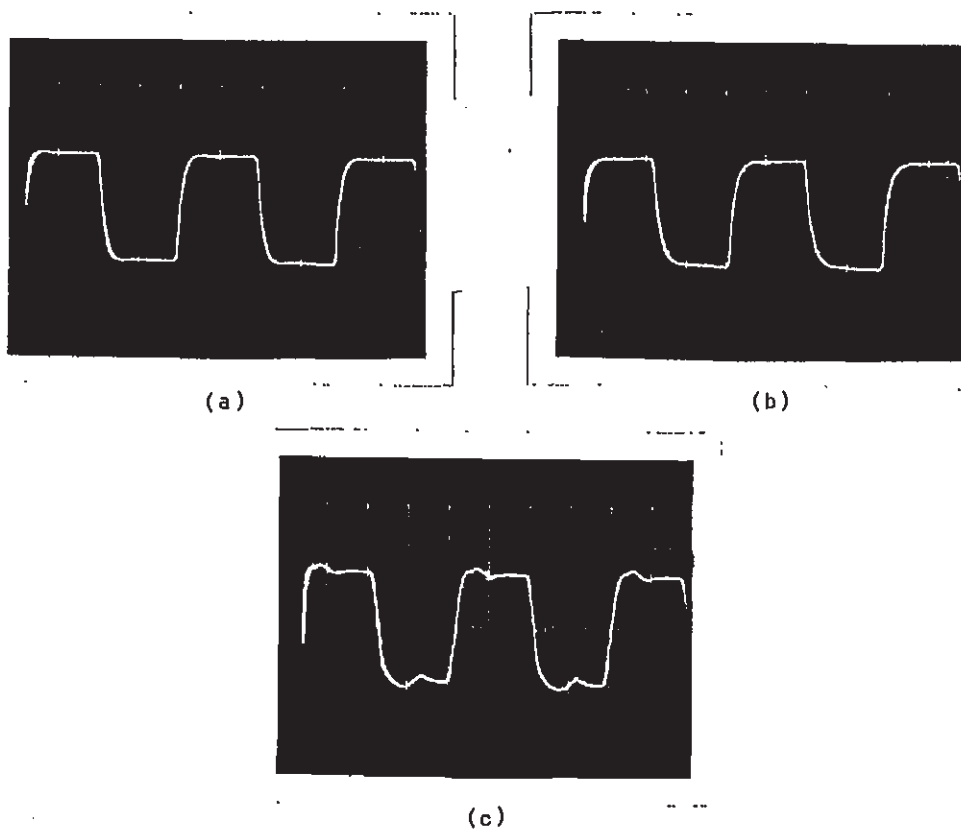


FIGURE 19: 500-kHz squarewave response. a) small-signal, 8-ohm load (1V/div); b) small-signal, 1-ohm and 1-uF series load (1V/div); c) full-power, 8-ohm load (20V/div).