

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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BROADCOM CORPORATION  
Petitioner

v.

SIGNAL ENHANCEMENT TECHNOLOGIES LLC  
Patent Owner

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Case IPR2014-00189  
Patent 7,493,097

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Before KARL D. EASTHOM, KALYAN K. DESHPANDE, and  
MATTHEW R. CLEMENTS, *Administrative Patent Judges*.

CLEMENTS, *Administrative Patent Judge*.

DECISION  
Institution of *Inter Partes* Review  
37 C.F.R. § 42.108

## I. INTRODUCTION

Broadcom Corporation (“Petitioner”) filed a petition requesting *inter partes* review of claims 7-11 (“the challenged claims”) of U.S. Patent No. 7,493,097 (Ex. 1101, “the ’097 patent”). Paper 3 (“Pet.”). Signal Enhancement Technologies LLC (“Patent Owner”) filed a Preliminary Response on March 13, 2014. Paper 9 (“Prelim. Resp.”). We have jurisdiction under 35 U.S.C. § 314.

The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides as follows:

THRESHOLD.—The Director may not authorize an *inter partes* review to be instituted unless the Director determines that the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.

Upon consideration of the petition, we determine that the information presented by Petitioner establishes that there is a reasonable likelihood that Petitioner would prevail in showing unpatentability of claims 7-11 of the ’097 patent. Accordingly, pursuant to 35 U.S.C. § 314, we institute an *inter partes* review of claims 7-11 of the ’097 patent.

### A. Related Proceedings

Petitioner and Patent Owner indicate that the ’097 patent is involved in a case captioned *Signal Enhancement Technologies LLC v. Broadcom Corporation*, Civil Action No. 8:12-cv-02072 (C.D. Cal.) (“the Litigation”). Pet. 1; Paper 6 at 2. Petitioner also has filed a separate petition for *inter partes* review of claims 1-4, 6, and 13-20 of the ’097 patent (IPR2014-

00188) and a petition for *inter partes* review of a related patent: IPR2014-00193 (U.S. Patent No. 6,785,530). Pet. 1.

*B. The '097 patent*

The '097 patent relates generally to communication devices and, in particular, to a mixer output stage. Ex. 1101, col. 1, ll. 7-8. Wireless receivers were traditionally built in a super heterodyne configuration, but due to cost and space efficiency, modern communication device receivers are often configured as a direct conversion receiver. *Id.* at ll. 33-37. In a direct conversion receiver, the modulated signal is down-converted directly to baseband in a single stage, whereas in a super heterodyne configuration, the receiver converts the signal to an intermediate frequency before demodulation to baseband. *Id.* at ll. 37-41. To down-convert the signal in a direct conversion receiver, a mixer in connection with a local oscillator is used to isolate the desired baseband signal. *Id.* at ll. 42-44. One problem that plagued prior art mixer designs is that, as the gain increased, an undesirably large amount of noise or non-linearity was introduced. *Id.* at ll. 47-50. Various solutions were proposed in the prior art, but the solutions introduced additional noise, increased current consumption, or both. *Id.* at ll. 52-55.

Figure 3 is reproduced below.

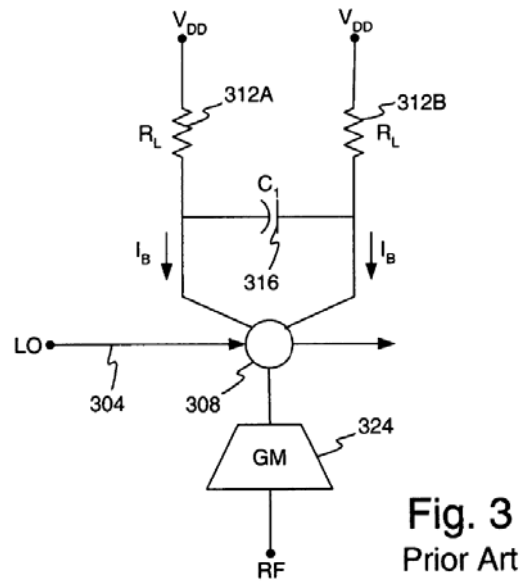


Figure 3 depicts an exemplary implementation of a prior art mixer. *Id.* at col. 4, ll. 37-38. Local oscillator input 304 is provided to mixer core 308, which also receives an input current  $I_B$  through resistors 312A and 312B (collectively 312). *Id.* at ll. 39-41. Current  $I_B$  represents the bias current. Another input of mixer core 308 connects to transconductance stage (GM) 324, which in turn connects to the radio frequency (RF) input. *Id.* at ll. 48-51.

To increase the gain of the mixer, the value of  $R_L$  may be increased to generate a signal magnitude that is sufficiently large for the subsequent processing elements. *Id.* at col. 5, ll. 10-16. However, raising  $R_L$  increases the voltage drop across resistors 312, thereby lowering the voltage headroom across mixer core 308. *Id.* at ll. 17-21. This is undesirable because it results in clipping and non-linearity of the output signal. *Id.* at ll. 23-27. As result, increasing  $R_L$  is not a viable option. *Id.* at ll. 27-28.

One alternative is to replace pull-up resistors 312 with transistors, but this structure results in increased current consumption by the transistors, and the transistors also contribute noise to the signal. *Id.* at ll. 30-33. As a result, this solution is also undesirable. *Id.* at ll. 34-35.

To address these issues, the '097 patent discloses a mixer configured to amplify the mixer output signal—i.e., the wanted signal—without introducing unwanted noise, increasing current consumption, or clipping and distorting the output signal. *Id.* at col. 1, ll. 63-67. In general, a mixer output stage is configured with a virtual ground at the mixer output to thereby de-couple the level of gain from the mixer configuration and to establish output linearity over the range of output frequencies. *Id.* at col. 1, l. 67 to col. 2, l. 3. The amplifier may comprise an operational amplifier or a trans-conductance device. *Id.* at col. 2, ll. 21-22.

Figure 4 is reproduced below.

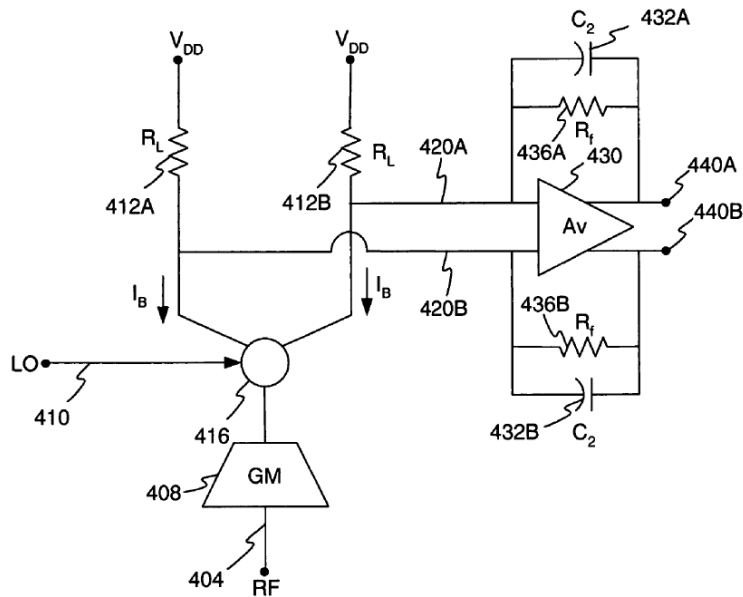


Fig. 4

Figure 4 depicts an example embodiment of a mixer output stage of the present invention. *Id.* at col. 5, ll. 36-37. In this embodiment, amplifier 430 connects to mixer core 416 via nodes 420A and 420B. *Id.* at ll. 59-60. Amplifier 430 may comprise any device configured to convert a current signal input to a voltage signal, such as an operational amplifier. *Id.* at ll. 60-64.

Feedback resistor 436A and feedback capacitor 432A connect in parallel between node 420A and output 440A. *Id.* at col. 6, ll. 4-6. Likewise, feedback resistor 436B and feedback capacitor 432B connect in parallel between node 420B and output 440B. *Id.* at ll. 6-8. In contrast to prior art embodiments, the value of resistors 412 does not control the level of gain and, as such, it is not necessary to increase  $R_L$  in order to increase gain to a desired magnitude. *Id.* at ll. 12-15. Instead, gain of amplifier 430 is controlled at least in part by the values of resistors 436. *Id.* at ll. 18-19. Increasing the value  $R_f$  of resistors 436 increases mixer gain. *Id.* at l. 36. This overcomes the drawbacks of the prior art by breaking the link between mixer gain and the value of  $R_L$ , in which an overly high  $R_L$  causes clipping and non-linearity of the mixer output. *Id.* at ll. 40-43.

Nodes 420 appear as virtual grounds, thereby causing current to flow through pull-up resistors 412 and into the operational amplifier 430 via nodes 420. *Id.* at col. 6, l. 66 to col. 7, l. 1. The virtual ground results from the feedback of the amplifier 430 and the loop gain. *Id.* at col. 7, ll. 1-3. The current is converted to a voltage at the output 440 of the amplifier 430

and the output gain of the amplifier 430 is controlled at least in part by the value  $R_f$  of feedback resistors 436. *Id.* at ll. 3-6.

In other embodiments, amplifier 430 may be replaced with a trans-impedance amplifier configured to generate an output signal that comprises a current signal. *Id.* at Fig. 5, col. 7, ll. 27-30.

### *C. Exemplary Claim*

Independent claim 7 is representative of the challenged claims. Claim 7 is reproduced below:

7. A mixer output stage comprising:
  - a positive input connected to gain device;
  - a negative input connected to the gain device;
  - a gain device configured to receive and process a mixer core output signal to generate a processed version of the mixer core output, the gain device further having a positive output terminal and a negative output;
  - a first feedback loop connected to the positive input and the negative output and having at least one resistive element;
  - and
  - a second feedback loop connected to the negative input and the positive output and having at least one resistive element;
  - wherein the mixer output stage is configured to establish a virtual ground at the positive input and the negative input for certain frequencies.

*D. References Relied Upon*

Petitioner relies upon the following references:

Kuiri	US 7,062,248	June 13, 2006 (filed Jan. 16, 2003)	Ex. 1102
Crols,	A 1.5 GHz Highly Linear CMOS Downconversion Mixer, 30 IEEE JOURNAL OF SOLID- STATE CIRCUITS, 736-42 (July 1995) (“Crols”)		Ex. 1103
Yamaji	US 6,381,449	Apr. 30, 2002	Ex. 1104
Kamath	US 7,177,613	Feb. 13, 2007 (filed Sept. 30, 2004)	Ex. 1105
Ravatin	2003/0186658	Oct. 2, 2003	Ex. 1106

*E. The Asserted Grounds of Unpatentability*

Petitioner argues that the challenged claims are unpatentable based upon the following grounds:

Reference[s]	Basis	Claims challenged
Kuiri	§ 102	7-11
Crols	§ 102	7-11
Yamaji	§ 102	7-10
Kamath	§ 102	7-11
Ravatin	§ 102	7-11

II. ANALYSIS

*A. Claim Construction*

In an *inter partes* review, claim terms in an unexpired patent are interpreted according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b); Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14,



2012). Also, claim terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

1. “*virtual ground*” (claims 7 and 11)

Petitioner proposes that “virtual ground” be construed to mean “a voltage level that is not physically connected to ground, yet has the same potential as ground.” Pet. 11-12. The ’097 patent uses the term “virtual ground,” but does not define it. In the Litigation, Petitioner and Patent Owner agreed on the construction proposed by Petitioner. *Id.* at 12 (citing Ex. 1116). Petitioner contends that its proposed construction is consistent with the ordinary meaning of the term and cites a textbook for support. *Id.* at 11-12 (citing Ex. 1114, 65 (“We speak of terminal 1 as being a **virtual ground**—that is, having zero voltage but not physically connected to ground.”)). Patent Owner does not dispute Petitioner’s proposed construction. On this record, we are persuaded that the broadest reasonable interpretation of “virtual ground” consistent with the specification of the ’097 patent is “a voltage level that is not physically connected to ground, yet has the same potential as ground.”

2. “*mixer core*” (claim 7)

Petitioner proposes that “mixer core” be construed to mean “a circuit to translate signals from one frequency to another.” Pet. 12-13. The ’097 patent uses the term “mixer core,” but does not define it. Petitioner contends that its proposed construction is consistent with both the specification of the

'097 patent and the ordinary meaning of the term “mixer core.” *Id.* at 12-13 (citing Ex. 1101, 5:49-53, 6:61-66; Ex. 1115, 155). Specifically, Petitioner contends that “mixer core” is a broad term that does not refer solely to a Gilbert Cell mixer. *Id.* at 12-13. According to Petitioner, the construction proposed by Patent Owner in the Litigation would improperly limit the claimed invention to a preferred embodiment—a Gilbert Cell mixer—and improperly exclude other mixers and mixer cores. *Id.* at 12-13 (citing Ex. 1116). Patent Owner, however, does not propose a construction of “mixer core.” Nor does Patent Owner dispute Petitioner’s proposed construction of “mixer core.” On this record, we are persuaded that the broadest reasonable interpretation of “mixer core” consistent with the specification of the '097 patent is “a circuit to translate signals from one frequency to another.”

3. *“wherein the mixer output stage is configured to establish a virtual ground at the positive input and the negative input for certain frequencies” (claim 7)*

Petitioner does not propose a construction for this phrase. Patent Owner proposes that these phrases be construed to require maintenance of a virtual ground at the amplifier input node “for only certain frequencies output by the mixer.” Prelim. Resp. 9-11. Patent Owner argues that the '097 patent discloses two embodiments. *Id.* at 3-7. The first embodiment, as depicted in Figure 4, is based on an op-amp, and therefore maintains the virtual ground for only certain lower frequencies. *Id.* The second embodiment, depicted in Figure 5, is based on a trans-impedance amplifier, and therefore maintains the virtual ground for all frequencies. *Id.* Claim 7, unlike claims 1 and 13, recites explicitly that the mixer output stage is

configured to establish a virtual ground only “for certain frequencies.” Ex. 1101, col. 10, ll. 31-33. Patent Owner argues that claim 7 should be interpreted to exclude embodiments that maintain a virtual ground for *all* frequencies. Prelim. Resp. 10-11.

We are not persuaded that Patent Owner’s proposal is the broadest reasonable interpretation of these phrases that is consistent with the specification of the ’097 patent. Patent Owner’s proposed construction would narrow the scope of the claims by excluding those embodiments in which the virtual ground is maintained not just “for certain frequencies,” as recited in claim 7, but also for *all* frequencies. Claim 7 does not explicitly exclude embodiments in which a virtual ground is maintained for all frequencies. Moreover, Patent Owner has not provided sufficient and credible evidence that such a limitation should be read into the claim phrases. For example, Patent Owner’s contentions imply that the “gain device” recited in claim 7 must be an operational amplifier, but dependent claims 8 and 9 specify that “the gain device” of claim 7 comprises “a trans-impedance device” (claim 8) or “a trans-resistance device” (claim 9), not an operational amplifier. Conversely, Patent Owner’s contentions imply that the “amplifier” recited in claims 1 and 13 must be a trans-impedance amplifier, but dependent claims 2 and 16 specify that “the amplifier” of claims 1 and 13, respectively, comprises “an operational amplifier.” Because independent claim 7 must be broad enough to encompass embodiments based upon trans-impedance device (claim 8) and a trans-resistance device (claim 9), we decline to construe this phrase to exclude

embodiments in which a virtual ground is maintained for *all* frequencies. Under the broadest reasonable interpretation of this phrase consistent with the specification of the '097 patent, the claim language encompasses the establishing of a virtual ground for all frequencies.

4. “*mixer core output signal*” (claim 7)

Petitioner does not propose a construction for this term. Patent Owner proposes that this term be construed to require receiving the mixer output directly without intervening processing. Prelim. Resp. 11-13. Patent Owner contrasts claim 7, which recites, “a gain device configured to receive and process a mixer core output signal,” with claim 13, which recites, “receiving the processed signal, *or a signal related to the processed signal.*” *Id.* (emphasis added). According to Patent Owner, the patentee used the term “mixer core output signal” in claim 7 to refer only to the mixer output, and not to signals that are merely *related to* the mixer output. *Id.* As will become evident in the Analysis section below, Patent Owner argues that several references do not disclose an amplifier “configured to receive a mixer core output signal” because a capacitor filters the signal received by the amplifier.

The term “mixer core output signal” is used only in claim 7 and in the Summary portion of the Specification, where claim 7 is restated. Ex. 1101, col. 2, ll. 39-40. However, similar terms are used in the '097 patent. For example, the '097 patent equates the term “mixer output signal” with “wanted signal.” *Id.* at col. 1, ll. 63-65 (“a mixer is disclosed that is configured to amplify the mixer output signal, *i.e.*[.,] *wanted signal*”)

(emphasis added). The '097 patent also uses the term “mixer output signal” to refer to “the output **716** of the mixer output stage.” *Id.* at col. 9, ll. 45-50. Moreover, the '097 patent contemplates the filtering of unwanted, or “blocker,” signals. *Id.* at col. 6, ll. 55-58 (“In one embodiment, the blocker comprises an unwanted interferer that may pass through the mixer because it is at a frequency that is in close proximity to the desired signal. *Supplemental filtering may eliminate the blocker.*” (emphasis added)). Patent Owner has not provided sufficient and credible evidence that the patentee intended the term “mixer output” to exclude a filtered output—i.e., the *wanted* signal—from a mixer. On this record, we construe “mixer core output signal” to include “the wanted signal, undesired signals from the mixer, or both.”

*B. The Challenged Claims – Anticipated by Kuiri*

Petitioner argues that claims 7-11 are unpatentable under 35 U.S.C. § 102(e) as anticipated by Kuiri. Pet. 14-22. In support of this ground of unpatentability, Petitioner provides detailed explanations as to how each claim limitation is disclosed by Kuiri, and relies upon the Declaration of Dr. Richard R. Spencer (“Dr. Spencer.”). *Id.* (citing Ex. 1107 ¶¶ 33-48).

*Kuiri (Exhibit 1102)*

Kuiri describes a mixer used with direct conversion RF receivers. Ex. 1102, col. 1, ll. 7-10.

Figure 3 is reproduced below.

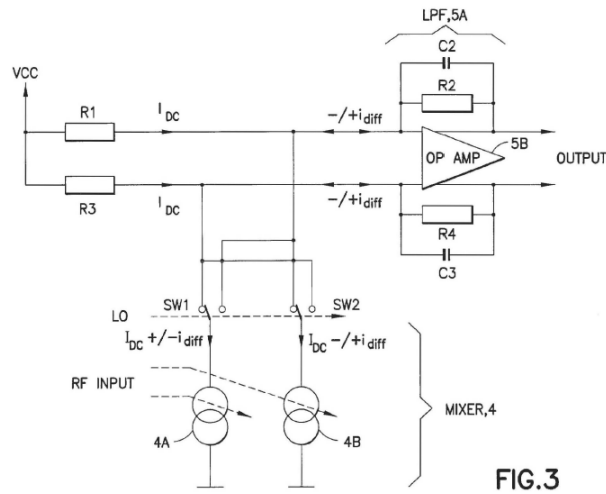


FIG.3

Figure 3 shows an embodiment of mixer 5 and improved low pass filter 5A. *Id.* at col. 4, ll. 9-12. The output currents from mixer core 4 are connected to the virtual ground node of operational amplifier (“op amp”) 5B. *Id.* at ll. 12-14. Because of feedback, both inputs to op amp 5B are at the same DC potential and differential currents are forced to go through the feedback circuitry. *Id.* at ll. 14-16.

Figure 4 is reproduced below.

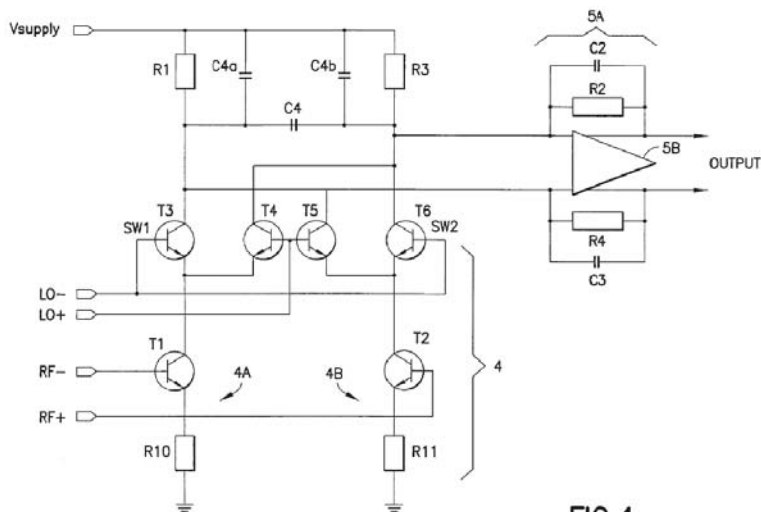


FIG.4

Figure 4 is a more detailed schematic diagram of the embodiment of mixer 4 and improved first low pass filter (“LPF”) 5A shown in Figure 3. *Id.* at col. 4, ll. 40-42. Mixer 4 is based on bipolar transistors, having an RF input, an LO input, and a mixer core comprised of transistors T3, T4, T5, and T6. *Id.* at ll. 44-59. The inputs to op amp 5B are connected between R1 and R3 and the collectors of transistor pairs (T3, T5) and (T4, T6), respectively. *Id.* at ll. 59-61. An additional capacitance, C4, is connected between the inputs to op amp 5B to serve as a filter for removing high frequency mixing components. *Id.* at ll. 61-63.

Analysis

In light of the arguments and evidence, Petitioner has established a reasonable likelihood that claims 7-11 are unpatentable as anticipated by Kuiri.

For example, we are persuaded that the record supports a finding that the limitations of independent claim 7 listed in the first column of the following table are met by the corresponding disclosure of Kuiri identified in the second column of the table:

<i>Independent Claim 7</i>	<i>Kuiri</i>
positive input	-/+i <sub>diff</sub> input to op amp 5B
negative input	-/+i <sub>diff</sub> input to op amp 5B
gain device	op amp 5B
first feedback loop & second feedback loop	path comprising R2 and C2, and path comprising R4 and C3

Independent claim 7 also recites “wherein the mixer output stage is configured to establish a virtual ground at the positive input and the negative input for certain frequencies.” Kuiri discloses that “[t]he output currents

from the mixer core **4** are connected to the virtual ground node of the operational amplifier (op amp) **5B**.” Ex. 1102, col. 4, ll. 12-14; *see also id.* at col. 3, ll. 44-46, col. 9, ll. 8-10.

We are not persuaded by Patent Owner’s argument that op amp 5B of Kuiri is not “configured to receive and process a mixer core output signal,” as recited in claim 7, because Kuiri’s op amp 5B receives “the mixer output” only after that output is filtered by capacitor C4. Prelim. Resp. 14-15. Patent Owner’s argument is based upon a claim construction that we declined to adopt. As discussed above, we construe the term “mixer core output signal” to include the wanted signal or filtered signals. While Kuiri discloses the use of capacitance C4 to “attenuate higher frequency signals at the output of the mixer **4**” (Kuiri, col. 5, ll. 3-4), such filtering does not prevent op amp 5B from receiving *the wanted signal*.

### Conclusion

We are persuaded that Petitioner has established a reasonable likelihood that it would prevail in showing that independent claim 7 is unpatentable as anticipated by Kuiri. We also are persuaded with respect to dependent claims 8-11.

### *C. The Challenged Claims – Anticipated by Crols*

Petitioner argues that claims 7-11 are unpatentable under 35 U.S.C. § 102(b) as anticipated by Crols. Pet. 22-26. In support of this ground of unpatentability, Petitioner provides detailed explanations as to how each claim limitation is disclosed by Crols, and relies upon the Declaration of Dr. Spencer. *Id.* (citing Ex. 1107 ¶¶ 49-60).



Crols (Exhibit 1103)

Crols describes a CMOS mixer topology for use in highly integrated downconversion receivers. Ex. 1103, Abstract. The topology is based on the use of four cross-coupled CMOS transistors operated in the triode region and connected to a virtual ground point. *Id.* at 736. Two capacitors are added on the virtual ground points. *Id.* Figure 1 is reproduced below.

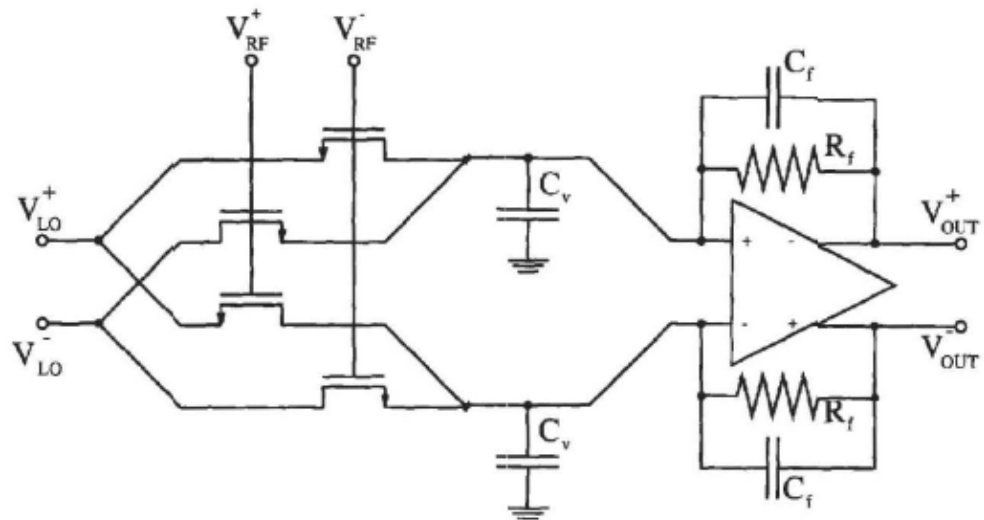


Fig. 1. The mixer topology with the extra capacitor on the virtual ground nodes.

*Id.* at 737. In order to let the input structure operate correctly for all frequencies, there may not be a signal on the virtual ground nodes of the mixer at any time. *Id.* Capacitors  $C_v$  ensure that all high-frequency currents injected to the virtual ground nodes are filtered out and not converted into voltages. *Id.* The op-amp still generates the virtual ground for low frequencies. *Id.* By using this structure, it is possible to optimize the input structure for high frequencies (more than 1 GHz) while designing the op-amp for low-frequency operations (a few MHz). *Id.*

Analysis

In light of the arguments and evidence, Petitioner has established a reasonable likelihood that claims 7-11 are unpatentable as anticipated by Crols.

For example, we are persuaded that the record supports a finding that the limitations of independent claim 7 listed in the first column of the following table are met by the corresponding disclosure of Crols identified in the second column of the table:

<i>Independent Claim 7</i>	<i>Crols</i>
positive input, and negative input	inputs to op-amp
gain device	op-amp
first feedback loop & second feedback loop	first path comprising $C_f$ and $R_f$ , and second path comprising $C_f$ and $R_f$

Independent claim 7 also recites “wherein the mixer output stage is configured to establish a virtual ground at the positive input and the negative input for certain frequencies.” Crols discloses that “[t]he topology is based on the use of four cross-coupled CMOS transistors operated in the triode region and connected to a virtual ground point [6].” Ex. 1103, 736. Crols further discloses that “[t]here are however two very important capacitors added on the virtual ground nodes of this topology (the capacitors  $C_v$  in Fig. 1).” *Id.* at 737. Crols further discloses that, “[t]his is normally done with the feedback structure over the opamp which creates the virtual ground at its inputs.” *Id.*

We are not persuaded by Patent Owner’s argument that Crols’s op amp is not “configured to receive and process a mixer core output signal,” as

recited in claim 7, because it receives “the mixer output” only after that output is filtered by capacitors  $C_v$ . Prelim. Resp. 15-16. Patent Owner’s argument is based upon a claim construction that we declined to adopt. As discussed above, we construe the term “mixer core output signal” to include the wanted signal, or filtered signals. While Crols discloses the use of capacitors  $C_v$  to “make sure that all high-frequency currents injected to the virtual ground nodes are filtered out and not converted into voltages” (Ex. 1103, 737), such filtering does not prevent Crols’s op amp from receiving *the wanted signal*.

Conclusion

We are persuaded that Petitioner has established a reasonable likelihood that it would prevail in showing that independent claim 7 is unpatentable as anticipated by Crols. We also are persuaded with respect to dependent claims 8-11.

*D. Other Grounds*

Petitioner also asserts the following grounds of unpatentability:

Reference[s]	Basis	Claims challenged
Yamaji	§ 102	7-10
Kamath	§ 102	7-11
Ravatin	§ 102	7-11

Pet. 27-43. Petitioner does not explain how these grounds are more persuasive than the grounds on which we institute. These asserted grounds are denied as redundant in light of Petitioner’s failure to show otherwise and

the determination that there is a reasonable likelihood that the challenged claims are unpatentable based on the grounds of unpatentability on which we institute an *inter partes* review. See 37 C.F.R. § 42.108(a).

### III. CONCLUSION

For the foregoing reasons, we determine that the information presented in the petition establishes that there is a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of claims 7-11 of the '097 patent.

The Board has not made a final determination on the patentability of any challenged claims.

### IV. ORDER

Accordingly, it is

ORDERED that pursuant to 35 U.S.C. § 314, an *inter partes* review is hereby instituted on the following grounds:

1. Claims 7-11 under 35 U.S.C. § 102 as anticipated by Kuiri; and
2. Claims 7-11 under 35 U.S.C. § 102 as anticipated by Crols.

FURTHER ORDERED that no other grounds raised in the Petition are authorized for *inter partes* review;

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(d) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial on the grounds of unpatentability authorized above; the trial commences on the entry date of this decision; and

FURTHER ORDERED that an initial conference call with the Board is scheduled for 2:00 PM Eastern Time on May 26, 2014; the parties are

directed to the Office Patent Trial Practice Guide<sup>1</sup> for guidance in preparing for the conference call, and should be prepared to discuss any proposed changes to the Scheduling Order entered concurrently herewith and any motion the parties anticipate filing during the trial.

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<sup>1</sup> Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,765-66 (Aug. 14, 2012).

Case IPR2014-00189

Patent 7,493,097

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