IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of:	Liu *et al.*	
U.S. Patent No.:	6,146,997	
Issue Date:	Nov. 14, 2000	Atty Docket No.: 39843-0011IP1
Appl. Serial No.:	09/407,268	
Filing Date:	Sep. 29, 1999	
Title:	METHOD FOR FORMING SELF-ALIGNED CONTACT HOLE	

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PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT NO. 6,146,997 PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42

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SAM-1010	U.S. District Court District of Delaware (Wilmington) CIVIL DOCKET FOR CASE #: 1:13-cv-02033-RGA

Samsung Electronics Co. Ltd, Samsung Electronics America, Inc., Samsung Semiconductor, Inc., Samsung Austin Semiconductor, LLC, and Samsung Telecommunications America, LLC (collectively "Petitioner" or "Samsung") petition for *Inter Partes* Review ("IPR") under 35 U.S.C. §§ 311–319 and 37 C.F.R. § 42 of claims 1-14 ("the Challenged Claims") of U.S. Patent No. 6,146,997 ("the '997 Patent"). As explained below, there exists a reasonable likelihood that Petitioner will prevail in demonstrating unpatentability of at least one Challenged Claim based on teachings set forth in the references presented in this petition.

I. MANDATORY NOTICES UNDER 37 C.F.R § 42.8(a)(1)

A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1)

Samsung Electronics Co. Ltd, Samsung Electronics America, Inc., Samsung Semiconductor, Inc., Samsung Austin Semiconductor, LLC, and Samsung Telecommunications America, LLC (collectively "Petitioner" or "Samsung") are the real parties-in-interest.

B. Related Matters Under 37 C.F.R. § 42.8(b)(2)

Petitioner is not aware of any disclaimers, reexamination certificates or petitions for *inter partes* review for the '997 Patent. The '997 Patent is the subject of Civil Action Number 1:13-cv-02033 (Del) filed December 16, 2013.

C. Lead And Back-Up Counsel and Service Information

Petitioner designates W. Karl Renner, Reg. No. 41,265, as Lead Counsel and Roberto Devoto, Reg. No. 55,108, as Backup Counsel, both available at 3200 RBC

Plaza, 60 South Sixth Street, Minneapolis, MN 55402 (T: 202-783-5070; F: 202-783-2331), or electronically by email at IPR39843-0011IP1@fr.com.

II. PAYMENT OF FEES – 37 C.F.R. § 42.103

Petitioner authorizes the Patent and Trademark Office to charge Deposit Account No. 06-1050 for the fee set in 37 C.F.R. § 42.15(a) for this Petition and further authorizes for any additional fees to be charged to this Deposit Account.

III. REQUIREMENTS FOR IPR UNDER 37 C.F.R. § 42.104

A. Grounds for Standing Under § 42.104(a)

Petitioner certifies that the '997 Patent is available for IPR. The present petition is being filed within one year of service against Petitioner, which was on December 17, 2013. *See* Ex. 1010, p. 4, entry 5 ("SUMMONS Returned Executed by Home Semiconductor Corporation. Samsung Telecommunications America LLC served on 12/17/2013" (emphasis added)) Petitioner is not barred or estopped from requesting this review on the below-identified grounds.

B. Challenge Under § 42.104(b) and Relief Requested

Petitioner requests IPR of the Challenged Claims on the grounds set forth in the table shown below, and requests that each of the Challenged Claims be found unpatentable. An explanation of unpatentability under the statutory grounds identified below is provided in the form of detailed description that follows, indicating where each element can be found in the cited prior art, and the relevance of that

prior art. Additional explanation and support for each ground of rejection is set forth in Ex. 1003, Declaration of Dr. Gary Rubloff.

Ground	'121 Patent Claims	Basis for Rejection
Ground 1	**1-14**	**§102: Doshi**
Ground 2	**1 and 3-8**	**§102: Becker**
Ground 3	**2 and 9-14**	**§103: Becker in view of Wong**

The '997 Patent issued from U.S. patent application number 09/407,268 (the U.S. '268 application), which was filed on September 29, 1999, and claimed priority to Taiwanese Patent Application No. 88107602 (the Taiwanese '602 application), filed on May 11, 1999.

Doshi qualifies as prior art at least under 35 U.S.C. § 102(e) because the patent application of Doshi was filed in the United States before the earliest potential priority date of May 11, 1999 of the Taiwanese '602 application. Specifically, Doshi (Ex. 1005) was filed on June 10, 1998 as application number 09/095,432, and claimed benefit of U.S. provisional application No. 60/051,287 ("the '287 provisional", Ex. 1008), filed on June 30, 1997. As discussed in Section III(B)(1) below, the effective prior art date for Doshi is June 30, 1997, i.e., the filing date of the '287 provisional, because the subject matter relied upon by Petitioner is disclosed in the '287 provisional.

Becker qualifies as prior art under 35 U.S.C. § 102(b) because Becker was issued in the United States more than one year earlier than the U.S. filing date of the '997 Patent. Specifically, Becker (Ex. 1006) was issued on June 23, 1998 as U.S. Patent No. 5,770,498, which was more than one year before the filing date of September 29, 1999 of the U.S. '268 application. Pre-AIA 35 U.S.C. § 102(b). ("A person shall be entitled to a patent unless [. . .] (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, ***more than one year prior to the date of application for patent in the United States***.") (Emphasis added.)

Wong qualifies as prior art at least under 35 U.S.C. § 102(b). Specifically, as indicated by page 2 of Ex. 1009, Wong was published in 1987 in the Proceedings of the First International Symposium on Ultra Large Scale Integration Science and Technology, which was more than one year earlier than the filing date of September 29, 1999 of the U.S. '268 application. Ex. 1009, p. 2.

1. The Earliest Priority Date of Doshi is June 30, 1997, the Provisional Application Filing Date

A patent applied in a rejection under § 102(e)(2) is prior art as of the filing date of its corresponding provisional application for commonly disclosed subject matter. *See In re Giacomini*, 612 F.3d 1380, 1384-85 (Fed. Cir. 2010) Doshi qualifies as prior art under § 102(e)(2) because Doshi is a "a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for [the '997 patent]." § Pre-AIA 35 U.S.C. 102(e)(2). The '287 provisional, which is the provisional application for Doshi, was filed on June 30, 1997, and discloses common subject matter as the Doshi disclosure relied upon by petitioner in challenging claims 1 to 14 of the '997 patent. Ex. 1008, p. 1.

Specifically, both Doshi and the '287 provisional include Figures 1, 2a to 2c, and 3a to 3k. Moreover, column 4, line 66 to column 7, line 28 of Doshi describes Figures 2a to 2c in detail, while page 10, line 2 to page 14, line 3 of the '287 provisional include the same corresponding descriptions. Similarly, column 7, line 29 to column 11, line 21 of Doshi describes Figures 3a to 3k in detail, while page 14, line 4 to page 20, line 13 of the '287 provisional also include the same corresponding descriptions. Accordingly, the effective prior art date for Doshi is June 30, 1997.

C. Claim Construction under 37 C.F.R. §§ 42.104(b)(3)

Each term of a claim subject to IPR is given its "broadest reasonable construction in light of the specification of the patent in which it appears." [1] 37 C.F.R.

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[1] Because the standards of claim interpretation applied in litigation differ from PTO proceedings, any interpretation of claim terms in this IPR is not binding upon Petitioner in any litigation(s) related to the subject patent. *See In re Zletz*, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

§ 42.100(b). Accordingly, for purposes of this proceeding only, Petitioner submits constructions for the following terms.

1. "forming a conformal layer of [etch barrier material/silicon nitride] overlying the substrate" (claims 1 and 9)

Claim 1 recites "forming a conformal layer of etch barrier material overlying the substrate surface." Claim 9 recites "forming a conformal layer of silicon nitride overlying the substrate surface."

Merriam Webster's Dictionary defines the word "conformal" as "conserving the size of all angles and therefore the shape of every elementary triangle." Ex. 1007, p. 3. Merriam Webster's Dictionary defines the word "conform" as "to have the same shape, outline, or contour." *Id.*

Fig. 2B of the '997 patent shows that "a conformal layer of silicon nitride 62 is deposited over the substrate surface using low pressure chemical vapor deposition (LPCVD)." Ex. 1001, col. 2:60-62. Prior to the deposition of the silicon nitride layer 62, at least the oxide layer 60, the gate oxide layer 52, and the gate electrodes 54 have been formed on the substrate 50. *Id.*, col. 2:48-59. As shown in the following annotated version of Fig. 2B of the '997 patent, the silicon nitride layer 62 thus is not in direct contact with the substrate 50. Rather, the silicon nitride layer, as highlighted in blue, is supported by the substrate 50, as highlighted in

green, where at least the oxide layer 60, the gate oxide layer 52, and the gate electrodes 54, as highlighted in orange, are between the silicon nitride layer 62 and the surface of the substrate 50. Moreover, the contour of the silicon nitride layer 62 appears to conform to the contour of the oxide layer 60, the gate oxide layer 52, and the gate electrodes 54 that have already been formed on the surface of the substrate 50.

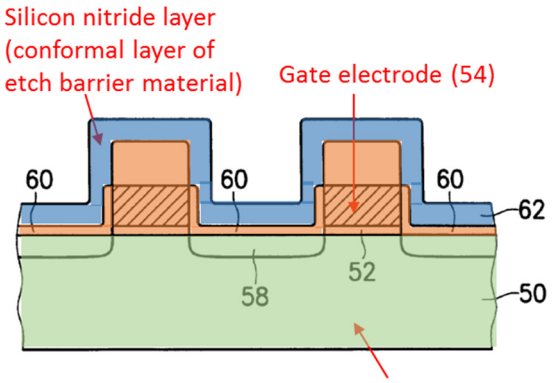


Fig. 2B

Accordingly, it is reasonable, for purposes of this proceeding in which the broadest reasonable construction standard applies, to consider the term "forming a conformal layer of [etch barrier material/silicon nitride] overlying the substrate surface" as broad enough to encompass "forming a layer of [etch barrier material/silicon nitride] supported by the substrate surface, the layer of [material] having a contour that conforms to a contour of one or more structures already formed on the substrate surface." *See* Ex. 1003, ¶¶ 24-26.

2. "forming an oxide layer over the diffusion region" (claims 2 and 9)

Each of claims 2 and 9 recites "forming an oxide layer over the diffusion region."

Merriam Webster's Dictionary defines the word "over" as "above." Ex. 1007, p. 4.

Within the specification of the '997 patent, the term "over" is applied consistent with the Merriam Webster's Dictionary definition to reference items that are above each other, even when separated by an intermediary item. Specifically, referring to Fig. 1B, the '997 patent discloses a "layer of silicon nitride 22 having a thickness of about 100 to 600 Å is deposited *over* the substrate surface using low pressure chemical vapor deposition (LPCVD)". Ex. 1001, col. 32-35. As shown in the annotated Fig. 1B below, prior to the deposition of the silicon nitride layer 22, at least the oxide layer 20, the gate oxide layer 12, and the gate electrodes 14 have been formed on the substrate 10. *Id*., col. 1:24-31. The silicon nitride layer 22, as highlighted in blue, is above the substrate 10, as highlighted in green, where at least the oxide layer 20, the gate oxide layer 12, and the gate electrodes 14, as highlighted in orange, are between the silicon nitride layer 22 and the surface of the substrate 10.

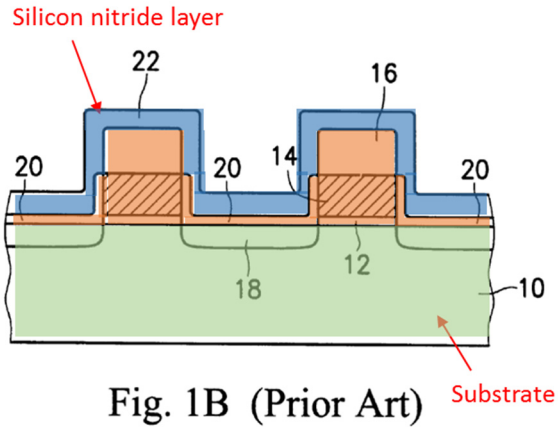


Fig. 1B (Prior Art)

Accordingly, it is reasonable, for purposes of this proceeding in which the broadest reasonable construction standard applies, to consider the term "forming an oxide layer over the diffusion region" as broad enough to encompass "forming an oxide layer above the diffusion region." *See* Ex. 1003, ¶¶ 27-28.

3. "spacer" (claims 1 and 9)

Merriam Webster's Dictionary defines the word "spacer" as "one that spaces." Ex. 1007, p. 6.

The '997 patent does not expressly define the term "spacer." According to the '997 patent, a spacer is a structure that is formed before or during formation of the contact hole. *See* Ex. 1001, col. 1:24-67, Ex. 1001, col. 2:24-28, col. 3:17-21, and col. 3:33-39. Functionally, the '997 patent discloses that a spacer is a structure that can "prevent shorting between the gate electrode and the conductive plug." Ex. 1001, col. 3:36-39.

Accordingly, it is reasonable, for purposes of this proceeding in which the broadest reasonable construction standard applies, to consider the term "spacer" as

broad enough to encompass "a structure that spaces between two conductive structures." *See* Ex. 1003, ¶¶ 29-31.

4. "etching an opening through the insulating layer self-aligned and borderless to the diffusion region" (claims 1 and 9)

The '997 patent discloses that "***[s]elf-alignment is a technique in which multiple levels of regions on the wafer are formed using a single mask***, thereby eliminating the alignment tolerance required by additional masks. This powerful approach is being used more often as circuit sizes decrease. Self-aligned contacts are often used in memory cells where contacts are limited only by the spacers and field oxide bird's beak or a contact window landing pad. Therefore, ***the mask contact window can be oversized relative to the contact area underneath, and no contact borders are needed***, resulting in significant space saving." Ex. 1001, col. 1:11-20 (emphasis added).

Based on this '997 patent usage, it is reasonable, for purposes of this proceeding in which the broadest reasonable construction standard applies, to consider the term "etching an opening through the insulating layer self-aligned and borderless to the diffusion region" as broad enough to encompass "etching an opening to the diffusion region using a single mask through multiple layers including the insulating layer, where the mask contact window is oversized relative to the diffusion region." *See* Ex. 1003, ¶¶ 32-34.

IV. SUMMARY OF THE '997 PATENT

A. Brief Description

Generally, the '997 patent is directed to a method for forming a self-aligned contact hole. Ex. 1001, claims 1 and 9. Self-alignment is a technique in which multiple levels of regions on the wafer are formed using a single mask, where the mask contact window may be oversized relative to the contact area underneath. *Id.*, col. 1:11-20; Ex. 1003, ¶ 15. For example, a spacer can be used to define the boundary of the contact area of a self-aligned contact hole. Ex. 1003, ¶ 15. Moreover, the spacer arranged between the contact area and an adjacent conductive structure (e.g., a gate electrode) can prevent shorting between the contact area and the adjacent conductive structure after the contact plug in the contact hole has been formed. Ex. 1001, col. 3:32-39.

According to the inventors of the '997 patent, in the conventional process, the formation of a spacer and the formation of a contact hole are two separate processes. The two separate processes increase manufacturing costs and decreases the throughput. *Id.* col. 1:65-67. For example, referring to the annotated Fig. 1C of the '997 patent below, after gate electrodes 14 and diffusion regions 18 have been formed on a substrate 10, a conformal silicon nitride layer 22 is deposited over the gate electrodes 14 and the diffusion regions 18, and a spacer 22a of silicon nitride is formed by an anisotropic etch. *Id.*, col. 1:33-40; Ex. 1003, ¶ 16.

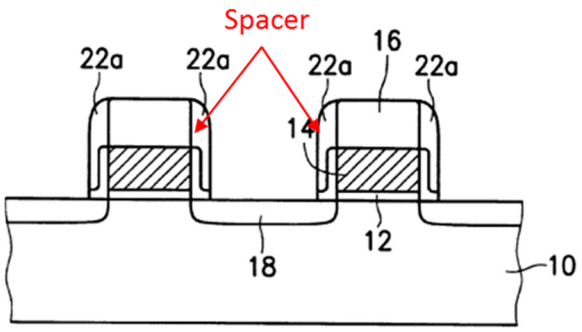


Fig. 1C (Prior Art)

Following the spacer formation, a second layer of silicon nitride layer 24 is formed, followed by the formation of an inter-layer dielectric (ILD) insulating layer 26. Ex. 1001, col. 1:41-50. Referring to the annotated Fig. 1E below, a contact hole 29 is lithographically defined, and the insulating layer 26 is etched. *Id.*, col. 1:51-67. The second layer of silicon nitride layer 24 acts as an etch stop for the self-aligned contact hole. The second layer of silicon nitride layer 24 is then etched away, exposing the previously formed spacer 22a and the contact area (i.e., diffusion region 18) for contact plug formation. *Id*; Ex. 1003, ¶ 17.

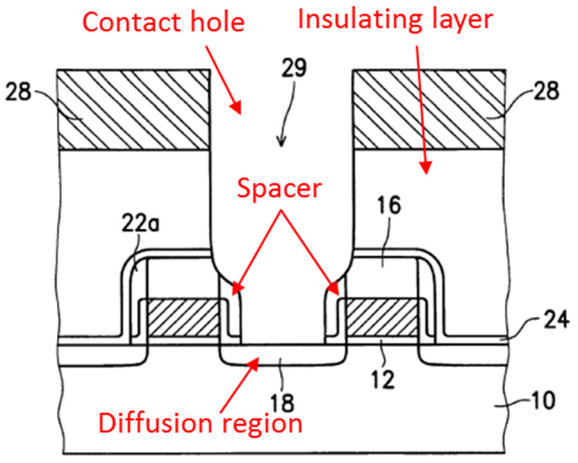


Fig. 1E (Prior Art)

The purported novelty of the '997 patent is to combine the spacer formation step and the contact hole exposure step into a single processing step to reduce the number of process steps. Ex. 1001, col. 1:65-67; col. 2:5-14; col. 3:40-47. The reduction of processing steps may reduce manufacturing costs and increase throughput. *Id.* For example, referring to the annotated Fig. 2B of the '997 patent below, after gate electrodes 54, diffusion regions 58, a thermal oxide layer 60, and gate oxides 52 have been formed on a substrate 50, a conformal layer of silicon nitride 62 is deposited over the substrate surface. *Id.*, col. 2:48-67; Ex. 1003, ¶¶ 18-19.

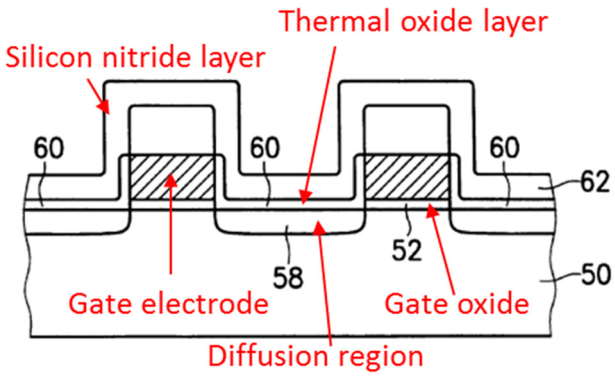


Fig. 2B

Referring to the annotated Fig. 2C of the '997 patent below, a planarized ILD insulating layer 64 is formed over the conformal layer of silicon nitride 62, and a photoresist layer 66 is formed and patterned to expose the contact hole. Ex. 1001, col. 3:1-24. An etch that is highly selective to the silicon nitride layer 62 is performed to etch away the insulating layer 64. *Id;* Ex. 1003, ¶ 20.

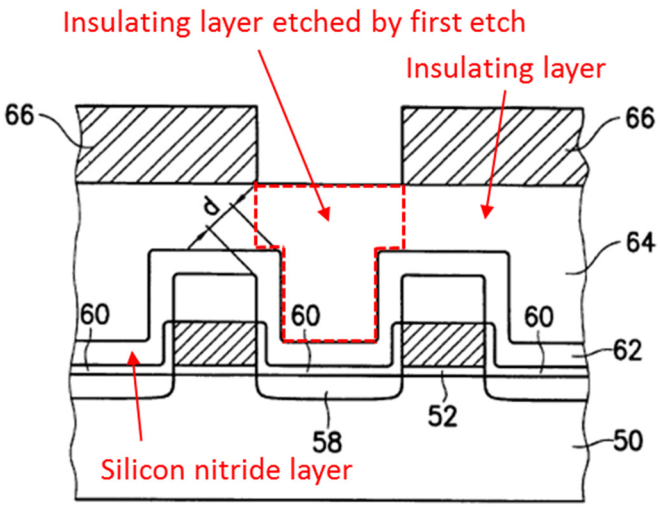


Fig. 2C

Referring to the annotated Fig. 2D of the '997 patent below, following the first selective etch of the insulating layer 64, the silicon nitride layer 62 is anisotropically etched to expose the diffusion region 58. Ex. 1001, col. 3:1-24. Due to the directionality of the anisotropic etch, a spacer 62a is formed on the sidewall of the electrode 54 during the same silicon nitride etch that exposes the diffusion region 58 to complete the contact hole 67. *Id.* After the contact hole 67 is filled with conductive material to form a conductive plug, the spacer 62a can be used to prevent shorting between the gate electrode 54 and the conductive plug. *Id.* col. 3:33-39; Ex. 1003, ¶ 21.

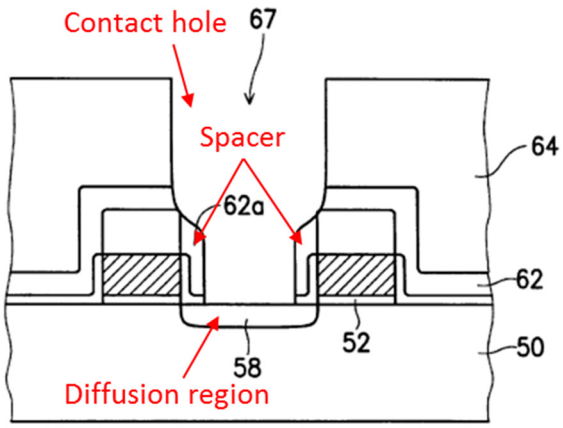


Fig. 2D

B. Summary of the Prosecution History of the '997 Patent

The '997 Patent issued from U.S. patent application number 09/407,268, which was filed on September 29, 1999, and claimed priority to Taiwanese Patent Application No. 88107602, filed on May 11, 1999. Ex. 1002, p. 6.

On March 2, 2000, the U.S. Patent and Trademark Office ("the Office") mailed a non-final Office Action. *Id*., p. 55. In the non-final Office Action, the Office rejected claims 1, 2, 4, 6, 8, 9, 12 and 14 under 35 U.S.C. § 102(b) over U.S. Patent No. 5,734,185 ("Iguchi"), and rejected claims 5, 7, 11, and 13 under 35 U.S.C. § 103(a) over Iguchi in view of U.S. Patent No. 5,753,547 ("Ying").

In the Response filed on May 31, 2000, the applicant referred to the recited steps of "etching an opening through the insulating layer self-aligned ... anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etched barrier material on

the side wall of the gate electrode," and argued that "Iguchi fails to teach or disclose forming a spacer after forming a contact hole in the insulating layer using self-aligned technology." *Id.*, pp. 62-63. No claim amendments were filed.

In the Notice of Allowance issued on June 12, 2000, the Examiner revealed his belief that the prior art failed to teach "a method for forming a self-aligned contact hole, comprising the steps of providing a semiconductor substrate having a gate electrode and a diffusion region; forming a conformal layer of etch barrier material overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode; forming an insulating layer overlying the barrier layer; etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop; and anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etch barrier material on the sidewall of the gate electrode." *Id.*, p. 68.

V. MANNER OF APPLYING CITED PRIOR ART TO EVERY CLAIM FOR WHICH IPR IS REQUESTED, THUS ESTABLISHING A REASONABLE LIKELIHOOD THAT AT LEAST ONE CLAIM OF THE '997 PATENT IS UNPATENTABLE

This petition shows how the references listed above anticipate or render obvious the Challenged Claims of the '997 Patent. As detailed below, this petition demonstrates a reasonable likelihood of Petitioners prevailing with respect to each (and therefore at least one) of the Challenged Claims of the '997 Patent.

As noted above in section IV(B), the Office allowed the claims of the '997 Patent based on the Examiner's belief that the prior art failed to teach all of the limitations as recited in claim 1. However, an inspection of the Response filed on May 31, 2000 reveals that the feature that the applicant relied upon as distinguishable from the cited prior art was the limitation of "etching an opening through the insulating layer self-aligned ... anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etched barrier material on the side wall of the gate electrode." Ex. 1002, pp. 62-63. To this point, Petitioner found numerous prior art references that disclose forming a self-aligned contact hole, where an anisotropic etch of the etch barrier material exposes the diffusion region and simultaneously forms a spacer of the etched barrier material on the side wall of the gate electrode. As detailed below, each of Doshi and Becker, which was not of record during prosecution of the '997 Patent, discloses at least this very limitation.

A. Doshi Anticipates Claims 1-14.

Doshi discloses a method of fabricating an integrated circuit, including a method of fabricating contact openings. *See* Ex. 1005, Abstract; *see also* Ex. 1003, ¶ A-1. According to Doshi, gate electrode structures 10 and doped source/drain diffusion regions 7 and 7' are fabricated on a semiconductor substrate 2. Ex. 1005, col. 7:29 – 8:7. As shown in the following annotated version of Fig. 3d of Doshi, a

conformal layer of silicon nitride layer 30 is deposited over the gate electrode structures 10 and the source/drain diffusion regions 7 and 7', followed by a formation of a BPSG insulating layer 14. *Id.*, col. 8:8-36.

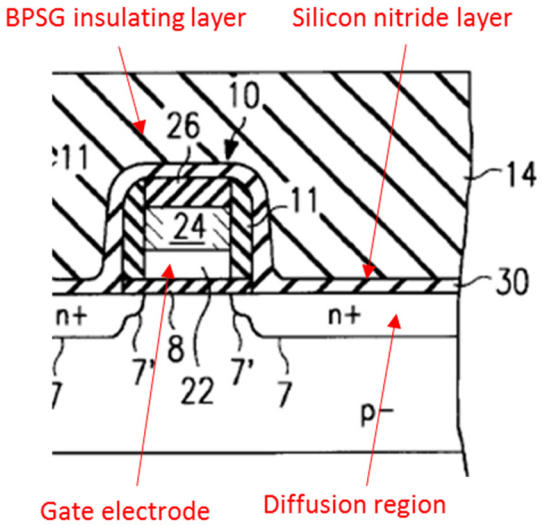


Fig. 3d, Doshi

Contact openings are then etched through the BPSG insulating layer 14 and the silicon nitride layer 30 ***using a two-step etch process***. *Id.*, Abstract and col. 9:25 – 10:16 (emphasis added). As disclosed in Doshi, the first etch selectively etches BPSG insulating layer 14 relative to the silicon nitride layer 30, and stops on the silicon nitride layer 30. *Id.* The second etch removes the silicon nitride layer 30. *Id.* Analogous to the teachings of the '997 patent and as shown in the following annotated version of Fig. 3g of Doshi, the second etch of silicon nitride in Doshi exposes the diffusion region 7 and simultaneously forms a spacer of silicon nitride 30 on the sidewall of the gate electrode structure 10.

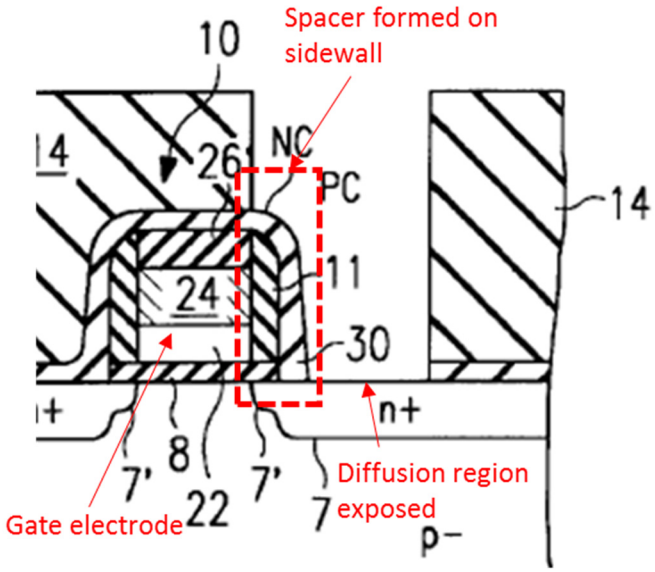


Fig. 3g, Doshi

Because Doshi describes the feature that justified allowance of independent claims 1 and 9 of the '997 patent, Doshi establishes a reasonable likelihood of prevailing on at least independent claims 1 and 9. As explained in greater detail below, Doshi includes all of the features of claims 1-14, and thus, establishing a reasonable likelihood that Petitioner will prevail in proving that claims 1-14 of the '997 patent are unpatentable over Doshi.

1. Doshi Anticipates Claim 1

Doshi discloses "*[a] A method for forming a self-aligned contact hole*," as recited in claim 1. *See* Ex. 1003, ¶ A-1. In particular, Doshi discloses that "[t]he present invention may be incorporated into the fabrication of an integrated circuit structure, and an integrated circuit structure so fabricated, by including a silicon nitride diffusion barrier layer underlying a planarizing doped oxide layer. The silicon

nitride layer is substantially conformal to structures such as gate structures and field isolation structures. ***Etching of contact openings through the combination of the doped oxide layer and the silicon nitride layer may be accomplished by way of a two-step process***." Ex. 1005, col. 4:10-18 (emphasis added). As disclosed in the '997 patent, "[s]elf-alignment is a technique in which multiple levels of regions on the wafer are formed using a single mask, thereby eliminating the alignment tolerance required by additional masks." Ex. 1001, col. 11-14. Since Doshi discloses etching contact openings through the combination of the doped oxide layer and the silicon nitride layer by way of a two-step process, Doshi disclose "*[a] A method for forming a self-aligned contact hole*," as recited in claim 1. *See* Ex. 1003, ¶ A-1.

Doshi discloses "*(a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon*," as recited in claim 1. *See* Ex. 1003, ¶¶ A-2 to A-3. Specifically, referring to the annotated Fig. 3a of Doshi below, Doshi discloses a p-type substrate 2, which is a semiconductor substrate. *Id*. Doshi further discloses a gate electrode formed on a semiconductor substrate. "Also in this example, ***gate structures 10*** are formed as layered structures, including polysilicon layer 22 in contact with gate oxide 8, tungsten silicide layer 24 overlying polysilicon layer 22, and silicon nitride layer 26 overlying tungsten silicide layer 24." Ex. 1005, col. 7:40-43. Doshi further discloses that source and drain regions, which

are diffusion regions, are formed on the semiconductor substrate. "Following definition of gate structures 10, ***light "reach-through" implants are performed*** in a self-aligned manner relative to gate structures 10 ***to define source/drain extensions 6' (for p-channel devices), 7' (for n-channel devices)***." Ex. 1005, col. 7:52-55 (emphasis added). "Following formation of sidewall filaments 11, ***source/drain implant and anneal is performed to form source/drain regions 6 (p+ type), 7 (n+ type). Source/drain regions 6, 7 are formed*** in a self-aligned manner relative to gate structures 10, in the conventional manner." *Id.* col. 7:66 – 8:3 (emphasis added).

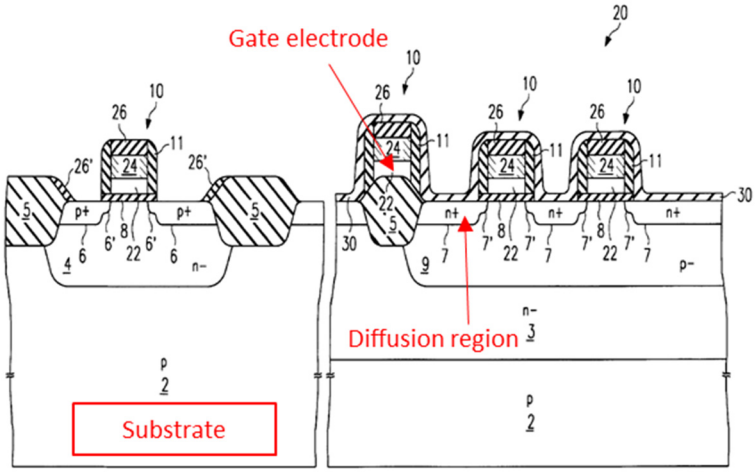


FIG. 3a

Doshi discloses "*(b) forming a conformal layer of etch barrier material overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode*," as recited in claim 1. *See* Ex. 1003, ¶¶ A-4 to A5. In particular, referring to the annotated Fig. 3b below, Doshi discloses that a conformal layer 30 of silicon nitride is formed overlying the surface

of substrate 2 including the source/drain diffusion regions and the upper surface and the sidewalls of the gate electrode. "According to the preferred embodiment of the invention, ***silicon nitride layer 30 is now formed overall***, preferably by way of low-pressure chemical vapor deposition (LPCVD), resulting in the structure illustrated in FIG. 3b." Ex. 1005, col. 8:8-11. Doshi further discloses that the silicon nitride layer 30 acts as an etch barrier, and therefore silicon nitride is an etch barrier material. "Contact openings (PC, BLC, CT) are etched through the BPSG layer (14) and the silicon nitride layer (30) using a two-step etch process. The first etch selectively etches silicon dioxide relative to silicon nitride, and thus stops on silicon nitride layer (30); besides ***serving as an etch stop***, silicon nitride layer (30) protects underlying active regions (6, 7) from damage that may be caused by ionized oxygen released during oxide etch." *Id.*, Abstract.

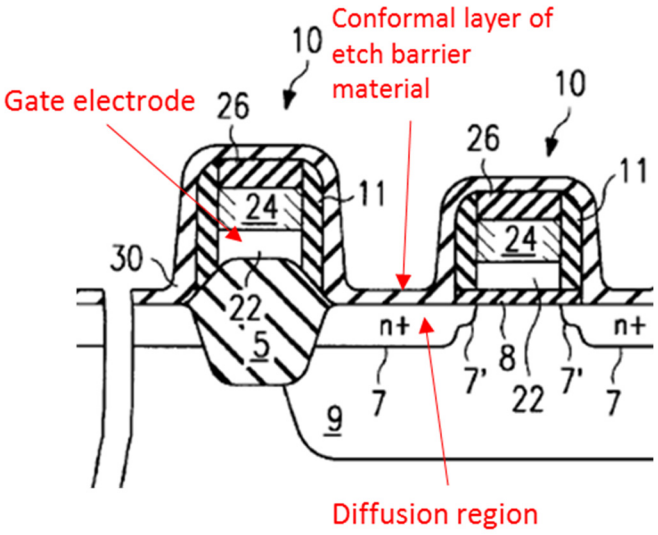


Fig. 3b, Doshi

Doshi discloses "*(c) forming an insulating layer overlying the barrier layer*," as recited in claim 1. *See* Ex. 1003, ¶¶ A-8 to A-9. In particular, referring to the annotated Fig. 3c below, Doshi discloses a deposition of a doped BPSG silicon dioxide layer 14 as an insulating layer over the silicon nitride barrier layer 30. "Referring now to FIG. 3c, integrated circuit 20 is illustrated after the deposition of doped BPSG silicon dioxide layer 14. BPSG layer 14 is preferably deposited in the conventional manner, for example by way of LPCVD, doped with both boron and phosphorous." Ex. 1005, col. 8:23-27.

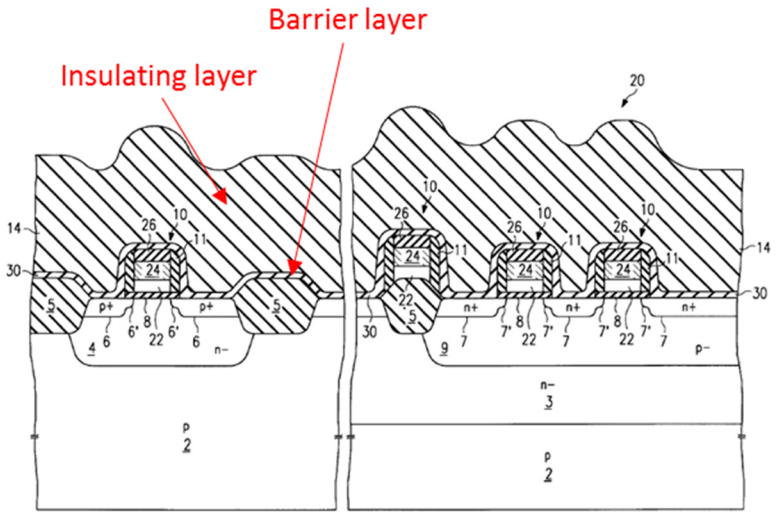


FIG. 3c

Doshi discloses "*(d) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop*," as recited in claim 1. *See* Ex. 1003, ¶¶ A-10 to A-11. In particular, referring to the annotated Fig. 3f below, Doshi discloses etching an opening through the BPSG layer 14 to the diffusion region 7 by using the silicon nitride layer 30 as an

etch stop. "According to this preferred embodiment of the present invention, etching of contact openings through BPSG layer 14 and nitride layer 30 is performed by way of a two-step etch. ***The first step is a "dry" etch of BPSG layer 14***, carried out in a plasma etch reactor as known in the art, a preferred example of which is the TEL DRM reactor. [. . .] Under these conditions, etching of BPSG layer 14 is relatively highly selective relative to etching of nitride layer 30, and as ***such the etch will tend to stop on nitride layer 30***." Ex. 1005, col. 9:34-50 (emphasis added).

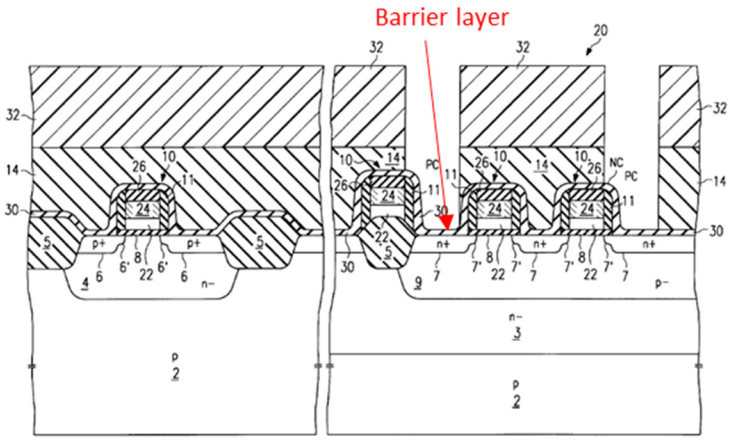


FIG. 3f

Doshi discloses the etching to the diffusion region as self-aligned and borderless. As discussed in Section III(C)(4), the '997 patent discloses that "[s]elf-alignment is a technique in which multiple levels of regions on the wafer are formed using a single mask, thereby eliminating the alignment tolerance required by additional masks." Ex. 1001, col. 11-14. Doshi discloses that "[c]ontact open-

ing locations are defined by way of conventional photolithography. FIG. 3e illustrates patterned photoresist layer 32, after exposure and development to define plug contact openings PC, at those locations where photoresist has been removed after development. ***The remaining portions of photoresist layer 32 serve, of course, as a mask for etch of the contact openings through BPSG layer 14 and nitride layer 30***." Ex. 1005, col. 9:26-33 (emphasis added). Accordingly, Doshi discloses "*etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop*," as recited in claim 1.

Doshi discloses "*(e) anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etch barrier material on the sidewall of the gate electrode*," as recited in claim 1. *See* Ex. 1003, ¶¶ A-12 to A-14. Specifically, Doshi discloses anisotropically etching the barrier layer underneath the opening. "Contact openings (PC, BLC, CT) are etched through the BPSG layer (14) and the silicon nitride layer (30) using a two-step etch process. The first etch selectively etches silicon dioxide relative to silicon nitride, and thus stops on silicon nitride layer (30); besides serving as an etch stop, silicon nitride layer (30) protects underlying active regions (6, 7) from damage that may be caused by ionized oxygen released during oxide etch. ***A brief nitride etch is then used to clear silicon nitride layer (30)***, without damaging

comer locations (NC) of the sidewall structures (11).” Ex. 1005, Abstract (emphasis added). “[T]he brief nitride etch used to clear nitride layer 30 from within plug contact locations PC has been observed to be ***highly anisotropic***.” *Id.*, col. 10:11-13 (emphasis added).

Referring to the annotated Fig. 3g of Doshi below, Doshi further discloses that the anisotropical etch of the barrier layer exposes the diffusion region and simultaneously forms a spacer of the etch barrier material on the sidewall of the gate electrode. Ex. 1003, ¶¶ A-13 to A-14. “FIG. 3g illustrates the construction of integrated circuit 20 after the completion of both etch steps, and the stripping of photoresist layer 32.” Ex. 1005, col. 9:65-67. Fig. 3g of Doshi illustrates that the diffusion region 7 has been exposed after the second etch. Ex. 1003, ¶¶ A-12 to A-13. Moreover, after the second etch, the silicon nitride layer 30 remained on the sidewall of the gate electrode 10 acts as a spacer, which provides a space as well as electrical insulation between the gate electrode 10 and the contact plug to be filled in the contact hole. Ex. 1003, ¶¶ A-13 to A-14.

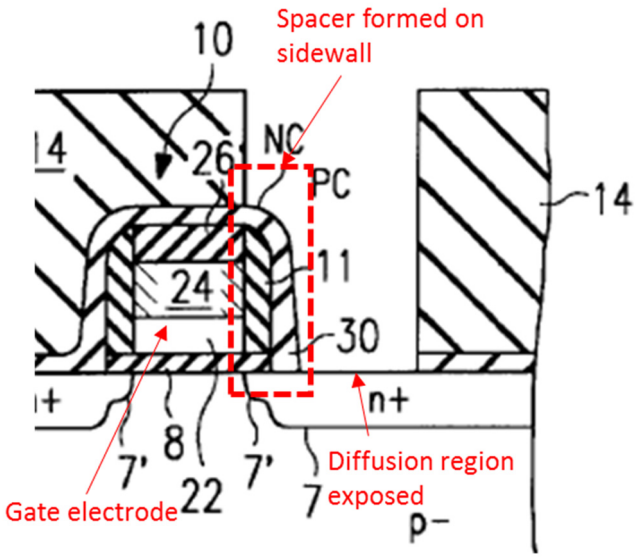


Fig. 3g, Doshi

2. Doshi Anticipates Claim 2

Doshi discloses "*forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode by thermal oxidation prior to forming the barrier layer*," as recited in claim 2. Ex. 1003, ¶¶ A-6 to A-7. In particular, Doshi discloses the formation of sidewall filaments 11, which are formed on the sidewalls of polysilicon layer 22 of the gate electrode by thermal oxidation. *Id.* "Following definition of gate structures 10, light "reach-through" implants are performed in a self-aligned manner relative to gate structures 10 to define source/drain extensions 6' (for p-channel devices), 7' (for n-channel devices), prior to the formation of sidewall filaments 11 along the sides of gate structures 10. According to the preferred embodiment of the invention, sidewall ***filaments 11 are formed by first oxidizing***

the sides of polysilicon layer 22." Ex. 1005, col. 7:52-59 (Emphasis added) Referring to the annotated Fig. 3b below, the barrier layer (i.e., the silicon nitride layer 30) is formed after the formation of the filaments 11, and therefore Doshi discloses forming an oxide layer on the sidewalls of the gate electrode by thermal oxidation prior to forming the barrier layer. Ex. 1003, ¶ A-6.

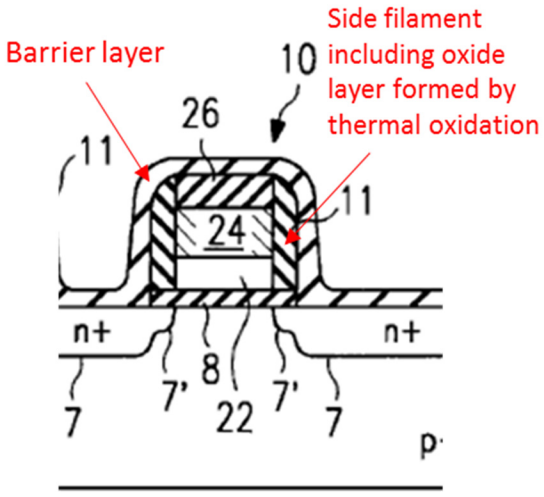


Fig. 3b, Doshi

Doshi further discloses forming an oxide layer over the diffusion region in at least two manners. First, as discussed in Section III(C)(2) and referring to the annotated Fig. 3b above, the side filament 11 is formed above the source/drain region 7', and illustrates that the oxide layer is formed *over* the diffusion region. Ex. 1003, ¶ A-7. Second, as Doshi discloses, the oxidation of the sidewall filaments 11 is performed right after the implantation of the source/drain extensions 6' and 7'. "Following definition of gate structures 10, light "reach-through" implants are performed in a self-aligned manner relative to gate structures 10 to define source/drain

extensions 6' (for p-channel devices), 7' (for n-channel devices), prior to the formation of sidewall filaments 11 along the sides of gate structures 10. According to the preferred embodiment of the invention, sidewall filaments 11 are formed by first oxidizing the sides of polysilicon layer 22." Ex. 1005, col. 7:52-59. Although not expressly disclosed in Doshi, during the thermal oxidation of the sides of polysilicon layer 22, thermal oxide is also formed over the source/drain regions because the source/drain regions are uncovered doped silicon, which is susceptible to thermal oxidation. Ex. 1003, ¶ A-7.

Accordingly, Doshi discloses "*forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode by thermal oxidation prior to forming the barrier layer*," as recited in claim 2.

3. Doshi Anticipates Claim 3

Doshi discloses that "*said gate electrode comprises a capping layer of silicon nitride*," as recited in claim 3. Ex. 1003, ¶ A-2. In particular, referring to the annotated Fig. 3a below, Doshi discloses that "gate structures 10 are formed as layered structures, including polysilicon layer 22 in contact with gate oxide 8, tungsten silicide layer 24 overlying polysilicon layer 22, and ***silicon nitride layer 26*** overlying tungsten silicide layer 24." Ex. 1005, col. 7:40-43 (emphasis added).

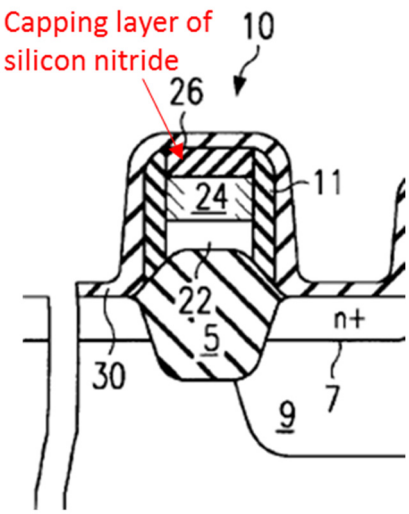


Fig. 3a, Doshi

4. Doshi Anticipates Claim 4

Doshi discloses that "*said barrier layer is a silicon nitride layer*," as recited in claim 4. Ex. 1003, ¶ A-4. Specifically, Doshi discloses that "[a]ccording to the preferred embodiment of the invention, ***silicon nitride layer 30*** is now formed overall, preferably by way of low-pressure chemical vapor deposition (LPCVD), resulting in the structure illustrated in FIG. 3b." Ex. 1005, col. 8:8-11 (emphasis added).

5. Doshi Anticipates Claim 5

Doshi discloses that "*said barrier layer has a thickness between about 100 to 500 Å*," as recited in claim 5, which depends on claim 4. Ex. 1003, ¶ A-5. In particular, Doshi discloses that "the thickness of nitride layer 30 may range from ***65Å to 250 Å***." Ex. 1005, col. 8:19-20 (emphasis added). *See also MPEP 2131.03(II) citing ClearValue Inc. v. Pearl River Polymers Inc.*, 668 F.3d 1340 at

1345 (Fed. Cir. 2012) (holding the claim anticipated because "there is no allegation of criticality or any evidence demonstrating any difference across the range.")

The '997 patent fails to demonstrate any criticality of the recited thickness between about 100 to 500 Å. In fact, the "about" language in claim 5 suggests that the thickness range is not critical. Moreover, the '997 patent discloses that "[t]he conformal layer 62 preferably has a thickness of about 100 to 500 Å, and more preferably has a thickness of about 200 to 350 Å," which further shows that the recited range is preferred, but not critical.

Accordingly, Doshi discloses that "*said barrier layer has a thickness between about 100 to 500 Å*," as recited in claim 5.

6. Doshi Anticipates Claim 6

Doshi discloses that "*said insulating layer comprises a layer of borophosphosilicate glass*," as recited in claim 6. Ex. 1003, ¶ A-8. Specifically, Doshi discloses that "[r]eferring now to FIG. 3c, integrated circuit 20 is illustrated after the deposition of ***doped BPSG silicon dioxide layer 14***. BPSG layer 14 is preferably deposited in the conventional manner, for example by way of LPCVD, doped with both boron and phosphorous" Ex. 1005, col. 8:23-27.

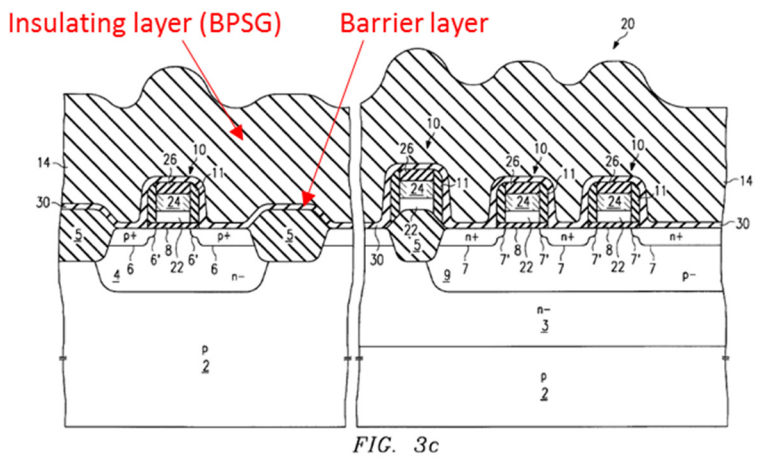


FIG. 3c

Doshi discloses that the insulating layer 14 is formed using BPSG, which is an acronym for borophosphosilicate glass. Ex. 1003, ¶ A-8. Accordingly, Doshi discloses that "said insulating layer comprises a layer of borophosphosilicate glass," as recited in claim 6.

7. Doshi Anticipates Claim 7

Doshi discloses "*depositing an insulating layer overlying the barrier layer*." Ex. 1003, ¶ A-9. In particular, Doshi discloses depositing a BPSG layer 14 above the silicon nitride layer 30. "A silicon nitride layer (30) is in place below the BPSG layer (14), and serves as a barrier to the diffusion of boron and phosphorous from the BPSG layer (14) during high temperature processes such as reflow and densification of the BPSG layer (14) itself." Ex. 1005, Abstract.

Doshi discloses "*planarizing the insulating layer*." Ex. 1003, ¶ A-9. Specifically, Doshi discloses that "[f]ollowing deposition and anneal [of the BPSG layer 14], ***a planarization etchback of BPSG layer 14 is performed*** according to this

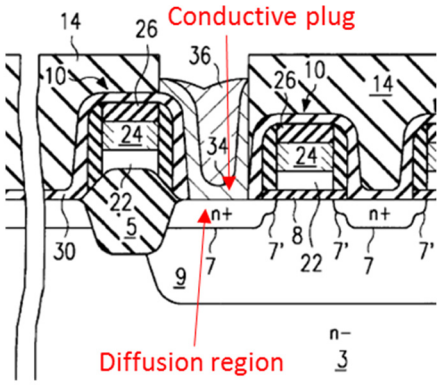
preferred embodiment of the invention. This etchback is performed without patterning, and is preferably a timed etch selected so that BPSG layer 14 remains over the top of all underlying structures." Ex. 1005, col. 8:66 – 9:4 (emphasis added).

Accordingly, Doshi discloses "*depositing an insulating layer overlying the barrier layer*" and "*planarizing the insulating layer*," as recited in claim 7.

8. Doshi Anticipates Claim 8

Doshi discloses "*forming a conductive plug in said opening to electrically connect to the diffusion region*," as recited in claim 8. Ex. 1003, ¶ A-15. In particular, referring to the annotated Fig. 3h of Doshi below, Doshi discloses that "[f]ollowing definition of plug contact openings PC, ***polysilicon plugs are formed*** therewithin, ***in contact with source/drain regions 7***." Ex. 1005, col. 10:17-19 (emphasis added).

Fig. 3h, Doshi



9. Doshi Anticipates Claim 9

The following lookup table below summarizes the proposed Doshi-based ground of anticipation rejections for claim 9, for the same reasons as set forth above in the referenced claims and argument sections.

Claims/ Recited Limitations	**Corresponding Claim(s)/ Recited Limitations**	**Corresponding Argument Section(s)**
Claim 9: "[a] method for forming a self-aligned contact hole."	Claim 1: "[a] method for forming a self-aligned contact hole."	Section V(A)(1)
Claim 9: "(a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon, said gate electrode comprising a capping layer."	Claim 1: "(a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon." Claim 3: "said gate electrode comprises a capping layer of silicon nitride."	Section V(A)(1) Section V(A)(3)
Claim 9: "(b) forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode by thermal oxidation."	Claim 2: "forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode by thermal oxidation prior to forming the barrier layer."	Section V(A)(2)
Claim 9: "(c) forming a conformal layer of silicon nitride overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode."	Claim 1: "(b) forming a conformal layer of etch barrier material overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode." Claim 4: "said barrier layer is a silicon nitride layer."	Section V(A)(1) Section V(A)(4)
Claim 9: "(d) forming an insulating layer overlying the conformal layer of silicon nitride."	Claim 1: "(c) forming an insulating layer overlying the barrier layer."	Section V(A)(1) Section V(A)(4)

	Claim 4: "said barrier layer is a silicon nitride layer."	
Claim 9: "(e) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the silicon nitride layer as an etch stop."	Claim 1: "(d) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop." Claim 4: "said barrier layer is a silicon nitride layer."	Section V(A)(1) Section V(A)(4)
Claim 9: "(e) anisotropically etching the silicon nitride layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of silicon nitride on the sidewall of the gate electrode."	Claim 1: "(e) anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etch barrier material on the sidewall of the gate electrode." Claim 4: "said barrier layer is a silicon nitride layer."	Section V(A)(1) Section V(A)(4)

Accordingly, for the reasons as set forth, Doshi anticipates claim 9.

10. Doshi Anticipates Claims 10-14

The table below summarizes the proposed Doshi-based ground of anticipation rejections for claims 10-14, for the same reasons as set forth above in the referenced claims and argument sections.

Claims/ Recited Limitations	**Corresponding Claim(s)/ Recited Limitations**	**Corresponding Argument Section(s)**
Claim 10: "said capping layer is a silicon nitride layer"	Claim 3: "said gate electrode comprises a capping layer of silicon nitride"	Section V(A)(3)

Claim 11: "said conformal layer of silicon nitride has a thickness between about 100 to 500 Å."	Claim 4: "said barrier layer is a silicon nitride layer." Claim 5: "said barrier layer has a thickness between about 100 to 500 Å."	Section V(A)(4) Section V(A)(5)
Claim 12: "said insulating layer comprises a layer of borophosphosilicate glass."	Claim 6: "said insulating layer comprises a layer of borophosphosilicate glass."	Section V(A)(6)
Claim 13: "depositing an insulating layer overlying the conformal layer of silicon nitride," and "planarizing the insulating layer."	Claim 4: "said barrier layer is a silicon nitride layer." Claim 7: "depositing an insulating layer overlying the barrier layer," and "planarizing the insulating layer."	Section V(A)(4) Section V(A)(7)
Claim 14: "forming a conductive plug in said opening to electrically connect to the diffusion region."	Claim 8: "forming a conductive plug in said opening to electrically connect to the diffusion region."	Section V(A)(8)

B. Becker Anticipates Claims 1 and 3-8

Becker discloses "[a]n etch process that uses a single partially etched spacer insulating layer to form both sidewall spacers and a diffusion barrier that protect areas of the substrate during subsequent processing steps in the formation of semiconductor devices". Ex. 1006, Abstract. According to Becker, gate electrodes 18 and p-type diffusion regions 28 are fabricated on a semiconductor substrate 12. *Id.*, col. 4:9-45. As shown in the following annotated version of Fig. 1 of Becker, a conformal layer of silicon nitride 30 is deposited over the gate electrodes 18 and the source/drain diffusion regions 28. *Id.*, col. 4:46 – 5:5.

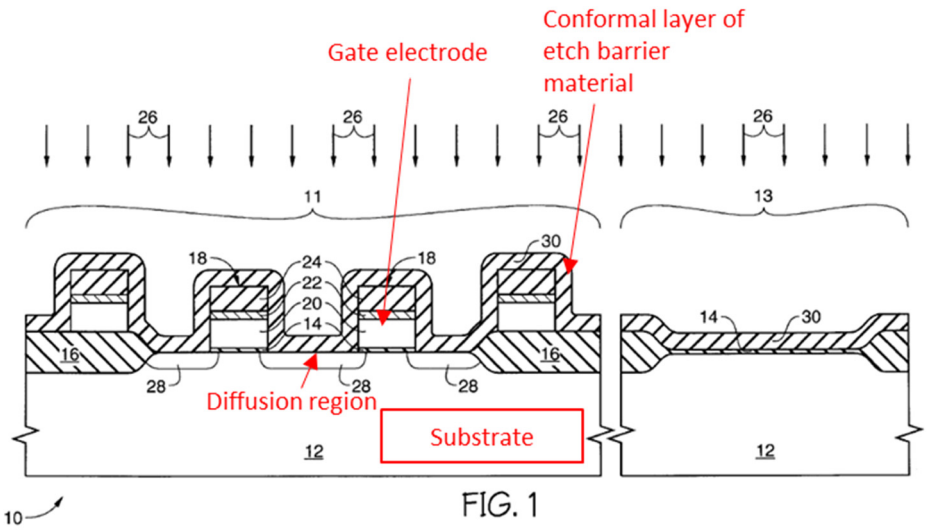


FIG. 1

As shown in the annotated Fig. 3 of Becker below, the silicon nitride layer 30 is thinned down by an anisotropic etch, and is used as a diffusion barrier to form n-type lightly doped drain source/drain regions 32a and 32b. *Id.*, col. 5:6-18.

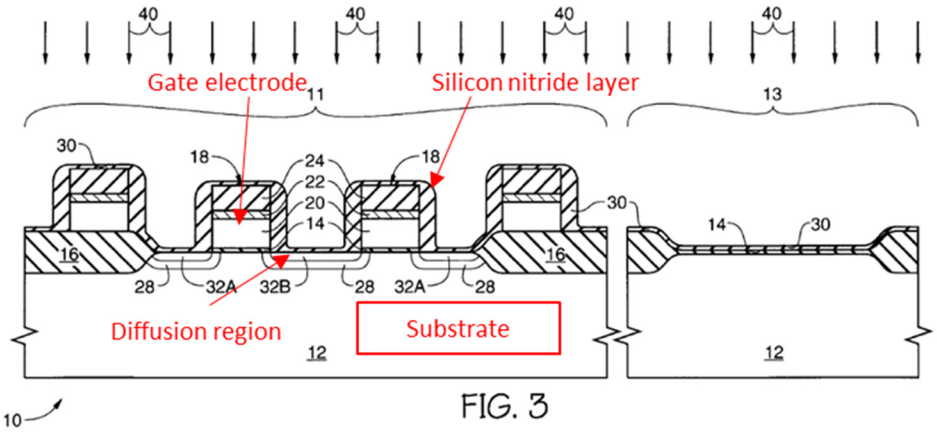


FIG. 3

A planarized BPSG insulating layer 36 is then formed over the silicon nitride layer 30, and contact openings 38 are formed by first etching through the BPSG insulating layer 36 using a dry etch that is ***selective to the silicon nitride layer 36***, which stops on the silicon nitride layer 36. *Id.*, col. 5:19-30. A second

anisotropic etch is performed to remove the silicon nitride layer 36. *Id.*, col. 5:30-39. Analogous to the teachings of the '997 patent and as shown in the following annotated version of Fig. 4 of Becker, the second anisotropic etch of silicon nitride in Becker exposes the diffusion regions 28 and simultaneously forms a spacer of silicon nitride 34 on the sidewall of the gate electrode 18.

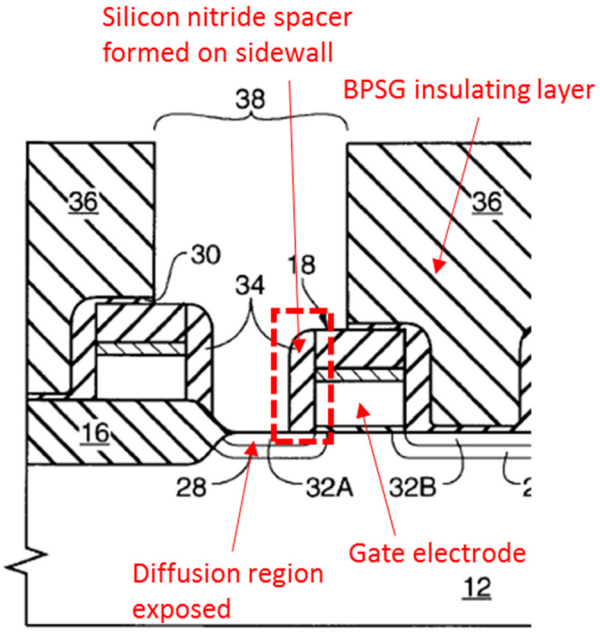


Fig. 4, Becker

Because Becker describes the feature that justified allowance of independent claim 1 of the '997 patent, Becker establishes a reasonable likelihood of prevailing on at least independent claim 1. As explained in greater detail below, Becker includes all of the features of claims 1, 3, 4, and 6-8, and thus, establishing a reasonable likelihood that Petitioner will prevail in proving that claims 1, 3-8 of the '997 patent are unpatentable over Becker.

1. Becker Anticipates Claim 1

Becker discloses "*[a] A method for forming a self-aligned contact hole*," as recited in claim 1. *See* Ex. 1003, ¶ B-1. In particular, Becker discloses a two-step etch using a single mask. "Another aspect of the invention provides a process for making a dynamic random access memory cell. This DRAM fabrication process includes the steps of: [. . .] e. ***etching the lower [BPSG] insulating layer*** to form a capacitor container over the first source/drain region and to expose the [silicon nitride] spacer insulating layer over the first source/drain region; f. ***etching the exposed portion of the [silicon nitride] spacer insulating layer*** to expose the first source/drain region." Ex. 1006, col. 2:30-51 (emphasis added). As disclosed in the '997 patent, "[s]elf-alignment is a technique in which multiple levels of regions on the wafer are formed using a single mask, thereby eliminating the alignment tolerance required by additional masks." Ex. 1001, col. 11-14. Since Becker discloses etching contact openings through the combination of the BPSG insulating layer and the silicon nitride layer by way of a two-step process, Becker disclose "*[a] A method for forming a self-aligned contact hole*," as recited in claim 1. *See* Ex. 1003, ¶ B-1.

Becker discloses "*(a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon*," as recited in claim 1. *See* Ex. 1003, ¶¶ B-2 to B-3. Specifically, referring to the annotated Fig. 2 of Becker below, Becker

discloses a lightly doped p-type silicon substrate 12, which is a semiconductor substrate. *Id*. Becker further discloses a gate electrode 18 formed on a semiconductor substrate. "***Transistor gate electrode 18 is formed*** by successively depositing or "stacking" layers of polysilicon 20, tungsten silicide 22 and silicon nitride 24 over thin gate insulating layer 14, and then patterning and etching those layers to expose substrate 12 at the desired locations of the source and drain for the access transistors." Ex. 1006, col. 4:22-27 (emphasis added). Becker further discloses that doped p-type regions 28, which are diffusion regions, are formed on the semiconductor substrate 12. "P-type impurities, typically boron atoms, are then implanted into the exposed portions of substrate 12, as shown symbolically by arrows 26. Boron ions are implanted at an energy level of approximately of 25-50 KeV, to a depth of approximately 1000 angstroms. The ***resulting doped p-regions 28*** extend into the channel area between the subsequently formed source and drain for each access transistor." Ex. 1006, col. 4:36-42, (emphasis added). The doped p-region 28 is a diffusion region. Ex. 1003, ¶¶ B-2 to B-3.

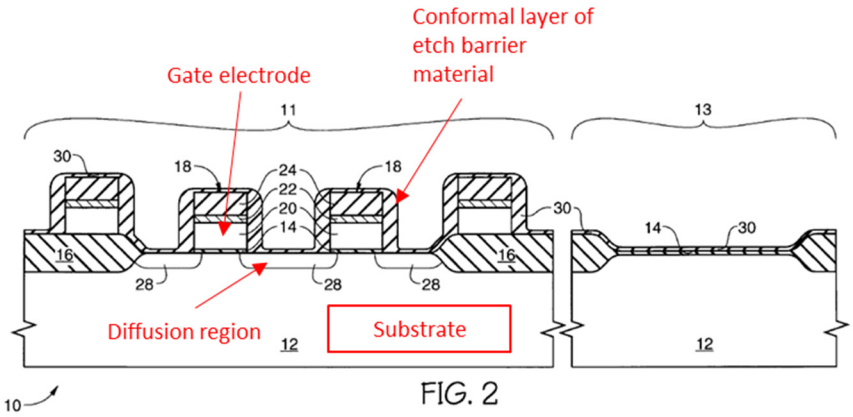


FIG. 2

Becker discloses "*(b) forming a conformal layer of etch barrier material overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode*," as recited in claim 1. *See* Ex. 1003, ¶¶ B-4 to B6. In particular, referring to the annotated Fig. 2 above, Becker discloses that a conformal layer 30 of silicon nitride is formed overlying the surface of substrate 12 including the p-doped diffusion regions 28 and the upper surface and the sidewalls of the gate electrode 18. "***A spacer insulating layer 30 is then deposited*** over the in process structure to a thickness typically in the range of 600 angstroms to 2,000 angstroms." Ex. 1006, col. 4:46-48. Becker further discloses that the silicon nitride layer 30 acts as an etch barrier, and therefore silicon nitride is an etch barrier material. "Spacer insulating layer 30 is preferably made of silicon nitride or other suitable insulating material that is ***selectively etchable with respect to oxide materials***." *Id.*, col. 4:51-54.

Becker discloses "*(c) forming an insulating layer overlying the barrier layer*," as recited in claim 1. *See* Ex. 1003, ¶ B-7. In particular, referring to the annotated Fig. 4 below, Becker discloses a deposition of a BPSG silicon dioxide layer 36 as an insulating layer over the silicon nitride barrier layer 30. "Referring to FIG. 4, a thick lower insulating layer 36, preferably made of borophospho-silicate glass (BPSG), is deposited and, if necessary, planarized." Ex. 1006, col. 5:19-21.

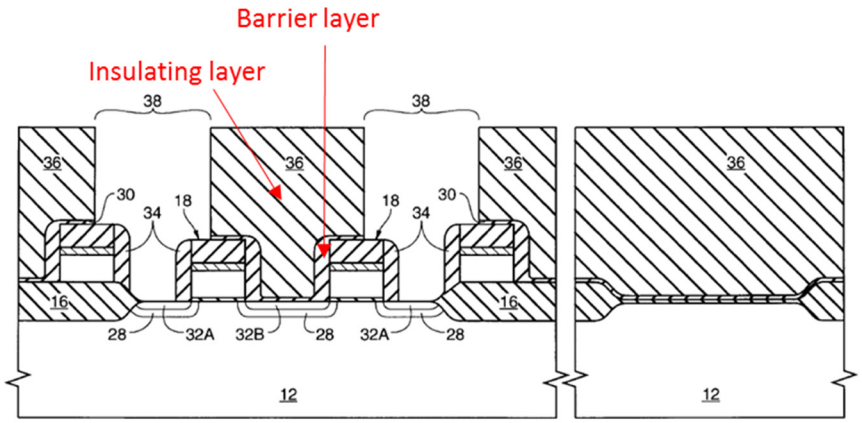


FIG. 4

Becker discloses "*(d) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop*," as recited in claim 1. *See* Ex. 1003, ¶¶ B-8 to B-9. In particular, Becker discloses etching an opening through the BPSG insulating layer 36 to the diffusion region 28 by using the silicon nitride layer 30 as an etch stop. "***Lower insulating layer 36 is patterned and etched*** to define capacitor contact corridors 38 (also commonly referred to as the capacitor containers) in lower insulating layer 36. The etch of lower insulating layer 36 utilizes a oxide etch process that is ***selective to silicon nitride to protect spacer insulating layer 30*** during any over etch of lower insulating layer 36." Ex. 1006, col. 5:21-27 (emphasis added).

Becker discloses the etching to the diffusion region as self-aligned and borderless. As discussed in Section III(C)(4), the '997 patent discloses that "[s]elf-alignment is a technique in which multiple levels of regions on the wafer are formed using a single mask, thereby eliminating the alignment tolerance required

by additional masks." Ex. 1001, col. 11-14. Becker discloses "a process for making a dynamic random access memory cell. This DRAM fabrication process includes the steps of: [. . .] e. ***etching the lower [BPSG] insulating layer*** to form a capacitor container over the first source/drain region and to expose the [silicon nitride] spacer insulating layer over the first source/drain region; f. ***etching the exposed portion of the [silicon nitride] spacer insulating layer*** to expose the first source/drain region." Ex. 1006, Abstract (emphasis added). Becker discloses two levels of regions formed using a single mask. Ex. 1003, ¶ B-9. Accordingly, Becker discloses "*etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop*," as recited in claim 1.

Becker discloses "*(e) anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etch barrier material on the sidewall of the gate electrode*," as recited in claim 1. *See* Ex. 1003, ¶ B-10. Specifically, referring to the annotated Fig. 4 of Becker below, Becker discloses that "[a]fter lower insulating layer 36 has been completely removed from source/drain regions 32a, the ***etch chemistry is changed to remove the remainder of spacer insulating layer 30 and thereby expose source/drain regions 32a***. This etch of the remainder of spacer insulating layer 30 ***produces the same spacer 34 profile*** as conventional processes." Ex. 1006, col.

5:32-38 (emphasis added). "[T]he spacer insulating layer is ***anisotropically etched*** to form substantially vertical spacers along sidewalls of the gate electrodes." *Id.*, claim 11 (emphasis added).

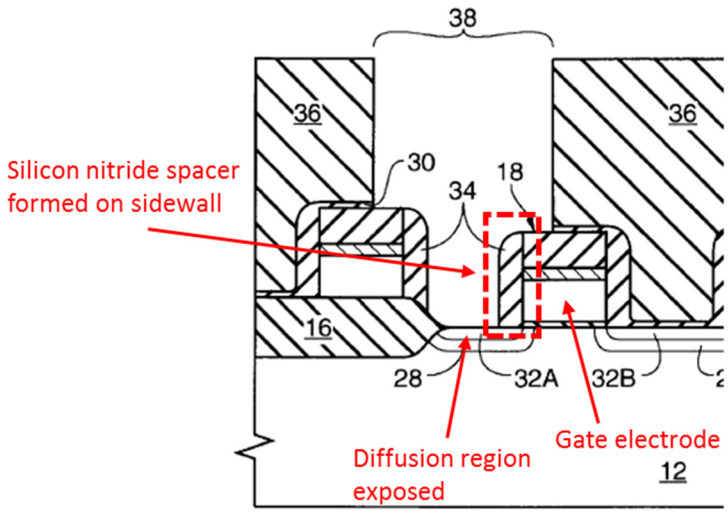


Fig. 4, Becker

Accordingly, for the reasons set forth above, Becker anticipates claim 1.

2. Becker Anticipates Claim 3

Becker discloses that "*said gate electrode comprises a capping layer of silicon nitride*," as recited in claim 3. Ex. 1003, ¶ B-2. In particular, referring to the annotated Fig. 2 below, Becker discloses that "Transistor gate electrode 18 is formed by successively depositing or "stacking" layers of polysilicon 20, tungsten silicide 22 and ***silicon nitride 24*** over thin gate insulating layer 14, and then patterning and etching those layers to expose substrate 12 at the desired locations of the source and drain for the access transistors." Ex. 1006, col. 4:22-27 (emphasis added)

Accordingly, Becker anticipates claim 3.

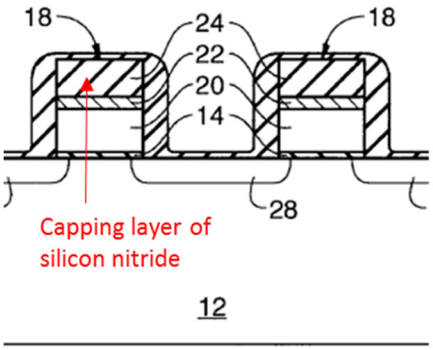


Fig. 2, Becker

3. Becker Anticipates Claim 4

Becker discloses that "*said barrier layer is a silicon nitride layer*," as recited in claim 4. Ex. 1003, ¶ B-4. Specifically, Becker discloses that "***[s]pacer insulating layer 30 is preferably made of silicon nitride*** or other suitable insulating material that is selectively etchable with respect to oxide materials." *Id.*, col. 4:51-54.

Accordingly, Becker anticipates claim 4.

4. Becker Anticipates Claim 5

Becker discloses that "*said barrier layer has a thickness between about 100 to 500 Å*," as recited in claim 5, which depends on claim 4. Ex. 1003, ¶ B-5. In particular, Becker discloses that "[a] spacer insulating layer 30 is then deposited over the in process structure to a thickness typically in the range of 600 angstroms to 2,000 angstroms. [. . .] In conventional processes, the horizontal portions of spacer insulating layer 30 would now be etched completely to form spacers along

the sidewalls of gate electrodes 18 and to expose thin gate oxide 14 and the underlying contact regions 28 in substrate 12. By contrast, according to the present invention, ***spacer insulating layer 30 is patterned and etched to a thickness in the range of 50 angstroms to 400 angstroms, preferably about 100 angstroms***, as shown in FIG. 2." Ex. 1006, col. 4:46-62 (emphasis added).

Referring to the annotated Fig. 2 below, Becker discloses that after an anisotropic etch to thin down the silicon nitride etch barrier layer 30, the thickness of the silicon nitride etch barrier layer is in the range of 50 angstroms to 400 angstroms, preferably about 100 angstroms. *Id.*; *see also* Ex. 1003, ¶ B-5. The preferred thickness of 100 angstroms anticipates the recited thickness range of "between about 100 to 500 Å." *See MPEP 2103.03(I)* ("A SPECIFIC EXAMPLE IN THE PRIOR ART WHICH IS WITHIN A CLAIMED RANGE ANTICIPATES THE RANGE"); *see also Titanium Metals Corp. of America v. Banner*, 778 F.2d 775, 782 (Fed.Cir.1985) (holding that "when, as by a recitation of ranges or otherwise, a claim covers several compositions, the claim is 'anticipated' if one of them is in the prior art.")

Moreover, the thickness range of 50 angstroms to 400 angstroms anticipates the recited thickness range of "between about 100 to 500 Å." *See MPEP 2131.03(II) citing ClearValue Inc. v. Pearl River Polymers Inc.*, 668 F.3d 1340 at 1345 (Fed. Cir. 2012) (holding the claim anticipated because "there is no allegation

of criticality or any evidence demonstrating any difference across the range.") The '997 patent fails to demonstrate any criticality of the recited thickness between about 100 to 500 Å. In fact, the "about" language in claim 5 suggests that the thickness range is not critical. In addition, the '997 patent discloses that "[t]he conformal layer 62 preferably has a thickness of about 100 to 500 Å, and more preferably has a thickness of about 200 to 350 Å," which further shows that the recited range is preferred, but not critical.

Accordingly, for the reasons set forth above, Becker discloses that "*said barrier layer has a thickness between about 100 to 500 Å*," as recited in claim 5. Becker therefore anticipates claim 5.

5. Becker Anticipates Claim 6

Becker discloses that "*said insulating layer comprises a layer of borophosphosilicate glass*," as recited in claim 6. Ex. 1003, ¶ B-7. Specifically, Becker discloses that "a thick lower insulating layer 36, preferably made of ***borophosphosilicate glass*** (BPSG), is deposited and, if necessary, planarized." Ex. 1006, col. 5:19-21." Ex. 1006, col. 5:19-21 (emphasis added).

Accordingly, Becker anticipates claim 6.

6. Becker Anticipates Claim 7

Becker discloses "*depositing an insulating layer overlying the barrier layer*," and "*planarizing the insulating layer*," as recited in claim 7. Ex. 1003, ¶ B-

7. In particular, Becker discloses depositing a BPSG layer 36 above the silicon nitride layer 30. "Referring to FIG. 4, ***a thick lower insulating layer 36, preferably made of borophosphosilicate glass*** (BPSG), is deposited and, if necessary, ***planarized***." Ex. 1006, col. 5:19-21." Ex. 1006, col. 5:19-21 (emphasis added).

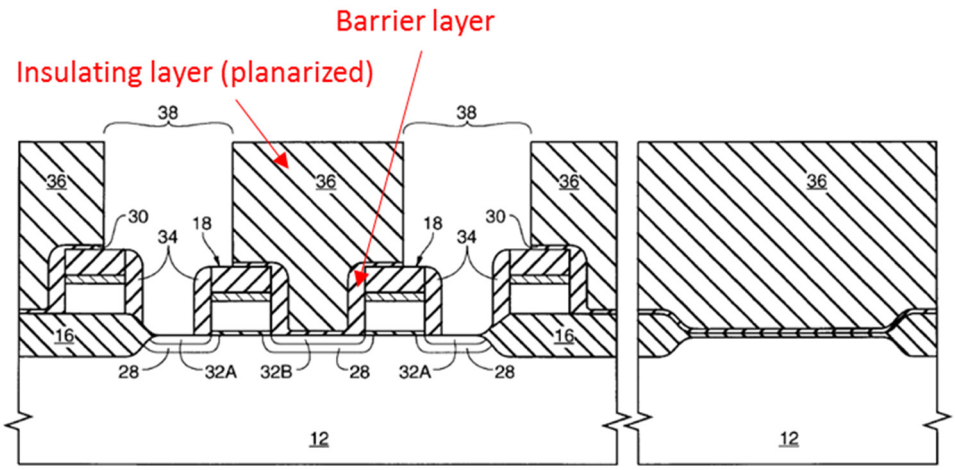


FIG. 4

Accordingly, Becker anticipates claim 7.

7. Becker Anticipates Claim 8

Becker discloses "*forming a conductive plug in said opening to electrically connect to the diffusion region*," as recited in claim 8. Ex. 1003, ¶ B-11. In particular, referring to the annotated Fig. 6 of Becker below, Becker discloses that "storage poly 42 is patterned and etched or subjected to a chemical mechanical polish (CMP) to ***form capacitor first conductors 44***." Ex. 1006, col. 5:45-48 (emphasis added). The capacitor first conductors 44 constitute a conductive plug that electrically connects to the diffusion region. Ex. 1003, ¶ B-11. That is, the conductors 44 are conductive plugs in that they are conductive and plug the contact corridors 38

by virtue of covering the interface between the corridors 38 and the source/drain diffusion regions 32A, thereby providing electrically connectivity. *Id.*

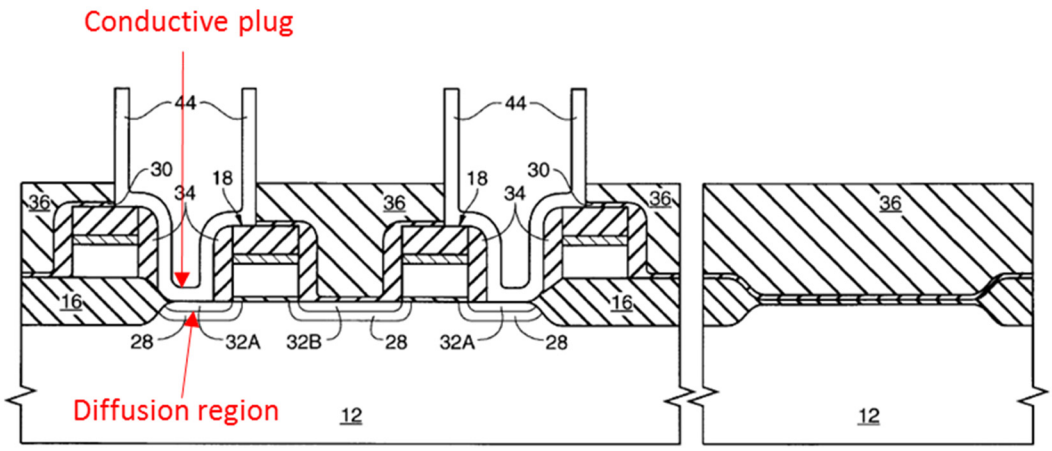


FIG. 6

C. Becker in View of Wong Renders Obvious Claims 2 and 9-14

Wong is a non-patent publication titled "Process Induced Degradation of Thin Oxides," published in 1987 in the Proceedings of the First International Symposium on ULSI Science and Technology by the Electrochemical Society. Ex. 1009, pp. 1-3. The Electrochemical Society is a leading international nonprofit organization founded in 1902 for professionals in the electrochemical and solid-state science and technology fields. Ex. 1003, ¶ B-12.

Wong's paper investigates the integrity degradations of the thin gate oxide during post-oxidation processing. Ex. 1009, p. 3. According to Wong, the reactive ion etch (RIE) process used to define the polysilicon gate structure increases the defect density of the thin oxide, and decreases the yield of fabricated devices. *Id.*,

pp. 3, 5, 6. As described by Wong, a reoxidation of polysilicon gate sidewall using thermal oxidation reduces the defect density in the thin oxide and therefore improves the yield of the fabricated devices. *Id.* Becker discloses forming a thin gate insulating layer 14 and then forming a stack of gate electrode layers on the gate insulating layer 14. Ex. 1006, col. 4:9-35. The stack of gate electrode layers includes a polysilicon layer 20. *Id.* Transistor gate electrode 18 is formed by patterning and etching the stack of gate electrode layers using "conventional methods well known in the art." *Id.* Persons of skill would have readily recognized that a conventional method for etching the stack of gate electrode layers is RIE. Ex. 1003, ¶ B-14. Having read Wong, persons of skill would therefore have recognized that after the RIE etch, defects may be created in the gate oxide that would decrease the device yield. *Id.* Persons of skill also would have readily recognized the benefit of applying the reoxidation of polysilicon sidewalls of the gate as described in Wong to form an oxide layer on the polysilicon layer 20 in Becker by a thermal oxidation to help improve the device yield in Becker. *Id.*

1. Becker in View of Wong Renders Claim 2 Obvious

Becker does not appear to expressly disclose "*forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode by thermal oxidation prior to forming the barrier layer*," as recited in claim 2. Becker discloses forming a transistor gate electrode 18 by etching a stack of gate electrode materials on a

thin gate oxide. Referring to the annotated Fig. 1 of Becker below, "wafer 10 comprises a lightly doped p-type single crystal silicon substrate 12 which has been oxidized to form thin gate insulating layer 14 and thick field oxide regions 16. [. . .] Transistor gate electrode 18 is formed by successively depositing or "stacking" layers of ***polysilicon 20***, tungsten silicide 22 and silicon nitride 24 over thin gate insulating layer 14, and then patterning and etching those layers to expose substrate 12 at the desired locations of the source and drain for the access transistors. These layers, which are deposited and patterned and ***etched using conventional methods well known in the art***, are also typically removed in much of the periphery, as shown in FIG. 1." Ex. 1006, col. 4:9-30 (emphasis added).

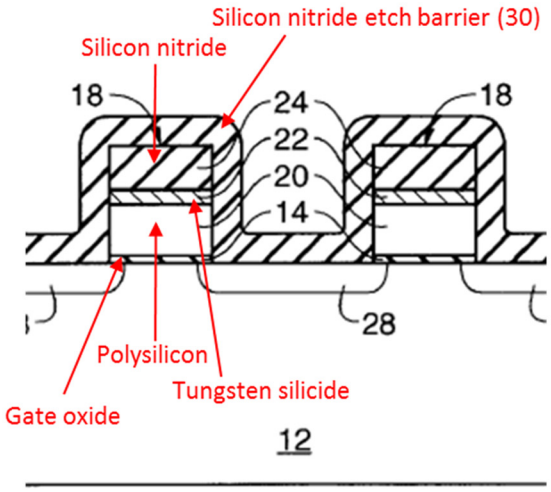


Fig. 1, Becker

Wong's paper investigates the integrity degradations of the thin gate oxide during post-oxidation processing. Ex. 1009, p. 3. According to Wong, the reactive ion etch (RIE) process used to define the polysilicon gate structure increases the

defect density of the thin oxide, and decreases the yield of fabricated devices. *Id.*, pp. 3, 5, 6. As described by Wong, a reoxidation of polysilicon gate sidewall using thermal oxidation reduces the defect density in the thin oxide and therefore improves the yield of the fabricated devices. *Id.* Specifically, referring to Table III of Wong below, with a gate oxide thickness of 12.5 nm, the yield of good capacitor after a polysilicon gate etch without reoxidation is 83%. By growing 104 nm of oxide on the polysilicon sidewall using thermal oxidation, the yield is improved to 95%. Similarly, with a gate oxide thickness of 22.5 nm, the yield of good capacitor after a polysilicon gate etch without reoxidation is 83%. By growing 52 nm of oxide on the polysilicon sidewall using thermal oxidation, the yield is improved to 98%. *Id.; see also* Ex. 1003, ¶ B-13.

TABLE III: PERCENT GOOD CAPACITOR[1] AFTER REOXIDATION OF POLYSILICON SIDEWALL USING RIE DEFINED GATE STRUCTURE[2]

Gate Oxide (nm)	Polysilicon Oxide Sidewall (nm)		
	None	52	104
12.5	83%	90%	95%
22.5	83%	98%	-

Persons of skill would have readily recognized that a conventional method for etching the stack of gate electrode layers in Becker is through a reactive ion etch. Ex. 1003, ¶ B-14. Having read Wong, persons of skill would have recognized that after the RIE etch, defects would be created in the gate oxide, affecting

the device yield. *Id.* Persons of skill, therefore, would have readily appreciated the benefit of improving the device yield, by applying a reoxidation of the polysilicon sidewall as described in Wong to form an oxide layer on the polysilicon gate electrode layer 20 in Becker using thermal oxidation after the etching of the gate electrode 18 and prior to the deposition of the silicon nitride etch barrier layer 30 in Becker. *Id.*

Moreover, persons of skills would have readily recognized that the formation of an oxide layer on the polysilicon gate electrode layer 20 in Becker by a thermal oxidation would also form an oxide layer over the p-doped diffusion region 28. Ex. 1003, ¶ B-15. Specifically, if the gate oxide over the p-doped diffusion region 28 had been removed prior to the thermal oxidation, the p-doped diffusion region 28 is uncovered doped silicon, and is susceptible to thermal oxidation. *Id*. If the gate oxide were still present prior to the thermal oxidation, the gate oxide would grow thicker during oxidation of the polysilicon gate sidewall, again forming thermal oxide over the p-doped diffusion region 28 during oxidation of the gate polysilicon sidewall. *Id.*

Accordingly, Becker in view of Wong discloses "*forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode by thermal oxidation prior to forming the barrier layer*," as recited in claim 2. Therefore Becker in view of Wong renders claim 2 obvious.

2. Becker in View of Wong Renders Claim 9 Obvious

The lookup table below summarizes the proposed Becker-based ground of obviousness rejections for claim 9, for the same reasons as set forth above in the referenced claims and argument sections.

Claims/ Recited Limitations	**Corresponding Claim(s)/ Recited Limitations**	**Corresponding Argument Section(s)**
Claim 9: "[a] method for forming a self-aligned contact hole."	Claim 1: "[a] method for forming a self-aligned contact hole."	Section V(B)(1)
Claim 9: "(a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon, said gate electrode comprising a capping layer."	Claim 1: "(a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon." Claim 3: "said gate electrode comprises a capping layer of silicon nitride."	Section V(B)(1) Section V(B)(3)
Claim 9: "(b) forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode by thermal oxidation."	Claim 2: "forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode by thermal oxidation prior to forming the barrier layer."	Section V(C)(1)
Claim 9: "(c) forming a conformal layer of silicon nitride overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode."	Claim 1: "(b) forming a conformal layer of etch barrier material overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode." Claim 4: "said barrier layer is a silicon nitride layer."	Section V(B)(1) Section V(B)(3)

Claim 9: "(d) forming an insulating layer overlying the conformal layer of silicon nitride."	Claim 1: "(c) forming an insulating layer overlying the barrier layer." Claim 4: "said barrier layer is a silicon nitride layer."	Section V(B)(1) Section V(B)(3)
Claim 9: "(e) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the silicon nitride layer as an etch stop."	Claim 1: "(d) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop." Claim 4: "said barrier layer is a silicon nitride layer."	Section V(B)(1) Section V(B)(3)
Claim 9: "(e) anisotropically etching the silicon nitride layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of silicon nitride on the sidewall of the gate electrode."	Claim 1: "(e) anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etch barrier material on the sidewall of the gate electrode." Claim 4: "said barrier layer is a silicon nitride layer."	Section V(B)(1) Section V(B)(3)

Accordingly, for the reasons as set forth, Becker in view of Wong renders claim 9 obvious.

3. Becker in View of Wong Renders Claims 10-14 Obvious

The lookup table below summarizes the proposed Becker-based ground of obviousness rejections for claims 10-14, for the same reasons as set forth above in the referenced claims and argument sections.

Claims/ Recited Limitations	**Corresponding Claim(s)/ Recited Limitations**	**Corresponding Argument Section(s)**
Claim 10: "said capping layer is a silicon nitride layer"	Claim 3: "said gate electrode comprises a capping layer of silicon nitride"	Section V(B)(2)
Claim 11: "said conformal layer of silicon nitride has a thickness between about 100 to 500 Å."	Claim 4: "said barrier layer is a silicon nitride layer." Claim 5: "said barrier layer has a thickness between about 100 to 500 Å."	Section V(B)(3) Section V(B)(4)
Claim 12: "said insulating layer comprises a layer of borophosphosilicate glass."	Claim 6: "said insulating layer comprises a layer of borophosphosilicate glass."	Section V(B)(5)
Claim 13: "depositing an insulating layer overlying the conformal layer of silicon nitride," and "planarizing the insulating layer."	Claim 4: "said barrier layer is a silicon nitride layer." Claim 7: "depositing an insulating layer overlying the barrier layer," and "planarizing the insulating layer."	Section V(B)(3) Section V(B)(6)
Claim 14: "forming a conductive plug in said opening to electrically connect to the diffusion region."	Claim 8: "forming a conductive plug in said opening to electrically connect to the diffusion region."	Section V(B)(7)

Accordingly, for the reasons as set forth, Becker in view of Wong renders claims 10-14 obvious.

VI. REDUNDANCY

This petition is being filed with grounds of rejections based on Doshi and Becker as primary references. Although numerous prior art references related to self-aligned contacts disclose an anisotropic etch that exposes the diffusion region and simultaneously forms a spacer of the etched barrier material on the

side wall of the gate electrode, Petitioner has presented only those grounds necessary to sufficiently demonstrate that each claim of the ’997 patent is not patentable, having demonstrated how various teachings address the claims divergently.

Petitioner submits that Doshi and Becker raise two non-redundant grounds of rejections because of their different treatment of the “spacer” recited in the claims. For example, claim 1 of the ’997 patent recites “forming a spacer of the etch barrier material on the sidewall of the gate electrode.” As discussed in Section V(A)(1) above, Doshi discloses forming a spacer of silicon nitride 30 on the sidewall of the gate electrode 10, where a sidewall filament 11 is between the spacer of silicon nitride 30 and the gate electrode 10. The spacer of silicon nitride 30 is therefore formed in the position of not being in direct contact with the gate electrode 10. On the other hand, as discussed in Section V(B)(1) above, Becker discloses a spacer of silicon nitride that is formed in direct contact with the sidewall of the gate electrode. While both are believed to be “on” the sidewall of the gate electrode, they are believed to be non-redundant in the manner in which they meet this feature.

Accordingly, Petitioner respectfully requests that the Board institute rejections on all grounds presented in this petition, in part because Petitioners have worked hard to reduce the burden on the PTAB through presentation of

just two grounds, and in part to avoid prejudicing the Petitioners based on at least the differentiated treatment of "on" mentioned above. However, to the extent the Board institutes fewer than the limited number of presented grounds, Petitioner requests that the Board institute at least the Doshi-based ground of rejections.

VII. CONCLUSION

The prior art references identified in this Petition provide new, non-cumulative technological teachings which indicate a reasonable likelihood of success as to Petitioner's assertion that the Challenged Claims of the '997 Patent are not patentable pursuant to the grounds presented. Accordingly, Petitioner respectfully requests institution of IPR for the Challenged Claims of the '997 Patent for each of the grounds presented herein.

Respectfully submitted,

Dated: 12/16/2014

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CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on December 17, 2014, a complete and entire copy of this Petition for *Inter Partes* Review and all supporting exhibits were provided by Federal Express, cost prepaid, to the Patent Owner by serving the correspondence address of record as follows:

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