

1c894 U.S. PTO



438	Class	639	Subclass
ISSUE CLASSIFICATION			

PATENT NUMBER

6146997



6146997

U.S. UTILITY PATENT APPLICATION

O.I.P.E. SCANNED <u>CTH(3) Q.A. me</u>	PATENT DATE <u>NOV 14 2000</u>
-------------------------------------------	-----------------------------------

SECTOR	CLASS <u>438</u>	SUBCLASS <u>639</u>	ART UNIT <u>2818</u>	EXAMINER <u>Dang</u>
--------	---------------------	------------------------	-------------------------	-------------------------

FILED WITH: ☐ DISK (CRF) ☐ FICHE
(Attached in pocket on right inside flap)

PREPARED AND APPROVED FOR ISSUE

ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)						
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					
<u>438</u>	<u>639</u>	<u>438</u>	<u>639</u>	<u>253</u>	<u>631</u>	<u>626</u>	<u>634</u>	
INTERNATIONAL CLASSIFICATION		<u>257</u>	<u>336</u>	<u>344</u>	<u>346</u>			
<u>H01L</u>	<u>21/4763</u>	<u>357</u>	<u>15</u>	<u>59</u>	<u>67</u>			

☐ Continued on Issue Slip Inside File Jacket

9-2800 Formal Drawings (5 sheets) set 1 9-29-99

<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg. <u>5</u>	Figs. Drwg. <u>9</u>	Print Fig. <u>20</u>	Total Claims <u>14</u>	Print Claim for O.G. <u>1</u>
<input type="checkbox"/> a) The term of this patent subsequent to _____ (date) has been disclaimed.	<u>PHUC DANG</u> <u>6/12/00</u> (Assistant Examiner) (Date)			NOTICE OF ALLOWANCE MAILED	
<input type="checkbox"/> b) The term of this patent shall not extend beyond the expiration date of U.S. Patent No. _____.	<u>David Nelms</u> Supervisory Patent Examiner Technology Center 2800 <u>6/01</u> (Primary Examiner) (Date)			<u>6114100</u> ISSUE FEE <u>6W</u> Amount Due <u>1210.00</u> Date Paid <u>7-24-00</u>	
<input type="checkbox"/> c) The terminal _____ months of this patent have been disclaimed.	<u>Scruen</u> <u>6/5/00</u> (Legal Instruments Examiner) (Date)			ISSUE BATCH NUMBER <u>N 84</u>	
WARNING: The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368. Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.					

Form PTO-436A
(Rev. 10/97)

Issue Fee

(LABEL AREA)

Formal Drawings (5 sheets) set 1
(FACE)

PATENT APPLICATION



09407268

1994 U.S. PTO

09/23/99



09/23/99

INITIALS 10/1/99

CONTENTS

Date received
(Incl. C. of M.)
or
Date Mailed

Date received
(Incl. C. of M.)
or
Date Mailed

1. Application _____ papers.		42. _____	
2. <u>Priority Paper</u>	<u>12-13-99</u>	43. _____	
3. <u>Rejection (3 months)</u>	<u>3 2 00</u>	44. _____	
4. <u>Request for Reconsideration</u>	<u>5/31/00</u>	45. _____	
5. <u>PTOL-37</u>	<u>6/14/00</u>	46. _____	
6. _____		47. _____	
7. _____		48. _____	
8. _____		49. _____	
9. _____		50. _____	
10. _____		51. _____	
11. _____		52. _____	
12. _____		53. _____	
13. _____		54. _____	
14. _____		55. _____	
15. _____		56. _____	
16. _____		57. _____	
17. _____		58. _____	
18. _____		59. _____	
19. _____		60. _____	
20. _____		61. _____	
21. _____		62. _____	
22. _____		63. _____	
23. _____		64. _____	
24. _____		65. _____	
25. _____		66. _____	
26. _____		67. _____	
27. _____		68. _____	
28. _____		69. _____	
29. _____		70. _____	
30. _____		71. _____	
31. _____		72. _____	
32. _____		73. _____	
33. _____		74. _____	
34. _____		75. _____	
35. _____		76. _____	
36. _____		77. _____	
37. _____		78. _____	
38. _____		79. _____	
39. _____		80. _____	
40. _____		81. _____	
41. _____		82. _____	

(FRONT)

ISSUE SLIP STAPLE AREA (for additional cross references)

POSITION	INITIALS	ID NO.	DATE
FEE DETERMINATION	<i>gk</i>		<i>10/8/99</i>
O.I.P.E. CLASSIFIER		<i>20019</i>	<i>10/8/99</i>
FORMALITY REVIEW			

INDEX OF CLAIMS

✓ Rejected N Non-elected
 = Allowed I Interference
 - (Through numeral) Canceled A Appeal
 + Restricted O Objected

Claim	Date	Claim	Date	Claim	Date
1		51		110	
2		52		112	
3		53		113	
4		54		114	
5		55		115	
6		56		116	
7		57		117	
8		58		118	
9		59		119	
10		60		120	
11		61		121	
12		62		122	
13		63		123	
14		64		124	
15		65		125	
16		66		126	
17		67		127	
18		68		128	
19		69		129	
20		70		130	
21		71		131	
22		72		132	
23		73		133	
24		74		134	
25		75		135	
26		76		136	
27		77		137	
28		78		138	
29		79		139	
30		80		140	
31		81		141	
32		82		142	
33		83		143	
34		84		144	
35		85		145	
36		86		146	
37		87		147	
38		88		148	
39		89		149	
40		90		150	
41		91			
42		92			
43		93			
44		94			
45		95			
46		96			
47		97			
48		98			
49		99			
50		100			

If more than 150 claims or 10 actions
staple additional sheet here

(LEFT INSIDE)

SEARCHED

Class	Sub.	Date	Exmr.
257	336	2/24/00	PD
↓	344	↓	↓
↓	346	↓	↓
357	59	2/24/00	PD
↓	15	↓	↓
↓	67	↓	↓
438	253	2/25/00	PD
↓	631	↓	↓
↓	626	↓	↓
↓	634	↓	↓
Update as noted	search above	6/12/00	PD

SEARCH NOTES (INCLUDING SEARCH STRATEGY)

EAST SEARCH	Date	Exmr.
	2/25/00	PD
EAST SEARCH	6/12/00	PD

INTERFERENCE SEARCHED

Class	Sub.	Date	Exmr.
257	336	6/12/00	PD
↓	344	↓	↓
↓	346	↓	↓
357	59	↓	↓
↓	15	↓	↓
↓	67	↓	↓
438	253	↓	↓
↓	631	↓	↓
↓	626	↓	↓
↓	634	↓	↓

(RIGHT OUTSIDE)

PATENT APPLICATION SERIAL NO. 09-407268

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

10/08/1999 JARTIS 00000038 09407268
01 FC:101 760.00 OP

PTO-1556
(5/87)

*U.S. GPO: 1996-433-214/80404

SERIAL NUMBER	09/407,268	FILING DATE	09/29/99	CLASS	438	GROUP ART UNIT	2812	ATTORNEY DOCKET NO.	420662000600
---------------	------------	-------------	----------	-------	-----	----------------	------	---------------------	--------------

APPLICANT	JACSON LIU, HSINCHU HSIEN, TAIWAN; JING-XIAN HUANG, HSINCHU CITY, TAIWAN.								
	CONTINUING DOMESTIC DATA*** VERIFIED <u>NONE</u> PD								
	371 (NAT'L STAGE) DATA*** VERIFIED <u>NONE</u> PD								
	FOREIGN APPLICATIONS*** VERIFIED <u>YES</u> TAIWAN PD 88107602 05/11/99								
IF REQUIRED, FOREIGN FILING LICENSE GRANTED 10/18/99									
ADDRESS	Foreign Priority claimed 35 USC 119 (a-d) conditions met <input checked="" type="checkbox"/> Yes <input type="checkbox"/> no <input type="checkbox"/> Met after Allowance Verified and Acknowledged PD Examiner's Initials Initials					STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
						TWX	5	14	2
TITLE	MORRISON & FOERSTER LLP 2000 PENNSYLVANIA AVENUE NW WASHINGTON DC 20006-1888								
	METHOD FOR FORMING SELF-ALIGNED CONTACT HOLE								
FILING FEE RECEIVED		FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT NO. _____ for the following:				<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees (Filing) <input type="checkbox"/> 1.17 Fees (Processing Ext. of time) <input type="checkbox"/> 1.18 Fees (Issue) <input type="checkbox"/> Other _____ <input type="checkbox"/> Credit			
\$760						275			

Please type a plus sign (+) inside this box →

PTO/SB/05 (12/97) (modified)
A. ed for use through 09/30/00. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

**UTILITY
PATENT APPLICATION
TRANSMITTAL**

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. 420662000600

Total Pages 24

First Named Inventor or Application Identifier

Jacson-LIU and Jing-Xian HUANG

Express Mail Label No. EJ004420079US

CERTIFICATE OF MAILING BY "EXPRESS MAIL"

Express Mail Label No.: EJ004420079US

Date of Deposit: September 29, 1999

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 39 C.F.R. § 1.10 on the date indicated above and is addressed to Assistant Commissioner for Patents, Washington, D.C. 20231.

Blanche H. Cook

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO:

Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☒ Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)
2. ☒ Specification [Total Pages 10]
(preferred arrangement set forth below)
- Descriptive title of the invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claim(s)
- Abstract of the Disclosure
3. ☒ Drawing(s) (35 USC 113) [Total Sheets 5]
4. ☒ Oath or Declaration [Total Pages 3]
a. ☒ Newly executed (original)
b. ☐ Copy from a prior application (37 CFR 1.63(d)
(for continuation/divisional with Box 17 completed)
[Note Box 5 below]
i. ☐ **DELETION OF INVENTOR(S)**
Signed statement attached deleting inventor(s) named in
the prior application, see 37 CFR 1.63(d)(2) and 1.33(b)
5. ☒ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the
oath or declaration is supplied under Box 4b, is considered as being
part of the disclosure of the accompanying application and is hereby
incorporated by reference therein.

6. ☐ Microfiche Computer Program (Appendix)
7. ☐ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ☐ Computer Readable Copy
b. ☐ Paper Copy (identical to computer copy)
c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ☒ Assignment Papers (cover sheet & document(s))
9. ☐ 37 CFR 3.73(b) Statement [] Power of Attorney
(when there is an assignee)
10. ☐ English Translation Document (if applicable)
11. ☐ Information Disclosure
Statement (IDS)/PTO-1449 [] Copies of IDS
Citations
12. ☐ Preliminary Amendment
13. ☒ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
14. ☐ Small Entity [] Statement filed in prior application,
Statement(s) Status still proper and desired
15. ☐ Certified Copy of Priority Document(s)
(if foreign priority is claimed)
16. ☐

17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No:

18. CORRESPONDENCE ADDRESS

Barry E. Bretschneider
Registration No. 28,055

Morrison & Foerster LLP
2000 Pennsylvania Avenue, N.W.
Washington, D.C. 20006-1888
Telephone: (202) 887-1545
Facsimile: (202) 887-0763

dc-176657

- ☒ If a paper is untimely in the above-referenced application by applicant or his/her representative, the Assistant Commissioner is hereby petitioned under 37 C.F.R. § 1.136(a) for the minimum extension of time required to make said paper timely. In the event a petition for extension of time is made under the provisions of this paragraph, the Assistant Commissioner is hereby requested to charge any fee required under 37 C.F.R. § 1.17(a)-(d) to Deposit Account No. 03-1952. However, the Assistant Commissioner is **NOT** authorized to charge the cost of the issue fee to the Deposit Account.

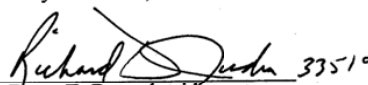
The filing fee has been calculated as follows:

FOR	NUMBER FILED	NUMBER EXTRA	RATE	CALCULATIONS
TOTAL CLAIMS	14 - 20 =	0	x \$18.00	\$
INDEPENDENT CLAIMS	2 - 3 =	0	x \$78.00	\$
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ \$260.00	\$
			BASIC FEE	\$760.00
TOTAL OF ABOVE CALCULATIONS =				\$760.00
Reduction by 1/2 for filing by small entity (Note 37 C.F.R. §§ 1.9, 1.27, 1.28). If applicable, verified statement must be attached.				\$
Assignment Recording Fee (if enclosed)				\$40.00
TOTAL =				\$800.00

- ☒ A check in the amount of \$800.00 is attached.
- ☒ Under 35 USC 119, this application claims the benefit of Taiwanese priority application Serial No. 88107602, filed May 11, 1999. A copy of the priority document will be filed at a later date.
- Applicant(s) hereby petitions for any required relief including extensions of time and authorizes the Assistant Commissioner to charge the cost of such petitions and/or other fees or to credit any overpayment to Deposit Account No. 03-1952 referencing docket no. 420662000600. A duplicate copy of this transmittal is enclosed, for that purpose.

Dated: September 29, 1999

Respectfully submitted,

By:  33519
for Barry E. Bretschneider
Registration No. 28,055

Morrison & Foerster LLP
2000 Pennsylvania Avenue, N.W.
Washington, D.C. 20006-1888
Telephone: (202) 887-1545
Facsimile: (202) 887-0763

TITLE

METHOD FOR FORMING SELF-ALIGNED CONTACT HOLE

BACKGROUND OF THE INVENTION

5 Field of the Invention

The present invention relates in general to the fabrication of semiconductor devices, and more particularly to a simplified method for forming a self-aligned contact hole.

10 Description of the Related Arts

Self-alignment is a technique in which multiple levels of regions on the wafer are formed using a single mask, thereby eliminating the alignment tolerance required by additional masks. This powerful approach is being used more often as circuit sizes decrease. Self-aligned contacts are often used in memory cells where contacts are limited only by the spacers and field oxide bird's beak or a contact window landing pad. Therefore, the mask contact window can be oversized relative to the contact area underneath, and no contact borders are needed, resulting in significant space saving. Referring to FIGS. 1A-1E, a conventional process of forming a self-aligned contact hole is illustrated in cross-sectional views. The process will be described as follows.

FIG. 1A shows a semiconductor substrate 10 having two closely spaced field effect transistors with gate electrodes 14, source/drain diffusion regions 18, and gate oxides 12. The gate electrodes 14, commonly consisting of polysilicon and silicide, are capped with an insulator 16 of silicon nitride. Next, a thin oxide layer 20 is formed over the substrate surface and on the sidewalls of the gate electrode 14 by rapid thermal oxidation at about 800 to 1100° C.

Referring to FIG. 1B, a conformal layer of silicon nitride 22 having a thickness of about 100 to 600 Å is

deposited over the substrate surface using low pressure chemical vapor deposition (LPCVD). The conformal silicon nitride layer 22 is anisotropically etched to form nitride spacers 22a on the sidewalls of the gate electrodes 22 and the cap layers 16, as shown in FIG. 1C. Then, the thin oxide layer on the substrate surface is removed by HF solution to expose the diffusion region 18.

Referring to FIG. 1D, a conformal layer of etch barrier material 24 is deposited over the diffusion region 18, the cap layers 16, and the sidewall spacers 22a. The barrier layer is typically a silicon nitride layer having a thickness of about 100 to 500 Å. A layer of insulator 26 is deposited over the substrate as inter-layer dielectric (ILD) and is preferably planarized. The insulating layer 26 may consist of one or more dielectric depositions of spin on glass (SOG), silicon oxide, borophosphosilicate (BPSG), and so on.

Referring to FIG. 1E, using a photoresist mask 28, a contact hole 29 is etched in the insulating layer 26 with the barrier layer 24 serving as an etch stop, which is finally removed to expose the diffusion region 18. The etching of the insulating layer 26 is selective to the capping layers 16 and sidewall spacers 22a encapsulating the gate electrodes 14 so that the contact hole is self-aligning in nature.

The fabricating method described above, however, requires complicated processes. For example, two depositions of silicon nitride are required for forming the conformal layer 22 and the barrier layer 24, respectively. Besides, the two layers are to be etched individually. The conformal nitride layer 22 is etched to form nitride spacers 22a, and the barrier layer 24 is etched to reveal the

underlying diffusion region 18 after the contact hole etching. Thus, improvements are needed to eliminate process steps so as to reduce the manufacturing cost and to increase the throughput.

5

SUMMARY OF THE INVENTION

It is therefore an object of the invention to provide a simplified method for forming a self-aligned contact hole.

To accomplish the above objective, the present invention provides a method for forming a self-aligned contact hole. In this method, the conformal layer used for forming sidewall spacers of gate electrodes will not be etched until a contact opening is formed, such that the conformal layer can serve as an etch barrier that protects the diffusion region during the contact hole etching. Thus, there is no need for depositing another etch barrier layer. Furthermore, the etching for sidewall spacers can be thus incorporated into the contact hole etching, thereby eliminating process steps.

The present method for forming a self-aligned contact includes the steps of: (a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon; (b) forming a conformal layer of etch barrier material overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode; (c) forming an insulating layer overlying the barrier layer; (d) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop; and (e) anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etch barrier material on the sidewall of the gate electrode.

4

Other objects, features, and advantages of the present invention will become apparent from the following detailed description which makes reference to the accompanying drawings.

5

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A through 1E are cross-sectional views illustrating the steps of a conventional method for fabricating a self-aligned contact hole; and

10 FIGS. 2A through 2D are cross-sectional views illustrating the steps for fabricating a self-aligned contact hole according to a preferred embodiment of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

15

Now in keeping with the objective of this invention, the method for fabricating a self-aligned contact hole is described in detail.

Referring to FIG. 2A, two closely spaced field effect transistors with gate electrodes **54**, source/drain diffusion regions **58**, and gate oxides **52** are defined in a semiconductor substrate **50** using known processes. The gate electrodes **54**, preferably consisting of polysilicon and tungsten silicide, are capped with an insulator **56** of silicon nitride. The process details for forming such field effect transistors are well known and will not be described here. Next, a thin oxide layer **60** having a thickness of about 150 Å is formed over the substrate surface and on the sidewalls of the gate electrode **54** by rapid thermal oxidation at about 800 to 1100° C.

25

Referring to FIG. 2B, a conformal layer of silicon nitride **62** is deposited over the substrate surface using low pressure chemical vapor deposition (LPCVD). The conformal silicon nitride layer **62**, as described earlier, acts as

30

sidewall spacers of gate electrode 54 as well as an etch stop at contact hole etching. The conformal layer 62 preferably has a thickness of about 100 to 500 Å, and more preferably has a thickness of about 200 to 350 Å.

5 Referring to FIG. 2C, a layer of insulator 64 is deposited over the substrate as inter-layer dielectric (ILD) and is preferably planarized. The insulating layer 64 may consist of one or more dielectric depositions of spin on glass (SOG), silicon oxide, borophosphosilicate (BPSG), and
10 the like. It should be particularly noted that the process steps of anisotropically etching for sidewall spacers and depositing a barrier layer necessary in the conventional method are omitted here.

Referring to FIG. 2D, using a photoresist mask 66, a
15 contact hole 67 is etched in the insulating layer 64 in a self-aligned manner. During this etch, the conformal nitride layer 62 serves as an etch barrier to protect the diffusion region 58 from being attacked by etching. Moreover, as depicted in FIG. 2C, it provides extra
20 thickness d to protect the gate electrode 54 when compared to that of the conventional method (see FIG. 1C for reference). Next, the conformal nitride layer 62 underneath the opening is anisotropically etched to remove the portion over the diffusion region 58. Simultaneously with this etch,
25 nitride spacers 62a are formed on sidewalls of the gate electrode 54. After removing the photoresist 66, the thin oxide layer 60 is removed by HF solution to expose the diffusion region 58, thereby completing the contact hole.

Thereafter, a conductive plug can be formed in the
30 contact hole 67 to electrically connect to the diffusion region 58. The conductive plug is preferably chosen from polysilicon, tungsten, molybdenum, aluminum alloys, copper

alloys, and the like. It can be formed by overfilling the contact hole and removing the conductive material outside of the contact hole by etch back or chemical mechanical polishing.

- 5 According to a feature of the present invention, because the conformal nitride layer 62 is not etched until the contact opening is formed, it provides extra thickness d to protect the gate electrode 54 at the contact hole etching. Further, the same nitride layer is anisotropically etched to
10 form sidewall spacers that prevent shorting between the gate electrode and the conductive plug.

The simplified method of the invention overall reduces one etch step and one deposition step as compared to the conventional method illustrated by FIGS. 1A through 1E.

- 15 Accordingly, the manufacturing cost is reduced and the throughput is increased. Further, since the method of the present invention provides a better etch barrier at the contact hole etching, it is advantageous in process tolerance and reliability.

- 20 While the invention has been particularly shown and described with the reference to the preferred embodiment thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is:

- 1 1. A method for forming a self-aligned contact hole,
2 comprising the steps of:
3 (a) providing a semiconductor substrate having a gate
4 electrode and a diffusion region thereon;
5 (b) forming a conformal layer of etch barrier material
6 overlying the substrate surface including the diffusion
7 region and the upper surface and the sidewalls of the gate
8 electrode;
9 (c) forming an insulating layer overlying the barrier
10 layer;
11 (d) etching an opening through the insulating layer
12 self-aligned and borderless to the diffusion region by using
13 the barrier layer as an etch stop; and
14 (e) anisotropically etching the barrier layer
15 underneath the opening, thereby exposing the diffusion
16 region and simultaneously forming a spacer of the etch
17 barrier material on the sidewall of the gate electrode.
- 1 2. The method as claimed in claim 1, further comprising
2 a step of forming an oxide layer over the diffusion region
3 and on the sidewalls of the gate electrode by thermal
4 oxidation prior to forming the barrier layer.
- 1 3. The method as claimed in claim 1, wherein said gate
2 electrode comprises a capping layer of silicon nitride.
- 1 4. The method as claimed in claim 1, wherein said
2 barrier layer is a silicon nitride layer.
- 1 5. The method as claimed in claim 4, wherein said
2 barrier layer has a thickness between about 100 to 500 Å.

1 6. The method as claimed in claim 1, wherein said
2 insulating layer comprises a layer of borophosphosilicate
3 glass.

1 7. The method as claimed in claim 1, wherein step (c)
2 comprises:
3 depositing an insulating layer overlying the barrier
4 layer; and
5 planarizing the insulating layer.

1 8. The method as claimed in claim 1, further comprising
2 forming a conductive plug in said opening to electrically
3 connect to the diffusion region.

1 9. A method for forming a self-aligned contact hole,
2 comprising the steps of:
3 (a) providing a semiconductor substrate having a gate
4 electrode and a diffusion region thereon, said gate
5 electrode comprising a capping layer;

6 (b) forming an oxide layer over the diffusion region
7 and on the sidewalls of the gate electrode by thermal
8 oxidation;

9 (c) forming a conformal layer of silicon nitride
10 overlying the substrate surface including the diffusion
11 region and the upper surface and the sidewalls of the gate
12 electrode;

13 (d) forming an insulating layer overlying the conformal
14 layer of silicon nitride;

15 (e) etching an opening through the insulating layer
16 self-aligned and borderless to the diffusion region by using
17 the silicon nitride layer as an etch stop; and

18 (e) anisotropically etching the silicon nitride layer
19 underneath the opening, thereby exposing the diffusion

0467-4448-US/880011
Final/Esmond

20 region and simultaneously forming a spacer of silicon
21 nitride on the sidewall of the gate electrode.

1 10. The method as claimed in claim 9, wherein said
2 capping layer is a silicon nitride layer.

1 11. The method as claimed in claim 9, wherein said
2 conformal layer of silicon nitride has a thickness between
3 about 100 to 500 Å.

1 12. The method as claimed in claim 9, wherein said
2 insulating layer comprises a layer of borophosphosilicate
3 glass.

1 13. The method as claimed in claim 9, wherein step (d)
2 comprises:
3 depositing an insulating layer overlying the conformal
4 layer of silicon nitride; and
5 planarizing the insulating layer.

1 14. The method as claimed in claim 9, further
2 comprising forming a conductive plug in said opening to
3 electrically connect to the diffusion region.

0467-4448-US/880011

09/407,268

0467-4448-US/880011
Final/Esmond

TITLE

METHOD FOR FORMING SELF-ALIGNED CONTACT HOLE

ABSTRACT OF THE DISCLOSURE

- 5 A simplified method for forming a self-aligned contact hole is disclosed. The method comprises the steps of (a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon; (b) forming a conformal layer of etch barrier material overlying the substrate
- 10 surface including the diffusion region and the upper surface and the sidewalls of the gate electrode; (c) forming an insulating layer overlying the barrier layer; (d) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier
- 15 layer as an etch stop; and (e) anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etch barrier material on the sidewall of the gate electrode.

09407268 002000

PATENT
Docket No.

DECLARATION FOR UTILITY PATENT APPLICATION

AS A BELOW-NAMED INVENTOR, I HEREBY DECLARE THAT:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and [sole/joint] inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD FOR FORMING SELF-ALIGNED CONTACT HOLE

, the specification of which is attached hereto unless the following box is checked:

☐ was filed on _____ as United States Application Serial
No. _____ and was amended on _____ (if
applicable).

I HEREBY STATE THAT I HAVE REVIEWED AND UNDERSTAND THE
CONTENTS OF THE ABOVE-IDENTIFIED SPECIFICATION, INCLUDING THE CLAIMS,
AS AMENDED BY ANY AMENDMENT REFERRED TO ABOVE.

I acknowledge the duty to disclose information which is material to the patentability as
defined in 37 C.F.R. § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any
foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International
application which designated at least one country other than the United States listed below and
have also identified below, by checking the box, any foreign application for patent or inventor's
certificate, or PCT International application having a filing date before that of the application on
which priority is claimed:

Application No.	Country	Date of Filing (day/month/year)	Priority Claimed?
88107602	Taiwan, R.O.C.	11/05/1999	<input checked="" type="checkbox"/> Yes <input type="checkbox"/> No
			<input type="checkbox"/> Yes <input type="checkbox"/> No
			<input type="checkbox"/> Yes <input type="checkbox"/> No

I hereby claim benefit under 35 U.S.C. § 119(e) of any United States provisional
application(s) listed below:

Application Serial No.	Filing Date

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 C.F.R. § 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application.

Application Serial No.	Filing Date	Status
		<input type="checkbox"/> Patented <input type="checkbox"/> Pending <input type="checkbox"/> Abandoned

I hereby appoint the following attorneys and agents to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

Mani Adeli (Reg No. 39,585)	Erwin J. Basinski (Reg No. 34,773)
Paula A. Borden (Reg No. 42,344)	Sean Brennan (Reg No. 39,917)
Barry E. Bretschneider (Reg No. 28,055)	Nicholas Buffinger (Reg No. 39,124)
Alan W. Cannon (Reg No. 34,977)	Mark R. Carter (Reg No. 39,131)
Robert K. Cerpa (Reg No. 39,933)	Thomas E. Ciotti (Reg No. 21,013)
Niki D. Cox (Reg No. 42,446)	Raj S. Davé (Reg No. 42,465)
E. Victor Donahue (Reg No. 35,492)	Stephen C. Durant (Reg No. 31,506)
Tyler Dylan (Reg No. 37,612)	Sean M. Fitzgerald (Reg No. 42,537)
Hector Gallegos (Reg No. 40,614)	Douglas Hodder (Reg No. 41,840)
Charles D. Holland (Reg No. 35,196)	Madeline I. Johnston (Reg No. 36,174)
Richard D. Jordan (Reg No. 33,519)	Cindy S. Kaplan (Reg No. 40,043)
Ararat Kapouytian (Reg No. 40,044)	Antoinette F. Konski (Reg No. 34,202)
Jung-Hua Kuo (Reg No. 41,918)	Susan K. Lehnhardt (Reg No. 33,943)
Wen Liu (Reg No. 32,822)	Shmuel Livnat (Reg No. 33,949)
David C. Lundmark (Reg No. 42,815)	Harry J. Macey (Reg No. 32,818)
Thomas D. Mays (Reg No. 34,524)	Gladys H. Monroy (Reg No. 32,430)
Kate H. Murashige (Reg No. 29,959)	Dahna S. Pasternak (Reg No. 41,411)
Catherine M. Polizzi (Reg No. 40,130)	William C. Revelos (Reg No. 42,101)
Robert Saltzberg (Reg No. 36,910)	J. Michael Schiff (Reg No. 40,253)
Debra A. Shetka (Reg No. 33,309)	Lee K. Tan (Reg No. 39,447)
E. Thomas Wheelock (Reg No. 28,825)	Thomas G. Wiseman (Reg No. 35,046)
Frank Wu (Reg No. 41,386)	

and:

Please direct all communications to:

Barry E. Bretschneider

Morrison & Foerster LLP
2000 Pennsylvania Avenue, N.W.
Washington, D.C. 20006-1888

Please direct all telephone calls to Barry E. Bretschneider at (202) 887-1545.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under § 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

✓ 1999.9.17

Date

✓ Jason - Liu

Name: Jacson-LIU (Last name: LIU)

Residence: Same as the Post Office Address (Below)

Citizenship: Taiwan, R.O.C.

Post Office Address: No. 14-7, Lin 4, Hou-Ko Tsun, Hou-Ko Hsiang,
Hsinchu Hsien, Taiwan, R.O.C.

✓ 1999.9.15

Date

✓ Jing-Xian Huang

Name: Jing-Xian HUANG (Last name: HUANG)

Residence: Same as the Post Office Address (Below)

Citizenship: Taiwan, R.O.C.

Post Office Address: No. 20-46, Lane 104, Gian-Keng 1 Rd., Lin 24,
Guan-Kung Li, East District, Hsinchu City, Taiwan,
R.O.C.

Date

Name:

Residence:

Citizenship:

Post Office Address:

Date

Name:

Residence:

Citizenship:

Post Office Address:

Date

Name:

Residence:

Citizenship:

Post Office Address:

09407268-022999

APPROVED	O.G. FIG. 2 D	
BY	CLASS	SUBCLASS
DRAFTSMAN	438	639

6148997

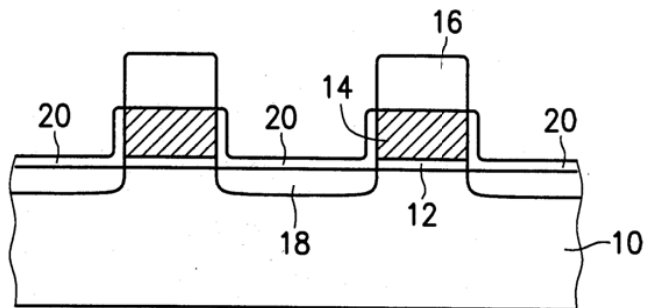


Fig. 1A (Prior Art)

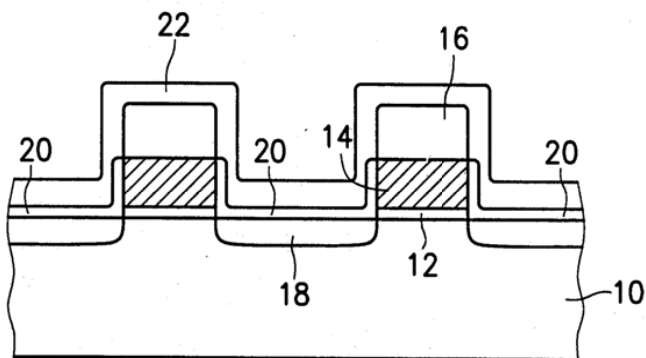


Fig. 1B (Prior Art)

Sup 9

APPROVED	D.G. 110.	
BY	CLASS	SUPPLIES
DRAFTSMAN		

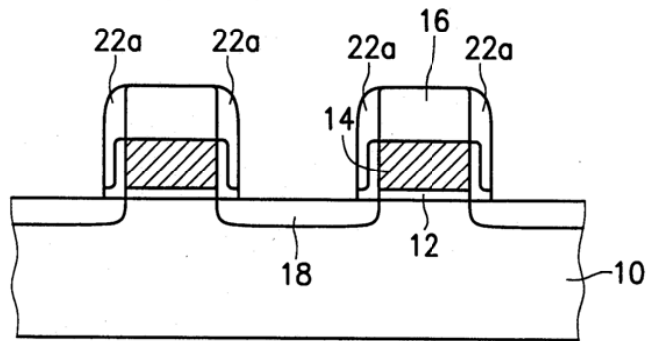


Fig. 1C (Prior Art)

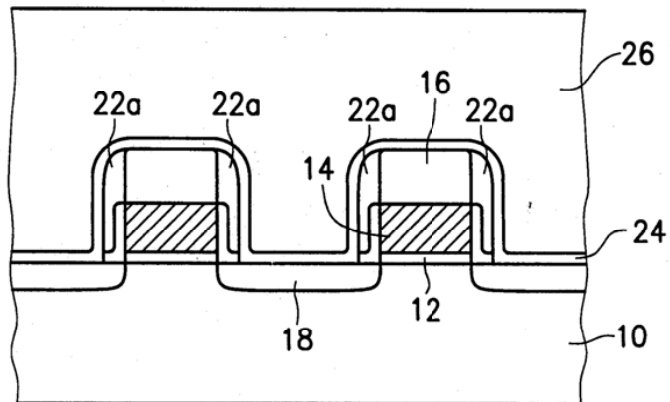


Fig. 1D (Prior Art)

666260-892/0460

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

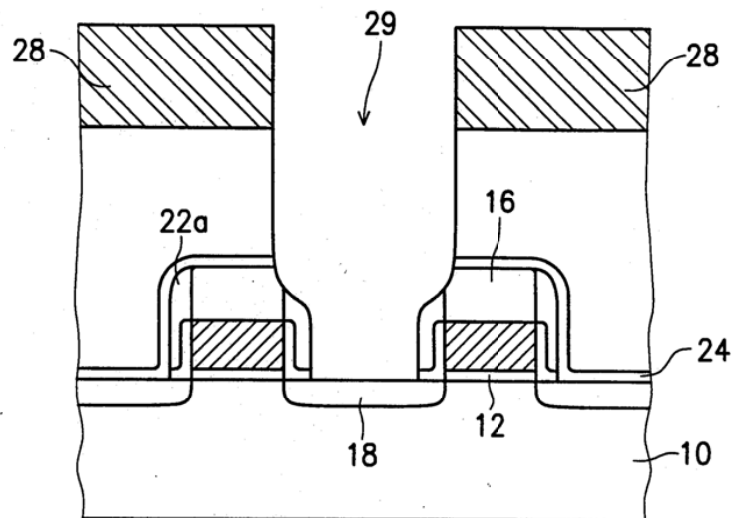


Fig. 1E (Prior Art)

09407268-092999

APPROVED	O.D. PG.	
BY	CLASS	SUBCLASS
DRAWN		

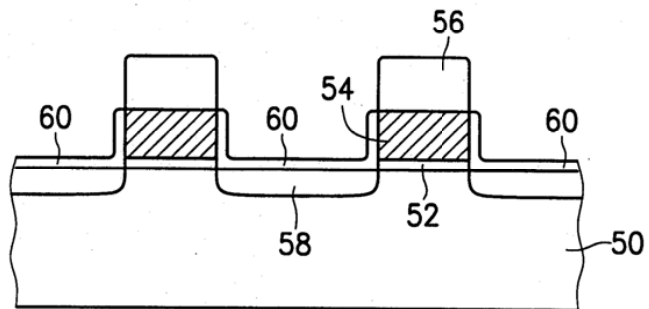


Fig. 2A

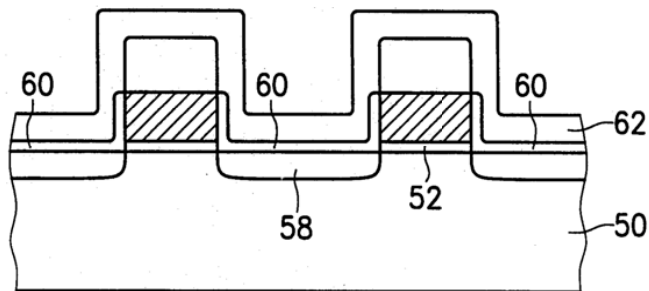


Fig. 2B

09407268-092999

APPROVED	O.G. FIG. 2D	
BY	CLASS	SUBCLASS
DRAFTSMAN	438	639

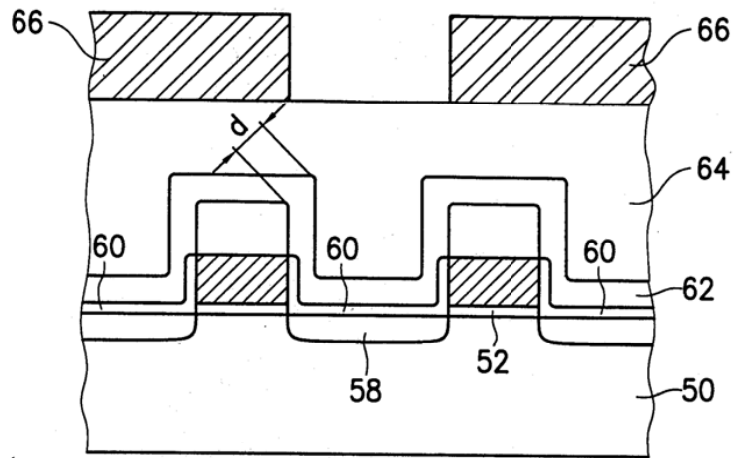


Fig. 2C

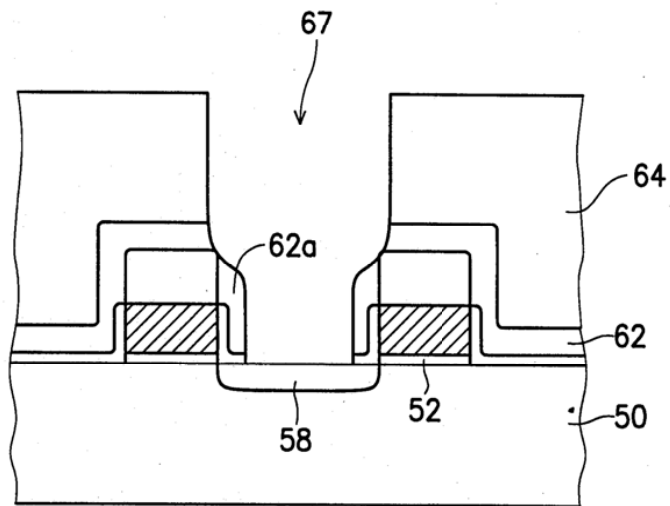


Fig. 2D

09407268-092999

PRINT OF DRAWINGS
AS ORIGINALLY FILED

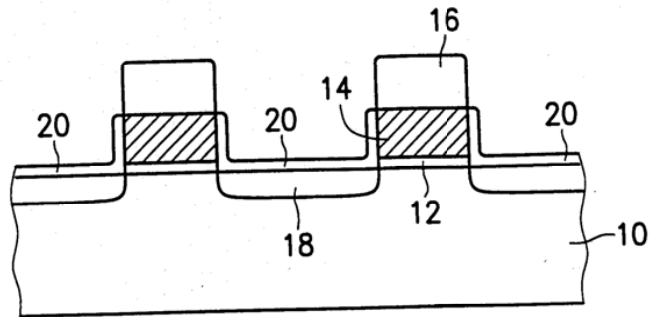


Fig. 1A (Prior Art)

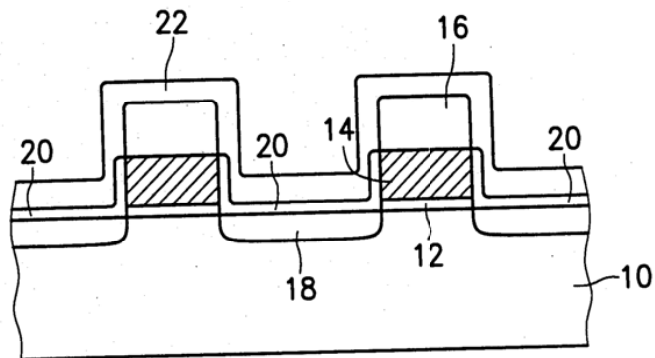


Fig. 1B (Prior Art)

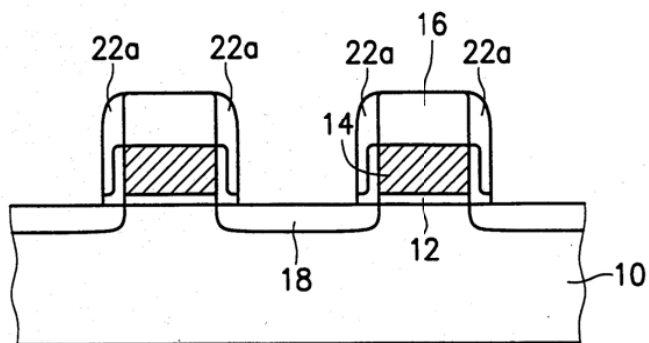


Fig. 1C (Prior Art)

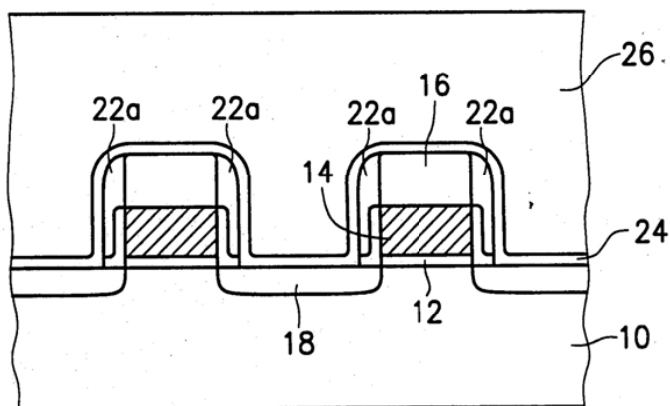


Fig. 1D (Prior Art)

PRINT OF DRAWINGS
AS ORIGINALLY FILED

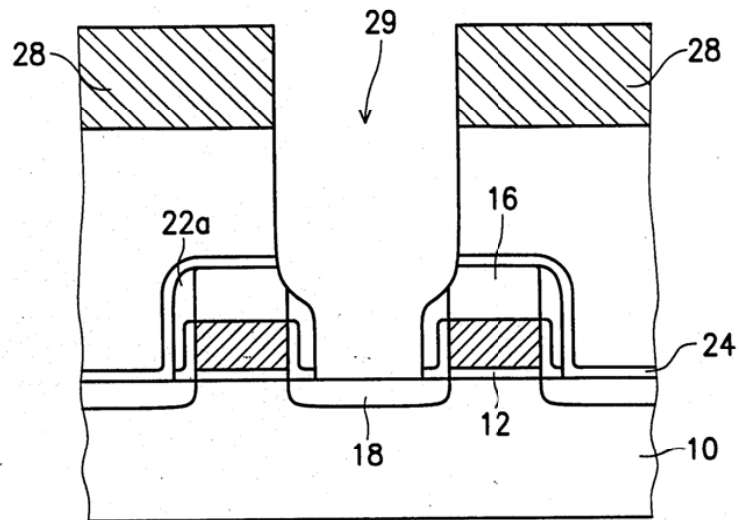


Fig. 1E (Prior Art)

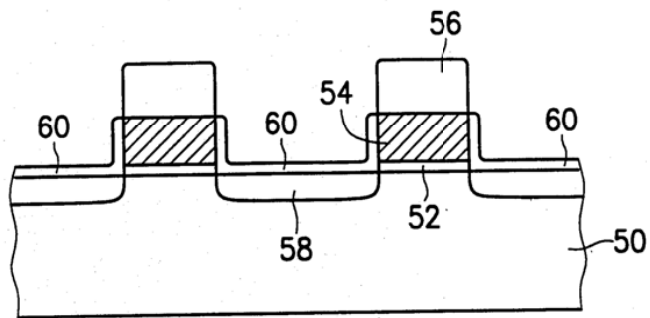


Fig. 2A

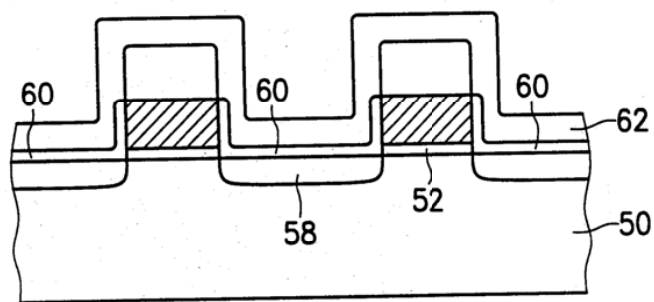


Fig. 2B

00107268-10299

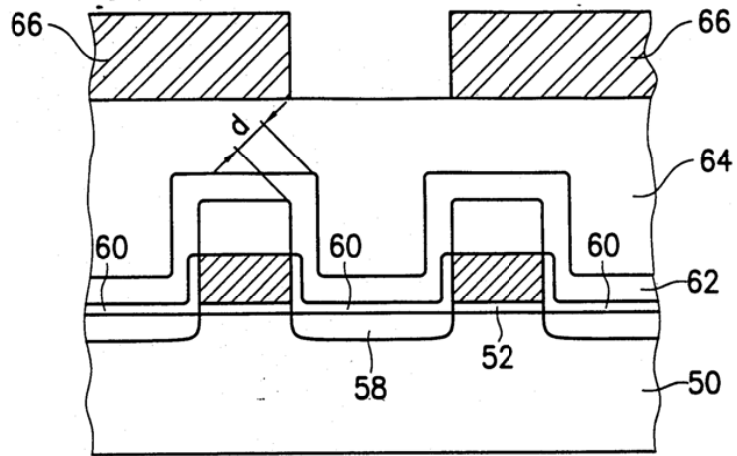


Fig. 2C

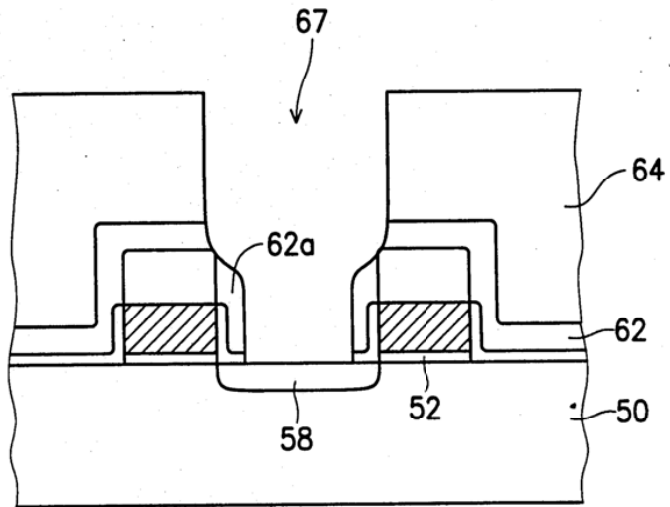


Fig. 2D

#2
Priority
Paper
PATENT 1-8-00
Docket No.
Client Ref.

CERTIFICATE OF HAND DELIVERY

I hereby certify that this correspondence is being hand filed with the United States Patent and Trademark Office in Washington, D.C. on December 13, 1999.

Jinrong Li

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

Jacson LIU et al.

Serial No.: 09/407,268

Filing Date: September 29, 1999

For: METHOD FOR FORMING SELF-
ALIGNED CONTACT HOLE



Examiner: to be assigned

Group Art Unit: 2812

TRANSMITTAL OF PRIORITY DOCUMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

RECEIVED

DEC 14 1999

TECHNOLOGY CENTER 2800

Sir:

Under the provisions of 35 USC 119, applicants hereby claim the benefit of the filing date of Taiwan patent application No. 88107602, filed May 11, 1999.

A certified copy of the priority document is attached to perfect applicants' claim for priority.


It is respectfully requested that the receipt of this certified copy attached hereto be acknowledged in this application.

In the event that the transmittal letter is separated from this document and the Patent and Trademark Office determines that an extension and/or other relief is required, applicant petitions
dc-186247

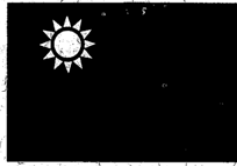
for any required relief including extensions of time and authorizes the Assistant Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to Deposit Account No. 03-1952. However, the Assistant Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Dated: December 13, 1999

Respectfully submitted,

By: 
Barry E. Bretschneider
Registration No. 28,055

Morrison & Foerster LLP
2000 Pennsylvania Avenue, N.W.
Washington, D.C. 20006-1888
Telephone: (202) 887-1545
Facsimile: (202) 887-0763



中華民國經濟部智慧財產局

INTELLECTUAL PROPERTY OFFICE
MINISTRY OF ECONOMIC AFFAIRS
REPUBLIC OF CHINA

茲證明所附文件，係本局存檔中原申請案的副本，正確無訛，
其申請資料如下：

This is to certify that annexed is a true copy from the records of this
Office of the application as originally filed which is identified hereunder:

申請日：西元 1999 年 5 月 11 日
Application Date

申請案號：88107602
Application No.

申請人：台灣茂矽電子股份有限公司
Applicant(s)

RECEIVED

DEC 14 1999

TECHNOLOGY CENTER 2800

局長
Director General


陳明邦

發文日期：西元 1999 年 11 月
Issue Date

發文字號：140150
Serial No.

申請日期：	案號：
類別：	

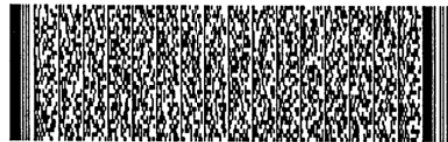
(以上各欄由本局填註)

發明專利說明書		
一、 發明名稱	中 文	自對準接觸窗製程
	英 文	
二、 發明人	姓 名 (中文)	1. 劉永男 2. 黃景賢
	姓 名 (英文)	1. Jacson-Liu 2.
	國 籍	1. 中華民國 2. 中華民國
	住、居所	1. 新竹縣湖口鄉湖口村4鄰14之7號 2. 新竹市東區軍功里24鄰建功一路104巷20之46號
三、 申請人	姓 名 (名稱) (中文)	1. 台灣茂矽電子股份有限公司
	姓 名 (名稱) (英文)	1.
	國 籍	1. 中華民國
	住、居所 (事務所)	1. 新竹科學工業園區力行路十九號
	代表人 姓 名 (中文)	1. 胡洪九
	代表人 姓 名 (英文)	1.
		

四、中文發明摘要 (發明之名稱：自對準接觸窗製程)

本發明揭示一種將側壁層回蝕刻與接觸窗蝕刻合併的自對準接觸窗製程，藉由本發明的簡化製程可提高產能並使閘極在蝕刻接觸窗時有較厚的蝕刻阻障層保護，免於遭到蝕刻穿透。本發明製程包括下列主要步驟：(a)提供一半導體基底，其上形成複數個電晶體元件，分別包括一閘極和一對源/汲極擴散區，閘極上並形成有一絕緣覆蓋層；(b)形成一阻障層覆蓋在基底與電晶體元件上；(c)形成一平坦的絕緣層覆蓋在阻障層上；(d)以阻障層為蝕刻終止層，選擇性地蝕刻絕緣層，以形成一自對準窗口對應於源/汲極擴散區；以及(e)非等向性地蝕刻窗口底下之阻障層，以露出源/汲極擴散區作為接觸區，同時於閘極的側壁形成一側壁層。

英文發明摘要 (發明之名稱：)



本案已向

國(地區)申請專利

申請日期

案號

主張優先權

無

有關微生物已寄存於

寄存日期

寄存號碼

無

五、發明說明 (1)

【發明領域】

本發明是有關於半導體製程技術，且特別是有關於一種自對準接觸(self-aligned contact; SAC)製程，相較於傳統製程，本發明將側壁層回蝕刻與接觸窗的蝕刻合併，可減少製程步驟，更重要的是，本發明在閘極與接觸窗之間提供了一個較厚的蝕刻阻絕層，可減少蝕刻穿透的機率。

【發明背景】

在提高積體電路的包裝密度和減少晶片尺寸的不斷努力中，不同圖案層之間的對準誤差是主要的障礙所在，因此便有許多自我對準(self-aligned)的結構被提出來，用以縮減元件之間的距離，增加元件的密集度。例如自我對準接觸窗的結構，可允許接觸窗與閘極的重疊，因此提高了元件的密集度，並提供了適當的保護以防短路。

所謂的"自我對準"，是利用設計中既定的幾何結構，作為次一製程步驟中意欲形成結構的遮蔽或窗口，能夠使元件的各組成部份不偏不倚地建構在適當的位置。在自我對準接觸窗的製程中，可提供對失去對準較大的容忍度。這樣的疊重是可允許的，因為自我對準接觸點是以一種在接觸窗與閘極間提供額外絕緣的方法所形成，以致可防止短路。

為進一步了解本發明之背景，以下配合第1A~1E圖說明傳統的自對準接觸窗的製程。首先請參照第1A圖，在一



五、發明說明 (2)

半導體基底10上形成有兩個相鄰的場效電晶體，包括閘極14、源/汲極擴散區18、閘極氧化層12等，其中閘極14，通常是由一層複晶矽與一層矽化金屬(如 WSi_2)所共同組成的複晶矽化金屬(polycide)。在閘極上方具有一層材質為氮化矽的覆蓋層(cap layer)16。接著，在800~1100℃之製程溫度下，以一道快速熱氧化(RTO; rapid thermal oxidation)製程，在基底10表面及閘極14側壁形成一薄氧化層20，同時藉由該熱製程修補基底表面的缺陷。

請參照第1B圖，以低壓化學氣相沈積法(LPCVD)沈積一層厚約100~600埃的氮化矽層22，覆蓋在基底既有之元件上。此氮化矽層22經過回蝕刻後，在閘極14與覆蓋層16的側壁形成一氮化側壁層22a，如第1C圖所示。蝕刻完畢後，以一道氫氟酸的清洗程序將基底10表面的薄氧化矽層去除，露出源/汲極擴散區18。

請參照第1D圖，接下來，以化學氣相沈積法在基底上沈積一層材質為氮化矽的阻障層24，厚度約100~500埃其延伸覆蓋在側壁層22a、覆蓋層16及源/汲極擴散區18的表面，以作為後續自對準接觸蝕刻時的蝕刻阻絕層。然後，在基底上沈積一種或一種以上的絕緣材料，例如氧化矽、硼磷矽玻璃、旋塗式玻璃等，並將之平坦化，作為內層介電層(Inter Layer Dielectrics; ILD)26。

請參照第1E圖，以微影製程在介電層26上形成一光阻單幕28，露出欲形成自對準接觸窗的區域，進行絕緣層26的非等向性蝕刻。蝕刻過程中，是以氮化矽阻障層24為蝕



五、發明說明 (3)

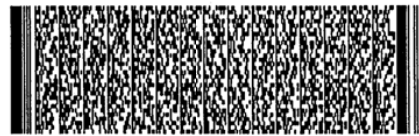
刻終止層，其中並藉由氮化矽覆蓋層16與氮化矽側壁層22a對閘極14提供適當的阻絕效果。蝕刻完絕緣層26後，將接觸窗範圍中的氮化矽阻障層24去除，露出作為接觸區的源/汲極擴散區18，即完成自對準接觸窗29的製作。之後的製程更包括：去光阻及形成一導電層填入窗口，藉此與接觸區18形成電性連接。

在上述的自對準接觸製程中，為了避免蝕刻損及閘極與源/汲極接觸區，必須在閘極14上製作氮化矽側壁層22a以及在接觸區18上製作氮化矽阻障層24，因此需要個別的沈積氮化矽與回蝕刻程序，使得整個製程步驟極其繁複。為克服上述困難，本發明揭示一種將側壁層回蝕刻與接觸窗蝕刻合併的簡化製程，以期提高產能、減少成本。另外，藉由本發明的製程，可使閘極在蝕刻接觸窗時有較厚的蝕刻阻障層保護，免於遭到蝕刻穿透。

【發明概述】

本發明的目的在於提供一種自對準接觸窗製程，其可簡化上述習知的製程步驟，同時提昇閘極電極與自對準接觸窗之間的隔離效果。

為達上述目的，本發明提供一種簡化的自對準接觸窗製程，其特徵在於將側壁層的回蝕刻合併在接觸窗的蝕刻。如此一來，除了可省略側壁層的回蝕刻步驟外，再者，由於側壁層的材料本身可作為蝕刻阻障層，不需要沈積額外的阻障層在接觸區上，因此又可減少一道沈積步驟。



五、發明說明 (4)

根據本發明的方法，其主要步驟包括：(a)提供一半導體基底，其上形成複數個電晶體元件，分別包括一閘極和一對源/汲極擴散區，閘極上並形成有一絕緣覆蓋層；(b)形成一阻障層覆蓋在基底與電晶體元件上；(c)形成一平坦的絕緣層覆蓋在阻障層上；(d)以阻障層為蝕刻終止層，選擇性地蝕刻該絕緣層，以形成一自對準窗口對應於源/汲極擴散區；以及(e)非等向性地蝕刻窗口底下之阻障層，以露出源/汲極擴散區作為接觸區，同時於閘極的側壁形成一側壁層。

為讓本發明之上述和其他目的、特徵、和優點能更明顯易懂，下文特舉一較佳實施例，並配合所附圖式，作詳細說明如下：

【圖式之簡單說明】

第1A~1E圖為一系列剖面圖，用以說明習知製作自對準接觸窗的流程。

第2A~2D圖為一系列剖面圖，用以說明本發明一較佳實施例製作自對準接觸窗的流程。

【符號說明】

- 10、50~半導體基底；
- 12、52~閘氧化層；
- 14、54~閘極；
- 16、56~閘極覆蓋層；
- 18、58~源/汲極擴散區；



五、發明說明 (5)

- 20、60~薄氧化層；
- 22、24、62~氮化矽層；
- 26、64~內層介電層；
- 28、66~光阻層；
- 29、67~自對準接觸窗。

【實施例】

以下將配合第2A~2D圖詳細說明本發明製作自對準接觸窗的流程。首先，如第2A圖所示，在半導體基底50先以傳統之製程技術形成複數個電晶體元件，其分別包括閘極氧化層52、閘極54、源/汲極擴散區58。閘極54通常是由一層複晶矽與一層矽化金屬(如 WSi_2)所共同組成的複晶矽化金屬(polycide)，另外在閘極上方具有一層材質為氮化矽的覆蓋層(cap layer)56。接著，在800~1100℃之製程溫度下，以一道快速熱氧化(RTO; rapid thermal oxidation)製程，在基底50表面及閘極54側壁形成一層厚約150埃的薄氧化層60。此薄氧化層60可在後續的蝕刻程序中保護源/汲極擴散區58，同時藉由該熱製程可修補基底表面的缺陷。

請參照第2B圖，以低壓化學氣相沈積法(LPCVD)沈積一氮化矽阻障層62，覆蓋在基底既有之元件上。在本發明中，此氮化層62兼具習知技術中的閘極側壁層與自對準接觸蝕刻的蝕刻終止層兩種功能，其厚度約在100~500埃之間，較佳約200~350埃左右。



五、發明說明 (6)

請參照第2C圖與第2D圖，接下來有別於習知程序，本發明略過以回蝕刻形成側壁層以及沈積氮化矽阻障層的步驟(如前文中對應於第1B圖至1D圖之流程)，直接在基底上沈積一種或一種以上的絕緣材料，例如氧化矽、硼磷矽玻璃、旋塗式玻璃等，並將之平坦化，作為內層介電層(Inter Layer Dielectrics; ILD) 64。

之後，以光阻圖案66為罩幕，依序定義介電層64、氮化矽層62、薄氧化矽層60，以形成一自對準窗口67，如第2D圖所示。首先，以微影製程在介電層64上形成一光阻罩幕66，露出欲形成自對準接觸窗的區域，然後選擇性的蝕刻介電層64，形成一對應於源/汲極擴散區58的窗口。蝕刻過程中，利用氮化矽層62當作蝕刻終止層以達到自我對準的目的，並避免閘極遭到蝕刻損傷。接著，非等向性地蝕刻窗口底下之氮化矽層，以將源/汲極擴散區58上方的氮化矽層去除，並藉此同時在閘極54的側壁形成一氮化矽側壁層62a。將光阻66去除後，以一道氫氟酸的清洗程序將接觸窗底下的薄氧化矽層60去除，露出源/汲極擴散區58作為接觸區，即完成一自對準接觸窗的製程。之後的製程更包括：形成一導電層填入窗口67，藉此與接觸區58形成電性連接。

相較於習知製程，由於本發明中作為蝕刻終止層的氮化矽層62未經過回蝕刻的程序，因此在定義接觸窗時可提供額外的厚度(如第2C圖標號d所示)保護閘極免於遭到蝕刻損傷；而且此氮化矽層經過回蝕刻後，可提供一個完整



五、發明說明 (7)

的氮化矽側壁層，避免閘極與後續接觸金屬發生短路的機率。

由以上可知，本發明的簡化製程，藉由將側壁層回蝕刻與接觸窗的蝕刻合併，可減少一道回蝕刻步驟與一道阻障層的沈積步驟，有助於提高產能、減少成本。另外，藉由本發明的製程，可使閘極在蝕刻接觸窗時有較厚的蝕刻阻障層保護，可提高元件的可靠度與製程的操作容許度。

雖然本發明已以一較佳實施例揭露如上，然其並非用以限定本發明，任何熟習此技藝者，在不脫離本發明之精神和範圍內，當可作各種之更動與潤飾，因此本發明之保護範圍當視後附之申請專利範圍所界定者為準。



六、申請專利範圍

1. 一種自對準接觸窗製程，包括下列步驟：

(a) 提供一半導體基底，其上形成複數個電晶體元件，分別包括一閘極和一對源/汲極擴散區，該閘極上並形成有一絕緣覆蓋層；

(b) 形成一阻障層覆蓋在該基底與電晶體元件上；

(c) 形成一平坦的絕緣層覆蓋在該阻障層上；

(d) 以該阻障層為蝕刻終止層，選擇性地蝕刻該絕緣層，以形成一自對準窗口對應於該源/汲極擴散區；以及

(e) 非等向性地蝕刻該窗口底下之阻障層，以露出該源/汲極擴散區作為接觸區，同時於該閘極的側壁形成一側壁層。

2. 如申請專利範圍第1項所述之製程，其中在步驟(b)之前更包括：

以熱氧化法在該源/汲極擴散區表面與該閘極側壁形成一氧化層。

3. 如申請專利範圍第1項所述之製程，其中該絕緣覆蓋層為一氮化矽層。

4. 如申請專利範圍第1項所述之製程，其中該阻障層為一氮化矽層。

5. 如申請專利範圍第4項所述之製程，其中該氮化矽層的厚度為100~500埃。

6. 如申請專利範圍第1項所述之製程，其中該絕緣層包括一硼磷矽玻璃層。

7. 如申請專利範圍第1項所述之製程，其中步驟(c)包



六、申請專利範圍

括：

沈積一絕緣層覆蓋在該阻障層上；以及
將該絕緣層平坦化。

8. 如申請專利範圍第1項所述之製程，其中在步驟(e)
後更包括：

形成一導電層填入該窗口，藉此與該接觸區形成電性
連接。

9. 一種自對準接觸窗製程，包括下列步驟：

(a) 提供一半導體基底，其上形成複數個電晶體元件
，分別包括一閘極和一對源/汲極擴散區，該閘極上並形
成有一絕緣覆蓋層；

(b) 以熱氧化法在該源/汲極擴散區表面與該閘極側
壁形成一氧化層；

(c) 形成一氮化矽層覆蓋在該基底與電晶體元件上；

(d) 形成一平坦的絕緣層覆蓋在該阻障層上；

(e) 以該氮化矽層為蝕刻終止層，選擇性地蝕刻該絕
緣層，以形成一自對準窗口對應於該源/汲極擴散區；

(f) 非等向性地蝕刻該窗口底下之氮化矽層，於該閘
極的側壁形成一氮化矽側壁層，並露出該源/汲極擴散區
表面之氧化層；以及

(g) 去除該源/汲極擴散區表面之氧化層，露出該源/
汲極擴散區作為接觸區。

10. 如申請專利範圍第9項所述之製程，其中該絕緣覆
蓋層為一氮化矽層。



六、申請專利範圍

11. 如申請專利範圍第9項所述之製程，其中步驟(c)該氮化矽層的厚度為100~500埃。

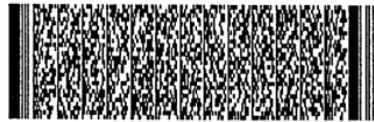
12. 如申請專利範圍第9項所述之製程，其中該絕緣層包括一硼磷矽玻璃層。

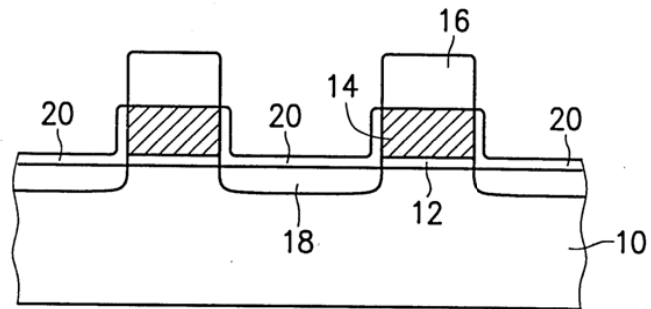
13. 如申請專利範圍第9項所述之製程，其中步驟(d)包括：

沈積一絕緣層覆蓋在該阻障層上；以及
將該絕緣層平坦化。

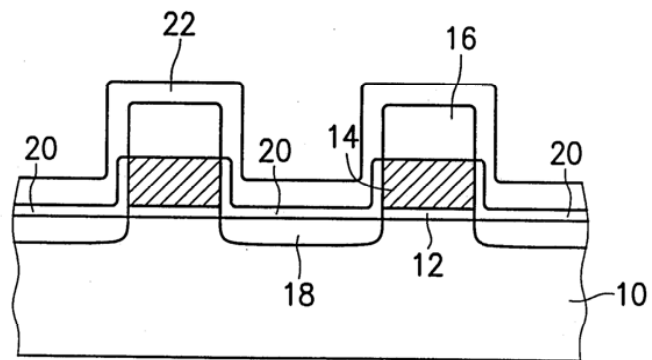
14. 如申請專利範圍第9項所述之製程，其中在步驟(g)之後更包括：

形成一導電層填入該窗口，藉此與該接觸區形成電性連接。

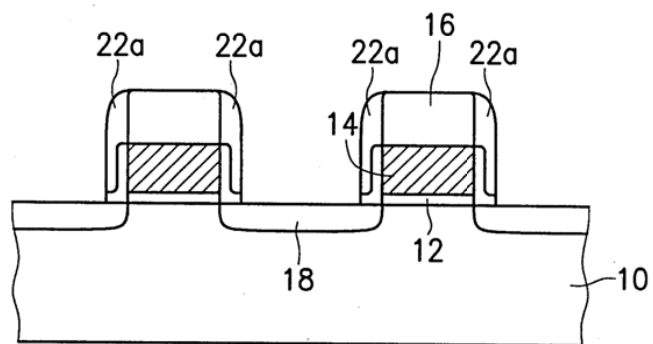




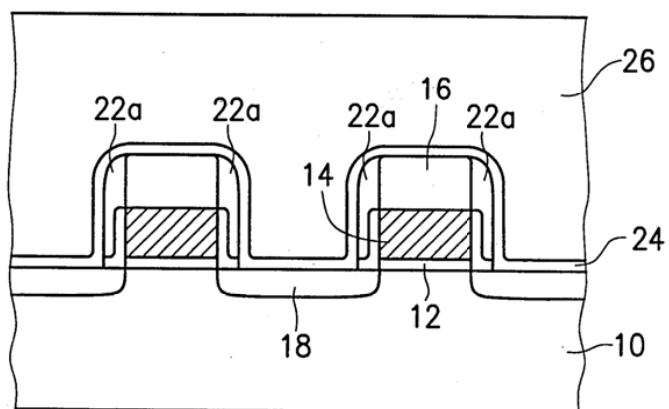
第1A圖



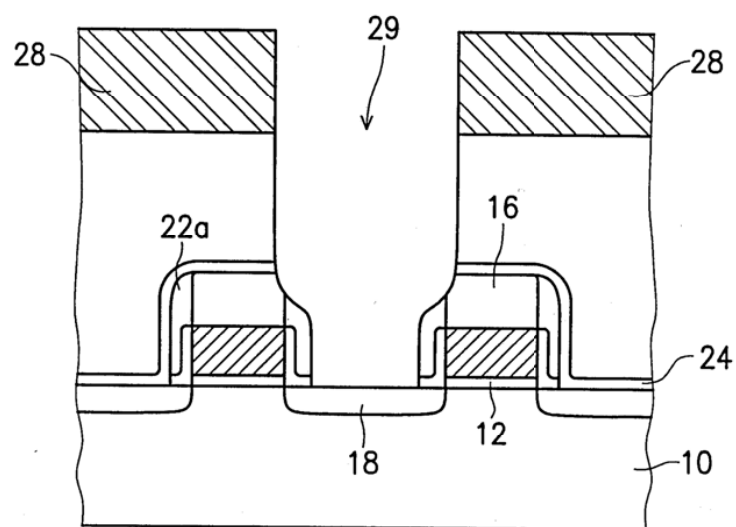
第1B圖



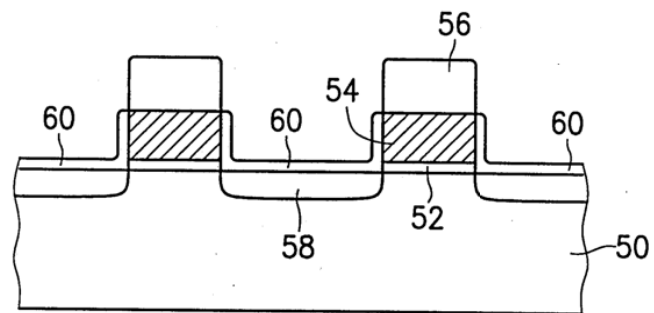
第 1C 圖



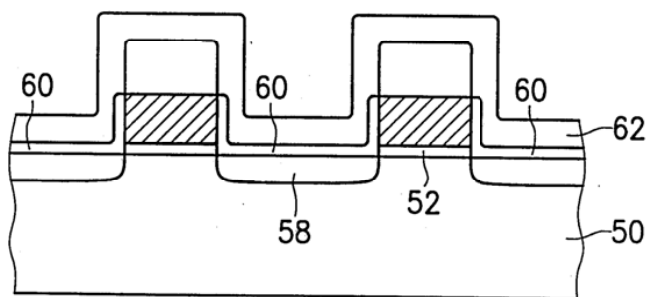
第 1D 圖



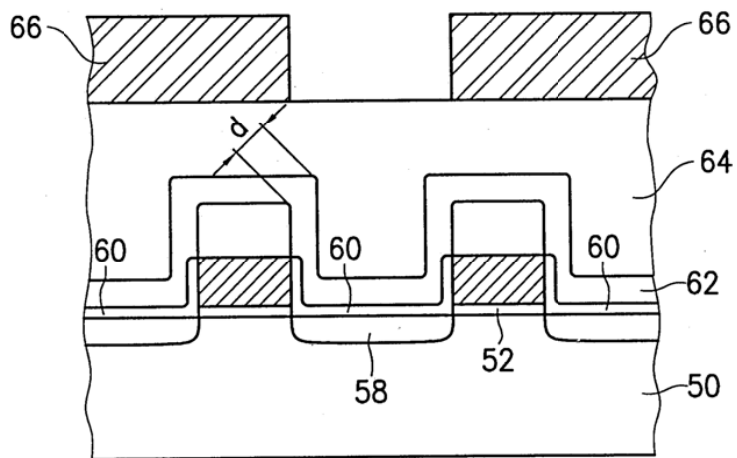
第 1E 圖



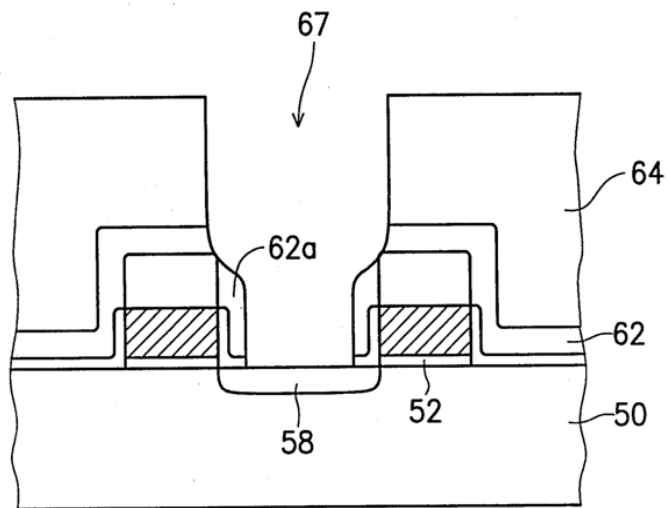
第2A圖



第2B圖



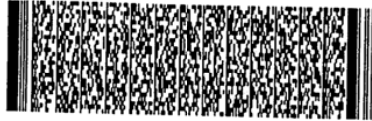
第2C圖



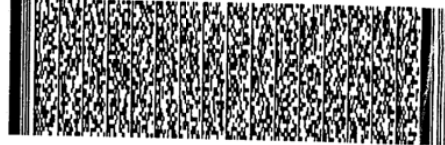
第2D圖

申請案件 稱:自對準接觸窗製程

第 1/13 頁



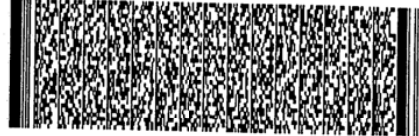
第 2/13 頁



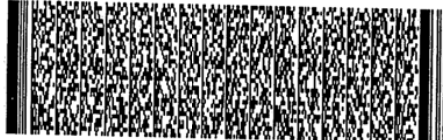
第 4/13 頁



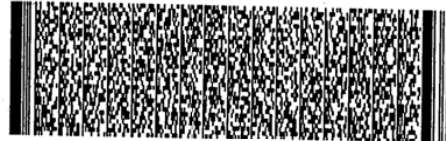
第 4/13 頁



第 5/13 頁



第 5/13 頁



第 6/13 頁



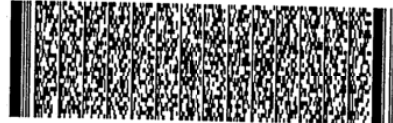
第 6/13 頁



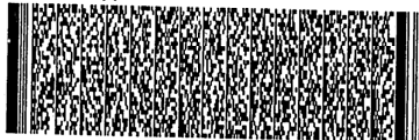
第 7/13 頁



第 7/13 頁



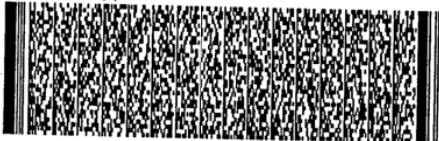
第 8/13 頁



第 8/13 頁



第 9/13 頁



第 9/13 頁



第 10/13 頁



第 11/13 頁



申請案件 稱:自對準接觸窗製程

第 11/13 頁



第 12/13 頁



第 12/13 頁



第 13/13 頁





UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

09/407268

APPLICATION NO. 09/407268	FILING DATE 03/29/99	FIRST NAMED INVENTOR LIU	ATTORNEY DOCKET NO. 120662000600
------------------------------	-------------------------	-----------------------------	-------------------------------------

MORRISON & FOERSTER LLP
2000 PENNSYLVANIA AVENUE NW
WASHINGTON DC 20006-1888

MM42/0302

EXAMINER DANG, P

ART UNIT 2818	PAPER NUMBER
------------------	--------------

DATE MAILED: 03/02/00

#3

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/407,268	LIU ET AL.	
	Examiner	Art Unit	
	Phuc T. Dang	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

1) ☐ Responsive to communication(s) filed on ____.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-14 is/are pending in the application.

 4a) Of the above claim(s) ____ is/are withdrawn from consideration.

5) ☐ Claim(s) ____ is/are allowed.

6) ☒ Claim(s) 1-14 is/are rejected.

7) ☐ Claim(s) ____ is/are objected to.

8) ☐ Claims ____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on ____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

 a) ☒ All b) ☐ Some * c) ☐ None of the CERTIFIED copies of the priority documents have been:

 1. ☐ received.

 2. ☒ received in Application No. (Series Code / Serial Number) 88/107,602.

 3. ☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

 * See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

14) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	17) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). ____
15) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	18) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
16) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____	19) <input type="checkbox"/> Other: _____

Application/Control Number: 09/407,268
Art Unit: 2818

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement submitted on 12/13/1999 was filed after the mailing date of the instant application on 9/29/1999. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the petition is granted and the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 4, 6, 8-9, 12 and 14 are rejected under 35 U.S.C. 102(b) as being participated by Iguchi et al. (U. S. Patent No. 5,734,185).

The reference teaches every positive step of the claimed invention in that it discloses a method for forming a self-aligned contact hole, comprising the steps of :

Application/Control Number: 09/407,268
Art Unit: 2818

- a) providing a semiconductor substrate having a gate electrode and a diffusion region;
- b) forming a conformal layer of etch barrier material overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode;
- c) forming an insulating layer overlying the barrier layer;
- d) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop; and
- e) anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etch barrier material on the sidewall of the gate electrode (see column 4, line 40 to column 5, line 15) as cited in claims 1 and 9 and the step of forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode by thermal oxidation prior to forming the barrier layer (see column 13, lines 38-43) as cited in claim 2 and the barrier layer layer is a silicon nitride (see column 18, lines 60-62) as cited in claim 4 and the insulating layer comprises a layer of borophosphosilicate glass (see column 10, lines 53-55) as cited in claims 6 and 12 and further comprising forming a conductive plug in the opening to electrically connect to the diffusion region (see column 10, lines 50-52) as cited in claims 8 and 14.

Application/Control Number: 09/407,268
Art Unit: 2818

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 5, 7, 11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iguchi et al. as applied to claims above, and further in view of Ying (U.S. Patent No. 5,753,547).

4. Iguchi et al. teach all the limitations of the method as noted above except for the teaching of the barrier layer and the conformal layer of silicon nitride have a thickness between about 100 to 500 angstroms (see column 4, lines 59-65) as cited in claims 5 and 11 and the steps of depositing an insulating layer overlying the barrier layer and planarizing the insulating layer (see ABSTRACT) as cited in claims 7 and 13.

It would have been obvious to one having ordinary skill in the art to have used the teaching from Ying in Iguchi et al. process of forming a self-aligned contact hole since it would reduce the process steps, complexity, time and cost.

5. Claims 3 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lepseller et al. (U.S. Patent No. 4,675,715).

Lepseller et al. teach the gate electrode comprising of a capping layer of silicon nitride (see column 5, lines 13-17) as cited in claims 3 and 10.

Application/Control Number: 09/407,268
Art Unit: 2818

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuc T. Dang whose telephone number is 703-305-1080. The examiner can normally be reached on 8:00 am-5:00 pm.
7. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on 703-308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7382 for regular communications and 703-308-5841 for After Final communications.
8. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

February 23, 2000


David Nelms
Supervisory Patent Examiner
Technology Center 2800

Phuc T. Dang *PD*
Examiner
Art Unit 2818

Notice of References Cited				Application/Control No.		Applicant(s)/Patent Under Reexamination			
				09/407,268		LIU ET AL.			
				Examiner		Art Unit			
				Phuc T. Dang		2818			
U.S. PATENT DOCUMENTS									
*		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	DOCUMENT SOURCE **		
							APS	OTHER	
<input type="checkbox"/>	A	5,734,185	Mar. 1998	Iguchi et al.	257	336	<input type="checkbox"/>	<input type="checkbox"/>	
<input type="checkbox"/>	B	5,753,547	May. 1998	Ying	438	253	<input type="checkbox"/>	<input type="checkbox"/>	
<input type="checkbox"/>	C	4,675,715	Jun. 1987	Lepselter et al.	357	59	<input type="checkbox"/>	<input type="checkbox"/>	
<input type="checkbox"/>	D	5,545,579	Aug. 1996	Liang et al.	437	44	<input type="checkbox"/>	<input type="checkbox"/>	
<input type="checkbox"/>	E	5,623,153	Apr. 1997	Liang et al.	257	336	<input type="checkbox"/>	<input type="checkbox"/>	
<input type="checkbox"/>	F						<input type="checkbox"/>	<input type="checkbox"/>	
<input type="checkbox"/>	G						<input type="checkbox"/>	<input type="checkbox"/>	
<input type="checkbox"/>	H						<input type="checkbox"/>	<input type="checkbox"/>	
<input type="checkbox"/>	I						<input type="checkbox"/>	<input type="checkbox"/>	
<input type="checkbox"/>	J						<input type="checkbox"/>	<input type="checkbox"/>	
<input type="checkbox"/>	K						<input type="checkbox"/>	<input type="checkbox"/>	
<input type="checkbox"/>	L						<input type="checkbox"/>	<input type="checkbox"/>	
<input type="checkbox"/>	M						<input type="checkbox"/>	<input type="checkbox"/>	
FOREIGN PATENT DOCUMENTS									
*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUBCLASS	DOCUMENT SOURCE **	
								APS	OTHER
<input type="checkbox"/>	N							<input type="checkbox"/>	<input type="checkbox"/>
<input type="checkbox"/>	O							<input type="checkbox"/>	<input type="checkbox"/>
<input type="checkbox"/>	P							<input type="checkbox"/>	<input type="checkbox"/>
<input type="checkbox"/>	Q							<input type="checkbox"/>	<input type="checkbox"/>
<input type="checkbox"/>	R							<input type="checkbox"/>	<input type="checkbox"/>
<input type="checkbox"/>	S							<input type="checkbox"/>	<input type="checkbox"/>
<input type="checkbox"/>	T							<input type="checkbox"/>	<input type="checkbox"/>
NON-PATENT DOCUMENTS									
*		DOCUMENT (Including Author, Title Date, Source, and Pertinent Pages)						DOCUMENT SOURCE **	
								APS	OTHER
<input type="checkbox"/>	U							<input type="checkbox"/>	<input type="checkbox"/>
<input type="checkbox"/>	V							<input type="checkbox"/>	<input type="checkbox"/>
<input type="checkbox"/>	W							<input type="checkbox"/>	<input type="checkbox"/>
<input type="checkbox"/>	X							<input type="checkbox"/>	<input type="checkbox"/>

*A copy of this reference is not being furnished with this Office action. (See Manual of Patent Examining Procedure, Section 707.05(a).)
 **APS encompasses any electronic search i.e. text, image, and Commercial Databases.
 U.S. Patent and Trademark Office
 PTO-892 (Rev. 03-98)

Notice of References Cited

Part of Paper No. 3

818

PATENT
Docket No. 420662000600

CERTIFICATE OF HAND DELIVERY

I hereby certify that this correspondence is being hand filed with the United States Patent and Trademark Office in Washington, D.C. on
May 31, 2000.

Sherri N. Shipe
Sherri N. Shipe

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

Jacson LIU et al.

Serial No.: 09/407,268

Filing Date: September 29, 1999

For: METHOD FOR FORMING SELF-
ALIGNED CONTACT HOLE



Examiner: Phuc T. DANG

Group Art Unit: 2818

6/6/00
Smith
RECEIVED
JUN - 1 2000
TC 2800 MAIL ROOM

REQUEST FOR RECONSIDERATION UNDER 37 CFR 1.111

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action mailed March 2, 2000, Applicants submit the following remarks and request reconsideration of the pending claims.

REMARKS

Claims 1-14 are pending in the application and are presented for reconsideration.

Claims 1, 2, 4, 6, 8, 9, 12, and 14 were rejected under 35 USC 102(b) as being anticipated by U.S. Patent No. 5,734,185 to Iguchi, et al. ("Iguchi"). This rejection is respectfully traversed.

Applicants submit that Iguchi fails to teach or disclose forming a spacer after forming a contact hole in the insulating layer using self-aligned technology. Claim 1, for example, recites "etching an opening through the insulating layer self aligned...anisotropically etching the barrier

dc-210117

layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etched barrier material on the side wall of the gate electrode." By not forming the spacer of gate electrodes until a contact opening is formed, the claimed invention has the advantage of allowing the conformal layer to serve as an etch barrier that protects the diffusion region during the contact hole etching. Thus, the claimed invention has the additional advantage of not needing to deposit another etch barrier layer. Iguchi fails to provide these advantages because of the method of forming the spacers taught, namely forming spacers before the gate electrodes.

Iguchi teaches a step of forming plural spacers (16a) before the gate electrodes 19 and 20 formed. See column 14, line 43 to column 15, line 15. After forming the gate electrodes 19 and 20, source/drain regions 31 and 32 are formed in the substrate. Then, an interlayer insulating film is formed over the gate electrodes in the source/drain regions. Further, the process taught by Iguchi prevents the use of self-aligning technology because contact holes formed in the interlayer insulating film that expose the source/drain regions cannot be formed using the self-aligning technology in conjunction with the process taught by Iguchi as apparent to those of ordinary skill in the art.

The Examiner cites column 4, line 40 to column 5, line 15 as support for the proposition that Iguchi teaches forming a spacer of the etch barrier material on the side wall of the gate electrode after the gate electrode has been formed. However, Applicants submit that this portion of the specification is misleading. By reference to column 13, line 38 to column 15, line 15 and Figs. 2A-D, 3E-H and 4I-L, it is apparent that the spacers 16a are formed (see Figs. 3F and 3G) before gate electrodes 19 and 20 (see Figs. 4I and 4J). Further, the claims recite providing the gate electrodes and substrate before forming portions of the transistor, whereas Iguchi teaches forming portions of the transistor prior to forming the gate electrodes. Thus, Iguchi teaches forming the contact hole before forming the spacers 16a and forming the spacers 16a before the gate electrodes 19 and 20.

Independent claim 9 includes features similar to those recited in claim 1, and the remaining dependent claims depend from claims 1 and 9, including all the features recited therein. As stated above, Iguchi fails to teach or suggest each and every element recited in claim 1. Therefore, Iguchi also fails to teach or suggest all of the features recited in claims 2-14. Accordingly, Applicants respectfully request the withdrawal of the rejection of claims 1, 2, 4, 6, 8, 9, 12, and 14 under 35 USC 102(b).

Claims 5, 7, 11, and 13 were rejected under 35 USC 103(a) as being unpatentable over Iguchi in view of U.S. Patent No. 5,753,547 to Ying ("Ying"). This rejection is respectfully traversed.

As stated above, Iguchi fails to teach or suggest each and every feature in the independent claims 1 and 9. Further, Ying fails to teach or suggest the missing features of Iguchi. Thus, Iguchi, alone or in combination with Ying, fails to teach or suggest each and every element of claims 1 and 9. Claims 5 and 7 depend from claim 1 and claims 11 and 13 depend from claim 9. Therefore, Iguchi, alone or in combination with Ying, fails to teach or suggest each and every element in claims 5, 7, 11, and 13. Accordingly, Applicants respectfully request the withdrawal of the rejection of claims 5, 7, 11, and 13 under 35 USC 103(a).

Claims 3 and 10 were rejected under 35 USC 103(a) as being unpatentable over US Patent No. 4,675,715 to Lepselter, et al. ("Lepselter"). This rejection is respectfully traversed.

Applicants submit that Lepselter suffers from the same deficiencies cited with respect to Iguchi above. Namely, Lepselter fails to teach or disclose forming a spacer after forming a contact hole in the insulating layer using self-aligned technology. Thus, Lepselter fails to teach or suggest each and every feature in the independent claims 1 and 9. Claim 3 depends from claim 1 and claim 10 depends from claim 9. Therefore, Lepselter fails to teach or suggest each and every element in claims 3 and 10. Accordingly, Applicants respectfully request the withdrawal of the rejection of claims 3 and 10 under 35 USC 103(a).

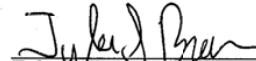
Applicants respectfully submit that all of the pending claims are in condition for allowance, which action is requested.

In the event that the transmittal letter is separated from this document and the Patent and Trademark Office determines that an extension and/or other relief is required, Applicants petition for any required relief including extensions of time and authorize the Assistant Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952**, referencing docket no. 420662000600. However, the Assistant Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Respectfully submitted,

Dated: May 31, 2000

By:


Tyler S. Brown
Registration No. 36,465

Morrison & Foerster LLP
2000 Pennsylvania Avenue, N.W.
Washington, D.C. 20006-1888
Telephone: (202) 887-1545
Facsimile: (202) 887-0763



**UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office**

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
-----------------	-------------	----------------------	---------------------

09/407,268 09/29/99 LIU

J 420662000600

MORRISON & FOERSTER LLP
2000 PENNSYLVANIA AVENUE NW
WASHINGTON DC 20006-1888

MMC2/0614

EXAMINER

DANG, P

ART UNIT

PAPER NUMBER

2818

DATE MAILED:

06/14/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Notice of AllowabilityApplication No.
09/407,268

Applicant(s)

Jacson Liu

Examiner

Phuc Dang

Group Art Unit

2818

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance and Issue Fee Due or other appropriate communication will be mailed in due course.

☒ This communication is responsive to May 31, 2000.

☒ The allowed claim(s) is/are 1-14.

☒ The drawings filed on Sep 29, 1999 are acceptable.

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been
☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

A SHORTENED STATUTORY PERIOD FOR RESPONSE to comply with the requirements noted below is set to EXPIRE THREE MONTHS FROM THE "DATE MAILED" of this Office action. Failure to timely comply will result in ABANDONMENT of this application. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.

☐ Applicant MUST submit NEW FORMAL DRAWINGS

☐ because the originally filed drawings were declared by applicant to be informal.

☐ including changes required by the Notice of Draftsperson's Patent Drawing Review, PTO-948, attached hereto or to Paper No. _____.

☐ including changes required by the proposed drawing correction filed on _____, which has been approved by the examiner.

☐ including changes required by the attached Examiner's Amendment/Comment.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the reverse side of the drawings. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

☐ Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Any response to this letter should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included.

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

☐ Interview Summary, PTO-413

☐ Examiner's Amendment/Comment

☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material

☒ Examiner's Statement of Reasons for Allowance

David Nelms
Supervisory Patent Examiner
Technology Center 2800

DETAILED ACTION

Response to Amendment

1. This office action is in response to amendment filed on May 31, 2000.
 - Claims 1-14 are pending in the application.

Examiner's Statement of Reasons for Allowance

2. The following is an examiner's statement of reasons for allowance:

The prior art of record fail to teach or fairly suggest a method for forming a self-aligned contact hole, comprising the steps of providing a semiconductor substrate having a gate electrode and a diffusion region; forming a conformal layer of etch barrier material overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode; forming an insulating layer overlying the barrier layer; etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop; and anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etch barrier material on the sidewall of the gate electrode

In the present invention, the steps of anisotropically etching the barrier layer underneath the opening to increase the electrode area of the semiconductor devices..


3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submission should be clearly labeled "Comments on Statement of Reasons for Allowance".

Application/Control Number: 09/407,268

Page 3

Art Unit: 2818

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuc T. Dang whose telephone number is 703-305-1080. The examiner can normally be reached on 8:00 am-5:00 pm.
5. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on 703-308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-5841 for regular communications and 703-308-5841 for After Final communications.
6. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.


David Nelms
Supervisory Patent Examiner
Technology Center 2800

Phuc T. Dang PD
Examiner
Art Unit 2818

June 12, 2000

Notice of References Cited				Application No. 09/407,268		Applicant(s) Jacson Liu	
				Examiner Phuc Dang		Group Art Unit 2818	
U.S. PATENT DOCUMENTS							
	DOCUMENT NO.	DATE	NAME		CLASS	SUBCLASS	
A	5,436,188	7/1995	Chen		437	52	
B							
C							
D							
E							
F							
G							
H							
I							
J							
K							
L							
M							
FOREIGN PATENT DOCUMENTS							
	DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUBCLASS	
N							
O							
P							
Q							
R							
S							
T							
NON-PATENT DOCUMENTS							
	DOCUMENT (Including Author, Title, Source, and Pertinent Pages)					DATE	
U							
V							
W							
X							



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

NOTICE OF ALLOWANCE AND ISSUE FEE DUE

MORRISON & FOERSTER LLP
2000 PENNSYLVANIA AVENUE NW
WASHINGTON DC 20006-1888

MMC2/0614

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
09/407,268	09/29/99	014	DANG, P	2818 06/14/00
First Named Applicant	LIU, 35 USC 154(b) term ext. = 0 Days.			
TITLE OF INVENTION	METHOD FOR FORMING SELF-ALIGNED CONTACT HOLE			

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
0	420662000600	438-639.000	N94 UTILITY	NO	\$1210.00	09/14/00

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.

HOW TO RESPOND TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

- A. If the status is changed, pay twice the amount of the FEE DUE shown above and notify the Patent and Trademark Office of the change in status, or
- B. If the status is the same, pay the FEE DUE shown above.

If the SMALL ENTITY is shown as NO:

- A. Pay FEE DUE shown above, or
- B. File verified statement of Small Entity Status before, or with, payment of 1/2 the FEE DUE shown above.

II. Part B-Issue Fee Transmittal should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B Issue Fee Transmittal should be completed and returned. If you are charging the ISSUE FEE to your deposit account, section "4b" of Part B-Issue Fee Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give application number and batch number. Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PATENT AND TRADEMARK OFFICE COPY

PTOL-85 (REV. 10-98) Approved for use through 06/30/99. (0651-0033)

PART B—ISSUE FEE TRANSMITTAL

Complete and mail this form, together with applicable fees, to: **Box ISSUE FEE**
Assistant Commissioner for Patents
Washington, D.C. 20231

MAILING INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE. Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Issue Fee Receipt, the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

MORRISON & FOERSTER LLP
 2000 PENNSYLVANIA AVENUE NW
 WASHINGTON DC 20006-1888

MMC2/0614



Note: The certificate of mailing below can only be used for domestic mailings of the Issue Fee Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing.

Certificate of Mailing

I hereby certify that this Issue Fee Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above on the date indicated below.

LaVerne Whetstone (Depositor's name)

(Signature)

July 24, 2000 (Date)

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
09/407,268	09/29/99	014	DANG, P	2818 06/14/00
First Named Applicant	LIU, 35 USC 154(b) term ext. = 0 Days.			

TITLE OF INVENTION: METHOD FOR FORMING SELF-ALIGNED CONTACT HOLE

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
0 420662000600	438-639.000	N84	UTILITY	NO	\$1210.00	09/14/00

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363). Use of PTO form(s) and Customer Number are recommended, but not required.

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47) attached.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

Morrison & Foerster LLP

2 _____
 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the PTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE
 Mosel Vitelic, Inc.

(B) RESIDENCE: (CITY & STATE OR COUNTRY)

Hsinchu, Taiwan

Please check the appropriate assignee category indicated below (will not be printed on the patent)

☐ individual ☒ corporation or other private group entity ☐ government

4a. The following fees are enclosed (make check payable to Commissioner of Patents and Trademarks):

☒ Issue Fee
☒ Advance Order - # of Copies 6

4b. The following fees or deficiency in these fees should be charged to:

DEPOSIT ACCOUNT NUMBER 03-1952
 (ENCLOSE AN EXTRA COPY OF THIS FORM)

☐ Issue Fee
☐ Advance Order - # of Copies

The COMMISSIONER OF PATENTS AND TRADEMARKS IS requested to apply the Issue Fee to the application identified above.

(Authorized Signature) Barry E. Bretschneider Reg. 29,055

(Date)

NOTE: The Issue Fee will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the Patent and Trademark Office.

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending on the needs of the individual case. Any comments on the amount of time required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND FEES AND THIS FORM TO: Box Issue Fee, Assistant Commissioner for Patents, Washington D.C. 20231

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

07/25/2000 HND0R2 00000010 09407268

01 FC:142
 02 FC:561

1210.00 GP
 18.00 GP

TRANSMIT THIS FORM WITH FEE

PTOL-85B (REV. 10-96) Approved for use through 06/30/99. OMB 0651-0033

Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

55er

PATENT APPLICATION FEE DETERMINATION RECORD Effective November 10, 1998					Application or Docket Number	
CLAIMS AS FILED - PART I						
		(Column 1)	(Column 2)			
FOR		NUMBER FILED	NUMBER EXTRA			
BASIC FEE						
TOTAL CLAIMS		14	minus 20 =	*		
INDEPENDENT CLAIMS		2	minus 3 =	*		
MULTIPLE DEPENDENT CLAIM PRESENT						
* If the difference in column 1 is less than zero, enter "0" in column 2						
CLAIMS AS AMENDED - PART II						
		(Column 1)	(Column 2)	(Column 3)		
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	
	Total	*	Minus	**	=	
	Independent	*	Minus	***	=	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM					
		(Column 1)	(Column 2)	(Column 3)		
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	
	Total	*	Minus	**	=	
	Independent	*	Minus	***	=	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM					
		(Column 1)	(Column 2)	(Column 3)		
AMENDMENT C		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	
	Total	*	Minus	**	=	
	Independent	*	Minus	***	=	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM					
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20." *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3." The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.						

SMALL ENTITY TYPE <input type="checkbox"/>		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
	380.00	OR		760.00
X\$ 9=		OR	X\$18=	
X39=		OR	X78=	
+130=		OR	+260=	
TOTAL		OR	TOTAL	760

SMALL ENTITY TYPE <input type="checkbox"/>		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X\$ 9=		OR	X\$18=	
X39=		OR	X78=	
+130=		OR	+260=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

SMALL ENTITY TYPE <input type="checkbox"/>		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X\$ 9=		OR	X\$18=	
X39=		OR	X78=	
+130=		OR	+260=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	