

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of:     Liu *et al.*  
U.S. Patent No.:    6,146,997  
Issue Date:          Nov. 14, 2000  
Appl. Serial No.:    09/407,268  
Filing Date:         Sep. 29, 1999  
Title:                METHOD FOR FORMING SELF-ALIGNED CONTACT  
                         HOLE

### **DECLARATION OF DR. GARY W. RUBLOFF**

1.     My name is Gary W. Rubloff. I am a Director at the Maryland NanoCenter, a Director at the Center for Nanostructures for Electrical Energy Storage (NEES), and a Minta Martin Professor of Engineering at the University of Maryland at College Park. I also serve from time to time as an independent consultant providing expertise in several technical fields, including thin film transistor technology, advanced process controls, semiconductor materials, semiconductor processes, and semiconductor manufacturing. I have been asked to offer technical opinions relating to U.S. Patent No. 6,146,997, and prior art references relating to its subject matter. My current *curriculum vitae* is attached as Ex. 1004 and some highlights follow.

2.     I earned my M.S. (1967) and Ph.D. (1971) in Physics from the University of Chicago after earning my B.S. (1966) in Physics from Dartmouth College.

3. After completing my Ph.D., I worked for IBM's Thomas J. Watson Research Center, where, over a 20 year period from 1973 to 1993, I carried out research as a Research Staff Member and served in several research management positions. My focus was initially in surface and interface science, particularly the consequences of chemical reactions which lead to silicide compound formation, with broad implications in VLSI/ULSI technology. After this I worked as Technical Assistant to a Research Vice-President, which gave me a broad appreciation and interaction with leadership in Silicon Technology, GaAs, Packaging, and Optoelectronics areas being pursued by IBM Research. Then, as manager and senior manager for the Thin Film Materials and Processing group in the Silicon Technology Department, I led research in integrated processing, which represented the research counterpart of cluster tool processing in manufacturing. This program included surface cleaning, thermal oxidation, chemical vapor deposition, physical vapor deposition, plasma processing, and electrical and structural characterization. Subsequently as manager for the Thin Film Process Modeling group in the Manufacturing Research Department, I supervised modeling and simulation efforts directed at chemical vapor deposition and plasma processing, ranging from fundamental chemistry to its implications for manufacturing equipment design.

4. After IBM I served at North Carolina State University (NSCU) as a professor in the Department of Electrical Engineering and Associate Director of the Center for Advanced Electronic Materials Processing, a large program on silicon device processing sponsored by the National Science Foundation (NSF) Engineering Research Center (ERC) program, the Semiconductor Research Corporation (SRC), and Sematech. At the University of Maryland at College Park (UMCP), I have served in several leadership position. Upon joining I became Director of the Institute for Systems Research ([www.isr.umd.edu](http://www.isr.umd.edu)), an NSF ERC. An important research outcome was my collaboration with other faculty groups to address – also with NSF and SRC support – how to create a platform for understanding and optimizing equipment and process technology with factory flow logistics.

5. In 2004, I founded the Maryland NanoCenter ([www.nanocenter.umd.edu](http://www.nanocenter.umd.edu)), which to the present day, helps coordinate nanotechnology research and educational programs at UMCP. As founding director, I continue to supervise a large clean room and microscopy infrastructure, maintain a general picture of the research directions of about 80 faculty member groups, and encourage the development of outstanding joint programs involving our faculty.

6. In 2009 I led a successful proposal to establish a new Energy Frontier Research Center supported by the Department of Energy. Entitled “Nanostructures for Electrical Energy Storage”, NEES seeks to elucidate the underpinnings for a new generation of nanostructure-based electrochemical energy storage ([www.efrc.umd.edu](http://www.efrc.umd.edu)). As Director I am able to guide this program and to ensure that it exploits at least in part the lessons I have learned from the silicon microelectronics industry, particularly in process and equipment technology, and in process integration. This year our achievements were recognized with a renewal of this large program (\$25.2M to date, now involving 10 institutions across the country).

7. During my time at the various positions noted above, I authored over 250 journal publications and numerous conference presentations . Some of these publications lie in areas of possible relevance to the patent at issue, reflected in the examples as follows: **silicides**: "Microscopic Compound Formation at the Pd/Si(111) Interface," *Phys. Rev. Lett.* 43, pp. 1836, 1979; "Microscopic Properties and Behavior of Silicide Interfaces," *Surface Science*, 132, pp. 268-314, 1983; **metal-oxide-semiconductor (MOS) devices**: "High-Temperature SiO<sub>2</sub> Decomposition at the SiO<sub>2</sub>/Si Interface," *Phys. Rev. Lett.* 55, pp. 2332, 1985; "Defect Formation in Thermal SiO<sub>2</sub> by High Temperature Annealing," *Appl. Phys. Lett.* 49, pp. 1525, 1986; "Defect Generation in MOS Structures Correlated with

the Interface Reaction of Si and SiO<sub>2</sub>," *Proceedings of the European Materials Research Society Meeting Symposium A*, Strasbourg, France, June 17-20, 1986; "Defect Microchemistry at the SiO<sub>2</sub>/Si Interface," *Phys. Rev. Lett.* 58, pp. 2379, 1987; "Role of Surface Passivation in the Integrated Processing of MOS Structures," Digest of Technical Papers, 1990 Symposium on VLSI Technology, IEEE Cat. No. 90CH2874-6, 10-1, pp. 117-118, 1990; **integrated processing and cluster tools**: "Ultraclean, Integrated Processing of Thermal Oxide Structures," *Appl. Phys. Lett.* 57, pp. 1254, 1990; "Integrated Processing for Microelectronics Science and Technology," *IBM J. Res. Devel.* 36 (2), pp. 233-276, 1992; "Concepts in Competitive Microelectronics Manufacturing," *J. Vac. Sci. Technol. B* 12 (4), pp. 2727-40, Jul/Aug 1994; "Evaluating the Impact of Process Changes on Cluster Tool Performance," *IEEE Trans. Semicond. Manuf.* 13 (2), pp. 181-192, May 2000; "Understanding the Impact of Equipment and Process Changes with a Heterogeneous Semiconductor Manufacturing Simulation Environment," *Proc. 2000 Winter Simulation Conference*, vol. 2, pp. 1491-1498, Orlando, FL, December 10-13, 2000; "Integrated Processing of MOS Gate Dielectric Structures," *IEEE Transactions on Semiconductor Manufacturing* 7 (1), pp. 96-100, Feb. 1994; **chemical vapor deposition (CVD)**: "CVD Growth of Rough-Morphology Silicon Films over a Broad Temperature Range," *Appl. Phys. Lett.* 63 (10), pp. 1387-89, Sept. 6, 1993; "Sub-Atmospheric CVD (SACVD) Ozone/TEOS

Process for SiO<sub>2</sub> Trench Filling,” *J. Vac. Sci. Technol. B* 13 (4), pp. 1888-92, Jul/Aug 1995, “Integrated Dynamic Simulation of Rapid Thermal Chemical Vapor Deposition of Polysilicon,” *IEEE Trans. Semicond. Manuf.* 11 (1), pp. 63-74, Feb. 1998; **tungsten chemical vapor deposition (W-CVD)**: “In-situ Sensing using Mass Spectrometry and its Use for Run-to-Run Control on a W CVD Cluster Tool,” *Characterization and Metrology for ULSI Technology: 2000 International Conference*, vol. 550, pp. 249-253, Gaithersburg, MD, 26-29 June 2000; “Run to Run Control in Tungsten CVD using H<sub>2</sub>/WF<sub>6</sub> at Low Pressures,” *J. Vac. Sci. Technol. B* 19 (5), pp. 1931-41, Sept/Oct 2001; “Process Diagnostics and Thickness Metrology using in-situ Mass Spectrometry for the Chemical Vapor Deposition of W from H<sub>2</sub>/WF<sub>6</sub>,” *J. Vac. Sci. Technol. B* 18 (3), pp. 1352-63, May/June 2000; **in-situ process sensing**: “Process Sensing and Metrology in Gate Oxide Growth by Rapid Thermal Chemical Vapor Deposition using SiH<sub>4</sub> and N<sub>2</sub>O,” *J. Vac. Sci. Technol. B* 17 (4), pp. 1417-23, Jul/Aug 1999.

8. I am also a named inventor for 25 issued U.S. patents. These patents include U.S. Patent No. 5,290,358, entitled “System for controlling thickness profile of deposited thin film layers over three-dimensional topography: gaseous reactant beam provision, beam collimation, specific angle of incidence of beam, reaction probability of beam with surface”; U.S. Patent No. 4,692,348, entitled “Low Temperature Shallow Doping of Si by Silicide Snowplow through

Polysilicon”; European Patent No. 0 187 706 A2, entitled “A method of coating an organic substrate with a metal”; European Patent No. 0 567 748 B1, entitled “Fabrication of rough silicon surfaces”; and U.S. Patent No. 6,821,910, entitled “Spatially programmable microelectronics process equipment using segmented gas injection showerhead with exhaust gas recirculation.”

9. My work has been recognized and appreciated by my peers in academia and in the industry. For example, I have been elected as a Fellow in the American Vacuum Society and the American Physical Society. I also received several invention and research awards at IBM. In 2000, I received the Gaede-Langmuir Prize from the American Vacuum Society for “the inventive application of surface science and vacuum technology to the semiconductor industry, and for fostering an effective bridge between AVS research and manufacturing”. This refers to my leadership role in developing ultraclean, integrated processing methods as a counterpart to the emergence and refinement of cluster tools for multi-chamber processing in manufacturing. In 2004, I was named a Minta Martin Professor by UMCP in recognition of my significant scholarly contributions to my areas of research.

10. I am familiar with the content of U.S. Patent No. 6,146,997 (the ’997 patent). Additionally, I have reviewed the following: U.S. Patent Number 6,277,720 (“Doshi”); U.S. Patent Number 5,770,498 (“Becker”); “Process Induced

Degradation of Thin Oxides” by Wong *et al.*, Proc. 1st Int. Symp. Ultra Large Scale Integration Sci. Technol. (1987) (“Wong”); and excerpts of the Webster’s Third New International Dictionary (1986), including definitions for the term “conform,” “conformal,” “over,” and “spacer.”

11. Counsel has informed me that I should consider these materials through the lens of one of ordinary skill in the art related to the ’893 patent at the time of the earliest purported priority date of the ’893 patent, and I have done so during my review of these materials. I believe one of ordinary skill as of December 9, 1996 (the filing date of U.S. Patent Application No. 08/760,665) would have a master’s degree or higher in electrical engineering, materials science, chemical engineering, physics, or chemistry, and two to three years of experience in the semiconductor processing industry. I base this on my own personal experience, including my knowledge of colleagues and others at the time.

12. I have no financial interest in either party or in the outcome of this proceeding. I am being compensated for my work as an expert on an hourly basis. My compensation is not dependent on the outcome of these proceedings or the content of my opinions.

13. My opinions, as explained below, are based on my education, experience, and background in the fields discussed above.

14. This declaration is organized as follows:



- I. Brief Overview of the '997 Patent (page 9)
- II. Terminology (page 14)
- III. Legal Standards for Prior Art (page 21)
- IV. Doshi (page 26)
- V. Becker and Combinations Based on Becker (page 38)
- VI. Conclusion (page 50)

**I. Brief Overview of the '997 Patent**

15. The '997 patent is directed to a method for “forming a self-aligned contact hole.” Ex. 1001, Abstract. Self-alignment is a technique in which multiple levels of regions on the wafer are formed using a single mask, where the mask contact window may be oversized relative to the contact area underneath. *Id.*, col. 1:11-20. More specifically, the '997 describes a method of forming a spacer structure that is used to form the self-aligned contact hole. As described below, a spacer can be used to define the boundary of the contact area of a self-aligned contact hole. Moreover, the spacer arranged between the contact area and an adjacent conductive structure (e.g., a gate electrode) can prevent shorting between the contact area and the adjacent conductive structure after the contact plug in the contact hole has been formed. *Id.*, col. 3:32-39.

16. According to the inventors of the '997 patent, in the conventional process, the formation of a spacer and the formation of a contact hole are two

separate processes. For example, referring to the annotated Fig. 1C of the '997 patent below, after gate electrodes 14 and diffusion regions 18 have been formed on a substrate 10, a conformal silicon nitride layer 22 is deposited over the gate electrodes 14 and the diffusion regions 18, and a spacer 22a of silicon nitride is formed by an anisotropic etch. *Id.*, col. 1:33-40. One of ordinary skill in the art would understand that the diffusion region 18 is conductive because the diffusion region 18 has been implanted with dopants, and the dopants have been activated to obtain the desirable electrical properties.

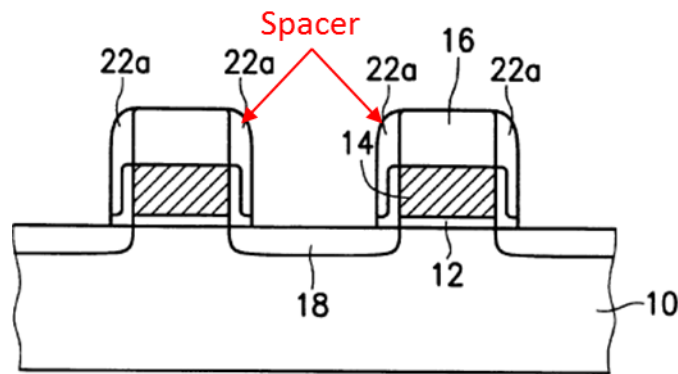


Fig. 1C (Prior Art)

17. Following the spacer formation, a second layer of silicon nitride layer 24 is formed, followed by the formation of an inter-layer dielectric (ILD) insulating layer 26. *Id.*, col. 1:41-50. Referring to the annotated Fig. 1E below, a contact hole 29 is lithographically defined, and the insulating layer 26 is etched. *Id.*, col. 1:51-67. The second layer of silicon nitride layer 24 acts as an etch stop for the self-aligned contact hole. The second layer of silicon nitride layer 24 is

then etched away, exposing the previously formed spacer 22a and the contact area (i.e., diffusion region 18) for contact plug formation. *Id.* Note that the arrangement of the spacer defines the boundary of the contact area of the self-aligned contact hole, i.e., how much of the diffusion region is exposed.

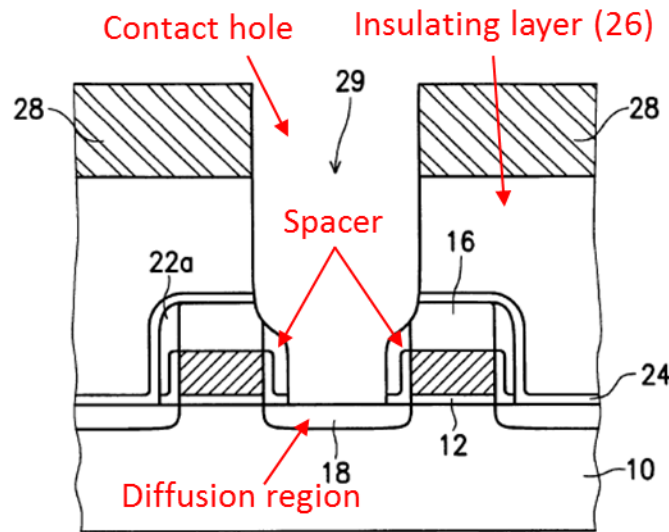
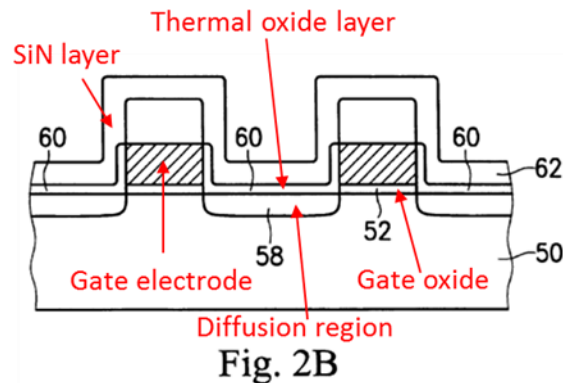


Fig. 1E (Prior Art)

18. The purported novelty of the '997 patent is to combine the spacer formation step and the contact hole exposure step into a single processing step to reduce the number of process steps. *Id.*, col. 1:65-67; col. 2:5-14; col. 3:40-47. The reduction of processing steps may reduce manufacturing costs and increase throughput. *Id.*

19. Referring to the annotated Fig. 2B of the '997 patent below, after gate electrodes 54, diffusion regions 58, a thermal oxide layer 60, and gate oxides 52 have been formed on a substrate 50, a conformal layer of silicon nitride 62 is

deposited over the substrate surface. *Id.*, col. 2:48-67. The '997 patent describes that the thermal oxide layer 60 is formed by rapid thermal oxidation. The '997 patent does not describe the purpose for forming the thermal oxide layer 60. There are a number of well-known reasons that one of ordinary skill in the art may wish to form a thermal oxide layer 60 after forming the gate electrodes 54. For example, the dry etch process used to form the gate electrodes 64 may create defects in the gate oxide that would affect the yield of the devices. The rapid thermal oxidation would reduce the defect density in the gate oxide, and improves the yield of the devices. Ex. 1009, p. 3.



20. Referring to the annotated Fig. 2C of the '997 patent below, a planarized ILD insulating layer 64 is formed over the conformal layer of silicon nitride 62, and a photoresist layer 66 is formed and patterned to expose the contact hole. *Id.*, col. 3:1-24. First, a high selectivity etch is used to etch away the insulating layer 64 while minimally etching the silicon nitride layer 62, which performs as an etch stop in this step. *Id.* I have annotated Fig. 2C to show the

region of the insulating layer that would be etched away by the first etch. The etch stops at the silicon nitride layer 62 because the etch is highly selective to silicon nitride.

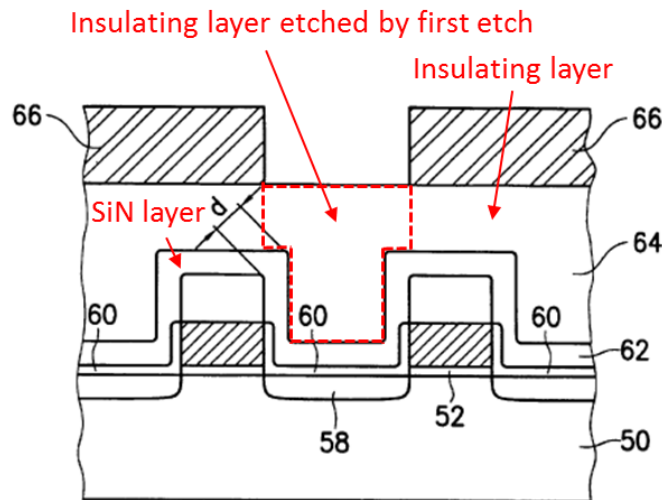


Fig. 2C

21. Referring to the annotated Fig. 2D of the '997 patent below, following the first selective etch of the insulating layer 64, the silicon nitride layer 62 is anisotropically etched to expose the diffusion region 58. *Id.* Due to the directionality of the anisotropic etch, a spacer 62a is formed on the sidewall of the electrode 54 during the same silicon nitride etch that exposes the diffusion region 58 to complete the contact hole 67. *Id.* The contact hole 67 is formed in a self-aligned and borderless manner because the portion of the diffusion region 58 exposed by the second silicon nitride etch is determined by the dimensions of the spacer 62a, and not by the dimension of the lithography mask. After the contact hole 67 is filled with conductive material to form a conductive plug, the spacer 62a

can be used to prevent shorting between the gate electrode 54 and the conductive plug. *Id.* col. 3:33-39.

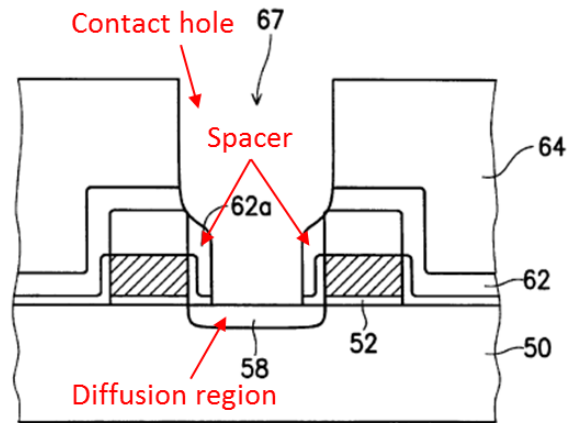


Fig. 2D

## II. Terminology

22. I have been informed that claim terminology must be given the broadest reasonable interpretation during an IPR proceeding. I have been informed that this means the claims should be interpreted as broadly as their terms reasonably allow, but that such interpretation should not be inconsistent with the patent's specification and with usage of the terms by one of ordinary skill in the art. Counsel has also informed me that this may yield interpretations that are broader than the interpretation applied during a District Court proceeding, such as the pending *Home Semiconductor Corporation v. Samsung Electronics Co. Ltd. et al.* litigation.

23. I have been informed that it would be useful to provide some guidance in this proceeding with respect to certain terms, and have been asked to consider

the terms below and corresponding constructions. As part of that, for each term addressed below, I considered each term's context within the claim, each term's use within the specification, and my understanding of how one of ordinary skill in the art would understand the term around the time of the purported invention.

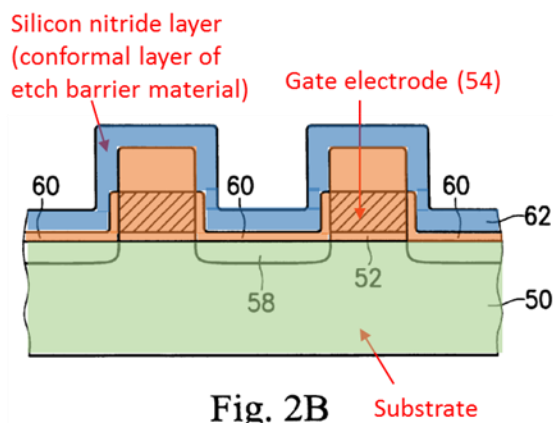
24. I have considered whether a broadest reasonable interpretation of “forming a conformal layer of [etch barrier material/silicon nitride] overlying the substrate surface” would be broad enough to cover “forming a layer of [etch barrier material/silicon nitride] supported by the substrate surface, the layer of [material] having a contour that conforms to a contour of one or more structures already formed on the substrate surface.” I believe that it would, because such an interpretation is not inconsistent with the '997 patent's specification and the understanding one of ordinary skill in the art would ascribe to this term when looking for the broadest reasonable construction.

25. Merriam Webster's Dictionary defines the word “conformal” as “conserving the size of all angles and therefore the shape of every elementary triangle.” Ex. 1007, p. 3. Merriam Webster's Dictionary defines the word “conform” as “to have the same shape, outline, or contour.” *Id.*

26. Fig. 2B of the '997 patent shows that “a conformal layer of silicon nitride 62 is deposited over the substrate surface using low pressure chemical vapor deposition (LPCVD).” Ex. 1001, col. 2:60-62. Prior to the deposition of the

silicon nitride layer 62, at least the oxide layer 60, the gate oxide layer 52, and the gate electrodes 54 have been formed on the substrate 50. *Id.*, col. 2:48-59. As shown in the following annotated version of Fig. 2B of the '997 patent, the silicon nitride layer 62 thus is not in direct contact with the substrate 50. Rather, the silicon nitride layer, as highlighted in blue, is supported by the substrate 50, as highlighted in green, where at least the oxide layer 60, the gate oxide layer 52, and the gate electrodes 54, as highlighted in orange, are between the silicon nitride layer 62 and the surface of the substrate 50. Moreover, the contour of the silicon nitride layer 62 appears to conform to the contour of the oxide layer 60, the gate oxide layer 52, and the gate electrodes 54 that have already been formed on the surface of the substrate 50. Consistent with the dictionary definitions, the contour of the silicon nitride layer 62 appears to conform to the contour of the oxide layer 60, the gate oxide layer 52, and the gate electrodes 54 that have already been formed on the surface of the substrate 50. Based on the consistent usage between the dictionary meaning and the disclosure of the '997 patent, I conclude that a broadest reasonable interpretation of "forming a conformal layer of [etch barrier material/silicon nitride] overlying the substrate surface" would be broad enough to cover "forming a layer of [etch barrier material/silicon nitride] supported by the substrate surface, the layer of [material] having a contour that conforms to a contour of one or more structures already formed on the substrate surface."

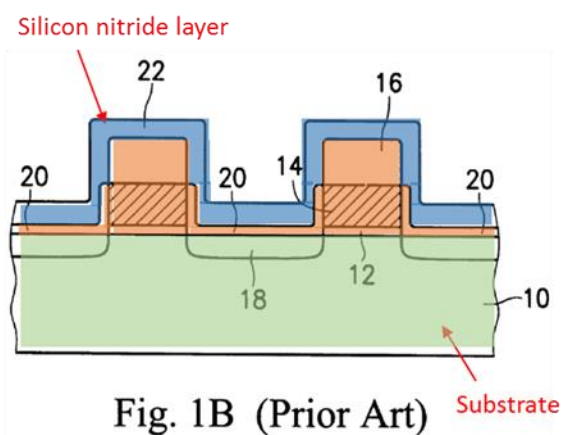




27. I have considered whether a broadest reasonable interpretation of “forming an oxide layer over the diffusion region” would be broad enough to cover “forming an oxide layer above the diffusion region.” I believe that it would, because such an interpretation is not inconsistent with the ’997 patent’s specification and the understanding one of ordinary skill in the art would ascribe to this term when looking for the broadest reasonable construction.

28. Within the specification of the ‘997 patent, the term “over” is applied consistent with the Merriam Webster’s Dictionary definition to reference items that are above each other, even when separated by an intermediary item. Specifically, referring to Fig. 1B, the ’997 patent discloses a “layer of silicon nitride 22 having a thickness of about 100 to 600 Å is deposited *over* the substrate surface using low pressure chemical vapor deposition (LPCVD)”. Ex. 1001, col. 32-35. As shown in the annotated Fig. 1B below, prior to the deposition of the silicon nitride layer 22, at least the oxide layer 20, the gate oxide layer 12, and the gate electrodes 14 have

been formed on the substrate 10. *Id.*, col. 1:24-31. The silicon nitride layer 22, as highlighted in blue, is above the substrate 10, as highlighted in green, where at least the oxide layer 20, the gate oxide layer 12, and the gate electrodes 14, as highlighted in orange, are between the silicon nitride layer 22 and the surface of the substrate 10. Based on the descriptions of the '997 patent, the '997 patent appears to use the term “over” as broadly as to encompass “above,” which is consistent with the Merriam Webster’s Dictionary definition. I further note that the term “over” is being used in the '997 patent in a manner that is consistent with how one in the ordinary skill in the art in this technical field would have used it. Therefore, I conclude that a broadest reasonable interpretation of “forming an oxide layer over the diffusion region” would be broad enough to cover “forming an oxide layer above the diffusion region.”



29. I have considered whether a broadest reasonable interpretation of “spacer” would be broad enough to cover “a structure that spaces between two conductive structures.” I believe that it would, because such an interpretation is

not inconsistent with the '997 patent's specification and the understanding one of ordinary skill in the art would ascribe to this term when looking for the broadest reasonable construction.

30. Merriam Webster's Dictionary defines the word "spacer" as "one that spaces." Ex. 1007, p. 6.

31. The '997 patent does not expressly define the term "spacer." According to the '997 patent, a spacer is a structure that is formed before or during formation of the contact hole. *See* Ex. 1001, col. 1:24-67, Ex. 1001, col. 2:24-28, col. 3:17-21, and col. 3:33-39. Functionally, the '997 patent discloses that a spacer is a structure that can "prevent shorting between the gate electrode and the conductive plug." Ex. 1001, col. 3:36-39. Based on the consistent usage between the dictionary meaning and the disclosure of the '997 patent, I conclude that a broadest reasonable interpretation of "spacer" would be broad enough to cover "a structure that spaces between two conductive structures."

32. I have considered whether a broadest reasonable interpretation of "etching an opening through the insulating layer self-aligned and borderless to the diffusion region" would be broad enough to cover "etching an opening to the diffusion region using a single mask through multiple layers including the insulating layer, where the mask contact window is oversized relative to the diffusion region." I believe that it would, because such an interpretation is not

inconsistent with the '997 patent's specification and the understanding one of ordinary skill in the art would ascribe to this term when looking for the broadest reasonable construction.

33. In particular, the '997 patent discloses that “[s]elf-alignment is a technique in which multiple levels of regions on the wafer are formed using a single mask, thereby eliminating the alignment tolerance required by additional masks. This powerful approach is being used more often as circuit sizes decrease. Self-aligned contacts are often used in memory cells where contacts are limited only by the spacers and field oxide bird's beak or a contact window landing pad. Therefore, *the mask contact window can be oversized relative to the contact area underneath, and no contact borders are needed*, resulting in significant space saving.” Ex. 1001, col. 1:11-20 (emphasis added).

34. One of ordinary skill in the art would understand that in a self-aligned process, the mask contact window would be oversized relative to a target area, such as the contact area, which allows an increase in lithography tolerance. Based on the consistent usage between the '997 patent's specification and the understanding one of ordinary skill in the art, I conclude that a broadest reasonable interpretation of “etching an opening through the insulating layer self-aligned and borderless to the diffusion region” would be broad enough to cover “etching an opening to the diffusion region using a single mask through multiple layers

including the insulating layer, where the mask contact window is oversized relative to the diffusion region.”

### **III. Legal Standards for Prior Art**

35. I understand that a patent or other publication must first qualify as prior art before it can be used to invalidate a patent claim.

36. I understand that a U.S. or foreign patent qualifies as prior art to an asserted patent if the date of issuance of the patent is prior to the invention of the asserted patent. I further understand that a printed publication, such as an article published in a magazine or trade publication, qualifies as prior art to an asserted patent if the date of publication is prior to the invention of the asserted patent.

37. I understand that a U.S. or foreign patent also qualifies as prior art to an asserted patent if the date of issuance of the patent is more than one year before the filing date of the asserted patent. I further understand that a printed publication, such as an article published in a magazine or trade publication, constitutes prior art to an asserted patent if the publication occurs more than one year before the filing date of the asserted patent.

38. I understand that a U.S. patent qualifies as prior art to the asserted patent if the application for that patent was filed in the United States before the invention of the asserted patent.

#### **A. Legal Standards for Anticipation**

39. I understand that documents and materials that qualify as prior art can be used to invalidate a patent claim as anticipated or as obvious.

40. I understand that, once the claims of a patent have been properly construed, the second step in determining anticipation of a patent claim requires a comparison of the properly construed claim language to the prior art on a limitation-by-limitation basis.

41. I understand that a prior art reference “anticipates” an asserted claim, and thus renders the claim invalid, if all elements of the claim are disclosed in that prior art reference, either explicitly or inherently (i.e., necessarily present).

42. I understand that anticipation in an *inter partes* review must be shown by a preponderance of the evidence.

#### **B. Legal Standards for Obviousness**

43. I understand that even if a patent is not anticipated, it is still invalid if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person of ordinary skill in the pertinent art.

44. I understand that a person of ordinary skill in the art provides a reference point from which the prior art and claimed invention should be viewed. This reference point prevents one from using his or her own insight or hindsight in deciding whether a claim is obvious.

45. I also understand that an obviousness determination includes the consideration of various factors such as (1) the scope and content of the prior art, (2) the differences between the prior art and the asserted claims, (3) the level of ordinary skill in the pertinent art, and (4) the existence of secondary considerations such as commercial success, long-felt but unresolved needs, failure of others, etc.

46. I understand that an obviousness evaluation can be based on a combination of multiple prior art references. I understand that the prior art references themselves may provide a suggestion, motivation, or reason to combine, but other times the nexus linking two or more prior art references is simple common sense. I further understand that obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references may be supplied by the direction of the marketplace.

47. I understand that if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

48. I also understand that practical and common sense considerations should guide a proper obviousness analysis, because familiar items may have obvious uses beyond their primary purposes. I further understand that a person of

ordinary skill in the art looking to overcome a problem will often be able to fit together the teachings of multiple publications. I understand that obviousness analysis therefore takes into account the inferences and creative steps that a person of ordinary skill in the art would employ under the circumstances.

49. I understand that a particular combination may be proven obvious merely by showing that it was obvious to try the combination. For example, when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp because the result is likely the product not of innovation but of ordinary skill and common sense.

50. The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, the patent claim is likely obvious.

51. It is further my understanding that a proper obviousness analysis focuses on what was known or obvious to a person of ordinary skill in the art, not just the patentee. Accordingly, I understand that any need or problem known in



the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.

52. I understand that a claim can be obvious in light of a single reference, without the need to combine references, if the elements of the claim that are not found explicitly or inherently in the reference can be supplied by the common sense of one of skill in the art.

53. I understand that secondary indicia of non-obviousness may include (1) a long felt but unmet need in the prior art that was satisfied by the invention of the patent; (2) commercial success of processes covered by the patent; (3) unexpected results achieved by the invention; (4) praise of the invention by others skilled in the art; (5) taking of licenses under the patent by others; (6) deliberate copying of the invention; (7) failure of others to find a solution to the long felt need; and (8) skepticism by experts. I understand that evidence of secondary indicia of non-obviousness, if available, should be considered as part of the obviousness analysis.

54. I also understand that there must be a relationship between any such secondary considerations and the invention. I further understand that contemporaneous and independent invention by others is a secondary consideration supporting an obviousness determination.

55. In sum, my understanding is that prior art teachings are properly combined where a person of ordinary skill in the art having the understanding and knowledge reflected in the prior art and motivated by the general problem facing the inventor, would have been led to make the combination of elements recited in the claims. Under this analysis, the prior art references themselves, or any need or problem known in the field of endeavor at the time of the invention, can provide a reason for combining the elements of multiple prior art references in the claimed manner.

56. I understand that obviousness in an *inter partes* review must be shown by a preponderance of the evidence.

#### **IV. Doshi**

A-1. Doshi teaches a method of fabricating an integrated circuit, including a method of fabricating contact openings. *See* Ex. 1005, Abstract. Doshi describes that “[e]tching of contact openings through the combination of the doped oxide layer and the silicon nitride layer may be accomplished by way of a two-step process.” Ex. 1005, col. 4:10-18. Consistent with the teaching of the ’997 patent, etching contact openings through the combination of the doped oxide layer and the silicon nitride layer by way of a two-step process as described in Doshi is a method for forming a self-aligned contact hole. Ex. 1001, col. 1:11-14.

A-2. Referring to the annotated Fig. 3a of Doshi below, Doshi shows a gate electrode 10 formed on a p-type silicon substrate 2. A p-type substrate is a semiconductor substrate. The gate structures 10 are formed “as layered structures, including polysilicon layer 22 in contact with gate oxide 8, tungsten silicide layer 24 overlying polysilicon layer 22, and silicon nitride layer 26 overlying tungsten silicide layer 24.” Ex. 1005, col. 7:40-43. One of ordinary skill in the art would understand that gate structures 10 are gate electrodes. One of ordinary skill in the art would also understand that the silicon nitride layer 26 is an insulating capping layer of the gate electrode, where the silicon nitride layer 26 provides insulation and protection from dopant diffusion and anisotropic etching.

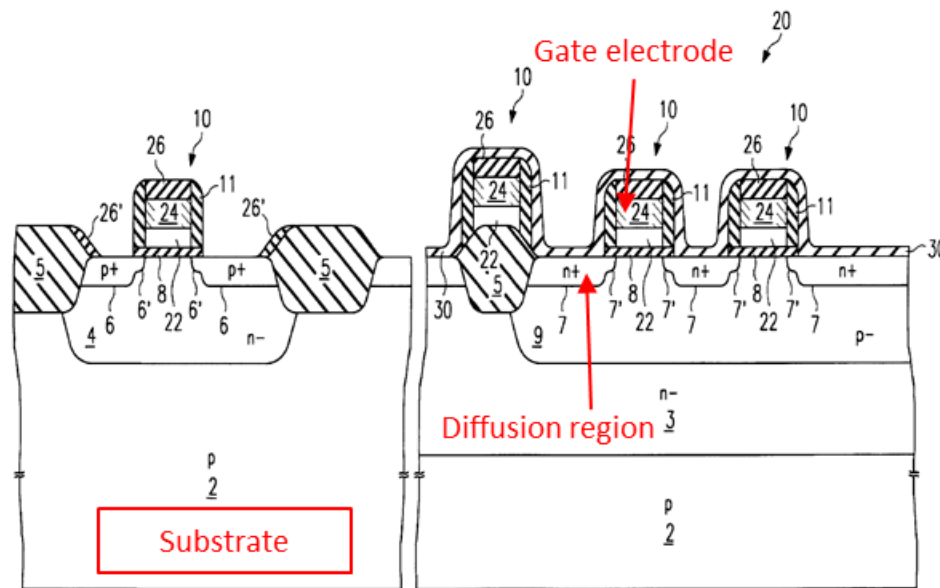


FIG. 3a

A-3. Doshi also teaches a formation of sidewall filaments 11. I note that his description shows that the purpose of the sidewall filaments 11 is to engineer

the doping profiles (concentration vs. position) of the source and drain with respect to their proximity to the gate electrodes. Specifically, Doshi describes the formation of lightly doped source/drain extensions 6' and 7' prior to the formation of the sidewall filaments 11, so that heavier doped source/drain regions can be spaced further from the gate electrode edge. "Following definition of gate structures 10, light "reach-through" implants are performed in a self-aligned manner relative to gate structures 10 to define source/drain extensions 6' (for p-channel devices), 7' (for n-channel devices)." Ex. 1005, col. 7:52-55. Doshi further discloses that heavily-doped p+ and n+ source and drain regions are formed on the semiconductor substrate. "Following formation of sidewall filaments 11, source/drain implant and anneal is performed to form source/drain regions 6 (p+ type), 7 (n+ type). Source/drain regions 6, 7 are formed in a self-aligned manner relative to gate structures 10, in the conventional manner." *Id.* col. 7:66 – 8:3. One of ordinary skill in the art would understand that source/drain regions 6, 7 and source/drain extensions 6' and 7' are diffusion regions formed by ion implantations on the silicon substrate 2.

A-4. Referring to the annotated Fig. 3b below, Doshi discloses that a conformal layer 30 of silicon nitride is formed overlying the surface of substrate 2 including the source/drain diffusion regions and the upper surface and the sidewalls of the gate electrode. "According to the preferred embodiment of the

invention, *silicon nitride layer 30 is now formed overall*, preferably by way of low-pressure chemical vapor deposition (LPCVD), resulting in the structure illustrated in FIG. 3b.” Ex. 1005, col. 8:8-11. Doshi further discloses that the silicon nitride layer 30 acts as an etch barrier, and therefore silicon nitride is an etch barrier material. “Contact openings (PC, BLC, CT) are etched through the BPSG layer (14) and the silicon nitride layer (30) using a two-step etch process. The first etch selectively etches silicon dioxide relative to silicon nitride, and thus stops on silicon nitride layer (30); besides *serving as an etch stop*, silicon nitride layer (30) protects underlying active regions (6, 7) from damage that may be caused by ionized oxygen released during oxide etch.” *Id.*, Abstract (emphasis added). Doshi therefore discloses that the silicon nitride layer 30 is deposited as an etch stop layer, or an etch barrier layer.

A-5. Doshi further teaches that “the thickness of nitride layer 30 may range from 65Å to 250 Å.” Ex. 1005, col. 8:19-20. I note that the silicon nitride thickness range of 65Å to 250 Å as disclosed in Doshi overlaps with the range of about 100 Å to 500 Å as recited in claims 5 and 11 of the ’997 patent. I further note that the ’997 patent does not describe any reasons for picking the thickness range of 100 Å to 500 Å, other than simply stating that “[t]he conformal layer 62 preferably has a thickness of about 100 to 500 Å, and more preferably has a thickness of about 200 to 350 Å.” Ex. 1001, col. 2:65-67.

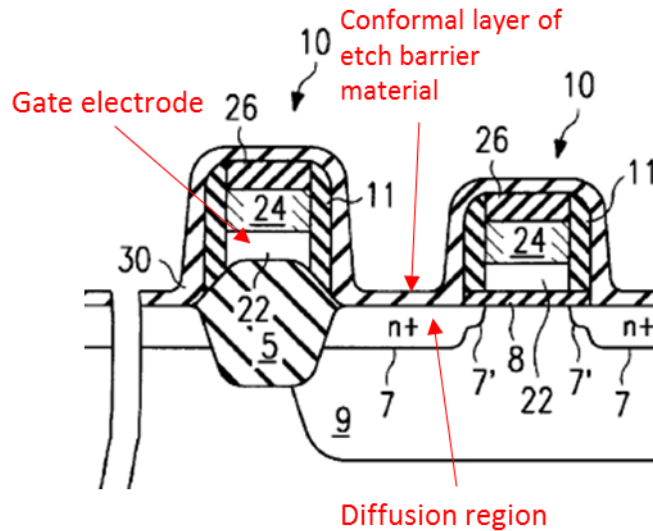


Fig. 3b, Doshi

A-6. Note that prior to depositing the silicon nitride layer 30, Doshi discloses the formation of sidewall filaments 11, which are formed on the sidewalls of polysilicon layer 22 of the gate electrode by thermal oxidation. *Id.* “According to the preferred embodiment of the invention, sidewall ***filaments 11 are formed by first oxidizing the sides of polysilicon layer 22.***” Ex. 1005, col. 7:57-59 (emphasis added). Referring to the annotated Fig. 3b below, the barrier layer (i.e., the silicon nitride layer 30) is formed after the formation of the filaments 11, and therefore Doshi discloses forming an oxide layer on the sidewalls of the gate electrode by thermal oxidation prior to forming the barrier layer.

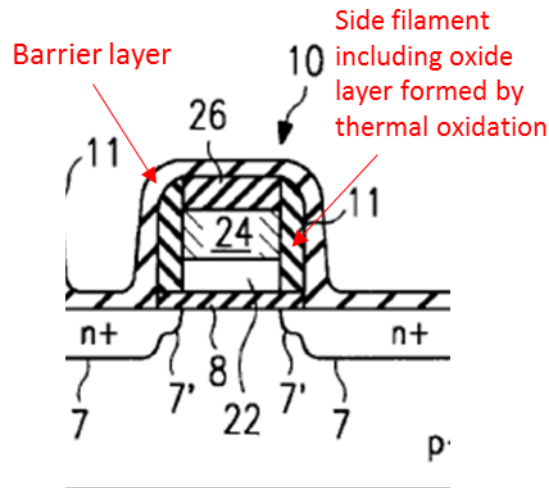
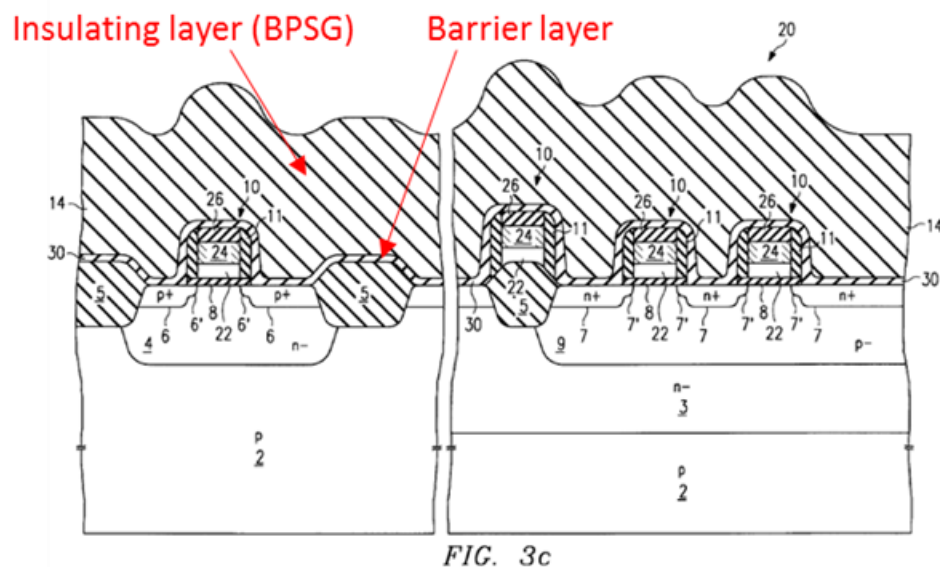


Fig. 3b, Doshi

A-7. Doshi further discloses forming an oxide layer over the diffusion region in at least two manners. First, referring to the annotated Fig. 3b above, the side filament 11 is formed above the source/drain region 7', and illustrates that the oxide layer is formed over the diffusion region, specifically the lightly doped source/drain 7'. Second, as Doshi discloses, the oxidation of the sidewall filaments 11 is performed right after the implantation of the source/drain extensions 6' and 7'. "Following definition of gate structures 10, light "reach-through" implants are performed in a self-aligned manner relative to gate structures 10 to define source/drain extensions 6' (for p-channel devices), 7' (for n-channel devices), prior to the formation of sidewall filaments 11 along the sides of gate structures 10. According to the preferred embodiment of the invention, sidewall filaments 11 are formed by first oxidizing the sides of polysilicon layer 22." Ex. 1005, col. 7:52-59. Although not expressly disclosed in Doshi, during the thermal oxidation of the

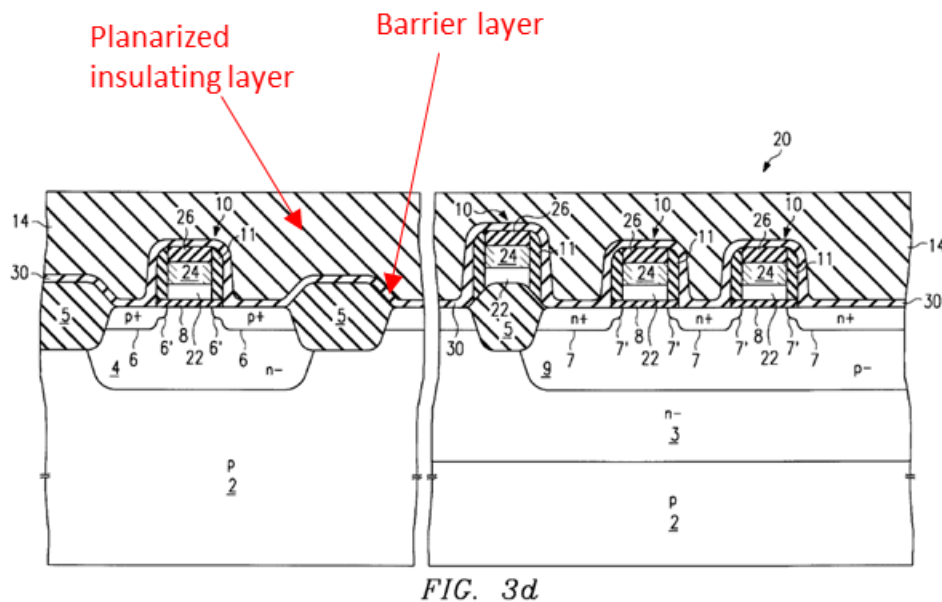
sides of polysilicon layer 22, thermal oxide is also formed over the source/drain regions because the source/drain regions are uncovered doped silicon, which is susceptible to thermal oxidation. Even if the source/drain regions were covered by a thin layer of gate oxide during the implantation step, one of ordinary skill in the art would recognize that the gate oxide covering the source/drain regions will grow thicker during the thermal oxidation of the gate structures 10.

A-8. Referring to the annotated Fig. 3c below, Doshi discloses a deposition of a doped BPSG silicon dioxide layer 14 as an insulating layer overlying the silicon nitride barrier layer 30. BPSG is an acronym for borophosphosilicate glass. “Referring now to FIG. 3c, integrated circuit 20 is illustrated after the deposition of doped BPSG silicon dioxide layer 14. BPSG layer 14 is preferably deposited in the conventional manner, for example by way of LPCVD, doped with both boron and phosphorous.” Ex. 1005, col. 8:23-27.



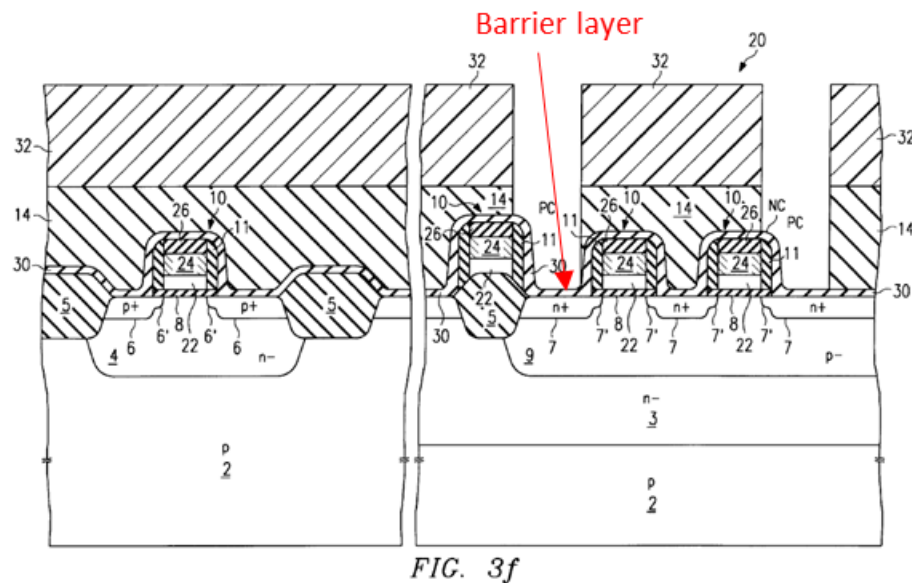


A-9. Fig. 3c shows that the BPSG insulating layer 14 is deposited overlying the silicon nitride barrier layer 30. Moreover, Doshi discloses that “[f]ollowing deposition and anneal [of the BPSG layer 14], a planarization etchback of BPSG layer 14 is performed according to this preferred embodiment of the invention. This etchback is performed without patterning, and is preferably a timed etch selected so that BPSG layer 14 remains over the top of all underlying structures.” Ex. 1005, col. 8:66 – 9:4. As shown in the annotated Fig. 3d of Doshi below, the planarization etchback of BPSG layer 14 planarizes the BPSG layer 14.



A-10. Referring to the annotated Fig. 3f below, Doshi discloses etching an opening through the BPSG layer 14 to the diffusion region 7 by using the silicon nitride layer 30 as an etch stop. “According to this preferred embodiment of the present invention, etching of contact openings through BPSG layer 14 and nitride

layer 30 is performed by way of a two-step etch. *The first step is a “dry” etch of BPSG layer 14*, carried out in a plasma etch reactor as known in the art, a preferred example of which is the TEL DRM reactor. [. . .] Under these conditions, etching of BPSG layer 14 is relatively highly selective relative to etching of nitride layer 30, and as *such the etch will tend to stop on nitride layer 30.*” Ex. 1005, col. 9:34-50 (emphasis added).



A-11. Doshi discloses etching an opening through the BPSG layer 14 to the diffusion region as a self-aligned and borderless process. The '997 patent describes that “[s]elf-alignment is a technique in which multiple levels of regions on the wafer are formed using a single mask, thereby eliminating the alignment tolerance required by additional masks.” Ex. 1001, col. 11-14. Doshi discloses that “[c]ontact opening locations are defined by way of conventional photolithography. FIG. 3e illustrates patterned photoresist layer 32, after exposure and development

to define plug contact openings PC, at those locations where photoresist has been removed after development. *The remaining portions of photoresist layer 32 serve, of course, as a mask for etch of the contact openings through BPSG layer 14 and nitride layer 30.*” Ex. 1005, col. 9:26-33 (emphasis added). One of ordinary skill in the art would understand that the two step etch described in Doshi is a self-aligned and borderless process.

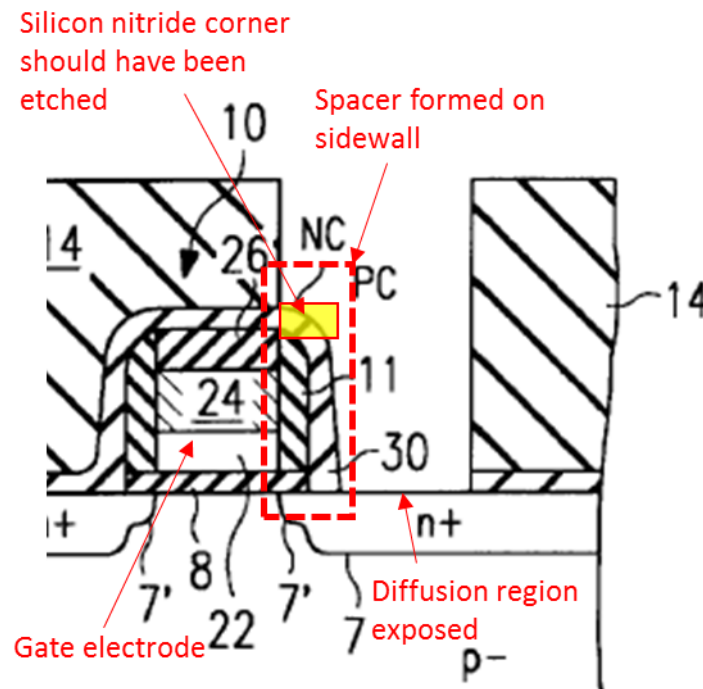
A-12. Doshi describes the second etching step, which is the anisotropically etching of the barrier layer underneath the opening. “Contact openings (PC, BLC, CT) are etched through the BPSG layer (14) and the silicon nitride layer (30) using a two-step etch process. The first etch selectively etches silicon dioxide relative to silicon nitride, and thus stops on silicon nitride layer (30); besides serving as an etch stop, silicon nitride layer (30) protects underlying active regions (6, 7) from damage that may be caused by ionized oxygen released during oxide etch. *A brief nitride etch is then used to clear silicon nitride layer (30)*, without damaging corner locations (NC) of the sidewall structures (11).” Ex. 1005, Abstract (emphasis added). “[T]he brief nitride etch used to clear nitride layer 30 from within plug contact locations PC has been observed to be *highly anisotropic*.” *Id.*, col. 10:11-13 (emphasis added).

A-13. Referring to the annotated Fig. 3g of Doshi below, Doshi further discloses that the anisotropic etch of the barrier layer exposes the diffusion region

and simultaneously forms a spacer of the etch barrier material on the sidewall of the gate electrode. “FIG. 3g illustrates the construction of integrated circuit 20 after the completion of both etch steps, and the stripping of photoresist layer 32.” Ex. 1005, col. 9:65-67. Fig. 3g of Doshi illustrates that the diffusion region 7 has been exposed after the second etch. Moreover, after the second etch, the silicon nitride layer 30 remained on the sidewall of the gate electrode 10 acts as a spacer, which provides a space as well as electrical insulation between the gate electrode 10 and the contact plug to be filled in the contact hole. Analogous to what is disclosed in the '997 patent, the second anisotropic etch of the silicon nitride layer exposes the diffusion region and simultaneously forms a spacer of the etch barrier material on the sidewall of the gate electrode.

A-14. I noticed that the corner of the silicon nitride layer 30, which is exposed to the silicon nitride dry etch, is not shown as etched in Fig. 3g. I believe this is a mistake in Fig. 3g, as an anisotropic etch of silicon nitride would have removed the same thickness of the silicon nitride covering the diffusion region and the silicon nitride at the corner. In fact, Doshi discloses that “the brief nitride etch used to clear nitride layer 30 from within plug contact locations PC has been observed to be highly anisotropic, and because of this anisotropy in combination with its brevity, minimizes damage at the sidewall [corner] locations NC of gate structures 10 in integrated circuit 20.” Ex. 1005, col. 10:11-16. By stating that the

damage at the corner locations NC of the gate structures 10 is minimized, Doshi acknowledges that the silicon nitride corner on the gate structures would have been etched by the dry etch process, as one of ordinary skill in the art would understand how the process would have worked.



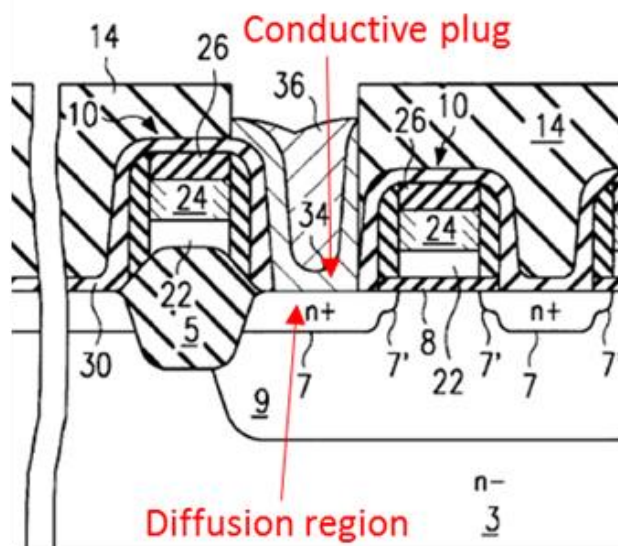
**Fig. 3g, Doshi**

A-15. Referring to the annotated Fig. 3h of Doshi below, after the contact opening is formed, a polysilicon plug is formed in the contact opening. “Following definition of plug contact openings PC, *polysilicon plugs are formed* therewithin, *in contact with source/drain regions 7.*” Ex. 1005, col. 10:17-19. One of ordinary skill in the art would recognize that polysilicon is conductive, and therefore a polysilicon plug is a conductive plug that electrically connects to the source/drain regions, which are diffusion regions. I note that a dictionary meaning for the word

“plug” is “a piece of wood, metal, or other material used or serving to fill a hole.”

Ex. 1007, p. 7. I am not aware of any special meaning for the term “conductive plug.” I believe the term “conductive plug” would be broad enough to cover “one or more conductive materials used to at least partially fill a hole,” as illustrated by the polysilicon plug in Fig. 3h of Doshi.

Fig. 3h, Doshi



## V. Becker and Combinations Based on Becker

### A. Becker

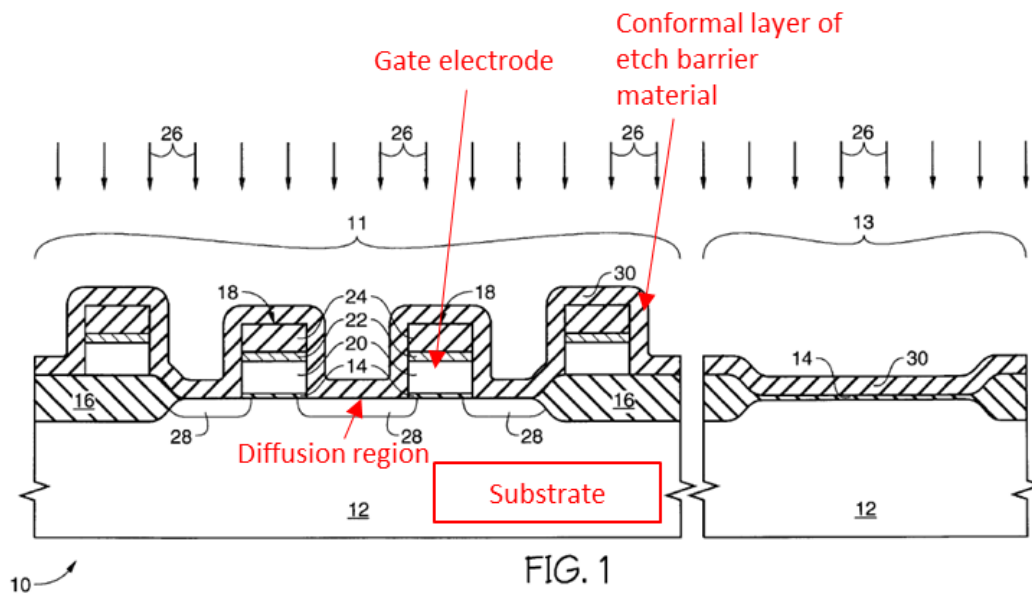
B-1. Becker discloses “[a]n etch process that uses a single partially etched spacer insulating layer to form both sidewall spacers and a diffusion barrier that protect areas of the substrate during subsequent processing steps in the formation of semiconductor devices”. Ex. 1006, Abstract. Becker discloses a two-step etch using a single mask. “Another aspect of the invention provides a process for making a dynamic random access memory cell. This DRAM fabrication process

includes the steps of: [. . .] e. *etching the lower [BPSG] insulating layer* to form a capacitor container over the first source/drain region and to expose the [silicon nitride] spacer insulating layer over the first source/drain region; f. *etching the exposed portion of the [silicon nitride] spacer insulating layer* to expose the first source/drain region.” Ex. 1006, col. 2:30-51 (emphasis added). As disclosed in the ’997 patent, “[s]elf-alignment is a technique in which multiple levels of regions on the wafer are formed using a single mask, thereby eliminating the alignment tolerance required by additional masks.” Ex. 1001, col. 11-14. Since Becker discloses etching contact openings through the combination of the BPSG insulating layer and the silicon nitride layer by way of a two-step process, Becker discloses a method for forming a self-aligned contact hole.

B-2. Referring to the annotated Fig. 1 of Becker below, Becker discloses a lightly doped p-type silicon substrate 12, which is a semiconductor substrate. Becker further discloses a gate electrode 18 formed on a semiconductor substrate. *“Transistor gate electrode 18 is formed* by successively depositing or "stacking" layers of polysilicon 20, tungsten silicide 22 and silicon nitride 24 over thin gate insulating layer 14, and then patterning and etching those layers to expose substrate 12 at the desired locations of the source and drain for the access transistors.” Ex. 1006, col. 4:22-27 (emphasis added). One of ordinary skill in the art would understand that the silicon nitride layer 24 is an insulating capping layer of the gate

electrode 18, where the silicon nitride layer 24 provides insulation and protection from dopant diffusion and anisotropic etching.

B-3. Becker further discloses that doped p-type regions 28, which are diffusion regions, are formed on the semiconductor substrate 12. “P-type impurities, typically boron atoms, are then implanted into the exposed portions of substrate 12, as shown symbolically by arrows 26. Boron ions are implanted at an energy level of approximately of 25-50 KeV, to a depth of approximately 1000 angstroms. The resulting doped p-regions 28 extend into the channel area between the subsequently formed source and drain for each access transistor.” Ex. 1006, col. 4:36-42. The doped p-region 28 is a diffusion region.



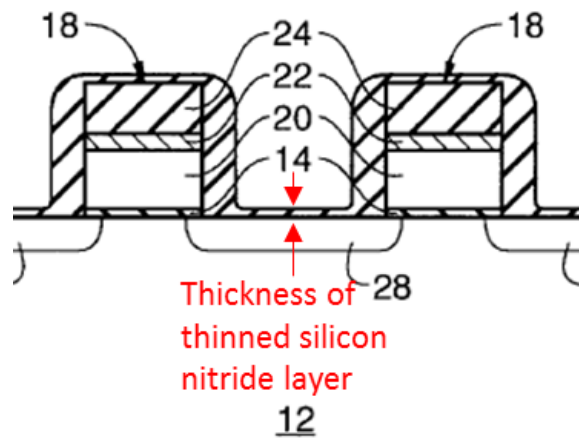
B-4. Referring to the annotated Fig. 1 above, Becker discloses that a conformal layer 30 of silicon nitride is formed overlying the surface of substrate 12



including the p-doped diffusion regions 28 and the upper surface and the sidewalls of the gate electrode 18. “A *spacer insulating layer 30 is then deposited* over the in process structure to a thickness typically in the range of 600 angstroms to 2,000 angstroms.” Ex. 1006, col. 4:46-48. Becker further discloses that the silicon nitride layer 30 acts as an etch barrier for an oxide etch, and therefore silicon nitride is an etch barrier material. “Spacer insulating layer 30 is preferably made of silicon nitride or other suitable insulating material that is *selectively etchable with respect to oxide materials.*” *Id.*, col. 4:51-54.

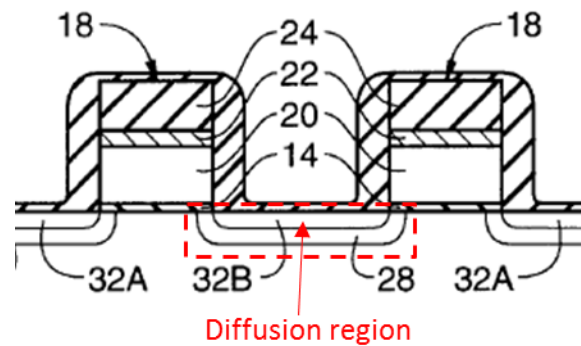
B-5. Referring to the annotated Fig. 2 below, Becker discloses that the silicon nitride spacer insulating layer 30 is thinned down to a thickness range of 50 angstroms to 400 angstroms, preferably about 100 angstroms, by a timed anisotropic etch to form an implant barrier layer. Ex. 1006, col. 4:58-66. I note that after thinning, the silicon nitride thickness range of 50 to 400 angstroms as disclosed in Becker overlaps with the range of about 100 Å to 500 Å as recited in claims 5 and 11 of the '997 patent. I also note that after thinning, the preferred thickness of 100 angstroms as disclosed in Becker falls within the range of about 100 Å to 500 Å as recited in claims 5 and 11 of the '997 patent. I further note that the '997 patent does not describe any reasons for picking the thickness range of 100 Å to 500 Å, other than simply stating that “[t]he conformal layer 62 preferably

has a thickness of about 100 to 500 Å, and more preferably has a thickness of about 200 to 350 Å.” Ex. 1001, col. 2:65-67.



**Fig. 2, Becker**

B-6. Referring to Fig. 3 below, Becker discloses forming lightly doped drain implants (LDDs) by implanting n-type impurities to create source/drain regions 32a and 32b. Ex. 1006, col. 5:6-18. One of ordinary skill in the art would understand that the source/drain regions 32a and 32b are diffusion regions. I note that the n-type diffusion regions 32a and 32b are formed in the p-type diffusion regions 28. However, one of ordinary skill in the art would understand that the concentration of the p-type dopant in the diffusion regions 32a and 32b would not have changed with the n-type doping. Thus, I believe that a diffusion region, namely the p-type doped region 28, is formed prior to the deposition of the silicon nitride film 30. This diffusion region is still a diffusion region after the n-type source/drain formation.



B-7. Referring to the annotated Fig. 4 below, Becker discloses a deposition of a BPSG silicon dioxide layer 36 as an insulating layer over the silicon nitride barrier layer 30. Becker further discloses planarizing the BPSG glass layer.

“Referring to FIG. 4, a thick lower insulating layer 36, preferably made of borophosphosilicate glass (BPSG), is deposited and, if necessary, planarized.” Ex. 1006, col. 5:19-21.

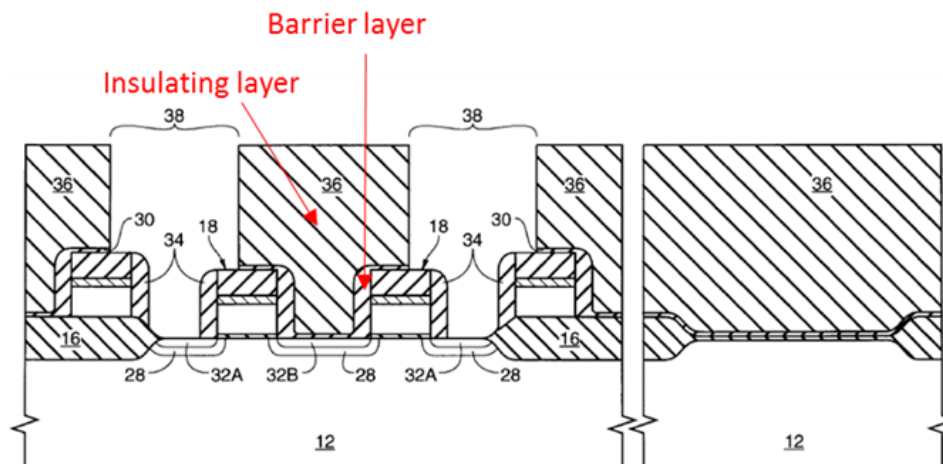


FIG. 4

B-8. Becker further discloses etching an opening through the BPSG insulating layer 36 to the diffusion region 28 by using the silicon nitride layer 30 as

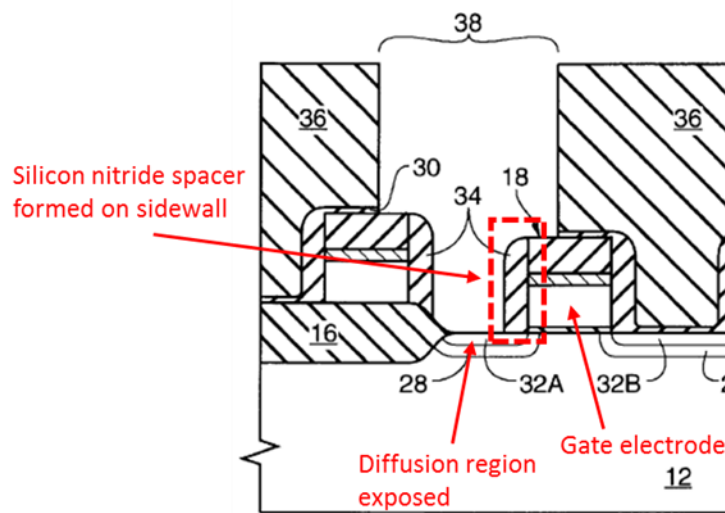
an etch stop. “***Lower insulating layer 36 is patterned and etched*** to define capacitor contact corridors 38 (also commonly referred to as the capacitor containers) in lower insulating layer 36. The etch of lower insulating layer 36 utilizes a oxide etch process that is ***selective to silicon nitride to protect spacer insulating layer 30*** during any over etch of lower insulating layer 36.” Ex. 1006, col. 5:21-27 (emphasis added).

B-9. Becker discloses the etching to the diffusion region as self-aligned and borderless. Specifically, Becker discloses “a process for making a dynamic random access memory cell. This DRAM fabrication process includes the steps of: [. . .] e. ***etching the lower [BPSG] insulating layer*** to form a capacitor container over the first source/drain region and to expose the [silicon nitride] spacer insulating layer over the first source/drain region; f. ***etching the exposed portion of the [silicon nitride] spacer insulating layer*** to expose the first source/drain region.” Ex. 1006, Abstract (emphasis added). Consistent with the definition of the self-alignment technique in the ’997 patent, Becker discloses two levels of regions formed using a single mask. Accordingly, Becker discloses etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop.

B-10. Referring to the annotated Fig. 4 of Becker below, Becker discloses that “[a]fter lower insulating layer 36 has been completely removed from

source/drain regions 32a, the *etch chemistry is changed to remove the remainder of spacer insulating layer 30 and thereby expose source/drain regions 32a*. This etch of the remainder of spacer insulating layer 30 *produces the same spacer 34 profile* as conventional processes.” Ex. 1006, col. 5:32-38 (emphasis added).

“[T]he spacer insulating layer is *anisotropically etched* to form substantially vertical spacers along sidewalls of the gate electrodes.” *Id.*, claim 11 (emphasis added). Analogous to what is disclosed in the '997 patent, the second anisotropic etch of the silicon nitride layer exposes the diffusion region and simultaneously forms a spacer of the etch barrier material on the sidewall of the gate electrode.



**Fig. 4, Becker**

B-11. Referring to the annotated Figs. 5 and 6 of Becker below, Becker discloses that “storage poly 42 is patterned and etched or subjected to a chemical mechanical polish (CMP) to *form capacitor first conductors 44*.” Ex. 1006, col. 5:45-48 (emphasis added). The capacitor first conductors 44 constitute a

conductive plug that electrically connects to the diffusion region. That is, the conductors 44 are conductive plugs in that they are conductive and plug the contact corridors 38 by virtue of covering the interface between the corridors 38 and the source/drain diffusion regions 32A, thereby providing electrical connectivity. I note that a dictionary meaning for the word “plug” is “a piece of wood, metal, or other material used or serving to fill a hole.” Ex. 1007, p. 7. I am not aware of any special meaning for the term “conductive plug.” I believe the term “conductive plug” would be broad enough to cover “one or more conductive materials used to at least partially fill a hole,” as illustrated by the conductor 44 in Fig. 6 of Becker.

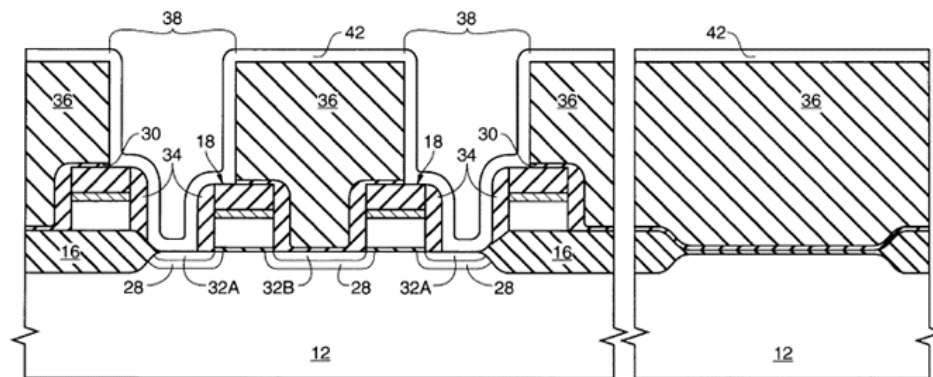


FIG. 5



B-13. Wong's paper investigates the integrity degradations of the thin gate oxide during post-oxidation processing. Ex. 1009, p. 3. According to Wong, the reactive ion etch (RIE) process used to define the polysilicon gate structure increases the defect density of the thin oxide, and decreases the yield of fabricated devices. *Id.*, pp. 3, 5, 6. As described by Wong, a reoxidation of polysilicon gate sidewall using thermal oxidation reduces the defect density in the thin oxide and therefore improves the yield of the fabricated devices. *Id.* Specifically, referring to

Table III of Wong below, with a gate oxide thickness of 12.5 nm, the yield of good capacitor after a polysilicon gate etch without reoxidation is 83%. By growing 104 nm of oxide on the polysilicon sidewall using thermal oxidation, the yield is improved to 95%. Similarly, with a gate oxide thickness of 22.5 nm, the yield of good capacitor after a polysilicon gate etch without reoxidation is 83%. By growing 52 nm of oxide on the polysilicon sidewall using thermal oxidation, the yield is improved to 98%. *Id.*

**TABLE III: PERCENT GOOD CAPACITOR<sup>1</sup> AFTER  
REOXIDATION OF POLYSILICON SIDEWALL USING RIE  
DEFINED GATE STRUCTURE<sup>2</sup>**

Gate Oxide (nm)	Polysilicon Oxide Sidewall (nm)		
	None	52	104
12.5	83%	90%	95%
22.5	83%	98%	-

B-14. Becker discloses forming a thin gate insulating layer 14 and then forming a stack of gate electrode layers on the gate insulating layer 14. Ex. 1006, col. 4:9-35. The stack of gate electrode layers includes a polysilicon layer 20. *Id.* Transistor gate electrode 18 is formed by patterning and etching the stack of gate electrode layers using “conventional methods well known in the art.” *Id.* Persons of skill would have readily recognized that a conventional method for etching the stack of gate electrode layers is RIE. Having read Wong, persons of skill would




therefore have recognized that after the RIE etch, defects may be created in the gate oxide that would decrease the device yield. Persons of skill also would have readily recognized the benefit of applying the reoxidation of polysilicon sidewalls of the gate as described in Wong to form an oxide layer on the polysilicon layer 20 in Becker by a thermal oxidation to help improve the device yield in Becker. *Id.* Therefore, it would have been obvious to a person of ordinary skill in the art to combine the teachings of Becker and Wong to form a layer of oxide film on the polysilicon layer 20 by thermal oxidation after the gate electrode 18 formation, but prior to deposition the silicon nitride etch barrier layer 30.

B-15. Moreover, a person of ordinary skill in the art would have readily recognized that the formation of an oxide layer on the polysilicon gate electrode layer 20 in Becker by a thermal oxidation would also form an oxide layer over the p-doped diffusion region 28. Specifically, if the gate oxide over the p-doped diffusion region 28 had been removed prior to the thermal oxidation, the p-doped diffusion region 28 is uncovered doped silicon, and is susceptible to thermal oxidation. If the gate oxide were still present prior to the thermal oxidation, the gate oxide would grow thicker during oxidation of the polysilicon gate sidewall, again forming thermal oxide over the p-doped diffusion region 28 during oxidation of the gate polysilicon sidewall.

## VI. Conclusion

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Signature:   
Gary W. Rubloff, PhD

Date: December 16, 2014