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PROCESS INDUCED DEGRADATION OF THIN OXIDES

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ABSTRACT

The purpose of this work is to investigate integrity degradations of thin oxides during post-oxidation processing. We found that channel ion implantation through thin oxide degrades the oxide and that ion implantation using low energy boron induces less oxide damage than BF₂ implant. RIE to define polysilicon gate structure degrades the quality of thin oxide; nevertheless these defects can be substantially reduced by subsequent sidewall oxidation of polysilicon. Polysilicon sidewall oxidation is also necessary to protect the thin oxide from degradation by source/drain ion implantation. Finally, during silicide formation on polysilicon, with the same titanium thickness, increasing polysilicon thickness reduces defects generated in the thin oxides by this processing step.

INTRODUCTION

Thin (10nm-20nm) thermal oxides are widely used in silicon integrated circuits as insulator for gate dielectric and storage capacitors. For the past 30 years, a great deal of efforts have been devoted to the growth of high quality SiO₂ films and the study of their properties. However, as we approach ultra large scale integration (ULSI), the need to understand the effects of post-oxidation processing on these thin thermal oxides becomes more apparent. For device applications, the quality of thin oxides must be maintained from growth through to the end of the fabrication sequence. Currently, information of this kind is still very limited in the literature. The purpose of this work is to investigate integrity degradations of thin oxides during post-oxidation processing. Particularly, we report the effects on the quality of 10nm oxide by channel ion implantation through oxides, surface cleaning of the oxide before polysilicon deposition, reactive ion etching to define polysilicon gate structure,

source/drain ion implantation, chemical etching of polysilicon oxide, and silicide formation on polysilicon.

EXPERIMENTAL

Figure 1 shows the processing steps being investigated for thin oxide degradation. To insure the uniformity of starting silicon surfaces, a sacrificial oxide was first grown on all wafers and then removed. Next, 12.5nm oxide was grown at either 800 or 900 °C (Fig. 1a), followed by channel ion implantation using either BF_2 or boron at $2 \times 10^{12} \text{ cm}^{-2}$. The implant energy for BF_2 was 36 keV and that for boron was either 15 keV or 36 keV, (Fig. 1b). Some of these implanted oxides were stripped and regrown at the same temperature as the previous oxidation. RCA clean without HF was used in some cases immediately before low pressure chemical vapor deposition (LPCVD) of undoped polysilicon (Fig. 1c). Doping of the polysilicon was accomplished by phosphorous ion implantation through a screen oxide at 50 keV and $8 \times 10^{15} \text{ cm}^{-2}$ and the gate electrode was defined by reactive ion etching using CCl_2F_2 . Source/Drain ion implantation with arsenic at 40 keV and $2 \times 10^{15} \text{ cm}^{-2}$ and phosphorous at 30 keV and $1 \times 10^{14} \text{ cm}^{-2}$ was carried out after polysilicon sidewall oxidation. Finally, the polysilicon screen oxide was removed with dilute hydrofluoric acid and titanium silicide contact was formed on polysilicon electrodes.

For the degradation studies of all processing steps other than titanium silicide formation on polysilicon, aluminum was evaporated on polysilicon and MOS capacitors were formed by dry etching the polysilicon layer using Al as a mask (Fig. 2). To minimize the effect of reactive ion etching on dielectric breakdown, polysilicon patterns were defined on the field oxide (Fig. 2a) for all our studies except those investigating RIE processes. For the effects of reactive ion etching on dielectric breakdown, structures where the polysilicon edge is on field oxide (Fig. 2a) and those with edge on gate oxide (Fig. 2b), as well as aluminum gated structures where the thin oxides are not exposed to any RIE processes (Fig. 2c) were investigated.

Except otherwise specified in the text, breakdown tests for the thin oxides were performed on either 1.8mm^2 or 0.26mm^2 capacitors using the current ramp technique¹. Briefly, the gate was biased negatively with respect to the p-type substrate to avoid surface depletion. The tests were carried out on 3-4 wafers with 84 capacitors from each wafer. The defect density D was calculated from $Y = \exp(-A \times D)$ where A is capacitor area and Y is the wafer yield, defined as the percentage of good capacitors that can withstand more than $1 \mu\text{A}$ current without breaking down.

RESULTS AND DISCUSSIONS

Our results indicate that channel ion implantation increases defect density and hence, degrades the yield of thin oxides grown at 900 and 800°C (Fig. 3a and 3b). As shown in Fig. 3a, implantation with BF_2 at 36 keV through oxides grown at 900°C produced very high defect density in the oxide (85 cm^{-2}). These defects can be significantly reduced by stripping and regrowing the gate oxide. Nevertheless some residual defects still remain in the regrown oxide, as evidenced by its higher defect density as compared to the control. Boron implant at 15 keV through 900°C oxides produced lower defect density than BF_2 implant at 36 keV, although the first condition yields a deeper boron profile in the silicon substrate.

Comparison between Fig. 3a and 3b shows that although oxide grown at 900°C intrinsically has less defects than that grown at 800°C, the oxide grown at 800°C is less susceptible to BF_2 implantation damage than that grown at 900°C. The defect density is decreased by a factor of four. Boron implant at 36 keV produced only slightly higher defect density than BF_2 implant at the same energy (equivalent boron implant energy at 8 keV). BF_2 implant and regrowth produced oxides with even better quality than that of the control without implant. The improvement of 800°C oxide over that of 900°C oxide is perhaps due to the slower oxidation at the lower temperature, leading to different interfacial and bulk structures at 800°C than at 900°C². Because of the possible different structures at different oxidation temperatures, the oxide grown at lower oxidation temperature could therefore be less susceptible to damage by ion implantation.

The cleaning of thin oxide surfaces using RCA procedure without HF does not appear to cause any degradation of the oxide integrity. Extensive results on the degradation of thin oxides by polysilicon doping/activation process were reported³. In our case, within our experimental conditions, the doping of polysilicon by phosphorous ion implantation appears to have no effects on the breakdown properties of thin oxides. This may be due to the fact that in our structure, the polysilicon layer may act as a defect absorbing barrier for the underlying oxide during ion implantation.

Reactive ion etching (RIE) with CCl_2F_2 to define polysilicon gate was studied using oxides grown at 800°C. This process was found to induce additional defects in the thin oxides. Comparison was made among three structures: Al gated capacitors with thin oxide unexposed to any RIE processing (Fig. 2c), polysilicon gated capacitors with the polysilicon edge defined on the field oxide using RIE (Fig. 2a), and devices with the gate edge defined on the gate oxide using RIE (Fig. 2b). Structure where polysilicon edge on the gate oxide is defined by plasma (Fig. 2b) is also investigated. Our results show that the Al gated structures always have lower defect density than all the polysilicon gated structures, regardless whether the gate

is defined on the field oxide or on the gate oxide and also regardless whether the polysilicon gate is defined by RIE or plasma etching (Table I). Furthermore, comparing defects generated by RIE in the field oxide and those in the thin oxide and also the defects generated by RIE and by plasma etching (Table I) show that the integrity of the thin oxide is very sensitive to the RIE process, i.e. RIE induces defects in the thin oxides. The charging of the thin oxide during RIE process or during abrupt equipment power on/off could be a source for these defects⁴. The degradation of thin oxide by RIE processing obviously is not well understood. Studies varying reactive gases and instrumental factors are currently under investigation.

The next two studies involve the impacts on the integrity of thin oxides by polysilicon sidewall oxidation and source/drain ion implantation. Since these edge effects are more pronounced in devices with a large perimeter/area ratio, special test sites were fabricated with the perimeter/area ratio as large as 1.3×10^4 (Table II). These test sites have polysilicon lines running alternately over field oxides and gate oxides. Capacitors with perimeter/area ratio as small as 3.8×10^{-3} were also fabricated. These particular test sites serve as oxide quality monitors in addition to the the Al gated monitors that we routinely use in our experiments. The gate insulator was evaluated by leakage current measurements at a fixed gate voltage. A good capacitor is one with leakage current less than 1 nA at -4 V on the gate.

Table III shows the effect of sidewall oxidation of polysilicon on the RIE induced oxide defects. The reoxidation of RIE defined polysilicon reduces the defect density in the thin oxide. This reduction is independent of the perimeter/area ratio and is enhanced with increasing reoxidation time. The improvement in oxide quality by sidewall oxidation of polysilicon could be due to the additional post-oxidation anneal in oxygen.

Table IV summarizes the effects of source/drain ion implantation on the integrity of the thin oxide. Our investigation indicates that within our implant conditions, sidewall oxidation is necessary in order to minimize yield loss, confirming results reported earlier by Osburn⁵. Increasing yield in the thin oxide is correlated with increasing polysilicon oxide sidewall thickness and decreasing perimeter length in the structure. It is interesting to note that source/drain ion implantation degrades the thin oxide even in the case where the polysilicon edge is defined on the field oxide (site F). Again charging in the oxide during ion implantation, even in the case of the field oxide, may be the cause for the yield loss.

Much controversies exist in literature on the effects of chemical etching of polysilicon oxide to the thin oxide integrity. It was thought that hydrofluoric acid, while etching polysilicon oxides, would at the same time penetrate through the grain boundaries of polysilicon and attack the thin oxides. However our data indicates that

no effect can be observed even with an overetch time of 100%. We can only speculate at this point that the different results may be due to different polysilicon grain size or different polysilicon deposition conditions employed in various studies.

Finally, during silicide formation on polysilicon, with the same titanium thickness, high defect density in the oxide is observed for decreasing polysilicon thickness (Table V). We have shown before⁶ that during final silicide anneals, titanium silicide can be seen diffusing through polysilicon. Thinner polysilicon films require less time for the metal silicide to penetrate and interact with the thin oxide underneath. The fact that some interaction(s) exists at the thin oxide can be demonstrated by the one order of magnitude increase in interface trap densities between the silicided and non-silicided devices and these interface traps generated by silicidation cannot be removed even by extensive forming gas anneal. Silicide annealing temperature also seems to play a role in the oxide breakdown where higher final annealing temperature reduces defect density in the oxide (Table V). Our data thus suggests that as we scale down polysilicon thickness for ULSI applications, simultaneously we should also scale down Ti thickness in order to minimize process degradation to thin oxides.

SUMMARY

Our studies indicate that for channel ion implantation, thin oxide grown at 800°C is less susceptible to BF_2 implant than oxide grown at 900°C. Low energy boron implant induces less oxide damage than BF_2 implant and therefore is more preferable. Stripping and regrowing thin oxides after ion implantation reduce defect density, however this process changes the dopant profile in the silicon substrate. Reactive ion etching of polysilicon degrades the thin oxide, nevertheless the defects thus generated can be reduced by the subsequent sidewall oxidation of polysilicon. Sidewall oxidation is also necessary to protect the thin oxide from degradation by source/drain ion implantation. Finally, during silicide formation on polysilicon, with the same titanium thickness, high defect density in the oxide is observed for decreasing polysilicon thickness. Thus when we reduce polysilicon thickness, we should also scale down Ti thickness in order to maintain oxide integrity.

It is evident that as we scale down the device dimensions and the corresponding oxide thickness, in addition to the growth of high quality thin oxides, understanding and characterization of the defects generated by post-oxidation processing is also essential in order to minimize device degradation and maximize circuit yield.

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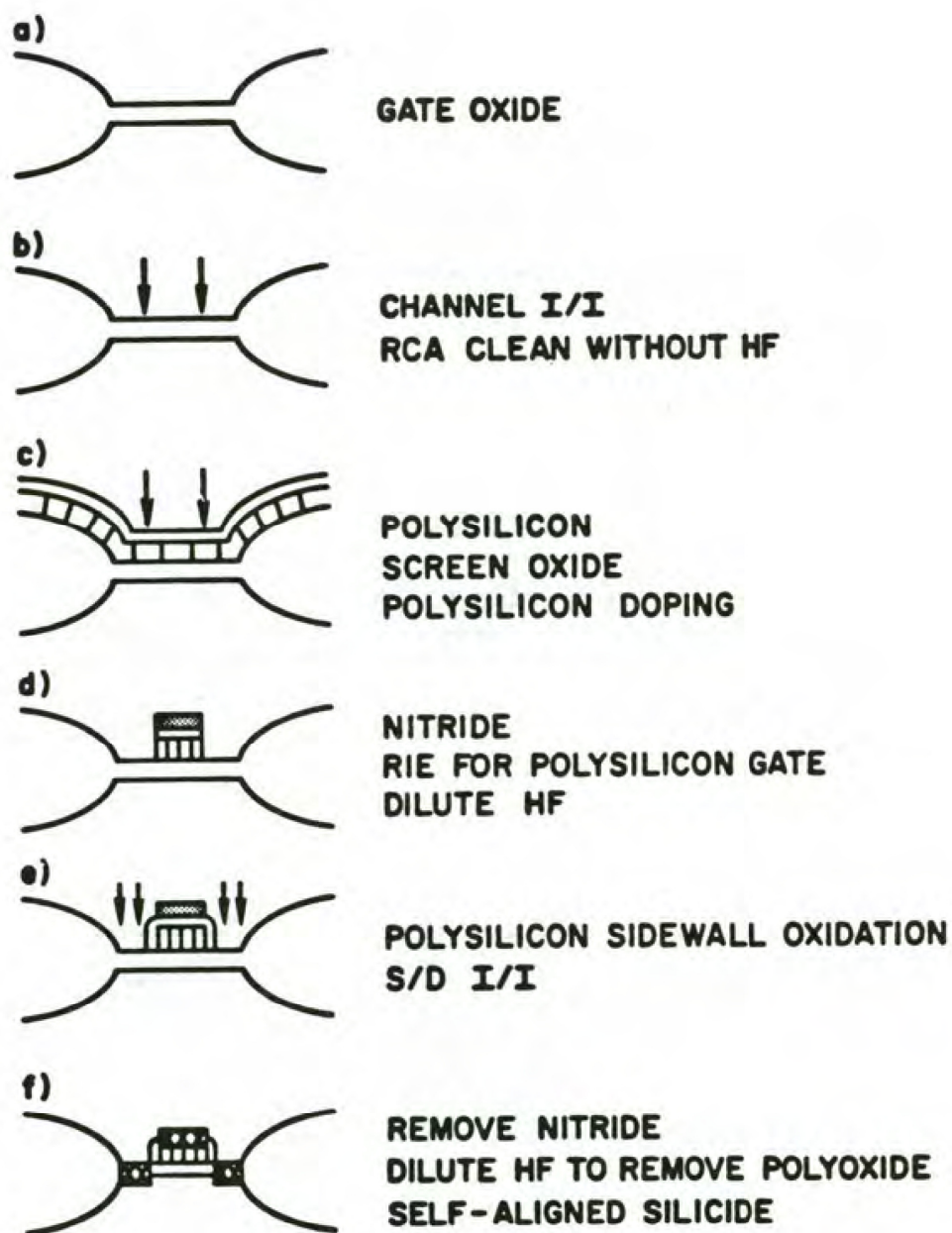


Fig.1 Processing steps investigated in the thin oxide degradation studies.

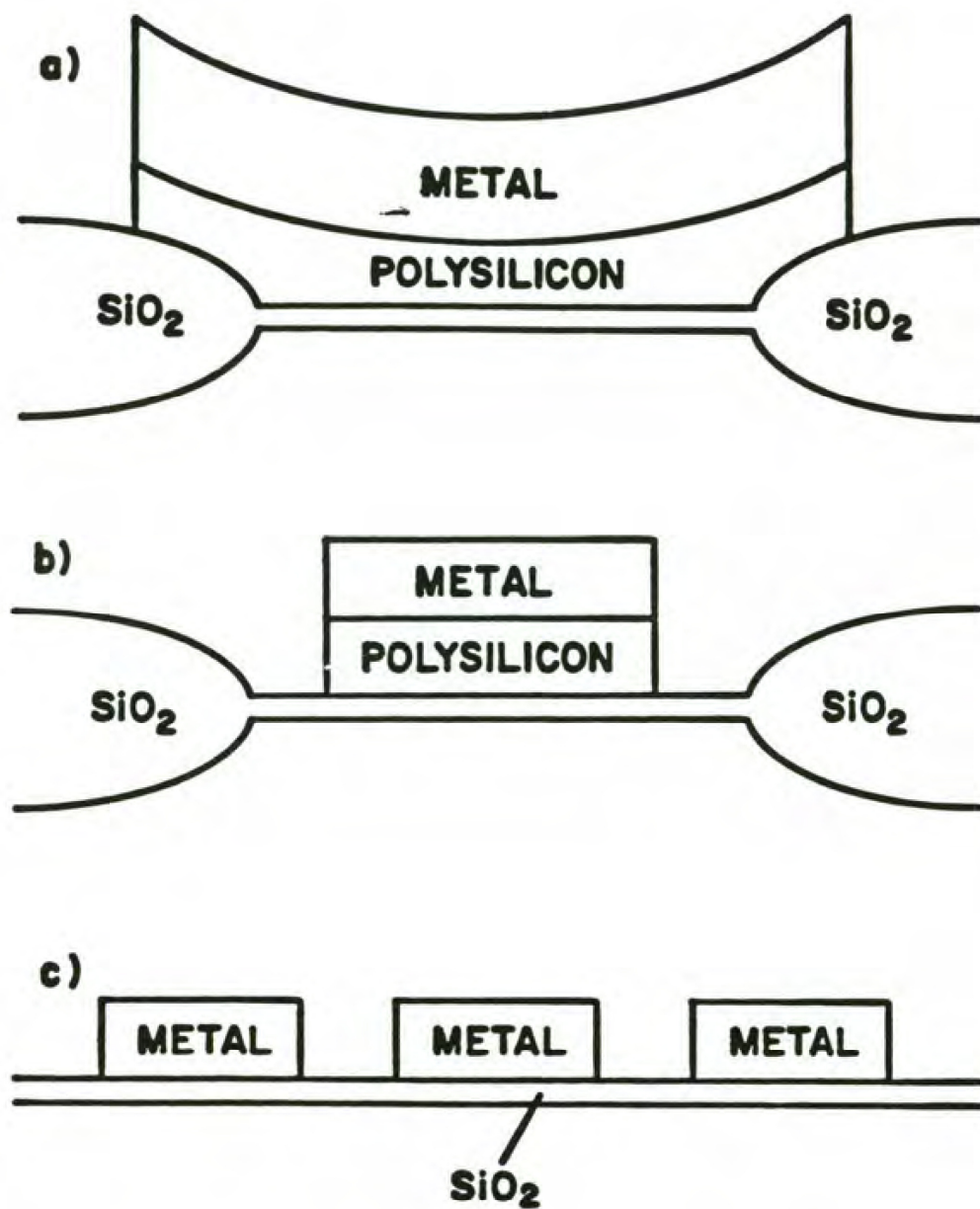


Fig.2 Test structures used in the thin oxide degradation studies.

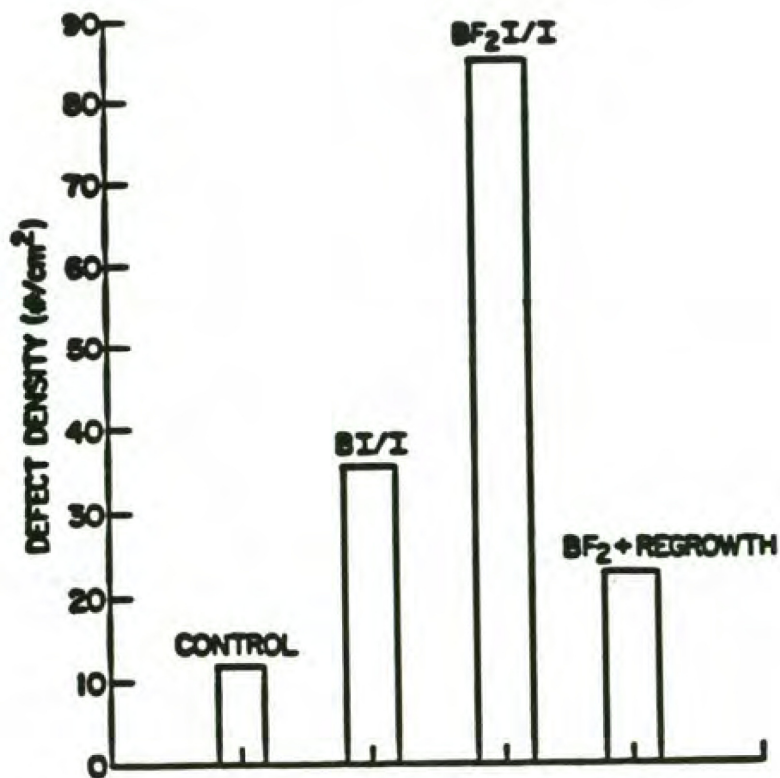


Fig.3(a) Effect of channel ion implantation on defect density of 12.5nm gate oxides grown at 900°C.

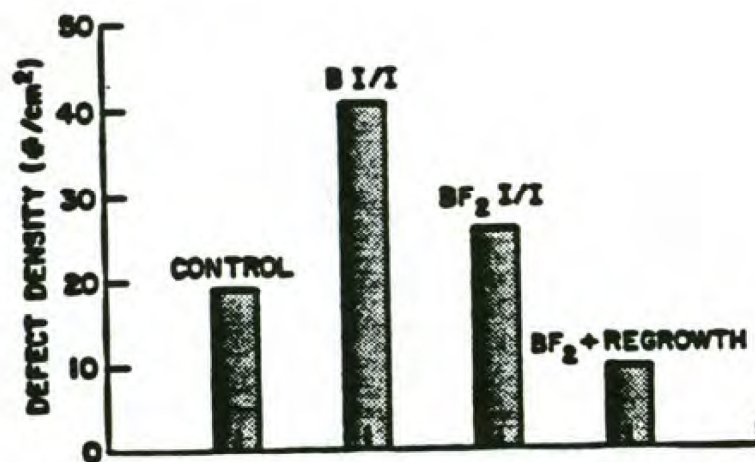


Fig.3(b) Effect of channel ion implantation on defect density of 12.5nm gate oxides grown at 800°C.

TABLE I: DEFECT DENSITIES IN THIN OXIDES AFTER RIE DEFINITION OF POLYSILICON GATES

Structure	Defect Density (#/cm ²)	
	800°C Oxide ¹	900°C Oxide ¹
Al Gate (60 mil dot, Fig 2c)	1.6	2.0
PolySi Gate (60 mil dot, plasma etched, Fig. 2b)	26	22
PolySi Gate (edge on field oxide, RIE, Fig. 2a)	19	-
PolySi Gate (edge on gate oxide, RIE, Fig. 2b)	88	-

1. 12.5 nm

TABLE II: TEST SITES FOR THIN OXIDE DEGRADATION

Site	Perimeter (cm)	Area x 10 ⁴ (cm ²)	Ratio ($\frac{P}{A} \times 10^{-4}$)
A	9.6	7.2	1.3
B	38.4	29	1.3
C	154	115	1.3
D	614	460	1.3
E ¹	1.32	346	0.0038
F ²	1.32	346	0.0038

1. Polysilicon gate edge defined on field oxide
2. Polysilicon gate edge defined on gate oxide

**TABLE III: PERCENT GOOD CAPACITOR¹ AFTER
REOXIDATION OF POLYSILICON SIDEWALL USING RIE
DEFINED GATE STRUCTURE²**

Gate (nm)	Polysilicon Oxide Sidewall (nm)		
	None	52	104
Oxide			
12.5	83%	90%	95%
22.5	83%	98%	-

1. Good capacitor is defined as those with leakage current less than 1 nA at an applied voltage of -4V on the gate. 40 capacitors tested per case. Oxide thickness is 12.5 nm.
2. Site E from Table II.

**TABLE IV: PERCENT GOOD CAPACITOR¹ AFTER SOURCE/DRAIN ION
IMPLANTATION²**

Site ³	Polysilicon Oxide Sidewall (nm)		
	None	52	104
A	45	93	88
B	28	93	90
C	18	63	80
D	0	52	65
E	55	83	88
F	65	90	93

1. Good capacitor is defined as those with leakage current less than 1 nA at an applied voltage of -4V on the gate. Forty capacitors total tested per case. Oxide thickness is 12.5 nm.
2. Arsenic at 40 keV, 2×10^{15} ions/cm² and phosphorous at 30 keV, 1×10^{14} ions/cm²
3. See Table II.

TABLE V: DEGRADATION OF THIN OXIDE DURING TITANIUM SILICIDE FORMATION¹ ON POLYSILICON

Silicide Annealing Temp. (°C)	Defect Density (#/cm ²)	
	300 nm Poly Si	150 nm Poly Si
No Silicide	19	19
2nd Silicide Anneal at 700°C	40	43
2nd Silicide Anneal at 750°C	32	43
2nd Silicide Anneal at 800°C	10	215

1. Evaporated Ti at 35 nm, followed by 1st silicide anneal at 600°C - 700°C, selective etch of Ti, then the second silicide anneal at temperatures as shown.