

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of:	Liu <i>et al.</i>	
U.S. Patent No.:	6,146,997	IPR Control No.: IPR2015-00460
Issue Date:	Nov. 14, 2000	
Appl. Serial No.:	09/407,268	
Filing Date:	Sep. 29, 1999	
Title:	METHOD FOR FORMING SELF-ALIGNED CONTACT HOLE	

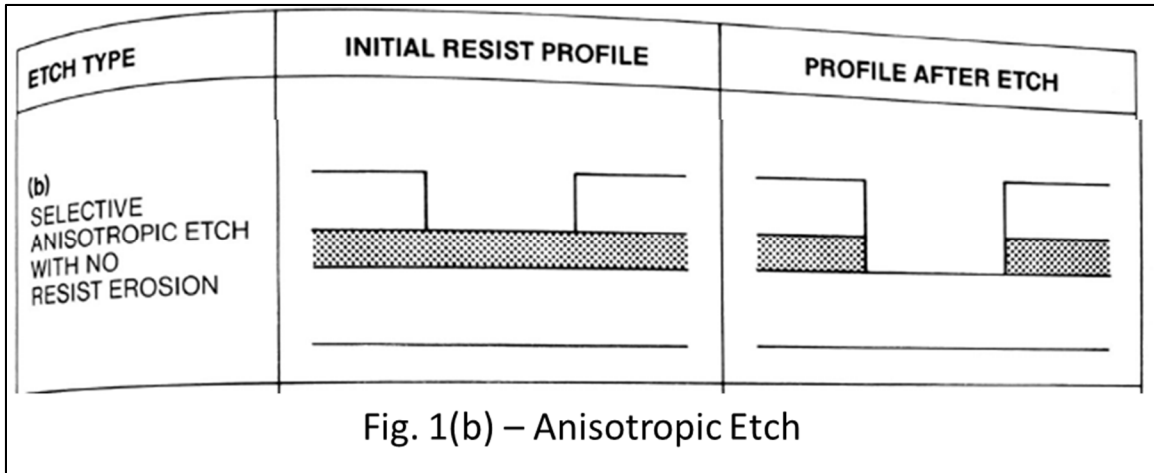
DECLARATION OF DR. GARY W. RUBLOFF

1. I have reviewed the “Patent Owner Response” and “Declaration of Ron Maltiel” filed on August 31, 2015 in connection with IPR2015-00460. I have also reviewed the transcript of Mr. Maltiel’s deposition on November 9, 2015 in connection with this IPR. Applying the standards and legal principles that I applied when drafting the declaration entitled “Declaration of Dr. Gary W. Rubloff” dated December 16, 2014, I found various inaccurate and/or misleading statements in both the Patent Owner’s Response (“Response”) and Mr. Maltiel declaration. Below, I address some of these statements.

2A. HSC states that “[t]he nitride etch process designed to clear the nitride layer 30 would etch every part of layer 30 exposed under the contact opening.” Paper 18, p. 19. HSC cites to Doshi’s disclosure that the brief and anisotropic nitride etch “clear[s] nitride layer 30 from within plug contact locations PC” and “remove[s] nitride layer 30 from bit line contact location BLC” as support for its contention that no portion of nitride layer 30 remains following the etch process.

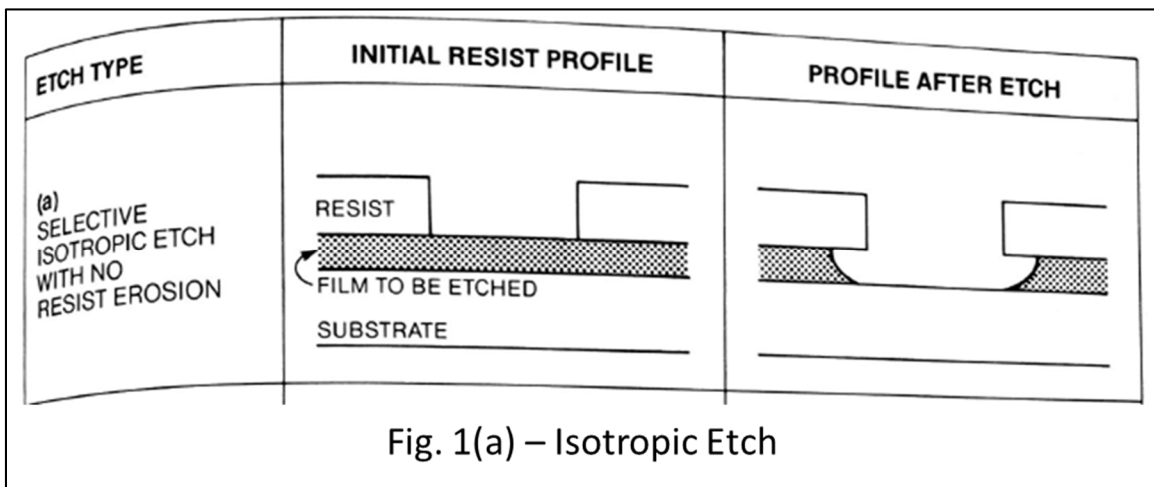
Id., p. 17. I disagree, as a person of ordinary skill in the art (“POSITA”) reviewing Doshi would have found it evident that the silicon nitride layer 30 would remain on sidewalls to form a spacer after Doshi’s “highly anisotropic” etch in view of both the anisotropy of the etch and the expressly stated goal of Doshi to minimize damage to gate structures 10 and sidewall filaments 11. Ex. 1005, col. 10:4-17. A complete removal of the silicon nitride layer 30 from the sidewalls of Doshi’s contact holes using a highly anisotropic etch is inconsistent with Doshi’s disclosure. Specifically, a complete removal would expose the sidewall filaments 11 and expose gate structures 10 to potential damage, in direct contravention to Doshi’s explicitly stated goal of minimizing damage to these structures.

2B. Exhibit 1014 is a textbook titled “VLSI Handbook,” authored by Dr. Norman Einspruch, which is a well-known textbook in the area of semiconductor processing prior to the filing date of the ’997 patent. Referring to Einspruch as an example, a POSITA would have understood that a highly anisotropic etch generally indicates that the etch rate in a perpendicular/vertical direction (i.e., etching from top to bottom) is much greater than the etch rate in a lateral/horizontal direction (i.e., etching from the side). Ex. 1014, p. 3. For example, Fig. 1(b) of Einspruch shows a typical etch profile from an anisotropic etch:



Id., p. 4.

2C. By contrast, Fig. 1(a) of Einspruch shows a typical etch profile from an isotropic etch, where etch rates are equal in both directions:



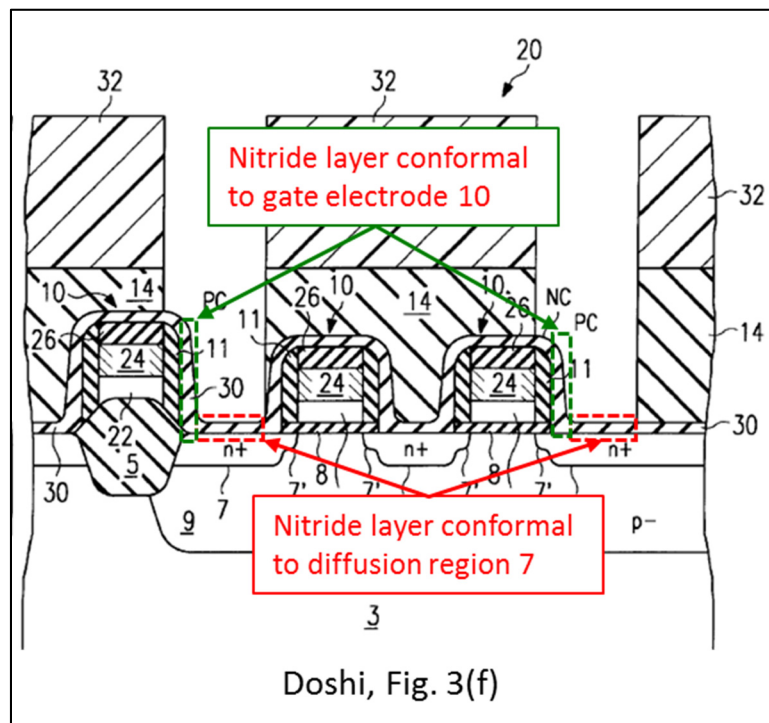
Id.

2D. Therefore, a POSITA would have understood that an aggressive over-etch, which is an etch that takes much longer than the time required to clear the surface covering the diffusion region, would be required to completely remove the nitride layer 30 from the sidewalls when using a highly anisotropic etch. In

addition, a POSITA also would have readily recognized that such an aggressive over-etch would damage sidewall filaments 11 and also would likely damage the gate structures 10.

2E. In particular, referring to FIG. 3g of Doshi, after the nitride film 30 covering the NC of filaments 11 and gate structures 10 is etched through via the faster vertical etching of the highly anisotropic nitride etch, the subsequent additional etching time used to remove the remaining sidewall portions of film 30 would result in etch of the NC portion of the filaments 11 and the gate structures 10. During this additional time, given that filaments 11 are partially formed of silicon nitride, the highly anisotropic silicon nitride etch would readily etch into the portions of the filaments 11 formed of nitride and, because of the physicality of highly anisotropic etches, would also etch into the portions of the filaments 11 formed of oxide, albeit likely to a lesser degree. Ex. 1005, col. 7:52-65. Moreover, the silicon nitride layer 26 of the gate structures 10 also may be etched as the NC portion of gate structures 10 progressively become exposed during the over-etching needed to completely remove the film 30. A POSITA would have recognized that the damage caused by this over-etch is inconsistent with Doshi's disclosure that its etch "substantially minimize[s]" damage "to the corners of gate structures 10 and sidewall filaments 11." Ex. 1005, col. 10:4-16. A POSITA would have understood that such damage to the structures 10 and sidewall

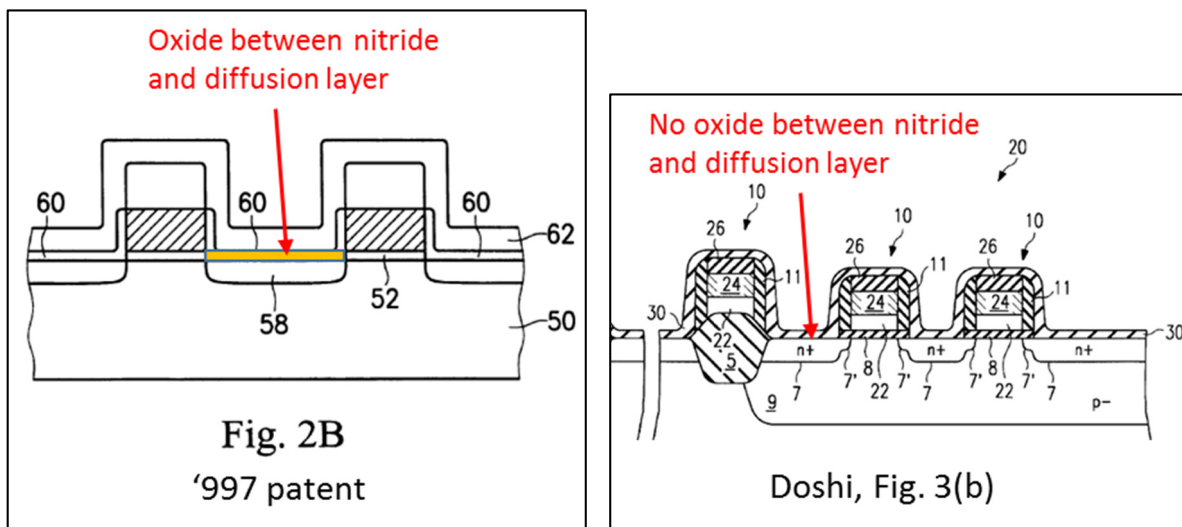
filaments 11 undesirably increases the likelihood of shorts occurring between a contact plug and the gate electrode. Thus, a POSITA would not have been led by Fig. or otherwise to believe that Doshi's highly anisotropic nitride etch completely removes the film 30 from Doshi's contact holes. A POSITA would have understood Doshi's description of brief nitride etching to clear nitride layer 30 from within PC or BLC region to mean that the brief and highly anisotropic nitride etch is used to clear the nitride layer 30 that is conformal to the diffusion region 7, without suggesting that such a brief and anisotropic etch would clear the nitride layer 30 that is conformal to the sidewall of the gate electrode 10.



2F. A POSITA would have understood that, if the goal of an etch is to remove the entire nitride layer regardless of direction, an isotropic etch would be

preferred over an anisotropic etch. Since Doshi expressly discloses that a highly anisotropic nitride etch is used to expose the diffusion region, a POSITA would have understood that Doshi does not teach removal of the nitride layer 30 on the sidewall. A POSITA would have understood that there is a good reason for using a highly anisotropic etch, as a highly anisotropic etch maintains the dimension of the contact hole, which is critical for preventing electrical shorting between the contacts and the gate electrodes.

2G. As illustrated in the annotated Fig. 2B of the '997 patent and the annotated Fig. 3(b) of Doshi below, in Doshi, there is no gate oxide between the silicon diffusion layer and the silicon nitride layer 30. Ex. 1001, Fig. 2B; Ex. 1005, Fig. 3b, col. 8:3-22.



2H. In Doshi, after the diffusion region 7 is exposed by the silicon nitride etch, therefore, a POSITA would have understood that the diffusion region 7, like

the filaments 11 and gate electrode structures 10, are also vulnerable to etch damage from the over-etch required to completely remove the layer 30. Doshi teaches the importance of tightly controlling the dimensions of the diffusion region 7, including the junction depth of the diffusion region 7, due to the heightened sensitivity of these dimensions to process variations. A POSITA would have understood that since the devices are highly sensitive, damage to this area would be undesirable:

“[t]hese extremely small critical dimensions not only result in high density and high performance integrated circuit operation, but also involve significant sensitivity to process variations and parameters.” Ex. 1005, col. 6:61-64.

2I. A POSITA would have readily recognized that exposing the diffusion region 7 to an aggressive over-etch would compromise the tight control of the dimensions of the diffusion region 7 by introducing variable damage and, in doing so, would cause undesirable process variation that can compromise the high density and high performance of Doshi’s integrated circuits.

2J. Doshi discloses that the junction depth of the diffusion region 7 is on the order of 0.3 μm (300 nm). Ex. 1005, col. 6:57-64. Moreover, a POSITA would have readily recognized the height of the nitride sidewall 30 on the gate electrode 10 would be on the order of several hundred nm, as Doshi discloses that the height of the BPSG layer is on the order of 500 nm. Ex. 1005, col. 8:32-36. Thus, consistent with the common understanding of a POSITA, an aggressive over-etch

to remove the silicon nitride layer 30 on the sidewall would likely damage the diffusion region 7, in contrast to Doshi's goal of achieving tight dimensional control to achieve the desirable dimensions for the high performance. 1005, col. 6:57-64. I note that Mr. Maltiel offered a similar statement during his deposition when discussing the '997 patent:

Petitioner: "Without the oxide layer 60, the anisotropic etch of the conformal nitride layer 62 would etch the diffusion region 58, correct?"

Mr. Maltiel: "Well, unless you -- it's -- again, you have selectively with the nitride and the silicon. So when you etch the layer 60, you -- you still -- what I'm saying, *if you don't have the layer 60*, so when you etch the nitride layer 62, you still would be able to stop on the silicon. *You likely can damage it if you go for too long*. But if you have one controlled process, you would be able to manage it. But this is part of the reason why you have layer 60 there."

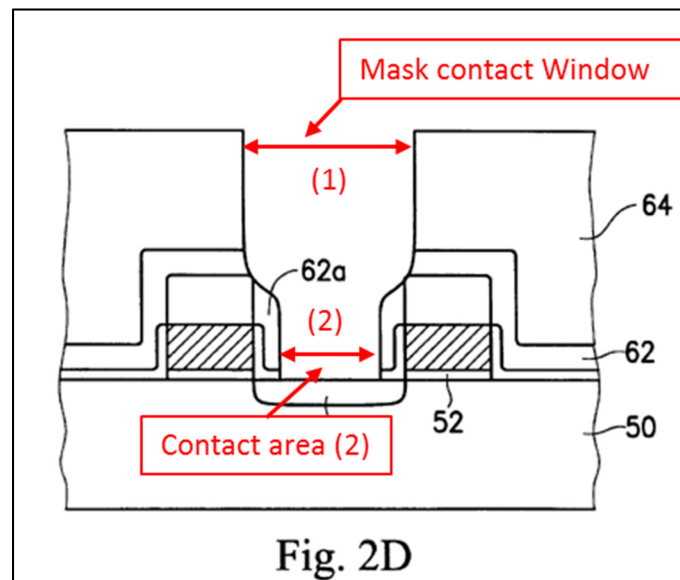
Ex. 1012 at 156:2-14 (emphasis added).

2K. Thus, a POSITA would not have been led to conclude that Doshi's etch process completely removes the layer 30 from the contact holes because the over-etch contemplated by such an interpretation would likely damage the diffusion region 7 of Doshi's device. Complete removal of the layer 30, therefore, would be inconsistent with Doshi's teachings indicating the desirability to tightly control the small, critical dimensions of the diffusion region 7 due to its particular sensitivity to process variations and parameters.

3A. HSC states that "Doshi's specification teaches that nitride layer 30 is removed from the contact hole locations during the nitride etch step." Paper 18, pp.

16-17. HSC points to Fig. 3k of Doshi to support this statement, pointing out that Fig. 3k shows that silicon nitride 30 is completely removed from sidewalls during a bit line contact (BLC) formation. Paper 18, pp. 18-22; Ex. 2002, ¶ 68. Mr. Maltiel declares that there is no indication that Fig. 3k's depiction of the etch process in the BLC location is erroneous or unreliable. Paper 18, 21; Ex. 2002, ¶ 69. However, I believe Fig. 3k appears erroneous and therefore unreliable. While Fig. 3g's depiction of the PC holes is largely consistent with the rest of Doshi's disclosure, Fig. 3k's depiction of the BLC hole, in contrast, directly undermines Doshi's express goal of minimizing damage to structures 10 and filaments 11. That is, because Fig. 3k fails to show a self-aligned contact hole formed by Doshi's two step etch process, a POSITA would have recognized that the gate structures 10 and sidewall filaments 11 may be damaged during etching as a result of even a minor mask misalignment. A POSITA would have recognized that the depiction of the BLC hole in Fig. 3k is erroneous in that it should have shown the silicon nitride layer 30 remaining on the sidewalls, thereby depicting the BLC hole as a self-aligned contact hole consistent with Doshi's goal of protecting structures 10 and filaments 11 from damage. Given the anisotropy of the two-step etch process used for both the PC and BLC formation and Doshi's goal of minimizing damage, a POSITA would have concluded that nitride 30 would remain on sidewalls of both Figs. 3g and 3k, with Fig. 3k being erroneous for failing to depict this nitride.

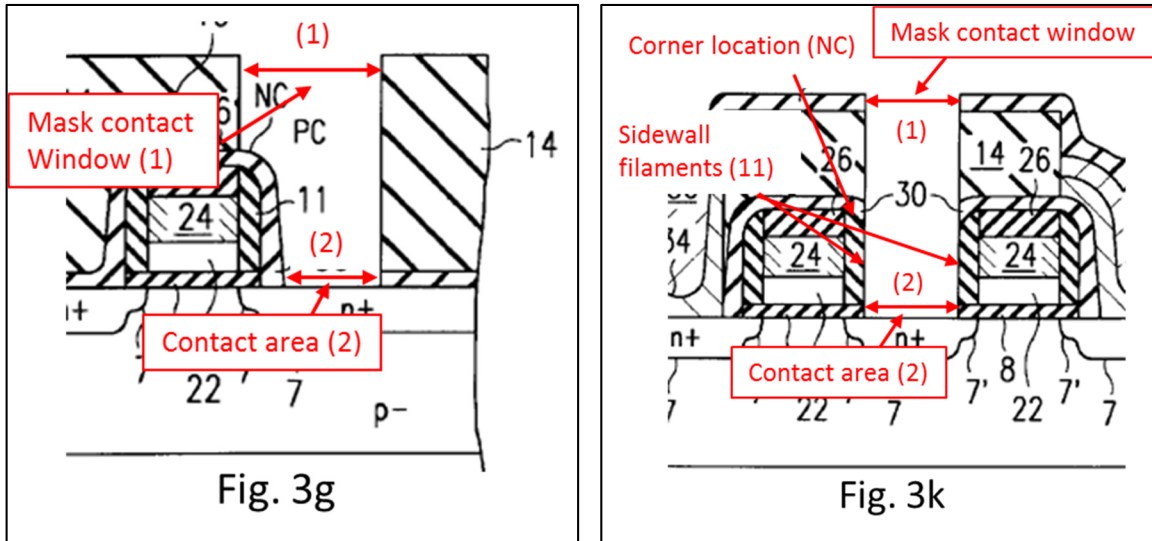
3B. Referring to the annotated Fig. 2D of the '997 patent below, a self-aligned contact hole is a single-mask process where the dimension of the mask contact window is oversized relative to the dimension of the contact area underneath in order to eliminate the alignment tolerance required by additional masks. Ex. 1001, col. 1:10-23; Ex. 1003, ¶ 15; Ex. 2002, ¶ 22. The self-aligned contact hole is achieved by a two-step etch, where the first etch uses the silicon nitride layer 62 as a etch stop, and the second anisotropic etch ensures that the portion of the diffusion region 58 exposed by the second silicon nitride etch is determined by the lateral dimensions of the spacer 62a, and not by the dimension of the lithography mask. Ex. 1001, col. 3:10-24; Ex. 1003, ¶ 21.



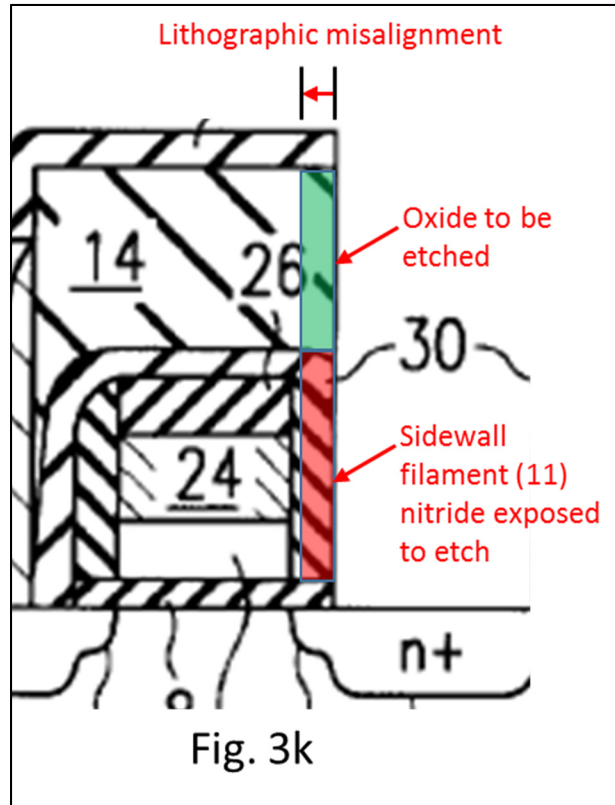
3C. Doshi also discloses a method for forming a self-aligned contact hole. Paper 1, pp. 19-20; Ex. 1003, ¶ A-1. Similar to the '997 patent, the self-aligned contact openings in Doshi are formed using a two-step etch process. Ex. 1005,

Abstract and col. 9:25 – 10:16. The first etch selectively etches BPSG insulating layer 14 relative to the silicon nitride layer 30, and stops on the silicon nitride layer 30. *Id.*, Fig. 3f; Ex. 1003, ¶ A-12. The second, highly anisotropic, etch is a timed etch that removes the silicon nitride layer 30 to expose the diffusion regions 7. Ex. 1005, col. 9:64 – col. 10:16 and col. 10:63 – col. 11:9; Ex. 1003, ¶ A-12.

3D. Comparing the annotated Fig. 3g with the annotated Fig. 3k below, Fig. 3g shows that the dimension of the mask contact window is indeed oversized relative to the dimension of the contact area. This is consistent with a POSITA's understanding of a self-aligned contact hole. On the other hand, Fig. 3k shows that the dimension of the mask contact window matches the dimension of the contact area, suggesting to a POSITA that Fig. 3k may be erroneous. The depiction of a contact hole in Fig. 3k would not be consistent with a POSITA's understanding of a self-aligned contact hole, as there is no room for any lithographic misalignment.

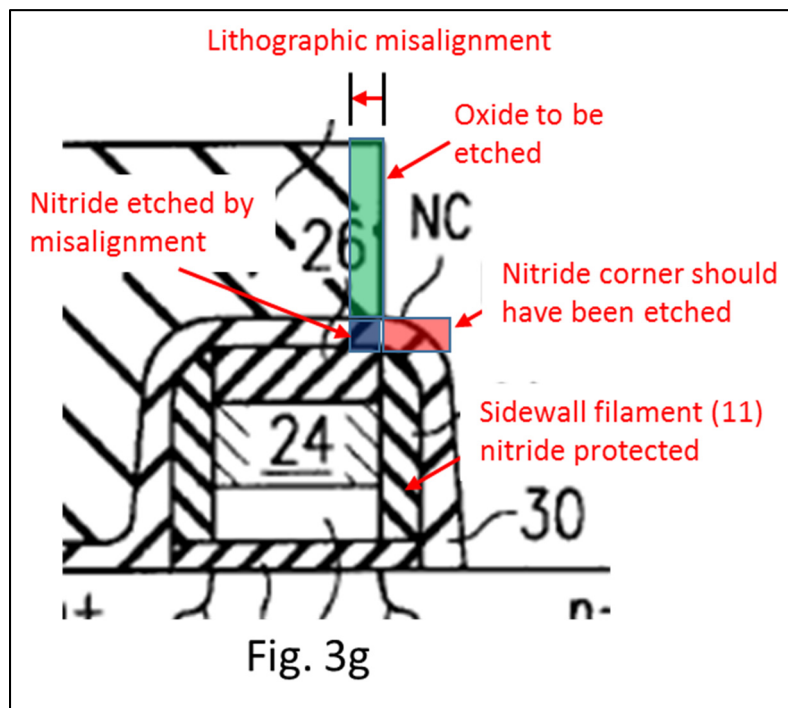


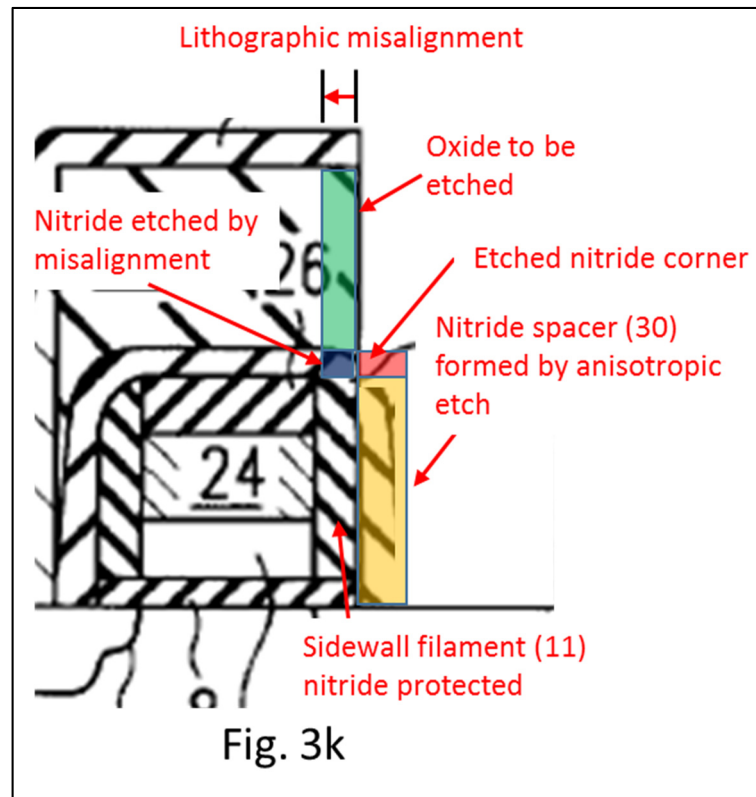
3E. As an example, according to Fig. 3k as revealed by the annotations shown below, any misalignment would result in Doshi's highly anisotropic silicon nitride etch damaging the sidewall filaments 11. Ex. 1005, col. 7:57-62. The result is shown in the annotated Fig. 3k below, where a lithographic misalignment would cause the BPSG oxide (shown in green) to be etched by the first oxide etch, and some portion of the nitride of the sidewall filament 11 (shown in red) exposed to the second nitride etch. A POSITA would have recognized that this result would directly contradict with Doshi's disclosure that the second nitride etch is used to clear silicon nitride layer (30), without damaging corner locations (NC) of the sidewall structures (11). Ex. 1005, Abstract. Thus, HSC's interpretation of Fig. 3k would be rejected by a disinterested POSITA.



3F. On the other hand, if the sidewall silicon nitride layer 30 is not etched away by Doshi's highly anisotropic etch as shown in the revised version of Fig. 3k below, the BLC hole would be a self-aligned contact hole akin to the PC holes shown in Fig. 3g. As evident by comparing the annotated version of Fig. 3g to the revised version of Fig. 3k below, both the PC holes and the corrected BLC hole would tolerate lithographic misalignments without exposing the sidewall filaments 11 to damage, a result consistent with Doshi's expressly stated goal that the etch of the nitride layer 30 not damage the filaments 11. Thus, contrary to HSC's assertion, it is Fig. 3k, rather than Fig. 3g, that requires reconciliation for it to properly reflect Doshi's teachings. HSC advances that Fig. 3g is "riddled with

errors.” Paper 18, p. 18. I disagree. Consistent with my previous declaration, I note that even with a misalignment, the anisotropic etch of silicon nitride would have removed the same thickness of the silicon nitride covering the diffusion region and the silicon nitride at the corner (covered in yellow). Ex. 1003, ¶ A-14. Other than the one error that I previously pointed out in my December 16, 2014 Declaration, Fig. 3g is wholly consistent with Doshi’s disclosure.





4A. HSC states “[e]ven if we ignore the teaching of Doshi and accept Samsung’s argument that nitride layer 30 is left on the sidewalls of the gate electrode is a spacer, it would not satisfy the ‘simultaneously forming’ requirement of claims 1 and 9.” Paper 18, p. 22. HSC cites to my statement during deposition that prior to the nitride etch, the silicon nitride layer 30 can perform the function of spacing between two conductive structures. Paper 18, pp. 22-23. I believe HSC’s characterization of my testimony is improper and misleading, as HSC has omitted my subsequent statements that follow the statements quoted by HSC, where I acknowledged that whether Doshi discloses a structure that may function as a spacer before the nitride etch process is not the proper inquiry:

HSC: “So it is not a spacer?”

Dr. Rubloff: “Well, a diffusion barrier is a kind of spacer.”

HSC: “Okay. So it is a spacer?”

Dr. Rubloff: “Yes.”

HSC: “Okay.”

Dr. Rubloff: “*But that's not the spacer that's at issue here.* I realize that.”

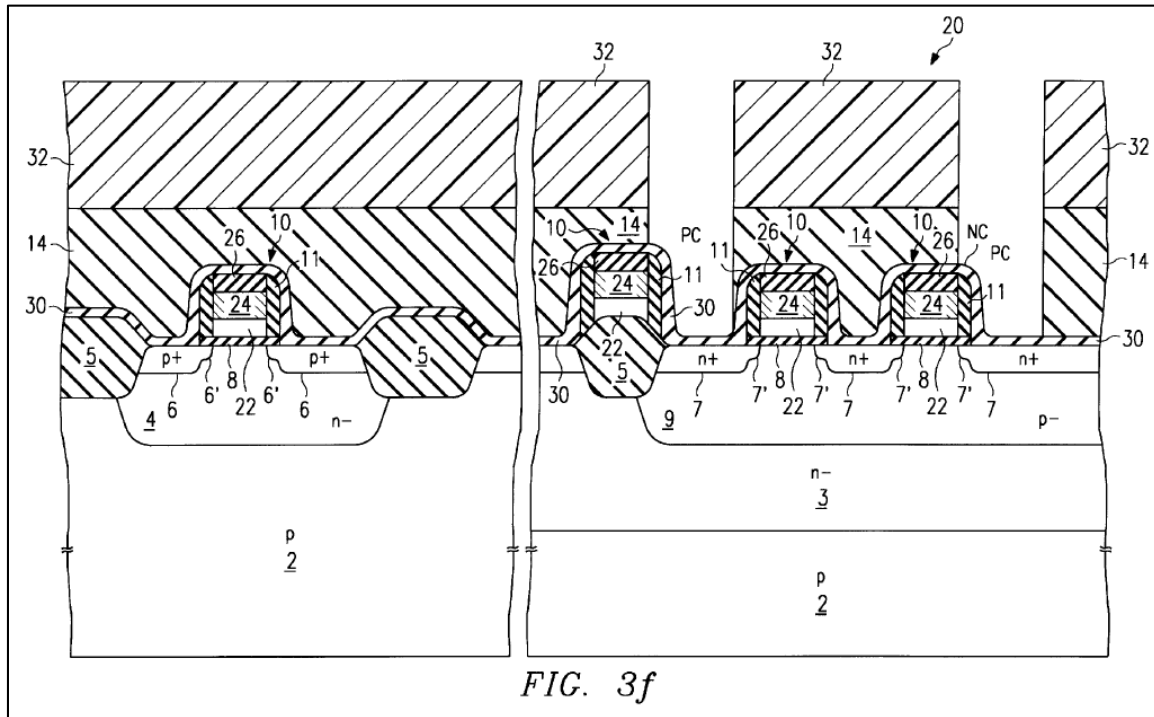
HSC: “I don't follow you.”

Dr. Rubloff: “No. *I think your question was, at this stage after both etches of BPSG and nitride is done, how do we know there's still a nitride sidewall spacer?* And that's a different -- that's a different question.”

Ex. 2004 at 196:10 – 197:1.

5A. Mr. Maltiel declared that even though the nitride etch in Doshi is anisotropic, it would still be able to clear a thin layer like nitride layer 30. Ex. 2002, ¶ 71. I disagree with his reasoning. First, he declared that some of the nitride layer would already be removed during the initial oxide etch. However, Doshi discloses that etching of the BPSG layer 14 is relatively highly selective relative to etching of nitride layer 30, and the oxide etch will tend to stop on nitride layer 30. Ex. 1005, col. 9:48-50. Moreover, looking at Fig. 3f of Doshi, a POSITA would have recognized that this oxide etch is anisotropic. Thus, if any of the nitride layer is to be removed during the initial oxide etch, a POSITA would have understood that more nitride on the diffusion region would have been removed

than the nitride on the sidewall of the gate electrode, and this would further help with the sidewall spacer formation.



5B. Mr. Maltiel further declared that an anisotropic nitride etch would still remove some material in the lateral direction, and that the nitride etch would be designed to include over etch to ensure that there is no nitride or residual oxide left on the substrate surface that could interfere with forming a good contact. Ex. 2002, ¶ 71. A POSITA would have recognized that even with an over etch, the anisotropic etch would not be able to completely remove the nitride layer 30 on the sidewall. A POSITA would have understood that a comparison between the etch rate that is perpendicular to the wafer surface and the etch rate that is lateral to the wafer surface would determine the anisotropy of an etch. Ex. 1014, p. 3.

Assuming, for example, that the etch rate in the perpendicular direction is 10 Å per second, a POSITA would have understood that the etch rate in the lateral direction would be much less than 10 Å per second for a highly anisotropic etch. As an example, if the etch rate in the lateral direction is 1 Å per second, a POSITA would have understood that it would take 10 times as much time to remove the material laterally than to remove the material vertically. As another example, if the etch rate in the lateral direction is 2 Å per second, a POSITA would have understood that it would take 5 times as much time to remove the material laterally than to remove the material vertically. A POSITA also would have understood that the purpose of an over etch is to ensure that there is no nitride or residual oxide left on the substrate surface, and would not have selected an over etch time that is several times that of the calculated etch time needed to clear out the contact area by the vertical etch, as it would risk damaging the devices (e.g., diffusion region) underneath. Therefore, a highly anisotropic etch in Doshi would form a nitride film on the sidewall of the nitride instead of completely clearing it.

5C. Mr. Maltiel declared that Doshi is, at best, agnostic as to whether any residual nitride material remains on the gate structure. Ex. 2002, ¶ 72. I disagree. As I have declared earlier, Fig. 3g of Doshi explicitly shows a spacer being formed by the nitride layer 30. Ex. 1003, ¶¶ A-12 to A-14. Doshi's disclosure that the nitride etch is brief and highly anisotropic would further lead a POSITA to

recognize that the nitride etch would form a nitride spacer on the sidewall of the electrode 10.

5D. Mr. Maltiel declared that any nitride materials left on the sidewalls would not have a predictable and uniform shape or thickness, and depending on this residual material as a spacer would greatly increase the risk of conduction between the gate and the contact plug. Ex. 2002, ¶ 74. I disagree. Doshi discloses that the thickness of the nitride layer can range from 65 Å to 250 Å. Ex. 1005, col. 8:19-20. Doshi further discloses that the etch for this layer is a timed etch that is brief and highly anisotropic. *Id.*, col. 9:64 – col. 10:16. A POSITA would have recognized that a profile of the spacer would be predictable under a timed etch. A POSITA would have recognized that the thickness of the nitride layer can be selected to yield a desirable profile. Moreover, a POSITA would have recognized that forming a spacer using the silicon nitride layer 30 would decrease, not increase the risk of conduction between the gate and the contact plug, as the sidewall filaments 11 also would provide additional physical separation between the gate and the contact plug.

6A. HSC states that during the oxidation of the polysilicon gate sidewalls, the diffusion regions are covered by the gate oxide layer, and not uncovered doped silicon. Paper 18, p. 28. During my deposition, I declared that whether the exposed region is uncovered silicon, or silicon covered by thin oxide, an oxide layer would

be formed because thermal oxide has linear growth rate in the thin regime. Mr. Maltiel declared during his deposition that it is unlikely that an oxide layer would be formed on the gate oxide during the thermal oxidation of the polysilicon gate sidewalls:

Petitioner: "But that oxide layer 8 would be exposed to further oxidation, correct?"

Mr. Maltiel: "It's -- I mean, it's a short process and the polysilicon oxidize faster, and it's not likely that the -- you will create more oxide when you have already oxide layer 8 on the substrate there which are the extension. If you go -- and you don't want to have this process too long anyhow because you just want to cover the edge of the polysilicon gate with a oxide layer, so it's -- it's a different case.


Ex. 1012 at 170:10-20.

6B. I disagree with Mr. Maltiel's statement. Doshi discloses that the junction depths in MOSFET transistors with 0.5 μm channel lengths and smaller are typically on the order of 0.30 μm . Ex. 1005, col. 1:30-32. A POSITA would have understood that generally, for a 0.5 μm device channel length, the gate oxide layer would be on the order of a few nanometers. A POSITA would have understood that this oxide layer thickness would be within the linear growth rate regime. Thus a POSITA would have understood that a thicker oxide layer would be formed over the diffusion region during the thermal oxidation of the polysilicon gate sidewalls. That is, even if the diffusion region is covered by a gate oxide layer during the oxidation of the polysilicon gate sidewalls, a thicker oxide layer

would still be formed during oxidation, and the resulting thickened oxide layer covers the diffusion region.

Conclusion

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Signature: 
Gary W. Rubloff, PhD

Date: 11/30/2015