

1 UNITED STATES PATENT AND TRADEMARK OFFICE
2 BEFORE THE PATENT TRIAL AND APPEAL BOARD
3

4 SAMSUNG ELECTRONICS CO. LTD,
5 SAMSUNG ELECTRONICS AMERICA, INC.,
6 SAMSUNG SEMICONDUCTOR, INC., and
7 SAMSUNG AUSTIN SEMICONDUCTOR, LLC.

8 Petitioner

9 vs.

10 HOME SEMICONDUCTOR CORPORATION

11 Patent Owner

12 Case IPR2015-00459 Patent 6,150,244
13 Case IPR2015-00460 Patent 6,146,997
14 Case IPR2015-00466 Patent 6,030,893
15 Case IPR2015-00467 Patent 6,030,893
16

17 VIDEO DEPOSITION OF RON MALTIEL

18 Redwood City, California

19 November 9, 2015

20 VOLUME I (Pages 1 – 194)
21
22

23 Reported by:

24 Rebecca L. Romano,

25 RPR, CSR No. 12546

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17 Video Deposition of Ron Maltiel, taken on
18 behalf of the Petitioner, Fish & Richardson, P.C.,
19 500 Arguello Street, Suite 500, Redwood City,
20 California, beginning at 9:26 a.m., November 9,
21 2015, before Rebecca L. Romano, Certified Shorthand
22 Reporter, No. 12546.
23
24
25

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2

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20 ALSO PRESENT:

21 Jason Saylor, Videographer

22

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1 Redwood City, California, November 9, 2015

2 9:26 a.m.

3 ---o0o---

4

5 THE VIDEOGRAPHER: Here begins

6 Disc No. 1, Volume No. 1 in the deposition of

7 Ron Maltiel in the matter of

8 Samsung Electronics Company, Ltd.,

9 Samsung Electronics America, Incorporated,

10 Samsung Semiconductor, Incorporated, and

11 Samsung Austin Semiconductor, LLC, versus

12 Home Semiconductor Corporation.

13 Today's date is November the 9th, 2015.

14 The time is 9:26 a.m. This deposition is being

15 taken at Fish & Richardson, PC, 500 Arguello

16 Street, Suite 500, in the city of Redwood City,

17 California 94063, and was made at the request of

18 the petitioner.

19 I am Jason Saylor, the videographer, and

20 the court reporter is Rebecca Romano from

21 Gregory Edwards, LLC.

22 Counsel and all present, please identify

23 yourselves and state whom you represent.

24 MR. COLAIANNI: Joseph Colaianni of

25 Fish & Richardson on behalf of the Samsung

1 petitioners.

2 MR. HSIEH: Andy Hsieh of
3 Fish & Richardson representing petitioner, Samsung.

4 MR. CHEN: Jerry Chen from
5 TechKnowledge Law Group for Home Semiconductor.

6 THE VIDEOGRAPHER: The court reporter
7 will now please swear in the witness.

8 THE REPORTER: If you could raise your
9 right hand for me, please.

10 THE DEPONENT: (Complies.)

11 THE REPORTER: You do solemnly state,
12 under penalty of perjury, that the testimony you
13 are about to give in this deposition, shall be the
14 truth, the whole truth and nothing but the truth?

15 THE DEPONENT: I do.

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1 RON MALTIEL,
2 having been administered an oath, was examined and
3 testified as follows:
4

5 EXAMINATION

6 BY MR. COLAIANNI:

7 Q. Good morning.

8 A. Good morning.

9 Q. Could you state your full name for the
10 record, please.

11 A. Ron Maltiel.

12 Q. And it's Dr. Maltiel, correct?

13 A. No, no, no. I have a -- I'm not a
14 doctor. I have a master and engineering degree
15 also.

16 Q. Okay. And would you state your address
17 for the record, please, Mr. Maltiel.

18 A. 19743 Yuba Court, Saratoga, California
19 95070.

20 Q. And you understand that you have taken an
21 oath today?

22 A. Yes.

23 Q. And you've been deposed before, have you?

24 A. Yes.

25 Q. Approximately how many times?

1 A. I am not sure. Like 13 or 14 times, I
2 believe.

3 Q. Were your prior depositions in connection
4 with patent infringement actions?

5 A. Mostly.

6 Q. You have served as an expert in patent
7 infringement actions before, correct?

8 A. Yes.

9 Q. Approximately how many -- how many times
10 have you served as an expert?

11 A. I'm not sure. It's something more than
12 30.

13 Q. Okay. And in your prior depositions, did
14 you testify on the topic of invalidity before?

15 A. Yes.

16 Q. How about infringement; did you ever
17 testify about -- relating to infringement?

18 A. Yes.

19 Q. Has a court or agency ever excluded any
20 of your opinions from evidence for any reason?

21 A. No.

22 Q. Have you ever worked for
23 Home Semiconductor in the past?

24 A. I mean, I worked in this case and related
25 case.

1 Q. Prior -- prior to this action, had you
2 worked for Home Semiconductor before?

3 A. No.

4 Q. When you said you worked on a related
5 case, what were you referring to?

6 A. Before the IPR exchange, there was a case
7 regarding a -- some assumption products. It --
8 it's -- it's related case. It was put on hold due
9 to the IPR.

10 Q. I see.

11 You were a rep working for
12 Home Semiconductor in connection with the District
13 Court action between Samsung and Home
14 Semiconductor; is that correct?

15 A. Yes.

16 Q. And you were working on that District
17 Court action in your capacity as an expert or some
18 other capacity?

19 A. As an expert.

20 Q. Okay. Did you provide a deposition in
21 that case?

22 A. No. I believe no.

23 Q. That case has been stayed --

24 A. Yes.

25 Q. -- correct?

1 Have you ever worked for or adverse to
2 Samsung prior to this action?

3 A. Yes.

4 Q. Okay. Do you recall which -- which
5 actions?

6 A. I don't really recall the cases. It's --
7 it's stated on my CV. I just don't remember. I
8 think the Rambus case. It was against Samsung
9 and -- yeah. And it seems to have been other
10 cases. I think it may be many years ago I worked
11 for Fish & Richardson on a case. It was a Samsung
12 case, but I'm not 100 percent sure. If it was a
13 Samsung case or not, I don't remember now.

14 MR. COLAIANNI: Okay. Let's mark as our
15 first exhibit today a copy of Exhibit HOME-2003.
16 This is a copy, I believe, of your CV.

17 (Exhibit 1 was marked for identification
18 by the court reporter and is attached hereto.)

19 Q. (By Mr. Colaianni) Do you recognize what
20 the court reporter has marked as Exhibit 1?

21 A. It look like my CV.

22 Q. Did you prepare Exhibit 1?

23 A. Yes.

24 Q. Okay. And does Exhibit 1 look accurate,
25 to the best of your knowledge?

1 A. I mean, I have to use both to compare if
2 it's accurate, but it look accurate.

3 Q. Okay.

4 A. Because it could be someplace some more
5 the -- but -- but it look like, yes.

6 Q. Okay. And you have been a consultant
7 since 1993; is that correct?

8 A. Yes.

9 Q. And part of your consulting work is
10 serving as an expert witness in patent infringement
11 matters, correct?

12 A. Yes.

13 Q. Approximately what percentage of your
14 consultancy involves work on patent infringement
15 matters?

16 A. I mean, it varies. It's how -- I never
17 looked at it as a percentage. I'm not sure what is
18 the answer.

19 Q. Yeah, I don't need anything exact.

20 I mean, would you say that half or more
21 than half of your -- your work is derived from
22 patent infringement actions?

23 A. Probably more than half, I would say.

24 Q. Is it more than 75 percent?

25 A. I don't know, because it's varied at what

1 time period we are talking. It's -- I mean, it's
2 hard to put it more accurate -- more precisely than
3 more than half.

4 Q. And what other types of consultancy work
5 have you done since 1993, besides patent
6 infringement litigation work?

7 A. In the semiconductor field, in -- I have
8 start up other companies that want to do some work
9 in semiconductors. And I consult investors that is
10 interested to invest in new semiconductor
11 technology or in stocks of semiconductor
12 technology. And I consulted companies that were
13 evaluating patent portfolio for investment purposes
14 of that nature.

15 Q. Okay. And you have attached to your CV a
16 list of litigation-related experience at the back
17 of Exhibit 1.

18 Do you see that?

19 A. Yes. I mean -- you mean starting from
20 page 4?

21 Q. Correct.

22 A. Uh-huh.

23 Q. Did you prepare this list of -- of
24 litigations?

25 A. Yes.

1 Q. Okay. Is this complete, at least as to,
2 I guess, 2013?

3 A. I believe so, yeah. I believe it is. I
4 mean, to the best of my knowledge, yeah.

5 Q. You mentioned that you had done some
6 consulting in connection with start-ups; is that
7 correct?

8 A. Yeah.

9 Q. Were those start-up companies that you
10 were involved in forming or just that you were
11 consulting with as an -- as an outside consultant?

12 A. Outside consultant.

13 Q. I see.

14 So your last work for a semiconductor
15 company was with Maxim Integrated Products; is that
16 correct?

17 A. As an employee. I also have a blog that
18 I publish a lot of information about semiconductor
19 technology, application and implementation in the
20 market.

21 Q. That's a blog that you -- you created?

22 A. Yeah, for the last ten years.

23 Q. On page 3 of Exhibit 1, you have a number
24 of patents identified.

25 Do you see that?

1 A. Yes.

2 Q. Were these patents that you filed for
3 while you were working in industry?

4 A. Yes. I said to them measuring the
5 nondestructive -- not the -- the measuring of
6 them -- they -- the first two -- no, sorry. The
7 first one and the third one, the '923 and the '611,
8 I think I was -- I was -- I file it in between
9 companies, but I don't remember exactly the dates,
10 so -- of the filing of the patents.

11 Q. Okay. But these patents were filed while
12 you were working with Intel or Maxim or AMD, or one
13 of the companies that you were with in the
14 industry, correct?

15 A. They were filed during the time period
16 that I was an employee of semiconductor -- well,
17 some of them, like the gold-doped IC resistor, this
18 was filed when I was Stanford. And Intel was after
19 looking of using it. And then the three that
20 related to flash and DRAM, they -- the '552, the
21 '580, and I believe it's '309 were filed after I
22 joined AMD.

23 The two other, I think they were filed
24 in -- I don't remember exactly, but they were filed
25 after I left AMD, before I joined Maxim, or

1 something like this for -- as for short period,
2 edification and so on.

3 Q. So the patents identified in -- on
4 page 3 were filed certainly before you left Maxim
5 in 1993, correct?

6 A. Correct. The patent were filed before
7 1993. The one about the -- the two related to
8 measuring the property of device through
9 manufacturing, the 55 -- the -- sorry -- '923 and
10 the '611, there was also a European application,
11 which I don't remember the date of it. And it was
12 a complicated process and I don't know what
13 happened to it. So I don't know about the date of
14 filing of that one, of the European one.

15 Q. Okay. Do you have any other patents
16 either issued or pending other than the six
17 mentioned in your CV?

18 A. Well, it was the one that I mentioned,
19 the European application. I only found out about
20 it later and -- so I don't remember the number of
21 the -- but it's related to them -- the '611 and the
22 '923.

23 Q. Okay. Let's talk a little bit about your
24 work on this matter, but do you recall when you
25 were first contacted to work on this IPR?

1 A. I don't recall exactly -- oh, the IPR or
2 the -- because, see, I started initially on the
3 district case it is now in state. And the IPR, I
4 would say within the last nine months roughly.
5 Less than a year, I would guess, because I don't
6 remember exactly.

7 Q. Okay. And as part of your work on the
8 IPR, you prepared several declarations, correct?

9 A. Yes.

10 Q. And approximately how much time did you
11 spend preparing those declarations?

12 A. I don't know. I would say more than
13 100 hours, but I'm not sure. I never quantified.

14 Q. Okay. And you mean -- you say the 100
15 hours, you mean on the -- the three declarations
16 you prepared together?

17 A. Well, the -- the '893 is two, so I put it
18 four IPR. But, yeah, I'm talking about all of
19 them. I -- not -- I don't know all four. One by
20 itself because I never look at it by itself. I
21 mean, I -- when I do the preparation, I work on --
22 sometimes on these and sometimes on other, but I
23 don't quantify it.

24 Q. And are the material that you relied on
25 in preparing your declarations identified in the

1 declarations?

2 A. Yes. I believe so, yeah.

3 Q. There's nothing that you relied on that
4 is not identified in the declarations?

5 A. Well, my industry experience. But this
6 way, it's -- I guess my industry experience is
7 identified by my CV, I guess you can say. But
8 there wasn't a document that I used, as far as I
9 remember, that wasn't identified.

10 Q. Okay. Was there anything that you wanted
11 to -- strike that.

12 Was there any materials that you
13 requested, but that were not provided to you?

14 A. I don't think so.

15 Q. Okay. So you felt you had sufficient
16 information to form the opinions that are expressed
17 in your declarations?

18 A. Yes.

19 Q. You attended the deposition of Samsung's
20 experts, correct?

21 A. Yes.

22 Q. Dr. Rubloff.

23 A. Yes.

24 Q. Do you know Dr. Rubloff? Are you
25 familiar with his work?

1 A. Not before the deposition.

2 Q. Okay. Did you do anything to prepare for
3 today's deposition?

4 A. Yes.

5 Q. What did you do?

6 A. I mean, I review my declarations and
7 thought about stuff and basically this kind of...

8 Q. Are there any documents you reviewed
9 besides your declarations?

10 A. Well, I reviewed a -- some of the stuff
11 that is referenced in deposition.

12 Q. So some of the materials that were
13 referenced in Dr. Rubloff's deposition?

14 A. No, no, in my deposition.

15 Q. Okay. Are -- are you referring to your
16 declaration?

17 A. Yeah, that in my dec- -- I refer to my
18 declaration. And in my declarations was some
19 reference, so I look briefly at these references or
20 reference.

21 Q. Okay. Did you -- did you speak to
22 anybody to prepare for today's deposition?

23 A. I spoke with the attorney, Jerry.

24 Q. Besides the attorney, did you speak to
25 anybody else to prepare for the deposition?

1 A. No.

2 Q. Do you recall how much time you spent
3 preparing for the deposition?

4 A. I'm not sure. I'm not sure. I have to
5 prepare for the deposition. I mean -- I don't
6 know -- 20, 30 hours, maybe more. I'm not sure.

7 Q. Okay. So let's start -- I think what we
8 should do is start with the IPR that is numbered
9 IPR 2015-00466, and this is an IPR involving the
10 '893 patent.

11 Okay?

12 A. Okay.

13 Q. Do you recall preparing a declaration in
14 connection with that IPR?

15 A. Yes.

16 MR. COLAIANNI: So let's -- let's mark a
17 few exhibits. We'll mark as Exhibit 2
18 SAMSUNG-1001 -- this is the '893 patent. And we
19 can mark as Exhibit 2 your declaration, in
20 connection with the '466 IPR, which is marked
21 HOME-2002.

22 (Exhibits 2 and 3 were marked for
23 identification by the court reporter and are
24 attached hereto.)

25 Q. (By Mr. Colaianni) Do you recognize

1 Exhibit 2 and 3?

2 A. I mean, they look like -- Exhibit 2 look
3 like the '893 patent. And Exhibit 3 -- it's a long
4 document, but it look like my declaration regarding
5 the 00466 IPR.

6 Q. Okay. And you studied the '893 patent in
7 connection with your work on the '466 IPR, correct?

8 A. Yes.

9 Q. Did you read the '893 patent's
10 prosecution history as well?

11 A. Yes.

12 Q. The '893 patent talks about forming a low
13 stress second tungsten layer, correct?

14 A. Right. It's one of the thing it mention.
15 It has many other thing, but it is one of the
16 thing --

17 Q. Correct.

18 A. -- it includes.

19 Q. The -- the '893 patent discloses, in a
20 traditional tungsten CVD process, a first layer of
21 void-free and good step coverage tungsten film is
22 deposited to fill a contact hole, correct?

23 MR. CHEN: Objection. Form.

24 THE DEPONENT: It's -- it's part of the
25 thing it describe, yeah.

1 Q. (By Mr. Colaianni) And the '893 patent
2 discloses that that -- in -- in the traditional
3 process, the first layer has what's referred to in
4 the patent as a high stress, correct?

5 A. Yeah, it's correct, the high stress, the
6 first one.

7 Q. And in connection with the traditional
8 tungsten CVD process, the '893 patent discloses the
9 formation of a second layer of tungsten film that's
10 deposited to fabricate interconnect lines, correct?

11 A. Yes.

12 Q. So let's take a look at figure 1 of the
13 '893 patent.

14 Figure 1 is illustrating prior art,
15 correct?

16 A. Yes.

17 Q. And figure 1 shows this first tungsten
18 film labeled as element 16, correct?

19 A. Yes.

20 Q. And that first tungsten layer is
21 deposited using a first CVD step, correct?

22 MR. CHEN: Objection. Form.

23 THE DEPONENT: Yeah, it is deposited
24 using a CVD process.

25 Q. (By Mr. Colaianni) Do you distinguish

1 between a process and a step?

2 A. Well, I'm trying to be more specific
3 because "step" is just a general term and "process"
4 is the way of making something.

5 Q. Does a process include multiple steps?

6 A. It -- sometimes. But process is more
7 discrete. It's -- it's varied on the circumstance.
8 It's hard to generalize, but a -- a -- a CVD
9 process could include the -- putting gases in
10 and -- and changing -- heating the wafer. So it
11 would be several -- you can call them steps. But
12 within -- so it can -- everything can cut to a
13 smaller and smaller increment and call each one a
14 step.

15 Q. Do -- okay.

16 Do -- do you have an understanding of the
17 term "step" as it relates to the, you know, field
18 of semiconductor fabrication?

19 A. Yes. It vary on the circumstance you are
20 talking about, but I understand the -- the way it
21 is in the semiconductor industry.

22 Q. In -- in -- in the context of fabricating
23 materials such as disclosed in the '893 patent, is
24 there some understanding of the word "step" that
25 you -- that -- that -- that you have?

1 A. Not so much for the '893. I mean, unless
2 you can point me to a specific example what you are
3 asking me about. But for a -- when you put a wafer
4 in a machine, like a CVD machine, you have several
5 operations, and this operation end up creating the
6 CVD layer. So this is what I was referring to in
7 CVD process.

8 Q. So in -- I just want to make sure we're
9 talking on the same --

10 A. Uh-huh.

11 Q. -- same page here.

12 A process can include one step or
13 multiple steps; is that fair?

14 MR. CHEN: Objection. Form.

15 THE DEPONENT: It depend on the
16 circum- -- circumstance. So you see I made it --
17 if you show me example what you mean or where you
18 find it in my declaration, I can explain further,
19 but I cannot just -- not in a -- just talk about it
20 because I'm not clear on the circumstance.

21 Q. (By Mr. Colaianni) Well, we were talking
22 about this first tungsten layer 16 in figure 1 --

23 A. Uh-huh.

24 Q. -- and you said it was formed by CVD
25 process.

1 A. Yeah.

2 Q. Does that formation of that first layer
3 include multiple steps?

4 A. So you see here today, if you look at the
5 '893, column 1, line 49, it says the first tungsten
6 film 16 is performed by using the first step of
7 chemical vapor deposition of tungsten, so -- I
8 mean, so when we need to look at the patent using
9 the language of the inventor and so he call here
10 the chemical vapor deposition creating the first
11 layer, the first step.

12 Q. And '893 patent talks about a second step
13 in which the second tungsten film 18 is deposited
14 on the first tungsten film 16, correct?

15 A. Yeah, 18. If we go to column 1, line 52,
16 it said the second tungsten film 18 is performed by
17 using the second step of chemical vapor deposition
18 of tungsten.

19 Q. The '893 patent discloses that the second
20 tungsten film 18 has high stress, correct?

21 A. The first -- the first one is high
22 stress.

23 Q. In the prior art, doesn't the patent talk
24 about the second tungsten film having high stress?

25 MR. CHEN: Objection. Form.

1 THE DEPONENT: You are talking about the
2 prior art. But -- I mean -- okay. So I thought
3 you talking about the -- the invention.

4 That in the prior art, it says that you
5 have high stress and that could cause wafer
6 bending. It's like line 55, column 1. They said
7 the tungsten -- the -- so the second tungsten film
8 18 is the high stress.

9 Q. (By Mr. Colaianni) The patent doesn't
10 explicitly state why the second tungsten film 18
11 has high stress, does it?

12 A. I believe it does not. Let me check.

13 Well, it says -- if you look at column 1,
14 line 54, it says that you don't do -- let me -- let
15 me read it.

16 Unfortunately, tungsten etching process
17 is absent in this conventional process, so the
18 second tungsten film is a high stress.

19 THE VIDEOGRAPHER: The time is 9:57 a.m.
20 and we are off the record.

21 (Recess taken.)

22 THE VIDEOGRAPHER: The time is 10:00 a.m.
23 and we are on the record.

24 Q. (By Mr. Colaianni) So are you saying
25 that the second tungsten film 18 in the prior art,

1 figure 1, is high stress because there's been no
2 etch-back process?

3 A. Yes.

4 MR. CHEN: Objection. Form.

5 THE DEPONENT: Yes, it's -- this is what
6 he's saying in the specification in column 1,
7 line 54 to 56 to 57.

8 Q. (By Mr. Colaianni) Was it known to
9 person skilled in the art, at the time of '893
10 patent, that performing an etch-back process could
11 reduce the stress of the film?

12 A. It was known that you can get either
13 properties from the -- in the manufacturing
14 process, but in -- it wasn't -- some people knew
15 about it, but it wasn't -- I mean, everybody know
16 about it.

17 Q. Is it -- is it possible to deposit a low
18 stress second tungsten film on top of a high stress
19 first tungsten film without doing etch back?

20 A. If you use different condition for the
21 deposition, you can have a different stress between
22 the different layers.

23 Q. What type of deposition would you need
24 to -- to do to achieve that?

25 A. Well, it's -- I mean, it's -- it states

1 here in claim 1 that you -- or either claim 1 -- so
 2 that by doing in a different temperatures, little
 3 steps, you can achieve low stress. Not by itself,
 4 including gases, it says, and concerning to change
 5 the specific flows and so on.

6 Q. Would the -- strike that.

7 The process that is described in prior
 8 art figure 1 of the '893 patent was performed in a
 9 single chamber, correct?

10 A. Yes.

11 Q. Was it known to persons skilled in the
 12 art at the time of the '893 patent to deposit of
 13 void-free, high stress first tungsten film followed
 14 by a low stress second tungsten film in a single
 15 chamber?

16 MR. CHEN: Objection. Form.

17 THE DEPONENT: It's -- I mean, it was
 18 known using certain specific -- a process condition
 19 that you can deposit these two film. But you
 20 wouldn't really fully completely fill the hole
 21 with -- without a void with the first layer. So
 22 it's -- wouldn't be something that he just will
 23 know from the top of his head, person of ordinary
 24 skill in the art.

25 Q. (By Mr. Colaianni) You -- you say that

1 it was not known at that time how to fill the
2 contact hole without a void; is that --

3 A. No.

4 Q. -- correct?

5 A. I was saying that you have to really be
6 very careful of the condition of how you make the
7 first layer in order to fully completely fill the
8 hole when -- when you deposit the first layer.

9 Q. Correct.

10 But under the right conditions, it was
11 known, at the time of the '893 patent, to form that
12 void-free first tungsten layer at high stress
13 followed by a low stress second tungsten layer all
14 in a single chamber, correct?

15 MR. CHEN: Objection to form.

16 THE DEPONENT: It -- I mean -- it was --
17 I mean, people knew that they can -- using a very
18 specific condition, they can get partially filled a
19 bottom -- with the bottom layers and then deposit
20 the top layers. But to get 100 percent fully
21 filled the bottom layers -- I mean, the hole with
22 the bottom layers without any void or crevasse was
23 known to be very tricky and it wasn't so obvious.

24 Q. (By Mr. Colaianni) Is it your testimony
25 that it was not possible to have formed a void-free

1 first high stress tungsten layer?

2 A. Yeah, it was possible, but we are talking
3 about what a person is skilled in the art, if he
4 get a new project and he supposed telling deposit
5 me a tungsten that would fill full the hole, you
6 wouldn't know if that -- it wouldn't be something
7 that would be known. Known by that time.

8 Q. If you look at -- back at figure 1 of the
9 '893 patent, does that figure show the contact hole
10 completely filled?

11 A. I mean, it is just an illustration. So
12 it shows -- it more time to show you where each of
13 the layers are related to the other. It's not a
14 ASM code section of a product. It's a digital. So
15 they are not really try to -- to be -- it's just an
16 illustration.

17 Q. But the illustration to figure 1 does
18 show the contact hole completely filled without any
19 voids, correct?

20 A. Yes. It shows filled without the void.

21 Q. And you testified a moment ago that the
22 process of figure 1 was performed in a single
23 chamber, correct?

24 A. The prior art.

25 Q. Correct. The prior art.

1 A. Yes.

2 Q. Were there disadvantages to formation of
3 semiconductor devices in a single chamber?

4 A. I mean, they would have an issue with
5 control of the process and the temperature drift
6 and try to show you exactly how this is described
7 here in the patent.

8 Yeah, it's in column 1, line, I guess,
9 15. So 21 -- so when you have a -- if I
10 remember -- is the question that -- can you repeat
11 the question.

12 Q. Sure.

13 My question was whether there were
14 disadvantages to formation of semiconductor devices
15 in a single chamber environment.

16 A. Uh-huh. Yeah. So -- this -- column 1 --
17 I mean, line 15 through 20, it's talking about
18 that -- using chemical vapor deposition
19 conventionally, the chemical vapor deposition of
20 tungsten is performing a single chamber because
21 going -- the tungsten film must fix the temperature
22 of the process. It cannot have any temperature
23 drift condition happen in order to keep the --
24 consistent quality of the film and the same
25 thickness of the film.

1 Q. What you just read from the patent is an
2 example of some disadvantages associated with the
3 single chamber process?

4 MR. CHEN: Objection to form.

5 THE DEPONENT: Well, it's -- it's an
6 issue that you have to be very careful about it
7 because -- they said when you make semiconductors,
8 it's a very delicate process. You are trying to
9 make million of devices that are very tiny and all
10 of them look the same. So you need to make sure
11 that for every tiny device on a dye, it would have
12 the same structure and the same properties.

13 So if you have temperature drift, you can
14 have a variation in the thickness. The reaction
15 wouldn't happen as well, and you can have on --
16 cause the die and cause you to report that someone
17 was able to lay a thicker layer, another transistor
18 to have a thinner layer. So this is why you need
19 to control it tightly.

20 Q. (By Mr. Colaianni) Despite those
21 concerns, it was possible to form a low stress
22 second tungsten layer in the single chamber at that
23 time, correct?

24 A. They -- stress is -- is a -- I mean, you
25 need to -- to produce the low stress film. It's --

1 you have to use certain kind of control -- control
2 condition. And so if you maintain this condition,
3 you can produce this low stress film.

4 Q. It was known in the art at the time of
5 the '893 patent to use multiple chambers for
6 formation of semiconductor devices; isn't that
7 correct?

8 MR. CHEN: Objection. Form.

9 THE DEPONENT: People were already using
10 different chamber for different purposes at the
11 time, yes.

12 Q. (By Mr. Colaianni) Were there advantages
13 to using multiple chambers as opposed to a single
14 chamber?

15 MR. CHEN: Objection to form.

16 THE DEPONENT: Well, using -- so, see,
17 people at the time are using multiple chambers or
18 different chamber are done. One was done for age;
19 one was done for deposition. And it would help the
20 throughput of the fab and -- because you -- you
21 have the wafer stay in the machine and so on. So
22 it was -- it was all being implemented using
23 multiple chamber for different purposes.

24 Q. (By Mr. Colaianni) Was it advantageous
25 to do the deposition and the etch steps in

1 different chambers?

2 A. Well, you -- usually you cannot do the
3 etch and deposition in the same chamber because
4 it's different and -- it's different type of
5 equipment, the one doing the etch and deposition.
6 And you don't have one chamber do both.

7 Q. Let's take a look at figure 2 of the '893
8 patent.

9 And figure 2 shows a contact hole formed
10 by etching of a dielectric layer 24; is that
11 correct?

12 A. Yes.

13 Q. Turn over the page to figure 4 of the
14 '893 patent.

15 Figure 4 shows the first conductive layer
16 30 filling the contact hole, correct?

17 A. Yes.

18 Q. And in figure 4, the contact hole is
19 completely filled, isn't it?

20 A. Yes.

21 Q. The first conductive layer 30 is formed
22 at a first CVD chamber, according to the '893
23 patent, correct?

24 A. Let me just look here at the patent.

25 Yes, in the column 2, line 60, you

1 describe for me the first conductive layer 24. And
2 the first conductive layer celtic on dielectric 24
3 and it's -- and goes on to the next page, column 3,
4 all the way to line 13. And we describe that --
5 that you formed this layer, the first layer in the
6 contact hole.

7 Q. The first conductive layer 30 can be
8 tungsten, correct?

9 A. Yes.

10 Q. And the first tungsten layer 30 has
11 properties of high stress, good step coverage and
12 it's void-free, correct?

13 A. Correct.

14 Q. What is your understanding of the
15 terminology "step coverage" in connection with the
16 '893 patent?

17 A. That -- when you -- see, when you start
18 the deposition, these structure are very deep
19 structure that -- they are much deeper than the
20 opening on the top. You can think of it like a
21 coffee mug or -- that is very tall.

22 So when you are trying to fill it, you
23 are trying to put layers on the tops of this, which
24 is the area surrounding the hole, in the side of
25 the hole, in the bottom of the hole.

1 And because it's much deeper than it's --
2 the opening is wide, you don't always get the same
3 rate of deposition on a bottom, on the side than
4 you get on the area surrounding the hole outside of
5 the hole.

6 Q. So would you characterize the step
7 coverage in terms of the deposition rate along the
8 sidewalls of the hole against the deposition rate
9 on the -- on the plainer surface?

10 MR. CHEN: Objection to form.

11 THE DEPONENT: It's -- you have to look
12 at the -- so, see, it's a three-dimensional process
13 that is happening real time. So the one thing
14 which is clear is that you compare deposition if
15 you have -- to a fully planar flat surface with no
16 hole nearby to what's happening along the wall of
17 the hole and the -- how much of the water we are
18 trying to deposit to reach the bottom of the hole.
19 And even the edge where the tip of the hole -- when
20 you get in the hole, this region by itself has a
21 different deposition rate than in the middle of the
22 wall.

23 Q. (By Mr. Colaianni) So how would you
24 characterize a -- a good step coverage in -- in the
25 context of the '893 patent?

1 A. A good step coverage would be that you
2 get the same deposition everywhere that I described
3 previously that -- outside of the hole and the rest
4 of the areas.

5 Q. So, for example, in figure 4 of the '893
6 patent, the thickness of the layer 30 outside the
7 hole appears to be the same thickness as the layer
8 inside the hole.

9 Does that indicate good step coverage?

10 A. Yes, because when you have same thickness
11 everywhere, then it's 100 percent -- it's 100
12 percent step coverage.

13 Q. So good step coverage would mean
14 approximately the same thickness of the layer
15 outside the hole as it would everywhere inside of
16 the -- the hole?

17 MR. CHEN: Objection to form.

18 THE DEPONENT: Yeah. I mean, a good step
19 coverage would give you the same thickness that is
20 surrounding the hole and then the edge of the hole
21 and along the wall of the hole and the bottom of
22 the hole.

23 Q. (By Mr. Colaianni) So uniformity of
24 thickness of the layer along the sidewalls of the
25 hole would be indicative of good step coverage; is

1 that fair?

2 A. Can you repeat it, please.

3 Q. Sure.

4 The uniformity of thickness --

5 A. Uh-huh.

6 Q. -- of the layer along the sidewalls of
7 the hole would be indicative of good step coverage?

8 A. Well, because, see, "uniformity" is a --
9 it's a broader term. And it's used to describe the
10 property of the layer that it deposit and how well
11 you control it in manufacturing. And it's -- it's
12 one of the parameters it could affect step
13 coverage, but it's not the only one that would
14 affect the step coverage.

15 Q. Well, non-uniformity -- well, non-uniformity of
16 thickness along the sidewalls would be indicative
17 of step coverage that is not good, though, correct?

18 A. So there are -- there are two separate
19 term. One is "uniformity" and another one is "step
20 coverage."

21 And you use -- so you see that having a
22 good uniformity, it's not good enough to ensure you
23 good step coverage. So this is why I cannot use
24 the word "uniformity" to -- to say whether you have
25 a good step coverage or not.

1 Q. I -- I understand.

2 Would you agree that uniformity of
3 thickness along the sidewalls would be something
4 that's indicative of good step coverage, even
5 though there are other factors that also would have
6 to be considered?

7 MR. CHEN: Objection to form.

8 THE DEPONENT: Not by itself because
9 it's -- it's not the only thing to determine. It's
10 also a question of how much you get to the bottom
11 of the contact, not just the sidewall that affect
12 the step coverage.

13 Q. (By Mr. Colaianni) The -- the thickness
14 along the bottom, that would be roughly the same as
15 the thickness along the sidewalls in order to
16 characterize step coverage as good?

17 A. You need it to be everywhere to be the
18 same thickness. The -- not just the -- the
19 sidewall, the bottom and so on and...

20 Q. The '893 patent itself doesn't define
21 step coverage, correct?

22 A. No, I -- I believe it doesn't define
23 the -- what is step coverage. It's -- it's
24 well-known in the industry.

25 Q. With respect to figure 4 -- going back to

1 figure 4, the patent discloses that the first
2 tungsten layer 30 fills the contact hole, correct?

3 A. Yeah, I believe it does. Yeah.

4 Q. The patent discloses that the height of
5 the contact hole can be from 10,000 angstroms to
6 50,000 angstroms, correct?

7 A. In the example they mention, yeah -- the
8 example for figure 2 in column 2, line 58 to 59, it
9 says the thickness of the dielectric layer 24 is
10 from 10,000 -- is about 10,000 to 50,000 angstrom.
11 So the contact hole in this would be the dimension
12 for the contact hole in figure 2.

13 Q. And the patent also discloses that the
14 thickness of the first tungsten film 30 ranges from
15 500 angstroms to 9,000 angstroms, correct?

16 A. Yes. In column 3, lines 6, it says
17 generally -- so the next one, line 7 -- the
18 thickness of the first conductive layer 30 has
19 500 to 9,000 angstrom thick.

20 Q. So converting that to microns, that would
21 be roughly .05 microns to .9 microns, correct?

22 A. Yes.

23 Q. How can a film that has a thickness from
24 .5 microns to -- excuse me -- .05 microns to
25 .9 microns fill a contact hole having a height from

1 10,000 to 50,000 angstroms?

2 MR. CHEN: Objection to form.

3 THE DEPONENT: He's just trying to show
4 that for the specific parameter that he's using,
5 what film thickness he can deposit. It's in
6 figure -- he doesn't use -- I mean, it's -- he
7 doesn't say the dimension, the weights of the --
8 the opening in figure 2.

9 Q. (By Mr. Colaianni) Is the hole filled
10 when the layer is deposited on the two sidewalls
11 meet?

12 A. Yeah. I mean, this -- I mean, when the
13 two sides meet. Basically, the way it shows in
14 figure 4, when the two sides meet, then the hole
15 is -- get filled.

16 Q. And the hole in figure 4 is completely
17 filled because there's no void after the tungsten
18 layer 30 is deposited, correct?

19 A. Yes.

20 Q. So a filled void-free contact hole is a
21 completely filled contact hole, correct?

22 A. Yes, in general. Because, see, it can
23 fill the void, but it don't necessarily -- because,
24 see, void is separate from filled contact because
25 it can create void when you halfway through the

1 deposition, not to wait to the end. Because, see,
2 if the two top -- the top of the tip of the --
3 the -- the opening of the contact, if these two
4 sides meet, this is your -- create the void at that
5 point, or if it happen low deep, so the void is
6 separate from fully fill.

7 Q. But a fully filled hole not having any
8 voids, correct?

9 A. Yeah. If it's fully filled, it wouldn't
10 have a void.

11 Q. So a completely filled contact hole would
12 be void-free; is that fair?

13 A. Yeah. But you see -- but going back to
14 earlier question about the thickness of the layer
15 deposited in the -- the size of the opening is also
16 defined -- he giving the range. So it's not the
17 description in column -- in -- starting from
18 column 2, line 60, all the way for column 3,
19 line 13.

20 He doesn't give just one value. He give
21 a range of value. So he's just showing you the
22 condition that will give you this kind of
23 properties of film.

24 Q. Okay. But just to be clear, a completely
25 filled contact hole is void-free, correct?

1 A. Yeah. If it's completely full, there
2 would be no void in it. I mean, even those are
3 independent term, you see, because they -- because,
4 you see, you have one term which is the "step
5 coverage" which is a bit different from "completely
6 filled."

7 Because, you see, you can completely
8 fill, it would look as if you have a good step over
9 it, but you have left a void in the middle. So --
10 so there -- there are really three separate term,
11 the "step coverage," the -- the "void" and
12 "completely filled."

13 Q. Right. No, I -- I understand.

14 I'm -- I'm just trying to clarify that a
15 hole that is completely filled will not have any
16 voids, correct?

17 A. It's -- I mean, it should be because you
18 see that the problem is that when -- when people
19 say they completely fill, they don't always know
20 whether it would leave a void or not. So see if
21 you -- if you -- basically, if you fully -- if it's
22 just the top, you connect just on the top, the two
23 edge of the top, you go the -- the tungsten so the
24 two sides match. And so if you look from the top,
25 it look as if it's completely filled. But it would

1 fill with every void because inside the hole you
2 didn't really fill it, and you can put a second
3 layer of tungsten underneath and so on. But the
4 figure that you have, the void would cause a little
5 problem with the reliability and other issue.

6 So you cannot use them as synonyms that
7 says if it's completely filled it's -- it doesn't
8 have void because completely filled, it's --
9 it's -- I mean, it's described of -- a certain
10 property that you see in certain circumstance. But
11 a void is something that -- it's a different --
12 it's not identical. It's related term, but it's
13 not identical.

14 Q. But -- but if a hole has voids in it,
15 it's not completely filled, right?

16 A. Yes, it wouldn't be completely. I mean,
17 it would still -- I mean, if it has a void, it
18 wouldn't be, in reality, completely filled, but it
19 could appear as if it's completely filled because
20 at the top get connected.

21 Q. Correct. It may appear that way from the
22 top, but -- but the hole would not be completely
23 filled if there are voids in there, correct?

24 A. On theoretical level you can say even
25 this, but when you are dealing with the

1 manufacturing world, then you cannot -- if somebody
2 comment that I did this thing and it looked
3 completely filled, you cannot know whether it has a
4 void or not. So it wouldn't be -- you wouldn't
5 know from somebody tell you, person skilled in the
6 art, it's completely filled, whether it has a void
7 or not.

8 Q. In the context of the '893 patent, a
9 completely filled hole is void-free, correct?

10 A. Well, yeah. The way it is described in
11 the patent that -- that when you completely filled
12 the hole using this conditions, it wouldn't produce
13 voids.

14 MR. CHEN: Is this a good time for a
15 break or --

16 MR. COLAIANNI: Sure. If you would like
17 to take a break, we can do that.

18 (Discussion off the stenographic record.)

19 THE VIDEOGRAPHER: The time is
20 10:36 p.m. -- a.m. and we are off the record.

21 (Recess taken.)

22 THE VIDEOGRAPHER: The time is 10:53 a.m.
23 and we are on the record.

24 Q. (By Mr. Colaianni) In the context of the
25 '893 patent when the term "void-free" is used, it's

1 referring to the contact hole being completely
2 filled to the top of the hole, correct?

3 A. We are talking about it being filled,
4 too. Yeah, this was -- I don't understand. What
5 is the question?

6 Q. Sure.

7 In the context of the '893 patent --

8 A. Okay.

9 Q. -- void-free means that the contact hole
10 is filled to the top of the hole, correct?

11 A. Void-free means that there is no space --
12 there's no area inside the contact that is not
13 filled with, let's say, the tungsten material.

14 Q. Because if there were a void and you --
15 well, strike that.

16 If -- if the hole were not completely
17 filled, the formation of the second layer would
18 leave a void, correct?

19 A. It could. And -- and it's not only issue
20 is when you have a void that -- or say when you
21 have a void, you can have outgassing later or can
22 create cracks in the material later, and it
23 wouldn't pass reliability tests. Or if it would
24 pass, it would fail in the field when you have a
25 environment of steam or high temperature or some of

1 this. So this way you want to avoid having a void.

2 Q. And -- and the way to do that is to fill
3 the hole completely to the top?

4 A. All the way through. I mean, the side
5 fully filled and not just the top cover.

6 Q. You should take a look at figure 5 of the
7 '893 patent, please.

8 In figure 5, the second conductive layer
9 32 is deposited on the first conductive layer 30,
10 correct?

11 A. Yes. You -- you put the second
12 conductive, yeah.

13 Q. And the second conductive layer 32 is
14 formed in a second CVD chamber, correct?

15 A. Yeah. It's the way describing column 3,
16 line 14, all the way to 34.

17 Q. And the second conductive layer 32 can be
18 tungsten, correct?

19 A. Yes, it's could be tungsten.

20 Q. And the tungsten layer 32 is formed at a
21 higher temperature than the first tungsten layer
22 30, correct?

23 A. Yeah. It's mentioned the -- the
24 temperature in column 3, line 25, to temperature
25 for this -- this second tungsten is between 450 to

1 490 centimeter. While on the top of page -- of
2 column 3 at line 4, it said the temperature for the
3 first layer in range of 400 to 450. Column 3, line
4 4.

5 Q. The second tungsten layer 32 is formed at
6 a lower gas flow rate than the first tungsten layer
7 30, correct?

8 A. Yes. Like it's in column 3, line 27,
9 26/27, it is mentioned a flow of the -- tungsten
10 flow rate of 15 to 60 sccm, one for the first
11 layer. In column 3, line 5 and 6, it described the
12 first layer being formed as a glass flow of about
13 50 to 90 sccm.

14 Q. The second tungsten layer 32 has the
15 property of low stress, correct?

16 A. Yes.

17 Q. The second tungsten layer 32 is not used
18 to fill the contact hole, correct?

19 A. Yeah, because you have the surface
20 completely filled in the first step and void-free
21 and good step coverage look like in line 13 for the
22 first film. And then you put the top layer and the
23 second layer on top of it.

24 Q. Now, in the '893 patent, the first and
25 second tungsten layers are formed in separate DVD

1 chambers, correct?

2 A. CVD chamber, yeah.

3 Q. Correct.

4 A. Yeah, correct. I thought you said "DVD"
5 chamber --

6 Q. Oh.

7 A. -- so that's why I said "CVD" chamber.
8 Maybe I did call it -- but, anyway, it's CVD
9 chamber, yeah.

10 Q. And for the formation of the first
11 tungsten layer 30, the temperature of the process
12 is controlled in a fixed temperature range of 400
13 to 450 degrees Celsius, correct?

14 A. Yes.

15 Q. And for that first tungsten layer 30, the
16 gas flow is controlled at a fixed flow rate in the
17 range of 50 to 90 sccm, correct?

18 A. Yeah.

19 Q. For the first tungsten layer, the
20 deposition time is controlled at a particular fixed
21 time range of about 10 to 100 seconds; is that
22 correct?

23 A. Yes. It's -- it's describing was the
24 flow rate and the timing, column 3, line 5 through
25 7 or so.

1 Q. And the thickness of the first tungsten
2 layer 30 is approximately 500 to 900 angstroms,
3 correct?

4 A. Yes.

5 Q. And the first tungsten layer 30 is a high
6 stress layer, according to the '893 patent,
7 correct?

8 A. Yes.

9 Q. Then the second tungsten layer 32 is
10 formed at a temperature in the range of 450 to
11 490 degrees Celsius, correct?

12 A. Yes.

13 Q. And in the second tungsten layer 32, the
14 gas flow is controlled at a particular flow rate in
15 the range of 50 to 60 sccm, correct?

16 A. Yes, they are describing column 3,
17 line 25 to 28.

18 Q. For the second tungsten layer 32, the
19 deposition time is controlled in a range of about
20 10 to 100 seconds, correct?

21 A. Yes.

22 Q. And the second tungsten layer 32 has the
23 thickness of around to 300 to 8,000 angstroms,
24 correct?

25 A. Yeah, it's like describing column 3,

1 line 26 to 29.

2 Q. And the first tungsten layer is described
3 in the '893 patent as being low stress, correct?

4 MR. CHEN: Objection to form.

5 THE DEPONENT: Yes, it says that the
6 first is as low stress there.

7 Q. (By Mr. Colaianni) The '893 patent does
8 not disclose what constitutes high stress versus
9 low stress; is that correct?

10 A. Correct.

11 MR. CHEN: Objection to form.

12 Q. (By Mr. Colaianni) The '893 patent
13 doesn't describe a way to measure the stress of
14 those layers, does it?

15 A. Right. We know not to -- that you
16 measure the stress. I mean, it -- it just
17 basically says that -- that the stress -- it
18 compare the stress of the two layers. I mean, it
19 say one is higher stress and one is the lower
20 stress.

21 Q. Was it well known to persons skilled in
22 the art at that time how to measure the stress
23 level of a layer?

24 A. I believe so. The -- the manufacturer of
25 the process equipment would tell them what to do.

1 Q. Are you aware of particular ways to
2 measure the stress of layers, such as the first and
3 second tungsten layers described in the '893
4 patent?

5 A. That you can use some optical way; that
6 by bending the wafer and seeing that they -- how
7 much -- or looking at the wafer that were coming
8 out and see how much they bend and -- because, you
9 see -- I mean, it -- the purpose of the -- or the
10 reason why they care about the stress, it says two
11 main reason.

12 One, that if you have too high stress,
13 the wafer basically could break, so -- so it's
14 very -- you don't need to be a very experienced
15 person that when the wafer come out and it's
16 broken, that you know the issue, and one of the
17 potential is likely to be the stress.

18 And so this would be the first most
19 simple, the most extreme case. But you can have
20 also the wafer bending, which means that when you
21 transport -- when the wafer gets -- moved between
22 one piece of equipment to another piece of
23 equipment, it wouldn't be able to move smoothly
24 and -- because you can think of it -- it's like --
25 the wafer, it look like a coaster, basically, that

1 you put something on around the coaster. And if
2 the coaster is not flat on the bottom and when you
3 move it from one piece equipment to another, it
4 wouldn't fit there or it wouldn't go smoothly or it
5 gets stuck in between and -- and so this is one
6 indication -- one indication that the stress is too
7 high in that step.

8 And the other indication would be that if
9 you have too high stress, the wafer would be bent.
10 But maybe it's not bent to the level that when you
11 are on this dedicate equipment, you move it from
12 one machine to another, you are able to do this.
13 But when you are doing the -- the step of the
14 masking where you do a photographic process, when
15 you shine light on the wafer and expose an area, if
16 some area bent -- if the edge it's like more lower
17 than the middle, then you wouldn't get -- you
18 wouldn't be able to have the wafer in focus, both
19 the center of the wafer and the edge of the wafer.

20 So this -- this would be another problem
21 that you run into. So these are the issues that
22 you will know what the stress is; that you have
23 stress problem.

24 Q. Would you use a test wafer to measure the
25 stress?

1 A. You can. But, see, you use initially
2 test wafer, but you need to have the full
3 structure -- see, the first test you can do on a
4 test wafer, but later you use wafer that would have
5 the full pattern of the dies, because in extreme
6 case of stress, you notice it even on a flat wafer.

7 But in -- in a low level of stress, which
8 it still could be problematic, you only notice it
9 is when you have all the structure, because it sees
10 that -- if you have a high-stress material and a
11 lot of it is along the edge of the wafer. And when
12 you have, let's say, near a lot of contact, a lot
13 of structure, it will make it bend more and --
14 versus if just -- if they are next to an empty
15 space. So this is why it's important to use also
16 patent wafer and -- so you start for sure with test
17 wafer, but then you have to use production.

18 Q. Are the techniques you just described
19 used to measure the stress across the whole wafer,
20 after the deposition of the tungsten films?

21 A. Yeah. You need the tungsten deposition
22 to see what stress you have.

23 Q. But would those techniques be used to
24 measure the stress across the entire wafer? Is
25 that what you're saying?

1 A. Well, you need to be able to know the
2 stress across the entire wafer because you -- your
3 process -- I mean, you manufacture a full wafer.
4 You cannot just -- the equipment is not set up --
5 the production equipment to make the semiconductor
6 is not set up to run with partial wafers.

7 Q. Are the techniques that you describe for
8 measuring the stress applicable to measure the
9 stress of the tungsten films, whether they were
10 formed in one chamber versus multiple chambers?

11 A. Well, the technique that I mentioned that
12 you can measure it in a -- in any kind of a
13 production because you see the outcome that -- in
14 subsequent steps, if the stress is too high and
15 you -- or the wafer is too bent and it doesn't fit
16 in the next machine, so you can see it in full
17 values processes.

18 Q. And -- and those techniques for measuring
19 stress would be applicable regardless of whether
20 the two tungsten films were formed in the same
21 chamber or different chambers, correct?

22 A. You can measure them independently of the
23 way you make the film.

24 Q. Okay. Going back to the discussion that
25 we had about the formation of the first and second

1 tungsten films --

2 A. Uh-huh.

3 Q. -- the '893 patent does not appear to
4 provide any examples with specific process
5 parameters for these two layers, other than the --
6 the ranges we discussed earlier, correct?

7 MR. CHEN: Objection to form.

8 THE DEPONENT: Well, it shows the range
9 that you can use to make the first layer, so -- and
10 it was a range for producing the second layers. So
11 it provide this example for spectrum of a way of
12 making it.

13 Q. (By Mr. Colaianni) Right.

14 Other than those ranges, there's no
15 examples with specific process parameters forming
16 those two layers, though, correct?

17 MR. CHEN: Objection to form.

18 THE DEPONENT: I mean, there is values
19 that are in the claims for the values, layer
20 thicknesses and so on. But in a specification,
21 it's going just -- the range for forming the first
22 layer and the range of forming the second layer.

23 Q. (By Mr. Colaianni) In order to determine
24 the relationship between those process parameters
25 and the wafer stress level, could one skilled in

1 the art use test wafers to measure the stress level
2 across different conditions using known techniques?

3 MR. CHEN: Objection to form.

4 THE DEPONENT: You can use -- you can
5 start with test wafer to look at this parameter and
6 see if the wafer is too bold and if it bend and --
7 and if you are not able to get it in -- well, for
8 getting in focus, you probably don't need a patent
9 wafer. So you can start with it, but for sure you
10 need to look at the fully processed wafer -- fully
11 production wafer and evaluate it carefully, whether
12 it bend or bows or if you can get in focus
13 everywhere because the die from one end of the
14 wafer to the center of the wafer, the focal -- I
15 mean bottom left -- bottom -- I mean top right -- I
16 mean top and left and right. So you want to see
17 you stay in focus everywhere. So you need to look
18 at a fully production wafer. You cannot just use
19 test wafer.

20 Q. (By Mr. Colaianni) Can the process
21 parameters in the value ranges provided in the '893
22 patent for forming the -- the two tungsten layers
23 be used for depositing the layers in a single
24 chamber?

25 A. Well, they tell me that they -- you can

1 use this range of parameter to deposit them in a --
 2 in a tungsten deposition chamber and you can use --
 3 I mean, you can use it at different time in a
 4 different circumstance to deposit the first layer
 5 and then deposit the second layer.

6 Q. And -- and you're referring to depositing
 7 the two layers in a single chamber?

8 MR. CHEN: Objection to form.

9 THE DEPONENT: Well, I'm saying that you
 10 have to do a separate deposition, and one of them
 11 would be depositing the -- the first layer and then
 12 under different circumstance you deposit the second
 13 layer.

14 Q. (By Mr. Colaianni) In the same chamber?

15 A. Yeah, after -- in the same chamber in
 16 different circumstance.

17 Q. What different circumstances are you
 18 referring to?

19 A. So you see that when a -- when you are
 20 trying to do a deposition of these two different
 21 layers, you have -- you have one set of parameters
 22 that is used to do the first deposition, like the
 23 one that is in -- I mean, column 2, starting from
 24 60 -- line 60 to column 3, line 13.

25 So this is the condition that you

1 deposited the first layers. And you would --
2 deposited them. And then in a different set of
3 parameters, you can deposit it in the -- in the
4 chamber using the range that is defined in
5 column 3, line 14 to 34, 35.

6 Q. So the parameter ranges for the second
7 tungsten deposition disclosed in the '893 patent
8 could be used for depositing the second tungsten
9 layer in a single chamber?

10 MR. CHEN: Objection to form.

11 THE DEPONENT: Well, you see that the --
12 the ranges are different and the temperature are
13 different. So you need to have the chamber
14 controlled and having the right flow -- I mean the
15 equipment to pass the gases through and the
16 temperature to be controlled accurately.

17 And they are different, so you need to
18 make sure that you have the right control and the
19 right temperature and the right flow accomplish. I
20 mean, you need to make sure you accomplish both for
21 one set and then for the other set of conditions.

22 You see, you also need to make sure that
23 the -- they are calibrated for the ranges that we
24 mentioned, and you have to worry about the amount
25 of particulate that you create in one process

1 versus the other.

2 So you see, for example, the second
3 chamber or the second deposition, it's a low flow.
4 You don't need to clean it. And so often is the
5 first one, so you have to -- and the process varies
6 functional of however clean the chamber is, so you
7 have to -- so it's not so straightforward.

8 Q. (By Mr. Colaianni) But the -- the
9 calibration of the chamber and the adjustment of
10 the conditions would be something within the realm
11 of a person skilled in the art, correct?

12 A. Well, theoretically, he can know about
13 them, but he have to -- he has to be aware that he
14 should make sure that they are calibrated and --
15 so, see, when -- when you calibrate it -- a chamber
16 to reach a certain temperature or to stay at this
17 temperature stable, you -- it doesn't stay in the
18 temperature forever. You have to verify that the
19 calibration is still -- stays the same after the --
20 I mean the fifth load, the third load -- so the
21 frequency, how often you have to calibrate and so
22 on vary and depend on the equipment and the
23 temperature. So you have a different parameter --
24 a different level of what you need to control for
25 calibration at the first temperature than the

1 second.

2 And so on theoretical basis maybe you
3 will know, but he wouldn't -- cognizant of it and
4 to make sure that both stays within the range -- I
5 mean the -- the calibration. Because, see, you can
6 have one of them. The calibration have to be, just
7 for sake of discussion, every 30 load, another one
8 every 60 loads.

9 So a person of skill -- ordinary skill in
10 the art wouldn't know that -- unless somebody tell
11 him -- that for the other process that you don't
12 need to calibrate it as often. He would know one
13 parameter and could assume automatically it apply
14 for the other one. So it wouldn't be something
15 that would be obvious.

16 Q. But a person skilled in the art at -- at
17 the time of this patent knew how to form both the
18 first and second tungsten layers in a single
19 chamber, right?

20 A. Yeah. I mean, somebody give him the
21 conditions and so on, he would know how to do it,
22 yeah.

23 Q. Let's take a look at your declaration.
24 This was marked as Exhibit 3, I believe, to the
25 deposition today.

1 A. Yeah.

2 Q. And Exhibit 3 contains all of your
3 opinions relating to the -- the 466 IPR, correct?

4 A. Correct.

5 Q. And in connection with your opinions, you
6 do not dispute the claim constructions proposed by
7 Samsung in its petition, correct?

8 A. Can you show me what you are referring
9 to? Which page are you on?

10 Q. Well -- well, Samsung had proposed some
11 constructions to certain claim language.

12 Do you recall that?

13 A. Yes.

14 Q. And you have not offered any contrary
15 opinion relating to the interpretation of that
16 claim language, correct?

17 A. Yeah. It's -- it's -- basically, it's
18 paragraph 41 through 44, is the one that --

19 Q. Yes. That's what I was looking for.

20 A. Yeah. Uh-huh.

21 Q. And you haven't applied any -- any
22 constructions to any of the claim language that is
23 not set forth in the declaration, correct?

24 MR. CHEN: Objection to form.

25 THE DEPONENT: Yeah. I mean, I just used

1 the -- this is the level of what assumption I
2 propose and for this specific parameter that is
3 mentioned in claim 41 through 44 and...

4 Q. (By Mr. Colaianni) But you haven't
5 applied any -- any interpretations to any of the
6 other claim language that's not specifically set
7 forth in your declaration, correct?

8 MR. CHEN: Objection to form.

9 THE DEPONENT: Can -- can you repeat the
10 question.

11 Q. (By Mr. Colaianni) Sure.

12 If -- at any -- any understanding of the
13 claim language that you applied in your analysis is
14 set forth in your declaration, correct?

15 A. Yes.

16 Q. Okay. There -- there's no meaning to the
17 claim language that you -- that you applied, but
18 that you didn't include in your declaration?

19 A. Correct.

20 MR. COLAIANNI: Okay. Let's -- let's
21 mark another exhibit. This is the Miyazaki prior
22 art. It's the U.S. Patent No. 5,843,840, and
23 it's -- was produced as SAMSUNG-1005. And it will
24 be Deposition Exhibit 4.

25 //

1 (Exhibit 4 was marked for identification
2 by the court reporter and is attached hereto.)

3 Q. (By Mr. Colaianni) Do you recognize
4 Exhibit 4?

5 A. Yeah. It look like the '840 patent.

6 Q. And you studied the Miyazaki prior art
7 reference in connection with forming your opinions,
8 correct?

9 A. Yes.

10 Q. So if we look at column 1 of Miyazaki
11 reference in the background section, Miyazaki
12 discloses that as the diameter of the contact holes
13 become small with advanced microminiaturization, a
14 void would occur in the contact hole if a process
15 has poor step coverage, correct?

16 A. Which line you are referring to?

17 Q. I am looking at approximately line 50
18 through 55.

19 A. Let me read it.

20 Okay.

21 Q. Do you agree that Miyazaki discloses that
22 as the diameter of the contact hole becomes small
23 with advanced microminiaturization, a void would
24 occur on the contact hole if the process has poor
25 step coverage?

1 A. Yeah, it's one of the circumstances that
2 you have a void.

3 Q. Miyazaki describes a fine contact hole as
4 a contact hole having a diameter not greater than
5 .5 microns, correct?

6 A. I believe so, yeah.

7 Q. You -- you can focus --

8 A. Yeah. Yeah, it's in --

9 Q. Okay.

10 A. I found it in column 2, line 53.

11 Q. Correct.

12 Miyazaki discloses that CVD can be used
13 to achieve an excellent step coverage in order to
14 prevent void generation, correct?

15 A. Yes.

16 Q. But according to the Miyazaki reference,
17 after depositing a tungsten having an excellent
18 step coverage using CVD, an internal stress of the
19 metal film can cause the wafer to -- to bend,
20 correct?

21 A. Uh-huh. Correct.

22 Q. And this wafer bending would lead to
23 what's described as "vacuum suction failure"?

24 A. Uh-huh.

25 Q. Is that correct?

1 A. Yeah.

2 Q. Can you turn to figure 2A of the Miyazaki
3 reference, please.

4 A. Okay.

5 Q. Figure 2A illustrates a silicon oxide
6 film 12 formed on a silicon substrate 11, correct?

7 A. Yes.

8 Q. And according to Miyazaki, a desired
9 circuit has been formed on the silicon
10 substrate 11, correct?

11 A. I mean, yes. He talking general about
12 forming a circuit area.

13 Q. The -- the circuit is not shown --

14 A. But later is formed, yeah.

15 Q. I'm sorry?

16 A. Yeah, later is formed the circuit, right.

17 Q. Right.

18 The circuit is not shown in figure A,
19 but -- but you agree that it's -- it's there,
20 correct?

21 A. Yeah. Yeah, I mean -- yes.

22 Q. Figure -- figure 2A shows that a contact
23 hole 13 is formed by selectively etching the
24 silicon oxide film 12, correct?

25 A. Yeah. Yeah.

1 Q. And the purpose of the contact hole 13 is
2 to electrically connect the circuit formed on the
3 substrate 11 to another conductive region somewhere
4 else, correct?

5 A. Yeah, to this conductive layer that would
6 be formed above it, yeah.

7 Q. So by selectively etching the silicon
8 oxide film 12, a part of the circuit on the silicon
9 substrate 11 is exposed, correct?

10 A. It looks like this, yeah. It doesn't
11 describe it in full detail. But potentially, yeah.

12 Q. And the exposed region of the circuit
13 would be conductive, right?

14 A. Probably.

15 Q. That's the whole reason for the contact
16 hole, right, is to --

17 A. Yeah, it -- it doesn't -- it's not
18 required there, but it's potentially, yeah.

19 Q. The -- the contact hole is formed in
20 order to connect the conductive portion of the
21 circuit to something else that's conductive,
22 correct?

23 A. I mean, it could form a capacitor plate.
24 I mean, that -- he doesn't really describe it,
25 but...

1 Q. But you would expect the exposed -- the
2 region of the circuit that's being connected by the
3 contact hole to be conductive, correct?

4 A. Often they are -- I mean, they would be
5 conductive structure, yeah.

6 Q. And -- and figure 2A also shows a
7 refractory metal layer 14 deposited on the contact
8 hole, correct?

9 A. Yes.

10 Q. What -- what purpose does the refrac- --
11 refractory metal layer serve?

12 A. To -- for adhe- -- adhesion for a
13 subsequent layers that you put inside this all and
14 to have a good connection to the layer that -- in
15 this case, the silicon substrate 11.

16 Q. Okay. Looking at figure 2B, Miyazaki
17 discloses that tungsten film 15 that is formed by a
18 CVD process, correct?

19 A. Yes.

20 Q. Is the tungsten film 15 formed by a
21 blanket tungsten CVD process?

22 A. It's formed by -- it's described in
23 column 2, line 6 through 11. It's formed by CVD
24 using tungsten hexafluoride and hydrogen. And --
25 and then it says the condition is it's -- mentioned

1 the flow rate of 50 to 100 sccm and deposition
2 temperature of 400 to 460.

3 Q. Would you consider that to be a blanket
4 tungsten CVD process?

5 A. Yeah, it's a CVD process that deposit a
6 layer of tungsten all the way across the wafer.
7 This is a condition described in -- in column 2,
8 line 6 through 11.

9 Q. Miyazaki describes the tungsten film 15
10 as having excellent step coverage, correct?

11 A. Yes. It is -- yup.

12 Q. Miyazaki discloses that a blanket
13 tungsten CVD process is used to fill a fine contact
14 hole having a diameter not greater than .5 microns
15 without void, correct?

16 MR. CHEN: Objection to form.

17 THE DEPONENT: Well, it says that you
18 fill the contact hole in -- that you use film 15 --
19 see, it's for -- for the figure 2B, I think he's --
20 the only time he's talking about -- let me
21 double-check -- is it in the column 2, line 6
22 through 11, he describes creating this
23 tungsten film and -- and he describes how the film
24 is. But I don't think he mentioned, so he doesn't
25 have a void, this specific film. In this point,

1 he's talking about -- specifically about this
2 figure 2B.

3 Q. (By Mr. Colaianni) Well, if you take a
4 look at column 2 of paragraph beginning at line 21,
5 there's a reference there to a blanket CVD process
6 used to fill the fine contact hole having a
7 diameter not greater than .5 microns without void,
8 correct?

9 A. Yes.

10 Q. And the blanket CVD process is the
11 tungsten CVD process of figure 2B, correct?

12 A. Yes. It's -- it's mentioned there in
13 the -- in this column 2, line 21 and 22.

14 MR. COLAIANNI: Okay. We need to change
15 the tape here, so if you want to take a quick
16 break.

17 THE DEPONENT: Sure.

18 MR. CHEN: Sure.

19 (Discussion off the stenographic record.)

20 THE VIDEOGRAPHER: The time is 11:34 a.m.
21 and this concludes DVD No. 1 to the videotaped
22 deposition of Ron Maltiel. The time -- we are off
23 the record at 11:34.

24 (Recess taken.)

25 THE VIDEOGRAPHER: This marks the

1 beginning to DVD No. 1 in Volume No. 1 -- or I'm
2 sorry -- this is DVD No. 2 in Volume No. 1 to the
3 deposition of Ron Maltiel. The time is 11:43 a.m.
4 and we are on the record.

5 Q. (By Mr. Colaianni) In column 2 of the
6 Miyazaki reference, around lines 37 through 40,
7 Miyazaki discloses that in order to lower the
8 stress of a tungsten film, it is the general
9 practice to form a film deposition under a supply
10 rate controlling condition by lowering the flow
11 rate or by elevating the deposition temperature or
12 by doing both.

13 Do you see that?

14 A. It doesn't say "or by doing both" in
15 this -- you -- you're talking which lines, 37 to
16 41?

17 Q. Yes.

18 A. Yeah. It doesn't mention the word "both"
19 that way.

20 Q. Well, he says "and/or," doesn't he?

21 A. Yeah, he say "and/or."

22 Q. So it -- it's one or the other -- or the
23 other or both, correct?

24 A. Yes.

25 Q. Do you have an understanding of the term

1 "supply rate controlling conditions" in this
2 context?

3 A. Yes. It means by the -- that the
4 reaction is controlled by the -- you can think of
5 it of the amount of the molecule available for the
6 reaction. It's what you supply. You supply the
7 tungsten fluoride. So you control -- you don't
8 flood the chamber with a huge of amount of tungsten
9 fluoride.

10 Q. In -- in a supply rate controlling
11 condition, is the supply of the reactants that
12 control the tungsten deposition in the contact
13 hole? Is that correct?

14 A. Can you repeat the question.

15 Q. Sure.

16 In a supply rate controlling condition --

17 A. Uh-huh.

18 Q. -- is the supply of the reactants that
19 control the tungsten deposition in the contact
20 hole? Correct?

21 A. Yes. Yeah.

22 Q. Okay. Looking at figure 3B of the
23 Miyazaki reference, Miyazaki discloses that when
24 you deposit a tungsten film under the supply rate
25 controlling condition, the internal stress of the

1 tungsten is low, but a void is formed in the
2 contact hole due to the poor step coverage,
3 correct?

4 A. Yes. I mean, 3B show a void when you
5 form a layer 16.

6 Q. And the void is not desirable because the
7 reliability of the wiring conductor would be
8 affected, correct?

9 A. Yes, it's the reliability and the --
10 yeah.

11 Q. So going back to figure 2B, Miyazaki
12 discloses that a tungsten film having an excellent
13 step coverage to fill the contact hole without void
14 is known in the prior art, correct?

15 A. It's -- well, he describe in figure 2B
16 that you form a tungsten film 15 by using tungsten
17 fluoride and hydrogen and you get an excellent step
18 coverage.

19 And 3B is talking about -- he doesn't
20 specify the condition that you form there as 3B, I
21 think. Let me just see a minute.

22 Your produce film is low stress by --
23 when you run the supply rate control condition and
24 you get less good step coverage and you also form
25 void 18.

1 Q. Right.

2 With respect to figure 2B, Miyazaki
3 discloses that a tungsten film having excellent
4 step coverage fills a contact hole without void,
5 correct?

6 A. Wait a minute. Where does it say that it
7 fill without a void? It should -- I mean, it show
8 that it has an excellent step coverage.

9 Q. There -- there's no void in the contact
10 hole shown in figure 2B, correct?

11 A. I mean, it's hard to know. And it is
12 just representative. For sure, in 3B show a very
13 large void. In 2B, it says it's an excellent step
14 coverage, but it doesn't mention whether he has a
15 void or not, I believe.

16 Q. Well, with respect to -- to figure -- I'm
17 sorry.

18 With respect to column 2, lines 21
19 through 25 of Miyazaki, there's a disclosure of
20 forming a contact hole -- I'm sorry. Strike that.

21 With respect to column 2, lines 21
22 through 25 of Miyazaki, there's a disclosure of
23 tungsten film filling a contact hole without void,
24 correct, in the prior art?

25 A. Yes. Yes. Yeah.

1 Q. And -- and that's referring to the -- the
2 embodiment of figure 2B, correct?

3 A. Yeah, it's -- it's referring to the prior
4 example.

5 Q. And Miyazaki discloses that the tungsten
6 film having an excellent step coverage is formed
7 under a reaction rate controlling condition,
8 correct?

9 A. Well, he doesn't describe it -- he
10 describe it for layer 16. He describes 3A and 3B,
11 I guess. But for figure 2B and 2 -- 2B, he doesn't
12 mention that the -- with a reaction. Because, see,
13 he's talking in 2 about reaction rate controlling,
14 while in 3 he's talking a supply rate controlling.

15 Q. Let -- let's -- right. So let's -- let's
16 see if we can focus on figure 2B.

17 In column 2, lines 6 through 10 --

18 A. Uh-huh.

19 Q. -- figure 2B is described as a tungsten
20 film having an excellent step coverage formed under
21 reaction rate controlling condition, correct?

22 A. Yes.

23 Q. And how is the reaction rate controlling
24 condition different from a supply rate controlling
25 condition?

1 A. Because, see, the reaction rate, it's
2 tied more to what happened at the surface there or
3 inside the chamber -- not purely on the surface,
4 inside the chamber -- so that when you depend on
5 how the molecule produce -- during the reaction,
6 produces the tungsten film.

7 While in the supply rate, you -- you
8 control more how many molecules are available to do
9 the reaction. So you control when you enter the
10 chamber.

11 Q. So --

12 A. When they entered the chamber, the
13 molecules.

14 Q. Is the reaction rate controlling
15 condition dependent on the supply rate of the
16 reactants to the surface?

17 A. Yeah, but they are not the one that are
18 limiting it. Because, see, it depends on how much
19 surface is available, for example, for the
20 reaction.

21 Q. So in the reaction rate controlling
22 condition, the supply rate of the reactants is not
23 controlling the deposition rate of the tungsten
24 film, correct?

25 A. For the specifics circumstance they are

1 doing, yeah.

2 Q. You say "the specific circumstances they
3 are doing."

4 A. Yeah, doing.

5 Q. Are you referring to the Miyazaki
6 reference or something different?

7 A. No, no, to the Miyazaki reference.

8 Q. Now, let's talk about the first
9 embodiment disclosed in the Miyazaki reference,
10 which is describing in connection with figures 4A
11 through 4D.

12 A. Okay.

13 Q. If you look at figure 4A, figure 4A shows
14 that a contact hole was formed on a silicon
15 substrate 1 by patterning and etching silicon oxide
16 film 2, correct?

17 A. Can you repeat it. Sorry.

18 Q. Sure.

19 Figure 4A of Miyazaki shows that a
20 contact hole is formed on a substrate 1 by
21 patterning a silicon oxide film 2, correct?

22 A. Yes.

23 Q. Figure 4 also shows an adhesion
24 layer 3 formed on the contact hole, correct?

25 A. Yes.

1 Q. The adhesion layer 3 is formed by
2 depositing a titanium film, a titanium nitrate
3 film, correct?

4 A. I believe so.

5 Q. It's described at column 5, at
6 approximately line 54, if you want to check that.

7 A. Yes. Yes. Correct.

8 Q. The thickness of the titanium film was on
9 the order of 500 to 2,000 angstroms, correct?

10 A. Yes.

11 Q. The thickness of the titanium nitrate
12 film is also on the order of 500 to
13 2,000 angstroms, correct?

14 A. Correct.

15 Q. And figure 4A also shows a tungsten
16 film 4 deposited on the adhesion layer 3, correct?

17 A. Correct.

18 Q. And the adhesion layer 3 is deposited to
19 help the tungsten film 4 adhere to the contact
20 hole, correct?

21 A. Yes.

22 Q. According to the Miyazaki reference, the
23 tungsten film 4 is formed under a reaction rate
24 controlling condition, correct?

25 A. Where does it say it's under reaction

1 rate controlling --

2 Q. You can consult column 5, line 66, to the
3 top of column 6, line 3.

4 A. He's talking about figure -- I guess
5 figure 5. No -- well, figure 5 show a range of
6 condition and temperature. It shows the
7 temperature and range of flow rate. Okay.

8 Q. But the tungsten film 4 is disclosed by
9 Miyazaki as being formed under reaction rate
10 controlling conditions so the film can have
11 excellent step coverage, correct?

12 A. I mean, the way it's written, that he
13 described initially how you form layer 4. And then
14 he described figure 5 and he say that if --
15 basically, if you look at column 5, line 66, if the
16 tungsten is deposited under condition of forming --
17 having access, namely, under rate control, the
18 stress.

19 So describes it -- if you are -- he
20 describe it as figure 5; that you want to have
21 certain stress and good step coverage. You would
22 want to, right, control reaction.

23 Q. Figure 4A of Miyazaki states that the
24 tungsten film is formed without void, correct?

25 A. Yes. When you deposit this film, it has

1 no void. It's in column 5, line 59 and 60.

2 Q. Correct.

3 And -- and according to Miyazaki, if the
4 tungsten film 4 is formed under a reaction rate
5 controlling condition, the contact hole was
6 filled -- is filled without the void, correct?

7 A. Well -- I mean, it -- when he talks about
8 the reactant -- about reaction rate control
9 condition, he's talking about figure 5 when he
10 says -- if you have a reaction rate controlling
11 condition and you will get a good -- a step
12 coverage for the various ranges described in
13 figure 5.

14 Q. And -- and under the reaction rate
15 controlling condition, you will fill the hole with
16 the tungsten film having no void, correct?

17 A. He doesn't talk about void. He's talking
18 about you get a good step coverage.

19 Q. Well, but he says later at column 6,
20 approximately lines 34 through 37, that the
21 tungsten film will fill the contact hole having no
22 void, correct?

23 A. Yeah, but he doesn't say for -- for
24 which -- if he's talking about figure 4B or just
25 the -- the condition of figure 5, you don't have

1 the void.

2 Q. Well, he's talking here about the -- the
3 first embodiment, correct?

4 A. The section is about first embodiment,
5 the general section.

6 Q. Correct.

7 And the first embodiment is described in
8 connection with figures 4A through 4D, correct?

9 A. But in the middle of it, he's also
10 discussing figure 5, and figure 5 doesn't apply
11 purely to embodiment -- the first embodiment.

12 Q. You believe figure 5 does not apply to
13 the first embodiment?

14 A. He doesn't -- because, see, first
15 embodiment yet is an implementation. In figure 5,
16 he doesn't say whether he use that implementation
17 or not.

18 Q. In -- in figure 5, there's reference --
19 well, strike that.

20 In the text describing figure 5, there's
21 reference to the tungsten film that's being
22 deposited, and that reference refers to the
23 tungsten film that's discussed in connection with
24 the first embodiment, correct?

25 A. It's not clear. It's -- it could be, but

1 it's not -- see, the figure, he put the word "if"
2 in.

3 Q. Where -- just for the record, where are
4 you reading?

5 A. That in column 5, line 64, he start
6 describing what -- in figure 5. Then if you -- two
7 line down to line 66, he mention if the film is --
8 the tungsten film is deposited under a condition of
9 forming an excellent step coverage; namely, under a
10 reaction rate. Then it mention the stress.

11 Q. Right.

12 And the -- that sentence that says "If
13 the tungsten film is deposited under a condition
14 of" -- "of forming a film," it's referring to the
15 tungsten film that's discussed earlier in that same
16 paragraph, correct?

17 A. Well, he says that he doesn't -- he
18 doesn't limit it to it. He said you have to ensure
19 that you have a rate con- -- control -- reaction
20 rate controlling condition, and then you get this
21 excellent step coverage and so on. But he doesn't
22 purely associate it with embodiment 1 only or
23 he's -- he's just saying if you have a rate -- he's
24 talking general about rate controlling reaction.

25 Q. But certainly it's reasonable to read

1 this reference to the tungsten film in connection
2 with figure 5 as referring to the tungsten film 4
3 that is disclosed just a few lines earlier,
4 correct?

5 MR. CHEN: Objection to form.

6 THE DEPONENT: I mean, it could be it's
7 related to it, but 5 is -- cover other
8 circumstance.

9 Q. (By Mr. Colaianni) Okay. You would
10 agree that Miyazaki does disclose the tungsten
11 film 4 filling the contact hole without void, as
12 shown in figure 4C, correct?

13 A. In -- he described the tungsten film 4
14 filling the contact hole is now void. It's in
15 column 5, line 60.

16 Q. Let's talk about --

17 A. He's talking about 4A, actually. He was
18 talking the 4A in this paragraph.

19 So you see it's -- this paragraph start
20 on line 49 that's shown in paragraph 4A. And he
21 describes how you create this film and you end it
22 in line 60.

23 Q. The -- the contact hole shown in -- in
24 the first embodiment of Miyazaki is completely
25 filled without void, correct?

1 A. Yeah. I mean, the -- it describe -- I
2 mean, it's shown in -- it's -- basically, this
3 paragraphs we have just been talking in column 5,
4 line 49 through 60, you mention about filling the
5 contact hole is now void.

6 Q. Let's talk about some of the other
7 embodiments of Miyazaki.

8 A. Uh-huh.

9 Q. With regards to figures 8A through 8D,
10 Miyazaki discloses the third through the sixth
11 embodiments, correct?

12 MR. CHEN: Objection to form.

13 THE DEPONENT: So I see 8A -- so say it
14 again. That 8A to 8D is it -- and it's -- for the
15 certain embodiment, it's written on page --
16 column 7, line 25 through -- I mean 25, 26 -- it
17 says that certain embodiment is referenced to 8A
18 from 8 -- with reference to figures 8A to 8D.

19 Q. (By Mr. Colaianni) And figures 8A
20 through 8D correspond to the third, fourth, fifth
21 and sixth embodiments of the Miyazaki reference,
22 correct?

23 A. Right. So embodiments served like in
24 column 7, line 25 through 26. The first embodiment
25 is in -- it's in column 8, line 15 through 16. It

1 says also that the first embodiment of the present
2 invention will be described with reference to
3 figure 8A to 8D. And the fifth embodiment, it's
4 down in the same page in column 8, line 47. The
5 fifth embodiment described first is shown in 8A.
6 And then continue with 8C later in column 8,
7 line 56, or for sure it's figure 8C. It's continue
8 talking about the fifth embodiment.

9 Q. In -- in column 5 of Miyazaki reference,
10 around lines 15 through 20, where it's describing
11 the figures, it says that figures 8A through 8D
12 correspond to the third through sixth embodiments,
13 correct?

14 A. Yes.

15 Q. Okay. Figure 8A shows a contact hole
16 formed on a silicon substrate 11 by etching a
17 silicon oxide layer 12, correct?

18 A. Yes.

19 Q. And although it's not shown in figure 8A,
20 Miyazaki discloses that a circuit has been formed
21 on the silicon substrate 11, correct?

22 A. Yeah, likely, probably there is a silicon
23 substrate.

24 Q. And -- and as we discussed before, a
25 conductive portion of the circuit would be exposed

1 by the contact hole formation, correct?

2 A. Typically, yes. Yeah.

3 Q. Now, according to the Miyazaki reference,
4 the contact hole 13 can have a diameter of
5 .5 microns, correct?

6 A. Yes, I believe he mentioned .5 microns.

7 Q. What thickness of film would be required
8 to completely fill a contact hole having a diameter
9 of .5 microns?

10 A. You need the thickness greater than -- I
11 mean the -- the -- more than half of the width of
12 the opening because these are narrow opening and
13 you have many, many, in the millions, of this
14 contact holes, because each die -- and you have
15 hundreds of dies in each wafer -- and you need to
16 have enough molecules to be able to go into and
17 fill up each of these hole, because it is much
18 easier to deposit in the planar surface in these
19 holes.

20 Q. So you say more than half of the -- of
21 the diameter of the hole?

22 A. More than half of the diameter of the
23 hole.

24 Q. Okay. So if you look at figure 8B, there
25 is a refractory metal layer 14 deposited inside the

1 contact hole, correct?

2 A. Yes.

3 Q. You don't take account of the refractory
4 metal layer in your declaration, correct?

5 MR. CHEN: Objection to form.

6 THE DEPONENT: I don't mention it. I
7 mean, I don't -- I don't specifically cite to it in
8 my declaration.

9 Q. (By Mr. Colaianni) The refractory metal
10 layer 14 is formed by depositing a titanium film
11 and a titanium nitride film, correct?

12 A. Yeah.

13 Q. And the refractory metal layer 14 acts as
14 an adhesion layer, correct?

15 A. Correct.

16 Q. The refractory metal layer would have a
17 certain thickness, correct?

18 A. Yes.

19 Q. The thickness of the refractory metal
20 layer 14 would be similar to the thickness of the
21 adhesion layer 3 in -- in figure 4, correct?

22 MR. CHEN: Objection to form.

23 THE DEPONENT: I mean, you cannot just --
24 I mean, it's -- you cannot say that -- I mean,
25 because one is independent from the other.

1 Q. (By Mr. Colaianni) Well, both the
2 refractory metal layer and the adhesion layer are
3 formed from titanium film and titanium nitride
4 film, correct?

5 A. Yes.

6 Q. And they both serve the purpose of
7 adhesion, correct?

8 A. Yeah, but it's different circumstance.
9 It cannot just assume that one would apply for the
10 other.

11 Q. You -- you -- you would not expect them
12 to have similar thicknesses?

13 A. I mean, I would expect them to have range
14 of thick- -- thicknesses, but it depend on the
15 specific example what thicknesses you would need.

16 Q. And both the refractory metal layer and
17 the adhesion layer 3 are formed between tungsten
18 layer and the silicon oxide layer, correct?

19 A. Yes.

20 Q. And according to Miyazaki, the thickness
21 of the titanium film in the adhesion layer 3 is
22 between 500 and 2,000 angstroms, correct?

23 A. Yes.

24 Q. And Miyazaki discloses that the thickness
25 of the titanium nitride film in the adhesion

1 layer 3 is also on the order of 500 to
2 2,000 angstroms, correct?

3 A. Yes.

4 Q. You would -- you would expect the
5 refractory metal layer 14 to be at least as thick
6 as the adhesion layer 3, correct?

7 MR. CHEN: Objection to form.

8 THE DEPONENT: Not necessarily because --
9 I mean, it's -- you have also the issue of the
10 reflectivity of the tungsten that you deposit there
11 in the grain side. So it wouldn't necessarily
12 always be the same to specific example.

13 Q. (By Mr. Colaianni) But you would expect
14 them to be of similar thicknesses, since they are
15 serving the same role and are positioned in the
16 same location in the circuit, correct?

17 A. The -- I mean, it's then -- there are
18 differences between these examples and they -- so
19 they -- what you need from the layer and elicit
20 would be different for its thicknesses.

21 Q. But you wouldn't expect them to be vastly
22 different thicknesses, based on the context in
23 which they're described in the Miyazaki reference,
24 correct?

25 MR. CHEN: Objection to form.

1 THE DEPONENT: It could be vastly -- I
2 mean, it depend what you mean by different -- see
3 that the -- each word is a specific -- everything
4 is relative. So I mean, it -- I mean, I wouldn't
5 vastly -- I mean, it still it has to -- it has to
6 fit inside the hole, so it couldn't be thicker than
7 the hole size.

8 But -- but it has certain property. And
9 it's only done for adhesion, so it would be on the
10 same -- I mean, to be -- it has to be similar. It
11 would fit in the hole and you still have the space
12 to put the tungsten in. But this -- this is the
13 extreme end boundary condition for -- between these
14 two layers.

15 Q. (By Mr. Colaianni) You would agree that
16 the -- regardless of how thick the refractory metal
17 layer is, the film thickness required to fill the
18 empty space in the contact hole would be -- would
19 be less than .25 microns, correct?

20 A. No, I was actually saying the opposite
21 earlier; that you need more than half the
22 centimeter of the contact to fill -- fully fill the
23 hole when you have million and million of contacts
24 because each die -- and you have a hundred of dies
25 on each wafer, so you need it to be even more than

1 the -- the -- half of the weights -- half of the
2 diameter of the contact.

3 Q. But -- but in the case of Miyazaki, where
4 you have a refractory metal layer partially filling
5 the hole, you would need actually less film
6 thickness required to fill the empty space in the
7 contact hole, correct?

8 A. You would need less amount --

9 MR. CHEN: Objection.

10 THE DEPONENT: I mean, less thick --
11 thickness of the tungsten inside the hole than in
12 the case that if you did not have refractory index.

13 Q. (By Mr. Colaianni) You noted in your
14 declaration that .2 micron thickness of the
15 tungsten film could not completely fill a .5 micron
16 diameter hole, correct?

17 A. Yes. Yes.

18 Q. With the presence of the refractory metal
19 layer in the hole, it's possible that the .2 micron
20 thickness tungsten could fill the hole, correct?

21 A. No, because you need them -- because --
22 like the way I was saying, you need it to be more
23 in -- I wouldn't say vastly more, but you need to
24 have a substantially more than the half of -- I
25 mean half of the diameter of the contact to fill.

1 So you even if you have the refractory metal, when
2 you have .2, it still wouldn't be able to
3 completely fill it.

4 Q. Well, yet a moment ago you said that the
5 presence of the refractory metal layer would allow
6 you to have less thickness of the tungsten layer,
7 correct?

8 A. Less than you would have in a case if you
9 wouldn't have refractory. But still you need to
10 have substantial amount -- substantial thickness in
11 order to completely fill the hole.

12 Q. And you would need in this case, if
13 you're talking about a .5 micron diameter hole --

14 A. Okay.

15 Q. -- and you have refractory metal layer
16 formed in the hole --

17 A. Okay.

18 Q. -- you would need less than half of that
19 diameter of tungsten thickness to fill the hole
20 completely, correct?

21 A. No, no, because -- I mean, it -- it's --
22 see, it's -- it's not so simple. It's not when
23 you're trying to fill this contact you are limited
24 by amount of the -- the reactant that are available
25 to come to each of these contacts. And when you

1 start filling it at the top, then on the side and
2 the bottom, less reactant are able to get in.
3 Actually, if you have a refractive metal, you are
4 even making it narrower and harder for reactant to
5 get to the bottom. So it's -- you will -- you will
6 need more than for sure half the width -- half of
7 the diameter of the hole to fill it, because you
8 have many of the solids are very close to each
9 other, and they are -- okay. So in confidence they
10 are stealing molecules from each other. So you
11 need to satisfy all of them to be able to fill
12 it -- to fill them.

13 Q. But you would agree that the diameter of
14 the hole, after the patterning of the refractory
15 metal layer, is now less than 25 microns, correct?

16 A. Yeah, the diameter of the hole become a
17 bit smaller, yeah.

18 Q. Depending on the thickness of the
19 refractory metal layer, correct?

20 A. Yeah, it becomes --

21 Q. So there's less space to fill with the
22 tungsten film, correct?

23 A. Yeah, but you also -- at the same time,
24 you are blocking the entrance to all; because when
25 it becomes smaller, the aspect ratio still stays

1 fairly high and it's -- it will be hard to fill the
2 side and the bottom of the hole.

3 Q. But -- but you would still have less
4 physical space to fill in the hole because of the
5 presence of the refractory metal layer, correct?

6 A. You would have less space, but you are --
7 at the same time that you have less space, you make
8 it harder to fill it, is what I'm trying to say.
9 Because when you put the refractory metal on the
10 top, the top is the very sensitive point because
11 it's -- it's basically the gate for the reactant to
12 go into this vertical structure. And if you make
13 the gate smaller, you have less reactant being able
14 to go into the hole and fill it.

15 I think I describe it. I say in my --
16 yeah, it's paragraph 64, that -- the part of
17 paragraph 64 that the forming of .2 micron film
18 over a contact using tungsten would likely mean
19 that the thickness of tungsten filament, the one in
20 the hole, is even less than .2 micron. When a
21 layer is deposited, typically the deposition rate
22 along the side and bottom of the hole is lower
23 since the deposition rate outside of the planar on
24 the flat planar surface. The flow --

25 And this is the same thing as when I was

1 talking about the gate. So when I was talking
2 about the gate a moment ago, referring -- the flow
3 of reactants into the hole is limited by its access
4 to the hole opening. Limiting the supply of fresh
5 reactant into -- inside the smaller hole will
6 further reduce the deposition rate within the hole.

7 Q. Do you believe a different thickness of
8 tungsten film would be required if the refractory
9 metal layer were not there?

10 A. Yeah. I mean, I -- because, basically,
11 that you need to have film thick enough that you
12 would be able to fill up the hole because it's
13 different environment inside the hole.

14 Q. Do you -- do you agree that the presence
15 of the refractory metal layer means that the
16 thickness of the tungsten film required to fill the
17 hole would be -- would be less than without the
18 refractory metal layer?

19 A. Not necessarily, because like the way I
20 was saying is that it's -- you are making the
21 gate -- you can think of the opening -- contact
22 opening like a gate for each of these contact hole.
23 So you make the gate smaller so less reactant can
24 go into, so it could take a minute. You need a
25 thicker layer being deposited on the surface before

1 you can really fully fill the hole.

2 Q. So -- so it's your opinion that the same
3 thickness of tungsten layer may be required to fill
4 the hole, whether the refractory metal layer is
5 present or not?

6 A. No, no, no. I wasn't saying the same
7 thickness. I was saying the refractory will make a
8 difference, but it slows down the reaction and it
9 could end up even requiring to deposit even more
10 when you have a refractory rate.

11 Q. But the thickness of the tungsten film
12 required to fill the hole with the refractory metal
13 layer present will be smaller than without the
14 refractory metal layer, correct?

15 A. No, because the -- the figure give a --
16 at the entrance -- and when I say "the entrance,"
17 the opening of the hole. It's like a gate; that
18 when you make it smaller opening by having the
19 refractory metal making it a bit smaller, you
20 are -- end up depositing -- you need to go longer
21 and deposit more before you can ready for some more
22 and deposit more on the surface. You have to put
23 more in this deposition process.

24 Q. But -- but the thickness required to fill
25 that space will be less if you have the refractory

1 metal layer formed in the hole, correct?

2 A. But you are doing the same deposition,
3 and the deposition has decided, okay, I want to
4 deposit -- I don't know -- half a micron, quarter
5 micron, three-quarters. So you are going through
6 one deposition process. So when you are -- during
7 the deposition process, you have -- you are going
8 through it as long as it take to do this. Like,
9 let's say if you decide to deposit three-quarters
10 of microns or continue depositing as long as it
11 take to deposit three-quarter of the microns.

12 Q. Sure.

13 But just as a matter of common sense,
14 the -- the refractory metal layer is going to take
15 up some of the space within the contact hole,
16 correct?

17 A. Yes.

18 Q. There's going to be less physical space
19 to fill in that contact hole with the tungsten film
20 after you've deposited the refractory metal layer,
21 correct?

22 A. Yeah, but you wouldn't be able to finish
23 filling it during a shorter deposition time or
24 shorter single layer because it's -- not every
25 reactant is able to get in there.

1 Q. Okay. So the process may take longer,
2 but -- but the thickness of the film required to
3 fill the hole will be less because of the presence
4 of the refractory metal layer, correct?

5 A. The thickness of the film will be -- on
6 the surface, it will be thicker film because it
7 take longer.

8 Q. The film will be -- will -- strike that.

9 Filling the hole with the refractory
10 metal layer present will require a thicker amount
11 of film --

12 A. Well --

13 Q. -- than without the refractory metal
14 layer?

15 A. It could, because on the surface outside
16 of the contact, you will end up depositing a
17 thicker layer during this period of time.

18 Q. But you have less space within the hole
19 to fill after the refractory metal layer has been
20 deposited, though, correct?

21 A. Inside the -- see, because inside the
22 hole you have a limited size; that this is what you
23 are limited. But the -- we are talking about the
24 thickness of the film being deposited. So you
25 deposit the film both outside of the hole and

1 inside the hole. Outside the hole, the film will
2 be thicker because it take longer when you have a
3 smaller opening to be able to fill fully this full
4 thickness without having a void.

5 Q. Inside the hole they require a thickness
6 of the tungsten film would be less to completely
7 fill the hole in the presence of the refractory
8 metal layer, correct?

9 MR. CHEN: Objection to form.

10 THE DEPONENT: It will be -- it will be
11 small -- you need a smaller amount of tungsten
12 inside the hole. But at the same time, the area on
13 the flat surface, you will have a thicker layers
14 because it take longer to be able to have all the
15 reactant go into the hole and fill it.

16 Q. (By Mr. Colaianni) When you say the flat
17 surface, are you referring to the bottom of the
18 contact hole?

19 A. No, I'm talking to the -- the flat -- the
20 edges outside surrounding the contact hole.

21 Q. You talking about areas outside the
22 contact hole?

23 A. Yeah, but to deposit tungsten layer at
24 the same time.

25 Q. Right.

1 I'm referring to the area within the
2 contact hole. And inside the contact hole, the --
3 the thickness of the layers being deposited would
4 be -- would be less than what you would need to
5 deposit to fill the hole without the refractory
6 metal layer, correct?

7 MR. CHEN: Objection to form.

8 THE DEPONENT: Eventually -- I mean,
9 because it takes longer and it could also form a
10 void when you have the refractory metal inside the
11 holes, because it's harder to fill it.

12 Q. (By Mr. Colaianni) So would it take a
13 thicker film to fill a .4 micron diameter hole than
14 a .5 micron diameter hole?

15 A. That the -- it could take longer because
16 you need to -- to go through a longer deposition
17 which end up depositing a thicker layer of -- of
18 tungsten on a flat surface.

19 Q. Well, regardless of the timing, the
20 thickness required inside the hole to fill a
21 smaller hole is less, as a matter of common sense,
22 right?

23 A. Yeah, but you see -- but the thing that
24 you are missing here, that these are deposition,
25 and you cannot choose the deposition time by the

1 fact that you have a smaller hole so you have less
2 surface -- less space to fill. You have to go
3 longer because it's harder to do. And while you
4 are doing longer, the film thickness becomes
5 thicker in quite a few areas around it.

6 Q. The -- the film --

7 A. And it could lead to void also.

8 Q. The -- the film thickness outside the
9 hole is thicker?

10 A. Yeah, but this is also the top corner
11 of -- which is the most sensitive thing which you
12 fill there, the top corner of the contact. You
13 always -- the films are -- is the thickest and you
14 have to be careful -- I mean, unless you make the
15 contact smaller so that you don't totally close the
16 opening on the top. Because it sees that it's --
17 for basic material science properties, that the top
18 opening is that you can have reactant -- reaction
19 happening from every direction because see that
20 it's -- it's -- you can think of like a point that
21 you can have molecule attaching themselves to it from
22 every possible direction. So it's usually the
23 thickest part.

24 And what you have to be careful that you
25 are not in a -- creating a structure that you are

1 totally fill the top surface -- I mean the top
2 opening and closing it, and then you get a large
3 void inside.

4 Q. Miyazaki discloses that the first
5 tungsten film has excellent step coverage, correct?

6 A. Which tungsten film? Which you
7 talking --

8 Q. The -- the tungsten film 15 that fills
9 the contact hole in figure 8C, for example.

10 A. Yeah.

11 Q. And -- and good step coverage means that
12 the thickness on -- on the sidewalls and the planar
13 surface of the contact hole is -- is the same
14 everywhere, correct?

15 (Brief interruption.)

16 (Discussion off the stenographic record.)

17 Q. (By Mr. Colaianni) Good step coverage
18 means that the thickness of the film along the
19 sidewalls and the planar surface of the hole was
20 the same everywhere, correct?

21 A. Yes.

22 Q. And Miyazaki discloses a tungsten film
23 that has excellent step coverage, correct?

24 A. Yes.

25 Q. So would you agree that the thickness of

1 the tungsten film in Miyazaki would be the same
2 along the sidewalls and the planar surface of the
3 contact hole?

4 MR. CHEN: Objection to form.

5 THE DEPONENT: It's a -- I mean, it will
6 be -- see, not when they say "good step coverage."
7 Let -- let me clarify it.

8 It's not that the thickness is the same,
9 because you always will get more in the plain
10 surface -- I mean, not always. But typically, when
11 you are doing this process on a plain surface, you
12 get more -- more material deposited inside the hole
13 and the edge of the hole. It's basic material
14 properties.

15 When they say "good step coverage," it
16 says that they are able to fill the inside in a
17 conform shape and close it nicely, gradually,
18 without creating a void. But you see that this is
19 one reason why, when I was talking about that the
20 refractory index in example 3 is different from --
21 could be different from the rest of them because
22 you have a different -- you can end up having a
23 different deposition properties and different
24 characteristics, as far as step coverage.

25 So you cannot assume that if you have a

1 good step coverage, it's ensure that you wouldn't
2 form a void.

3 Q. (By Mr. Colaianni) But you would agree
4 that the tungsten film in Miyazaki, which has
5 excellent step coverage, would completely fill the
6 contact hole as shown, for example, in figure 8C,
7 correct?

8 MR. CHEN: Objection to form.

9 THE DEPONENT: It's -- I mean, it shows
10 that it -- it's nicely filled the holes up, but --
11 I mean, it is -- it's just illustration of how the
12 structure look like. And here's the same figure
13 for multiple embodiment and it's just showing the
14 different structures. It's not just that 8C is
15 just one specific way when you deposit, you create
16 this structure.

17 Q. (By Mr. Colaianni) Right.

18 But -- but figure 8C does show the
19 contact hole completely filled with the tungsten
20 film 15, correct?

21 MR. CHEN: Objection to form.

22 THE DEPONENT: Figure -- I mean, it's --
23 it just illustration, so it shows that it is a good
24 filling; that it's -- that it look filled.

25 Q. (By Mr. Colaianni) Yeah, it's completely

1 filled in -- in figure 8C, correct?

2 A. Yeah, in 8C, it shows it's completely
3 filled and it's illustrations that -- a general
4 illustration that -- to explain the principle.

5 Q. With respect to the -- the thickness of
6 the tungsten film, Miyazaki discloses in column
7 7 -- and I'm referring to lines 55 to 64,
8 roughly -- that the --

9 A. Which lines?

10 Q. I'm sorry. Let -- let's back up.
11 Column 7, roughly lines 55 or 56 through
12 63, 64.

13 A. Uh-huh.

14 Q. Miyazaki discloses that the contact hole
15 has a diameter .5 microns, correct?

16 A. Yeah.

17 Q. And he's referring here to figure 8C,
18 correct?

19 A. Yeah.

20 Q. That this discussion is in character with
21 the embodiment of figure 8C, correct?

22 A. Yeah, figure 8C, he's talking about.

23 Q. And he says around line 59, "For example,
24 when the contact hole having a diameter of
25 0.5 microns, the thickness of the deposited film is

1 0.2 microns or more," correct?

2 A. Yes.

3 Q. So Miyazaki allows the thickness of the
4 deposited tungsten film to be greater than .2
5 microns, correct?

6 A. Yeah, greater. Uh-huh.

7 Q. And he discloses that figure of
8 .2 microns or more as an example, correct?

9 A. Yes.

10 Q. So -- so the disclosure here can
11 encompass tungsten films thicker than .2 microns in
12 the embodiment of figure 8C, correct?

13 A. Yes.

14 Q. And one -- the -- the overarching goal of
15 the Miyazaki reference is to provide a stress --
16 excuse me -- a low stress, void-free interconnect,
17 correct?

18 A. Yes.

19 MR. CHEN: Objection to form.

20 Q. (By Mr. Colaianni) And that's -- that's
21 achieved with the -- when the contact hole is
22 completely filled, correct?

23 MR. CHEN: Objection to form.

24 THE DEPONENT: No. The -- the last
25 stress is independent from the size of the hole --

1 of the contact hole. The low stress is the
2 property of the film deposited in this condition.

3 Q. (By Mr. Colaianni) But -- but the
4 void-free nature of the objective is achieved
5 through completely filling the contact hole,
6 correct?

7 MR. CHEN: Objection to form.

8 THE DEPONENT: Well, yeah. I mean, it --
9 you need to fully fill the contact opening in order
10 to having a -- a void.

11 MR. COLAIANNI: Okay. Is this a good
12 time for a lunch break?

13 MR. CHEN: Yeah. Sounds good.

14 MR. COLAIANNI: Okay.

15 THE VIDEOGRAPHER: The time is 12:41 p.m.
16 and we are off the record.

17 (Recess taken.)

18 THE VIDEOGRAPHER: The time is 1:25 p.m.
19 and we are on the record.

20 Q. (By Mr. Colaianni) Welcome back.

21 A. Good afternoon.

22 Q. When we left, we were talking about the
23 Miyazaki reference, and I just have a couple more
24 questions on the embodiment we were talking about.

25 If we look back at figure 8C, for

1 example.

2 The -- the first tungsten film 15 is
3 formed under a reaction rate controlling condition
4 to realize excellent step coverage, correct?

5 A. When he's talking about embodiment and --

6 Q. I'm referring you, if you want to check
7 this, to figures -- excuse me.

8 A. Embodiment 1.

9 Q. Column 7, lines 50 to 55.

10 A. Yeah, rate -- rate control.

11 Q. The -- the tungsten film 15 is formed
12 under a reaction rate controlling condition to
13 realize excellent step coverage, correct?

14 A. Yeah, to deposit under rate -- yeah,
15 correct, under rate control reaction -- reaction
16 rate controlled condition with a good step
17 coverage.

18 Q. And if you look at figure 8D, there is
19 disclosed there a second CVD tungsten film 16
20 that's formed on the tungsten film 15, correct?

21 A. Yes.

22 Q. And according to Miyazaki, that second
23 tungsten film 16 is formed under a supply rate
24 controlling condition to produce a low-stress film,
25 correct?

1 A. I'm trying to find it in the -- the
2 specifications.

3 Q. Yeah. You can take a look at column 7,
4 line 64 through column 8, line 2, if you want to
5 check that.

6 A. Yes, he mentioned it's under supply rate
7 condition is film 16.

8 Q. So the tungsten film 16 has a step
9 coverage that is worse than the first tungsten
10 film 15, correct?

11 A. Yes. It -- it clearly was, yeah.

12 Q. Okay. Now, with respect to the
13 embodiments 3, 4 and 5 of the Miyazaki reference,
14 you acknowledge that Miyazaki specifies the
15 thickness of the first layer as around .2 microns
16 or more, correct?

17 A. Yeah, for -- yeah, I mentioned for
18 embodiments 3 and in line like -- column 7,
19 line 61. Embodiment 4 in line 37 and -- and in
20 embodiment 5 in column 8, line 65.

21 Q. Thank you.

22 Does Miyazaki specify a thickness of the
23 second layer in embodiments 3, 4 and 5?

24 A. I don't believe so. And it doesn't look,
25 at least from looking at these pages, it is

1 specified in the thickness of the second layer.

2 Q. The purpose of the second layer in
3 embodiments 3 through 5 is to reduce the stress of
4 the first layer, correct?

5 MR. CHEN: Objection to form.

6 THE DEPONENT: Well, it's -- I mean, so,
7 see, the first layer is done to fill the contacts
8 and then establish conductivity between the layer
9 underneath it to the layer 16, which will be
10 deposited later. So it's a -- I mean, you deposit
11 this film for purpose of creating electrical wires
12 and connecting them to the substrate.

13 Q. (By Mr. Colaianni) Well, does the second
14 layer in embodiments 3 through 5 help prevent
15 manufacturing problems such as wafer bending?

16 A. Yeah, by having it deposited at a lower
17 stress. I mean, having it deposited so it would be
18 a layer which would have less stress.

19 Q. Is it possible for the second layer to be
20 so thin that it fails to prevent wafer bending?

21 MR. CHEN: Objection. Form.

22 THE DEPONENT: Yeah -- yeah. I mean --
23 yeah, if it's too thin relative to the specific
24 circumstance of the topography on the wafers, how
25 many contact all you have and how -- how deeply --

1 I mean how you filled with the first layer, then
2 the second layer could be not adequate to prevent a
3 wafer bending.

4 Q. (By Mr. Colaianni) Do you believe a
5 person skilled in the art would understand how
6 thick the second layer would need to be in order to
7 prevent problems like wafer bending from occurring?

8 A. Sometimes. Because, see, it depends
9 how -- how easy to control the -- the process or
10 the topography that it is dealing. So, see -- I
11 mean, you have fabrication lines that -- they are
12 the same kind of a wafer that's -- only they make
13 only one product and they always see the same
14 topographies that you need to fill the contact
15 hole. While you have other places, like these
16 CMCs, that they get -- some product have smaller
17 die with fewer contact and another -- another
18 product with more contact. So you have a different
19 topology that you are trying to fill and create
20 environment and the stress is not too high.

21 Q. In the context of figures 8C and 8D of
22 Miyazaki, do you believe a person skilled in the
23 art would understand how thick the second layer
24 would have to be to avoid wafer bending or other
25 manufacturing problems?

1 MR. CHEN: Objection to form.

2 THE DEPONENT: Not automatically in --
3 because it depend on its experience and the -- and
4 the product that it's dealing with and -- and it
5 depends how much the first layer would vary. So I
6 mean, he will know that he probably have to play --
7 pay close attention if the wafer bend or not, but
8 you wouldn't necessarily know what cause it or --
9 or how to avoid it just by somebody telling me this
10 wafer got bent or something.

11 Q. (By Mr. Colaianni) But a person skilled
12 in the art would understand certain ways to measure
13 the stress or the wafer bending that we talked
14 about earlier, correct?

15 A. Yeah, you would be able to measure that.
16 Yeah.

17 Q. And based on that information, it would
18 be within the realm of a person skilled in the art
19 to figure out a relevant thickness for the second
20 layer to avoid problems of wafer bending, correct?

21 A. I mean, he will know that -- if he has a
22 problem or not and -- but to go to the next step of
23 figuring out if the cause was because a second
24 layer was too thin or -- or if the cause was
25 because of the deposition condition where the

1 process corner -- when I say "process corner," you
2 see that for each process, it's not that you die
3 one parameter and it's always separate in this
4 condition, you have a range that the parameter will
5 vary, like plus or minus 10 percent, or the
6 temperature go up plus or minus degrees. So you
7 can have a set of circumstances the temperature is
8 at the process corner, it's at the end of the
9 highest of the range and the flow rate is the
10 lowest or the highest. So when you reach this
11 condition, you can end having even the lower level
12 either having too high stress or the wrong
13 thickness.

14 So he will know that what are the
15 potential -- several potential causes, but he
16 wouldn't know which -- which one of them was the --
17 one causing them.

18 Q. That's -- that's something that would be
19 understandable through reasonable experimentation,
20 though, correct?

21 MR. CHEN: Objection to form.

22 THE DEPONENT: That after some
23 experimentation and experience, he would be able to
24 know where to look for it. But by seeing that the
25 wafer bend or operator telling him that too many

1 wafer don't make it through to the next. I mean --
2 so the transport between the chambers of the
3 advanced machines, he -- he would know what he need
4 to look at, but he wouldn't know which one was --
5 is the cause because it's a complicated processes
6 and a lot of interaction between the various
7 processes and the various steps.

8 Q. (By Mr. Colaianni) Right.

9 But those are the types of problems that
10 are encountered when people design semiconductors,
11 correct?

12 A. Yeah. But if you are somebody who design
13 semiconductor processes, you are more aware that
14 the level of interaction and the importance of them
15 knowing -- I mean, looking how one step is impacted
16 by another steps. So it's not something that
17 person is skilled in the art would know all the
18 potential and things that you need to watch for or
19 what range to define, let's say, for a thickness
20 deposition because it could affect something up in
21 the subsequent one or several step later.

22 Q. And this -- your opinion there is
23 based -- is that based on your personal experience?

24 A. It's experience in the industry that I
25 am -- it's a well-known for fact. For example,

1 there's something called "copy exactly" -- I think
2 it's called something like "copy exactly."

3 Intel is famous for it. When they tried
4 to make -- open a new fabrication line using the
5 same technology -- going through the same
6 technology, they buy everything exactly the same,
7 exactly the same equipment, the same transport to
8 transfer the wafer. Everything would look exactly
9 the same because the parameters that affect these
10 devices are -- there are many times how to know and
11 anticipate in advance because it create million and
12 millions of transistors that you need to develop
13 them to be within a very small permutation range in
14 order for each die to work. Because not even that
15 they are not having a good yield. But to have one
16 die working, you need every transistor for it -- if
17 it -- the many transistor, all of them, would have
18 just small variations.

19 Q. I -- I appreciate that. But getting back
20 to what we're talking about here --

21 A. Uh-huh.

22 Q. -- in connection with --

23 A. Sure.

24 Q. -- with the -- with the prior art, the --
25 the thickness of the second layer is something that

1 a person skilled in the art would be able to
2 ascertain through some experimentation based on
3 well-known wafer stress testing that we talked
4 about earlier, correct?

5 MR. CHEN: Objection to form.

6 THE DEPONENT: With -- with guideline
7 with somebody who is more experienced, he will know
8 what -- what test to do that -- in order to create
9 the right properties of these complex structures.

10 Q. (By Mr. Colaianni) Now, the sixth
11 embodiment of the Miyazaki reference discloses that
12 the overall stress of the two-layer tungsten
13 deposition is a function of the ratio of the film
14 thickness of the first and second layers, correct?

15 A. Correct.

16 Q. And embodiment 6 discloses what stress
17 levels each of the first and second films and which
18 thickness they should have in order to achieve an
19 overall stress level, correct?

20 A. He doesn't mention the thicknesses of the
21 films.

22 Q. He -- well, let's take a look, if we can.
23 Okay. Let's -- let's move on.

24 And how would a person skilled in the art
25 determine the stress level in the first layer and

1 the second layer of embodiment 6 of Miyazaki?

2 A. That a person of ordinary skill in the
3 art would need to have new experiment with guidance
4 and it wouldn't be obvious to him. And it's even
5 possible he wouldn't realize it. And he will get
6 concern quality -- properties by changing the
7 thicknesses of the layers and -- and so it is just
8 by experiment he can see which one of them works.
9 Or he would have a guideline that you need to keep
10 this -- the first layer at certain thickness range,
11 the second layer at certain thickness range, and
12 you just follow it. And this is what I have been
13 told you need to do.

14 Q. Embodiment 6 does disclose the ratio of
15 the thicknesses between the two tungsten layers,
16 correct?

17 A. It doesn't disclose. It said that you
18 should control the ratio in order to achieve
19 certain stress level, but it doesn't tell you the
20 ratios to be -- I mean, it's -- well, maybe it says
21 it has to be no greater than 70 percent of the
22 ratios, is the only thing that it says. So
23 anywhere from 0 to 70, I guess is -- I don't know.
24 This is not very specific and is the only thing I
25 see it mentioned anything about what the ratios

1 are.

2 Q. Well -- well --

3 A. Unless I'm missing it and I don't see it
4 here.

5 Q. I'm sorry. Take a look at figure 12.
6 The -- figure 12 discloses the -- the film
7 thickness composition ratios, correct?

8 A. Of figure 12. Yeah, it -- it disclose --
9 it shows what -- what ratio you can have and what
10 stress you will get.

11 Q. And there were -- there were techniques
12 available to persons skilled in the art to -- to
13 measure the stress of the first and second layer,
14 correct?

15 A. Yes.

16 Q. How would you determine the overall
17 stress of the two-layer structure in embodiment 6?

18 A. By looking at the structure that has the
19 two layers created together and doing it in both
20 stress wafer and product wafer.

21 Q. And how would you determine a desired
22 overall stress for the two-layer structure in
23 embodiment 6 to prevent wafer bending or feed
24 errors?

25 A. By experimenting with different ratios

1 and seeing they give you -- that the wafer -- I
2 think that someplace here there is a table that is
3 showing the -- I could be off -- that showing how
4 many of them would fail.

5 Yeah. You see that in figure 6, it's
6 showing that -- I believe figure 6, it's showing --
7 I mean, showing you the percent of -- when you talk
8 100 percent in feed system. So how many of them --
9 how many wafer you can pass through a system that
10 feed wafer to a machine before you start seeing a
11 failure.

12 And is showing that if the stress go
13 greater than 10 -- 10 to the 10 -- 10 to the 10 to
14 the 9, then you basically have 100 percent failure.
15 But between 8 -- you start seeing problem, I think
16 it's probably like 9 -- between 9 and -- starting
17 from 9 -- 10 to the 9, you start seeing some
18 failures.

19 Q. If you know the stress of the first layer
20 and the stress of the second layer and the desired
21 overall stress to prevent wafer bending, you can
22 determine the ratio thickness of the first and
23 second layers, correct?

24 A. Can you repeat it.

25 Q. Sure. That was a complicated question.

1 I'll try it again.

2 A. No problem.

3 Q. If you know the -- the stress of the
4 first and second layers --

5 A. Okay.

6 Q. -- and you know the desired overall
7 stress that you want to prevent wafer bending or
8 feed errors --

9 A. Uh-huh.

10 Q. -- you can determine the ratio of the
11 thickness of the first and second layers in
12 embodiment 6, correct?

13 A. Yeah, you can -- if you knew the -- the
14 stress of each of the layers in -- you can
15 determine a certain ratio is give you a certain
16 stress level.

17 Q. And if you know the ratio of thickness of
18 the first layer and the second layer to prevent
19 errors and you know the thickness of the first
20 layer, you can determine the thickness of the
21 second layer, correct?

22 A. Yeah, if you know the thickness of the --
23 the first layer, you can determine the thickness of
24 the second layer.

25 Q. Any method that you would use to

1 determine the stress of the first and second layers
2 in embodiment 6 could also apply to determine the
3 stress of first and second layers in embodiments 3
4 through 5, correct?

5 A. You can apply the same test, but it
6 wouldn't be something that will be obvious in a
7 person asking now would see if he can do it,
8 because embodiment 6 is very different from the
9 other embodiment he's talking about. Basically is
10 just changing ratio of two layers in order to get
11 certain stress level.

12 Q. Well, but it's possible to apply the same
13 test to determine the stress levels of the first
14 and second layer in both sets of embodiments,
15 correct?

16 A. You can theoretically apply the same
17 test, but person who is skilled in the art wouldn't
18 think of doing something like this because
19 embodiment 6 is going in totally different
20 directions than the earlier embodiment.

21 Q. I just want to clarify.

22 What -- what is the totally different
23 direction you're referring to?

24 A. So, see, embodiment 6 just telling you
25 that if you want to achieve a certain stress level,

1 you can play with the ratio of thicknesses. It
2 doesn't tell you what condition you make the
3 layers, what stress it would have, while the other
4 embodiments are talking of putting layers with
5 conditions that create a certain stress on each of
6 the layers.

7 It doesn't tell you in -- to have one
8 layer at one thickness, the other one at different
9 thickness. It doesn't mention anything about the
10 ratio of the thickness in order to get a certain
11 stress. It's going totally different direction.

12 Q. Embodiment 3 through 5 disclosed the
13 process parameters for making the layers a certain
14 thickness, correct?

15 A. Three to 5 disclose specific parameters
16 to form layers with certain stress level. This is
17 the only thing that they do. They don't mention
18 about the ratio of the two layers in none of the
19 embodiments 3 to 5.

20 Q. Figure 6 does disclose the -- disclose
21 the ratio of the thicknesses, correct?

22 A. Figure --

23 Q. I'm sorry. Strike that.

24 I meant embodiment 6 discloses the ratio
25 of the thicknesses, correct?

1 A. Embodiment 6 discloses the ratio -- I
2 mean, it says that you get different stress level
3 by changing the ratio and you can bring example in
4 line -- column 9, line 50, 51, that -- it's talking
5 about the layer of 15 is not greater than
6 70 percent of the thickness ratio.

7 Q. A person skilled in the art could
8 determine the thickness of the second layer in
9 embodiments 3 through 5 based on the teachings of
10 embodiment 6, correct?

11 A. No. I mean, because it's the --
12 embodiment 6 is not part of embodiment 3 to 5. It
13 doesn't tell him what thickness it should have for
14 the second layer.

15 Q. Well, embodiment 6 begins in the
16 specification at column 9, correct?

17 A. Yes.

18 Q. There's a discussion there of the sixth
19 embodiment and that discussion refers back to the
20 third and fourth embodiments, correct?

21 A. It just say that the -- the earlier
22 embodiment are -- you -- you use the earlier
23 embodiment to describe the structures that you
24 created to tungsten filament bar. You get contact
25 hole, you put oxide and -- above the substrate and

1 you make contact hole and so on.

2 Q. Correct.

3 The -- the -- the description of
4 embodiment 6 refers back to embodiments 3 through
5 5, with respect to at least the structural aspects,
6 correct?

7 A. Yeah, the structure that you put the --
8 the metal on.

9 Q. And process parameters would -- would
10 need to be used in forming the semiconductor
11 described in embodiments 3 through 5, correct?

12 A. Well, embodiments 3 to 5 describe a
13 process parameter to create their own structure and
14 the metal layer -- the low metal and the higher
15 metal layer.

16 Q. Yeah.

17 Those -- those process parameters apply
18 to the formation of that semiconductor described
19 in -- right?

20 A. And the embodi- -- for the specific
21 embodiment for its own set of parameters. 6, its
22 own, 7 -- no, sorry. 3, is its own. I mean --
23 sorry.

24 So we starting from -- 5 for its own.

25 Sorry.

1 3 has its own set of parameters. 4 has
2 its own. 5 has its own set of parameter of
3 creating the two layers.

4 Q. But you -- do you view embodiment 6,
5 described in the specification, as completely
6 unrelated to embodiment 3 through 5?

7 A. Well, I mean, it's independent
8 embodiments. It don't say that -- see, nowhere it
9 says in the -- I mean, it -- embodiment 3 that do
10 this -- I mean, do the first layer under this
11 condition and the second layer under this condition
12 and make the thickness of the two layers based on
13 what embodiment 6 called for. And, similarly, for
14 embodiment 4 and 5. So they are independent
15 embodiments.

16 Q. But -- but do you believe that
17 embodiment 6 is completely independent, completely
18 unrelated to embodiment 3 through 5?

19 A. I mean, it's related because it's done on
20 the same structure where you have the contact hole
21 that you are trying to contact with the substrate
22 to a metal layer above it and so on. But it's
23 totally different way of thinking about it,
24 embodiments 6, because it say different way to
25 achieve this -- the goal of reaching a certain

1 stress level and having the wafer not bend.

2 Q. Do you believe a person skilled in the
3 art would not be able to make a semiconductor
4 according to embodiment 6, based on the disclosure
5 of Miyazaki?

6 A. Just reading this, he wouldn't know how
7 to make the wafer because it doesn't specify the --
8 how to do it exactly, and so you wouldn't know
9 which -- I mean what recipes to use and so on.

10 Q. Do you believe embodiment 6 is covered by
11 any of the claims of the Miyazaki patent?

12 MR. CHEN: Objection to form.

13 THE DEPONENT: Let me just read the
14 claims for a second.

15 Can you repeat that question.

16 Q. (By Mr. Colaianni) Do you -- do you
17 believe embodiment 6 is covered by any of the
18 claims of the Miyazaki patent?

19 MR. CHEN: Objection to form.

20 THE DEPONENT: I mean, I -- it's
21 something that I didn't spend a lot of time in
22 focusing on it in my declaration, but it looked,
23 from the way the claim is written, that you
24 would -- in order for the claim to cover it, you
25 will have to use ion injection film, it looks like

1 what this claim called for. And I don't believe
2 that -- so 6 could be applied with the ion
3 injection, but embodiment 3 to 5 don't call for ion
4 injection.

5 Q. (By Mr. Colaianni) Would a person
6 skilled in the art understand that embodiment 3
7 discloses a recipe to deposit two tungsten films?

8 A. Yeah, because embodiment 3, which is
9 covering column 7, line 25, roughly, to --
10 beginning of column 8, he is talking about
11 figure 8A all the way including 8C. And so he's
12 talking about in -- let me just see. Yeah, it --
13 because it actually mention also figure 9. So it
14 is saying that you deposited the second film 16 and
15 it continues separation from -- so, yeah, a person
16 of ordinary skill in the art would know that
17 embodiment 3 called to form two films.

18 Q. And the same is true for embodiments 4
19 and 5? Those are recipes to deposit two tungsten
20 films, correct?

21 A. Yes, both of them shows it. It continues
22 to deposit a second film 16.

23 MR. COLAIANNI: Okay. I'm going to mark
24 another exhibit --

25 THE DEPONENT: Sure.

1 MR. COLAIANNI: This will be
2 Exhibit 5 and it is -- it appears to be
3 SAMSUNG-1016.

4 (Exhibit 5 was marked for identification
5 by the court reporter and is attached hereto.)

6 Q. (By Mr. Colaianni) Do you recognize
7 Exhibit 5?

8 A. Yeah. It's one of the reference to
9 Dr. Rubloff's declaration, I believe.

10 Q. This is the Felix prior art reference,
11 correct?

12 A. Yes.

13 Q. And you considered the Felix reference in
14 your analysis?

15 A. Yes.

16 Q. Felix references in is his title "ULSI."
17 Do you see that?

18 A. Yeah. Uh-huh.

19 Q. What does that stand for?

20 A. Ultra large scale integration, I believe.
21 I mean, it's just -- people come with the marketing
22 name of a new generation. So I think this is where
23 it's came from. VSI, ULSI.

24 Q. Can you take a look at figure 1 on
25 page 3 of the Felix reference, please.

1 A. Uh-huh.

2 Q. The figure 1 is captioned "5 levels
3 .35 micron CMOS interconnect schemes," correct?

4 A. Yes.

5 Q. Does .35 micron CMOS interconnect mean
6 that the diameter of CMOS interconnect is
7 .35 microns?

8 A. Well, it's -- not -- I mean, it's not so
9 straightforward. It turn into really marketing way
10 to label technology at certain size. See, it used
11 to be historically started that it would be the
12 smallest geometry that certain technology could
13 define would be .35, point -- half a micron, a
14 quarter or 25 nanometer, or whatever number is
15 used.

16 And then at certain point was -- they try
17 to make the transistor smaller. It used to be the
18 channel length would be the parameter which
19 wouldn't necessarily be even the smallest dimension
20 that you can define by the mask. It would just be
21 the smallest transistor conducted channel.

22 So it just -- in general terms that -- it
23 doesn't tell you -- it just tell you the general
24 generation of where this technology is, but you
25 cannot infer from it what specific future size

1 would be.

2 Q. But the diameter could -- strike that.

3 The diameter of the -- of the
4 interconnect could be .35 microns, correct?

5 A. Yeah, it shows that it's likely that this
6 technology -- by their definition, they use a .35
7 contact size or channel length, or something like
8 this.

9 Q. A CMOS interconnect can be a contact hole
10 or a via hole, correct?

11 A. Yes. Interconnect just basically means
12 that it's -- well, CMOS's technology is that it's
13 complementary MOS transistors, which are
14 experiential, which usually are devices that
15 consume less power, and these are the mainstream of
16 technology that has been used for the last 20, 30
17 years or longer.

18 An interconnect, it just -- they
19 conducting the layers in these devices. It's
20 connective different devices according to
21 interconnect. So you are just -- are you --
22 connect one -- one layer or one wire to another
23 wire, is what I infer from just seeing this title.
24 You have to wait specifically to see what exactly
25 he's talking about.

1 Q. With reference to figure 1, Felix
2 discloses that a layer of titanium or titanium
3 nitride is deposited in a contact hole, correct?

4 A. Yeah. Yeah, typically processed. Yeah.

5 Q. Felix disclosed that this layer of
6 titanium nitride can be an adhesion layer, correct?

7 A. Where does it say that it's adhesional?

8 Q. Referencing page 6 of the Felix reference
9 at the bottom of the page. There's a reference of
10 the layer for contact/adhesion barrier layers.

11 Do you see that?

12 A. So on page 6 on -- at the bottom, you
13 say?

14 Q. Page 6 of the -- of the ref- -- of the
15 document.

16 A. Oh, I was looking at page 6 -- the
17 multiple page number on -- so page 6, it's written
18 on the top page 6 or on the bottom?

19 Q. The bottom of page 6 under figure --

20 A. No, no, no. I mean the -- the page
21 number -- he has both page number on the top of the
22 page and he has page number on the bottom of the
23 page. So which page number are you talking about,
24 I'm asking?

25 Q. Okay. I'm referring to the page number

1 at the top of the page.

2 A. The one that is the page number on the
3 top. Okay. Yes.

4 Q. And right beneath figure 1, I'm referring
5 to. I think you're not on the right page.

6 A. Sorry. So this page?

7 Q. Yes.

8 A. So this page 6. So underneath figure 1.

9 Q. Do you see the reference there to the
10 contact adhesion barrier layers?

11 A. Yeah.

12 Q. So -- so would you agree that Felix
13 discloses that the layer of titanium or titanium
14 nitride can be an adhesion layer?

15 A. Well, he's just talking about a
16 different name process. He's talking about PVD,
17 which is physical vapor deposition. And it's not
18 really a CVD process. And he's also not talking
19 about -- I mean, he mention here aluminums. They
20 deposit a layer of aluminums in --

21 Q. But this layer that's being described is
22 an adhesion layer, correct?

23 A. But this isn't -- the adhesion -- it's --
24 so you see like the way we are talking earlier that
25 this process is really very complicated and every

1 step is tied to other step.

2 If something that adhesion to certain
3 layer that will be deposit later, it wouldn't
4 necessarily serve as a good adhesion, if it deposit
5 very different layers, because each layer which
6 is -- each material has certain chemical property
7 and only certain combination of addition layers
8 with a layer above it, it will -- it will have a
9 good adhere. And the adhesion basically mean that
10 when you put the later layer, the material would,
11 in subsequent steps, start to peel off, which then
12 you can start having debris on the wafer or defect
13 or contamination.

14 So not every adhesion layer that work for
15 one material work for different material. And,
16 also, when you use PVD process, it's different from
17 a CVD process so you wouldn't get the same
18 property. So you cannot assume that if it's
19 adhesion combination of layers that it will work in
20 a different combination layer it's a good adhesion.
21 It's similar to glue. See, glue that work for
22 metal and plastic is -- doesn't work for other
23 materials. So it's -- it's only adhesion for
24 certain materials.

25 Q. Right.

1 But Felix describes this layer as an
2 adhesion layer, correct?

3 A. For the specifics layer that he's talking
4 about. And he's talking there about a aluminum
5 alloy layer and he's using a PVD process. So is --
6 it's a different set of -- I mean, it's different
7 structure.

8 Q. And Felix discloses that the contact
9 holes are completely filled with tungsten using a
10 blanket CV- -- CVD step, at the top of the next
11 page, correct?

12 MR. CHEN: Objection to form.

13 THE DEPONENT: He said that he fill this
14 contact hole with a CVD tungsten and -- in etching
15 process, yeah.

16 MR. COLAIANNI: Okay. I'm finished with
17 the questioning for this '466 --

18 MR. CHEN: Okay.

19 MR. COLAIANNI: -- IPR. Do you want to
20 take a break or --

21 MR. CHEN: Yeah, let me take a quick
22 break and I'll see...

23 THE VIDEOGRAPHER: This marks the end to
24 DVD No. 2 in the video deposition of Ron Maltiel.
25 The time is 2:13 p.m. and we are off the record.

1 (Recess taken.)

2 THE VIDEOGRAPHER: This marks the
3 beginning to DVD No. 3 in the videotaped deposition
4 of Ron Maltiel. The time is 2:33 p.m. and we are
5 on the record.

6 EXAMINATION

7 BY MR. COLAIANNI:

8 Q. Good afternoon.

9 A. Good afternoon.

10 Q. This begins the deposition in the matter
11 of IPR 2015-00467.

12 And I will start by marking a few
13 exhibits. Let's -- let's mark Mr. Maltiel's
14 exhibit -- declaration as Exhibit 6.

15 (Exhibit 6 was marked for identification
16 by the court reporter and is attached hereto.)

17 Q. (By Mr. Colaianni) And we can mark the
18 prior art patent to EMESH, E-M-E-S-H,
19 U.S. Patent No. 5,407,698 as Exhibit 7, and that
20 was produced at SAMSUNG-1009.

21 (Exhibit 7 was marked for identification
22 by the court reporter and is attached hereto.)

23 Q. (By Mr. Colaianni) Do you have Exhibit 6
24 and 7 in front of you?

25 A. Yes, I do.

1 Q. And do you recognize Exhibit 6?

2 A. Yeah, it look like my declaration.

3 Q. And you prepared this declaration in
4 connection with this matter, correct?

5 A. Correct.

6 Q. And are the materials that you considered
7 in forming the opinions expressed in this
8 declaration set forth in the declaration?

9 A. I believe so.

10 Q. There are no other materials you
11 considered that are not identified in the
12 declaration, correct?

13 A. Correct.

14 Q. And with respect to the issue of claim
15 construction, you did not dispute the proposed
16 constructions of Samsung for purposes of this
17 matter; is that correct?

18 A. I think it's discussed here in --
19 in para- -- basically, it's paragraph 41, so 44
20 it's described that issues that were brought up by
21 Samsung in -- and I feel comfortable with the way
22 it states here.

23 Q. You're not applying a different
24 construction for those --

25 A. Yeah, you --

1 Q. -- claim -- okay.

2 A. -- you could use the construction
3 describing it.

4 Q. And you have not applied any -- any
5 constructions to the other claim language in your
6 analysis that -- that's expressed in this
7 declaration, correct?

8 A. Correct. I -- I mean, it's basically --
9 it's describing my declaration, what I use.

10 Q. Exhibit 6 sets forth a complete statement
11 of your opinions in this matter, correct?

12 A. Yeah. Correct.

13 Q. And Exhibit 7 is the Emesh prior art
14 reference.

15 Do you see that?

16 A. Yeah.

17 Q. And you relied on the Emesh prior art
18 reference in your opinions expressed in your
19 declaration, correct?

20 A. Yes.

21 Q. Let's talk about the Emesh prior art
22 reference. In particular, the second embodiment of
23 Emesh.

24 You would agree that embodiment 2 of
25 Emesh makes reference to figures 2A through 2E,

1 correct?

2 A. Let me try to locate it.

3 It's -- it's in the summary here, so
4 it's -- yes. It's -- the second embodiment is in
5 2A through 2E.

6 Q. And Emesh discloses that embodiment 2 is
7 advantageous in filing small via holes that are
8 about .5 microns, correct?

9 You can look at column 9, lines 50 to 55,
10 if you want to check that.

11 A. Yeah. So -- I mean, it talks about --
12 there about filling small via, half a micron size.

13 Q. Let's look at figure 2A of Emesh.
14 Figure 2A shows a silicon semiconductor wafer
15 labeled 14, correct?

16 A. Yes.

17 Q. And figure 2A shows a dielectric
18 insulating layer of silicon dioxide, correct?

19 A. Are you talking about the layer 22?

20 Q. Correct.

21 A. Yes. So it's -- yeah, it describe a
22 dielectric forming a contact.

23 Q. The via hole 20 is formed in figure 2A,
24 correct?

25 A. Well, I mean, in -- you are going to fill

1 it. It's in 2A that gives a layer of 16, which is
2 probably what you're trying to connect to in --

3 Q. And there's a conductive layer of metal
4 labeled 16 that is exposed in the via hole,
5 correct?

6 A. Yeah. But I mean, figure 2A, the hole is
7 not filled yet.

8 Q. Correct.

9 And with respect to figure 2B of Emesh,
10 there is shown in figure 2B a titanium nitride
11 adhesion layer 24 that is deposited in the via
12 hole 20, correct?

13 A. Yes.

14 Q. The adhesion layer helps to form a strong
15 chemical bond between the layers of tungsten and
16 the dielectric layer, correct?

17 A. Yes.

18 Q. Emesh discloses that the titanium nitride
19 adhesion layer 24 is about 800 angstroms in
20 thickness, correct?

21 A. Yes.

22 Q. Figure 2B also shows a tungsten
23 nucleation layer 26 deposited on the adhesion
24 layer 24, correct?

25 A. Yes.

1 Q. And that's disclosed that the tungsten
2 nucleation layer 26 is about 1,000 angstroms in
3 thickness, correct?

4 A. Yes.

5 Q. Now, in your declaration, which we marked
6 as Exhibit 6, you don't make any mention of the
7 thickness of the titanium nitride adhesion
8 layer 24, correct?

9 A. Yeah, don't specifically cite it.

10 Q. Okay. Now, looking at figure 2C of
11 Emesh, figure 2C shows a first tungsten layer 40
12 deposited on the tungsten nucleation layer 26,
13 correct?

14 A. Yes.

15 Q. And Emesh discloses that the first
16 tungsten layer 40 is deposited using a low H2 over
17 WF6 ratio of about 6 to 8 and 0 to 15 sccm in a
18 carrier gas of Argon at a total pressure of about
19 9 Torr, correct?

20 A. Yes.

21 Q. Emesh discloses that the first tungsten
22 layer 40 is deposited at 430 degrees Celsius,
23 correct?

24 A. You mentioned 4 -- see, I am looking at
25 column 9, when he was talking about -- I mean,

1 line 4 -- starting at 4 and going down -- so they
2 say -- so they say that they use the temperature of
3 430 with the high ratio of hydrogen to tungsten
4 fluoride.

5 Is this what you are -- I mean -- I'm not
6 sure -- can you repeat that question.

7 Q. Yes.

8 This disclosure in Emesh states that the
9 first tungsten layer 40 is deposited at 430 degrees
10 Celsius, correct?

11 A. It says that this layer 40 get
12 deposited -- yeah, it says that layer 40 get
13 deposited at 430 degrees Celsius.

14 Q. Okay. Emesh also discloses that the
15 first tungsten layer 40 has a step coverage of
16 greater than 90 percent, correct?

17 A. Yes.

18 Q. And what does it mean to have a step
19 coverage of greater than 90 percent?

20 A. That the amount that you fill inside the
21 hole is -- is up to 90 percent of what you would
22 fill in the flat area surrounding the hole.

23 Q. Looking back at figure 2D of Emesh,
24 figure 2D shows that the first tungsten layer 40 is
25 etched back with a tungsten plug filling the hole,

1 correct?

2 A. Yes. It's described in column 9, line 24
3 to 27. After depositing the tungsten, the filling
4 tungsten is etched back by conventional method such
5 as dry etching by exposure to plasma from SF₆,
6 figure 2D.

7 Q. The etch-back process in Emesh could be
8 performed using a chamber that's different from the
9 CVD chamber, correct?

10 A. Yes. It's typically done in a different
11 chamber than etch-back process.

12 Q. Okay. Looking at figure 2E of Emesh,
13 figure 2E shows a second tungsten layer 42, but
14 it's deposited on the first tungsten layer
15 layer 40, correct?

16 A. Yes. It's described in -- column 9,
17 line 30, the second layer of tungsten then is
18 deposited to a --

19 Q. Emesh also discloses that the second
20 tungsten layer 42 is deposited using a higher
21 hydrogen-to-tungsten-fluoride ratio of about 20 and
22 0 to 15 sccms at a total pressure of about 9 Torr,
23 correct?

24 A. Yes.

25 Q. Emesh also discloses that the second

1 tungsten layer 42 is deposited at 480 degrees
2 Celsius, correct?

3 A. Yes. It's in -- basically, it's in
4 column 9, line 32, all the way to 36.

5 Q. Emesh discloses that the deposition at
6 higher temperatures reduces film stress, correct?

7 A. Well, he's talking more about the
8 reflectivity and smaller grain size and so on, if
9 you look at line 40 to 46.

10 Q. I'm sorry. Where are you reading from?

11 A. I'm saying, column 9, line 40 to 46, he's
12 saying that the second film has a smaller grain
13 size, smaller surface, low diffuse reflectivity,
14 higher specular reflectivity to facilitate
15 photo-lithography for patenting the layer 42 to
16 define the interconnect structure.

17 Q. But the second -- but -- but -- strike
18 that.

19 The deposition at a higher temperature
20 does reduce the film stress, though.

21 Do you agree with that?

22 A. In general, it would reduce the film
23 stress, yeah.

24 Q. In -- in fact, at column 7, lines 60 to
25 62, Emesh discloses that deposition at higher

1 temperatures is beneficial and that it reduces the
2 film stress, correct?

3 A. Yeah, and not even close. Exactly close,
4 yeah.

5 MR. COLAIANNI: Going to mark another
6 exhibit. This will be Exhibit 8. And it's -- it
7 was produced at SAMSUNG-1010. It's the Mak, M-A-K,
8 prior art reference.

9 (Exhibit 8 was marked for identification
10 by the court reporter and is attached hereto.)

11 Q. (By Mr. Colaianni) Do you recognize
12 Exhibit 8?

13 A. It look like they make reference to
14 Dr. Rubloff's report.

15 THE REPORTER: Can you repeat the
16 doctor's name again?

17 THE DEPONENT: I'm not sure of the
18 spelling of his name.

19 Q. (By Mr. Colaianni) Dr. Rubloff?

20 A. Rubloff, yeah.

21 Q. R-U-B-L-O-F-F.

22 And did you consider this reference in
23 your analysis?

24 A. Yes.

25 Q. Could you look at figure 1 of the Mak

1 reference. It's on page 2.

2 A. Okay.

3 Q. Figure 1 shows an AMAT 5000 integrated
4 deposition and etch-back system, correct?

5 A. Yes.

6 Q. Are you familiar with this tool?

7 A. Yes.

8 Q. Have you worked with it before?

9 A. Yeah. I mean, it's -- it's been used in
10 the industry for a while. So, yeah, I'm familiar
11 with it.

12 Q. And Mak discloses that up to four process
13 chambers can be attached to the AMAT 5000
14 mainframe, correct?

15 A. Yes.

16 Q. Figure 1 of Mak shows two D -- CVD
17 chambers, correct?

18 A. Yes.

19 Q. And figure 1 of Mak shows an etch-back
20 chamber, correct?

21 A. Yes.

22 Q. And figure 1 of Mak shows an expansion
23 chamber, correct?

24 A. It does, expansion chamber.

25 MR. COLAIANNI: Okay. That's -- that's

1 all we had on this IPR.

2 MR. CHEN: Okay.

3 MR. COLAIANNI: So --

4 MR. CHEN: I don't have any redirect --

5 MR. COLAIANNI: Okay.

6 MR. CHEN: -- then. If you want to move
7 on to the next one, we can do that.

8 MR. COLAIANNI: Yeah, I think we probably
9 should. Given the time, we can probably at least
10 start --

11 MR. CHEN: Yeah.

12 MR. COLAIANNI: -- the next one.

13 MR. CHEN: Yeah.

14 MR. COLAIANNI: If that's all right.

15 MR. CHEN: Okay. Do you want to break
16 and go off the record?

17 MR. COLAIANNI: Just for a couple minutes
18 perhaps.

19 MR. CHEN: Okay.

20 THE VIDEOGRAPHER: The time is 2:54 p.m.
21 and we are off the record.

22 (Recess taken.)

23 THE VIDEOGRAPHER: The time is 3:05 p.m.
24 and we are on the record.

25 EXAMINATION

1 BY MR. COLAIANNI:

2 Q. Good afternoon.

3 This begins the deposition in the matter
4 of IPR 2015-00460, and I will start by marking
5 three exhibits.

6 Exhibit 9 will be the U.S. Patent
7 No. 6,146,997, and it was produced as SAMSUNG-1001.

8 (Exhibit 9 was marked for identification
9 by the court reporter and is attached hereto.)

10 MR. COLAIANNI: Exhibit 10 will be
11 Mr. Maltiel's declaration in this matter, which was
12 produced as HOME-2002.

13 (Exhibit 10 was marked for identification
14 by the court reporter and is attached hereto.)

15 MR. COLAIANNI: And Exhibit 11 will be
16 U.S. Patent No. 6,277,720 to Doshi, et al. It was
17 produced as SAMSUNG-1005.

18 (Exhibit 11 was marked for identification
19 by the court reporter and is attached hereto.)

20 Q. (By Mr. Colaianni) Do you have
21 Exhibits 9, 10 and 11 in front of you?

22 A. Yes, I do.

23 Q. Do you recognize these exhibits?

24 A. They look like the -- the patents that
25 petition was about, '997, my declaration regarding

1 these patents and the Doshi reference '720.

2 Q. And does your declaration, which is
3 marked as Exhibit 10, contain all of the opinions
4 you hold relating to this matter?

5 A. Yes, it does.

6 Q. Let's take a look at the '997 patent,
7 which is Exhibit 9, and maybe we can start with
8 reference to figure 2A.

9 With reference to figure 2A, this shows a
10 semiconductor substrate 50, gate oxides 52, two
11 gate electrodes 54 and source drain diffusion
12 regions 58.

13 Correct?

14 A. Yes.

15 Q. Figure 2A also shows two silicon nitride
16 caps 56 on the gate electrodes 54, correct?

17 A. Yeah. I believe so, yeah.

18 Q. And figure 2A shows two silicon -- excuse
19 me -- figure 2A shows a layer oxide 60 with a
20 thickness of 150 angstroms formed over the
21 substrate surface and on the side wall of the gate
22 electrodes 54, correct?

23 A. Yeah. It's described in column 2, on the
24 structure in column 2, in line 48 through 56 or
25 through -- up to 59.

1 Q. The oxide layer 60 is formed by rapid
2 thermal oxidation, correct?

3 A. Yes.

4 Q. And according to the '997 patent, the
5 gate electrodes 54 can be made of polysilicon and
6 tungsten silicide, correct?

7 A. Yes.

8 Q. The gate electrodes 54 are conductive,
9 correct?

10 A. Yes.

11 Q. And the silicon nitrate caps 56 are
12 insulators, correct?

13 A. Yes.

14 Q. The oxide layer 60 is also an insulator,
15 correct?

16 A. Yes.

17 Q. With respect to figure 2A, if you perform
18 a blanket metal deposition, for example, an
19 aluminum -- well, take as an example an aluminum
20 deposition by sputtering.

21 A. Okay.

22 Q. Would you agree that the silicon nitride
23 cap 56 and the oxide layer 60 would prevent the
24 gate electrodes 54 from forming a direct electrical
25 contact with the deposited metal?

1 A. Generally, yes. Yeah.

2 Q. Now, looking at figure 2B of the '997
3 patent, this shows a conformal layer of silicon
4 nitride 62 deposited over the substrate surface,
5 correct?

6 A. Yes.

7 Q. And the silicon nitride layer 62 is
8 deposited using low pressure chemical vapor
9 deposition, correct?

10 A. Yes.

11 Q. According to the '997 patent, the silicon
12 nitride layer 62 preferably has a thickness of
13 about 100 to 500 angstroms, correct?

14 A. Yes. And, more preferably, 200 to 350
15 described in column 2, line 60 through 67.

16 Q. The '997 patent states that the invention
17 would work for silicon nitride layer 62 thickness
18 of 100 angstroms, right?

19 MR. CHEN: Objection. Form.

20 THE DEPONENT: Layer 62, that could be
21 anywhere from 100 to 500, yes.

22 Q. (By Mr. Colaianni) Now, turn the page to
23 figure 2C.

24 Figure 2C shows that a layer of insulator
25 64 is deposited of the substrate, correct?

1 A. Yes.

2 Q. The insulator layer 64 can be silicon
3 oxide or BPSG, correct?

4 A. Yes.

5 Q. And according to the '997 patent, the
6 insulator layer 64 is preferably planarized,
7 correct?

8 A. Yes.

9 Q. Figure 2C shows an opening defined by a
10 photoresist mask 66, correct?

11 A. Which figure?

12 Q. Figure 2C.

13 A. So -- so can you repeat the question
14 again.

15 Q. Sure.

16 Figure 2C shows an opening defined by a
17 photoresist mask 66, correct?

18 A. Yes.

19 Q. Now, with reference to figure 2D, the
20 insulator layer 64 is etched using a photoresist
21 mask 66 as an etch barrier, correct?

22 A. So can you repeat the question --

23 Q. Yes.

24 A. -- for me.

25 Q. With reference to figure 2D, the

1 insulator layer 64 is etched using the photoresist
2 mask 66 as an etch barrier, correct?

3 A. Yeah.

4 Q. According to the '997 patent, the
5 conformal nitride layer 62 serves as an etch stop
6 during the etch of insulator 64, correct?

7 A. Yes.

8 Q. After the etch of the insulator layer 64,
9 the conformal nitride layer 62 is anisotropically
10 etched, correct?

11 A. Yes.

12 Q. During the anisotropic etch of the
13 conformal nitride layer 62, is the oxide layer 60
14 being etched as well?

15 A. Well -- yes, it -- I mean, afterwards,
16 it's in column 3, line 23 to -- 20 -- 23 to 24.
17 It's right here.

18 It's the thin oxide 60 is removed by
19 HF solution to expose the diffusion region 58.

20 Q. But the oxide 60 is not etched by the
21 nitride anisotropic edge, correct?

22 MR. CHEN: Objection to form.

23 THE DEPONENT: The nitride that -- you
24 mean the nitride 62 -- to etch nitride 62?

25 Q. (By Mr. Colaianni) The -- the ox- --

1 oxide 60 is not etched by the nitride anisotropic
2 etch for -- that etches nitride 62, correct?

3 MR. CHEN: Objection to form.

4 THE DEPONENT: Well, when you etch
5 nitride 62, it's possible that you remove little
6 bit of the oxide layers. But to fully clear this
7 area, it require this etch solution.

8 Q. (By Mr. Colaianni) So the etch is
9 selective, correct?

10 A. The nitride etch is selective, but every
11 selective etch, it etch as a layer adjusts to the
12 slower rate. This is what it mean selective. It's
13 not a -- it does not etch them at all. Just etch
14 it much smaller rate.

15 Q. I'm sorry. I just want to make sure I
16 understand what you said.

17 What -- what -- the what -- which rate?

18 A. So, see, when you do -- when you have
19 etch, which is selective, it means that you etch
20 the layers that you are trying to etch. It -- it's
21 certain control rated. You want to have it to be
22 fast and controllable and so on. But when you go
23 through this layer and you reach the layer
24 underneath it, it also etch the layer underneath
25 it. It just etch it at a lower rate than you etch

1 the one which you intended to etch.

2 Q. Without the oxide layer 60, the
3 anisotropic etch of the conformal nitride layer 62
4 would etch the diffusion region 58, correct?

5 A. Well, unless you -- it's -- again, you
6 have selectively with the nitride and the silicon.
7 So when you etch the layer 60, you -- you still --
8 what I'm saying, if you don't have the layer 60, so
9 when you etch the nitride layer 62, you still would
10 be able to stop on the silicon. You likely can
11 damage it if you go for too long. But if you have
12 one controlled process, you would be able to manage
13 it. But this is part of the reason why you have
14 layer 60 there.

15 Q. What is a typical selectivity between the
16 etch of silicon nitride and silicon -- and
17 silicon -- well, strike that. Let me -- let me
18 start over. That's --

19 What is the typical -- what is a typical
20 selectivity be- -- between etch of the silicon
21 nitride and the silicon for this anisotropic etch?

22 A. I mean, it could be greater than 5 to 1.
23 I mean, it could be 10 to 1, or maybe more. These
24 are the kind of numbers that you can see.

25 Q. Now, according to the '997 patent, after

1 the conformal nitrate etch, the oxide layer 60 is
2 removed by HF solution to expose the diffusion
3 region 58, correct?

4 A. Correct.

5 Q. Okay. So looking at figure 2D, a
6 sidewall spacer 62A is formed after the anisotropic
7 etch of the conformal nitride layer 62, correct?

8 A. Yes.

9 Q. So the material, the sidewall spacer 62A,
10 is nitride, correct?

11 A. Yes.

12 Q. The sidewall spacer 62A is not etched
13 away by the conformal nitride etch because the etch
14 is anisotropic, correct?

15 A. Yes.

16 Q. According to the '997 patent, the silicon
17 nitride layer 62 preferably has a thickness of
18 about 100 to 500 angstroms, correct?

19 A. Yes, it's double range. They are talking
20 1 to 500 or 200 to 350 preferably.

21 Q. The sidewall nitride would not be
22 completely etched away when the thickness of the
23 silicon nitride layer is 100 angstroms, correct?

24 A. Correct.

25 Q. According to the '997 patent, an

1 anisotropic etch would not completely etch away the
2 nitride sidewall 62A, correct?

3 MR. CHEN: Objection. Form.

4 THE DEPONENT: Can -- can you repeat this
5 question.

6 Q. (By Mr. Colaianni) Sure.

7 According to the '997 patent, an
8 anisotropic etch would not completely etch away the
9 nitride sidewall 62A, correct?

10 MR. CHEN: Objection to form.

11 THE DEPONENT: Yeah. It treats spaces.

12 Q. (By Mr. Colaianni) The '997 does not
13 disclose any process parameters for the anisotropic
14 etch, correct?

15 A. Correct.

16 Q. So as long as the etch process for the
17 silicon nitride layer 62 is anisotropic, the
18 sidewall nitride film would not be completely
19 etched away after the silicon nitride etch,
20 correct?

21 MR. CHEN: Objection to form.

22 THE DEPONENT: Yeah, as long as it use a
23 typical nitride etch process anisotropic.

24 Q. (By Mr. Colaianni) What do you mean by
25 "typical" in your answer?

1 A. So similar when a -- the vendor -- they
2 provide you different processes that you can use
3 for your equipment. So when you use this
4 processes, you get certain characteristics because
5 you want to have process that is controlled and
6 there is not too much variability and so on.

7 Q. Do you believe there are some anisotropic
8 etch processes that would -- that would completely
9 remove the sidewall spacers?

10 A. That would completely remove? It's -- I
11 mean, it would -- it depend on the -- the height of
12 the structure that you're trying to -- that you
13 make the space -- because the taller the structure
14 is the -- I mean, the more have -- the spacer would
15 be. So it would be harder to fully remove it.

16 And it's also a question of the nitride
17 thickness and the profile of the poly gate and the
18 layer 50 -- I mean, not 52 -- 54 and 56. So the
19 profile of all this combined structure, it create
20 the specific spacial shape.

21 And if you have the right spacial shape,
22 then it will be hard to fully remove it during an
23 anisotropic etch.

24 Q. Okay. So just to tie this together.

25 A. Sure.

1 Q. For the silicon nitrate layer 62 having a
2 thickness of 100 angstroms, as long as the etch
3 process for that layer is anisotropic, the sidewall
4 nitride film would not be completely etched by the
5 silicon nitride etch process, correct?

6 MR. CHEN: Objection to form.

7 THE DEPONENT: It's -- when you have a
8 certain other different layer thicknesses and
9 structure and using a specific process where you
10 have them -- the nitride layer that's really
11 preferably from 200 to 350, but you also can leave
12 if it's 100. Because I see it's in column 2,
13 paragraph -- it start at line 60 -- is talking
14 about this nitride layer thickness.

15 And then he's -- I mean, he's saying that
16 it's going to be all the way from 100, but he says
17 it's preferably from 200 to 350.

18 Q. (By Mr. Colaianni) But -- but the '997
19 patent discloses that if the nitride layer 62 is
20 100 angstroms, an anisotropic etch process would
21 not completely etch away the sidewall nitride film,
22 correct?

23 MR. CHEN: Objection to form.

24 THE DEPONENT: It's when you have the --
25 if you have the right combination of layer

1 thicknesses and gate thickness and the -- the
2 dielectric above the gate thickness, it create a
3 structure that wouldn't -- would remain there and
4 you wouldn't be able to -- I mean, the di- -- after
5 the anisotropic etch, it will remain there when you
6 have the combination of all these vials, layer and
7 profile together.

8 Q. (By Mr. Colaianni) But you agree there
9 are no process parameters associated with the
10 anisotropic etch disclosed in the '997 patent,
11 correct?

12 A. It doesn't provide the specific
13 parameter that you mentioned for the standard
14 anisotropic etch.

15 Q. So are you saying that if the silicon
16 nitride layer 62 is 100 -- 100 angstroms, there is
17 some anisotropic etch processes that would create a
18 space and some that would not?

19 A. No, I wasn't -- I mean, I was saying
20 that -- so, see, that he describe here -- this --
21 this structure already or all this several other
22 logic is very involved and it has many detail. And
23 all of them determine the structure and the shape
24 you can get it. And -- and especially when you
25 look at manufacturability that -- because every

1 variation for each of these layer, plus, minus
2 10 percent.

3 So he was saying that -- so you cannot
4 just say that if you have a nitride of 100
5 angstroms you always get space or you always don't
6 get space. You have to look at the situation.

7 And the situation that you have here is
8 that you have -- the space that you form here, it's
9 on the side of a gate. And the gate here it's
10 include them -- the layer in -- in 54 and 56. And
11 this specific structure, the shape of the sidewall
12 of it, will impact the shape of the spacer while
13 they doing the anisotropic etch. That's what I was
14 saying.

15 Q. So you were saying there would be
16 sidewall nitride film left after the etch; it's
17 just the shape that might vary, depending on the --
18 the etch parameters?

19 A. No. That -- I mean, the shape of the
20 structure that you put the nitride on would
21 determine the shape of the spacer. And this
22 together with the anisotropic etch could create --
23 I mean, would create the -- the spacer after you
24 finish the nitride etch.

25 Q. But a spacer would always remain after

1 the anisotropic etch, correct?

2 MR. CHEN: Objection to form.

3 THE DEPONENT: I mean, it would remain if
4 you have a posit it. You are a -- it's well
5 controlled so the shape of the structure that you
6 create in nitride is well controlled and you are
7 able to create the spacer then.

8 Q. (By Mr. Colaianni) But that -- that's
9 what the '997 patent is disclosing and claiming,
10 right?

11 A. For -- yeah. For a specific set of
12 circumstance, yeah.

13 Q. The -- the -- the patent is directed to
14 forming these sidewall spacers after anisotropic
15 etching, correct?

16 A. It's the wildest thing. I mean -- I
17 mean, if you look at the -- the claims is the same.
18 It describe forming a -- you have substrate and you
19 have a gate and diffusion and you put over the
20 barrier layers. And you put them in insulator
21 above it and you add to the opening an insulator.

22 And you use the barrier as a stoppage.

23 And then you add anisotropic, etch the barrier.

24 And you expose the diffusion and create the spacer
25 on the sidewalls.

1 Q. All -- all of the claims require forming
2 a spacer of the etch barrier material on the
3 sidewalls of the gate electrode, correct?

4 A. Yeah, it require forming a spacer on a
5 sidewall.

6 Q. And -- and the claims permit there to be
7 a barrier thickness of 100 angstroms, correct?

8 A. Yes. It's in -- claim 5 mentioned the --
9 the barrier thickness could be all the way down to
10 100.

11 Q. So -- so the patents are requiring there
12 to be a spacer formed on the sidewall of the gate
13 electrode after anisotropic etching, correct?

14 A. It require a spacer remaining there,
15 yeah.

16 Q. So as long as the conditions in claim 1
17 are met, a spacer would be formed by the
18 anisotropic etch, correct?

19 MR. CHEN: Objection to form.

20 THE DEPONENT: I mean, for -- if the
21 condition made to claim 1 -- I mean, it is
22 discussed what is patented by the '997.

23 Q. (By Mr. Colaianni) Right.

24 And that includes the formation of a
25 spacer after anisotropic etching, correct?

1 A. Yeah, the '997 requires a spacer be
2 formed during the anisotropic's etch of the
3 barrier.

4 Q. And claim 1 does not -- strike that.

5 The claims do not specifically define
6 process parameters for the anisotropic etch,
7 correct?

8 A. Yeah, it doesn't describe the process
9 parameters for the etch.

10 Q. Let's turn our attention to Exhibit 11,
11 which is the Doshi prior art reference, and let's
12 start with figure 3A of the Doshi reference.

13 Do you have figure 3A in front of you?

14 A. Yes, I do.

15 Q. Figure 3A shows gate structures labeled
16 10, correct?

17 A. Yes.

18 Q. The gate structures 10 are formed as
19 layered structures, including a polysilicon layer
20 22 and contact with gate oxide 8. Tungsten
21 silicide layer 24 overlying the polysilicon layer.
22 And a silicon nitride layer 26 overlying the
23 tungsten silicide layer, correct?

24 A. Yes, I believe so. It's -- let me try to
25 see what's in the description here.

1 So this is -- okay.

2 Q. And do you agree that gate oxide 8 is an
3 insulator?

4 A. Yeah, gate oxide 8 is an insulator.

5 Q. And do you agree that polysilicon layer
6 22 is a semiconductor?

7 A. Yes.

8 Q. Tungsten silicide layer 24 is a
9 conductor, correct?

10 A. Yes.

11 Q. Silicon nitride layer 26 is an insulator,
12 correct?

13 A. Yes.

14 Q. According to the Doshi reference, the
15 polysilicon layer 22, the tungsten silicide layer
16 24 and the silicon nitride layer 26 are deposited
17 by C -- CVD and then they're -- then are etched to
18 form the gate structures, correct?

19 A. Yes.

20 Q. And at this point, the gate oxide 8 is
21 not etched, correct?

22 A. Yes. It's describing in column 7 and 8
23 here. Is column 7 starting from line 30 -- I guess
24 40, and goes to line 52 -- 51 and 52 in column 7.

25 Q. Figure 3A also shows source drain

1 extensions 6 prime and 7 prime, correct?

2 A. Yes.

3 Q. According to Doshi, the source drain
4 extensions 6 prime and 7 prime are formed in a
5 self-aligned manner relative to gate structures 10,
6 correct?

7 A. Yeah.

8 Q. When Doshi discloses that light
9 reach-through implants are performed, that means
10 the implants pass through the gate oxide 8 into the
11 substrate to define the source drain extensions 6
12 prime and 7 prime, correct?

13 A. Yeah. This is before they form the
14 filament 11.

15 Q. For the region where the source drain
16 extensions 6 prime and 7 prime are defined, there
17 is no other layer on top of the gate oxide 8,
18 correct?

19 A. Well, I mean, they -- certain areas of
20 the -- the polysilicon and the silicide and the
21 nitride which are -- which are the gate, and you
22 have the gate oxide underneath it and you have in
23 between them -- between the gates where you do the
24 source drain implant. I mean, you do the -- the
25 reach -- what you call "reach-through" the lightly

1 doped portion of the source gate.

2 Q. But -- but just in the regions where the
3 6 prime and 7 prime are formed, there's -- there's
4 nothing on top of the gate oxide 8, correct?

5 A. There's nothing on top of the -- on the
6 gate when he does the -- when he do the implant for
7 the region, which -- now the prime region 6 and 7.

8 I notice above the region, it should be
9 later the source drain 8, 7 and 6.

10 Q. Figure 3A shows side filaments 11,
11 correct?

12 A. Yes.

13 Q. And the side filaments 11 are formed
14 after the definition of the source drain extension
15 6 prime, 7 prime, correct?

16 A. Yes.

17 Q. According to an embodiment of Doshi, the
18 sidewall filaments 11 are formed by first oxidizing
19 the sides of polysilicon layer 22, correct?

20 A. Yes. Yes.

21 Q. The oxidation states -- strike that.

22 The oxidation of the sides of polysilicon
23 layer 22 is performed through thermal oxidation,
24 correct?

25 A. It don't state that you can -- because I

1 think it's mentioned in column 7, in line 58 and
2 59. It's not stated.

3 Q. Would thermal oxidation be a well-known
4 way of forming the oxidation on the sides, to a
5 person skilled in the art?

6 A. You can use it, but thermal oxidation is
7 a process that -- it's more valuable and it's --
8 take longer time and it -- you have also -- so,
9 see, that for each of the processes you have a
10 limited thermal budget of -- for how long you can
11 get away from higher temperature. And so you're
12 trying to minimize the amount that you spend at
13 high temperature; because each high-temperature
14 step diffuse the dopant in a subset more, it could
15 cause more defect.

16 So this is why people prefer to use
17 rapid-thermal annealing or rapid-thermal processing
18 because it's a faster process and you spend less
19 time at the high temperature. And so it's more
20 commonly used process for...

21 Q. But thermal oxidation was a well-known
22 process at the time of the --

23 A. Yeah, it was --

24 Q. -- '997 patent, correct?

25 A. It was a known process. It was a

1 well-known process, but people more shifted to
2 rapid-thermal because it's more controllable,
3 faster throughput.

4 Q. During the oxidation of the sides of the
5 polysilicon layer 22 in figure 3A, the gate oxide
6 over the regions where the source drain extension 6
7 prime and 7 prime are defined would also be exposed
8 to oxidation, correct?

9 A. Well, you have oxide layer, oxide 8.

10 Q. But that oxide layer 8 would be exposed
11 to further oxidation, correct?

12 A. It's -- I mean, it's a short process and
13 the polysilicon oxidize faster, and it's not likely
14 that the -- you will create more oxide when you
15 have already oxide layer 8 on the substrate there
16 which are the extension.

17 If you go -- and you don't want to have
18 this process too long anyhow because you just want
19 to cover the edge of the polysilicon gate with a
20 oxide layer, so it's -- it's a different case.

21 Q. Well, but -- but during the oxidation of
22 the sides of the polysilicon layer, that gate oxide
23 region 8 would be exposed to further oxidation
24 then, correct?

25 A. The top of the oxide is exposed, but the

1 bottom of it, it's covered by all this layer of
2 oxide and it's a short process. So it's not likely
3 to oxidize further. But the polysilicon of the
4 grain boundary which oxidize very fast and as each
5 grain -- I mean, as each grain bother to get
6 oxidized, the grain -- similar like what I was
7 describing earlier, that it's well-known properties
8 in some material science that when you have
9 three-dimensional structure open, you can have --
10 the process could happen much faster because it
11 could happen from every direction, from
12 three-dimensional.

13 So the polysilicon -- as you oxidize the
14 grain boundary, each grain get more exposed and get
15 attacked from every direction, so it would be much
16 faster that oxidation will happen. And it's not
17 likely when you have a flat surface on the
18 substrate of on oxide already existing to be able
19 to oxidize through it.

20 Q. But -- but it would be exposed oxidation.
21 That -- that's all I was asking.

22 A. Right. I mean, to be -- to be -- the
23 surface of layer 8 of the gate oxide would be not
24 covered during this step between the gate 22 --
25 between the various gate 22.

1 Q. And so, therefore, it would be exposed to
2 oxidation?

3 A. It will expose surface, yeah, the top of
4 the oxide layers.

5 Q. According to the Doshi reference, after
6 oxidizing the sides of the polysilicon layer 22, a
7 layer of silicon nitride is deposited overall,
8 correct?

9 A. Are you referring for the -- when he is
10 creating the filament, or are you talking on a
11 later step?

12 Q. Correct, with respect to the creation of
13 the filament.

14 A. So, yes, I think he put a layer of
15 nitride over all. It's -- it's in column 7,
16 line 59 through 62, that he describe -- he create
17 the filament on the sidewalls.

18 Q. And then the silicon nitride is etched
19 anisotropically to remove the silicon nitride from
20 flat surfaces, leaving sidewall filaments 11
21 behind, correct?

22 A. Yes.

23 Q. The sidewall filaments 11 are used as an
24 implant barrier to define source drain regions
25 6 and 7 in a self-aligned manner, correct?

1 A. Yeah. It's one of the -- one of the
2 reasons that use -- at that point, use them for
3 this, yeah.

4 Q. Following the formation of the source
5 drain regions 6 and 7, the gate oxide layer 8 is
6 removed overall except from under the gate
7 structures 10, correct?

8 A. Yes. Column 8, it goes all the way from
9 column 7 and -- 66 to column 8, line 7.

10 Q. Okay. Could you please turn the page to
11 figure 3B of the Doshi reference.

12 A. Okay.

13 Q. In referring to figure 3B, this shows a
14 nitride layer 30 deposited overall, correct?

15 A. Yeah. It's -- it's -- it's covering
16 the -- all the various structures that deposit
17 layer 30.

18 Q. Figure 3B shows the nitride layer 30 is
19 conformal to the gate structures 10, correct?

20 A. Yes. It's sitting along the edges of --
21 covering the gate structure 10 along its edges.

22 Q. And according to Doshi, the thickness of
23 the nitride layer 30 can range from 65 to
24 250 angstroms, correct?

25 A. Yeah, I believe so. I think he mentioned

1 thickness.

2 Yeah, it's in column 8, in line 20, that
3 it ranges from 65 to 250.

4 Q. If you turn over to figure 3C, please.

5 Referring to figure 3C, this shows a BPSG
6 layer 14, correct?

7 A. Yes.

8 Q. And if you turn to figure 3D, figure 3D
9 shows that the BPSG layer 14 is planarized,
10 correct?

11 A. Yes.

12 Q. Turning to figure 3E, this shows that a
13 photoresist layer 32 has been patterned to define
14 plug contact openings labeled PC, correct?

15 A. Yes.

16 Q. Then turning over to figure 3F, figure 3F
17 shows that the BPSG layer 14 has been etched until
18 the nitride layer 30, correct?

19 A. I think it's described in column 9, I
20 think. Well, column 9 is -- I mean, it's partially
21 in column, because it describes in -- and it goes
22 to 3E -- M.

23 Well, it gets describes -- so I guess
24 it's -- yes. Column 9, line 34 to 55, at least to
25 57 or so.

1 Q. The nitride layer 30 is acting as an etch
2 stop layer in this BPSG etch, correct?

3 A. Well, it's -- it's etch -- I mean, it's a
4 diffusion barrier. They discuss quite a bit that
5 the reason that they put these layers as a
6 diffusion barrier and intentionally we want to make
7 it fairly similar.

8 So this is why he is using layer that --
9 from 65 to 250 angstroms. It's discussed -- yeah,
10 in column 8, line 20 and 19. So it says that
11 layer 30 present a good barrier to dopant
12 diffusion, and the thickness may range from 65 to
13 250, and so on.

14 Q. But the nitrate layer 30 is acting here
15 as an etch stop, correct?

16 A. Not exactly. It's a different material,
17 so it's -- so it's actually a different rate
18 somewhat, but -- but it's -- the main purpose of it
19 is the diffusion barrier.

20 So the BPSG he's talking about having
21 void for the BPSG, if you don't -- because people
22 used to use an oxide underneath the BPSG, and it
23 was void by the diffusion of dopant out of the
24 BPSGs and affecting the source of the fusion. And
25 if you first for diffuse out of the BPSG, then you

1 can even create void in the BPSG. So the main
2 function of the layer 30 is to be a barrier --
3 diffusion barrier.

4 Q. But you would agree that the BPSG etch
5 stops at the nitride layer 30, correct?

6 A. Generally -- sorry.

7 Q. I -- I was just saying -- well, let me --
8 let me ask it again.

9 You would agree that the BPSG etch stops
10 at nitrate layer 30 in figure 3F, correct?

11 MR. CHEN: Objection to form.

12 THE DEPONENT: Well, I mean, from the
13 figure, it's impossible to know because -- I mean,
14 I don't know exactly because -- I mean, exactly
15 where the BPSG stop at the figure and where the
16 nitride -- it starts and just illustration in the
17 figure. And I mean that occurs in the figure, some
18 other figures, say.

19 Q. (By Mr. Colaianni) Well, take a look, if
20 you would, at column 9 of the patent --

21 A. Okay.

22 Q. -- around line 50.

23 A. Okay.

24 Q. And Doshi is disclosing here that the
25 BPS -- SG etch will tend to stop at the nitrate

1 layer 30, correct?

2 A. Well, it tend to stop. It doesn't mean
3 always stop. And when you are dealing with million
4 transistor -- I mean, million contacts and -- it's
5 mostly millions. I mean, it's many millions cause
6 the die and cause the wafers. And sometime it will
7 stop and sometimes it will go a bit further.

8 Q. But the disclosure here relating to the
9 etch stopping at the nitrate layer 30 is consistent
10 with what is shown in figure 3F, which shows the
11 etch stopping at layer 30, correct?

12 MR. CHEN: Objection to form.

13 THE DEPONENT: Well, the figure 3F,
14 it's -- I mean, some other figure are not that
15 accurate and -- and like a -- if you look at 3F,
16 for example, the -- they have two opening PC. And
17 on the one -- the left one it shows that you have
18 BPSG all the way down to the bottom there. And so
19 it's not always -- I mean, that -- fully removed.
20 You see just example of the volubility maybe. That
21 is just what is trying to show in these pictures.

22 Q. (By Mr. Colaianni) Well, but -- but you
23 would agree that figure 3F does show the BPSG etch
24 stopping at layer 30, correct?

25 A. Well, I mean, because here on the -- the

1 PC on the left, it stop not at the layer 30, it --
2 it stops -- it's -- I mean, it's -- there's some
3 BPSG left and it's not just -- it stops before the
4 layer 30, so it's not really just on layer 30.
5 It's a timed etch.

6 Q. You -- you considered the entire
7 disclosure of Doshi, correct?

8 A. Yes, I did.

9 Q. So did -- did you -- did you look at the
10 abstract on the first page of Doshi?

11 A. Yes.

12 Q. And did you notice there that Doshi
13 characterizes the silicon nitride layer 30 as an
14 etch stop?

15 A. Well, he's -- if you look earlier, it is
16 considered a barrier to diffusion of boron and
17 phosphorous for the BPSG during the
18 high-temperature processes. And he has -- in many
19 places he describes how it serves as the barrier to
20 diffusion. And he described -- I mean, in his
21 abstract, that the reason why he shifted from using
22 an oxide to nitride, it's because as the device
23 becomes smaller, the oxide -- having an oxide as a
24 barrier beneath the BPSG was problematic. And so
25 this is why he shifted to nitride. And he just

1 use -- to be able to miniaturize the process
2 further, this is why he use such a thin layer of
3 nitride. It would still be a good barrier for
4 diffusion.

5 Q. Well, in addition to serving as a barrier
6 to the diffusion, it also serves as an etch -- etch
7 stop there, correct?

8 A. It's -- I mean, it's a side benefit that
9 is sometimes good, but -- I mean -- but if you read
10 the detailed description, he doesn't say will stop.
11 It says will tend to stop. That's -- if you look
12 at the word include "tend," it means that with the
13 variability it wouldn't totally stop.

14 Also, if you look at the figure, it show
15 clearly, you know, this figure, that he doesn't
16 always remove all the BPSG. If you look, you have
17 two PC opening: The left PC opening; on the right
18 side of it, you have BPSG remaining all the way
19 down.

20 Q. And -- and you're referring to figure 3F?

21 A. 3F, 3G. But, yeah, starting from 3F.
22 Let me see. Yeah, starting from 3F.

23 Q. But in figure 3F, the BPSG etch stops at
24 the nitride layer 30, right?

25 A. But not everywhere that -- so, see, this

1 is just cross-section. So if you look at the
2 contact opening on the left that -- this opening is
3 two sides. The left side of it, you remove the
4 BPSG and you don't know whether it stopped at the
5 30 or removed part of layer 30. But it look --
6 he's in layer 30, let's say. But on the right
7 side, you still have BPSG left on the same contact.

8 Q. But the etch stops in figure 3F at the
9 bottom of the etch when it reaches the nitrate
10 layer 30, correct?

11 A. It tend to stop, the way he describes it.

12 Q. Well, figure 3F shows it stopping there,
13 correct?

14 A. No, because you don't know how much of
15 the starting thickness of layer 30 and how much you
16 see there. In several of the figure, like 3G and
17 3K and L -- no, sorry 3 -- 3G and 3 -- 3G and 3J
18 and L even.

19 Q. But there is remaining -- there was a
20 portion of the nitrate layer 30 remaining in the --
21 after the BPSG etch in figure 3F, correct?

22 A. It looks that there is remaining portion,
23 yeah.

24 Q. It -- it -- it's shown in the figure,
25 correct? It's labeled 30?

1 A. Yeah, but this is to contact out of many
2 that you produce.

3 Q. And the -- and the reference describes
4 layer 30 as an etch stop in the abstract, correct?

5 A. It's found in the description in the
6 abstract. He also describe it as -- which is the
7 key one -- that is for the diffusion barrier and he
8 describe how to remove -- how he used to have an
9 oxide layer before this diffusion barrier and now
10 he use the nitride as a diffusion barrier.

11 Q. Right.

12 The silicon nitride layer serves as a
13 diffusion barrier and as an etch stop, as described
14 in the abstract, correct?

15 A. He's saying that the etch is a two-step
16 etch process. So he's saying that he -- I mean,
17 that when you look at the full description in the
18 specifications, it -- he tend to stop there, but
19 not always.

20 Q. Well, just looking at the abstract,
21 though, you would agree with me that it says that
22 silicon nitride layer 30 serves as an etch stop.

23 That's what it says, right?

24 A. I mean, the abstract is six line -- or I
25 don't know how many line -- 10 lines. And it's --

1 and then he has a description of quite a few pages
2 and, you know, 11 -- 11 columns and go with figure
3 up to K. So there are a lot of details that you
4 cannot describe when you mention 10 lines.

5 Q. But -- but you would agree with me,
6 though, that the silicon nitride layer 30 is
7 referred to as a etch stop in the abstract,
8 correct?

9 A. It mentions that it -- it -- first
10 etch then is selectively etched to silicon oxide
11 relative to the nitride and -- but then he -- I
12 mean, it -- yeah, it says that it -- but when you
13 go in more detail, he says that he tend to stop
14 there. If he felt that it always stop there, he
15 wouldn't use the word "tend."

16 Q. So is it your testimony that the silicon
17 nitrate layer 30 does not serve as an etch stop?

18 MR. CHEN: Objection to form.

19 THE DEPONENT: Not exactly. I'm saying
20 that -- so, see, in all this process you have
21 variability. And when he does the etch, he often
22 is able to stop there, but he doesn't always stop
23 there. And so it doesn't fully service in always
24 being able to stop and not having any issue.

25 Q. (By Mr. Colaianni) But in some instance,

1 the silicon nitride layer 30 can and does serve as
2 an etch stop as described in the patent, correct?

3 A. In some -- as it said in the patent, in
4 some instance, it stops at layer 30. In other
5 instance, it doesn't. So this is why you use the
6 word "tend."

7 Q. Well -- well, the patent doesn't say that
8 in some instances the nitride layer 30 serves as an
9 etch stop, does it?

10 A. The patent says it -- it tend to serve as
11 an etch to stop on the nitride 30. It's in line --
12 whatever -- 50.

13 Q. So you would agree that the reference --
14 strike that.

15 You would agree the Doshi reference does
16 disclose the silicon nitride layer 30 as serving as
17 an etch stop?

18 A. Yeah, but you put the qualifiers that it
19 tend to serve. It -- it tend to stop on nitride
20 layer 30.

21 Q. But the way it's described in the figures
22 and the abstract shows that it can and does serve
23 as an etch stop, correct?

24 A. The figure -- just for illustration --
25 the more detailed description are in the

1 specification. And this where he describe why he
2 use a certain layer and he tell you why he does the
3 etch, and he tell you the etch work a lot of the
4 time. But it just tend to do it, to stop on the
5 nitride.

6 Q. Can you show me anywhere where Doshi says
7 that the nitride layer does not serve as an etch
8 stop?

9 A. Well, I mean, when you use the word
10 "tend" to a person of the ordinary skill in the
11 art, you have to understand that you have the
12 reliability in the process, and this way to have
13 such -- such a short -- such a short -- I mean,
14 such a timed etch and -- and so he understand it
15 would stop a lot of time there, but not every time
16 that you have a perfectly stopping exactly when you
17 reach the nitride and so on.

18 Q. So you'd agree there is at least -- at
19 least a disclosure that in -- in most instances,
20 silicon layer 30 will act as an etch stop?

21 A. In a lot of the -- in a lot of the cases,
22 but you have a variability, so it's -- in each die,
23 so -- but in a lot of the cases, he stops there,
24 yeah.

25 Q. Okay. Now, returning to the figures in

1 Doshi, the nitride layer 30 that is formed over the
2 source drain region 7 is then etched using a brief
3 and highly anisotropic etch, correct?

4 A. Yes. Yeah.

5 Q. And according to Doshi, the thickness of
6 the nitride layer 30 may range from 65 to
7 250 angstroms, correct?

8 A. Yeah, I believe so.

9 Yeah, it's in column 8, line 20.

10 Q. So that means the thickness of the
11 nitride layer 30 could be 100 angstroms, correct?

12 A. Yes, it could be 65, 75, 100, 250.

13 Q. And according to the '997 patent, the
14 silicon nitride layer 62 preferably has the
15 thickness of about 100 to 500 angstroms, correct?

16 A. Yes.

17 Q. And in the '997 patent, when the silicon
18 nitride layer 62 has a thickness of 100 angstroms,
19 as long as the etching process is anisotropic, the
20 sidewall nitride film would not be completely
21 etched away, correct?

22 MR. CHEN: Objection to form.

23 THE DEPONENT: Yeah, it -- it wouldn't be
24 completely etched away when that specific
25 structures shows in the '997 patent.

1 MR. COLAIANNI: Let's take a short break.

2 MR. CHEN: Sure.

3 (Discussion off the stenographic record.)

4 THE VIDEOGRAPHER: This marks the end to
5 DVD No. 3 in the videotaped deposition of
6 Ron Maltiel. The time is 4:12 p.m. and we are off
7 the record.

8 (Recess taken.)

9 THE VIDEOGRAPHER: This marks the
10 beginning to DVD No. 4 in Volume 1 of the
11 deposition of Ron Maltiel. The time is 4:33 p.m.
12 and we are on the record.

13 Q. (By Mr. Colaianni) Looking back at
14 figure 3G of the Doshi prior art reference --

15 A. Uh-huh.

16 Q. -- there is shown in figure 3G the result
17 of a highly anisotropic etch process, correct?

18 A. I mean, there is each other -- it's --
19 basically it's -- the process of the device when
20 they reach this point in the -- in -- so it's in
21 column 9, he describes the steps that happens
22 when -- when you reach -- talking about -- column
23 9, line 56.

24 But there is -- actually at the bottom of
25 65, he says it -- when he's done how it -- when you

1 complete both etch steps and you remove the
2 photoresist 32, how it looks like.

3 Q. The -- strike that.

4 Portions of the silicon nitride layer 30
5 are removed through the highly anisotropic etch, as
6 shown in figure 3G, correct?

7 MR. CHEN: Objection to form.

8 THE DEPONENT: Yeah, in 3G it shows that
9 when you finish these two etch steps, he's able to
10 reach the substrate to make contact there.

11 Q. (By Mr. Colaianni) And after the highly
12 anisotropic etch portions of the silicon nitrate
13 layer 30 remain as shown in figure 3G, correct?

14 MR. CHEN: Objection to form.

15 THE DEPONENT: Right. I mean, after
16 the -- after he does the two-step etch, the first
17 one to remove the BPSG 14 and the second one,
18 remove the layer 30, he is able to reach the
19 contact arranging 7 to make contact with the PC
20 contact in figure 3G.

21 Q. (By Mr. Colaianni) But figure 3G shows
22 portions of the silicon nitride layer 30 that
23 remain after the anisotropic etch, correct?

24 A. Figure 3G is not accurate because it
25 doesn't show any impact of the nitride etch on

1 layer 30 on the side of the contact.

2 For example, the original which is NC --
3 that is -- shows it's -- it should -- it should be
4 quite a bit etched following the nitride portion of
5 the section. It still doesn't show it.

6 Q. You believe figure 3G is not accurate?

7 A. Yes.

8 Q. But you would agree that portion of
9 silicon nitride layer 30 would remain after the
10 highly anisotropic etch, correct?

11 MR. CHEN: Objection to form.

12 THE DEPONENT: It sometimes tend to
13 remain, but not always. They are -- they are
14 quoting -- forming them -- that they are other step
15 doesn't always stop there.

16 And also if you look for -- in summary,
17 in column 11 -- basically, column 11, line 22 to
18 40, he summarize of the overall process. And then
19 in the middle of it, he describes it -- what
20 happened to this underlying barrier, the diffusion
21 barrier. So this is in line 32 it start.

22 It says, "Secondly, the underlying
23 nitride layer enables the use of a two-step etch"
24 process "for which an etch stop is provided for the
25 first, oxide etch, step, but also in which the

1 etching of the nitride layer may be performed in
2 such a manner as to not damage any exposed sidewall
3 filaments."

4 So it basically shows that he realize
5 that due to the variability of the process, you
6 sometimes remove this nitride 30 in -- it's also
7 serve its function as this diffusion barrier, but
8 you want to make sure you don't damage the filament
9 underneath it. So it's -- basically, he's showing
10 that this step is mainly used as a diffusion
11 barrier and they are serving its purpose.

12 Q. (By Mr. Colaianni) But you would agree
13 that figure 3G shows a portion of the silicon
14 nitride layer 30 that remains after the anisotropic
15 etch process, correct?

16 MR. CHEN: Objection to form.

17 THE DEPONENT: It -- it sounds -- it
18 shows that it remain, but it has an inaccuracy
19 about the description of this layer 30 in this
20 figure 3G, so you cannot -- there's too many
21 assumption on the exact detail of it because it
22 doesn't show that the layer 30 is impacted at all
23 by the nitride etch on the side of the gate 24 and
24 22, and on the side above the filament, maybe
25 around the filament.

1 Q. (By Mr. Colaianni) Correct.

2 Figure 3G -- 3G shows that the layer 30
3 is not impacted by the anisotropic etch along the
4 sidewall, correct?

5 A. Yes. It...

6 MR. COLAIANNI: Okay. I don't think I
7 have any other questions for this IPR.

8 MR. CHEN: Okay. Take a quick break.
9 Let me review my notes to make sure.

10 MR. COLAIANNI: Okay.

11 THE VIDEOGRAPHER: The time is 4:41 p.m.
12 and we are off the record.

13 (Recess taken.)

14 THE VIDEOGRAPHER: The time is 4:59 p.m.
15 and we are back on record.

16 This concludes today's deposition of
17 Mark -- of Ron Maltiel and marks the end of DVD
18 No. 4 of 4. The time is now 4:59 p.m. and we are
19 off the record.

20 (Deposition adjourned at 4:59 p.m.)

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25

1 I, RON MALTIEL, do hereby declare under
2 penalty of perjury that I have read the foregoing
3 transcript; that I have made any corrections as
4 appear notes; that my testimony as contained
5 herein, as corrected, is true and correct.

6 Executed this ____ day of _____,
7 2015, at _____, _____.

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RON MALTIEL

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1 STATE OF CALIFORNIA) ss:
2 COUNTY OF CONTRA COSTA)

3

4 I, Rebecca L. Romano, CSR. 12546, do hereby
5 certify:

6 That the foregoing deposition testimony was
7 taken before me at the time and place therein set
8 forth and at which time the witness was
9 administered the oath;

10 That the testimony of the witness and all
11 objections made by counsel at the time of the
12 examination were recorded stenographically by me,
13 and were thereafter transcribed under my direction
14 and supervision, and that the foregoing pages
15 contain a full, true and accurate record of all
16 proceedings and testimony to the best of my skill
17 and ability.

18 I further certify that I am neither counsel
19 for any party to said action, nor am I related to
20 any party to said action, nor am I in any way
21 interested in the outcome thereof.

22 IN WITNESS WHEREOF, I have subscribed my name
23 this 11th day of November, 2015.

24

25

Rebecca L. Romano, RPR,
CSR. No 12546

1

DEPOSITION ERRATA SHEET

2

Case Name: Samsung Electronics Co., Ltd, et al vs.
Home Semiconductor Corporation

3

Name of Witness: Ron Maltiel

Date of Deposition: November 9, 2015

4

Job No. : 110916-RRH

Reason Codes: 1. To clarify the record.

5

2. To conform to the facts.

3. To Correct transcript errors.

6

Page _____ Line _____ Reason _____

7

From _____ to _____

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Page _____ Line _____ Reason _____

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From _____ to _____

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Page _____ Line _____ Reason _____

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From _____ to _____

12

Page _____ Line _____ Reason _____

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From _____ to _____

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Page _____ Line _____ Reason _____

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From _____ to _____

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Page _____ Line _____ Reason _____

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From _____ to _____

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Page _____ Line _____ Reason _____

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From _____ to _____

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Page _____ Line _____ Reason _____

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From _____ to _____

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Page _____ Line _____ Reason _____

23

From _____ to _____

24

Page _____ Line _____ Reason _____

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From _____ to _____

1

DEPOSITION ERRATA SHEET

2

Page ____ Line ____ Reason _____

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From _____ to _____

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Page ____ Line ____ Reason _____

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From _____ to _____

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Page ____ Line ____ Reason _____

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From _____ to _____

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Page ____ Line ____ Reason _____

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From _____ to _____

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Page ____ Line ____ Reason _____

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From _____ to _____

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Page ____ Line ____ Reason _____

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From _____ to _____

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Page ____ Line ____ Reason _____

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From _____ to _____

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Page ____ Line ____ Reason _____

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Page ____ Line ____ Reason _____

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Page ____ Line ____ Reason _____

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From _____ to _____

22

____ Subject to the above changes, I certify that

23

the transcript is true and correct

24

____ No changes have been made. I certify that

25

the transcript is true and correct.

RON MALTIEL