

1 UNITED STATES PATENT AND TRADEMARK OFFICE
2 BEFORE THE PATENT TRIAL AND APPEAL BOARD

3
4 SAMSUNG ELECTRONICS CO. LTD,
5 SAMSUNG ELECTRONICS AMERICA, INC.,
6 SAMSUNG SEMICONDUCTOR, INC., and
7 SAMSUNG AUSTIN SEMICONDUCTOR, LLC.

8 Petitioner

9 vs.

10 HOME SEMICONDUCTOR CORPORATION

11 Patent Owner

12 Case IPR2015-00459 Patent 6,150,244
13 Case IPR2015-00460 Patent 6,146,997
14 Case IPR2015-00466 Patent 6,030,893
15 Case IPR2015-00467 Patent 6,030,893

16 VIDEO DEPOSITION OF RON MALTIEL

17 Redwood City, California

18 November 10, 2015

19 VOLUME II (Pages 195 - 287)

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23 Reported by:

24 Rebecca L. Romano,

25 RPR, CSR No. 12546

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16
17 Video Deposition of Ron Maltiel, taken on
18 behalf of the Petitioner, Fish & Richardson, P.C.,
19 500 Arguello Street, Suite 500, Redwood City,
20 California, beginning at 9:29 a.m.,
21 November 10, 2015, before Rebecca L. Romano,
22 Certified Shorthand Reporter, No. 12546.
23
24
25

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2

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1 Redwood City, California, November 10, 2015

2 9:29 a.m.

3 ---o0o---

4

5 THE VIDEOGRAPHER: Good morning, Counsel.

6 Here begins Disc No. 1 to the Volume II

7 deposition of Ron Maltiel in the case captioned

8 "Samsung Electronics Company, Ltd.,

9 Samsung Electronics America, Incorporated,

10 Samsung Semiconductor, Inc., and Samsung Austin

11 Semiconductor, LLC, versus Home Semiconductor

12 Corporation."

13 Today's date is November 10th, 2015. The
14 time is approximately 9:29 a.m.

15 This deposition is being taken at
16 Fish & Richardson at 500 Arguello Street,
17 Suite 500, Redwood City, California 94063, and was
18 made at the request of the petitioner.

19 I'm Philip Knowles, the videographer, and
20 the court reporter is Rebecca Romano from
21 Gregory Edwards, LLC.

22 Counsel, please voice identify
23 yourselves.

24 MR. COLAIANNI: Joseph Colaianni of
25 Fish & Richardson, on behalf of the Samsung

1 petitioners.

2 MR. HSIEH: Andy Hsieh, Fish &
3 Richardson, on behalf of the Samsung petitioner.

4 MR. CHEN: Jerry Chen, TechKnowledge Law
5 Group for Home Semiconductor.

6 THE VIDEOGRAPHER: Will the court
7 reporter please swear in the witness again for
8 Volume II.

9 THE REPORTER: If you could raise your
10 right hand for me, please.

11 THE DEPONENT: (Complies.)

12 THE REPORTER: You do solemnly state,
13 under penalty of perjury, that the testimony you
14 are about to give in this deposition, shall be the
15 truth, the whole truth and nothing but the truth?

16 THE DEPONENT: I do.

17

18

19

20

21

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23

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25 /////

1 RON MALTIEL,
2 having been re-administered an oath, was examined
3 and testified further as follows:
4

5 (Exhibits 12, 13 and 14 were marked for
6 identification by the court reporter and are
7 attached hereto.)

8 EXAMINATION

9 BY MR. COLAIANNI:

10 Q. Good morning.

11 A. Good morning.

12 Q. Welcome back.

13 Today we are going to discuss the IPR
14 captioned "IPR 2015-00459," and I've had the
15 court reporter mark three exhibits for us.

16 The first one is Exhibit 12, and that is
17 the patent at issue, which is U.S. Patent
18 No. 6,150,244.

19 The second exhibit is Exhibit 13, and
20 that is your declaration submitted in this matter,
21 which was produced as HOME-2002.

22 And the third exhibit is Exhibit 14,
23 which is the prior art Nakamura U.S. Patent
24 No. 6,312,994 and was produced as SAMSUNG-1004.

25 Do you have Exhibits 12, 13 and 14 in

1 front of you?

2 A. Yes, I do.

3 Q. Okay. Let's start with Exhibit 14. This
4 is the Nakamura prior art reference.

5 You have considered the Nakamura prior
6 art reference as part of your analysis, correct?

7 A. Correct.

8 Q. And you're familiar with the Nakamura
9 reference?

10 A. Yes. Yes.

11 Q. Nakamura discloses a method of
12 fabricating a semiconductor device, correct?

13 A. Yes.

14 Q. One of the major goals of the Nakamura
15 reference is to provide a fabrication process
16 suitable for further micronization of a
17 semiconductor device, correct?

18 A. Yeah, using its -- his specific
19 construction of -- to make specific device
20 following his teaching.

21 Q. Another of the goals of the Nakamura
22 reference is to decrease the processing steps so as
23 to shorten the fabrication process and lower costs,
24 correct?

25 A. Yes. Yes. It's to do it while you

1 follow his teaching and for specific way to create
2 the structures, yeah.

3 Q. And people skilled in the art are always
4 looking for ways to shorten the fabrication process
5 and lower costs with respect to semiconductor
6 manufacture; is that fair?

7 MR. CHEN: Objection to form.

8 THE DEPONENT: Yes. Correct.

9 Q. (By Mr. Colaianni) Let's take a look at
10 the first embodiment disclosed in the Nakamura
11 reference, and this begins approximately column 9,
12 lines 25.

13 You reviewed this portion of the
14 specification, correct?

15 A. Correct.

16 Q. Nakamura describes here using an
17 isolation film 12 to define a device region 14,
18 correct?

19 A. Let me get together with the figures so I
20 would be sure that -- so it's -- okay.

21 Here in line 32, he's talking about
22 creating isolation film 12 on substrate 8.

23 Q. And the device region 14 is known as an
24 active region, correct?

25 A. Yes. Correct.

1 Q. And Nakamura also discloses the formation
2 of an insulation film labeled as 16, correct?

3 A. Correct.

4 Q. That insulation film 16 is a dielectric
5 layer, correct?

6 A. Yes.

7 Q. Nakamura then discloses depositing a
8 doped polysilicon crystal -- strike that.

9 Nakamura discloses depositing a doped
10 polycrystalline silicon film on top of the
11 insulation film 16, correct?

12 A. Yes. It's -- electrode 18, he call it.
13 It's on line 37 through 39.

14 Q. The doped polycrystalline silicon film is
15 a conductive layer, correct?

16 A. Correct.

17 Q. Nakamura then discloses depositing an
18 insulation film of silicon oxide, correct?

19 A. Are you talking about in layer 20?

20 Q. Well, I'm -- I'm referring to column 9 at
21 lines 39 and 40.

22 A. Yeah, that in the -- 39 and 40 is talking
23 about figure 1A and is referring to film 20 in
24 figure 1A.

25 Q. In the insulation film of silicon oxide

1 is a dielectric layer, correct?

2 A. Yes.

3 Q. So Nakamura describes forming a first
4 dielectric layer 16, first conductor layer 18 and a
5 second dielectric layer 20 on the substrate,
6 correct?

7 A. Yes.

8 MR. CHEN: Objection to form.

9 Q. (By Mr. Colaianni) With those layers
10 deposited, Nakamura describes patterning the layers
11 by lith- -- lithography and etching to form gate
12 electrodes, correct?

13 A. Yes. It is -- well, it's -- you said it
14 use the lithography and etching to form gate
15 electrodes that cover with insulation 20. So it
16 doesn't really describe when he deposited
17 insulation 20, but I guess you have to assume it's
18 done before. Okay.

19 Q. Figure 1A shows the resulting gate
20 electrodes after the patterning, correct?

21 A. Yes.

22 Q. And then Nakamura describes forming an
23 impurity doped region 22, correct?

24 A. Yes. This is in the next
25 paragraph starting from line 45, so 53 or so.

1 Q. And then Nakamura describes depositing a
2 silicon nitride film to form an etching stopper
3 film 24, correct?

4 A. Yes. He describe afterward that this is
5 in the paragraph 61 through 63, in figure 1B, that
6 they put film 24, which is the silicon nitride
7 formed by CVD, I guess.

8 Q. And that silicon nitride film 24 is a
9 dielectric layer, correct?

10 A. Yes, it's a dielectric.

11 Q. Nakamura then discloses an insulation
12 film deposited as the inter-layer insulation film,
13 correct?

14 A. Yes, this is in column 10, line 10
15 through 16. He's talking about figure 1C that he
16 deposits insulation at layer 26.

17 Q. And that insulation film 26 is another
18 dielectric layer, correct?

19 A. Yeah, it's a dielectric layer.

20 Q. Nakamura then describes planarizing the
21 insulation film 26, correct?

22 A. Yes. It's still in the
23 paragraph describing figure 1C that -- it's
24 column 10, line 10, so 16 or so. And they describe
25 that they planarize this insulation layer 26 to

1 create the structure shown in figure 1C.

2 Q. Nakamura then describes forming a
3 patterned photoresist 28, correct?

4 A. Yes. It's described a photoresist, as
5 shown in figure 2A, and he describe it in column 10
6 starting from line 17. So maybe all the way to 40.
7 Describe -- he create a pattern using the
8 photoresist.

9 Q. Nakamura next discloses that portions of
10 the inter-layer insulation film 26 are removed
11 through etching, correct?

12 A. Well, yeah. This is in the -- that he
13 remove them photoresist -- well, initially, he has
14 the photoresist 28, as shown in figure 2A. And
15 then he remove the photoresist and it continue the
16 etching, as shown in figure 2B.

17 Q. And through that etching, portions of the
18 insulation film 26 are removed, correct?

19 A. Both portion of 26 and also portion of
20 the 28 on top of the gate is thinned down. He has
21 something -- let me try to find it.

22 Q. Then Nakamura discloses --

23 A. Just a second. I was trying to find
24 where he describe it.

25 Q. Oh, I'm sorry.

1 A. So go ahead.

2 Q. Oh, okay. I thought you were --

3 A. No, no. I was trying to find something.

4 Q. Okay. Then the chemistry of the etch is
5 changed and portions of the etching stopper film 24
6 are removed by etching, correct?

7 A. This is after he removed the -- the
8 photoresist 28. Then he start -- I mean, then he
9 changed the etching process any further and
10 continued the etching where the layer of 26 is
11 exposed.

12 Q. And by that process removes portions of
13 the etching stopper film 24, correct?

14 MR. CHEN: Objection to form.

15 THE DEPONENT: Well, several things is
16 happening. He thinned down the layer 26 that was
17 underneath the mask 28. He removed portion of --
18 that portion that is above the gate 30.

19 Let me try to find it here in the -- the
20 declaration just for a second.

21 Q. (By Mr. Colaianni) Is there something
22 you're looking for specifically?

23 A. Well, it's the -- the -- the description
24 of -- that he remove the photoresist and he
25 continue etching. So it's separated and he does

1 initial etching, as shown in figure 2A, and then he
2 continued the etching in 2B.

3 And -- and the etching in 2B is done with
4 other photoresist mask.

5 Q. Okay. My -- my question was -- was,
6 specific, though.

7 I'm just asking, as part of the etching
8 process between figure 2A and 2B, portions of that
9 etching stopper film 24 are removed, correct?

10 A. It's -- it's removed, while at the same
11 time it's a process that is adjusted so you etch
12 the dielectric -- the third dielectric on top of
13 the gate at the same time that you etch the fourth
14 dielectric, which I guess is No. 26.

15 Q. Nakamura then discloses that the etching
16 process goes on until the silicon substrate 10 is
17 exposed in the regions for the source drain
18 diffused layer to be formed in the -- strike that.

19 Nakamura discloses that the etching
20 continues until the silicon substrate 10 is exposed
21 in the regions for the source drain diffused layer
22 to be formed in, correct?

23 MR. CHEN: Objection to form.

24 THE DEPONENT: It continue the etch using
25 this new edge chemistry, the one after you removed

1 the photoresist; that -- that you etch both sides
2 of the -- the -- the dielectric form that used to
3 be underneath the photoresist and dielectric 3 that
4 was not covered on photoresist, while you are going
5 through layer 24 trying to reach all the way to the
6 substrate.

7 Q. (By Mr. Colaianni) As part of the
8 etching, the etching stopper film 24 on the
9 sidewalls is not removed and remains the sidewall
10 insulation film 30 as well, correct?

11 A. Yes. While you are doing this etch, you
12 are defining the sidewall, but you have -- a
13 portion of it is -- is -- I mean, it -- it's done
14 while at the same time you have to have a very
15 specific etch chemistry that will be able to etch
16 both the dielectric 26 and the dielectric 30 at the
17 same time, so they -- the cup on top of the gate.
18 Outside gate gets sent down -- I mean, doesn't get
19 sent down too much relative to the dielectric
20 forms, while you're forming the shape of the
21 layer 30 on the side of the gate.

22 Q. Okay. So at the end of the etching
23 process described in Nakamura, contact holes 34 and
24 36 are created. The silicon substrate 10 is
25 exposed and sidewall insulation films 30 are

1 created on the gate electrodes, correct?

2 A. As a result of these two separate
3 operations that one use the photoresist and you
4 have the dielectric 26 and -- protected and the --
5 and then you remove the photoresist and you
6 continue the etch. You thin down the first
7 dielectric at the same time you remove the 20- --
8 layer 24 until you expose the original 34 and 36
9 and form spacer, while you're doing this two-step
10 operation or two- -- I mean the operation initially
11 with the photoresist and then with other
12 photoresist.

13 Q. The sidewall insulation film 30 are
14 spacers, correct?

15 A. The sidewall insulation film 30, yeah,
16 serve the function of a spacer.

17 Q. And the substrate 10 is exposed after the
18 etch, correct?

19 A. Yeah, the substrate get exposed after
20 this two-step or two-operation edge, one with the
21 photoresist and one with other photoresist.

22 Q. The contact holes 34 and 36 are trenches,
23 correct?

24 A. The -- say it again.

25 Q. The contact holes 34 and 36 are trenches,

1 correct?

2 A. Well, you form the trench while you --
3 see, the trenchers are created through this long
4 point -- combination of steps that you -- first you
5 create them and you have the mask 28, and as you go
6 through the etch, you deepen the trenches. And
7 then when you remove the mask, you continue etching
8 the form and deepening the trenches.

9 Q. In connection with the first embodiment,
10 Nakamura describes creating the source and drain
11 regions using ion implantation, correct?

12 A. Yes. I believe he use -- I -- yeah, he
13 use ion implantation to form the source light.

14 Q. And Nakamura also describes an
15 alternative to the use of ion implantation,
16 correct?

17 A. I don't think in embodiment 1 he
18 mentioning an alternative to ion implantation.

19 Q. There's a disclosure in Nakamura of
20 forming raised source and raised drain, correct?

21 A. I don't think it's in embodiment 1. Can
22 you point me where it says it in embodiment 1?

23 Q. Well, I'm talking about the reference
24 here as a whole, that Nakamura dis- -- discloses an
25 alternative to ion implantation for forming the

1 source and drain regions, correct?

2 MR. CHEN: Objection to form.

3 THE DEPONENT: So --

4 (Discussion off the stenographic record.)

5 THE VIDEOGRAPHER: The time is 9:53 a.m.

6 We're going off the record.

7 (Recess taken.)

8 THE VIDEOGRAPHER: The time is now

9 9:59 a.m. We are now back on the record.

10 Q. (By Mr. Colaianni) Nakamura discloses in
11 column 15 the formation of raised source and raised
12 drain, correct?

13 A. Let me look at it.

14 So he's using -- his -- his embodiment 4,
15 the one that is claim 14 and 15, and he's using --
16 he's illustrating it in figure 7A and 7B. And he
17 shows a -- that he has a raised source drain.

18 Q. And that disclosure is in column 15 of
19 Nakamura, correct?

20 A. Yeah, in column 15, he describe it.

21 Q. And this -- this description applies to
22 the proceeding embodiments as well, correct?

23 MR. CHEN: Objection to form.

24 THE DEPONENT: I don't understand what
25 you mean "proceeding," apply to proceeding -- can

1 you explain what you mean.

2 Q. (By Mr. Colaianni) Yeah.

3 The description of the raised form --
4 raised source and -- strike that.

5 The description in Nakamura of the
6 formulation of raised source and raised drain
7 applies to embodiments described before column 15,
8 correct?

9 A. Well, it describes specific -- it's a
10 specific embodiment and it create the other
11 structure in similar way that was done earlier. So
12 it's applied for that extent.

13 Q. Well, what -- what's disclosed in
14 column 15 is that ion implantation or the raised
15 source/raised drain could be used in any of the
16 embodiments disclosed in Nakamura, correct?

17 MR. CHEN: Objection to form.

18 THE DEPONENT: I don't see it says it.
19 It described it specifically for 4, which is
20 specific embodiment; that he used this implantation
21 to create the source drain that's in the -- I think
22 it's -- column 15, lines 30 to 45.

23 Q. (By Mr. Colaianni) In the paragraph just
24 above that, it indicates that there's an
25 alternative way to form the source drain, other

1 than ion implantation in the above-described
2 embodiments, correct?

3 A. Yeah -- yeah. In that paragraph he
4 mentioned that the raised source drain could be
5 used in the above-described embodiment is line 25.

6 Q. And with respect to the description at
7 column 15, lines 25 to 55, Nakamura describes that
8 the conductive film is doped and then subject to
9 suitable thermal treatment to diffuse the dopant
10 impurity from the electrodes 42 and 44 into the
11 silicon substrate to thereby form the source drain
12 diffused layer 38 and 40, correct?

13 A. Yes.

14 Q. So the thermal treatment described by
15 Nakamura drives the dopants into the substrate,
16 correct?

17 A. Yes.

18 Q. Let's take a look at figures 3A and 3B of
19 the Nakamura reference.

20 You reviewed figure 3A and 3B as part of
21 your analysis, correct?

22 A. Yes.

23 Q. Figures 3A and 3B illustrate problems
24 that could occur during the process described in
25 the first embodiment, correct?

1 A. Yes.

2 Q. Specifically, these figures illustrate a
3 case that disalignment takes place in the
4 lithography step of opening the contact holes 34
5 and 36, correct?

6 A. Yeah. When you have misalignment of the
7 mask between the layers, you have the contact
8 opening. Those perform -- not created optimally.

9 Q. And this misalignment is something you
10 would seek to avoid, correct?

11 MR. CHEN: Objection to form.

12 THE DEPONENT: You seek to minimize. You
13 can't really avoid it because part of the
14 process -- process fluctuation, you always have
15 certain misalignment. So it's -- you design the
16 process to be able to live with, but you try to
17 minimize it.

18 Q. (By Mr. Colaianni) Why do you want to
19 minimize the misalignment?

20 A. To avoid problem like the way it shows in
21 the figure 3A and 3B and -- so it's -- if you don't
22 do the process in the very specific structure in
23 the way it should be done, you can end up having --
24 creating different kind of structure.

25 Because if you compare 3B to A -- to 2B,

1 you can see that, for example, the opening 40 or
2 the area above the diffusion 40 -- was that there
3 when 3B -- is much narrower in the figures 3B,
4 which is where it has a original 40, while in
5 figure 2B, when you look at the area above 32,
6 which is the equivalent area to 40 in 3B, there the
7 opening is wider.

8 Q. Could you look at column 11 of Nakamura,
9 please.

10 A. Okay.

11 Q. And do you see at lines 59 or 61 where
12 Nakamura says that to ensure a disalignment margin,
13 it is necessary to extend the contact holes 34 and
14 36 sufficiently over the gate electrodes 18.

15 Do you see that?

16 A. Yes.

17 Q. So Nakamura is disclosing that when
18 implementing the first embodiment, it is necessary
19 to remove at least a portion of the dielectric
20 layers 24 and 26 over the gate electrode, correct?

21 MR. CHEN: Objection to form.

22 THE DEPONENT: What do you mean to remove
23 just a portion -- what -- can you refer me to where
24 in embodiment 1 you finding it?

25 Q. (By Mr. Colaianni) I was just looking at

1 the portion of the specification we were just
2 looking at, column 11, lines 59 to 61.

3 A. So this is the second embodiment. Okay.

4 Q. And what Nakamura is disclosing here is
5 that it's necessary to remove at least a portion of
6 the dielectric layers 24 and 26 over the gate
7 electrode when -- correct?

8 MR. CHEN: Objection to form.

9 THE DEPONENT: Well, in column 12, he
10 describe how to create the structure. Column 11
11 just tell you the issue is the first embodiment and
12 he doesn't describe the -- how it's created.

13 So let's -- let's follow the column 12.
14 So he says that you have a photoresist 28. This is
15 looking at figure 4 for column 28 -- I mean for
16 second embodiment.

17 So he's saying that you -- it look
18 from -- for ways that you partially etch back
19 dielectric for the -- that caused the wafer, which
20 is similar to the same the way you do in embodiment
21 1, you partially etch the forced dielectric. This
22 is now 26.

23 Then you put -- when it's planarized, you
24 are able put nicely the photoresist 28. And then
25 you do anisotropic etching of 28 using the

1 photoresist as a mask. And then you remove the
2 resist -- the photoresist and continue the pattern.

3 Q. (By Mr. Colaianni) Okay.

4 A. So this is describing in column 12,
5 roughly from line 10 all the way to 28 or so or 30.

6 Q. Can you look at figure 2A and 2B again,
7 please.

8 A. Sure. Yeah.

9 Q. With respect to these figures, if all the
10 material over the gate electrode were protected by
11 the mask, you would be increasing the likelihood of
12 a misalignment as shown, for example, in figure 3,
13 correct?

14 MR. CHEN: Objection to form.

15 THE DEPONENT: If it -- if it will be --
16 because, you see, you have the rim margin, which is
17 the weights of the spacer that you're creating in
18 2B. If you look at layer 30, you have a certain
19 weights of the spacer. And the spacer is
20 originally create this extension 22.

21 So -- so you can see the weights of this
22 column, which is the spacer that's the side of the
23 gates, and so you can increase the photoresist 28
24 above the gate in figure 2A above margin 16 and
25 so -- and still leave the margin, as long as it

1 doesn't extend past the spacer.

2 Q. (By Mr. Colaianni) But -- but you still
3 would be increasing the likelihood that a small
4 misalignment would occur, if the material over the
5 gate electrode were protected by the mask, right?

6 MR. CHEN: Objection to form.

7 THE DEPONENT: Well, you see that for --
8 the well-designed process and what this patent is
9 teaching is to make a manufacturable process. So
10 you design your process with a certain dimension
11 and certain space or size in taking, designing the
12 mask that the misalignment to be such that even in
13 a worst-case for misalignment, you still will
14 remain above the spacer, so you wouldn't create the
15 structure that's shown in 3B.

16 And this is part of -- of optimization of
17 manufacturing process and person in the ordinary
18 skill in the art would understand it.

19 Q. (By Mr. Colaianni) You want to minimize
20 the size of the mask over the electrodes to provide
21 yourself a margin for disalignment, correct?

22 MR. CHEN: Objection to form.

23 THE DEPONENT: Well, you want to control
24 it, because you still need to have a certain size
25 of the mask remaining there. So you want it to be

1 well defined with certain dimension and not vary
2 too much around these dimension.

3 Q. (By Mr. Colaianni) Sure.

4 But you want to minimize the size as much
5 as you can to provide yourself a margin, correct?

6 MR. CHEN: Objection to form.

7 THE DEPONENT: Not really. You need to
8 be wide enough so you are able to create the
9 spacers. If you minimize it too much, you wouldn't
10 be able to ensure that the spacer will have the
11 shape you want it. And you also can end up
12 starting etching into the layer 20, if it's too
13 small on top of the gate.

14 Q. (By Mr. Colaianni) So you -- you don't
15 believe that if all the material over the gate
16 electrode were protected by a mask, that you would
17 be increasing the likelihood of a small
18 disalignment? Is that -- that your testimony?

19 MR. CHEN: Objection to form.

20 THE DEPONENT: You want to optimize it so
21 it would be the right size, and you want to control
22 your process so your process is well controlled so
23 you don't have too much misalignment. Because if
24 your process is -- like, for example, if you didn't
25 planarize layer A, the top dielectric -- so it's

1 really flat so you can well define the photoresist
2 and create well-defined shape in the -- in the
3 photoresist 28 -- then you wouldn't have a good
4 shape of the structure 28 and you can run into this
5 problem. So this is why you stop the -- to do the
6 planarization up to a point that you have it
7 uniformly across the wafer.

8 Q. (By Mr. Colaianni) Okay. Can I get you
9 to answer my question.

10 A. Sure.

11 Q. Do you -- do you disagree that if all the
12 material over the gate electrode in figure 2B were
13 protected by a mask, you would be increasing the
14 likelihood of a small disalignment?

15 Do you disagree with that?

16 MR. CHEN: Objection to form.

17 THE DEPONENT: That -- it doesn't impact
18 the amount of misalignment, the size of the opening
19 or the size of the photoresist.

20 So, you see, the misalignment is the
21 properties of the photoresist itself. And it's
22 function of the planarization. So all this affect
23 the misalignment. So this is what I was trying to
24 say in the previous answer.

25 So the misalignment is function of the --

1 what you -- what is the material you putting on,
2 the photoresist material put, under what condition
3 and what surface you put on it. And so this will
4 determine how much it will be misaligned.

5 Q. (By Mr. Colaianni) Nakamura discloses
6 the necessity of removing a portion of the
7 dielectric layers 24 and 26, correct?

8 MR. CHEN: Objection to form.

9 THE DEPONENT: I mean, it -- you need to
10 remove the dielectric 24 and 26 as part of the
11 process of a -- the etch process that you create
12 the -- in this area that later you are putting 42
13 to connect region 38 to the outside wall, I guess
14 you can call it -- or region 40 also in figure 2C.

15 Q. (By Mr. Colaianni) In a case where the
16 contact hole 34 and 36 extends sufficiently over
17 the gate electrodes 18, a portion of the third
18 dielectric layer over the gate electrode would be
19 exposed during the first part of the etch in
20 figure 2A, correct?

21 MR. CHEN: Objection to form.

22 THE DEPONENT: Can you repeat the
23 question.

24 Q. (By Mr. Colaianni) Sure.

25 In a case where the contact holes 34 and

1 36 extend sufficiently over the gate electrodes 18,
2 a portion of the third dielectric layer over the
3 gate electrode would be exposed during the first
4 part of the etch shown in figure 2A, correct?

5 MR. CHEN: Same objection.

6 THE DEPONENT: If the photoresist 28
7 would be designed too small, it would make it -- it
8 will make the process less -- not manufacturable
9 because you will have region too much exposed on
10 top of the gate like region 20.

11 Q. (By Mr. Colaianni) So -- so are you
12 agreeing that a portion of the third dielectric
13 layer over the gate electrode would be exposed
14 during the first part of the etch?

15 MR. CHEN: Objection to form.

16 THE DEPONENT: If the -- I mean, if you
17 follow the teaching of the -- the Nakamura patent,
18 then you will have a -- and you do the -- the
19 situation you mentioned, this wouldn't be something
20 that Nakamura would want you to do, because you
21 want to control the size of the -- the size of the
22 shape of the photoresist 28. So you cover the gate
23 in dielectric 18 and version 20. So you wouldn't
24 want to create the situation that it is too small.

25 Q. (By Mr. Colaianni) What do you mean the

1 photoresist could be too small?

2 A. So, see, if you look at figure 2A and it
3 shows photoresist 28, when you doing the etch, you
4 want -- and there are three -- there are like
5 four -- you call them like cubes, the region of the
6 where 28 is. So two are on the left and the right
7 side of figure 2A and two are in the middle above
8 the gate 18 and the dielectric 20.

9 So I was talking about these two middle a
10 column of photoresist 28. So these two column you
11 want to be wide enough so you don't damage the gate
12 oxide -- the gate dielectric -- I mean the gate
13 conductor.

14 When I mean "damage," I mean that when
15 you start etching the layer in 24, and you can have
16 reaching to layer 20 to the conductor -- the gate
17 conductor deposit on 18.

18 Q. But the photoresist 28 can be designed
19 small enough so that the third dielectric layer is
20 exposed, correct?

21 A. Well, it's exposed -- you want it to be
22 exposed in the area that are to the right and left
23 of where originally the area 18 is, conductor 18,
24 because, see, this is -- if not, you will run into
25 problem showing in figure 3B.

1 Q. Let's talk about the other embodiments in
2 Nakamura.

3 There's a second and third embodiment
4 disclosed in column 11 and column 12, correct?

5 A. Yes. Column 12 is where certain
6 embodiments start. 11 and 12 is where second
7 embodiment is described.

8 Q. In column 12, Nakamura describes that the
9 second and third embodiments simplify the
10 lithography step of the first embodiment by
11 avoiding the masks over the gate electrodes,
12 correct?

13 A. Well, the second embodiment is different
14 from the third embodiment, so -- and the second
15 embodiment is talking about improving -- avoiding
16 the structure which you get in 3A and 3B. And
17 it's -- I guess it's in column 11, line 37, so -- I
18 guess so 50 or 60.

19 And in the -- and in the third
20 embodiment, it is only start in column 12, and you
21 use figure 5A through C and 6A and B. So it
22 describe it's -- it's a different embodiment in
23 third embodiment.

24 And I don't see it mentioning there. So
25 trying to improve misalignment, it should maybe say

1 it someplace, but he described more in column 12
2 and 13 how to make the -- that third embodiment.

3 Q. But -- but the same benefit would arise
4 in the third embodiment, correct?

5 A. Well, the third embodiment is different
6 from the second embodiment. They are not the same,
7 so -- so, I mean, you need to look at them
8 independently and I -- in my declaration, I
9 describe the first and third embodiment. So...

10 Q. You don't believe that the third
11 embodiment simplifies the lithography step of the
12 first embodiment by avoiding masks over the gate
13 electrodes?

14 A. It's -- it likely it does the same thing,
15 but it doesn't describe it in the -- in the column
16 that you refer to.

17 Q. But -- but the -- but the patent
18 describes that benefit applying to the first
19 embodiment, correct?

20 A. Well, it's mentioned in the second
21 embodiment, but it doesn't discuss it, as far as I
22 can see right now, in the third embodiment that...

23 Q. Okay. But the benefit would arise with
24 respect to the third embodiment.

25 You would agree with that, correct?

1 MR. CHEN: Objection to form.

2 THE DEPONENT: In the third embodiment,
3 if doing it differently from the first embodiment,
4 then you have a -- some benefit, the third
5 embodiment from doing -- they talk of your process
6 differently.

7 Q. (By Mr. Colaianni) Right.

8 The lithography is -- is -- process is
9 simplified, correct?

10 A. It's different. It's -- it's just a
11 different -- I'm not sure, when you say
12 "simplified," what you are referring to.

13 Q. It -- it avoids the formation of masks
14 over the gate electrodes.

15 It's simplified in that respect, isn't
16 it?

17 A. Yes.

18 MR. CHEN: Objection to form.

19 THE DEPONENT: I mean, it has its own
20 problems. But it's just a different set of
21 operations that are done in different sequence.

22 Q. (By Mr. Colaianni) But would you agree
23 that these -- the lithography of the third
24 embodiment avoids masks over the gate electrodes?

25 A. Yeah, if you look at figure 5C, which I

1 believe describe -- just one second. I try to find
2 it.

3 Basically, column 13, line 39 through
4 roughly 46 or '7, something like this.

5 Q. Both of the second and third embodiments
6 of Nakamura share the beginning of the process of
7 the first embodiments shown in figures 1A and 1B,
8 correct?

9 A. Yes. In the -- in column 12, it's refer
10 in general that the earlier step are -- are done --
11 fabricated the same as the first and second
12 embodiment and use the same reference number and --
13 and you start describing embodiment 3 from
14 figure 5A, basically, and it's -- it's column 12,
15 line 60 to 67.

16 Q. And both the second and third embodiments
17 describe planarizing the dielectric layer 26,
18 correct?

19 MR. CHEN: Objection to form.

20 THE DEPONENT: The -- the third
21 embodiment describe a -- a -- I guess it starts in
22 column 13, at line 26, that you deposit a
23 insulation layer on the entire surface. Basically,
24 all the way across from one end to the other end.
25 And then you planarize the surface and -- and -- so

1 this is for embodiment 3.

2 Let me try to find what it says for
3 embodiment -- oh, it says the planarization for
4 embodiment 2 -- I mean, it's -- I didn't focus
5 declaration on the detail of embodiment 2, and I
6 don't see it here. I mention which column -- I
7 mentioned the planarization --

8 Q. (By Mr. Colaianni) Well --

9 A. -- for embodiment 2.

10 Q. Take a look at column 12, if you would,
11 lines 7 through 11. It describes that the second
12 embodiment fabricated semiconductor device in the
13 same way as the first embodiments shown in
14 figures 1A through 1C.

15 Do you see that?

16 A. Yeah.

17 Q. So the second embodiment would
18 planarize that --

19 A. Okay.

20 Q. -- dielectric layer 26, correct?

21 A. Yes.

22 Q. The -- I'm sorry.

23 A. Like the way it's in embodiment 1, yeah.

24 Q. The second and third embodiments diverge
25 in the amount of the dielectric layer 26 that is

1 removed during the planarization step, correct?

2 A. Well, the second embodiment he say it's
3 similar to the first embodiment. So it doesn't --
4 so I'm not sure why you -- I mean, it -- it shows
5 that the embodiment 1 you have layer 26 is fairly
6 thick and cover higher above the gate.

7 I mean, you have a layer -- above
8 layer 24 in figure 1C, you have region 26 remaining
9 after the planarization.

10 Q. Right.

11 So the second embodiment would planarize
12 the dielectric layer 26, as shown in figure 1C,
13 correct?

14 A. Well, I think the second embodiment use
15 figure 4. And if you look in figure 4A, you have
16 the dielectric 26 above the gate -- above --
17 basically, you have a portion of layer 26 remaining
18 above layer 24 in figure 4A and also in figure 1C.

19 Q. In figure 4A, the planarization leaves
20 some of the dielectric layer 26 over the gate
21 electrodes, correct?

22 A. Yes. These are the gate -- I mean, there
23 is a layer 26 above layer 24, which is above
24 gate 18 in figure 4A.

25 Q. In the third embodiment, the dielectric

1 layer 26 is planarized all the way down to the
2 dielectric layer 24 over the gate electrodes,
3 correct?

4 A. Yeah, in figure 5B, it shows that the
5 layer 26 is removed all the way so layer 24 is not
6 covered by layer 26.

7 Q. So the difference in these planarization
8 steps, between the second and third embodiments, is
9 the amount of the dielectric layer 26 that's
10 removed, correct?

11 MR. CHEN: Objection to form.

12 THE DEPONENT: Can you repeat the
13 question.

14 Q. (By Mr. Colaianni) Sure.

15 The difference in the planarization steps
16 from the second embodiment to the third embodiment
17 is the amount of the dielectric layer 26 that is
18 removed, correct?

19 MR. CHEN: Objection to form.

20 THE DEPONENT: Yeah. You use a different
21 process so you are able to go all the way down to
22 layer 24 in embodiment -- the third embodiment
23 versus the earlier embodiment.

24 Q. (By Mr. Colaianni) Beyond this step of
25 planarizing the dielectric layer 26, the steps of

1 the second and third embodiments are the same,
2 correct?

3 MR. CHEN: Objection to form.

4 THE DEPONENT: When you say the -- the
5 step -- I mean, there are -- there are different
6 processes. I mean, different detail of the -- of
7 the way you make them, so -- at that -- just
8 planarization process itself is different between
9 these two embodiment.

10 Q. (By Mr. Colaianni) With regard to the
11 third embodiment, figure 6A shows a semiconductor
12 device after the etching process that removes the
13 third and fourth dielectric with the contact --
14 within the contact holes 34 to expose the
15 underlying diffusion regions, correct?

16 A. It shows that when you finish following
17 the sequence in embodiment third that is on
18 column 13 -- I guess starting line 43 -- that you
19 would do anisotropic etch initially with the
20 photoresist layers. And then later you remove the
21 photoresist layer like the way it says in column
22 13, line 47.

23 And then you continue the etch. Any
24 specific etch that would permit -- it says
25 specifically so you need a different etch which

1 uses that point so that you remove both 26 and 24.

2 It's substantially the same etch rate. This is
3 line -- column 13, line 48 to 52.

4 And then eventually when you finish this
5 etch, which goes more down to -- it's repeat again
6 that you want to make sure when you finish it, 24
7 and 26 would have the same height. It's line --
8 column 13, line 62. And then the contact is
9 basically exposed. It goes all the way to line 64.

10 Q. Okay. Let me -- let me unpack that.

11 So figure 6A shows the device after the
12 etch that removes the third and fourth dielectric,
13 correct?

14 A. Figure 6A shows the device after you
15 do -- so this process that I just described in
16 column 13, line -- I think I said 38, all the way
17 to line 6 -- 64. So when you follow this sequence,
18 you are not having the surface above 32 open.

19 Q. And that etching process removes the
20 third and fourth dielectric within the contact
21 holes 34, correct?

22 A. It does it while it's --

23 MR. CHEN: Objection to form.

24 THE DEPONENT: It does it while it's --
25 make sure that the layer 26 and -- and 24, it's

1 substantially the same etch rate. It's column 13,
2 line 51 to 52.

3 Q. (By Mr. Colaianni) And the removal of
4 the third and fourth dielectric, within the contact
5 hole, exposes the underlying diffusion regions in
6 figure 6A, correct?

7 MR. CHEN: Objection to form.

8 THE DEPONENT: It does it while -- I
9 mean, it's -- it's a -- it's a long process. You
10 start it initially with the photoresist and then
11 you remove the photoresist. And then when you
12 remove the photoresist, you continue this operation
13 until you get eventually the source drain 32
14 exposed -- the surface of source drain 32 exposed.

15 Q. (By Mr. Colaianni) I'm sorry, you said
16 which surface is exposed at the end?

17 A. Of the source drain of the region 30 --
18 the top surface of region 32. Because, see, region
19 32, it goes into the substrate. So you have the
20 top -- I mean, the top edge of it all the way
21 across from the wafer, you have the top area of --
22 that you have region 32 exposed.

23 Q. With regard to figure 6A, after the
24 etching process portions of the dielectric layer 26
25 remain, correct?

1 A. Yes, it's remain at this similar height.

2 And it's the region -- it's the dielectric 24.

3 Q. And these portions of the dielectric
4 layer 26 that remain were previously under the
5 resist layer 28, correct?

6 A. Yes, they were earlier underneath the
7 resist 28 during the etch process -- during the
8 initial part of the etch process, before you remove
9 the photoresist and continue the etch.

10 Q. When describing the third embodiment,
11 Nakamura describes creating the source and drain
12 regions using ion implantation, correct?

13 A. Yes.

14 Q. But as we discussed earlier, also
15 discloses an alternative to ion implantation,
16 correct?

17 MR. CHEN: Objection to form.

18 THE DEPONENT: Yes, in embodiment 4, it
19 says that you can use the -- the process described
20 in -- I guess it was column 15. You can use the --
21 it's roughly in the middle of the page there
22 that -- I think from -- yeah, 35 through 45, I
23 believe it is, that he says that you can use this
24 techniques or using -- or use this technique only
25 for the embodiment 3.

1 Q. (By Mr. Colaianni) Okay. Let's take a
2 look at your declaration --

3 A. Sure.

4 Q. -- which we marked as Exhibit 13 at the
5 beginning of the deposition.

6 Exhibit 13 is the declaration you
7 prepared in connection with this matter, correct?

8 A. Yes. I believe it look like it, yeah.

9 Q. Do you recall how much time you spent
10 preparing this declaration?

11 A. I'm not sure because I worked on all
12 the -- I mean, I was going back and forth between
13 different declarations, so I didn't really separate
14 one declaration by itself.

15 Twenty, 30 hours maybe. I'm not sure on
16 the number.

17 Q. Does Exhibit 13 contain all of the
18 opinions you have expressed in this matter?

19 A. Yes.

20 Q. And if you take a look at paragraph 5 of
21 your declaration, please.

22 You note here that the patent claims in
23 an IPR are given their broadest reasonable
24 interpretation.

25 Do you see that?

1 A. Yes, I see it.

2 Q. And did you apply any -- any
3 constructions to the claim language of the '244
4 patent as part of your analysis in this matter?

5 A. It's -- I believe so. Let me try to find
6 the paragraph where it's discussed.

7 It's starting in paragraph 34 and all the
8 way to 47. Maybe even more. Yeah, it's even more.
9 Yeah.

10 Q. Your opinions relating to the
11 construction of the claim language are fully
12 contained in section VI of your declaration?

13 A. Yes. I believe section VI cover --
14 discuss all of them, yeah.

15 Q. On page 9 of your declaration, there's a
16 section IV titled "Background of the '244 Patent."

17 Do you see that?

18 A. Just second.

19 Okay.

20 Q. Did you draft this section of the
21 declaration?

22 A. Yeah. I mean, I work with the attorneys
23 at some part. I have some part. They gave input,
24 but everything was reviewed and -- and approved by
25 me.

1 Q. In paragraph 21 of the declaration you
2 state that, "the formation of very shallowly doped
3 regions called shallow junctions is desirable."

4 Do you see that?

5 A. Yes.

6 Q. Is the primary goal of the '244 patent to
7 describe certain techniques performing these
8 shallow junctions?

9 MR. CHEN: Objection to form.

10 THE DEPONENT: It's -- it's a key area
11 that he cared about, but he basically was trying to
12 teach a new way to make manufacturable process.

13 Q. (By Mr. Colaianni) Can you turn the page
14 over to paragraph 24, please.

15 In paragraph 24 you state that "It is the
16 object of the '244 invention to provide a process
17 for facilitating the formation of raised source and
18 drains in miniaturized (i.e., deep sub-micron)
19 devices."

20 Do you see that?

21 A. Which paragraph? You are at 24?

22 Q. It's at the end of paragraph 24, yes.

23 A. It's one of the things that paragraph 24
24 mention, yeah.

25 Q. And you would agree that Nakamura also

1 provides a process for facilitating the formation
2 of raised source and drains in miniaturized
3 devices, correct?

4 MR. CHEN: Objection to form.

5 THE DEPONENT: Well, Nakamura teach his
6 own structures that -- to do a -- a -- I mean to --
7 for a process that also use a source -- a raised
8 source drain, yes.

9 Q. (By Mr. Colaianni) In paragraph 25, you
10 state that "The '244 invention teaches a method
11 where the gate electrode, including the sensitive
12 channel dielectric layer is formed before the
13 source and drain electrodes so that processing
14 problems associated with forming the gate in the
15 presence of delicate source and drains are voided."

16 Do you see that?

17 A. Yes.

18 Q. In the Nakamura reference, it is
19 described to form the gate electrodes before
20 forming the source and the drain electrodes,
21 correct?

22 A. Yes. But this is paragraph 25 talk about
23 the other stuff also that -- that you want to
24 have -- be compatible with deep sub-micron process.
25 So you want to make sure that you can use the

1 critical high-resolution lithographic. And the
2 control of the mask dimension and alignment is
3 critical that -- is less critical, since the
4 location of the edge of the source drain is outside
5 where the gate is; so that there are more than just
6 the one sentence you mentioned in paragraph 25.

7 Q. In paragraph 27 of your declaration, you
8 describe --

9 A. Sorry. Where?

10 Q. Paragraph 27.

11 A. Go ahead.

12 Q. You describe the process in the '244
13 patent up to through figure 3, correct?

14 A. Well, in paragraph 27, it's close to a
15 full page, so I'm not sure what you are referring
16 in paragraph 27.

17 Q. Well, in paragraph 27, you're describing
18 the process for manufacturing a semiconductor
19 that's described in the '244 patent, right?

20 A. Yeah. But you didn't say your question
21 what you are talking about, so I wasn't clear --

22 Q. And --

23 A. -- what you are asking me.

24 Q. And you describe the steps here up to
25 figure 3, correct?

1 A. Yes, I describe the process to make the
2 device up to figure -- creating the structure shown
3 in figure 3.

4 Q. Correct.

5 And at least up to figure 3, those steps
6 are also disclosed by Nakamura, correct?

7 MR. CHEN: Objection to form.

8 THE DEPONENT: I don't think so. There
9 isn't a figure in Nakamura that show the structure
10 of figure 3 of '244.

11 Q. (By Mr. Colaianni) Prior to the
12 planarization step described in Nakamura, the
13 process steps in the figures of Nakamura are
14 virtually identical to those in figure 3 of the
15 '244, correct?

16 A. It doesn't show that it's identical. I
17 mean, I don't see any figure in the '9 -- the
18 Nakamura '994 that look like the structure in
19 figure 3.

20 Q. For example, figures 1C of Nakamura,
21 figures 4A.

22 A. Well, 1C that show --

23 Q. And figure 5B.

24 A. I mean, 1C shows Nakamura -- it show two
25 transistor which are -- I mean, 18 with layer 20

1 above them. And there isn't in each -- and there
2 is -- each transistor is not covered by isolation
3 23, just at the edge, the two transistor. And you
4 have a region 22, a diffusion in -- in figure 1C
5 that you don't see region like this in figure 3.

6 And you also have in layer 26, which is
7 planarized leaving a flat surface all the way
8 across the wafer from one end to another end, with
9 a certain thickness above the gate 20, when in
10 figure 3, the -- the -- the top dielectric, the
11 layer 28, it's not planarized. It has controls
12 that generally follow the control of the gate in
13 the region in 1C. So there are many differences
14 between 1C and 3.

15 Q. Okay.

16 A. And I didn't look at other figure yet,
17 but -- I mean, this is just from 1C I see
18 differences.

19 Q. Okay. Let's talk about your claim
20 construction opinions that you've expressed in your
21 declaration in section VI.

22 If you look at page 16, paragraph 34.

23 A. Okay.

24 Q. And here you are interpreting the
25 language "top portion."

1 Do you see that?

2 A. I see it.

3 Q. And you state in paragraph 34 that the
4 term "top portion" is used to refer to the entire
5 top layer 28 shown in figure 3, correct?

6 MR. CHEN: Objection to form.

7 THE DEPONENT: Yeah, it's -- it's -- it's
8 written in paragraph -- it's the last sentence in
9 paragraph 34. "In the '244 patent, the term 'top
10 portion' is used to refer to the entire top of
11 layer 28."

12 Q. (By Mr. Colaianni) The claims don't use
13 the word "entire" when it talks about the
14 portion -- or the top portion, correct?

15 A. It's -- it's -- it's reasonable, by a
16 person in the ordinary skill of the art, that when
17 you're talking about semiconductor processes
18 that -- when you're doing a process on a top to be
19 all the way across -- you see that the -- this
20 technology -- I mean, all the semiconductor
21 technology, are technology where you do the process
22 for the full wafer. You don't just take a wafer
23 and just process a portion of it.

24 And so every process you try to apply,
25 it's done all the way across. This is how this

1 technology was evolved and how the cost was able to
2 go down, because you have a fixed cost of
3 processing full wafer. You don't just send part of
4 a wafer to be processed and the other part keep
5 back. You cannot.

6 But it give you the benefit that as you
7 process them, that since it's fixed cost, if you
8 are able to get them working, you get a low-cost
9 product. And as you evolve the technology, it
10 become cheaper and cheaper. And this is really
11 what more law is based on -- on this industry is
12 based on using process for one end of the wafer to
13 other end of the wafer.

14 And any reasonable person of skill in the
15 art will understand that when you do a process on a
16 wafer, it will done all the way on -- all the
17 surface of the wafer is exposed to the process.

18 Q. You understand the common meaning of the
19 term "portion" means something less than the whole,
20 correct?

21 MR. CHEN: Objection to form.

22 THE DEPONENT: Well, "portion" is a
23 section. I think it's the definition of it. I
24 think of it as a section.

25 Q. (By Mr. Colaianni) Yeah, it -- it's less

1 than the entire -- the entirety of something,
2 correct?

3 A. It doesn't -- I don't -- I'm not sure if
4 it has to be less than entirety. It's -- it's a
5 section, and it could be up to the full whole --
6 the -- the full length of the -- I guess if
7 somebody want to be -- says it is less than the
8 whole, they will need to specifically say a
9 portion, not including the whole.

10 Q. But the -- but the common usage of the
11 term "portion" kind of is less than the whole of
12 something, correct?

13 MR. CHEN: Objection to form.

14 THE DEPONENT: Not really. I mean, I
15 think a reasonable person of skill in the art
16 that -- wouldn't think of it that it limited to
17 always be less than the full size. It's also that
18 these are three-dimensional structures, so it's --
19 so it's a -- you wouldn't certainly look at it this
20 way.

21 Q. (By Mr. Colaianni) The -- the '244
22 patent talks about anisotropic etching to remove a
23 portion of the third dielectric layer 26 on top of
24 the gate electrode 27, correct?

25 A. Is it -- where -- I'm sorry. Where are

1 you referring to, which figure? Are you talking
2 about the Nakamura patent?

3 Q. No. The '244 patent, column 5, lines 28
4 to 30.

5 A. Yes, I see it is written there.
6 Anisotropic processes remove portion of the third
7 dielectric 26.

8 Q. And -- and what that means is that less
9 than all of the dielectric layer 26 is removed,
10 correct?

11 A. In a vertical direction you remove a
12 section or portion of the dielectric 26.

13 Q. You don't remove all of dielectric
14 layer 26?

15 A. In a vertical direction.

16 Q. You don't remove the entire layer across
17 the horizontal direction either, correct?

18 A. Well, you have to -- because this is
19 referring, I think, to figure 4. Because he is
20 talking -- so, see, in column 5, he initially talk
21 about the planarization. It's line 6.

22 "The top portion of the fourth dielectric
23 layer 28 is then planarized by a planarization
24 process."

25 So you cannot do a planarization process

1 with CMP by totally not removing the top layer all
2 the way across the wafer.

3 Q. Right.

4 So in this instance, removing a portion
5 of the dielectric layer does not mean removing the
6 entirety of the dielectric layer, correct?

7 A. Not really. I just read you a line 6, 7
8 and 8 that he's talking about the planarization
9 where he was removing the entire top portion of 28
10 to planarize it.

11 Q. I'm -- I'm --

12 A. To planarize it mean to make it flat.

13 Q. I'm talking about the reference I
14 directed you to in column 5 with respect to the
15 layer 26.

16 A. So layer 26 --

17 Q. Line 28, where it says, "The anisotropic
18 process also removes the portion of the third
19 dielectric layer 26 on top of the gate electrode
20 structure section 27."

21 And you would agree that that is
22 referring to the removal of less than all of the
23 dielectric layer 26, correct?

24 A. This talk about a different process.

25 This is a etch process, when you are going in a

1 vertical direction and you basically -- you are
2 removing it shown in figure 4; that when you don't
3 have the photoresist -- I mean, the area which are
4 not covered by the photoresist, you go down and you
5 etch. And this is what he's talking about, that
6 you etch the -- the trenches, which I guess is
7 shown -- the trenches that eventually become region
8 32A and 32B in figure 5.

9 Q. And in figure 5, there are portions of
10 layer 26 that remain after the etch, correct?

11 A. It's the section of layer 26 that are
12 covered underneath the -- the -- the dielectric 28
13 and also underneath the gate regions.

14 Q. Yes.

15 Those -- those sections of layer 26 are
16 not removed, correct?

17 A. Yeah, because when this is -- we are
18 talking here about an etch process; that then you
19 have a photoresist that -- so you do the etches
20 there, which are not covered by photoresist. But
21 in the planarization process described in the
22 earlier section of column 5 in line 6 or 8, he
23 planarize the full surface and then -- I think it
24 doesn't talk there about section in there.

25 Q. But -- but in figure 5, portions of the

1 dielectric layer 26 that were covering the gate
2 electrode were removed, correct?

3 A. Well, you see that in the -- let me look.
4 Where is the paragraph that you are referring to?

5 Do you see that in the section that you
6 talk, he is talking specifically that he remove
7 portion -- used the use "portion." While when he's
8 talking about the layer 28, that when you planarize
9 it, he doesn't use the word "portion." So the word
10 "portion" give it -- it's a different operation.

11 Q. But you would agree with me that in
12 claim 5 -- strike that.

13 In claim -- in figure 5, the etch process
14 removes a portion of the dielectric layer that
15 covered the gate electrode, but did not remove the
16 entirety of the dielectric layer, correct?

17 MR. CHEN: Objection to form.

18 THE DEPONENT: Well, you see, because
19 he's using here -- he describe it by saying that he
20 remove portion. He doesn't talk about the
21 planarization. So he remove section of layer 26.
22 It create the final structure shown in figure 5.

23 Q. (By Mr. Colaianni) Is your opinion that
24 the phrase "removing a top portion" in claim 1 and
25 14 limited to planarization?

1 MR. CHEN: Objection. Form.

2 THE DEPONENT: Can you show me what you
3 are referring to?

4 Q. (By Mr. Colaianni) Well, in your
5 declaration, you say that the '244 patent specifies
6 that the top portion is removed by planarization,
7 correct?

8 A. Well, it's not limited -- you see that --
9 claim 1 is not limited to planarization. He is
10 saying that the -- he remove the top portion of the
11 layer of the fourth dielectric to expose the cell
12 dielectric. So this is what's shown in figure 4 or
13 so -- figure -- when you go from figure 3 to 4, he
14 shows that he etch back the layer 28 until he get a
15 planar surface where the layer 26 is exposed on top
16 of the gate as shown in figure 4 and then you
17 throughput to 30.

18 So this is what is described in the -- in
19 the first claim, that removing the top portion of
20 the forced dielectric.

21 Q. So -- so you believe that removing the
22 top portion is not limited to planarization,
23 correct?

24 A. It's not limited to the word
25 "planarization," but -- I mean, you basically --

1 you -- it's basically not limited to something like
2 a CMP process, but you etch back down the -- this
3 dielectric 28 so you get a flat planar surface,
4 where you have the region in 26 exposed and
5 surrounded by region 28. The documentation on
6 figure 4 photo the surface on top of it.

7 Q. The '244 patent describes planarization
8 using the CMP process?

9 A. It's an embodiment that is shown in the
10 '244.

11 Q. And that's what you're referring to when
12 you were referring to removal of the entire top
13 portion, correct?

14 MR. CHEN: Objection to form.

15 THE DEPONENT: Well, it's -- I was
16 showing you the embodiment and how it look when
17 it -- when you illustrate it in figure -- going
18 from figure 3 to figure 4.

19 Q. (By Mr. Colaianni) There's no other
20 technique disclosed in the '244 patent for removing
21 the entire top portion, correct?

22 A. A person skilled in the art will
23 understand that you can remove a top portion by
24 also an etch-back process, and this was well-known
25 techniques, for example.

1 Q. But there's nothing disclosed in the '244
2 patent, other than planarization, for removing the
3 top portion, correct?

4 A. A person of ordinary skill in the art
5 would reasonably -- would know that there are other
6 method beside the chemical, mechanical polishing to
7 remove this top portion and expose layer 26, as
8 shown in the figure 4, while you are still at the
9 photoresist surface.

10 Q. Well, that may -- may be your opinion.
11 But I'm asking you to agree, there's nothing
12 disclosed explicitly in the patent for removing the
13 top portion besides planarization, correct?

14 MR. CHEN: Objection to form.

15 THE DEPONENT: Well, the patent disclosed
16 this embodiment of using CMP, yes.

17 Can we have break soon?

18 MR. COLAIANNI: Oh, yeah. Sure.

19 THE VIDEOGRAPHER: This marks the end of
20 DVD 1 in the deposition of Ron Maltiel, Volume II.
21 The time is 11:14 a.m. We're going off the record,
22 Counsel.

23 (Recess taken.)

24 THE VIDEOGRAPHER: Counsel, this now
25 begins DVD 2 in the Volume II deposition of

1 Ron Maltiel. The time is 11:30 a.m. We are now on
2 the record.

3 Q. (By Mr. Colaianni) With regard to your
4 declaration we were just looking at, on
5 paragraph 35, you have a reproduced figure 4 of the
6 '244 patent.

7 Do you see that?

8 A. Yeah, I see it.

9 Q. And in that paragraph you acknowledge
10 that there are portions of layer 28 that remain
11 after -- after portions of that layer were removed,
12 correct?

13 A. Well, it's the -- it's -- basically, it
14 says that removing a top of portion of said fourth
15 dielectric to expose a portion of third dielectric.

16 And then it says -- it -- '244, at
17 figure 3 show -- added to show the top portion of
18 layer 28. I mean the red notation.

19 Q. And after you remove the portion of
20 layer 28, other portions of layer 28 remain, as
21 shown in figure 4, correct?

22 A. The top portion -- it shows what happened
23 to the top portion of layer 28 during this process
24 going from -- after figure 3, which is also part of
25 this paragraph and annotated with this top portion

1 and then figure 4. So it's when you remove the top
2 portion.

3 Q. And when you remove a portion of the
4 layer 28, other portions of layer 28 remain, as
5 shown in figure 4, correct?

6 MR. CHEN: Objection. Form.

7 THE DEPONENT: Well, when you remove the
8 top portion of layer 28, you expose a section of
9 layer 26 above the gate, as shown in figure 4.

10 Q. (By Mr. Colaianni) I need you to answer
11 my question, sir.

12 When you remove a portion of layer 28,
13 other portions of layer 28 remain, as shown in
14 figure 4; isn't that correct?

15 MR. CHEN: Objection to form.

16 THE DEPONENT: It's -- you remove the top
17 portion of layer 28, and then portion of layer 28
18 remain, yeah.

19 Q. (By Mr. Colaianni) Thank you.

20 Paragraph 42 of your declaration --

21 A. Which one?

22 Q. Paragraph 42.

23 You note that Samsung has proposed a
24 construction for the terms "raised source" and
25 "raised drain," correct?

1 A. Yes.

2 Q. Okay. And you have not taken any issue
3 with Samsung's processed construction of those
4 terms, correct?

5 A. Correct.

6 Q. You talk later in paragraph 43 of your
7 declaration about the claim term "at the same
8 time."

9 Do you see that?

10 A. Yes.

11 Q. And this relates to the claim --
12 limitation of claim 1 that starts with removing
13 said fourth dielectric layer, correct?

14 A. It's -- I believe it's regarding
15 column 6, in this section that start from line 53,
16 roughly, or 52, all the way to 57 or '8.

17 Q. Correct.

18 That limitation in- -- includes the term
19 "at the same time" that you've offered an opinion
20 about here in your declaration, correct?

21 A. Yeah, it's in that paragraph -- it's
22 included the term "at the same time."

23 Q. In paragraph 47 of your declaration, at
24 the bottom of page 20, you say, "Thus, it is my
25 understanding that" this "whole limitation requires

1 a process step," correct?

2 A. It's -- it's the sentence in the middle
3 of the paragraph, yeah.

4 Q. Now, the specification describes this as
5 an etching process, correct?

6 A. It's a -- it's described in the -- in
7 the -- can you repeat your question.

8 Q. The specification describes
9 what you've -- what you're discussing in figure --
10 strike that.

11 The specification describes, which you
12 are discussing in paragraph 47 of your declaration,
13 as an etching process, correct?

14 A. Well, it -- it has a long specification.
15 It's a long description. It starts from -- I guess
16 column 5, line 10. And -- all the way to line,
17 roughly, 30 in column 5.

18 Q. And it's described as an etching process,
19 correct?

20 A. It has many words. I mean, I'm not sure
21 if it -- call it an etching process in -- the line
22 that I mentioned. Let me read it.

23 (Discussion off the stenographic record.)

24 Q. (By Mr. Colaianni) For example, at
25 column 5, line 25, it refers to this as an

1 anisotropic etching process, correct?

2 A. Well, it has the word "next." So you
3 have a photoresist you put there, which starts --
4 because I was saying started for -- I believe from
5 column -- I mean column 5, line 10.

6 So you put the photoresist and you define
7 it, and do other thing, and then you do the next,
8 you do the anisotropic etching using the
9 photoresist as a mask all the way through the etch.

10 Q. And the '244 patent refers to that
11 process as an etching process, correct?

12 A. Well, it doesn't -- it doesn't have a
13 subtitle calling this section etch process, this
14 section different things. It's -- it include here
15 the -- when you doing the etch. But it also
16 include putting the photoresist part of this
17 separation.

18 Q. Would you agree with me that the
19 specification refers to this as an anisotropic
20 etching process at column 5, line 25, "yes" or
21 "no"?

22 A. Line 25 talk about an anisotropic etch;
23 specifically, line 25.

24 Q. Anisotropic etching process, that's what
25 the word say in the '244 patent, correct?

1 A. That specific line has also the word
2 anisotropic etching and -- but the full sentence we
3 are talking is not just line 25. But that line
4 include anisotropic etching, yes.

5 Q. You don't want to seem to use the word
6 "process," do you?

7 A. No. It says the word "process" in this
8 line. After anisotropic etching, it says
9 "process. "

10 Q. Right.

11 That's the way this '244 patent
12 characterizes it, as an anisotropic etching
13 process, correct?

14 A. That specific line says it, yeah. But it
15 says before it also talk about the photoresist,
16 exposing the photoresist. And it include
17 photoresist operation.

18 If you start from line 10, the next -- a
19 second resist layer 30 is deposited on top of the
20 dielectric and expose the third dielectric. And it
21 says it's patterned. And so it says many things
22 besides just the word "etch" and "process. "

23 Q. It doesn't say anything about a step,
24 does it?

25 A. In line 25, it doesn't say the word

1 "step. "

2 Q. Not in connection with this etching
3 process, correct?

4 A. What do you mean in connection with it --
5 because I -- you asked me if it doesn't say the
6 word "step." So I agree that line 25 doesn't have
7 the word "step. "

8 Q. In connection with the description of
9 this etching process we're talking about, the
10 patent does not use the term "etching step"; isn't
11 that right?

12 A. It also doesn't call it --

13 Q. "Yes" or "no"; isn't that right?

14 A. I'm not sure what -- what you're
15 referring, that I agree that line 25 doesn't
16 mention the word "step. "

17 Q. In the anisotropic etching process we're
18 talking about, the '244 patent doesn't refer to
19 that process as an etching step, does it? "Yes" or
20 "no"?

21 A. Let me the read the full section.

22 Can you repeat your question.

23 Q. In the anisotropic etching process we're
24 talking about, the '244 patent doesn't refer to
25 that process as an etching step, correct?

1 A. The anisotropic etching that is discussed
2 in line 25 is part of the process of creating the
3 structure which is shown in figure -- whatever
4 figure -- the etching of the structure in figure --
5 you start in figure 3 and you end up all the way to
6 4 to figure 5.

7 So it doesn't call that one just the --
8 the process etch step. There's no title or -- for
9 this section of saying I'm going to describe the
10 etch process step.

11 Q. Now, the '244 patent does describe other
12 etching steps, for example, column 4, line 46,
13 correct?

14 There's reference there to an etching
15 step?

16 A. Just a second, let me read it.
17 Which line are you talking about?

18 Q. Column 4, line 46.
19 There's reference there to an etching
20 step.

21 Do you see that?

22 A. Yes. It's in line 46. It says
23 "subsequent etching step," correct.

24 Q. And, similarly, at the bottom of
25 column 4, there's a sentence that goes into the top

1 of column 5 that makes reference to an etching
2 step, correct?

3 It says, "This dielectric layer 26 will
4 serve as an etch-stop layer in a subsequent etching
5 step."

6 Do you see that?

7 A. Yes.

8 Q. But when the patent talks about removing
9 the unmasked fourth dielectric layer, the '244
10 patent describes that as an etching process,
11 correct?

12 A. Where are you referring to it?

13 Q. What we were talking about earlier, in
14 column 5, line 25.

15 A. Well, in that one is saying that it's
16 part of the operation that start in line 10, when
17 you put the photoresist. And after you've put the
18 photoresist in the finding, then you go through the
19 anisotropic etches — etching process.

20 Q. And the etching process described in
21 column 5 could have multiple steps, correct?

22 A. Yes, but it's described it here as a
23 photoresist during this process on a wafer.

24 Q. I'm — I'm sorry. So the etching process
25 described in column 5 could have multiple steps,

1 correct?

2 A. While you keeping the photoresist on this
3 describes starting from column 5, line 10.

4 Q. Let's go back to your declaration.

5 In paragraph 53, you offer opinions
6 relating to the claim language -- well, you offer
7 opinions with respect to the order of method steps
8 in some of the claims.

9 Do you see that?

10 A. Yes.

11 Q. In paragraph 54, you state that the
12 limitations are arranged in a specific logical
13 order and must be performed in sequence, correct?

14 A. Yes. It's part of paragraph 54, yeah.

15 Q. And -- but you agree there are certain --
16 that there can be semiconductor processing steps
17 that could be reversed in order without affecting
18 the formation of a device, correct?

19 MR. CHEN: Objection to form.

20 THE DEPONENT: Not really. It's -- like
21 the way I was describing earlier in four of the
22 other patents, it -- the other IPR actions, that
23 the -- these device are very delicate, and you have
24 to be very careful the way you make them.

25 And Intel came up with this concept which

1 is called "copy exact"; that when they try to do a
2 process in -- in -- as a fabrication line or as in
3 a location, to make sure that everything is done in
4 exactly the same way, because there's a lot of
5 interaction between the various operation, and a
6 lot of these devices -- or all these devices are
7 really very small in dimensions. So you don't
8 always understand and know in advance what would be
9 the impact.

10 And also, these are three-dimensional
11 structures, so you have to do it in certain
12 subsequence to make sure you get the right shape
13 and the right structure in a three-dimensional
14 fashion.

15 Q. (By Mr. Colaianni) But as a person
16 skilled in the art, you can't envision a scenario
17 where the -- any -- any process steps could be
18 reversed in order without affecting the formation
19 of the semiconductor device?

20 A. Not really. I mean, to show you how
21 sensitive these devices are, even when you have
22 a -- a -- you have a sequence of steps that are --
23 that the orders are well known and the computer
24 keep log until the order. But you even control
25 often how long you can wait between -- if you

1 finish operation in one machine and you want to
2 move to the next operation, if -- you have to be
3 careful that the wafer don't wait outside for too
4 long. So everything has to be done in a very
5 precise and controlled way now.

6 Q. You're aware that the board disagrees
7 with your opinion relating to the necessity of
8 performing the claim steps in a certain order,
9 correct?

10 MR. CHEN: Objection to form.

11 THE DEPONENT: I'm not sure -- I don't
12 remember exactly what is the board opinion. But
13 I'm just stating from my experience in the industry
14 and what is well known; that this concept of copy
15 exact is part of the reason why Intel has been so
16 successful making many wafer and make it very
17 successfully.

18 Another company -- Intel is a company
19 much larger than other one, Velodyne and Process
20 Technology, many other company, like they are few
21 generation ahead of other company. So it's well
22 known in semiconductor that these are delicate
23 device and you have to be very careful how you make
24 them, if you want to get good ending wafer in the
25 end.

1 Q. (By Mr. Colaianni) My question was,
2 you're not aware -- so you're not aware of the way
3 the board construed this claim language?

4 A. I remember that reading it and thinking
5 about it, but I don't remember the exact wording
6 that they use in -- in what specific circumstance
7 they were talking.

8 Q. So if -- if the board disagrees with your
9 opinions relating to the construction of those
10 method steps, that would change your opinions,
11 wouldn't it?

12 MR. CHEN: Objection to form.

13 THE DEPONENT: I would like to see the
14 specific wording of what the board say.

15 Q. (By Mr. Colaianni) What if the board
16 said that there was no requirement that those claim
17 steps be performed in a certain order?

18 MR. CHEN: Objection.

19 Q. (By Mr. Colaianni) That would affect
20 your opinion, wouldn't it?

21 MR. CHEN: Objection to form.

22 THE DEPONENT: It's -- it depends exactly
23 what are the circumstances are talking about, yeah.

24 Q. (By Mr. Colaianni) Okay. You're not
25 familiar with the -- what the board said regarding

1 that -- that -- that claim construction issue,
2 correct?

3 A. I read it a while back. I don't remember
4 all the detail of it.

5 MR. COLAIANNI: Okay. I'm just going to
6 switch gears, go into another area.

7 Do you think it would make sense to break
8 for lunch here quickly?

9 THE DEPONENT: Sure.

10 MR. CHEN: Sure.

11 MR. COLAIANNI: And come back so maybe we
12 could retool.

13 MR. CHEN: Yeah. Yeah.

14 MR. COLAIANNI: Is that fine?

15 MR. CHEN: Yeah, that's fine.

16 THE VIDEOGRAPHER: The time is 11:50 a.m.
17 Counsel, we are now going off the record.

18 (Recess taken.)

19 THE VIDEOGRAPHER: The time is now
20 12:43 p.m. We are now back on the record.

21 Q. (By Mr. Colaianni) Good afternoon.

22 A. Good afternoon.

23 Q. Can you go back to Exhibit 14, the
24 Nakamura patent, please, and take a look at
25 column 11.

1 And this morning, we were talking about a
2 statement around column -- I'm sorry -- around
3 line 50 -- 59, 60, 61, that says, "On the other
4 hand, to ensure a disalignment margin it is
5 necessary to extent the holes 34, 36 sufficiently
6 over the gate electrodes 18."

7 Do you see that?

8 A. Yes.

9 Q. Okay. Why is it necessary to extend the
10 contact holes over -- sufficiently over the gate
11 electrodes, as Nakamura states here?

12 A. It says there that it make them -- width
13 of the inter-layer insulation film 56 remain on the
14 gate electrode extremely narrow, which makes the
15 patterning difficult.

16 Well, it's -- I mean -- let me try to
17 read this few paragraph about it; because when we
18 talk about the other end, I'm not sure what is the
19 first end is about, because it doesn't disclose
20 some stuff earlier probably.

21 So sorry, repeat. So what is the
22 question?

23 Q. Well, the reason that Nakamura is stating
24 that it's necessary to extend the contact hole
25 sufficiently over the gate electrodes relates to

1 the misalignment problem described in connection
2 with figures 3A and 3B, correct?

3 A. Yes. He's talking here about the
4 misalignment in figure 3A and 3B and how you have
5 to be careful about the misalignment. But also you
6 want to make sure that it's not too narrow, the --
7 the -- the region he set -- in the photoresist -- I
8 mean, the region 26, you want to make sure it's not
9 too narrow.

10 Q. And -- and figure 3A and 3B relate to
11 this misalignment problem we discussed this
12 morning, correct?

13 A. Yes.

14 Q. And they are disclosed in the Nakamura
15 reference as relating to the -- the fabrication of
16 a semiconductor device, according to the first
17 embodiment, correct?

18 A. Yeah, it mention that this what happen
19 when you have the first embodiment. You will have
20 the -- you can have potentially the structure shown
21 in figure 3 and 3B, which is a problem for good
22 manufacturing process.

23 Q. So in the first embodiment, which is
24 shown in figures 2A through 2C, it would be
25 necessary to remove at least a portion of the

1 dielectric layers 24 and 26 over the gate
2 electrode, correct?

3 MR. CHEN: Objection to form.

4 THE DEPONENT: Yes. That you want to
5 remove a portion of this layer that are not covered
6 by the photoresist 28. This is how you start the
7 process of defining this region 34 and 36.

8 Q. (By Mr. Colaianni) And the remaining
9 portion would be narrower than the width of the
10 gate electrode, correct?

11 MR. CHEN: Objection to form.

12 THE DEPONENT: I'm not sure. What you --
13 can you explain what you're after?

14 Q. (By Mr. Colaianni) In -- after you
15 remove a portion of the layers 24 and 26.

16 A. And you're talking about embodiment --
17 the second embodiment?

18 Q. No. In figure 2B --

19 A. Oh.

20 Q. -- in the first embodiment.

21 A. Okay. So the first embodiment.

22 MR. COLAIANNI: Should I restate the
23 question --

24 MR. CHEN: Is there a question pending?

25 MR. COLAIANNI: Should I restate -- I'm

1 sorry. I wasn't sure. Let -- let -- let me repeat
2 the question, so -- I thought there was a question
3 pending, but let me restate it so we're clear.

4 THE DEPONENT: Sure.

5 Q. (By Mr. Colaianni) In figure 2B, the
6 remaining portions of the dielectric layer 26 and
7 the photoresist 28 are narrower than the width of
8 the gate electrode 18, correct?

9 MR. CHEN: Objection to form.

10 THE DEPONENT: I mean, they are narrower
11 than the full width of the layer 24 that is above
12 the gate 18 and 20. If you look in figure 2A, you
13 can see that layer 24 is covering the gate 18 and
14 the dielectric 20. So this is the full width that
15 you are -- want to protect -- I mean that you
16 want -- you want to protect that -- the region 20,
17 so you need the photoresist 28 to fit in it, but
18 you don't want to be able -- it's to be etched for
19 the layer 24 to attack the dielectric and
20 potentially the gate in this region that would make
21 the device not fully manufacturable, when you have
22 so many million of transistor across each die.

23 Q. (By Mr. Colaianni) Okay. So just --
24 just in response to my question, the remaining
25 portions of the dielectric layer 26 and the

1 photoresist 28 are narrower than the width of the
2 gate electrode 18 in figure 2B; is that correct?

3 MR. CHEN: Same objection.

4 THE DEPONENT: It tends to be wide enough
5 so it will be -- one side wide enough so you can
6 photograph this other structure, but it tends to be
7 narrower than the width of the gate when you take
8 into account that it's covered by layer 24 above it
9 on both sides. So it has to be narrower than the
10 full width when you take into account layer 24.

11 Q. (By Mr. Colaianni) One second, please.

12 A. No problem.

13 Q. Going back to column 11, please, for one
14 second.

15 The statement we were looking at,
16 line 59, where it says "to ensure a disalignment
17 margin it is necessary to extend the contact holes
18 sufficiently over the gate electrodes," do you have
19 an understanding of what it means to -- when it
20 says "sufficiently over the gate electrodes 18"?

21 A. Yeah, that it remain over the gate
22 electrode; that it doesn't -- because, see, if it's
23 not over the gate electrode, you get it the way
24 it's shown in 3B; that it's -- half is over the
25 gate and half of it is off -- off the gate

1 electrode.

2 Q. When it says "sufficiently over the gate
3 electrodes," is it referring to a specific portion
4 of the hole being formed over the electrode?

5 MR. CHEN: Objection to form.

6 THE DEPONENT: I mean, if the -- if part
7 of it is not over the gate electrode, it -- it
8 would impact the -- the spacer that it's trying to
9 create. It -- it impact also where you create a
10 diffusion region and -- see, if you look at 3B,
11 region 38, and we have the arrow or the wavy line
12 from the bottom pointing for region 38, and this
13 portion of the source drain is where you do the
14 implant, a deeper implant.

15 And you need to be able to control and
16 ensure that this implant is far -- far enough from
17 the gate so you can create -- call it likely dope
18 junction or you have a region underneath the
19 spacer. So this why you want to make sure that
20 the -- the photoresist -- the mask for photoresist
21 region 28 in figure 2A is remaining above the gate
22 18.

23 Q. (By Mr. Colaianni) So is it enough for
24 any portion or any part of the contact hole to be
25 formed over the gate electrode?

1 A. Well, you want -- so, see, to create the
2 spacer, it's a very tight process here we are
3 talking that you have to gate to be over the -- I
4 mean the photoresist to be over the gate, the
5 photoresist 28. And you want it to leave enough of
6 the layer 24 on the side of it exposed so you can
7 etch through it and create the spacer shape that
8 is -- I guess is layer 13, figure 2B.

9 Q. So when Nakamura says that the contact
10 holes are formed sufficiently over the gate
11 electrode, it's referring to the portions of the
12 openings of the contact holes 34 and 36 are formed
13 over the gate electrodes 18, correct?

14 MR. CHEN: Objection to form.

15 THE DEPONENT: Well, it says that there
16 are -- the edge of this contact hole is basically
17 where the gate electrode -- or where the region 28
18 end.

19 And he's talking here actually about
20 the -- the -- see, because this paragraph telling
21 you what happen as a result of where the resist 28
22 is, but it doesn't discuss resist 28. Because this
23 embodiment 2 is different. It's just talking about
24 what will happen if you follow the previous
25 embodiment, embodiment 1; you will get these

1 structures.

2 Q. (By Mr. Colaianni) But you agree that
3 this description here with respect to the formation
4 of the contact holes over the gate electrode
5 applies to the first embodiment, correct?

6 A. This description is referred to in
7 figure 3A and 3B, which are part of a -- the first
8 embodiment.

9 See, it says specifically in column 11,
10 line 43, roughly, starting -- "In the method for
11 fabricating semiconductor, according to the first
12 embodiment," he's talking where the contact hole
13 opening. And all this following is description in
14 the earlier paragraph -- in paragraph that starting
15 on line 36, he's talking about 3A and 3B and their
16 disadvantage; that he's trying to go around it,
17 during the process they describe in figure 4A to
18 4B.

19 Q. So in the first embodiment shown in
20 figure 2B, portions of the openings of the contact
21 hole 34 and 36 are formed above the gate
22 electrodes 18, correct?

23 MR. CHEN: Objection to form.

24 THE DEPONENT: He's talking -- I mean, in
25 figure 3A and 3B, when you have a misalignment

1 in -- in figure 2A to 2C, he's showing how they
2 optimize; perfectly done case of how the first
3 embodiment would look like.

4 Q. (By Mr. Colaianni) But -- but figure 2B
5 does show portions of the openings of the contact
6 holes 34 and 36 formed above the gate
7 electrodes 18, correct?

8 MR. CHEN: Objection to form --

9 THE DEPONENT: It is just an illustration
10 and you cannot really know by -- I cannot just take
11 it that the edge of the -- this gate electrode, the
12 photoresist that form the gate electrode 28, that
13 wouldn't be covering the -- the gate -- the gate
14 conductor 18 and the dielectric above it, 20.

15 Q. (By Mr. Colaianni) Well, but as it's
16 illustrated in figure 2B, you would agree that
17 portions of the openings of the contact holes 34
18 and 36 are formed over the gate electrodes,
19 correct?

20 A. I mean, the way it's -- if you use this
21 illustration, then you are going to get some cases
22 that you are getting showed by etchings for this
23 oxide above the conductor 18. So you wouldn't
24 design a process that -- a manufacturing process
25 with such a design that you are not protected, then

1 you won't get conductor.

2 Q. Well, that -- that may be your opinion.

3 But I'm just asking you the way it's illustrated in
4 figure 2B of the Nakamura reference, and that
5 figure does show the portions of the context hole
6 openings formed over the gate electrodes 18,
7 correct?

8 MR. CHEN: Objection to form.

9 THE DEPONENT: I mean, it's -- it's my
10 opinion that it's not shown accurately, because
11 most you can -- have you show of the implant going
12 through these edges. If it's not just protected,
13 it would affect the -- the polysilicon conductor.
14 And you can also create shorts, if you remove the
15 layer above the conductor. So, yeah, it's my
16 opinion that you would want it to be covered.

17 Q. (By Mr. Colaianni) You believe that
18 figure 2B is not accurate?

19 A. I believe it doesn't show the -- the full
20 case. It -- and it's not accurate. It -- a person
21 of ordinary skill in the art would know that you
22 need to protect the conductor from being shorted to
23 or being implanted to, during the steps that I
24 describe here.

25 Q. But you would agree that the way

1 figure 2B is, in fact, shown portions of the
2 openings of contact holes 34 and 36 are, in fact,
3 formed over the gate electrodes 18, right?

4 MR. CHEN: Objection to form.

5 THE DEPONENT: This illustration show
6 it's -- that the gates 28 is not go from edge to
7 edge of the gate conductor. But it's like the way
8 you are showing in figure 3A and 3B, you realize
9 it, is this embodiment is defective and has some
10 issues. So he, himself, knows that it's not a
11 perfect embodiment and it has issues.

12 Q. (By Mr. Colaianni) Well, I -- I
13 understand you believe there's issues with the
14 embodiment. But I'll ask you once more.

15 You agree with me that figure 2B, as it's
16 shown in Nakamura, shows portions of the openings
17 of contact holes 34 and 36 formed over the gate
18 electrodes 18, "yes" or "no"?

19 A. Even inventor of the Nakamura '944 agrees
20 that there is issues with embodiment 1. And,
21 yes -- I mean, it shows that the edge is not --
22 goes from fully above the gate.

23 Q. So you agree with me as to what figure 2B
24 shows on its face, correct?

25 MR. CHEN: Objection to form.

1 THE DEPONENT: The figure 2B, it shows
2 that the -- the gate -- I mean, the photoresist 28
3 and the -- it doesn't cover fully the gate. And
4 like the way I was saying, that even inventor knows
5 that this embodiment is defective.

6 Q. (By Mr. Colaianni) I understand that.
7 You said that several times.

8 A. Yeah, I know.

9 Q. But -- but you would agree with me that
10 what it does show is portions of the contact holes
11 34 and 36 formed over the gate electrodes, correct?

12 A. It shows both things.

13 Q. Okay. With respect to the problem that
14 you mentioned, a person skilled in the art, trying
15 to implement the first embodiment, would try to
16 address the misalignment problem, correct?

17 A. He will try, but -- I mean, it's -- the
18 inventor of the -- of this patent realize that it
19 won't be easy problem to address. And person
20 ordinarily skilled in the art wouldn't know exactly
21 how to avoid it because it's a complex problem and
22 these are very small structures; that you have
23 many, many of them on each die. And to make sure
24 that all of them are on there day in, day out, they
25 are fully refined and fully in the right place and

1 that the earlier layer defined correctly,
2 accurately and the later layer and in the alignment
3 between the layers to be defined accurately in
4 order to minimize and control the misalignment.
5 And it's -- it's related to many of the various
6 process steps at the die and earlier layers,
7 because misalignment is basically mean that you are
8 trying to align one layer to another.

9 You are trying to adjust the position of
10 the mask of the new layer relative to an earlier
11 layer, and the shape of the target on the wafer
12 that you are trying to align to is very specific
13 and it could vary. And so it's not something
14 that's simple; that a person skilled in the art
15 would be able to do it on his own.

16 Q. Well, but the Nakamura reference explains
17 how to address the misalignment problem, correct?

18 A. Nakamura says basically you shouldn't use
19 embodiment 1. This is why I said yesterday
20 embodiment 3, for example.

21 Q. And regardless, the way to -- of how to
22 address this problem, a person skilled in the art
23 would ensure that the contact holes 34 and 36 are
24 sufficiently formed over the gate electrode 18,
25 correct?

1 MR. CHEN: Objection to form.

2 THE DEPONENT: Nakamura doesn't believe
3 that it's possible to avoid this problem. This is
4 why I said yesterday that the teaching of Nakamura
5 that you have this misalignment problem, and this
6 is why it came with another embodiment.

7 Q. (By Mr. Colaianni) And he explains that
8 you would want to form the contact holes
9 sufficiently over the gate electrode, right?

10 A. Yeah, but he say it's extremely narrow,
11 which make the patterning difficult. He says
12 specifically extremely narrow and make it
13 difficult. And this is why he's going on with
14 suggesting the other embodiment. It's teaching
15 that it's extremely difficult to do it. And when
16 you are going down in smaller and smaller geometry,
17 it will become even more difficult and it wouldn't
18 be manufacturable.

19 MR. COLAIANNI: I don't think I have
20 further questions at this time for Dr. Maltiel.

21 MR. CHEN: Okay. Let's take a quick
22 break and --

23 MR. COLAIANNI: Sure.

24 MR. CHEN: -- give me five minutes and I
25 think...

1 MR. COLAIANNI: Sure.

2 THE VIDEOGRAPHER: The time is now

3 1:15 p.m. We're going off the record, Counsel.

4 (Recess taken.)

5 THE VIDEOGRAPHER: The time is 1:22 a.m.

6 We are now back on the record.

7 MR. CHEN: So I don't have any redirect.

8 MR. COLAIANNI: Okay.

9 THE VIDEOGRAPHER: This marks the end of
10 DVD 2 of 2 in the Volume II deposition of
11 Ron Maltiel. The time is 1:22 p.m. Counsel, we
12 are going off the record. Thank you.

13 (Deposition concluded at 1:22 p.m.)

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1 I, RON MALTIEL, do hereby declare under
2 penalty of perjury that I have read the foregoing
3 transcript; that I have made any corrections as
4 appear notes; that my testimony as contained
5 herein, as corrected, is true and correct.

6 Executed this ____ day of _____,
7 2015, at _____, _____.

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RON MALTIEL

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1 STATE OF CALIFORNIA) ss:

2 COUNTY OF CONTRA COSTA)

3

4 I, Rebecca L. Romano, CSR. 12546, do hereby
5 certify:

6 That the foregoing deposition testimony was
7 taken before me at the time and place therein set
8 forth and at which time the witness was
9 administered the oath;

10 That the testimony of the witness and all
11 objections made by counsel at the time of the
12 examination were recorded stenographically by me,
13 and were thereafter transcribed under my direction
14 and supervision, and that the foregoing pages
15 contain a full, true and accurate record of all
16 proceedings and testimony to the best of my skill
17 and ability.

18 I further certify that I am neither counsel
19 for any party to said action, nor am I related to
20 any party to said action, nor am I in any way
21 interested in the outcome thereof.

22 IN WITNESS WHEREOF, I have subscribed my name
23 this 12th day of November, 2015.

24

25

Rebecca L. Romano, RPR,

1	CSR. No 12546		
2	DEPOSITION ERRATA SHEET		
3	Case Name: Samsung Electronics Co., Ltd, et al vs.		
4	Home Semiconductor Corporation		
5	Name of Witness: Ron Maltiel		
6	Date of Deposition: November 10, 2015		
7	Reason Codes: 1. To clarify the record.		
8	2. To conform to the facts.		
9	3. To Correct transcript errors.		
10	Page _____	Line _____	Reason _____
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1 DEPOSITION ERRATA SHEET

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20 _____ Subject to the above changes, I certify that

21 the transcript is true and correct

22 _____ No changes have been made. I certify that

23 the transcript is true and correct.

24 _____

25 RON MALTIEL