

Samsung Electronics Co. LTD et al. (Petitioner)
v.
Home Semiconductor Co. (Patent Owner)

Trial No. IPR2015-00460
US 6,146,997



Before Hon. J.Y. Chang, J.B. Tornquist, and B.Z. Shaw,
Administrative Patent Judges

Agenda

- I. **The '997 Patent**
- II. Doshi's Anisotropic Etch Forms A Spacer
- III. Doshi Discloses Forming An Oxide Layer Over The Diffusion Region

The '997 Patent

- Invention is directed to a method of forming a self-aligned contact hole

[57]

ABSTRACT

A simplified method for forming a self-aligned contact hole is disclosed. The method comprises the steps of (a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon; (b) forming a conformal layer of etch barrier material overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode; (c) forming an insulating layer overlying the barrier layer; (d) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop; and (e) anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etch barrier material on the sidewall of the gate electrode.

IPR2015-00460, Ex. 1001, '997 Patent, Abstract

The '997 Patent

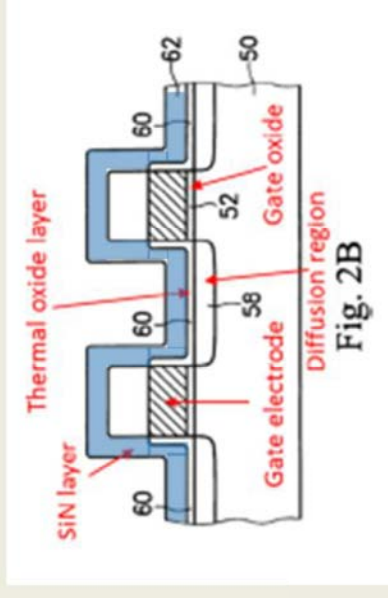
- A thin, conformal layer of silicon nitride 62 is deposited over the substrate surface.

19. Referring to the annotated Fig. 2B of the '997 patent below, after gate electrodes 54, diffusion regions 58, a thermal oxide layer 60, and gate oxides 52 have been formed on a substrate 50, a conformal layer of silicon nitride 62 is deposited over the substrate surface. *Id.*, col. 2:48-67. The '997 patent describes that the thermal oxide layer 60 is formed by rapid thermal oxidation. The '997 patent does not describe the purpose for forming the thermal oxide layer 60. There are a number of well-known reasons that one of ordinary skill in the art may wish to form a thermal oxide layer 60 after forming the gate electrodes 54. For example, the dry etch process used to form the gate electrodes 64 may create defects in the gate oxide that would affect the yield of the devices. The rapid thermal oxidation would reduce the defect density in the gate oxide, and improves the yield of the devices. Ex. 1009, p. 3.

IPR2015-00460, Ex. 1003, Rubloff 1st Dec. at Par. 4;
IPR2015-00460, Paper 1, Petition at p. 13

Referring to FIG. 2B, a conformal layer of silicon nitride 62 is deposited over the substrate surface using low pressure chemical vapor deposition (LPCVD). The conformal silicon nitride layer 62, as described earlier, acts as sidewall spacers of gate electrode 54 as well as an etch stop at contact hole etching. The conformal layer 62 preferably has a thickness of about 100 to 500 Å, and more preferably has a thickness of about 200 to 350 Å.

IPR2015-00460, Ex. 1001, '997 Patent.
at col. 2:60-67

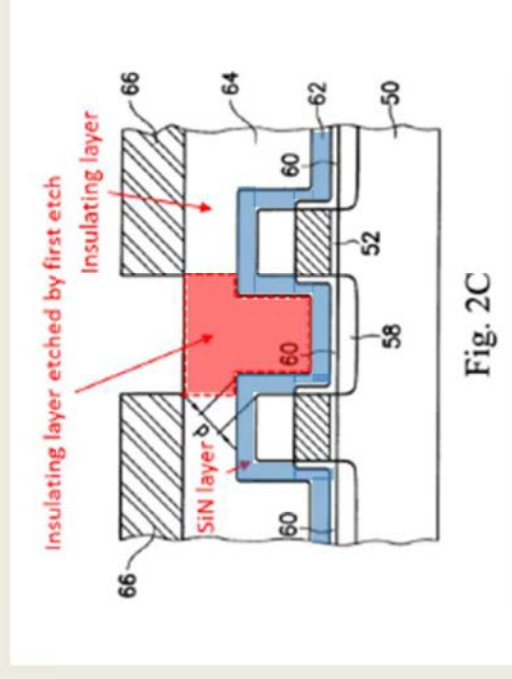


IPR2015-00460, Paper 1, Petition at p. 13

The '997 Patent

● First, selective, etch for a self-aligned contact hole

20. Referring to the annotated Fig. 2C of the '997 patent below, a planarized ILD insulating layer 64 is formed over the conformal layer of silicon nitride 62, and a photoresist layer 66 is formed and patterned to expose the contact hole. *Id.*, col. 3:1-24. First, a high selectivity etch is used to etch away the insulating layer 64 while minimally etching the silicon nitride layer 62, which performs as an etch stop in this step. *Id.* I have annotated Fig. 2C to show the region of the insulating layer that would be etched away by the first etch. The etch stops at the silicon nitride layer 62 because the etch is highly selective to silicon nitride.



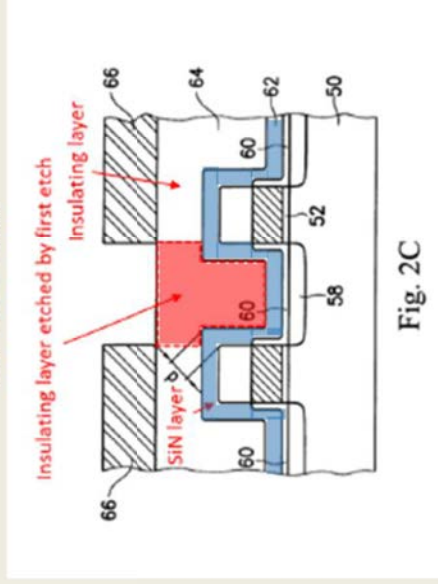
IPR2015-00460, Ex. 1003, Rubloff 1st Dec. at Par. 20;
IPR2015-00460, Paper 1, Petition at p. 13

IPR2015-00460, Paper 1, Petition at p. 14

The '997 Patent

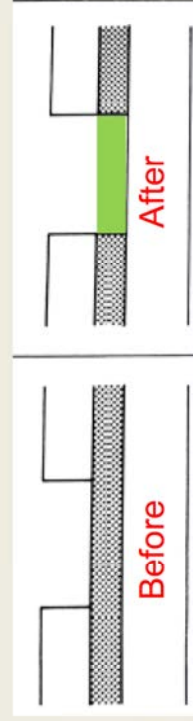
- Second, anisotropic, etch for a self-aligned contact hole

BPSG etch



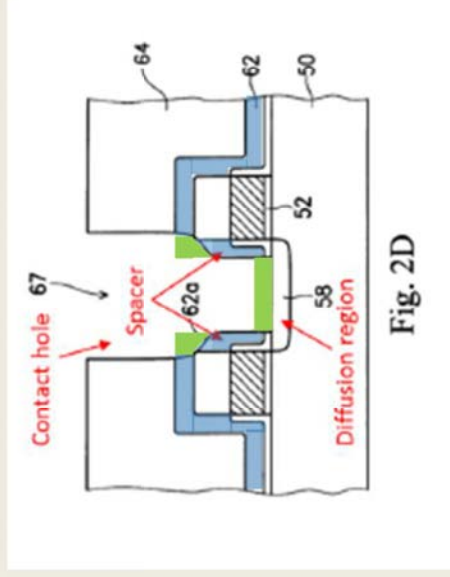
IPR2015-00460, Paper 1, Petition at p. 14

Anisotropic etch



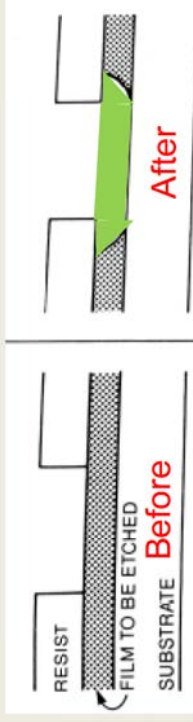
IPR2015-00460, Ex. 1014, Einspruch at p. 4;
IPR2015-00460, Ex. 1011, Rubloff 2nd Dec. at Par. 2B;
IPR2015-00460, Paper 21, Petitioner Reply at p. 13

Nitride etch



IPR2015-00460, Paper 1, Petition at p. 15

Isotropic etch



IPR2015-00460, Ex. 1014, Einspruch at p. 4;
IPR2015-00460, Ex. 1011, Rubloff 2nd Dec. at Par. 2C;
IPR2015-00460, Paper 21, Petitioner Reply at p. 13

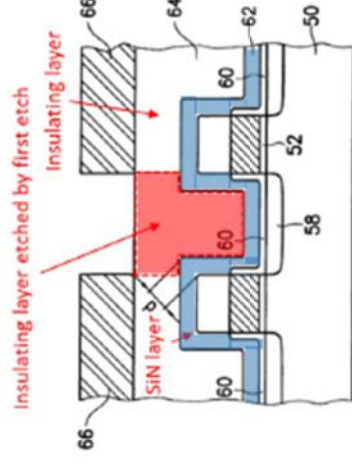
The '997 Patent

1. Thickness of nitride layer of 100 to 500 Å
2. Self-aligned contact hole
3. Anisotropic etch

The '997 Patent - Claim 1

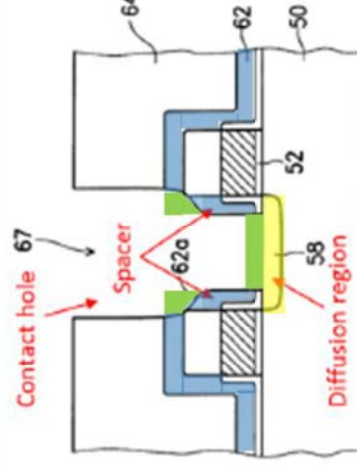
1. A method for forming a self-aligned contact hole, comprising the steps of:

- (a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon;
- (b) forming a conformal layer of etch barrier material overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode;
- (c) forming an insulating layer overlying the barrier layer;
- (d) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop; and
- (e) anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etch barrier material on the sidewall of the gate electrode.



BPSG etch Fig. 2C

IPR2015-00460, Paper 1, Petition at p. 14



Nitride etch Fig. 2D

IPR2015-00460, Paper 1, Petition at p. 15

Agenda

- I. The '997 Patent
- II. Doshi's Anisotropic Etch Forms A Spacer**
- III. Doshi Discloses Forming An Oxide Layer Over The Diffusion Region

1. A method for forming a self-aligned contact hole, comprising the steps of:

- (a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon;
- (b) forming a conformal layer of etch barrier material overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode;
- (c) forming an insulating layer overlying the barrier layer;
- (d) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop; and
- (e) anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etch barrier material on the sidewall of the gate electrode.

shown in FIG. 3a) defining the locations and sizes of the active regions and field oxide structures 5. Also in this example, gate structures 10 are formed as layered structures, including polysilicon layer 22 in contact with gate oxide 8, tungsten silicide layer 26 overlying polysilicon layer 22, and silicon nitride layer 30 overlying tungsten silicide layer 24.

IPR2015-00460, Ex. 1005, Doshi at col. 7:40-43
IPR2015-00460, Paper 1, Petition at p. 20

Following definition of gate structures 10, light "reach-through" implants are performed in a self-aligned manner relative to gate structures 10 to define source/drain extensions 6' (for p-channel devices), 7' (for n-channel devices), prior to the formation of sidewall filaments 11 along the sides of gate structures 10. According to the preferred embodiment of the invention, sidewall filaments 11 are

IPR2015-00460, Ex. 1005, Doshi at col. 7:52-55
IPR2015-00460, Paper 1, Petition at p. 21

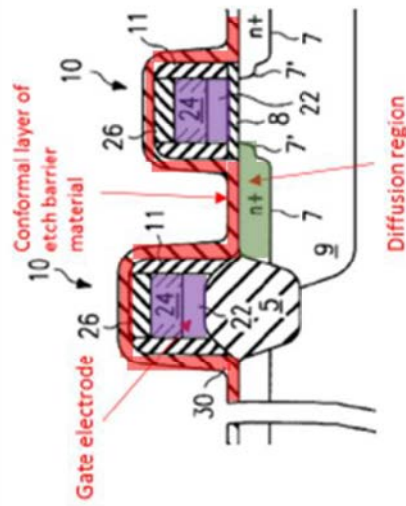


Fig. 3b, Doshi

IPR2015-00460, Paper 1, Petition at p. 22

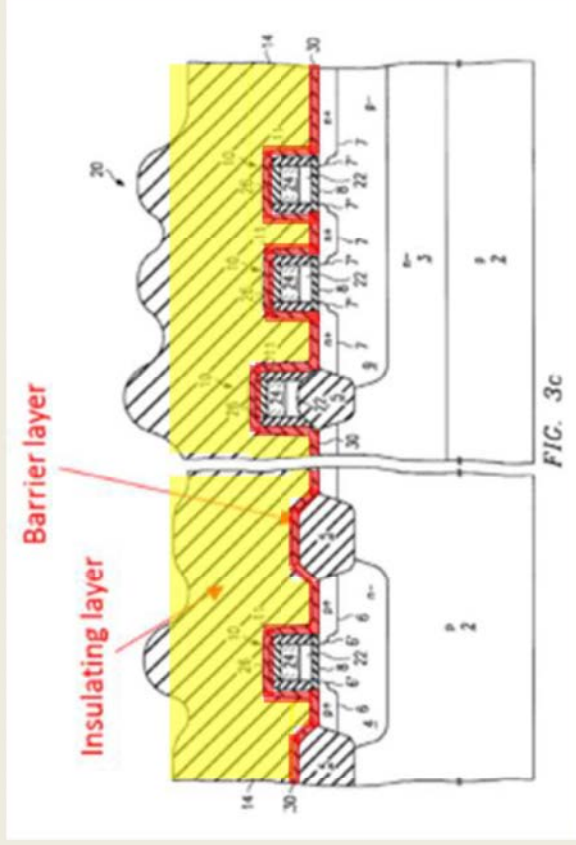
According to the preferred embodiment of the invention, silicon nitride layer 30 is now formed overall, preferably by way of low-pressure chemical vapor deposition (LPCVD), resulting in the structure illustrated in FIG. 3b. Nitride layer 30, as mentioned above and as described hereinbelow, will serve as a dopant barrier to boron and phosphorous residing in subsequently deposited doped silicon dioxide. It is preferred that nitride layer 30 be as thin as possible to minimize its etch time; however, nitride layer 30 must be sufficiently thick to have full integrity over the topography present in integrated circuit 20 to present a good barrier to dopant diffusion. In this embodiment of the invention, the thickness of nitride layer 30 may range from 65Å to 250 Å. The illustration of nitride layer 30 in FIG. 3b and the succeeding Figures is therefore not necessarily to scale.

IPR2015-00460, Ex. 1005, Doshi at col. 8:8-22
IPR2015-00460, Paper 1, Petition at pp. 21-22

U.S. No. 6,277,720 (“Doshi”)

1. A method for forming a self-aligned contact hole, comprising the steps of:

- (a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon;
- (b) forming a conformal layer of etch barrier material overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode;
- (c) forming an **insulating layer** overlying the **barrier layer**;
- (d) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop; and
- (e) anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etch barrier material on the sidewall of the gate electrode.



IPR2015-00460, Paper 1, Petition at p. 23

Referring now to FIG. 3c, integrated circuit 20 is illustrated after the deposition of doped BPSG silicon dioxide layer 14. BPSG layer 14 is preferably deposited in the conventional manner, for example by way of LPCVD, doped with both boron and phosphorous. As is well known in the

IPR2015-00460, Ex. 1005, Doshi at col. 8:23-27
IPR2015-00460, Paper 1, Petition at p. 23

1. A method for forming a self-aligned contact hole, comprising the steps of:

- providing a semiconductor substrate having a gate electrode and a diffusion region thereon;
- forming a conformal layer of etch barrier material overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode;
- forming an insulating layer overlying the barrier layer;
- etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop; and
- anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etch barrier material on the sidewall of the gate electrode.

According to this preferred embodiment of the present invention, etching of contact openings through BPSG layer 14 and nitride layer 30 is performed by way of a two-step etch. The first step is a "dry" etch of BPSG layer 14, carried out in a plasma etch reactor as known in the art, a preferred example of which is the TEL DRM reactor. In this preferred example, this first etch step is performed at a nominal pressure of 35 mtorr, at a nominal power level of 1700 watts, at a chamber temperature of 60° C., and at an electrode (and wafer) temperature of 20° C.; tolerance limits for each of these parameters is on the order of ±10%. The chemical species of the etch of BPSG layer 14 according to this preferred embodiment includes C_4F_8 at 10 sccm (±10%), CO at 240 sccm (±10%), and argon at 320 sccm (10%). Under these conditions, etching of BPSG layer 14 is relatively highly selective relative to etching of nitride layer 30, and as such the etch will tend to stop on nitride layer 30.

IPR2015-00460, Ex. 1005, Doshi at col. 9:34-50
IPR2015-00460, Paper 1, Petition at pp. 23-24

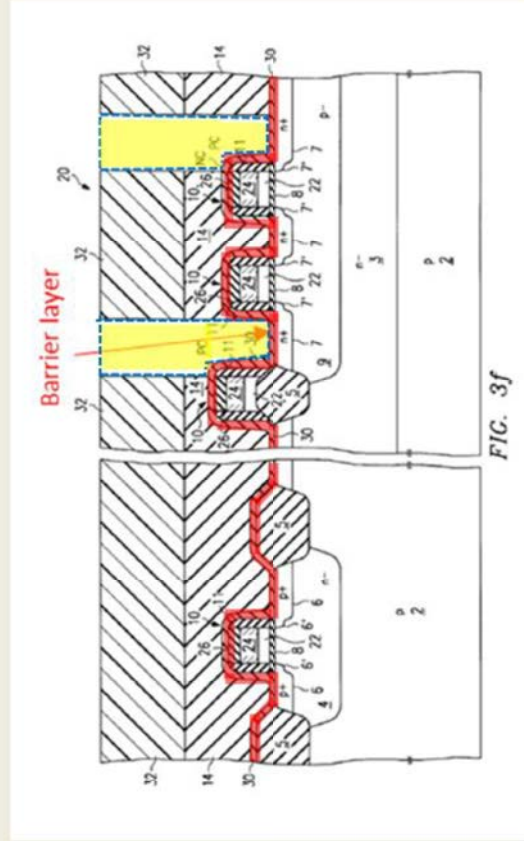


FIG. 3f

removed after development. The remaining portions of photoresist layer 32 serve, of course, as a mask for etch of the contact openings through BPSG layer 14 and nitride layer 30." Ex. 1005, col. 9:26-33 (emphasis added). One of ordinary skill in the art would understand that the two step etch described in Doshi is a self-aligned and borderless process.

IPR2015-00460, Ex. 1003, Rubloff 1st Dec. at Par. A-11
IPR2015-00460, Paper 1, Petition at pp. 23-24

Claim Construction – “Spacer”

● Petition:

Spacer = “a structure that spaces between two conductive structures.”

IPR2015-00460, Paper 1, Petition at pp. 9-10

● PTAB: No express construction required.

IPR2015-00460, Paper 11, Institution Decision at p. 8

According to a feature of the present invention, because the conformal nitride layer 62 is not etched until the contact opening is formed, it provides extra thickness d to protect the gate electrode 54 at the contact hole etching. Further, the same nitride layer is anisotropically etched to form sidewall spacers that prevent shorting between the gate electrode and the conductive plug.

IPR2015-00460, Ex. 1001, '997 Patent at col. 3:36-39;

IPR2015-00460, Paper 1, Petition at p. 9

formed on the substrate surface.” I believe that it would, because such an interpretation is not inconsistent with the '997 patent's specification and the understanding one of ordinary skill in the art would ascribe to this term when looking for the broadest reasonable construction.

IPR2015-00460, Ex. 1003, Rubloff 1st Dec. at Par. 24;

IPR2015-00460, Paper 1, Petition at pp. 9-10

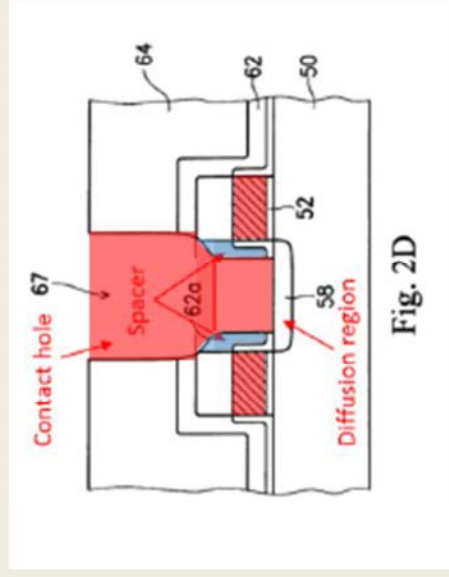


Fig. 2D

IPR2015-00460, Paper 1, Petition at p. 15

space·er \ˈspāṣər(r)\ n -s : one that spaces:

IPR2015-00460, Ex. 1007, Merriam Webster's Dictionary at p. 6;

IPR2015-00460, Paper 1, Petition at p. 9

Claim Construction – “Spacer”

● Patent Owner Response:

Spacer = “Purposefully Designed”

A person of ordinary skill in the art would understand that the term “spacer,” as it is used in the field of semiconductor fabrication, to mean a structure designed to creates physical separation between conducting structures. Maltiel Decl. at ¶ 40.

IPR2015-00460, Paper 18, PO Response at p. 7

defined function, such a construction would be unreasonably broad. A spacer is a structure that is purposefully designed into the fabrication process to achieve specific functions. Maltiel Decl. at ¶ 40. It is not just any material, no matter what size or shape, that spaces.

IPR2015-00460, Paper 18, PO Response at p. 8

Claim Construction – “Spacer”

● Petitioner Reply:

HSC’s construction should be rejected because it makes the touchstone of whether a structure is a spacer turn on a state of mind, i.e., intent, of a process designer, which is improper. See *Rowpar Pharm. Inc. v. Lornamead Inc.*, 2014 WL 1259777, at 9 (D. Ariz. Mar. 25, 2014) (Court rejected the words “desired effect” in a proposed construction as being “ambiguous” and as appearing “to focus on the intent of the manufacturer or users of the accused product” (emphasis added)); see also *Amazon.com, Inc. v. Barnesandnoble.com, Inc.*, 239 F.3d 1343, 1353 (Fed.Cir.2001) (“We are not prepared to assign a meaning to a patent claim that depends on the state of mind of the accused infringer.”) (Emphasis added). That

IPR2015-00460, Paper 21, Pet. Reply at pp. 2-3

Similarly, what happens if a process designer designed the structure to serve a purpose other than creating space but only later realizes or acknowledges that the structure also has the advantage of creating space between one conducting structure and another? According to HSC’s definition, such a structure would not be “purposefully designed” to create space and, therefore, would not be a spacer.

IPR2015-00460, Paper 21, Pet. Reply at p. 4

1. A method for forming a self-aligned contact hole, comprising the steps of:

- (a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon;
- (b) forming a conformal layer of etch barrier material overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode;
- (c) forming an insulating layer overlying the barrier layer;
- (d) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop; and
- (e) anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etch barrier material on the sidewall of the gate electrode.

It has been observed, in connection with the present invention, that the two-step etch of BPSG layer 14 and nitride layer 30 is particularly beneficial, as damage to the corners of gate structures 10 and sidewall filaments 11 is substantially minimized. In particular, sidewall corner locations NC illustrated in FIG. 3g have been observed to be particularly susceptible to damage from conventional nitride etches. However, the brief nitride etch used to clear nitride layer 30 from within plug contact locations PC has been observed to be highly anisotropic, and because of this anisotropy in combination with its brevity, minimizes damage at the sidewall corner locations NC of gate structures 10 in integrated circuit 20.

PR2015-00460. Ex. 1005. Doshi at col. 10:4-16

IPR2015-00460, Paper 1, Petition at pp. 25-26

IPR2015-00460, Paper 21, Pet. Reply at p. 14

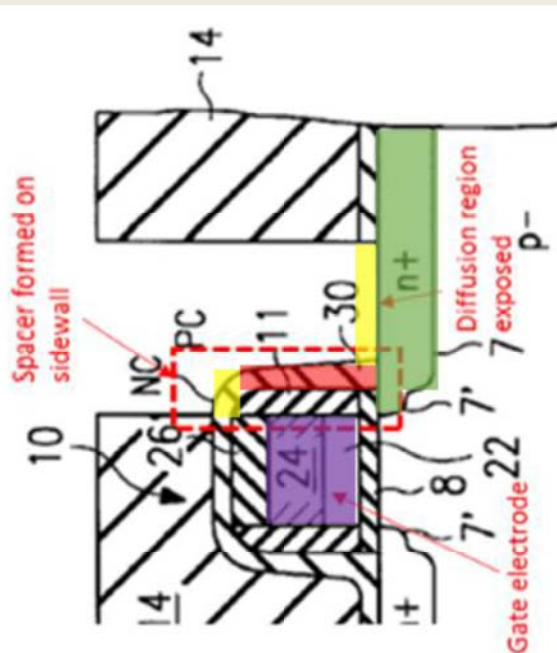


Fig. 3g, Doshi

IPR2015-00460, Paper 1, Petition at p. 27

Doshi discloses using a brief and highly anisotropic etch to minimize damage to gate structure 10 and sidewall filament 11

It has been observed, in connection with the present invention, that the two-step etch of BPSG layer 14 and nitride layer 30 is particularly beneficial, as damage to the corners of gate structures 10 and sidewall filaments 11 is substantially minimized. In particular, sidewall corner locations NC illustrated in FIG. 3g have been observed to be particularly susceptible to damage from conventional nitride etches. However, the brief nitride etch used to clear nitride layer 30 from within plug contact locations PC has been observed to be highly anisotropic, and because of this anisotropy in combination with its brevity, minimizes damage at the sidewall corner locations NC of gate structures 10 in integrated circuit 20.

IPR2015-00460, Ex. 1005, Doshi at col. 10:4-16
IPR2015-00460, Paper 1, Petition at pp. 25-27
IPR2015-00460, Paper 21, Pet. Reply at pp. 12-13

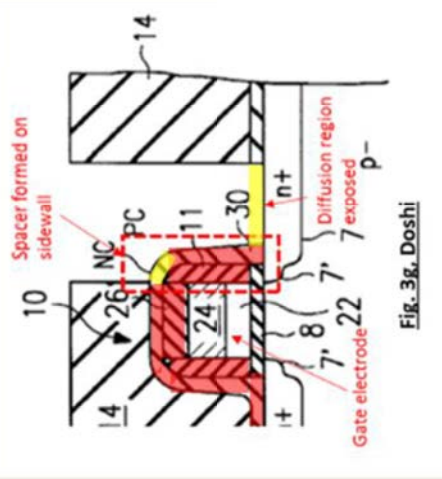


Fig. 3g, Doshi

IPR2015-00460, Paper 1, Petition at p. 22

(57)

ABSTRACT

A method of fabricating an integrated circuit, and an integrated circuit so fabricated, is disclosed. A silicon dioxide layer (14) that is doped with both boron and phosphorous, typically referred to as BPSG, is used as a planarizing layer in the integrated circuit structure, above which conductive structures (46, 52, 54) are disposed. A silicon nitride layer (30) is in place below the BPSG layer (14), and serves as a barrier to the diffusion of boron and phosphorous from the BPSG layer (14) during high temperature processes such as reflow and densification of the BPSG layer (14) itself. Contact openings (PC, BLC, CT) are etched through the BPSG layer (14) and the silicon nitride layer (30) using a two-step etch process. The first etch selectively etches silicon dioxide relative to silicon nitride, and thus stops on silicon nitride layer (30); besides serving as an etch stop, silicon nitride layer (30) protects underlying active regions (6, 7) from damage that may be caused by ionized oxygen released during oxide etch. A brief nitride etch is then used to clear silicon nitride layer (30), without damaging corner locations (NC) of the sidewall structures (11).

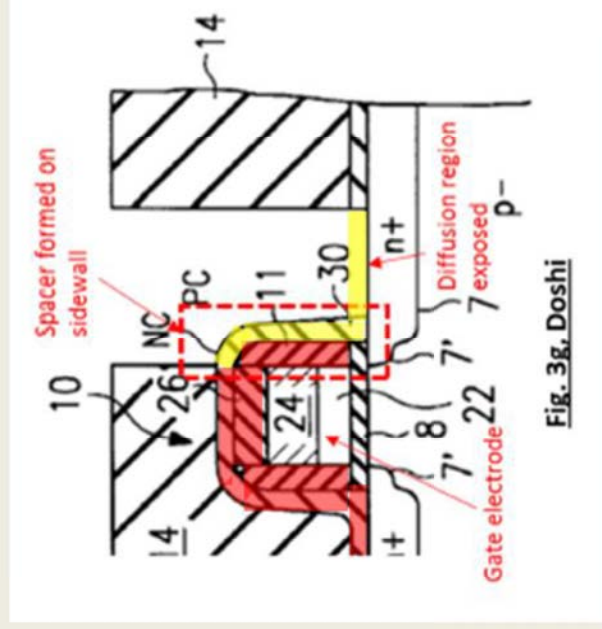
IPR2015-00460, Ex. 1005, Doshi at Abstract
IPR2015-00460, Paper 1, Petition at pp. 25-27
IPR2015-00460, Paper 21, Pet. Reply at pp. 12-13

HSC advocates the highly anisotropic etch removes every part of nitride 30

Figure 3g's errors are not confined to just the top corner. Maltiel Decl. at ¶

67. The nitride etch process designed to clear the nitride layer 30 would etch every part of layer 30 exposed under the contact opening. *Id.* Oddly, Fig. 3g shows the

IPR2015-00460, Paper 18, PO Response at p. 19



IPR2015-00460, Paper 1, Petition at p. 22

Complete removal of nitride on sidewall is inconsistent with Doshi's goal of minimizing damage

10. During this additional time, given that filaments 11 are partially formed of silicon nitride, the highly anisotropic silicon nitride etch would readily etch into the portions of the filaments 11 formed of nitride and, because of the physicality of highly anisotropic etches, would also etch into the portions of the filaments 11 formed of oxide, albeit likely to a lesser degree. Ex. 1005, col. 7:52-65.

Moreover, the silicon nitride layer 26 of the gate structures 10 also may be etched as the NC portion of gate structures 10 progressively become exposed during the over-etching needed to completely remove the film 30. A POSITA would have recognized that the damage caused by this over-etch is inconsistent with Doshi's disclosure that its etch "substantially minimize[s]" damage "to the corners of gate structures 10 and sidewall filaments 11." Ex. 1005, col. 10:4-16. A POSITA

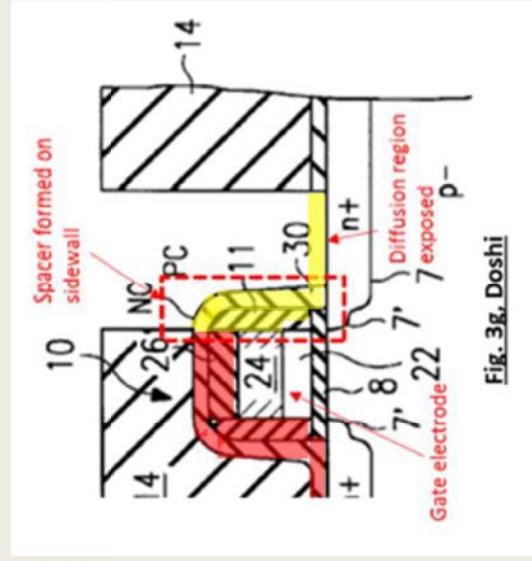


Fig. 3g, Doshi

IPR2015-00460, Paper 1, Petition at p. 22

Agenda

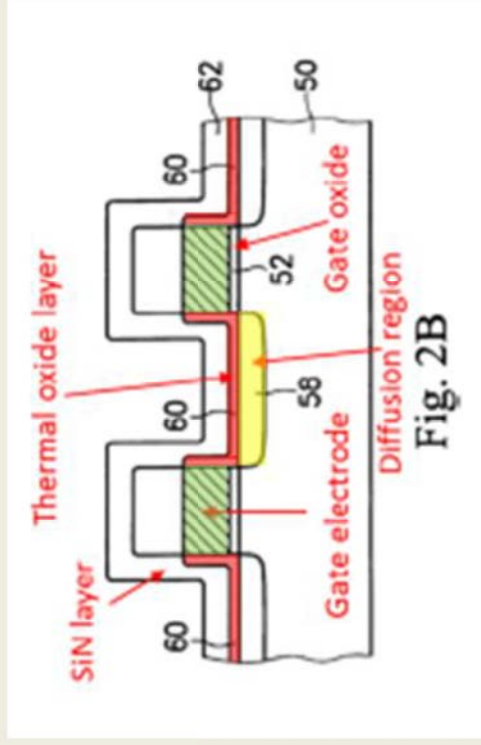
- I. The '997 Patent
- II. Doshi's Anisotropic Etch Forms A Spacer
- III. Doshi Discloses Forming An Oxide Layer Over The Diffusion Region**

The '997 Patent - Claims 2 & 9

2. The method as claimed in claim 1, further comprising a step of forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode by thermal oxidation prior to forming the barrier layer.

9. A method for forming a self-aligned contact hole, comprising the steps of:

- (a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon, said gate electrode comprising a capping layer;
- (b) forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode by thermal oxidation;
- (c) forming a conformal layer of silicon nitride overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode;
- (d) forming an insulating layer overlying the conformal layer of silicon nitride;
- (e) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the silicon nitride layer as an etch stop; and
- (e) anisotropically etching the silicon nitride layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of silicon nitride on the sidewall of the gate electrode.



IPR2015-00460, Paper 1, Petition at p. 13

Claim Construction – “Forming an oxide layer over the diffusion region”

- Petition: “forming an oxide layer above the diffusion region.”
- PTAB: No express construction required.

IPR2015-00460, Paper 1, Petition at pp. 7-9

IPR2015-00460, Paper 11, Institution Decision at p. 8

Referring to FIG. 1B, a conformal layer of silicon nitride 22 having a thickness of about 100 to 600 Å is deposited **over** the substrate surface using low pressure chemical vapor deposition (LPCVD). The conformal silicon nitride layer 22

IPR2015-00460, Ex. 1001, '997 Patent at col. 3:32-35;
IPR2015-00460, Paper 1, Petition at p. 8

to over \töve(r)\ adv [ME, adv. & prep., fr. OE *ofer*; akin to OHG *ufar*, adv., over, *ufar*, prep., over, ON *yfir*, adv. & prep., Goth *ufar*, prep., over, L *super*, adv. & prep., over, Gk *hyper*, adv. & prep., Skt *upari*, adv. & prep., over, OE *ufan* above. J 1 a (f) : from one point to another across an

\leave this new inquiry ~ in Monday ~ L. N. C. 1001, '997 Patent at col. 3:32-35;
you can stay ~> 3 a : ABOVE (the plane was directly ~>
b : so as to cover, conceal, or affect the whole surface or
expanse (the original logs were boarded ~> Amer. Guide
Series: Ark.) 4 a : at an end — often used in the phrase
over with (hiring) to set the business ~ with) b — used on a

IPR2015-00460, Ex. 1007, Merriam Webster's Dictionary at p. 4;
IPR2015-00460, Paper 1, Petition at p. 8

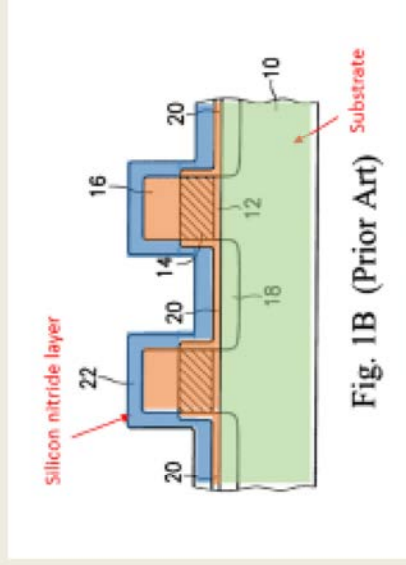


Fig. 1B (Prior Art)

IPR2015-00460, Paper 1, Petition at p. 9

Claim Construction – “Forming an oxide layer over the diffusion region”

- Patent Owner Response:

“Over” mandates “Covering”

Thus, the broadest reasonable interpretation of the term “forming an oxide layer over the diffusion region” in light of the specification in which it appears should be forming an oxide layer covering the diffusion region.¹

IPR2015-00460, Paper 18, PO Response at p. 10

Claim Construction – “Forming an oxide layer over the diffusion region”

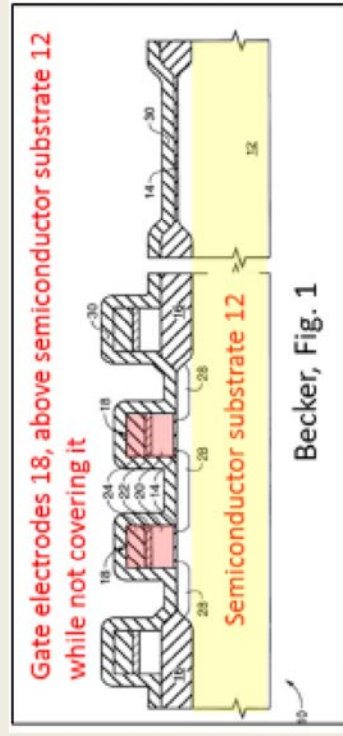
● Petitioner Reply:

At the outset, HSC's construction is too narrow and should be rejected. Under BRI, "limitations are not to be read into the claims from the specification." *In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993); Paper 11, p. 7. If HSC had intended for its claim to be limited to "covering" the diffusion region, HSC could have chosen to recite "covering"; it did not. HSC instead chose greater breadth through its recitation of "over." And, in this proceeding, HSC chose to maintain that breadth, as it forewent amending. Thus, HSC should not now be afforded amendment by fiat. See *In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989) ("during patent prosecution when claims can be amended, ambiguities should be recognized, scope and breadth of language explored, and clarification imposed.")

IPR2015-00460, Paper 21, Pet. Reply at p. 6

Moreover, within the specification of the '997 patent, the term "over" is applied consistent with the Merriam Webster's Dictionary definition to reference items that are above each other, even when separated by an intermediary item. Paper 1, p. 8; Ex. 1007, p. 4. Petitioner's proposed construction is also consistent with other literatures in this technology field, as cited in the Petition and not refuted by HSC. For example, U.S. Patent No. 5,770,498 ("Becker") discloses "forming a gate electrode over a semiconductor substrate." Ex. 1006, Abstract

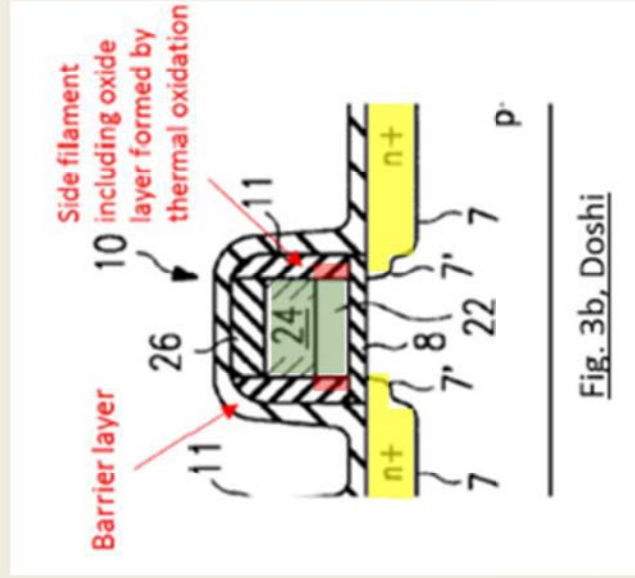
IPR2015-00460, Paper 21, Pet. Reply at p. 6



IPR2015-00460, Paper 21, Pet. Reply at p. 7

Doshi discloses forming an oxide layer on the sidewall of the gate electrode and above the diffusion region

2. The method as claimed in claim 1, further comprising a step of forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode by thermal oxidation prior to forming the barrier layer.



sides of gate structures 10. According to the preferred embodiment of the invention, sidewall filaments 11 are formed by first oxidizing the sides of polysilicon layer 22. A layer of silicon nitride is then deposited overall, and then etched anisotropically to remove the nitride from flat surfaces, leaving sidewall filaments 11 behind. As noted

IPR2015-00460, Ex. 1005, Doshi at col. 7:57-62
IPR2015-00460, Paper 1, Petition at pp. 27-29

IPR2015-00460, Paper 1, Petition at p. 28

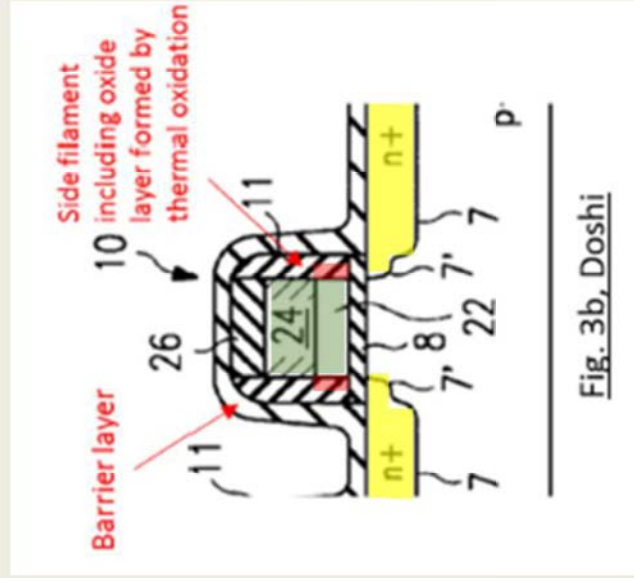
Claim limitation is met under Petitioner's and the Board's positions

As an initial matter, as established by Petitioner and undisputed by HSC, under Petitioner's proposed construction of the term "forming an oxide layer over the diffusion region," Doshi anticipates claims 2 and 9. Paper 1, pp. 27-29. Although the Board has determined that this term does not require express construction, the Board has also reached the conclusion that Doshi anticipates claims 2 and 9. Paper 11, pp. 8 and 15-16. HSC's proposed construction should be rejected for the reasons set forth above in Section(II)(B). Thus, Doshi anticipates claims 2 and 9 under either Petitioner or the Board's claim construction.

IPR2015-00460, Paper 21, Pet. Reply at pp. 23-24

Under HSC's construction, Doshi discloses forming an oxide layer over the diffusion region and on the sidewall of the gate electrode

2. The method as claimed in claim 1, further comprising a step of forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode by thermal oxidation prior to forming the barrier layer.



IPR2015-00460, Paper 1, Petition at p. 28

sides of polysilicon layer 22, thermal oxide is also formed over the source/drain regions because the source/drain regions are uncovered doped silicon, which is susceptible to thermal oxidation. Even if the source/drain regions were covered by a thin layer of gate oxide during the implantation step, one of ordinary skill in the art would recognize that the gate oxide covering the source/drain regions will grow thicker during the thermal oxidation of the gate structures 10.

IPR2015-00460, Ex. 1003, Rubloff 1st Dec at Par. A-7

Under HSC's construction, Doshi discloses forming an oxide layer over the diffusion region and on the sidewall of the gate electrode

regime. Thus a POSITA would have understood that a thicker oxide layer would be formed over the diffusion region during the thermal oxidation of the polysilicon gate sidewalls. That is, even if the diffusion region is covered by a gate oxide layer during the oxidation of the polysilicon gate sidewalls, a thicker oxide layer would still be formed during oxidation, and the resulting thickened oxide layer covers the diffusion region.

IPR2015-00460, Ex. 1011, Rubloff 2nd Dec at Par. 6B
IPR2015-00460, Paper 21, Pet. Reply at pp. 23-25

Appendix

Doshi discloses a brief and highly anisotropic etch

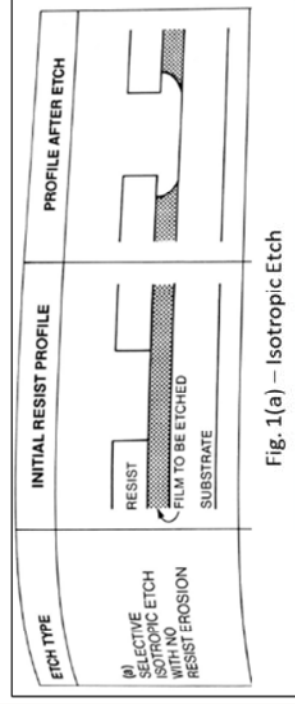
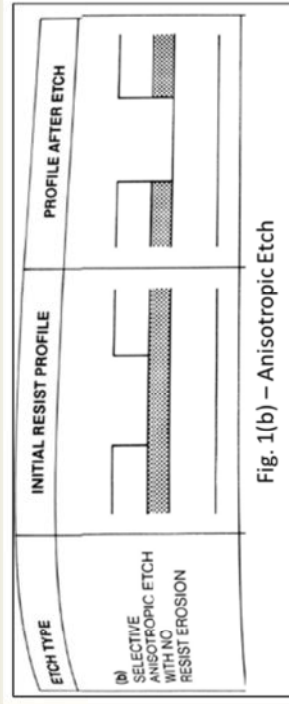
stated goal of minimizing damage to these structures. Ex. 1011, ¶ 2A. A POSITA would have understood that a highly anisotropic etch generally indicates that the etch rate in a perpendicular/vertical direction (i.e., etching from top to bottom) is much greater than the etch rate in a lateral/horizontal direction (i.e., etching from the side). Ex. 1014, p. 3; Ex. 1011, ¶¶ 2B-2C. Indeed, Mr. Maltiel stated that the taller the structure on the sidewall, the harder it would be to remove the structure:

Petitioner: "Do you believe there are some anisotropic etch processes that would -- that would completely remove the sidewall spacers?"

Mr. Maltiel: "That would completely remove? It's -- I mean, it would -- it depend on the -- the height of the structure that you're trying to -- that you make the space -- because the taller the structure is the -- I mean, the more have -- the spacer would be. So it would be harder to fully remove it."

Ex. 1012 at 159:7-15 (emphasis added).

IPR2015-00460, Paper 21, Pet. Reply at p. 13

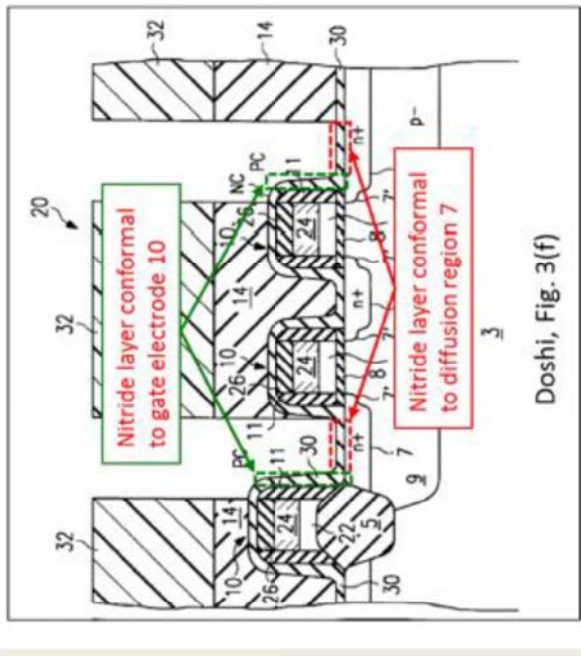


IPR2015-00460, Ex. 1014, Einspruch at p. 4
IPR2015-00460, Ex. 1011, Rubloff 2nd Dec. at Par. 2B-2C
IPR2015-00460, Paper 21, Pet. Reply at pp. 12-13

A POSITA would have understood that sidewall nitride would remain to form a spacer after Doshi's highly anisotropic etch

contact plug and the gate electrode. Thus, a POSITA would not have been led by Fig. or otherwise to believe that Doshi's highly anisotropic nitride etch completely removes the film 30 from Doshi's contact holes. A POSITA would have understood Doshi's description of brief nitride etching to clear nitride layer 30 from within PC or BLC region to mean that the brief and highly anisotropic nitride etch is used to clear the nitride layer 30 that is conformal to the diffusion region 7, without suggesting that such a brief and anisotropic etch would clear the nitride layer 30 that is conformal to the sidewall of the gate electrode 10.

IPR2015-00460, Ex. 1011, Rubloff 2nd Dec. at Par. 2E
IPR2015-00460, Paper 21, Pet. Reply at pp. 14-15



Doshi, Fig. 3(f)

IPR2015-00460, Ex. 1011, Rubloff 2nd Dec. at Par. 2E
IPR2015-00460, Paper 21, Pet. Reply at pp. 14-15

HSC: "Where does it say you will have remaining a nitride sidewall spacer?"
Dr. Rubloff: "It doesn't say it that way. It says it's a highly anisotropic etch, and it doesn't damage or remove much at the top at that corner above the sidewall filament. Therefore, one of ordinary skill would certainly conclude that that sidewall nitride structure remains [...] as a spacer."

IPR2015-00460, Ex. 2004, Rubloff 1st Depo. at 181:6-15
IPR2015-00460, Paper 21, Pet. Reply at p. 15

Complete removal of nitride on sidewall is inconsistent with Doshi's goal of minimizing damage

In particular, referring to FIG. 3g of Doshi, once the nitride film 30 covering the NC of filaments 11 and gate structures 10 is etched through via the faster vertical etching of the highly anisotropic nitride etch, the subsequent additional etching time used to remove the remaining sidewall portions of film 30 would result in etch of the NC portion of the filaments 11 and the gate structures 10. Ex. 1011, ¶ 2E. During this additional time, given that filaments 11 are partially formed of silicon nitride, the highly anisotropic silicon nitride etch would readily etch into the portions of the filaments 11 formed of nitride. Ex. 1005, col. 7:52-65; Ex. 1011, ¶ 2E. Moreover, the silicon nitride layer 26 of the gate structures 10 also may be etched as the NC portion of gate structures 10 progressively become exposed during the over-etching needed to completely remove the film 30. The damage caused by this over-etch is, simply put, inconsistent with Doshi's disclosure that its etch "substantially minimize[s]" damage "to the corners of gate structures 10 and sidewall filaments 11." Ex. 1005, col. 10:4-16; Ex. 1011, ¶ 2E.

IPR2015-00460, Paper 21, Pet. Reply at p. 14

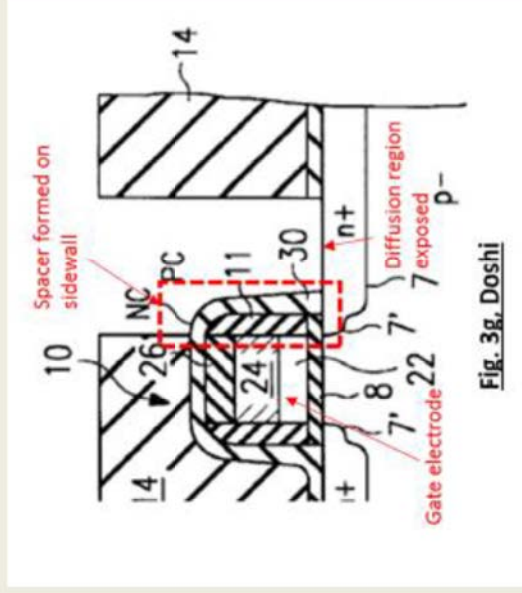
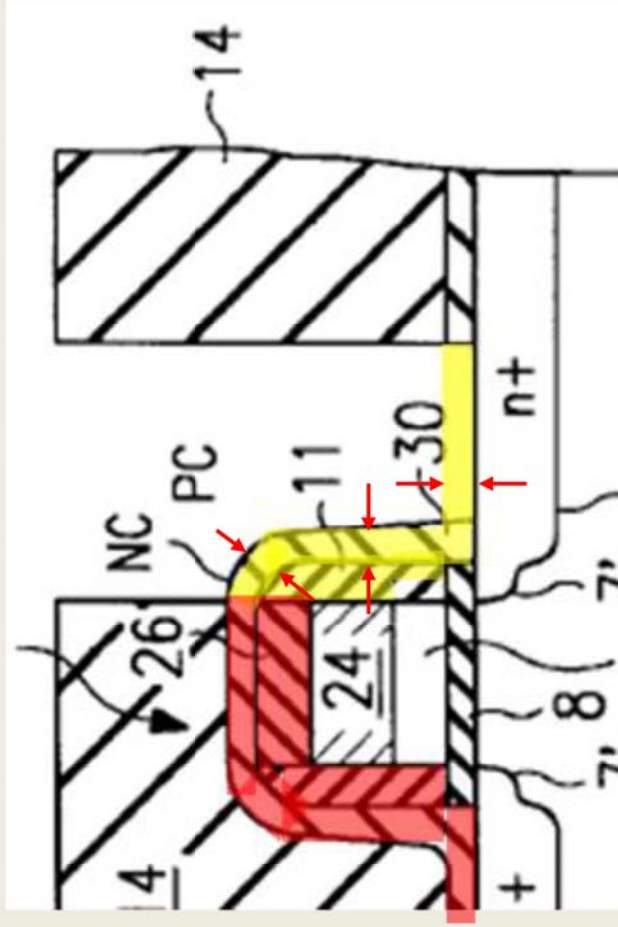


Fig. 3g, Doshi

IPR2015-00460, Paper 1, Petition at p. 27

Complete removal of nitride on sidewall is inconsistent with Doshi's goal of minimizing damage



Doshi, Fig. 3g

Complete removal of nitride on sidewall damages the diffusion region

For example, it is contemplated that channel lengths (i.e., the widths of gate structures 10 in the orientation of FIG. 2a) will be on the order of 0.35μ or less, and that the junction depths of source/drain regions 6, 7 will be on the order of 0.30μ . These extremely small critical dimensions not only result in high density and high performance integrated circuit operation, but also involve significant sensitivity to process variations and parameters.

IPR2015-00460, Paper 21, Pet. Reply at pp. 14-15
IPR2015-00460, Ex. 1005, Doshi at col. 6:57-64

Petitioner: "Without the oxide layer 60, the anisotropic etch of the conformal nitride layer 62 would etch the diffusion region 58, correct?"
Mr. Maltiel: "Well, unless you -- it's -- again, you have selectively with the nitride and the silicon. So when you etch the layer 60, you -- you still -- what I'm saying, *if you don't have the layer 60*, so when you etch the nitride layer 62, you still would be able to stop on the silicon. *You likely can damage it if you go for too long*. But if you have one controlled process, you would be able to manage it. But this is part of the reason why you have layer 60 there."

IPR2015-00460, Ex. 1012, Maltiel Depo, 156:2-14
IPR2015-00460, Paper 21, Pet. Reply at p. 17

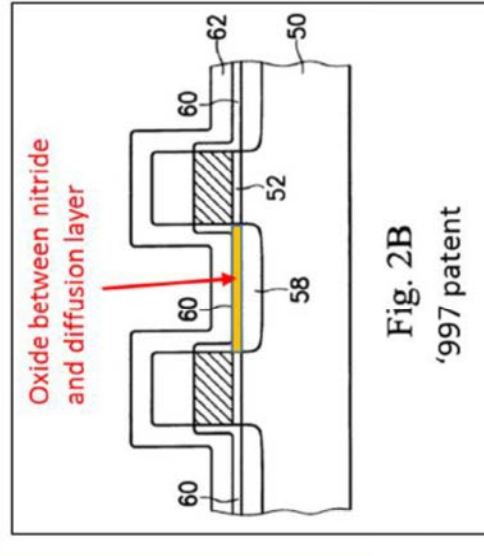
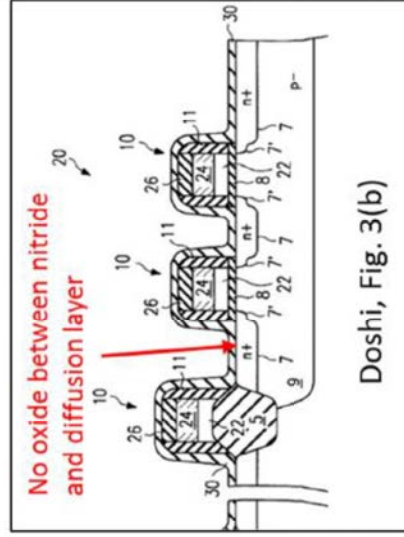


Fig. 2B
'997 patent



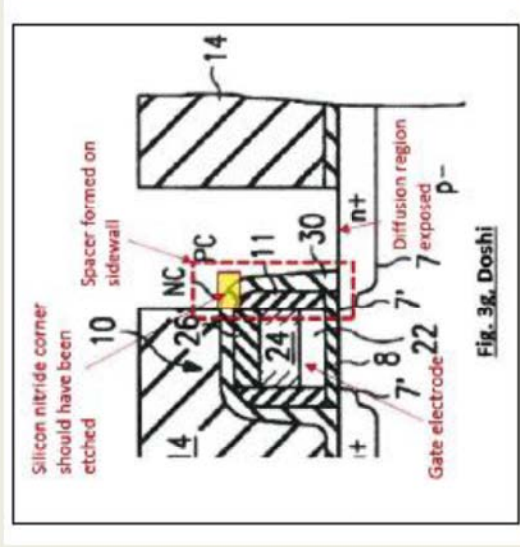
Doshi, Fig. 3(b)

IPR2015-00460, Ex. 1011, Rubloff 2nd Dec at Par. 2G
IPR2015-00460, Paper 21, Pet. Reply at p. 16

Petitioner relied on Fig. 3g, not Fig. 3k

HSC's argument to the contrary relies on Fig. 3k of Doshi that omits nitride 30 along its sidewalls when otherwise illustrating structures involved in bit line contact (BLC) formation. Petitioner never relied on Fig. 3k to satisfy the claims of the '997 patent, instead only relying on Fig. 3g, which clearly shows forming a spacer of nitride 30 along sidewalls as part of plug contact (PC) formation. The PC holes shown in Fig. 3g are not etched in the Fig. 3k rendering. HSC refers to

IPR2015-00460, Paper 21, Pet. Reply at p. 11



IPR2015-00460, Ex. 1003, Rubloff 1st Dec. at A-14
IPR2015-00460, Paper 18, PO Response at p. 19

Fig. 3k fails to show a self-aligned contact hole

Fig. 3k fails to show a self-aligned contact hole formed by Doshi's two-step etch process. Ex. 1011, ¶ 3A. That is, because Fig. 3k fails to show a self-aligned contact hole, gate structures 10 and sidewall filaments 11 are exposed to damage from etching as a result of even a minor mask misalignment. *Id.* A POSITA,

IPR2015-00460, Paper 21, Pet. Reply at p. 18

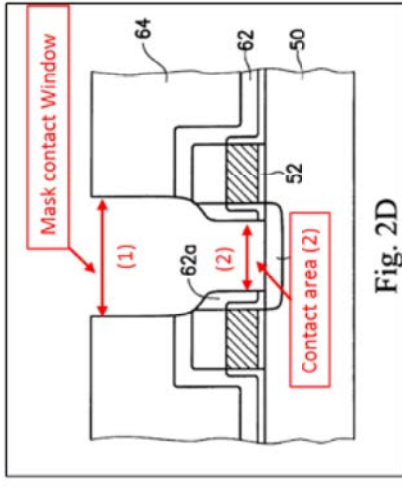


Fig. 2D

IPR2015-00460, Paper 21, Pet. Reply at p. 19
IPR2015-00460, Ex. 1011, Rubloff 2nd Dec. at Par. 3B

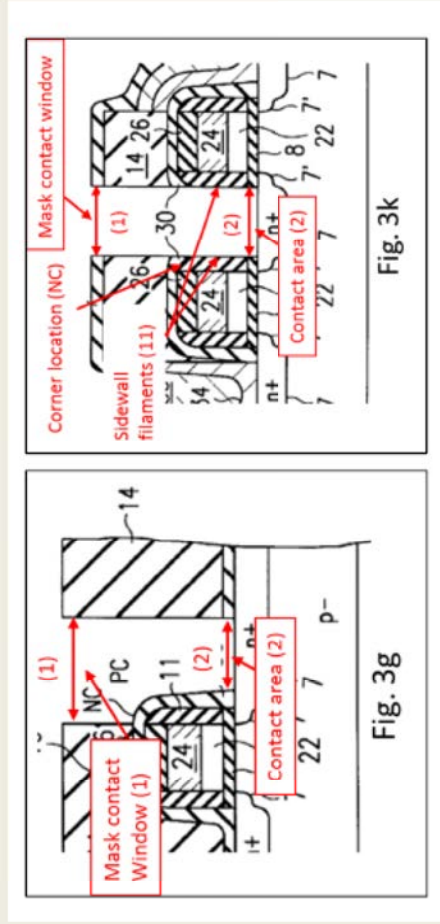


Fig. 3g

Fig. 3k

IPR2015-00460, Paper 21, Pet. Reply at pp. 19-20
IPR2015-00460, Ex. 1011, Rubloff 2nd Dec. at Par. 3E

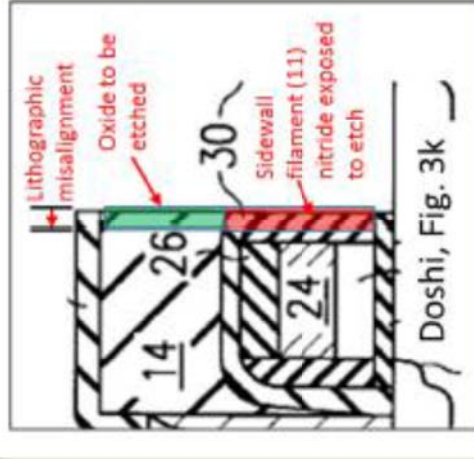
Fig. 3k is inconsistent with Doshi's disclosure

It has been observed, in connection with the present invention, that the two-step etch of BPSG layer 14 and nitride layer 30 is particularly beneficial, as damage to the corners of gate structures 10 and sidewall filaments 11 is substantially minimized. In particular, sidewall corner locations NC illustrated in FIG. 3g have been observed to be particularly susceptible to damage from conventional nitride etches. However, the brief nitride etch used to clear nitride layer 30 from within plug contact locations PC has been observed to be highly anisotropic, and because of this anisotropy in combination with its brevity, minimizes damage at the sidewall corner locations NC of gate structures 10 in integrated circuit 20.

IPR2015-00460, Ex. 1005, Doshi at col. 10:4-16

IPR2015-00460, Paper 1, Petition at pp. 25-27

IPR2015-00460, Paper 21, Pet. Reply at pp. 12-13



IPR2015-00460, Paper 21, Pet. Reply at p. 21

IPR2015-00460, Ex. 1011, Rubloff 2nd Dec. at Par. 3E

Indeed, the depiction of a contact hole in Fig. 3k would not be consistent

with a POSITA's understanding of a *self-aligned* contact hole, as there is no room

for any lithographic misalignment. *Id.* In other words, according to Fig. 3k as

revealed by the annotations shown below, any misalignment would result in

Doshi's highly anisotropic silicon nitride etch damaging the sidewall filaments 11

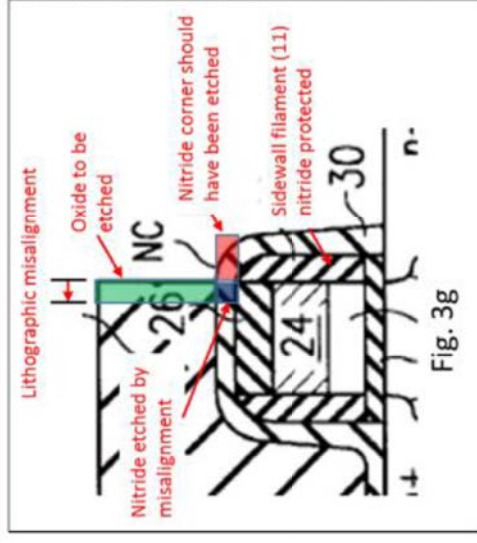
in a manner akin to that noted in Section(III)(B)(1)(i) above. Ex. 1005, col. 7:57-

62; Ex. 1011, ¶ 3E. This result directly contradicts Doshi's disclosure, and

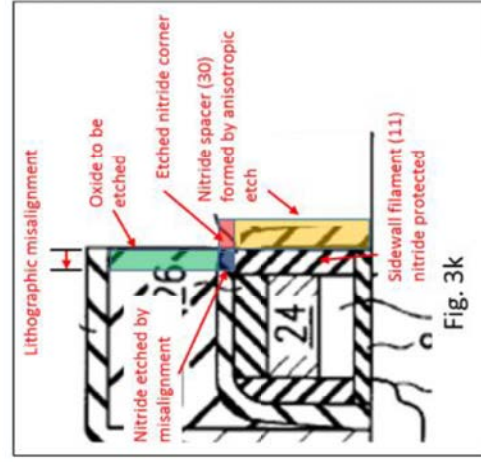
IPR2015-00460, Paper 21, Pet. Reply at p. 20

Fig. 3g is consistent with Doshi's disclosure

It has been observed, in connection with the present invention, that the two-step etch of BPSG layer 14 and nitride layer 30 is particularly beneficial, as damage to the corners of gate structures 10 and sidewall filaments 11 is substantially minimized. In particular, sidewall corner locations NC illustrated in FIG. 3g have been observed to be particularly susceptible to damage from conventional nitride etches. However, the brief nitride etch used to clear nitride layer 30 from within plug contact locations PC has been observed to be highly anisotropic, and because of this anisotropy in combination with its brevity, minimizes damage at the sidewall corner locations NC of gate structures 10 in integrated circuit 20.



IPR2015-00460, Ex. 1005, Doshi at col. 10:4-16
 IPR2015-00460, Paper 1, Petition at pp. 25-27
 IPR2015-00460, Paper 21, Pet. Reply at pp. 12-13



IPR2015-00460, Paper 21, Pet. Reply at pp. 12-13
 IPR2015-00460, Ex. 1011, Rubloff 2nd Dec. at 3F

The '997 Patent

Self-alignment is a technique in which multiple levels of regions on the wafer are formed using a single mask, thereby eliminating the alignment tolerance required by additional masks. This powerful approach is being used more often as circuit sizes decrease. Self-aligned contacts are often used in memory cells where contacts are limited only by the spacers and field oxide bird's beak or a contact window landing pad. Therefore, the mask contact window can be oversized relative to the contact area underneath, and no contact borders are needed, resulting in significant space saving. Referring to FIGS. 1A-1E, a conventional process of forming a self-aligned contact hole is illustrated in cross-sectional views. The process will be described as follows.

IPR2015-00460, Ex. 1001, '997 Patent.
at col. 1:11-23

Proper inquiry is whether Doshi's anisotropic etch forms a spacer

gate electrode.” By comparing Fig. 3f and Fig. 3g of Doshi, it is clear that Doshi's anisotropic nitride etch process etches the nitride barrier layer 30 underneath the PC opening, and simultaneously forms a spacer that is physically different from the unetched pre-existing spacer. It is this second etch-formed spacer that satisfies the claim. Moreover, HSC's reliance on Dr. Rubloff's testimony is misleading, as HSC has omitted statements made by Dr. Rubloff after the statements quoted by HSC, where he acknowledged that whether Doshi discloses a structure that may function as a spacer before the nitride etch process is not the right inquiry:

HSC: “So it is not a spacer?”
 Dr. Rubloff: “Well, a diffusion barrier is a kind of spacer.”
 HSC: “Okay. So it is a spacer?”
 Dr. Rubloff: “Yes.”
 HSC: “Okay.”
 Dr. Rubloff: “But that's not the spacer that's at issue here. I realize that.”
 HSC: “I don't follow you.”
 Dr. Rubloff: “No. I think your question was, at this stage after both etches of BPSG and nitride is done, how do we know there's still a nitride sidewall spacer? And that's a different -- that's a different question.”

IPR2015-00460, Paper 21, Pet. Reply at p. 23
 IPR2015-00460, Ex. 2004, Rubloff 1st Depo, 196:10-197:1
 IPR2015-00460, Ex. 1011, Rubloff 2nd Dec. at 4A

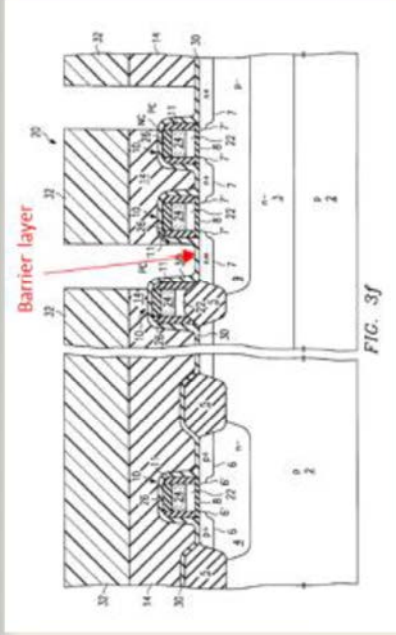


FIG. 3f

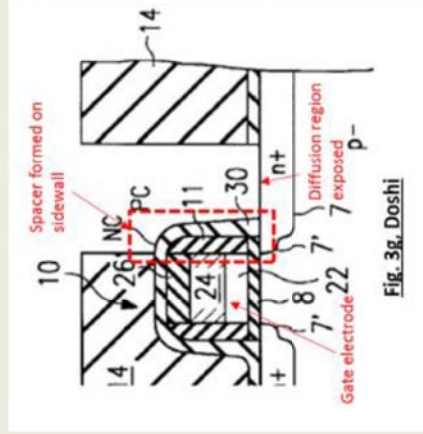


FIG. 3g, Doshi

IPR2015-00460, Paper 1, Petition at p. 27

Nitride etch is timed to stop as soon as nitride is cleared from the diffusion region

Q. Okay. When Doshi says that the damage is "substantially minimized," that indicates that the corners of gate structures 10 and sidewall filaments 11 will still suffer some damage; correct?

A. Well, this gets to zeros or not zeros.
(Laugh).

It indicates that there could be a very minimal amount of damage to the sidewall filaments. So if you look at the structure in FIG. 3G, which is I think the one you had -- had me looking at, the NC region starts the nitride removal etch with the nitride layer 30 covering the sidewall filaments 11 and the -- 3G -- and so this etch is intended to go through the nitride and then stop as soon as the silicon -- as the nitride is cleared from the diffusion region below.

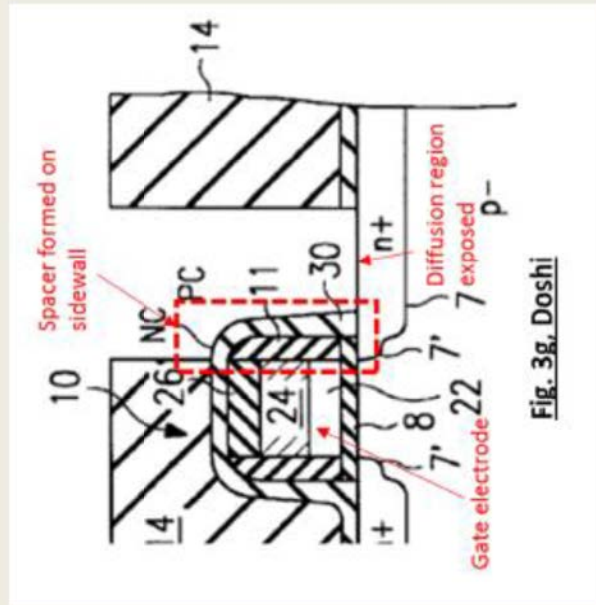


Fig. 3g, Doshi

IPR2015-00460, Paper 1, Petition at p. 27

Over-etch is used only to address a minor variation of thickness across the wafer

Q. So, for example, for some contacts, the nitride layer 30 might be a little bit thicker and for other contacts, the nitride layer 30 might be a little bit thinner; correct?

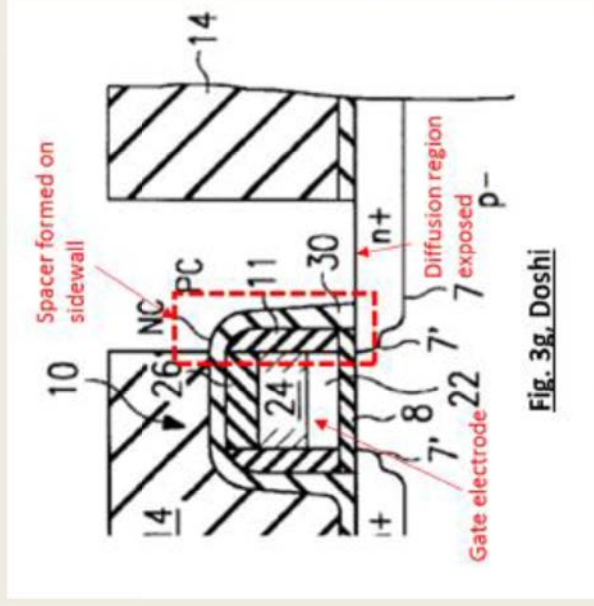
MR. COLAIANNI: Objection.

Hypothetical.

THE WITNESS: If you -- so -- so normally when people develop let's say the nitride CVD process, they will characterize uniformity across the wafer. These days you have, and in those days actually, that would have been 6- or 8-inch wafers, something like that. You will have

specifications that the RMS uniformity has to be 1 percent on thickness, something like that.

IPR2015-00460, Ex. 2006, Rubloff 2nd Depo. at 89:14 – 90:5



IPR2015-00460, Paper 1, Petition at p. 27

Doshi discloses thermal oxidation

Q. So Doshi doesn't specifically disclose thermal oxidation; correct?

MR. MUKERJI: Objection to form.

THE WITNESS: One of ordinary skill would interpret oxidizing any kind of silicon as thermal oxidation.

IPR2015-00460, Ex. 2004, Rubloff 1st Depo. at 172:17-22

Q. Well, how do you know that Doshi, when it says oxidizing the sides of the polysilicon layer, is referring to thermal oxidation as opposed to the other form of oxidation using the wet chemical electrodes?

A. If it were wet chemical, it would have said anodization because it's a standard way of describing it. Poured silicon is made this way, for example. And in this technology domain, silicon, oxidizing means you use O₂, or conceivably O₂ with some water, or conceivably N₂O, but it's a gas-phase process. Oxidizing means that what used to be silicon becomes a new compound.

IPR2015-00460, Ex. 2004, Rubloff 1st Depo. at 173:13 – 174:3

Thermal oxide is formed over the diffusion region during the oxidation of the polysilicon gate sidewalls

HSC: "And you said that during the oxidation process, an oxide layer would also be formed over the diffusion regions; is that correct?"

Dr. Rubloff: "Yes."

HSC: "And this is true if the diffusion region is uncovered silicon; correct?"

Dr. Rubloff: "Well, if it's -- *it's true if it's uncovered silicon, or if it's covered by thin oxide*. Because thermal oxide has linear growth rate in the thin regime. So if you already have a thin layer of oxide and you go to oxidizing conditions, you make it thicker."

IPR2015-00460, Ex. 2004, Rubloff 1st Depo, 171:19-172:13
IPR2015-00460, Paper 21, Pet. Reply at p. 25

Thermal oxide is formed over the diffusion region during the oxidation of the polysilicon gate sidewalls

Q. Well, but -- but during the oxidation of the sides of the polysilicon layer, that gate oxide region 8 would be exposed to further oxidation then, correct?

A. The top of the oxide is exposed, but the

IPR2015-00460, Ex. 1012, Maltiel Depo, 170:21-25

6B. I disagree with Mr. Maltiel's statement. Doshi discloses that the junction depths in MOSFET transistors with 0.5 μm channel lengths and smaller are typically on the order of 0.30 μm . Ex. 1005, col. 1:30-32. A POSITA would have understood that generally, for a 0.5 μm device channel length, the gate oxide layer would be on the order of a few nanometers. A POSITA would have understood that this oxide layer thickness would be within the linear growth rate regime. Thus a POSITA would have understood that a thicker oxide layer would be formed over the diffusion region during the thermal oxidation of the polysilicon gate sidewalls. That is, even if the diffusion region is covered by a gate oxide layer during the oxidation of the polysilicon gate sidewalls, a thicker oxide layer would still be formed during oxidation, and the resulting thickened oxide layer covers the diffusion region.

IPR2015-00460, Ex. 1011, Rubloff 2nd Dec. at 6B
IPR2015-00460, Paper 21, Pet. Reply at p. 25

The '997 Patent

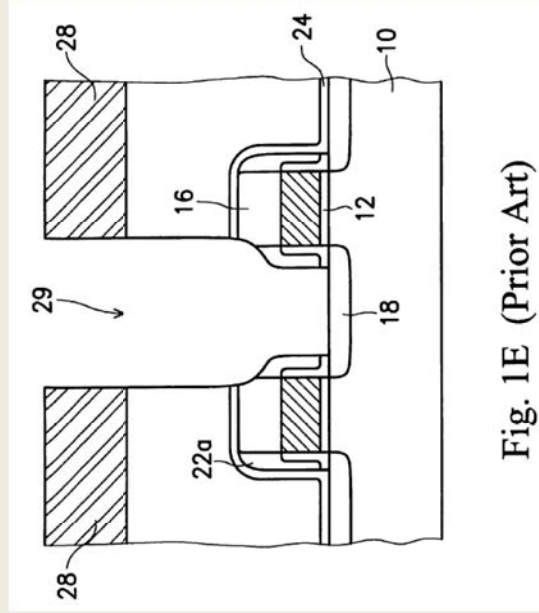


Fig. 1E (Prior Art)

Referring to FIG. 1E, using a photoresist mask 28, a contact hole 29 is etched in the insulating layer 26 with the barrier layer 24 serving as an etch stop, which is finally removed to expose the diffusion region 18. The etching of the insulating layer 26 is selective to the capping layers 16 and sidewall spacers 22a encapsulating the gate electrodes 14 so that the contact hole is self-aligning in nature.

IPR2015-00460, Ex. 1001, '997 Patent.
at col. 1:51-57

Argument Waived

B. DUE DATE 1

The patent owner may file—

- a. A response to the petition (37 C.F.R. § 42.120), and
- b. A motion to amend the patent (37 C.F.R. § 42.121).

The patent owner must file any such response or motion to amend by DUE DATE 1. If the patent owner elects not to file anything, the patent owner must arrange a conference call with the parties and the Board. The patent owner is cautioned that any arguments for patentability not raised in the response will be deemed waived.

IPR2015-00460, Paper 12, Scheduling Order at p. 3

The patent owner response is filed as an opposition to the petition and is subject to the page limits provided in § 42.24, §§ 42.120 and 42.220. The response should identify all the involved claims that are believed to be patentable and state the basis for that belief. Additionally, the response

Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012)

(emphasis added). As the Board has stated, our governing statute and Rules “clearly place some onus on the patent owner, once trial is instituted, to address the material facts raised by the petition as jeopardizing patentability of the challenged claims.” *Johnson Health Tech Co. v. Icon Health & Fitness, Inc.*, Case IPR2013-00463, slip op. at 12 (PTAB Jan. 29, 2015) (Paper 41). By addressing only the combination of the references, AAD

IPR2014-01156, Paper 36, Final Written Decision at p. 23
citing IPR 2013-00463, Paper 41 at p. 12