

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO. LTD,
SAMSUNG ELECTRONICS AMERICA, INC.,
SAMSUNG SEMICONDUCTOR, INC., and
SAMSUNG AUSTIN SEMICONDUCTOR LLC,
Petitioner,¹

v.

HOME SEMICONDUCTOR CORPORATION,
Patent Owner.

Case IPR2015-00460
Patent 6,146,997

Before JONI Y. CHANG, JON B. TORNQUIST, and BETH Z. SHAW,
Administrative Patent Judges.

SHAW, *Administrative Patent Judge.*

DECISION
Institution of *Inter Partes* Review

¹ Samsung Telecommunications America LLC, originally a real party-in-interest at the time of filing the Petition, no longer exists as a separate corporate entity, because it has merged with and into Samsung Electronics America, Inc. Paper 9.

IPR2015-00460
Patent 6,146,997

37 C.F.R. § 42.108

I. INTRODUCTION

Petitioner, Samsung Electronics Co. Ltd., Samsung Electronics America Inc., Samsung Semiconductor Inc., and Samsung Austin Semiconductor LLC (collectively “Samsung”), filed a Petition requesting an *inter partes* review of claims 1–14 of U.S. Patent No. 6,146,997 (Ex. 1001, “the ’997 patent”). Paper 1 (“Pet.”). Patent Owner, Home Semiconductor Corporation (“HSC”), did not file a Preliminary Response. We have jurisdiction under 35 U.S.C. § 314, which provides that an *inter partes* review may not be instituted unless the information presented in the petition “shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.”

For the reasons set forth below, we institute an *inter partes* review of claims 1–14 of the ’997 patent.

A. Related Matter

Samsung indicates that the ’997 patent is asserted in *Home Semiconductor Corporation v. Samsung Electronics Co. Ltd.*, No. 1:13-cv-02033 (D. Del.), filed December 16, 2013. Pet. 1.

B. The ’997 Patent

The ’997 patent relates to semiconductor device fabrication. Ex. 1001, 1:6–7. In particular, the ’997 patent discloses a method for forming a self-aligned contact hole. *Id.* at 1:5–10. The ’997 patent combines a spacer formation step and a contact hole exposure step into a single processing step to reduce the number of process steps. *Id.* at 1:65–67,

2:5–14, 3:40–47. The reduction of processing steps may reduce manufacturing costs and increase throughput. *Id.*

Figure 2B of the '997 patent is reproduced below (red annotations added by Samsung):

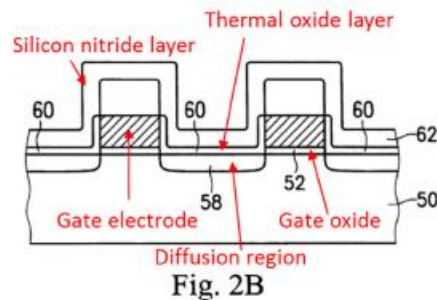


Figure 2B of the '997 patent illustrates that after gate electrodes 54, diffusion regions 58, thermal oxide layer 60, and gate oxides 52 have been formed on substrate 50, conformal layer of silicon nitride 62 is deposited over the substrate surface. *Id.* at 2:48–67.

Figure 2C of the '997 patent is reproduced below (red annotations added by Samsung):

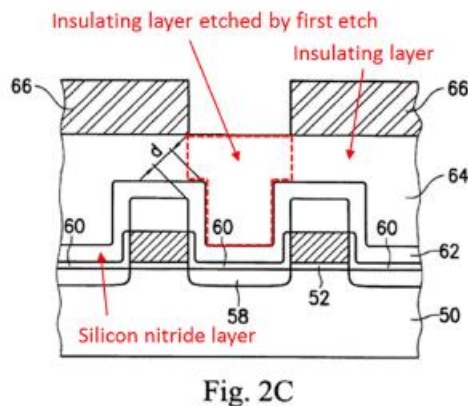


Figure 2C of the '997 patent illustrates planarized inter-layer dielectric insulating layer 64 formed over conformal silicon nitride layer 62, and photoresist layer 66 formed and patterned to expose contact hole 67. *Id.* at 3:1–24. An etch that is highly selective to silicon nitride layer 62 is performed to etch away insulating layer 64. *Id.*

Figure 2D of the '997 patent is reproduced below (red annotations added by Samsung):

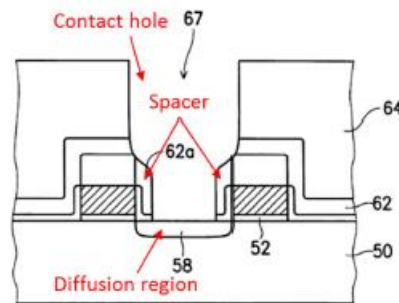


Fig. 2D

Figure 2D of the '997 patent illustrates that following the first selective etch of insulating layer 64, silicon nitride layer 62 is etched anisotropically to expose diffusion region 58. *Id.* at 3:1–24. Due to the directionality of the anisotropic etch, spacer 62a is formed on the sidewall of the electrode 54 during the same silicon nitride etch that exposes diffusion region 58 to complete contact hole 67. *Id.* After the contact hole 67 is filled with conductive material to form a conductive plug, spacer 62a can be used to prevent shorting between the gate electrode and the conductive plug. *Id.* at 3:33–39.

C. Illustrative Claim

Of the challenged claims, claims 1 and 9 are the only independent claims. Claims 2–8 depend, directly or indirectly, from claim 1; claims 10–14 depend from claim 9. Claim 1 reads as follows:

1. A method for forming a self-aligned contact hole, comprising the steps of:
 - (a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon;
 - (b) forming a conformal layer of etch barrier material overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode;
 - (c) forming an insulating layer overlying the barrier layer;
 - (d) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop; and
 - (e) anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etch barrier material on the sidewall of the gate electrode.

Ex. 1001, 3:54–4:4.

D. Prior Art Relied Upon

Samsung relies upon the following prior art references:

Doshi et al., U.S. Patent Number 6,277,720 B1, issued on Aug. 21, 2001 (Ex. 1005, “Doshi”).

Becker, U.S. Patent Number 5,770,498, issued on June 23, 1998 (Ex. 1006 (“Becker”).

Wong et al., *Process Induced Degradation of Thin Oxides*, PROC. 1ST INT. SYMP. ULTRA LARGE SCALE INTEGRATION SCI. TECHNOL. (1987) (Ex. 1009, “Wong”).

E. Asserted Grounds of Unpatentability

Samsung asserts the following grounds of unpatentability:

Challenged Claims	Basis	Reference(s)
1–14	§ 102(e)	Doshi
1 and 3–8	§ 102(b)	Becker
2 and 9–14	§ 103(a)	Becker and Wong

II. ANALYSIS

A. Claim Construction

In an *inter partes* review, claim terms in an unexpired patent are given their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b); *see also In re Cuozzo Speed Techs., LLC*, 778 F.3d 1271, 1281–82 (Fed. Cir. 2015) (“Congress implicitly adopted the broadest reasonable interpretation standard in enacting the AIA,” and “the standard was properly adopted by PTO regulation.”). We are mindful that “limitations are not to be read into the claims from the specification.” *In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993). Nevertheless, claims are not interpreted in a vacuum but are part of and read in light of the specification. *United States v. Adams*, 383 U.S.

39, 49 (1966) (“[I]t is fundamental that claims are to be construed in the light of the specifications and both are to be read with a view to ascertaining the invention.”). In that regard, the terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the Specification. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). The construction that stays true to the claim language and most naturally aligns with the inventor’s description is likely the correct interpretation. *Renishaw PLC v. Marposs Societa’ per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998).

Samsung proposes constructions for the following claim terms: “forming a conformal layer of [etch barrier material/silicon nitride] overlying the substrate,” “spacer,” and “etching an opening through the insulating layer self-aligned and borderless to the diffusion region,” which are recited in at least independent claims 1 and 9, and “forming an oxide layer over the diffusion region,” recited in claims 2 and 9. Pet. 5–10. For purposes of this decision, we determine that only the claim term discussed below requires express construction.

We construe “forming a spacer of the etch barrier on the sidewall of the gate electrode,” as recited in claim 1, as not requiring the spacer to be in direct contact with the gate electrode. *See* Pet. 57. This is consistent with the Specification of the ’997 patent, which does not require the spacers to touch the gate electrode directly. *See* Ex. 1001, Fig. 2D, 3:20–21.

B. Principles of Law

For a prior art reference to serve as an anticipatory reference, it must disclose every limitation of the claimed invention, either explicitly or inherently. *In re Schreiber*, 128 F.3d 1473, 1477 (Fed. Cir. 1997). We must analyze prior art references as an ordinary artisan would. *See Scripps Clinic & Res. Found. v. Genentech, Inc.*, 927 F.2d 1565, 1576 (Fed. Cir. 1991) (stating that to anticipate, “[t]here must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention”), *overruled on other grounds by Abbott Labs. v. Sandoz, Inc.*, 566 F.3d 1282 (Fed. Cir. 2009).

C. Anticipation of Claims 1–14 by Doshi

Samsung asserts that claims 1–14 are unpatentable under 35 U.S.C. § 102(e) as anticipated by Doshi. Pet. 19–36. To support its contentions, Samsung provides detailed explanations as to how Doshi meets each claim limitation. *Id.* Samsung also relies upon a Declaration of Dr. Gary W. Rubloff, for his technical testimony concerning the ’997 patent and prior art references. Ex. 1003. We begin our discussion with a brief summary of Doshi, and then we address Samsung’s contentions.

1. Priority Date

Samsung asserts Doshi qualifies as prior art at least under 35 U.S.C. § 102(e) because the patent application of Doshi was filed in the United States before the earliest potential priority date of May 11, 1999, of Taiwanese Patent Application No. 88107602. Pet. 3. Specifically, Doshi

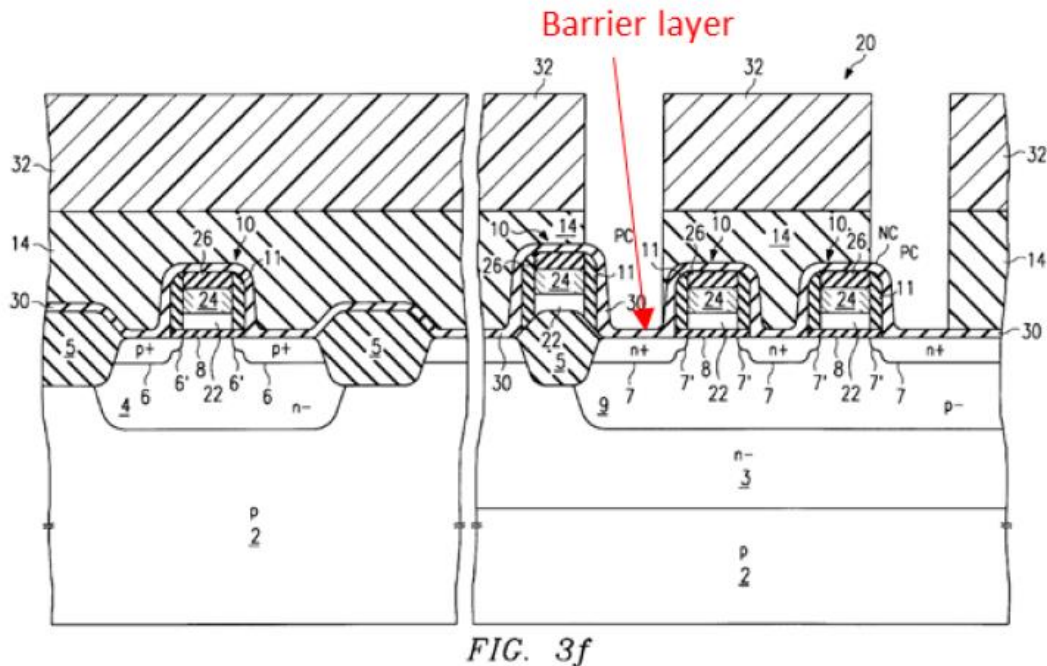
was filed on June 10, 1998 as application number 09/095,432, and claimed benefit of U.S. provisional application No. 60/051,287 (“the ’287 provisional,” Ex. 1008), filed on June 30, 1997.

On this record, we are persuaded that the ’287 provisional discloses common subject matter as the Doshi disclosure relied upon by Samsung in challenging claims 1 to 14 of the ’997 patent. Ex. 1008, 1. Specifically, both Doshi and the ’287 provisional include Figures 1, 2a to 2c, and 3a to 3k. Additionally, column 4, line 66 to column 7, line 28 of Doshi describes Figures 2a to 2c in detail, while page 10, line 2 to page 14, line 3 of the ’287 provisional include the same corresponding descriptions. Similarly, column 7, line 29, to column 11, line 21, of Doshi describes Figures 3a to 3k in detail, while page 14, line 4 to page 20, line 13 of the ’287 provisional also include the same corresponding descriptions. Accordingly, based on this record, we find the effective prior art date for Doshi is June 30, 1997.

2. Summary

Doshi discloses a method of fabricating an integrated circuit, including a method of fabricating contact openings. *See* Ex. 1005, Abstract. According to Doshi, gate electrode structures 10 and doped source/drain diffusion regions 7 and 7’ are fabricated on a semiconductor substrate 2. Ex. 1005, 7:29–8:7. Figure 3d of Doshi is reproduced below (red annotations added by Samsung):

Samsung directs our attention to Figure 3f of Doshi, reproduced below (red annotations added by Samsung):



Samsung argues Figure 3f shows etching an opening through BPSG layer 14 to diffusion region 7 by using silicon nitride layer 30 as an etch stop. As support, Samsung cites to the following disclosure in Doshi:

According to this preferred embodiment of the present invention, etching of contact openings through BPSG layer 14 and nitride layer 30 is performed by way of a two-step etch. ***The first step is a “dry” etch of BPSG layer 14***, carried out in a plasma etch reactor as known in the art, a preferred example of which is the TEL DRM reactor. [. . .] Under these conditions, etching of BPSG layer 14 is relatively highly selective relative to etching of nitride layer 30, and as ***such the etch will tend to stop on nitride layer 30***.

Pet. 24 (citing Ex. 1005, 9:34–50). On this record, we determine that Samsung has demonstrated sufficiently for purposes of this Decision that Doshi describes the etch through BPSG layer 14 will stop on nitride layer 30, which discloses etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop, as recited in independent claims 1 and 9.

4. Simultaneously forms a spacer of silicon nitride on the sidewall of the gate electrode structure

Samsung contends that Doshi describes a second etch of silicon nitride that exposes the diffusion region and simultaneously forms a spacer of silicon nitride on the sidewall of the gate electrode structure, as required by independent claims 1 and 9. Pet. 18. Based on this record, we are persuaded by Samsung's contention.

Samsung directs our attention to Figure 3g of Doshi, reproduced below (red annotations added by Samsung).

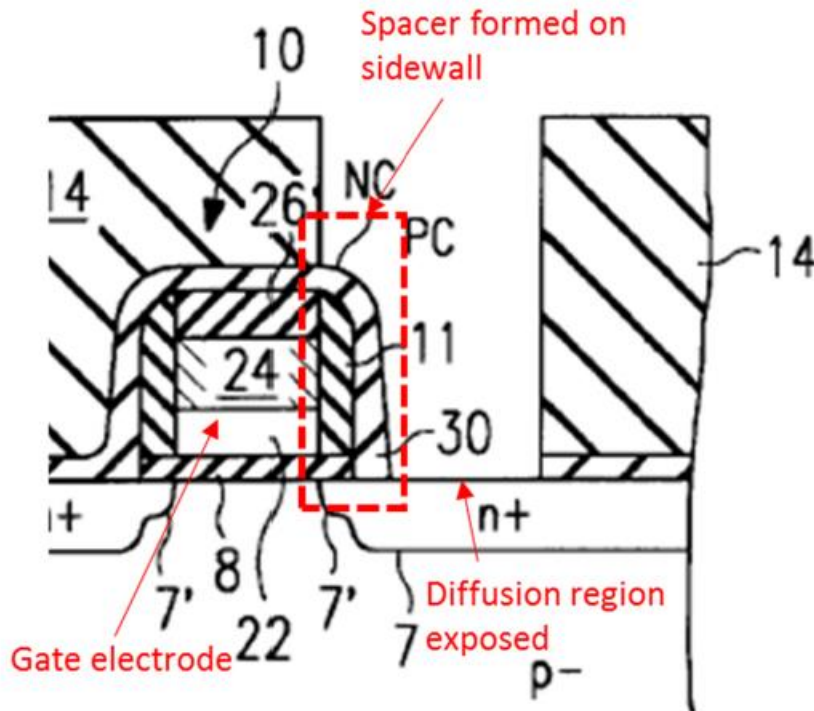


Fig. 3g, Doshi

Indeed, annotated Figure 3g of Doshi “illustrates the construction of integrated circuit **20** after the completion of both etch steps, and the stripping of photoresist layer **32**.” Ex. 1005, 9:65–67. After the second etch, the silicon nitride layer **30** remaining on the sidewall of gate electrode **10** acts as a spacer, which provides a space as well as electrical insulation between gate electrode **10** and the contact plug to be filled in the contact hole.

For the foregoing reason, we determine that Samsung has established sufficiently for purposes of this Decision that Doshi describes anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the

etch barrier material on the sidewall of the gate electrode, as recited in the claims at issue.

5. Forming an oxide layer over the diffusion region

Samsung contends that Doshi describes forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode, as required by claims 2 and 9, and forming the oxide layer by thermal oxidation prior to forming the barrier layer, as required by claim 2. Pet. 27–29, 34.

Doshi describes that sidewall filaments 11 are formed by first oxidizing the sides of polysilicon layer 22. Ex. 1005, 7:52–59. Figure 3b of Doshi is reproduced below (annotations by Samsung):

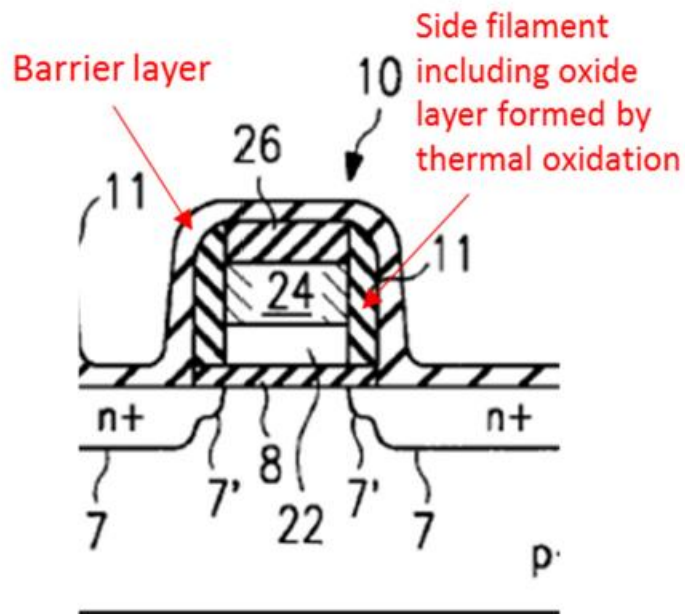


Fig. 3b, Doshi

Figure 3b illustrates that the barrier layer (i.e., the silicon nitride layer

30) is formed *after* the formation of the filaments 11, and therefore, we agree that Doshi discloses forming an oxide layer on the sidewalls of the gate electrode by thermal oxidation prior to forming the barrier layer.

For the foregoing reason, we determine that Samsung has established sufficiently for purposes of this Decision that Doshi discloses forming an oxide layer on the sidewalls of the gate electrode, as recited in claims 2 and 9, and forming the oxide layer by thermal oxidation prior to forming the barrier layer, as required by claim 2.

6. Dependent Claims 3–8 and 10–13

Samsung contends that claims 3–8 and 10–13 are anticipated by Doshi. Pet. 29–33, 35–36. As support, Samsung provides detailed explanations as to how the combination of prior art meets each claim limitation. *Id.* Samsung also relies upon the Declaration of Dr. Rubloff (Ex. 1003).

Upon consideration of Samsung’s explanations and supporting evidence, we are persuaded by Samsung’s contentions. For example, with respect to claims 3 and 10, which requires that said gate electrode comprises a capping layer of silicon nitride, Samsung directs our attention to Doshi, which discloses “**gate structures 10** are formed as layered structures, including polysilicon layer 22 in contact with gate oxide 8, tungsten silicide layer 24 overlying polysilicon layer 22, and silicon nitride layer 26 overlying tungsten silicide layer 24.” Pet. 20, 29 (Ex. 1005, 7:40–43)). With respect to claim 4, which requires the barrier layer is a silicon nitride layer, Samsung directs our attention to Doshi, which discloses “[a]ccording to the

preferred embodiment of the invention, *silicon nitride layer 30* is now formed overall, preferably by way of low-pressure chemical vapor deposition (LPCVD), resulting in the structure illustrated in FIG. 3b.” (Pet. 30 (citing Ex. 1005, 8:8–11)).

Dependent claims 5 and 11 require that “said barrier layer has a thickness between about 100 to 500Å.” Samsung directs our attention to Doshi, which discloses that “the thickness of nitride layer 30 may range from **65Å to 250Å**” (Pet. 30 (citing Ex. 1005, 8:19–20)). Samsung argues the ’997 patent fails to demonstrate any criticality of the recited thickness of between about 100 to 500 Å, and therefore, the claim is anticipated by Doshi’s disclosure of a thickness from 65 to 250 Å. Pet. 30.

“[W]hen, as by a recitation of ranges or otherwise, a claim covers several compositions, the claim is ‘anticipated’ if *one* of them is in the prior art.” *Titanium Metals Corp. of Am. v. Banner*, 778 F.2d 775, 782 (Fed. Cir. 1985). If there is no allegation of criticality of the claimed range, or any demonstration that the prior art reference fails to teach one of ordinary skill in the art how to use the claimed invention, then the claim may be anticipated even if the exact range is not disclosed. *See ClearValue, Inc. v. Pearl River Polymers, Inc.*, 668 F.3d 1340, 1345 (Fed. Cir. 2012).

Based on this record, we are persuaded by Samsung’s argument that Doshi anticipates the claimed range. Moreover, we find that the ’997 patent describes, in its “Description of the Related Arts,” with respect to Figure 1D which is labeled “Prior Art,” that a “barrier layer is typically a silicon nitride

layer having a thickness of about 100 to 500 Å.” Ex. 1001, 1:44–46, Fig. 1D.

Given the evidence in this record, we determine that Samsung has demonstrated a reasonable likelihood of prevailing on its assertions that claims 3–8 and 10–13 are unpatentable over the aforementioned combinations of prior art references.

D. Conclusion

For the foregoing reasons, we determine that Samsung has demonstrated a reasonable likelihood of prevailing on its assertion that independent claims 1–14 are anticipated by Doshi.

E. Other Asserted Grounds

As summarized in Section I(E) of this Decision, Petitioner asserts three grounds of unpatentability. Under 37 C.F.R. § 42.108(a), the Board has discretion to “authorize the review to proceed on all or some of the challenged claims and on all or some of the grounds of unpatentability asserted for each claim.” The Board also “may deny some or all grounds for unpatentability for some or all of the challenged claims.” 37 C.F.R. § 42.108(b); *see also* 35 U.S.C. § 314(a) (permitting institution of review under certain conditions, but not mandating institution of review under any conditions). In making such determinations, the Board considers 37 C.F.R. § 42.1(b), which requires “the just, speedy, and inexpensive resolution of every proceeding.”

We have determined to institute a trial on one of the three grounds. The two grounds upon which we do not institute a trial rely at least in part

on Becker. In this case, the decision not to authorize *inter partes* review on the other two patentability challenges is based on the claim construction of “forming a spacer of the etch barrier on the sidewall of the gate electrode,” as not requiring the spacer to be in direct contact with the gate electrode. As Petitioner states, Becker discloses a spacer of silicon nitride that is formed in direct contact with the sidewall of the gate electrode. Pet. 57. Therefore, we determine that we need not institute a trial on the other two grounds. Instituting a trial on those two patentability challenges would impede “the just, speedy, and inexpensive resolution of every proceeding” as required under 37 C.F.R § 42.1(b). In other words, considering multiple grounds for the same patentability issue unnecessarily would consume the time and resources of all parties involved.

CONCLUSION

For the foregoing reasons, we determine that the information presented in the Petition establishes that there is a reasonable likelihood that Samsung would prevail in challenging claims 1–14 of the ’997 patent as unpatentable. At this juncture, we have not made a final determination with respect to the patentability of the challenged claims, nor with respect to claim construction.

III. ORDER

For the foregoing reasons, it is

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review is hereby instituted for the following ground of unpatentability:

Claims 1–14 under 35 U.S.C. § 102(e) as anticipated by Doshi;

FURTHER ORDERED that no other ground of unpatentability asserted in the Petition is authorized for this *inter partes* review; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial will commence on the entry date of this decision.

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