

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO. LTD.,
SAMSUNG ELECTRONICS AMERICA, INC.,
SAMSUNG SEMICONDUCTOR INC., and
SAMSUNG AUSTIN SEMICONDUCTOR LLC,
Petitioner,

v.

HOME SEMICONDUCTOR CORPORATION,
Patent Owner

Case IPR2015-00460
Patent 6,146,997

**PATENT OWNER HOME SEMICONDUCTOR CORPORATION'S
RESPONSE TO PETITION FOR *INTER PARTES* REVIEW OF
UNITED STATES PATENT NO. 6,146,997**

Mail Stop PATENT BOARD
Patent Trial and Appeal Board
United States Patent and Trademark Office
PO Box 1450
Alexandria, Virginia 22313-1450

TABLE OF CONTENTS

	Page(s)
I. INTRODUCTION	1
II. RELIEF REQUESTED	2
III. OVERVIEW OF THE '997 PATENT	2
IV. HOME SEMICONDUCTOR'S PROPOSED CLAIM CONSTRUCTIONS	6
A. "spacer" (claims 1 and 9)	7
B. "forming an oxide layer over the diffusion region"	8
C. Samsung's Other Proposed Constructions	11
V. DOSHI DOES NOT ANTICIPATE THE CHALLENGED CLAIMS.....	12
A. Doshi Does Not Anticipate Claims 1, 2, and 9 Of The '997 Patent	12
1. Summary of Doshi	13
2. Doshi Does Not Anticipate Independent Claims 1 and 9 Because It Does Not Describe Simultaneously Etching and Forming A Spacer on the Sidewall of the Gate Electrode	16
3. Doshi Does Not Anticipate Claim 2 or Claim 9	24
VI. CONCLUSION.....	28

TABLE OF AUTHORITIES

	Page(s)
Cases	
<i>In re Cuozzo Speed Techs., LLC</i> , 793 F.3d 1268 (Fed. Cir. 2015)	6, 7
<i>Phillips v. AWH Corp.</i> , 415 F.3d 1303 (Fed. Cir. 2005)	12
<i>In re Schreiber</i> , 128 F.3d 1473 (Fed. Cir. 1997)	12
<i>Scripps Clinic & Res. Found. v. Genentech, Inc.</i> , 927 F.2d 1565 (Fed. Cir. 1991), <i>overruled on other grounds by</i> <i>Abbott Labs. v. Sandoz, Inc.</i> , 566 F.3d 1282 (Fed. Cir. 2009)	12
<i>Wahpeton Canvas Co. v. Frontier, Inc.</i> , 870 F.2d 1546 (Fed. Cir. 1989)	13
Other Authorities	
37 C.F.R. § 42.100(b)	6
37 C.F.R. § 42.120	1

I. INTRODUCTION

Pursuant to 37 C.F.R. § 42.120, Patent Owner Home Semiconductor Corporation (“Home Semiconductor”) hereby responds to the Petition for *Inter Partes* Review (“Pet.”) filed by various Samsung entities seeking cancellation of claims 1-14 (“Challenged Claims”) of U.S. Patent No. 6,146,997 (SAM-1001, hereinafter the “’997 patent”). The Board initiated this proceeding on one of the grounds proposed by Samsung – whether the Challenged Claims were anticipated under Section 102(e) by U.S. Patent No. 6,277,720 to Doshi (SAM-1005, hereinafter “Doshi”). Paper No. 11 at 20.

Doshi does not anticipate the Challenged Claims because Doshi does not disclose a process where spacers are formed on the side of the gate simultaneously with the etching process. Samsung’s sole evidence on this point is a drawing that has acknowledged errors, and thus fails to meet Samsung’s burden to prove invalidity by a preponderance of the evidence. For the reasons set forth below, as well as the facts provided by the Declaration of Ron Maltiel (Exh. 2002, hereinafter “Maltiel Decl.”) and the cross-examination of Samsung’s expert (Exhs. 2004 and 2005, hereinafter “Rubloff Tr.”), Home Semiconductor contends that all challenged claims are patentable, and requests that this Board so hold.

II. RELIEF REQUESTED

Home Semiconductor submits that the Board should hold that the Challenged Claims are patentable over the cited art – Doshi.

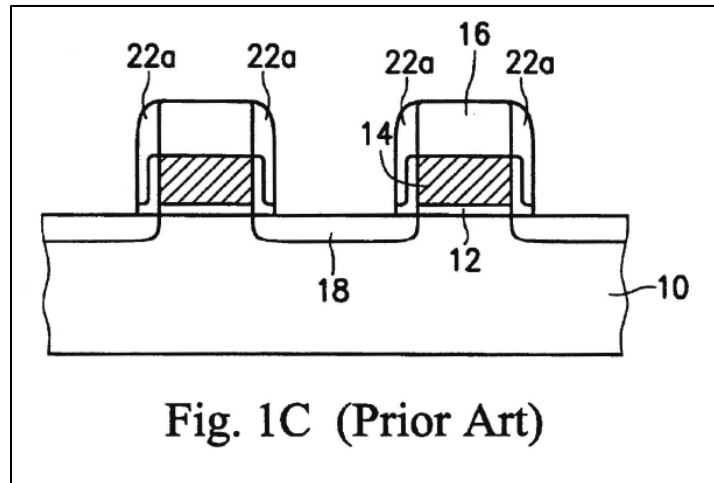
III. OVERVIEW OF THE '997 PATENT

The '997 patent discloses a method for forming a self-aligned contact hole that simplifies the manufacturing process. Specifically, the '997 patent teaches the use of a single conformal layer of nitride material as both the etch stop layer and as the material to form the sidewall spacers. '997 patent at Col. 2:6-14. The conformal layer is not etched until contact hole formation where it functions as an etch barrier to protect the diffusion regions. *Id.* Etching through this layer to expose the diffusion regions will then simultaneously form spacers on the sidewalls of the gate electrode. *Id.* By combining spacer formation with the contact hole etch, the '997 invention reduces the number of process steps and simplifies manufacturing. *Id.*

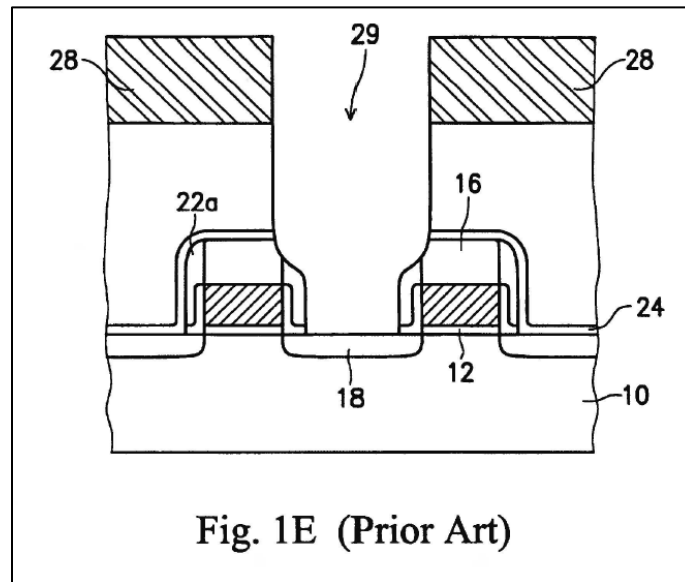
The '997 patent explains that “self-alignment is a technique in which multiple levels of regions on the wafer are formed using a single mask, thereby eliminating the alignment tolerance required by additional masks.” '997 patent at Col. 1:11-20. The '997 patent describes a conventional method of forming a self-aligned contact hole. The process begins with the formation of the gate electrode structure. '997 patent at Col. 1:26-31. A conformal layer of silicon nitride is then

deposited over the substrate surface and anisotropically etched to form nitride spacers 22a on the sidewalls of the gate electrodes. '997 patent at Col. 1:32-40;

Fig. 1C.



After sidewall spacers are formed, a conformal layer of etch barrier material (typically silicon nitride) is deposited over the structure. Next an insulating layer is deposited as the interlayer dielectric (ILD) and planarized. '997 patent at Col. 1:42-50. Using a photoresist mask 28, a contact hole is etched in the insulating layer using the nitride barrier layer as an etch stop so that contact hole 29 is self-aligning. '997 patent at Col. 1:51-57. Finally, the nitride barrier layer 24 is removed to expose the diffusion region.



'997 patent at Fig. 1E.

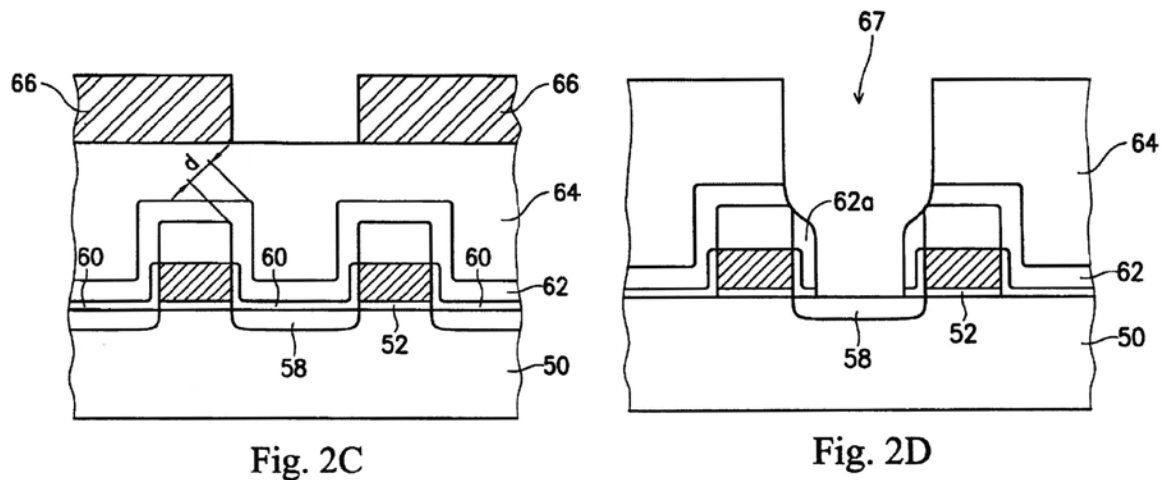
As the '997 patent explains, the conventional process is complicated because it requires two separate depositions of silicon nitride, one to form the spacers and one to form the etch barrier layer. '997 patent at Col. 1:58-67. The two layers also must be etched during different steps, further complicating the process. *Id.*

The invention of the '997 patent simplifies the process by combining the spacer formation step with the contact hole etch step. '997 patent at Col. 2:5-14. Much like the conventional method, the '997 patent's process begins with the formation of the gate electrode. This is followed by the deposition of a conformal layer of silicon nitride of sufficient thickness such that it "acts as sidewall spacers of gate electrode 54 as well as an etch stop at contact hole etching." '997 patent at Col. 2:60-67. A layer of insulating material is then deposited and planarized to form the ILD. '997 patent at Col. 3:1-5. Notably, "the process steps of

anisotropically etching for sidewall spacers and depositing a barrier layer

necessary in the conventional method are omitted here.” ’997 patent at Col. 3:5-9.

Using a photoresist mask 66, contact holes 67 are etched in the insulating layer 64 in a self-aligned manner, using the conformal nitride layer 62 as an etch barrier. ’997 patent at Col. 3:10-17. The conformal nitride layer 62 is then anisotropically etched to expose the diffusion region 58, simultaneously forming nitride spacers 62a on the sidewalls of the gate electrode. ’997 patent at Col. 3:17-21.



’997 patent, Figs. 2C and 2D. Because the conformal layer is not etched until the contact opening is formed, it also provides extra thickness to protect the gate electrode. See ’997 patent at Col. 3:32-35.

The simplified method of the invention overall reduces one etch step and one deposition step as compared to the conventional method illustrated in

Figs. 1A through 1E. Accordingly, the manufacturing cost is reduced and the throughput increased.

'997 patent at Col. 3:40-44. Thus, the key point of novelty for the '997 invention is the fact that it simplifies the manufacturing process and improves process efficiency. Representative claim 1 is shown below.

1. A method for forming a self-aligned contact hole, comprising the steps of:
 - (a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon;
 - (b) forming a conformal layer of etch barrier material overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode;
 - (c) forming an insulating layer overlying the barrier layer;
 - (d) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop; and
 - (e) anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etch barrier material on the sidewall of the gate electrode.

'997 patent at claim 1.

IV. HOME SEMICONDUCTOR'S PROPOSED CLAIM CONSTRUCTIONS

“A claim in an unexpired patent shall be given its broadest reasonable construction in light of the specification of the patent in which it appears.” 37

C.F.R. § 42.100(b); *see also In re Cuozzo Speed Techs., LLC*, 793 F.3d 1268 (Fed. Cir. 2015).

As set forth below, for the purposes of this proceeding only, Home Semiconductor submits constructions for the following terms.

A. “spacer” (claims 1 and 9)

The term “spacer” appears in claims 1 and 9 in the language “simultaneously forming a spacer of the etch barrier material on the sidewall of the gate electrode.”

A person of ordinary skill in the art would understand that the term “spacer,” as it is used in the field of semiconductor fabrication, to mean a structure designed to create physical separation between conducting structures. Maltiel Decl. at ¶ 40. In the time frame of the '997 invention, spacers were typically formed to create space between the gate electrode and other conductive structures. *Id.*

For example, spacers are commonly formed to create space between the gate electrode and doped regions in the substrate formed through ion implantation. Maltiel Decl. at ¶ 41. During implantation, the spacer shields portions of the substrate in the area near the gate electrode, creating separation between the gate and implanted region. *Id.* The extra separation helps reduce the problem of short channel effects. *Id.*

Spacers formed on the sidewalls of the gate electrode also help separate the conductive plug from the gate electrode, which can help prevent shorting effects. Maltiel Decl. at ¶ 42. This is the spacer function specifically mentioned in the '997 patent's specification. '997 patent at Col. 3:35-38 (“Further, the same nitride layer

is anisotropically etched to form sidewall spacers that prevent shorting between the gate electrode and the conductive plug.”).

Thus, the broadest reasonable interpretation of the term “spacer” in light of the specification in which it appears should be a structure designed to create physical separation between conducting structures.

Samsung’s proposed construction of “spacer” is “a structure that spaces between two conductive structures.” To the extent that Samsung’s construction includes any material that spaces, even if unintentionally formed and without a defined function, such a construction would be unreasonably broad. A spacer is a structure that is purposefully designed into the fabrication process to achieve specific functions. Maltiel Decl. at ¶ 40. It is not just any material, no matter what size or shape, that spaces.

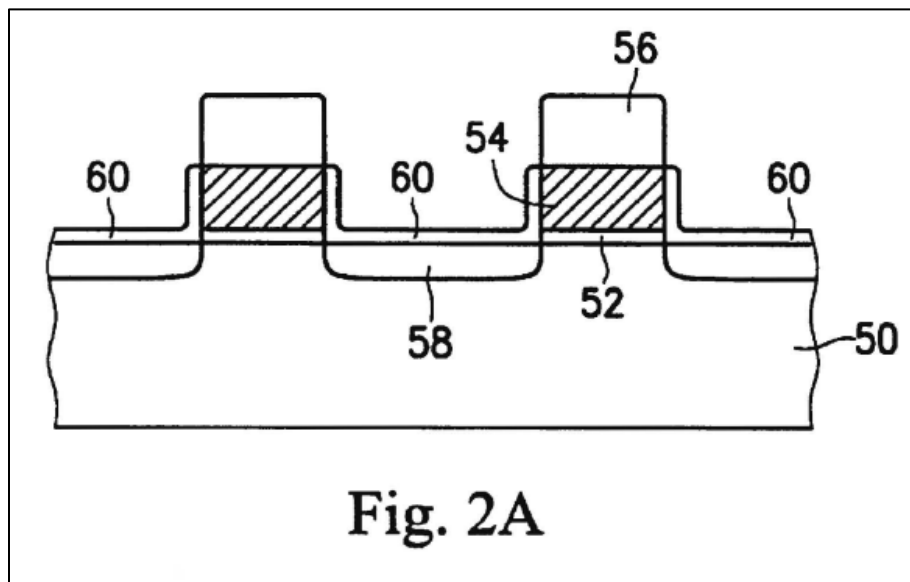
B. “forming an oxide layer over the diffusion region”

The phrase “forming an oxide layer over the diffusion region” appears in dependent claims 2 and 9. The word “over” has a number of definitions but in the context of the ’997 patent, the word is used to mean covering. *See, e.g.*, SAM-1007, Webster’s Third New International Dictionary (1986) at p. 4-5 (“so as to cover, conceal, or affect the whole surface or expanse”).

The ’997 patent uses the “over” exclusively to refer to a structure that is covering another structure. *See* ’997 patent at Fig. 1A, Col. 1:29-31 (“Next, a thin

oxide layer 20 is formed over the substrate surface[.]”); Fig. 1B, Col. 1:32-34 (“Referring to FIG. 1B, a conformal layer of silicon nitride 22 having a thickness of about 100 to 600 Å is deposited over the substrate surface[.]”); Fig. 1D, Col. 1:41-46 (“Referring to FIG. 1D, a conformal layer of etch barrier material 24 is deposited over the diffusion region 18, the cap layers 16, and the sidewall spacers 22a. . . . A layer of insulator 26 is deposited over the substrate as inter-layer dielectric (ILD)[.]”); Fig. 2A, Col. 2:55-57 (“[A] thin oxide layer 60 having a thickness of about 150 Å is formed over the substrate surface[.]”); Fig. 2B, 2:60-62 (“Referring to FIG. 2B, a conformal layer of silicon nitride 62 is deposited over the substrate surface using low pressure chemical vapor deposition (LPCVD)”); Fig. 2C, 3:1-2 (“Referring to FIG. 2C, a layer of insulator 64 is deposited over the substrate as inter-layer dielectric (ILD)”); Fig. 2D, 3:17-20 (“[T]he conformal nitride layer 62 underneath the opening is anisotropically etched to remove the portion over the diffusion region 58.”); Maltiel Decl. at ¶ 36.

Specifically, in the context of the claim limitation that requires “forming an oxide layer over the diffusion region,” that ’997 patent figure show that oxide layer 60 is covering the diffusion region 58. *Id.*



'997 patent at Fig. 2A; 2:55-57 (“[A] thin oxide layer 60 having a thickness of about 150 Å is formed over the substrate surface[.]”).

Thus, the broadest reasonable interpretation of the term “forming an oxide layer over the diffusion region” in light of the specification in which it appears should be forming an oxide layer covering the diffusion region.¹

Samsung proposes a construction of “forming an oxide layer over the diffusion region” to mean “forming an oxide layer above the diffusion region.” Samsung has substituted the word “over” with the word “above.” Pet. at p. 9. By doing so, Samsung appears to have broadened the construction such that the oxide layer only needs to be in a higher position than the diffusion region, but does not

¹ Covering, in this context, does not mean that there cannot be structures in between. For example, the conformal layer of silicon nitride and the ILD layer both cover the substrate even though the gate electrode is in between the layers and the substrate in some locations. See '997 patent at Figs. 2B and 2C.

need to be covering the diffusion region.² This construction is neither reasonable nor supported by the '997 patent specification. As stated above, the '997 patent never uses the word “over” to only mean a higher position than a structure without also covering that structure. There is no reason to rewrite the claim with new language, substituting “over” with “above,” simply to apply a broader construction, especially when the construction is not consistent with the teachings of the patent specification. Samsung’s proposed construction should be rejected.

C. Samsung’s Other Proposed Constructions

For the purposes of this proceeding only, Home Semiconductor does not dispute that Samsung’s propose claim constructions for the terms “‘forming a conformal layer of [etch barrier material/silicon nitride] overlying the substrate” and “etching an opening through the insulating layer self-aligned and borderless to the diffusion region” satisfy the broadest reasonable construction standard applicable to the proceedings for the Board, and will apply those constructions, where necessary, in this response. Home Semiconductor disputes whether these

² Samsung’s petition does not explicitly state that the intent is to broaden the construction such that the oxide layer only need to be higher, but not in the same vertical space, as the diffusion region. This understanding was only confirmed during the deposition of Samsung’s expert, Dr. Rubloff, where he stated that his construction would not require that the two objects be in the same vertical space. Rubloff Tr. 152:17-153:3.

constructions would necessarily be proper in a district court applying the claim construction tenets of *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005).

V. DOSHI DOES NOT ANTICIPATE THE CHALLENGED CLAIMS

The Board has initiated this proceeding to consider whether Doshi anticipates the Challenged Claims. Paper 11 at 20. For a prior art reference to serve as an anticipatory reference, it must disclose every limitation of the claimed invention, either explicitly or inherently. *In re Schreiber*, 128 F.3d 1473, 1477 (Fed. Cir. 1997). *See also Scripps Clinic & Res. Found. v. Genentech, Inc.*, 927 F.2d 1565, 1576 (Fed. Cir. 1991) (for anticipation, “[t]here must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention”), *overruled on other grounds by Abbott Labs. v. Sandoz, Inc.*, 566 F.3d 1282 (Fed. Cir. 2009). For the reasons set forth below, Doshi does not anticipate the Challenged Claims, and thus, all of the claims should be confirmed as patentable over Doshi.

A. Doshi Does Not Anticipate Claims 1, 2, and 9 Of The ’997 Patent

The Doshi reference does not anticipate claims 1, 2, and 9 of the ’997 patent. Doshi teaches a process that is the same as the admitted prior art described in the ’997 patent’s Background of the Invention section. Maltiel Decl. at ¶ 59. Like the conventional method described in the ’997 patent, Doshi describes a method where the spacer is formed in a separate step from the formation of the contact hole. *Id.*

Although Doshi does form self-aligned contacts through a two step etch process, that process is used exclusively to form contact holes. *Id.* Doshi does not combine spacer formation with the contact hole etch. *Id.* Thus, unlike the '997 invention, the Doshi reference does not reduce the number of process steps and does not simplify the manufacturing process. *Id.*

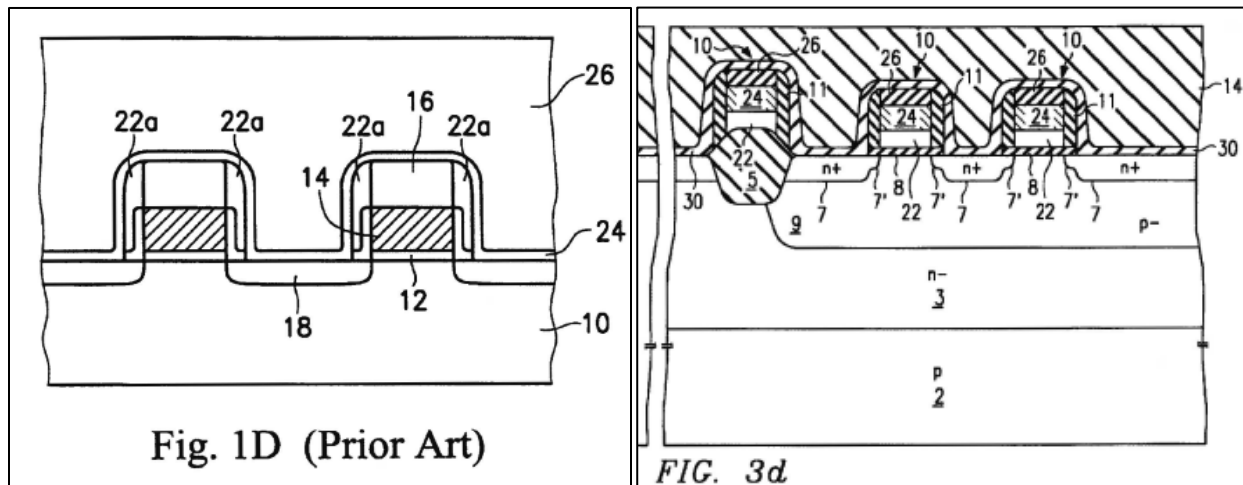
As shown below, Doshi does not teach each and every limitation of independent claims 1 and 9 of the '997 patent, and thus none of the Challenged Claims are anticipated because if the independent claims are not anticipated, the dependent claims cannot be anticipated. *See Wahpeton Canvas Co. v. Frontier, Inc.*, 870 F.2d 1546, 1552 (Fed. Cir. 1989) (Holding that “[o]ne who does not infringe an independent patent claim cannot infringe a claim dependent on (and thus containing all the limitations of) that claim.”) (*quoting Teledyne McCormick Selph v. United States*, 558 F.2d 1000, 1004, 214 Ct. Cl. 672 (1977)) Moreover, dependent claim 2 contains additional limitations that are not found in Doshi.

1. Summary of Doshi

Doshi describes a method for fabricating an integrated circuit using a silicon nitride layer as a diffusion barrier to prevent the diffusion of boron and phosphorus dopant from the BPSG layer into the substrate. Doshi at Abstract. Doshi also describes contact openings that are etched through the BPSG layer and then through the silicon nitride layer using a two-step etch process. *Id.*

The Doshi method begins by forming gate structures on the substrate, followed by the formation of light reach through implants. Doshi at Col. 7:29-57. Doshi then forms sidewall filaments 11 of the sidewalls of the gate electrode. Doshi at Col. 7:57-62. These sidewall filaments 11 are spacers of the Doshi device structure and are subsequently used during source/drain implantation to create space between the source/drain regions and the gate electrode. Doshi at Col. 7:66-8:5; Maltiel Decl. at ¶ 53, 63; Rubloff Tr. at 161:7-162:8. After implantation, a silicon nitride layer 30 is formed over the gate structure and the sidewall filaments. Doshi at Col. 8:8-14. The BPSG layer is then deposited, annealed, and etched back to leave substantially planar upper surface. Doshi at Col. 8:23-36; 8:66-9:12. Doshi teaches that the nitride layer blocks boron and phosphorus from diffusing into the source/drain regions during the BPSG reflow and annealing process. Doshi at Col. 8:37-65. Doshi refers to the nitride layer 30 as a barrier layer and as an etch stop. Doshi at Col. 8:56-57 (In addition, the prevention of diffusion by nitride layer 30 also ensures that BPSG layer 14 itself is of high integrity.”); 9:48-50 (“... as such the etch will tend to stop on nitride layer 30.”). Doshi never refers to the nitride layer 30 as a spacer or as material that will form a spacer.

When compared to the conventional process (admitted prior art) described in background of the '997 patent, the Doshi method appears strikingly similar. The figures below show both processes after formation of the interlayer insulator.



'997 patent at Fig. 1D; Doshi at Fig. 3d. As shown above, the two processes are effectively the same in relevant parts. Both show the thin etch stop layer (layer 24 in the '997 patent; layer 30 in Doshi) formed over the existing spacers (structure 22a in the '997 patent; structure 11 in Doshi) on the side walls of the gate electrode.

Much like the conventional process of the '997 patent, the next step in Doshi is the formation of self-aligned contact openings through a two-step etch process. Doshi at Col. 9:34-10:3 (for plug contacts); 10:39-11:9 (for bit line contacts). The first step is a dry etch of the BPSG layer which tends to stop on the nitride layer. Doshi at Col. 9:37-55; 10:43-61. The second step etches the nitride layer 30 and completes the contact openings. Doshi at Col. 9:56-10:16; 10:62-11:9. According

to Doshi, the nitride layer is removed from within the contact locations. Doshi at Col. 10:11-12 (“brief nitride etch used to clear nitride layer 30 from within plug contact locations PC”); 10:62-63 (“The second step of the two-step etch is then performed to remove nitride layer 30 from bit line contact location BLC.”). Doshi does not teach that nitride layer 30 is left on the sidewalls of the gate electrode to form spacers. Maltiel Decl. at ¶ 57.

2. Doshi Does Not Anticipate Independent Claims 1 and 9 Because It Does Not Describe Simultaneously Etching and Forming A Spacer on the Sidewall of the Gate Electrode

Doshi does not anticipate independent claims 1 and 9 of the '997 patent because Doshi does not disclose the following claim limitation:

anisotropically etching the barrier [silicon nitride] layer underneath the opening, thereby exposing the diffusion region *and simultaneously forming a spacer of the etch barrier material [silicon nitride] on the sidewall of the gate electrode.*

'997 patent at Col. 4:1-4.

This limitation requires the formation of spacers on the sidewalls of the gate electrode at the same time as the anisotropic etch step. Maltiel Decl. at ¶ 60.

Doshi does not form of spacers on the sidewalls of the gate structure during the

anisotropic etch during contact hole formation, and thus does not disclose this claim limitation.³ *Id.*

Samsung points to the nitride layer 30 as the material that forms the claimed spacer.⁴ Pet. at p. 26. However, Doshi's specification teaches that nitride layer 30 is removed from the contact hole locations during the nitride etch step.

[T]he brief nitride etch used to *clear nitride layer 30 from within plug contact locations PC* has been observed to be highly anisotropic[.]

Doshi at Col. 10:11-13 (emphasis added).

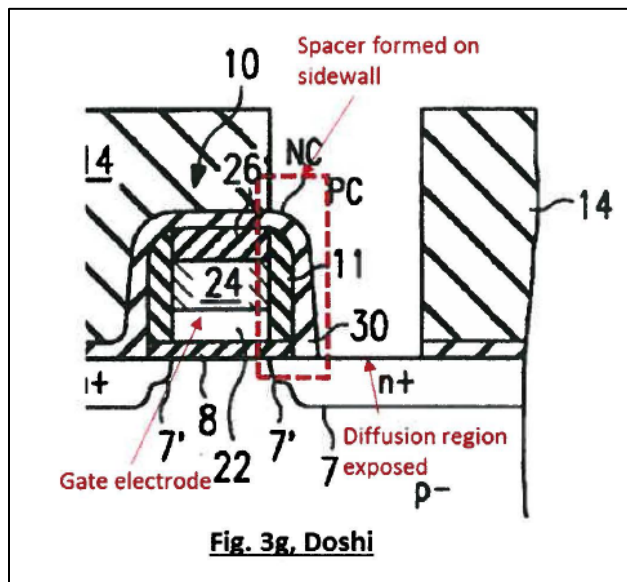
The second step of the two-step etch is then performed *to remove nitride layer 30 from bit line contact location BLC.*

Doshi at Col. 10:62-63 (emphasis added); Maltiel Decl. at ¶ 63. The objective of the nitride etch is to clear the nitride layer from within the contact locations and expose the source/drain regions in the substrate. Maltiel Decl. at ¶ 64. Doshi's specification does not disclose a process where a portion of nitride layer 30 remains following the etch process, much less a process where this material is used to form a spacer on the sidewall of the gate electrode. *Id.*; Doshi at Col. 8:8-54.

³ This is true under both proposed constructions of the term "spacer." Maltiel Decl. at ¶ 61.

⁴ Doshi describes the function of nitride layer 30 as a dopant diffusion barrier during BPSG reflow and an etch stop during contact hole formation. Doshi at Col. 8:11-14; Maltiel Decl. at ¶ 54. Doshi never states that the nitride layer 30 is deposited to form spacers. Maltiel Decl. at ¶ 57.

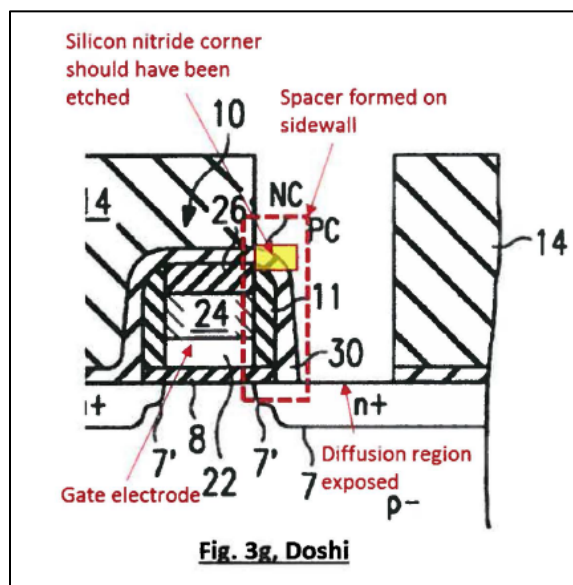
In the absence of any specification support, Samsung cites only Doshi Fig. 3g, which purports to show the results of the nitride etch at PC locations. Samsung argues that this figure shows that nitride material remains on the sidewalls of the gate electrode after the nitride etch step.



Pet. at p. 27. Samsung identifies this allegedly remaining portion of the nitride layer 30, and calls it a spacer formed of etch barrier material that is formed simultaneously with the etch.

Samsung's reliance on Fig. 3g should be rejected because Figure 3g is riddled with errors. Samsung's own expert Dr. Rubloff pointed out in his declaration that Figure 3g erred in its depiction of the etch results. Rubloff Decl. at A-14. According to Dr. Rubloff, the Fig. 3g fails to show the removal of nitride material at the top of the gate. Rubloff Decl. at A-14. This material should have been etched since it was also exposed within the contact opening.

I noticed that the corner of the silicon nitride layer 30, which is exposed to the silicon nitride dry etch, is not shown as etched in Fig. 3g. I believe this is a mistake in Fig. 3g, as an anisotropic etch of silicon nitride would have removed the same thickness of the silicon nitride covering the diffusion region and the silicon nitride at the corner.

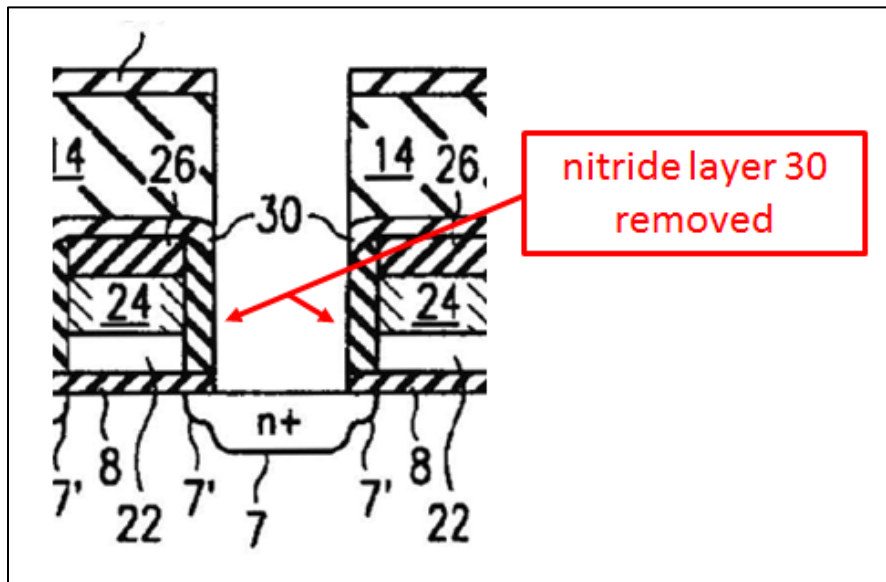


Rubloff Decl. at A-14; Rubloff Tr. at 203:11-204:15 (confirming error in figure).

Figure 3g's errors are not confined to just the top corner. Maltiel Decl. at ¶ 67. The nitride etch process designed to clear the nitride layer 30 would etch every part of layer 30 exposed under the contact opening. *Id.* Oddly, Fig. 3g shows the portion of nitride layer 30 covering the gate as completely unaffected by this etch process. *Id.* This is an undeniable error, and is consistent with Dr. Rubloff's identification of other errors. *Id.*; Rubloff Decl. at A-14; Rubloff Tr. at 203:11-204:15. Samsung cites no other evidence in its petition to establish the presence of the spacers formed simultaneously with the etch process. Dr. Rubloff's conclusion

to the contrary is simply not credible – he drew his conclusion that nitride material remains on the sidewall based on Fig. 3g, even while noting the clear error in the drawing. Rubloff Decl. at A-13 (citing Fig. 3g as showing material left on the sidewall after the nitride etch of nitride layer 30); A-14 (noting that Fig. 3g does not accurately depict the effect of the nitride etch on the nitride layer 30).

This error in Figure 3g is confirmed through a comparison to another figure that Doshi describes as showing the result of nitride etching in BLC locations. Maltiel Decl. at ¶ 68. Doshi describes forming BLC contact opening using essentially the same etch process as that used for the PC contact openings. Doshi at 10:40-11:21; Maltiel Decl. at ¶ 68. In these processes, the nitride etch parameters are identical. Doshi at 10:65-66 (showing both nitride etches with the same process parameters and stating that “[t]he second step is substantially identical to that performed in the two-step etch of plug contact locations PC.”). Because the etches are the same, they should have the same impact on nitride layer 30. Maltiel Decl. at ¶ 68. Figure 3k shows the result of the BLC etch, and establishes that the entire exposed portion of nitride layer 30 removed from the BLC contact location.



Doshi at Fig. 3k (annotation added). This result is both expected and consistent with how Doshi describes the nitride etch process. Maltiel Decl. at ¶ 69; Doshi at Col. 10:62-63 (“The second step of the two-step etch is then performed to remove nitride layer 30 from bit line contact location BLC.”). Moreover, unlike Doshi Fig. 3g’s depiction of the etch process of PC locations, there is no indication that Fig. 3k’s depiction of the etch process in the BLC location is erroneous or unreliable.⁵ Maltiel Decl. at ¶ 69; Rubloff Tr. at 209:8-210:10. Indeed, Dr. Rubloff either chose to ignore or simply did not consider that Fig. 3k showed the entire nitride

⁵ It is worth noting that Samsung’s expert Dr. Rubloff drew his conclusion that nitride material remains on the sidewall based on Fig. 3g, even while noting the clear error in the drawing. Rubloff Dec. at A-13 (citing Fig. 3g as showing material left on the sidewall after the nitride etch of nitride layer 30); A-14 (noting that Fig. 3g does not accurately depict the effect of the nitride etch on the nitride layer 30). He either chose to ignore or simply did not consider that Fig. 3k showed the entire nitride layer removed in the BLC location using the same nitride etch of the same nitride layer 30 within the same type of contact opening. Rubloff Tr. at 210:17-212:12.

layer removed in the BLC location using the same nitride etch of the same nitride layer 30 within the same type of contact opening. Rubloff Tr. at 210:17-212:12.

Further, from a technical perspective, it makes sense that Doshi would not leave nitride layer 30 on the sidewall as a spacer. Doshi simply doesn't need it. In the Doshi process, the sidewall filaments 11 are the spacers. Maltiel Decl. at ¶¶ 62, 46; Rubloff Tr. at 161:3-162:8. They are formed and perform their spacer function long before the nitride layer 30 (the etch barrier) is deposited. *Id.* With spacers already in place, Doshi would not then further complicate its process by teaching the formation of additional spacers from nitride layer 30. *Id.* This is why Doshi never mentions leaving nitride layer 30 on the sidewalls or that the material is there to form spacers. *Id.*

Thus, a person of ordinary skill in the art, reading Doshi, would understand that nitride layer 30 would be removed from within the contact opening locations (both PC and BLC locations) during the etch, and that no spacers would be formed simultaneously with the etch. Maltiel Decl. at ¶¶ 70-71. Accordingly, this limitation is not taught by Doshi, and Samsung has not established that the asserted claims are anticipated.

Even if we ignore the teaching of Doshi and accept Samsung's argument that nitride layer 30 is left on the sidewalls of the gate electrode is a spacer, it would not satisfy the "simultaneously forming" requirement of claims 1 and 9.

This element requires that the spacer formation occur at the same time as the anisotropic etch process used to form contact hole. However, according to Samsung's expert, Dr. Rubloff, nitride layer 30 on the sidewalls of the gate electrode is already a "spacer" during the BPSG reflow stage -- long before the contact hole etch process even begins.

Q. Right. So looking at figure 3d, a person of ordinary skill in the art would look at a portion of nitride layer 30 covering the sidewalls of the gate electrode and say that's a spacer right there?

A. Well, I would say it's a diffusion barrier during BPSG reflow, which is an annealing step.

Q. So it is not a spacer?

A. Well, a diffusion barrier is a kind of spacer.

Q. Okay. So it is a spacer?

A. Yes.

Rubloff Tr. at 196:2-14.

Q. Because you are saying that during BPSG formation, that portion of the nitride layer that's on the sidewall is acting as a diffusion barrier in the -

A. Lateral.

Q. -- lateral direction?

A. Yes.

Q. Thank you. And I think your point was, is that at that stage, that portion of the nitride layer, the portion that's on the sidewall of the gate, is functioning as a spacer; correct?

A. A diffusion barrier spacer.

Q. And that diffusion barrier spacer is within the definition of spacer that you provided in the context of the '997?

A. Yes.

Rubloff Tr. at 197:11-198:5. Thus, according to Dr. Rubloff, the “spacer” already exists during *before* the contact etch process. If it exists before, then it cannot also be “simultaneously” formed during that etch process. Thus, Samsung’s misreading of the Doshi reference as applied by its own expert, still would not result in anticipation.

3. Doshi Does Not Anticipate Claim 2 or Claim 9

Doshi does not anticipate claim 2 or claim 9 both require an additional step not described in Doshi:

[A] step of forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode by thermal oxidation.

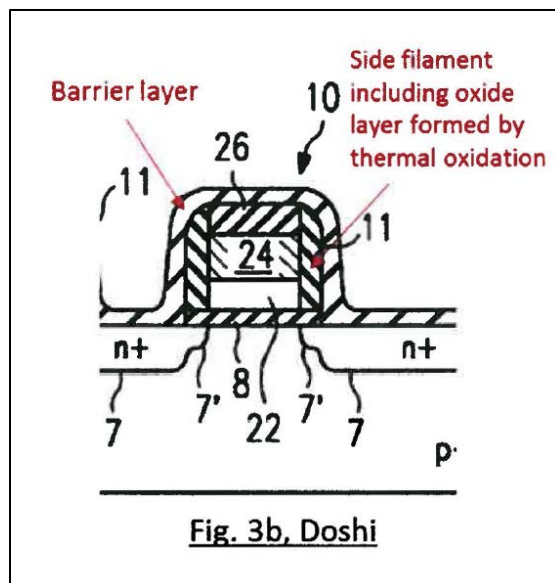
'997 patent at Col. 4:5-8; 4:32-34. Claim 2 depends from claim 1. Claim 9 is an independent claim.

This claim limitation specifically requires the formation of an oxide on the sidewalls of the gate electrode *and over the diffusion region*. Doshi does not teach forming an oxide layer over the diffusion regions. Doshi only states that the sides of the polysilicon layer are oxidized. Doshi at Col. 7:57-59 (“According to the preferred embodiment of the invention, sidewall filaments 11 are formed by

first oxidizing the sides of polysilicon layer 22.”). Doshi does not mention forming an oxide over diffusion regions and never depicts such an oxide layer in any of its figures. Maltiel Decl. at ¶ 78.

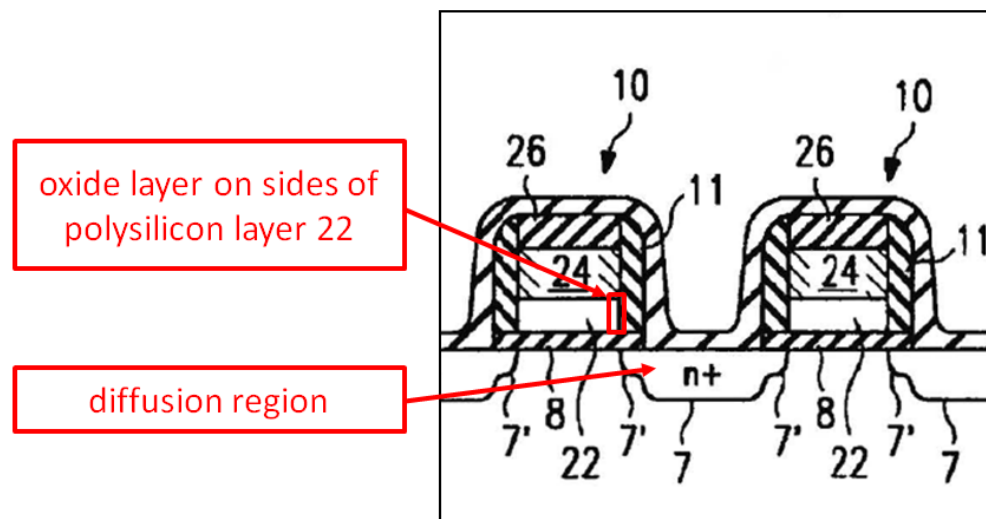
Samsung makes two arguments to support its contention that Doshi describes Doshi forming a oxide layer over the diffusion region. Pet. at p. 28-29. Neither of these arguments are persuasive.

First, Samsung argues that the oxide on the sidewalls of the gate electrode are still “over” the diffusion regions. Pet. at p. 28 ([T]he side filament 11 is formed above the source/drain region 7', and illustrates that the oxide layer is formed over the diffusion region.”).

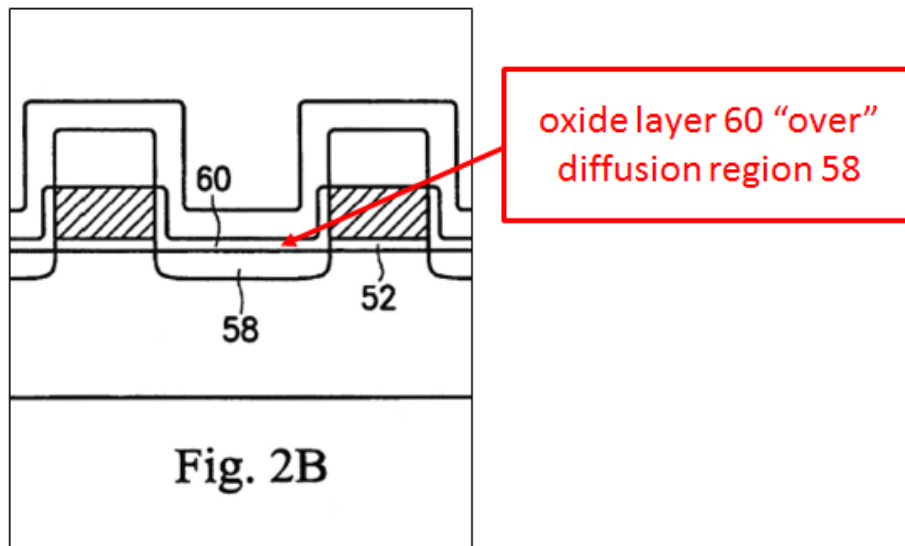


Samsung’s argument is based on its incorrect construction of the term “over” to require only that the oxide layer is higher than the diffusion region, without covering the diffusion region. As discussed in Section IV.B, Samsung’s

construction is wrong. The word “over” as it is used in the claim limitation and in the specification should be understood to mean covering. Thus, any oxide layer that satisfies the claim limitation must be formed such that it covers the diffusion region. An oxide layer formed on the sidewalls of the gate electrode, at the interface between the polysilicon layer 22 and the sidewall filament 11, would not cover the diffusion region. Maltiel Decl. at ¶ 79.



Doshi at 3b (annotations added to show what Samsung claims is an oxide layer “over” the diffusion regions). The figure below shows what the '997 patent requires.



'997 patent at Fig. 2B. As illustrated above, when the '997 patent claims an oxide layer formed over the diffusion region, it is claiming a layer that is actually covering that region, not just higher but off to the side.

Samsung's second argument is that Doshi's process for oxidizing the gate electrode sidewall would necessarily form an oxide layer over the diffusion region because that region is "uncovered doped silicon, which is susceptible to thermal oxidation." Pet. at p. 29. Samsung is wrong. In Doshi, the diffusion region is not uncovered doped silicon during the oxidation step. Maltiel Decl. at ¶ 81. That area, the source/drain regions, is actually covered by the gate oxide layer 8 which is not removed until *after* the oxidation process. *Id.*

Doshi describes etching the nitride layer 26, the tungsten silicide layer 24, and the polysilicon layer 22. Doshi at Col. 7:44-51. At this point, Doshi does not etch the gate oxide layer 8, which would still cover the entire substrate. Next,

reach through implants are performed to define the source/drain extension regions. These reach through implants are implants that pass through the gate oxide layer 8 and forms source/drain extension regions. Doshi at Col. 7:52-65. Next, the sidewalls of the polysilicon layer 22 are oxidized and the nitride sidewall filaments are formed. Finally, the source/drain implants are performed to define the source drain regions. It is only then, that Doshi removes gate oxide layer 8 from over the source/drain regions. Doshi at Col. 8:3-7 (“Following the formation of the source/drain regions 6, 7, gate oxide layer 8 is removed overall, except from under the gate structures 10.”). Thus, during the oxidation of the polysilicon gate sidewalls, the diffusion regions are covered by the gate oxide layer and not “uncovered doped silicon” as Samsung claims. Maltiel Decl. at ¶ 82.

For these reasons, Samsung has not established that Doshi discloses all limitations in claims 2 and 9, and thus these claims are not anticipated by Doshi.

VI. CONCLUSION

For the reasons set forth above, Doshi does not disclose or suggest the claimed invention, and the Challenged Claims would not have been anticipated in view of the identified art. The Challenged Claims should be confirmed as patentable over the art relied upon in this proceeding.

Case No. IPR2015-00460

Patent No. 6,146,997

Dated: August 31, 2015

Respectfully submitted,

By: /s/ Craig R. Kaufman
Registration No. 34,636
Lead Counsel for Patent Owner
TechKnowledge Law Group LLP
100 Marine Parkway, Suite 200
Redwood Shores, CA 94065
650-517-5200

APPENDIX OF EXHIBITS

Exhibit No.	Description
2002	Declaration of Ron Maltiel in Support of Patent Owner Response to Petition
2003	Ron Maltiel Curriculum Vitae
2004	Deposition Transcript of Gary W. Rubloff, Ph.D. Volume 1, August 18, 2015
2005	Deposition Transcript of Gary W. Rubloff, Ph.D. Volume 2, August 19, 2015

CERTIFICATE OF SERVICE

I hereby certify that on August 31, 2015, a true and correct copy of the foregoing PATENT OWNER HOME SEMICONDUCTOR CORPORATION'S RESPONSE TO PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT NO. 6,146,997 and all supporting exhibits were served electronically via email to the Petitioner by serving the correspondence email addresses of record as follows:

W. Karl Renner (Reg. No. 41,265)
FISH & RICHARDSON P.C.
3200 RBC Plaza
60 South Sixth Street
Minneapolis, MN 55402
Telephone: (202) 783-5070
Facsimile: (202) 783-2331
E-mail: renner@fr.com

Roberto Devoto (Reg. No. 55,108)
Indranil Mukerji (Reg. No. 46,944)
David L. Holt (Reg. No. 65,161)
FISH & RICHARDSON P.C.
3200 RBC Plaza
60 South Sixth Street
Minneapolis, MN 55402
Telephone: (202) 783-5070
Facsimile: (202) 783-2331
E-mail: IPR39843-0011IP1@fr.com
E-mail: devoto@fr.com
E-mail: mukerji@fr.com
E-mail: dth@fr.com

By: /s/ Deborah L. Grover
Deborah L. Grover
TechKnowledge Law Group LLP
100 Marine Parkway, Suite 200
Redwood Shores, CA 94065
650-517-5200