

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO. LTD.,
SAMSUNG ELECTRONICS AMERICA, INC.,
SAMSUNG SEMICONDUCTOR INC., and
SAMSUNG AUSTIN SEMICONDUCTOR LLC,
Petitioner,

v.

HOME SEMICONDUCTOR CORPORATION,
Patent Owner

Case IPR2015-00460
Patent 6,146,997

**DECLARATION OF RON MALTIEL IN SUPPORT OF PATENT OWNER
HOME SEMICONDUCTOR CORPORATION RESPONSE TO
PETITION FOR *INTER PARTES* REVIEW OF
UNITED STATES PATENT NO. 6,146,997**

I, Ron Maltiel, hereby declare as follows

I. INTRODUCTION

1. I have been retained as an expert on behalf of Home Semiconductor Corporation (Home Semiconductor”) for the above-captioned Petition for *Inter Partes* Review (“Pet.”) of U.S. Patent No. 6,146,997 (the “’997 patent”).

2. I am being compensated for my time in connection with this IPR at my standard consulting rate of \$500 per hour. My compensation is not dependent on the outcome of this proceeding, the results of my analysis, or on the substance of my opinions and testimony.

3. I have been asked to provide my opinion on the validity of the ’997 patent. In particular, I have been asked to consider whether claims 1-14 of the ’997 patent are patentable over certain published prior art references as identified in this declaration.

4. In preparing this Declaration, I have reviewed the ’997 patent, the file history of the ’997 patent, and the numerous prior references and technical references from the time of the invention. I have also reviewed the petition for *inter partes* review from Petitioners Samsung Electronics Co. Ltd., Samsung Electronics America, Inc., Samsung Semiconductor Inc., and Samsung Austin Semiconductor LLC (collectively “Petitioner” or “Samsung”), including the

material contained therein. I have also attended and reviewed the transcript of the deposition of Gary W. Rubloff, Ph.D in connection to this IPR.

5. I have been advised, and it is my understanding, that patent claims in the IPR are given their broadest reasonable interpretation in view of the patent specification, file history, and the understanding of one having ordinary skill in the relevant art at the time of the invention.

6. In forming the opinions expressed in this Declaration, I relied upon my education and experience in the relevant field of the art, and have considered the viewpoint of a person having ordinary skill in the relevant art at the time of the invention.

II. BACKGROUND AND QUALIFICATIONS

7. As indicated in my curriculum vitae (Exh. 2003), I have over 30 years' experience working in the field of semiconductor process and memory devices. My 30 years of experience includes working for four semiconductor companies: Intel, American Microsystems, Inc. (AMI), Advanced Micro Devices (AMD), and Maxim Integrated Products. Over these years, my work has focused on the development and optimization of semiconductor devices including the integration and technological developments made in the area of process, circuit, and design engineering into one final work product. Often I developed new process technologies, such as metal layers depositions and etches, integrating the

various steps into one working product. Prior to this, between 1978 and 1980, I was involved in the research of metallic impurities and their electrical behaviors at Stanford University.

8. As further described in my curriculum vitae, I have a Bachelor's of Science degree in Material Sciences and Engineering from Ben Gurion University in Israel. After that, I went on to Stanford University in Palo Alto, CA, where I earned a Master's Degree in Material Science. After earning the Master's Degree, I was awarded an Engineering Degree from Stanford University. An Engineering Degree is a graduate degree, post a master degree similarly to a Ph.D., but with an emphasis towards professional engineering work rather than towards theoretical research or university teaching. The required thesis for my Engineering Degree was related to semiconductor devices and electrical measurements of their properties.

9. I am currently working as an independent consultant where I provide consulting services in various aspects of semiconductor technology and manufacturing. Additionally, for more than 10 years, I have been managing a semiconductor industry website (www.maltiel-consulting.com) and providing to the semiconductor industry a resource full of pertinent information regarding semiconductor process technology and patents for various types of semiconductor devices. This resource addresses the information needs of technology companies,

attorneys, and investors and is used regularly by major semiconductor companies and universities from more than 99 countries.

10. I am the named inventor in several patents covering the area of semiconductor devices: U.S. Patent No. 4,978,923 titled “Electrical measurements of profile of semiconductor devices during their manufacturing process,” U.S. Patent No. 4,716,552 titled “Method and apparatus for non-destructive data in a shadow memory array,” U.S. Patent No. 4,956,611 titled “Electrical measurements of properties of semiconductor devices during their manufacturing process,” U.S. Patent No. 4,672,580 titled “Memory cell providing simultaneous non-destructive access to volatile and non-volatile data,” U.S. Patent No. 4,611,309 titled “Non-volatile dynamic ram cell,” and U.S. Patent No. 4,432,008 titled “Gold-doped IC resistor region.”

11. Due to my contributions to developments of memory devices and DRAM technology, I was recognized as a senior member of the IEEE in 2008, a recognition given only to IEEE members who have made outstanding technical contributions. IEEE stands for Institute of Electrical and Electronics Engineers, which is the leading professional association for electrical engineers. A senior member is the grade of IEEE members, where an individual is elected only after having significant relevant professional industry experience.

12. My professional and education background, as well as a listing of other matters on which I have provided consulting and/or provided testimony as a technical expert, are detailed in my curriculum vitae, attached to this Declaration.

III. UNDERSTANDING OF PATENT LAW

13. I am not a patent attorney, nor have I independently researched the law of patent validity. Attorneys have explained certain legal principles to me that I have relied on in forming my opinions as set forth in my Declaration.

A. Prior Art

14. I understand that prior art to the '997 patent includes patents and printed publications in the relevant art that predates the May 11, 1999 priority date I have been asked to assume for this patent for the purposes of this Declaration.

B. Anticipation

15. I understand that a claim is invalid if it is anticipated. I understand that anticipation of a claim requires that every element of a claim be disclosed expressly or inherently in a single prior art reference, as claimed. I understand that, to anticipate a patent claim, the prior art reference need not use the same words as the claim, but it must describe the requirements of the claim with sufficient clarity that a person of skill in the art would be able to make and use the claimed invention based on the single prior art reference.

16. In addition, I understand that, in order to establish that an element of a claim is “inherent” in the disclosure of a prior art reference, it must be clear to one skilled in the art that the missing element is an inevitable part of what is explicitly described in the prior art, and that it would be recognized as necessarily present by a person of ordinary skill in the art.

C. Obviousness

17. I understand that obviousness of a claim requires that the claim be obvious from the perspective of a person having ordinary skill in the relevant art at the time the alleged invention was made. I understand that a claim may be obvious from a combination of two or more prior art references.

18. I understand that an obviousness analysis requires an understanding of the scope and content of the prior art, any differences between the alleged invention and the prior art, and the level of ordinary skill in evaluating the pertinent art.

19. I understand that certain factors may support or rebut the obviousness of a claim. I understand that such secondary considerations include, among other things, commercial success of the patented invention, skepticism of those having ordinary skill in the art at the time of invention, unexpected results of the invention, any long-felt but unsolved need in the art that was satisfied by the alleged invention, the failure of others to make the alleged invention, praise of the

alleged invention by those having ordinary skill in the art, and copying of the alleged invention by others in the field. I understand that there must be a nexus—a connection—between any such secondary considerations and the alleged invention. I also understand that contemporaneous and independent invention by others is a secondary consideration tending to show obviousness.

20. I understand that a claim may be obvious if common sense directs one to combine multiple prior art references or add missing features to reproduce the alleged invention recited in the claims. If a person having ordinary skill in the relevant art can implement a predictable variation, obviousness likely bars its patentability. For the same reason, if a technique has been used to improve one device and a person having ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious. I further understand that a claim can be obvious if it unites old elements with no change to their respective functions, or alters prior art by mere substitution of one element for another known in the field and that combination yields predictable results. While it may be helpful to identify a reason for this combination, common sense should guide and no rigid requirement of finding a teaching, suggestion or motivation to combine is required. When a product is available, design incentives and other market forces can prompt variations of it, either in the same field or a different one.

IV. BACKGROUND OF THE '997 PATENT

A. Brief Overview of the '997 Patent

21. The '997 patent discloses a simplified method for forming a self-aligned contact hole. In addition to the conventional steps in fabricating a semiconductor device, the patented method discloses a method to simultaneously anisotropically etch the barrier layer to expose the diffusion layer and form a barrier etch material spacer on the sidewall of the gate electrode. '997 patent at Abstract.

22. The '997 patent explains that self-alignment is a technique in which multiple levels of regions on the wafer are formed using a single mask. This approach eliminates the alignment tolerance required by additional masks and results in significant space saving. '997 patent at Col. 1:11-20.

23. In a conventional process for semiconductor fabrication, the gate electrodes, consisting of polysilicon and silicide, are capped with an insulating layer of silicon nitride. A thin oxide layer is then formed over the substrate and the sidewalls of the gate electrode by rapid thermal oxidation. '997 patent at Col. 1:26-30.

24. Next, conformal layer of silicon nitride having a thickness of 100 to 600 angstroms is deposited over the substrate surface using low pressure chemical vapor deposition (LPCVD). This layer of silicon nitride is then anisotropically

etched to form nitride spacers on the sidewalls of the gate electrodes and the cap layers. Then, after the formation of the spacers, the thin oxide layer on the substrate is removed to expose the diffusion region. '997 patent at Col. 1:32-40.

25. A conformal layer of etch barrier material, typically silicon nitride with a thickness of 100 to 500 angstroms, is then deposited over the exposed diffusion region, the cap layers, and the sidewall spacers. Then an insulating layer of spin on glass (SOG), silicon oxide, borophosphosilicate, or the like, is deposited and planarized over the substrate. '997 patent at Col. 1:42-50. Then, using a photoresist mask, a contact hole is etched in the insulating layer with the silicon nitride barrier layer serving as an etch stop. Finally, the silicon nitride barrier layer is removed to expose the diffusion region. '997 patent at Col. 1:51-57.

26. The '997 patent explains that the above conventional process is unnecessarily complicated, as it required two separate depositions of silicon nitride for forming the conformal layer and barrier layer. These two distinct depositions further require two individual etching steps, increasing the number of processing steps.

27. The '997 patent addresses these issues by eliminating process steps and thus reducing manufacturing costs and increasing throughput. '997 patent at Col. 1:58-67. The '997 patent accomplishes this goal by not etching the conformal layer used for forming sidewall spacers until a contact opening is formed. By

waiting to etch the conformal layer, the conformal layer can serve as an etch barrier that protects the diffusion region during contact hole etching. This eliminates the need to deposit a second separate silicon nitride layer for the sole purpose of serving as an etch barrier layer.

28. Furthermore, the etching of the sidewall spacers can be performed at the same time the contact hole is etched. This process, as disclosed by the '997 patent, eliminates a number of process steps, thereby improving the method for fabricating semiconductor devices. '997 patent at Col. 2:5-28.

The simplified method of the invention overall reduces one etch step and one deposition step as compared to the conventional method illustrated in Figs. 1A through 1E. Accordingly, the manufacturing cost is reduced and the throughput increased. Further, since the method of the present invention provides a better etch barrier at the contact hole etching, it is advantageous in process tolerance and reliability.

'997 patent at Col. 3:40-46.

29. The benefit of simultaneous etching the spacer and opening the contact hole is that a more streamlined process is achieved. This would reduce the processing time, improve the yield due to better alignment, and minimize the number of defects during production.

V. PERSON OF ORDINARY SKILL IN THE ART

30. I have been advised that there are multiple factors relevant to determining the level of ordinary skill in the pertinent art, including the educational level of active workers in the field at the time of the invention, the sophistication of the technology, the type of problems encountered in the art, and the prior art solutions to those problems.

31. It is my opinion that a person having ordinary skill in the relevant art at the time of invention (*i.e.*, in 1999) is a person with a Bachelor's of Science degree in material science and engineering, chemical engineering, and three to four years of practical experience in the development, design, process, and manufacturing of semiconductor chips and technology. That person would be familiar with the issues such as integrating an interconnecting layer in the structure of fully processed semiconductor device. An individual with an advanced degree in material science and engineering or chemical engineering, would require less experience in the development, design, process, manufacturing, and integration of processes of semiconductor chips and technology (*e.g.*, two to three years).

VI. CLAIM CONSTRUCTION

A. “forming a conformal layer of [etch barrier material/silicon nitride] overlying the substrate”

32. I understand that Samsung has proposed that the term “forming a conformal layer of [etch barrier material/silicon nitride] overlying the substrate” be

construed as “forming a layer of [etch barrier material/silicon nitride] supported by the substrate surface, the layer of [material] having a contour that conforms to a contour of one or more structures already formed on the substrate surface.” I understand that, for the purposes of this proceeding, Home is not disputing Samsung’s proposed construction for this term.

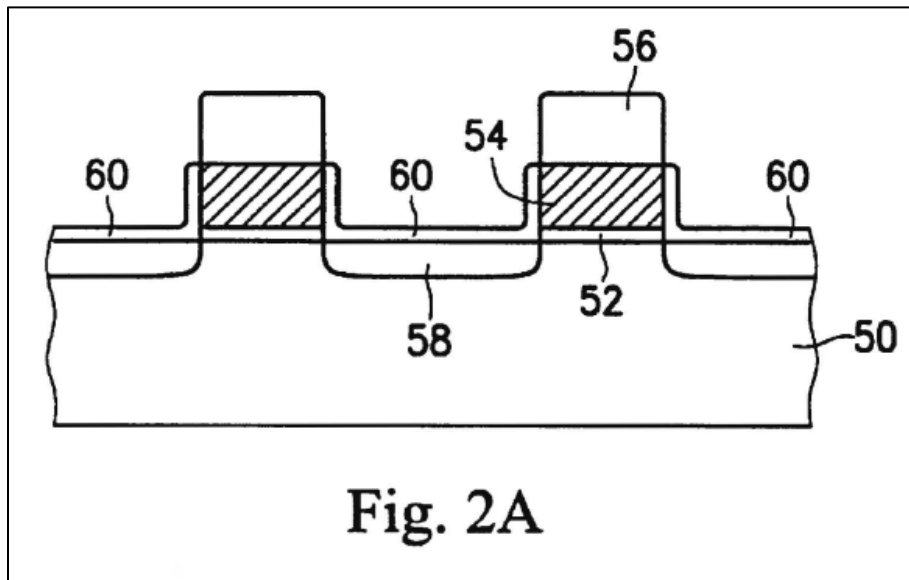
B. “forming an oxide layer over the diffusion region”

33. I understand that Samsung has proposed that the term “forming an oxide layer over the diffusion region” be construed as “forming an oxide layer above the diffusion region.”

34. I understand that Home Semiconductor has proposed that the term “forming an oxide layer over the diffusion region” be construed as “forming an oxide layer covering the diffusion region.”

35. I have considered and applied both constructions in my analysis of the ’997 patent and the prior art.

36. When describing the “oxide layer,” that ’997 patent figure show that oxide layer 60 is covering the diffusion region 58.



'997 patent at Fig. 2A; 2:55-57 (“[A] thin oxide layer 60 having a thickness of about 150 Å is formed over the substrate surface[.]”). Furthermore, the '997 patent uses “over” to refer to a structure that is covering another structure. *See* '997 patent at Fig. 1A, Col. 1:29-31; Fig. 1B, Col. 1:32-34; Fig. 1D, Col. 1:41-46; Fig. 2A, Col. 2:55-57; Fig. 2B, 2:60-62; Fig. 2C, 3:1-2; Fig. 2D, 3:17-20.

37. I believe that a person of ordinary skill in the art would understand the term “forming an oxide layer over the diffusion region” in light of the specification in which it appears to mean forming an oxide layer covering the diffusion region.

C. “etching an opening through the insulating layer self-aligned and borderless to the diffusion region”

38. I understand that Petitioner has proposed that the term “etching an opening through the insulating layer self-aligned and borderless to the diffusion region” be construed as “etching an opening to the diffusion region using a single

mask through multiple layers including the insulating layer, where the mask contact window is oversized relative to the diffusion region.” I understand that, for the purposes of this proceeding, Home is not disputing Samsung’s proposed construction for this term.

D. “spacer”

39. I understand that Petitioner has proposed that the term “spacer” be construed as “a structure that spaces between two conductive structures.” I understand that Home Semiconductor has proposed that the term “spacer” be construed to mean a structure designed to create physical separation between conducting structures.

40. A person of ordinary skill in the art understands that the term “spacer” in the field of semiconductor fabrication refers to a structure designed to create physical separation between conducting structures. A spacer is a structure that is purposefully designed into the manufacturing process in order to achieve specific functions. In the time frame of the ’997 invention, spacers were typically formed to create space between the gate electrode and other conductive structures.

41. For example, spacers are commonly formed to create space between the gate electrode and doped regions in the substrate formed through ion implantation. During implantation, the spacer shields portions of the substrate in

the area near the gate electrode, creating separation between the gate and implanted region. The extra separation helps reduce the problem of short channel effects.

42. Spacers formed on the sidewalls of the gate electrode also help separate the conductive plug from the gate electrode, which can help prevent shorting effects. This is the spacer function specifically mentioned in the '997 specification. '997 patent at Col. 3:35-38 ("Further, the same nitride layer is anisotropically etched to form sidewall spacers that prevent shorting between the gate electrode and the conductive plug.").

43. I apply these constructions as the broadest reasonable interpretation in view of the specification as would have been understood by a person of ordinary skill in the art as of Sept. 29, 1999 for the purposes of my Declaration.

VII. INVALIDITY ANALYSIS

44. Samsung relies on three prior art references in its petition for anticipation, U.S. Patent Nos. 6,277,720 (the "720 Patent" or "Doshi") and 5,770,498 (the "498 Patent" or "Becker"), and an additional prior art reference for obviousness, the article Process Induced Degradation of Thin Oxide, by C.Y. Wong, et al ("Wong"). I understand that the Board has initiated proceedings only as to the Doshi reference. My analysis below will be confined to the Doshi reference.

1. U.S. Patent No. 6,277,720 (the “720 Patent” or “Doshi”)

45. Doshi describes a method for fabricating an integrated circuit with a silicon dioxide layer that is doped with both boron and phosphorous and a silicon nitride layer below. Doshi further describes contact openings that are etched through the BPSG layer and then through the silicon nitride layer using a two-step etch process. Doshi at Abstract.

46. Doshi describes the conventional method of forming an integrated circuit. First the gate structures are disposed at various locations of the surface of the structured, overlying a gate oxide layer in order to define the channel regions of the transistor devices. Doshi at Col. 2:25-28.

47. The gate structures are fabricated with layers of polysilicon and a metal silicide. During the formation of the gate structure, a sidewall filament consisting of insulating material such as silicon dioxide or silicon nitride are typically formed at this time. Doshi at 2:25-40.

48. Then, a silicon dioxide film is disposed over the entire surface of the structure by way of chemical vapor deposition (CVD). Doshi at Col. 2:41-49. After deposition, the structure is subjected to a high temperature anneal and an etchback is performed. Doshi at Col. 2:51-55.

49. Following this, contact openings are then defined by photolithography and etched through undoped oxide films to expose locations of the gate structures and source/drain regions. Doshi at Col. 2:56-61.

50. According to Doshi, the purpose of undoped oxide film to serve as a barrier to boron and phosphorus dopant contained within the BPSG film which may occur during high temperature processes, as diffusion of dopant from BPSG film into the active regions is undesirable. Doshi at Col. 2:66-3:17.

51. As device sizes decrease, the undoped oxide film becomes incapable of preventing dopant diffusion because the thickness of the undoped oxide film decreases correspondingly. Doshi at Col. 3:18-21. The thickness of the undoped oxide film cannot be increased to prevent the dopant diffusion as it would result in undesirably dense integrated circuits. Doshi at Col. 3:21-24. Doshi was intended to address these issues. Doshi at Col. 4:10-18.

52. Doshi discloses the use of a silicon nitride diffusion barrier layer underlying a planarized doped oxide layer. Doshi at Col. 4:10-42. The methods for fabricating integrated circuits largely follow the conventional methods. However, instead of just an undoped oxide film barrier layer and BPSG film overlying the gate structure, Doshi discloses multiple layers, a nitride layer, a BPSG layer, an oxide layer, and an insulating layer, overlying the gate structure. Doshi at Col. 5:38-42.

53. In Doshi, after defining the gate structures, implants are performed to define source/drain extensions. Then the sidewall filaments (which are the spacers in Doshi) are formed, by first oxidizing the sides of the polysilicon layer and then by depositing a layer of silicon nitride overall which is then anisotropically etched to remove the nitride from flat surfaces, leaving sidewall filaments behind. Doshi at Col. 7:52-62. After the sidewall filaments are formed, source/drain implantation and anneal is performed to form source/drain regions, and then, only after the formation of the source/drain regions, the gate oxide layer is removed overall. Doshi at Col. 7:66-8:5.

54. After the removal of the gate oxide layer, a silicon nitride layer is formed, preferably by way of low-pressure chemical vapor deposition (LPCVD), to serve as an important dopant barrier layer to boron and phosphorous. Doshi at Col. 8:8-55. According to Doshi, it is preferred that the silicon nitride layer be as thin as possible to minimize etch time. Doshi at Col. 8:14-16.

55. After the deposition of the silicon nitride layer, the BPSG layer is deposited, annealed, and etched without patterning. Doshi at Col. 8:66-9:4. This etchback of the BPSG is simple etch which leaves the upper surface of the BPSG layer substantially planar. Doshi at Col. 9:4-9. Then contact opening locations are defined by conventional photolithography. Doshi at Col. 9:26-33.

56. Doshi discloses that the etching of the contact openings through the BPSG layer and the nitride layer at this time is typically a two-step etch process. The first etch is a “dry” etch of the BPSG layer. The second etch of the nitride layer is timed, brief and performed under similar conditions. Doshi at Col. 9:34-10:3. Doshi states that this two-step etch is particularly beneficial as damage to the corners of the gate structure and sidewall filaments is substantially minimized. Doshi at Col. 10:4-16.

57. Doshi states that the nitride layer is removed from within the contact locations. Doshi at Col. 10:11-12 (“brief nitride etch used to clear nitride layer 30 from within plug contact locations PC”); 10:63-64 (“The second step of the two-step etch is then performed to remove nitride layer 30 from bit line contact location BLC.”). Doshi does not teach that nitride layer 30 is left on the sidewalls of the gate electrode to form spacers.

58. Doshi further states that the etching through insulating layers, BPSG layer, and nitride layer may be performed with a single etch step, rather than a two-step etch when spacing permits. Doshi at Col. 11:11-21.

a) Doshi Does Not Anticipate Claim 1 and 9

59. The methodology taught in Doshi is the similar to the method described in the '997 Background of the Invention and overcome by the '997 invention. Doshi describes a method where the spacer is formed in a separate step

from the formation of the contact hole. In Doshi, the two-step self-aligned contact etch process is used exclusively to form contact holes. Doshi does not combine spacer formation with the contact hole etch. The Doshi method does not reduce the number of process steps and does not simplify the manufacturing process. That is not the objective of the Doshi disclosure.

60. Doshi does not anticipate claims 1 and 9 of the '997 patent because Doshi does not disclose “anisotropically etching the barrier [silicon nitride] layer underneath the opening, thereby exposing the diffusion region *and simultaneously forming a spacer of the etch barrier material [silicon nitride] on the sidewall of the gate electrode.*” This limitation requires the formation of spacers on the sidewalls of the gate electrode at the same time as the anisotropic etch step. Contrary to the requirements of the claim, Doshi does not form spacers on the sidewalls of the gate structure during the anisotropic etch of the etch stop barrier while contact holes are formed.

61. I understand that there are two proposed constructions for the term “spacer.” It does not matter which construction is applied. Both require a structure formed to perform spacer functions. Doshi does not disclose the formation of such a structure during the anisotropic etch step. Thus, Doshi does not teach “simultaneously forming a spacer of the etch barrier material [silicon nitride] on the sidewall of the gate electrode” under either construction.

62. Doshi does disclose the formation of spacers called sidewall filaments. Doshi at Col. 7:57-62. However, those spacers are formed (and used to define the source/drain implant) before the nitride layer 30 (the etch barrier) is even deposited. Thus Doshi already has spacers in the form of sidewall filaments 11. It does not need to form additional spacers from nitride layer 30. This would add complication to the process for no reason. This explains why Doshi never states that the nitride layer is left on the sidewall or that it is there to form a spacer on the gate electrode after the contact hole etch process.

63. When describing the contact etch process, Doshi teaches that nitride layer 30 is removed from the contact hole locations during the nitride etch step.

[T]he brief nitride etch used to *clear nitride layer 30 from within plug contact locations PC* has been observed to be highly anisotropic[.]

Doshi at Col. 10:11-13 (emphasis added).

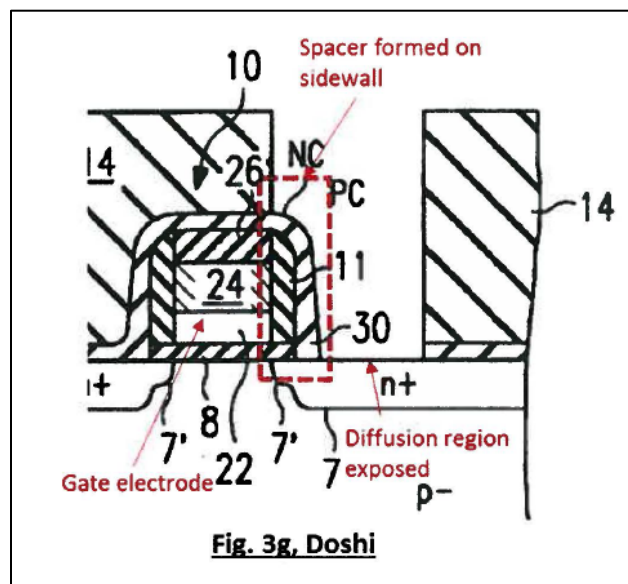
The second step of the two-step etch is then performed *to remove nitride layer 30 from bit line contact location BLC*.

Doshi at Col. 10:62-63 (emphasis added).

64. The objective of the nitride etch is to clear the nitride layer from within the contact locations and expose the source/drain regions in the substrate. Doshi never states that any portion of nitride layer 30 needs to remain following

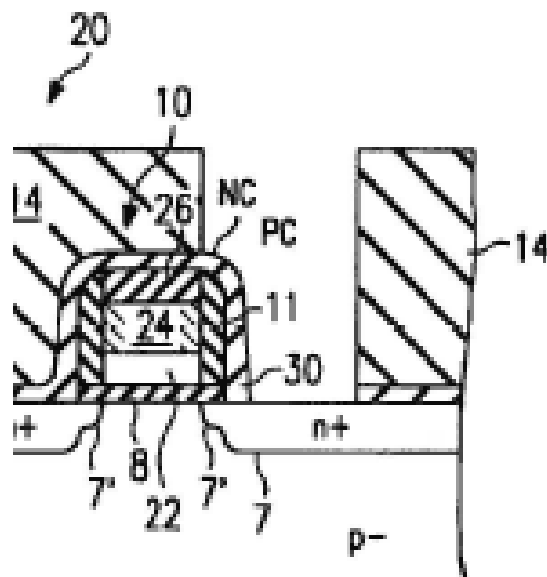
the etch process and definitely doesn't describe using the material to form a spacer on the sidewall of the gate electrode.

65. Samsung points to Doshi Fig. 3g, showing the results of the nitride etch at PC locations, as evidence that nitride material remains on the sidewalls of the gate electrode after the nitride etch step.



Pet. at p. 27. Doshi's depiction of the etch result in PC locations is inaccurate.

66. Samsung itself has pointed out that Fig. 3g fails to show the removal of nitride material at the top of the gate. This material on the top should have been etched similar to the way it was etched at the bottom of the contact opening.

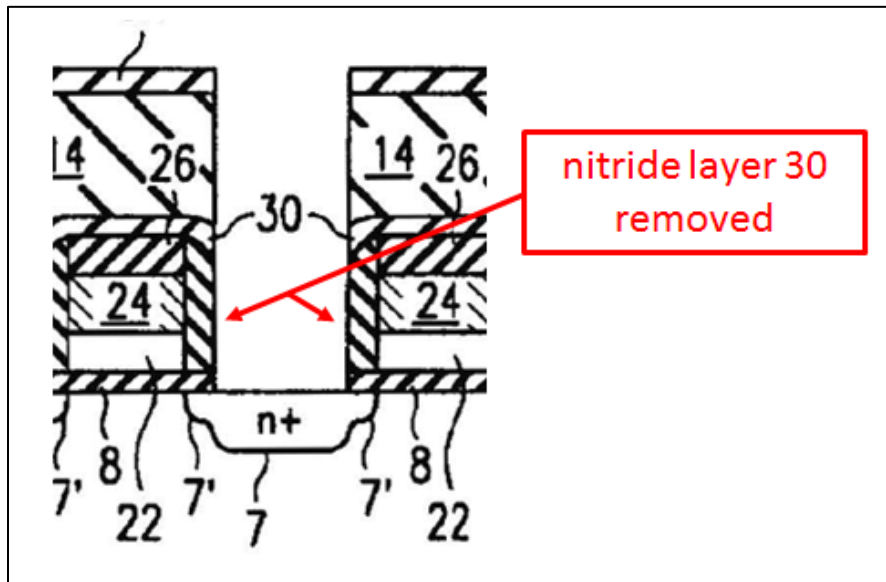


Doshi, Section of Fig. 3g.

67. The error isn't just confined to just the top corner. The nitride etch process designed to clear the nitride layer 30 would etch other portions of layer 30 exposed under the contact opening. Oddly, Fig. 3g shows the portion of nitride layer 30 covering the gate as completely unaffected by this etch process. This is an undeniable error.

68. Doshi's error in depicting the result of the nitride etch in PC locations is confirmed by comparison to Doshi's depiction of the same result in the BLC locations. Doshi describes forming BLC contact opening using essentially the same etch process as that used for the PC contact openings. Doshi at Col. 10:40-11:21. In fact, the nitride etch parameters are identical. Doshi at Col. 10:63-11:10 (showing both nitride etches with the same process parameters, stating that "[t]he second step is substantially identical to that performed in the two-step etch of plug

contact locations PC.”). Because the etches are the same, they should etch through the nitride layer 30 with the same result. When depicting the BLC etch in Fig. 3k, Doshi shows the entire exposed portion of nitride layer 30 removed from the BLC contact location.



Doshi, Section of Fig. 3k (annotation added).

69. This result is both expected and consistent with how Doshi describes the nitride etch process. Doshi at Col. 10:63-64 (“The second step of the two-step etch is then performed to remove nitride layer 30 from bit line contact location BLC.”). There is no indication that Fig. 3k’s depiction of the etch process in the BLC location is erroneous or unreliable.¹

¹ It is worth noting that Samsung’s expert Dr. Rubloff drew his conclusion that nitride material remains on the sidewall based on Fig. 3g, even while noting the clear error in the drawing. Rubloff Dec. at A-13 (citing Fig. 3g as showing material left on the sidewall after the nitride etch of nitride layer 30); A-14 (noting

70. A person of ordinary skill in the art, reading Doshi, would understand that nitride layer 30 would effectively be removed from within the contact opening locations (both PC and BLC locations). Doshi states that nitride layer 30 should be made “as thin as possible to minimize etch time.” Doshi at Col. 8:14-16. This indicates that Dosh had no intent to leave nitride material following the etch process. If Doshi wanted to form sidewall spacer, it would have required a least a sufficient thickness to ensure that enough material would be left after the etch to form those spacers. Doshi doesn’t do that.

71. Moreover, even though the nitride etch is anisotropic, it would still be able to clear a thin layer like nitride layer 30. First, some of the nitride layer would already be removed during the initial oxide etch. Although the anisotropic nitride etch would etch faster in the vertical direction, it would still remove some material in the lateral direction. In addition, the nitride etch would be designed to include over etch to ensure that there is no nitride (or residual oxide) left on the substrate surface that could interfere with forming a good contact. Due to the normal variability of layer thickness and etch processes across a wafer and from die to die, the etch processes must have a safety margin of over-etch. In fact, making sure

that Fig. 3g does not accurately depict the effect of the nitride etch on the nitride layer 30). He either chose to ignore or simply did not consider that Fig. 3k showed the entire nitride layer removed in the BLC location using the same nitride etch of the same nitride layer 30 within the same type of contact opening. Rubloff Tr. at 210:17-212:12.

that residual insulating material is completely cleared from the contact opening is the primary objective of the etch process since this will directly affect the performance of the device. All of these factors, in addition to the specific teaching of the Doshi reference, indicate that the nitride layer 30 is effectively removed from within the contact opening.

72. If Doshi wanted to teach that the nitride layer 30 remains on the sidewalls to form a spacer, it could have stated that explicitly. That is what Doshi does when it describes its actual spacers, the sidewall filaments 11. Doshi at Col. 7:52-62 (“A layer of silicon nitride material is deposited overall, and then etched anisotropically to remove nitride from the flat surfaces, leaving sidewall filaments 11 behind.”). Yet with respect to nitride layer 30, Doshi only refers to it as a diffusion barrier and an etch barrier. Doshi never states that any part of nitride layer 30 remains on the gate structure after the contact hole etch. Doshi is, at best, agnostic as to whether any residual nitride material remains on the gate structure. It is impossible to conclude that Doshi specifically discloses the formation of spacers when the issue is completely unaddressed, in fact the word “spacer” is never mentioned in Doshi.

73. Even if some residual nitride material was left on the sidewalls of the gate structure, that material would not be considered spacer. A spacer is a structure designed with a purpose and function. It would need to be a specific

material, shape, and dimension that are important to achieve its intended function. Doshi did not indicate that any nitride material 30 remains to form a spacer, much less state a purpose or the design characteristic to achieve a spacer function. A spacer is a specific structure that needs to be carefully designed into the structure of the device. It is not some residual material that one speculates might be left over from an etch process. Thus, even if the anisotropic nitride etch process did not fully clear all the nitride material left on the sidewalls of the gate, that leftover residual material would not be a “spacer” as required by the ’997 claims.

74. The material left on the sidewalls, if any, would not have a predictable and uniform shape or thickness after the etch process. As such, it could not reliably be used as a “spacer.” Any attempt to depend on this residual material on the sidewalls as a spacer would greatly increase the risk of conduction between the gate and the contact plug resulting in a defective device.

75. Doshi’s process does form spacers, but not out of the nitride layer 30. Doshi states that after the formation of the gate electrode stack, a layer of silicon nitride material 11 (not the etch barrier layer required by the claim) is deposited over the structure. The nitride material is then etched anisotropically to remove nitride from the flat surfaces and define sidewall filaments on the sides of the gate electrode. Doshi at Col. 7:52-62. These sidewall filaments 11 are the “spacers” that are then used to help control the source/drain implantation.

76. The discussion above applies equally to both claim 1 and claim 9.

b) Doshi Does Not Anticipate Claim 2 or Claim 9

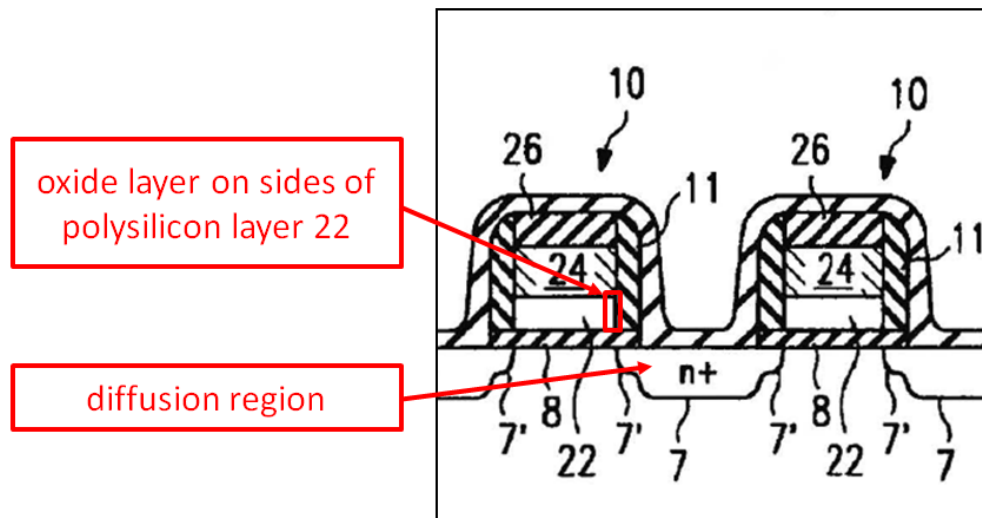
77. Doshi does not anticipate claim 2 or claim 9 which require “a step of forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode by thermal oxidation.”

’997 patent at Col. 4:5-8; 4:32-34.

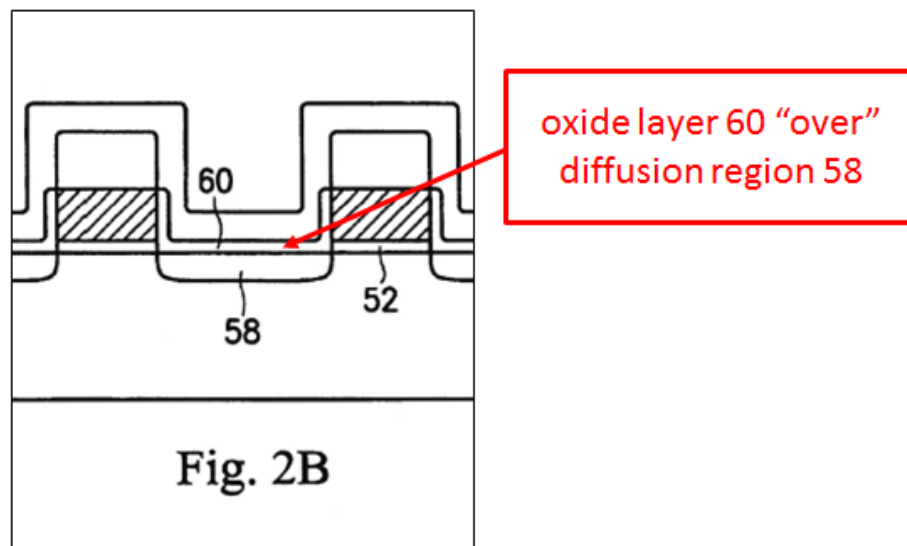
78. Doshi does not teach forming an oxide layer of the diffusion regions. Doshi states that the sides of the polysilicon layer are oxidized. Doshi at Col. 7:57-59 (“According to the preferred embodiment of the invention, sidewall filaments 11 are formed by first oxidizing the sides of polysilicon layer 22.”). Doshi does not mention forming an oxide over diffusion regions and does not depict such an oxide layer in any of its figures.

79. The oxide on the sidewalls of the gate electrode are not “over” the diffusion regions. The word “over” as it is used in the claim limitation and in the specification should be understood to mean covering. Thus, any oxide layer that satisfies the claim limitation must be formed such that it covers the diffusion region. An oxide layer formed on the sidewalls of the gate electrode, at the interface between the polysilicon layer 24 and the sidewall filament 11, would not cover the diffusion region.

80. The ’997 patent clearly illustrates how layer 60 covers layer 58.



Doshi at Fig. 3b (annotations added to show what Samsung claims is an oxide layer “over” the diffusion regions).



'997 patent at Fig. 2B. As illustrated above, when the '997 patent claims an oxide layer formed over the diffusion region, it is claiming a layer that is actually covering that region, not just higher but off to the side.

81. Samsung's argues that the Doshi process for oxidizing the gate electrode sidewall would necessarily form an oxide layer over the diffusion region because that region is "uncovered doped silicon, which is susceptible to thermal oxidation." Pet. at p. 29. In Doshi, the diffusion region is not uncovered doped silicon during the oxidation step. That area, the source/drain regions, is covered by the gate oxide layer 8 which is not removed until *after* the oxidation process.

82. When describing the initial etch process to define the gate structure, Doshi only describes etching the nitride layer 26, the tungsten silicide layer 24, and the polysilicon layer 22. Doshi at Col. 7:44-51. Doshi does not etch the gate oxide layer 8 which, at this point, would still cover the entire substrate. Next, reach through implants are performed to define the source/drain extension regions. These reach through implants are implants that pass through the gate oxide layer 8 and forms source/drain extension regions. Doshi at Col. 7:52-65. Next, the sidewalls of the polysilicon layer 22 are oxidized and the nitride sidewall filaments are formed. Finally, the source/drain implants are performed to define the source drain regions. It is only after this stage that Doshi states that the gate oxide layer 8 is removed from over the source/drain regions. Doshi at Col. 8:3-7 ("Following the formation of the source/drain regions 6, 7, gate oxide layer 8 is removed overall, except from under the gate structures 10."). During the oxidation of the

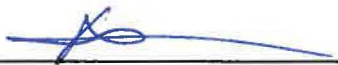
polysilicon gate sidewalls, the diffusion regions are covered by the gate oxide layer and not “uncovered doped silicon.”

83. I hereby declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct, and that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I understand that willful false statements are punishable by fine or imprisonment or both. *See* 18 U.S.C. § 1001.

Dated: August 31, 2015

Respectfully submitted,

By:



Ron Maltiel