UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SAMSUNG ELECTRONICS CO. LTD.,
SAMSUNG ELECTRONICS AMERICA, INC.,
SAMSUNG SEMICONDUCTOR INC., and
SAMSUNG AUSTIN SEMICONDUCTOR LLC,

Petitioner,

V. Case IPR2015-00459

HOME SEMICONDUCTOR CORPORATION Patent 6,150,244

Patent Owner. Patent 6,146,997

----------X VOLUME I

DEPOSITION OF

GARY W. RUBLOFF, PHD

Washington, DC 20005

Tuesday, August 18, 2015

Reported by: Denise D. Vickery, RMR, CRR

Job No. 173194

Tuesday, August 18, 2015

9:04 a.m.

DEPOSITION OF GARY W. RUBLOFF, PHD, held at the offices of:

FISH & RICHARDSON PC
1425 K Street NW, 11th Floor
Washington, DC 20005

Pursuant to notice, before Denise D. Vickery, Registered Merit Reporter, Certified Realtime Reporter, and Notary Public in and for the District of Columbia.

A P P E A R A N C E S

For the Petitioner and the Witness:
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Also Present:
Ron Maltiel, RMG and Associates

I N D E X

E X H I B I T S

RUBLOFF

(Exhibits attached to transcript.)

P R O C E E D I N G S

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GARY W. RUBLOFF, PHD

called for examination, and, after having been duly sworn, was examined and testified as follows:

EXAMINATION

BY MR. CHEN:

Q. Good morning.

MR. MUKERJI: We should probably -- I'm sorry to interrupt. We should probably do introductions --

MR. CHEN: Sure.

MR. MUKERJI: -- since we don't have a video camera and all that.

You want to go first?

MR. CHEN: Sure. Jerry Chen from TechKnowledge Law Group representing respondent, Home Semiconductor Corporation. With me is Ron Maltiel, expert for Home Semiconductor Corporation.

MR. MUKERJI: Indranil Mukerji and David Holt of Fish & Richardson representing the

petitioner and the witness here today. When I say "petitioner," I mean petitioner in all four of the RPIs that will be covered by this deposition or this cross-examination.

I'll also note for the record before we went on the record, counsel and I had a discussion about apportioning the cross-examination so it's clear which cross is for which declaration, and I think we agreed to try to work together on that.

BY MR. CHEN:

Q. Sure.

A. Am I supposed to introduce myself?

MR. MUKERJI: You'll be introducing yourself all day.

THE WITNESS: Okay.

MR. MUKERJI: So we can get going.

BY MR. CHEN:

Q. Good morning, Dr. Rubloff.

A. Good morning.

Q. My name is Jerry Chen. I'm an attorney with the firm of TechKnowledge Law Group. I

represent respondent, Home Semiconductor Corporation. I'll be taking your deposition on cross-examination today in connection with the IPRs filed by Samsung against the Home patents.

In today's cross-examination, I'll ask you questions related to the subject matter at issue in those RPIs. You will need to answer my questions truthfully and completely. The court reporter will record my questions and your answers in writing.

As explained, if your attorney objects, you may -- you must still answer all my questions.

You understand?

A. I understand.

Q. Okay. If you do not hear or understand my questions, please ask me to repeat or clarify. If you answer my questions, my assumption will be that you understood the questions.

You understand?

A. Yes.

Q. And if you need a break, please let me know and we'll take a break.

A. Thank you.

Q. Okay. Can you think of any reason that might affect your ability to provide truthful and complete answers to my questions today?

A. No.

Q. Okay. Do you have any questions before we start?

A. No.

Q. Okay. Dr. Rubloff, could you please state and spell your full name for the record?

A. Gary, G-a-r-y, Wayne, W-a-y-n-e, Rubloff, R-u-b-l-o-f-f.

Q. Dr. Rubloff, are you being compensated for your work on these matters?

A. Yes.

Q. What is your compensation?

A. For my time it's $400 an hour, and I think it's 600 an hour for deposition and testimony. I'm not sure about that.

Q. Okay.

A. I don't really remember what our agreement was.

Q. Okay.

A. But that's what it's been in some previous times.

Q. Are you currently retained by Samsung as an expert witness for other matters?

A. No, just the four things that are today.

Q. Okay. Prior to these current matters, these four IPRs, had you worked for Samsung on any other matters?

A. No.

Q. How long have you worked as an expert witness?

MR. MUKERJI: Objection to form.

THE WITNESS: You mean when was the first date that I did anything like this? Is that what the question is?

BY MR. CHEN:

Q. Sure. Yes. How long have you been working as an expert witness?

A. You mean in general for -- for different cases?

Q. For different cases, yes.

A. Yeah, I think -- I don't remember exactly, but I think I did a small case in California maybe in late '80s or early '90s. I don't remember.

Q. Okay.

A. And just a few cases since then.

Q. Were they all patent matters?

A. When you say "patent matters," you mean IP generally? I mean --

Q. Cases related to patents.

A. Yes. Yes.

Q. Were they all related to semiconductors?

A. Depends what you mean by "semiconductors."

Q. What was the subject matter of the cases generally?

A. So one, a small first one I recall had to do with semiconductor processing equipment, and then the only two that have been really kind of serious time consuming have been in LCD displays and the electronics, control transistor electronics that

goes into LCDs.

Q. Okay. Do you know how many cases prior to these matters you worked on as an expert witness?

A. Not offhand.

Q. Less than 10?

A. Yes, less than 10.

Q. Less than five?

A. I don't know.

Q. Okay. Do you remember in those prior cases whether you represented the patent holder?

A. I don't remember about -- so there were two large LE -- LCD cases, and I think I represented the owner of the patent. It was an infringement. No. I'm sorry. I'm sorry. Yes, I represented -- excuse me. I represented the holder of the patent who was suing for infringement.

Is that the right way to say it?

Q. Yes.

A. And in the first case, I don't remember who owned the patent.

And then for completeness, there were a couple of little things where people needed my

advice or wanted me to go to the Patent Office where they have -- they're having an informal hearing with the examiner, some things like that, but that's it.

Q. All right. But these cases are the first cases that you worked on that are related to a petition for review before the Patent Trial and Appeal Board?

A. You mean IPR cases?

Q. Yes.

A. I think so. I think I had one opportunity where I was asked to go to the Patent Office to talk with the examiners about the request that had been made for reexamination, but I think that's different from IPR.

Q. Do you remember when that case was?

A. I would guess three or four years ago, but I'm not sure.

Q. And in that case, did you represent the patent holder?

A. I don't know.

THE REPORTER: Exhibit 1.

(Document marked, for

identification purposes, as Rubloff Exhibit No. 1.)
BY MR. CHEN:
Q. Dr. Rubloff, I've asked the court reporter to mark as Exhibit 1 your curriculum vitae. I hope I pronounce that right. I'll just call it CV.
A. (Laugh).
Q. Please take a moment to review this document.
A. (Reviewing document). Okay.
Q. All right. Dr. Rubloff, is this your CV?
A. This is my CV as of I don't know what date, recent, fairly recent, but not completely up to date.
Q. Up to date with respect to at least this year, though?
A. Well, I don't know. I'd have to look in detail at some of these. I'm sorry. I think it's a fairly small matter, but I wouldn't like to say that it's certainly up to date as of a year ago. Because if you'll look at these conference

organization activities, you know, we're required -- not required but expected to have these long CVs.

Q. Right.

A. And, frankly, they're very hard to keep, up -- up to date on. So conference organization activities, I'm sure that there are things now in that don't appear here --

Q. Okay.

A. -- and probably more than a year ago.

Q. Okay.

A. Very hard to keep this kind of thing up to date.

Q. Sure. But largely current at least through 2013/2014?

A. Mostly current.

I guess I should note one or two things that have changed. I'm pleased to say that my position as director of the Center for Nanostructures for Electrical Energy Storage and my role as -- where is it here -- founding director of the Maryland NanoCenter have changed temporarily because I have acting directors for both of these.

Q. Okay.
A. Since I'm on sabbatical.
Q. Okay.
A. I'm very pleased to report that.
And probably the number of publications and stuff, that's changing on a weekly basis. So --
Q. Sure.
A. -- that won't be up to date.
Q. Okay. Now, Dr. Rubloff, have you worked in the field of semiconductor manufacturing?
A. In -- yes. Yes. In the -- in the research domain and in connection with people who are actually doing manufacturing and the development of manufacturing strategies.
Q. So you haven't worked directly yourself in doing manufacturing or developing manufacturing strategies; is that right?
MR. MUKERJI: Objection to form.
THE WITNESS: No, that's not the case. No. I have worked in manufacturing strategy development.
BY MR. CHEN:

Q. Oh.

A. I should mention, there's a publication on the list here, which I think was 1992, in the IBM journal, which is actually a summary of the work that I had done in research and collaborated with Don Bordonaro in IBM Burlington, who was in charge of the Strategic Equipment Council -- I think that's what it was called -- for the IBM Corporation.

So they were the ones central to making decisions about what kinds of tools to buy, what design changes are needed, and really driving the move toward manufacturing cluster tools. So that's -- that you can see in that publication.

And what was interesting about that is that my research groups were doing the research counterpart of cluster tools, which I'm sure we'll get into, and so we put our heads together and wrote a review paper about where this is actually going.

Q. When did you first start working with semiconductor manufacturing?

A. I guess the right introduction to that, it's a little cloudy how you would describe it

because I started out in as a kind of pure scientist in materials surfaces, and I got interested in electronic materials, which are relevant to semiconductor manufacturing, in about 1977.

And that underwent continuous evolution from kind of the science of interfaces of electronic materials, to the processes and equipment, to the integration of those schemes into process integration flow. And so by -- let's see. It was on silicide interfaces and then it went to CVD and etching and so on, and I would say -- let's see.

I joined the Silicon Technology Division in 1986 as a manager, and in 1985 I was a technical staff person to the vice president for logic and memory. So somewhere in there my science evolved to the technology and, in particular, the manufacturing aspects where -- where what I'm talking about is: What kinds of equipment do you use to make these kinds of devices? And how does that equipment carry out what you want to make these devices? And what are the manufacturability issues that are associated with using those things? In

particular, both equipment and also the process flow.

So I was very sensitized to that in those days, and I guess I'd say that that certainly, the time frame of around 1980, if you had asked me then, I would say, yes, I'm interested in working on aspects critical to semiconductor manufacturing.

Q. Okay. And was your work in research?

A. I was in the research division, but I had collaborations and interactions and -- I don't know -- partnerships with people at IBM Fishkill and IBM Burlington. Don Bordonaro, who I mentioned, I think his organization was central in helping and, as I hear it, underwriting applied materials to development of the 5000, which was the pioneering cluster tool that was introduced, I think, in 1987.

MR. MUKERJI: Dr. Rubloff -- before you ask the next question -- I'll just remind you. I don't know what confidentially -- confidentiality obligations you may have to your prior employers and that sort of thing, just respect that.

THE WITNESS: Yes.

MR. MUKERJI: This is a public proceeding. So don't reveal anything confidential. If you have a question about that, let us know.

THE WITNESS: Okay. Yeah. I think that there isn't anything, but I've been gone 20 years from IBM.

So to finish that story, as I -- as I worked in silicon technology, I became acquainted with the kinds of people who are doing device integration strategy and interacting with them and that was a nice residence because it related our capabilities in process research to their manufacturing considerations.

And then about the time -- let's see. This would have been, I guess, probably in the CV, of course.

Yes. So in 1992, I moved from a management role in silicon technology to a management role in manufacturing research department, and that allowed me to get new interactions and perspectives on particularly the

role of process modeling, logistics, factory flow, things like that. And these I think -- and I moved my niche in experimental research to process sensing for advanced process control.

And so I kept -- I know this is a slightly long-winded answer, but the fact is that I kept evolving into manufacturing and in the first technology roadmap, which was 1994 for the semiconductor industry, I was involved in the metrology section and we started the emphasis then on advanced process control, which has since become a reality.

So my research was in doing CVD process and can we tell what's the chemistry happening on the surface at that time by using appropriate sensors, and how do you turn that into a way of controlling those tools.

There are some very nice stories actually to tell about that.

BY MR. CHEN:

Q. So let me see if I can -- you know, correct me if I'm wrong in terms of how I summarize

your experience.

Your own work in the '80s was in research, but you collaborated with individuals who were more directly involved in manufacturing and your research had applicability to semiconductor manufacturing?

A. I think that's a reasonable approximation to what I gave as a much longer description.

Q. Did you work in the FAB?

A. Well, that's a complicated question. In a manufacturing FAB, the answer is no. In a development FAB, I had times when I would interact with people occasionally in that environment. In the research division, it's complicated because of the structure of IBM.

In the research division, we had an advanced clean room, which was a partnership with the Fishkill development divisions and the Burlington development and manufacturing divisions. So it's really hard to say where the line is there.

And my -- I had a number of management

roles and then, in addition, I'm a research staff member. I do research and that -- that research included management responsibilities for what was called -- yeah. Now, I can't remember the name of it, but an exploratory clean room facility in Yorktown research. So, and I was in that facility on a fairly regular basis.

So I know what a clean room is.

Q. But -- okay. But you didn't work in a manufacturing lab that was used to make commercial product; right?

A. No, I was not in the FAB in Burlington or Fishkill on a regular basis.

Q. Did you work in the field of thin films?

A. Certainly.

Q. What was your experience with thin films?

A. Let's see. My research in thin films, I guess I would say, started in around 19 -- I wonder if I can tell from here. It would have been -- I started IBM in '73. I think it must have been

about '77 when I turned my attention from catalytic surface science problems to the formation of metal silicides at the metal silicon interface. So that was depositing a thin film of metal, look at how it reacts with the silicon underneath, how silicides are formed, and all the implications that came from that.

And the thin film work has continued to this day and included the next generation of that work was MOS structures, metal-oxide-semiconductor structures, based largely on thermal oxidation. And then chemical vapor deposition and that was aimed at the silicon industry primarily, although later on we had sojourns into gallium nitride since I've been at Maryland, and so it's been continuously thin films of one sort or another.

Today it's atomic layer deposition which is a derivative or, let's say, the forefront of CVD for building nanostructures.

Q. Okay. How about etching? Did you do work with etching?

A. Yes, primarily dry etching or plasma

etching as you might call it. A little bit wet etching. We use wet etching as a kind of, you know, workhorse for simpler things.

Q. How about did you work with lithography?

A. Yes.

Q. What type of work did you do with lithography?

A. So most of our work didn't require high resolution lithography because we were really studying thin films and interfaces, but there have been some cases where we've done that especially more recently because we use -- so in the NanoCenter, which I direct, or not this semester but I direct, we have a clean room facility.

So I'm responsible ultimately for that, and so there's plenty of lithography. And then the program, which actually should be a CV correction here, I'm no longer doing biomaterials and bioMEMS, but for that we do lots of lithography as well as for the energy devices.

Q. Did any of your work with lithography

relate to semiconductor manufacturing?

A. Indirectly I would say, not principally.

Q. Did you do work with semiconductor process integration?

A. Yes, in various flavors. In one case, as one kind, the laboratory that I started in 1986 at IBM included capabilities for various kinds of chemical growth and evaporation techniques for deposition and also surface cleaning and -- let's see -- some -- some ion beam plasma work, not a major feature.

And there we were interested in looking at: If I put down a layer of this material under these conditions, what does that do to the next layer of some other material? In other words, that was the one embodiment of looking at the question of process integration, which is a very critical question.

But in another sense, the interactions that -- that I had with various people in IBM in research, particularly there were people that I

recall quite well interacting with, who would present a problem like this. Actually, one of them was: How do we make a self-aligned shallow trench isolation? And what can your CVD process do for that? And what's the dependency on etching?

And so I remember that in those days, because we knew how to do some of these processes and we were interested in semiconductor manufacturing technology, I and the people in my group had a lot of interaction with the device integration people in the silicon technology division who were working as part of what was called the ASTL, Advanced Silicon Technology Lab, that partnered our research division in Yorktown with IBM Burlington and IBM Fishkill development and manufacturing science.

So this notion of process integration is one that I've been, I would say, far more close to in kind of the strategic implications than how much I could do in my own research lab.

Q. So you didn't do any direct research with semiconductor process integration; is that

right?

MR. MUKERJI: Objection to form.

THE WITNESS: Would you restate that, please?

BY MR. CHEN:

Q. I was just trying to clarify the last statement you made.

You said that:

This notion of process integration is one that I would say that I'm far more close to in kind of the strategic implications and how I could do in my own research lab.

And I so wanted to clarify whether you meant that you didn't actually do any direct research or direct work with semiconductor process integration; is that right?

MR. MUKERJI: Same objection.

THE WITNESS: I don't think that's a fair way to characterize it.

So I was referring primarily to my discussions in the '80s --

BY MR. CHEN:

Q. Okay.

A. -- and early '90s with IBM technology people in research and in other divisions --

Q. Okay.

A. -- when I made that statement.

In terms of how much my -- let's say my publishable research has been in process integration, I think it's been pretty substantial.

Q. Okay.

A. So, for example, at a certain point in I think about late '80s, people were interested in making high-density capacitor structures and the question was: What can you do to make a high surface area out of thin film technology? And the answer to that we found was to use nucleation-controlled growth that allows you to make rough silicon surfaces.

Out of that I think we have a patent and a number of publications. That certainly is a process integration issue, although not the entire line that you have for making the device.

And then moving to the present, our

work has been recognized in energy storage, which uses the same thin film techniques as the semiconductor world does, CVD, ALD, oxidation, etc.

And we've been nationally recognized for building the world's smallest battery using highly conformal deposition by a kind of CVD technique called atomic layer deposition. Put two electrodes at either end of a nanoport and make a full-fledged battery. So that is certainly process integration example.

So, I mean, the bottom line is that my research students and the students who have to listen to me in lecture know what process integration is.

Q. Did you ever develop a semiconductor process for making a device?

A. Now, that's a very broad question. That's too broad a question for me to know how to parse.

Q. Okay. Did you ever develop the semiconductor process from beginning to end for manufacturing a semiconductor device?

A. You mean where my hands or my head were doing every single step and coming up with a different device or a different process flow?

Q. Yes.

A. No.

Q. Did you ever develop semiconductor processing --

A. Actually, I'm not sure anyone has done the whole thing alone.

Q. Okay. Did you work on a portion of a semiconductor process that was then used to manufacture a device?

A. I certainly worked on processes that are used in semiconductor device manufacturing and trying to see ahead what are the things that control that.

Yeah, I guess I could give an example. Actually, it's an interesting one.

I had a program with Northrup Grumman, which is interested in gallium nitride HEMT devices, and the trick in the HEMT device is that there's a capping layer of only 20 nanometers whose thickness

controls the performance of the HEMT device. And we developed and my group, working with the engineers at Northrup Grumman, we developed a realtime for institute sensor that could determine in realtime what the thickness and deposition rate of the CVD process was as MOCVD, gallium nitride, aluminum gallium nitride.

And we put in a process control so that in realtime we could tell how many layers are on the surface and then turn off the process when there's just the right number, and they were able -- we were able to control the aluminum gallium nitride cap layer thickness to 1%.

Q. Did you ever develop portions of a semiconductor process that was used to manufacture a MOS semiconductor device?

A. An M-O-S?

Q. Yes.

A. The one example was that we did some work on understanding the stability of the thermal SiO2 silicon interface high temperature annealing and we looked at what are the degradation mechanisms

that happen. And we started in research with the supposition that, well, if we can control the cleanliness of the process environment, the kind of thing cluster tube people worry about, we might be able to make better structures. We found exactly the reverse.

What happened was, there's a reaction where the silicon and the SiO2 form volatile silicon monoxide, which comes off the surface and ends up causing activation of existing defects, making them electrically active, and then later on leads to voids in the oxide film.

So this actually was the subject of both a number of publications and a patent, and in a sense that was adopted in manufacturing, but I'll tell you how.

Gary Barner, who was at Yorktown, was working with colleagues in Burlington. And they had noticed that when they did annealing in what they thought was a really good furnace, really clean, that the devices failed too often, more often than usual. And then he remembered our work and he said,

oh, they taught us what's going on there and all you have to do is to put some little bit of water or oxygen into the annealing environment. This problem will go away, and it did.

So I don't know what it really led to but --

Q. So --

A. -- that was gratifying.

Q. So your work, again, had applicability to semiconductor manufacturing or the manufacturing of semiconductor devices; is that what you're saying?

A. I think it had some relevance to them. You know, the people who work in development are usually doing a more evolutionary approach and more practical approach because you're trying to make things work.

Q. Right.

A. We were doing research that had, I think, a remarkable level of interaction and impact compared to what most people do in research.

Q. But your work wasn't in development;

correct?

A. No, I was in the research division.

Q. Okay. And so you didn't ever develop a semiconductor process or portion of a process that was to be used directly in the manufacturing of a semiconductor device; is that fair?

MR. MUKERJI: Objection to form.

THE WITNESS: It's hard for me to measure that because we had a very integrated environment in IBM across its divisions from research to manufacturing, and part of my hesitation is that the program that I started in 1986 at IBM was in a sense pioneering.

We brought together ultraclean process environments that could be coupled into process integration sequence, and part of that work was in low temperature epitaxy, which is sometimes called UHV/CVD epitaxy.

Bernie Meyerson was primarily responsible for that, but I think his ability to make that happen came from the vision that I had and that he and one or two other colleagues had in

creating this research -- special research environment. We call it integrated processing, but it's really a research version of cluster tool manufacturing.

BY MR. CHEN:

Q. Did you ever develop semiconductor processes for use in a commercial semiconductor device?

A. Well, I'll give you kind of the same example that this UHV/CVD epitaxy that Bernie Meyerson was primarily responsible has been a huge hit and certainly in manufacturing, but he was really the driver of that. And he built on some of the things that we together talked about and realized in my lab and the example I gave you of ultraclean annealing of MOS structures and so on.

Q. How would you distinguish between the field of research that you worked in and the development field?

A. In the research division, we had the freedom to choose which processes, which devices, which sequences of processes and structures and

devices we wanted to focus on. In development, there's a technology roadmap where we know that the industry has the -- it used to call it the national technology roadmap for semiconductors, then the international technology roadmap for semiconductors.

And then so this is pre-competitive roadmap where people should be trying to move the technology, and I would say that that roadmap defines vectors of what people should work on and that's what people in development largely do.

But now and then research can play a role in changing which vectors are adopted or making new vectors. So I think maybe a simple way to put it is that development is really mission oriented. Research has a mission, but it's an adjusted one. It's more adjustable mission.

Q. Do you understand what are the general goals in semiconductor manufacturing?

A. I think so.

Q. What are those general goals?

A. Well, very generally speaking, kind of broad-brush perspective, they're interested in

increasing performance, increasing or at least not hurting reliability, driving down costs, and those are leveraged by other things such as factory flexibility, process integration alternatives, and so on. Oh, and availability of equipment, equipment design.

Q. And these general goals are the typical objectives that someone might have when they're trying to develop a semiconductor process; correct?

MR. MUKERJI: Objection to form.

THE WITNESS: I think it depends on who's developing a process. So you said "a semiconductor process." Let's say I'm trying to develop an MOS isotropic etching process. I'm probably a process engineer, not a process integration specialist. My task is to make that single process work better.

So I really don't have as my mission the larger system goal of improving manufacturing costs and performance and so on. I have one piece of the puzzle. So that's quite different.

BY MR. CHEN:

Q. So the general goals that you had mentioned before are goals for the larger system?

A. Yes.

Q. All right.

A. Somebody, somebody at the top of the organization has to worry about those goals. Let me give you an example what I'm talking about.

In something like the -- what would have been the mid-'90s when I had been at North Carolina State University and I came to Maryland, where there were a different set of skills in the institute that I directed, we had a National Science Foundation program supported by also the Semiconductor Research Program to understand the interaction between an individual process model, like for CVD or etch or probably both of them, and the equipment models that carry out that process, which may be cluster tools and have some number of chambers on them that robots move things through.

And then you can have different numbers of these cluster tools, and the numbers that you

have in the configuration of each tells you how efficient your factory flow will be. And then the factory has to look at the horizon of what is going to be the demand for this product and that product.

So we had integrated models that went all the way from a specific materials thin film process to the horizon of changing demands and factory flow optimization.

So at the end of that is where those general goals lie, but those general goals depend on what happens at each little process. And if you make a process improvement, it will affect or may not affect the flow of product through a cluster tool or through a sector of the FAB.

So there's a whole hierarchy from individual process to the kinds of general goals that you're talking about.

Q. So I'm clear, when we talk about overall system, we're talking about the entire semiconductor process for manufacturing a device from beginning to end; correct?

A. Yes, and the way that it's made. I

mean, that's -- that's a factory, that's all the equipment in the factory, that's the sequence of processes that individual tools in the factory have to -- have to carry out.

Q. And then when you mention individual process, that is a subset of that overall semiconductor process, for example, you know, etching?

A. Uh-huh.

Q. Or deposition?

A. Yes.

Q. Okay. Who's responsible for assembling all the individual processes into a single overall system or overall process?

A. So I guess the best way to address that question is, this would typically involve a significant number of people, maybe a couple hundred or something like that. In IBM environment, only one I can speak to, these would involve development, probably manufacturing, probably equipment engineering, and some research people. So that's a team who wants to develop the next version of the

CMOS, or whatever it is, and so there will be some management leader there who has that responsibility of organizing the team and anticipating what it is that they're going to get together. Right?

Ah, I'll give you a good example.

When I was working in the -- this would have been in the '80s. When I was working on CVD, PVD processes, etching processes and so on, IBM was facing a huge transition. That transition was interconnect. We were at four levels of metal interconnect with aluminum as the conductor and silicon dioxide as the insulator.

And those people who would have been on such a team and the kind of strategic forecasters of where things can go -- this is this technology roadmapping environment -- identified the fact that it can't keep going this way because the capacitants between the wires is too large for the higher speeds. We anticipate smaller devices to give.

The resistivity of the aluminum wires is just too high, and so the desire was to replace aluminum with copper, including diffusion barriers,

adhesion layers and so on that would be necessary, and to replace the silicon dioxide insulator between the wires with low K dielectrics. These would be normally polymers or some kind of porous material.

And so there were teams of people and leaders of those teams who spent huge amounts of effort trying to figure out how do we get from aluminum SiO2 to copper polymer, and everybody was involved in that. All the people in my group.

At that time, I was second level manager, and so I had an etching group who worked under me and a physical vapor deposition group and a chemical vapor deposition group, which is kind of mine, and characterizations group, and everybody was focused on that problem.

So is there one person who's completely responsible? I don't know the answer to that. But it certainly is a hierarchal team that integrates a lot of things or you can't address that kind of problem.

And, incidentally, the change was successful. Everybody uses copper wiring today.

Q. All right. Let me again see if I understand what you're saying.

So for developing an overall semiconductor process for manufacturing a device, there will be individual team members or groups that might have responsibility or will have responsibility for a specific aspect of the process, and specific aspects might be etching or another aspect might be deposition or another aspect might be lithography; is that fair characterization?

MR. MUKERJI: Objection to form.

THE WITNESS: Those three things are essential to, let's say, changing the paradigm of going to a next generation process flow, but those are kind of at the bottom of the ladder and then there are levels in between.

So, for example, there might be a module of, well, how do we get this litho process to work with this etch process? What are the compatibilities and trade-offs between them?

BY MR. CHEN:

Q. Right.

A. It might be deposition and etchback, you know, all kinds.

Q. Okay. Let me see if I can approach it differently. I'm trying to understand the hierarchy.

A. And -- and clearly the average process engineer --

Q. Right.

A. -- who's working on one or two tools and processors, doesn't have this whole picture in mind.

Q. Right.

A. But most of them after a couple of years will understand that that etch process they're supposed to fix, the reason is it's linked to other things. If that etch process drifts off to the right, then the next thing is going to have to compensate for that or it's going to fail.

Q. Sure. Okay.

So at the -- for the development of a semiconductor process for manufacturing a device, at the base level of the hierarchy are the individual

process engineers who are responsible for specific aspects of the process like etching or deposition or lithography; is that correct?

MR. MUKERJI: Objection to form.

THE WITNESS: Well, I don't know about the base level, quite -- quite what you mean by that.

BY MR. CHEN:

Q. Okay. Could you describe again the general hierarchy for developing a semiconductor manufacturing process beginning with the --

MR. MUKERJI: Objection to form.

BY MR. CHEN:

Q. -- lowest level and then moving up the hierarchy to the individual who has the responsibility or visibility of the overall process?

MR. MUKERJI: Objection to form.

THE WITNESS: So you depicted a kind of vertical structure, a hierarchal structure. In one way or another, the organization has to have that, but you said developing a semiconductor process.

To me, that can mean an individual etch process. It can mean a kind of module etch coupled with lithography and so on, and so the people responsible for that are existing at all levels.

BY MR. CHEN:

Q. I'm talking about developing the process for manufacturing a device so it would include all the different steps that are needed to manufacture a device.

A. Well, remember that there's heritage here. It's very rare, if ever, that you just make a new -- a whole new structure.

Q. Sure.

A. Things evolve. If there are 25, 125 process steps to today's CMOS generation X, then most of the changes will be evolutionary. They might be in one process level, say etch, they might be in a module level, and it's not very often that it's something like I described with whole change in the interconnect world.

Does that help you?

Q. Not really. I'm still a little bit unclear. Maybe I'll try to approach it just another way.

The process engineer that you mentioned before who works on one of the specific aspects of the process, like etching or deposition or lithography or something of that nature, that individual is responsible for improving or developing a specific aspect of a process; correct?

A. How big did you mean the word "process" to apply?

Q. All right. Okay. You know what? This is --

A. I'm not trying to be difficult but --

Q. No, no. I understand. I want to make sure that we're on the same page in terms of how we use terms, and I think process is one of those that, depending on context, might have different meaning.

What is the term that you feel most comfortable with when I want to refer to the entire process for manufacturing a device, the process that includes, you know, multiple etch steps or multiple

deposition steps, and all those sort of individual processes?

A. I don't know what term I'd use for that. I mean, I don't think about it in that -- in that sense.

Maybe I can suggest one thing, though.

So I tell my students --

Q. Sure.

A. -- if you go to work for Intel or some company like that, first job is probably going to be equipment engineer or process engineer with a Ph.D. in this case, as my students do.

Q. Right.

A. And they are going to work with people who are, for example, they would often be an equipment engineer that has a master's degree or something like that. And I tell them that your first job is going to be kind of centered around a unit process, meaning it's etch and it's a Lam, whatever it is, etch tool.

And I tell them, what you should look for in your career is start to understand what

everybody else is doing. What's the implication of that etch process and that tool on other things in the sequence in that region? If you're working on interconnect, you're working on shallow trench isolation, or DRAM capacitors.

Because the job you really want is process integration engineer because then you're looking at several steps, and I was -- I thought about this hard when I was asked to define one of ordinary skill in the art, and I chose that to be actually for -- for all three patents at issue here.

Someone typically with a master's degree and, importantly, a couple of years of experience. Because when you come in with a master's degree, you may know how to run an etch tool, but what you really need to do is to understand its relationship to things around it in the process flow.

And so the only demarcation line I could offer is process or equipment engineer, process integration at some level, and then kind of the big driver is fourth level management or

something like that, who are organizing people at many levels if there's a major challenge to take on.

Q. Okay. So one of the terms you used was "unit process"?

A. Yes.

Q. Okay. If I use the term "unit process" to refer to, like, etching or deposition, like the specific aspect of a process, is that a fair way to use the term?

A. That's a good idea.

Q. All right.

A. That's actually what it's called.

Q. Okay.

A. Better idea. I didn't think to share that earlier.

MR. MUKERJI: Mr. Chen? I'm sorry. We've been going about an hour. You mind if we take a short break?

MR. CHEN: Sure. Let me just finish these definitions, and then we'll take a break. I was thinking about that too.

BY MR. CHEN:

Q. Okay. And then if I use the term "system process," can I use that to refer to the overall process that's used to manufacture a device that might include many unit processes?

A. I've never heard that term.

Q. Okay.

A. We'd be making it up.

Q. Well, I mean, I think it was used previously before, but is there a term then that I can use to refer to the overall process that includes many unit processes?

A. I don't know what the term would be. I'm trying to think what would be convenient for that. I mean, from a manufacturing standpoint, it's kind of factory flow. You go from this unit process, to that unit process, to that unit process and so on. But I'm not -- usually when you think about factory -- factory flow, you're thinking about the logistics of how you optimize getting stuff through the FAB and particularly associated with cost.

Q. How about integrated process?

A. This is troubling also because I've published that term too many times at the level of a short sequence of processes carried out in essentially cluster tool-type environments.

Q. Okay. So an integrated process may include multiple unit processes, but is not the full process?

MR. MUKERJI: Objection to form.

THE WITNESS: That's a really hard one because if you ask the director of IBM at Fishkill or Applied Materials Santa Clara, or something like that, what they call it, they probably use a similar kind of term. So everybody is trying to use the same term, but it's not the same thing.

BY MR. CHEN:

Q. Okay. Well, we just need to find terms so that when I'm asking you questions today in the deposition, you understand what I'm asking about and I understand what you're talking about.

So why don't we take a break, maybe you can give it some thought, and then when we come

back, we'll try to find the right term, terminology to use.

A. All right. Let me just ask a question, though.

Q. Sure.

A. In the patents at issue, these are different kinds of process steps in a certain sequence of a certain life to do something, and I don't -- some -- some go pretty far across the spectrum of steps that are in the whole factory.

Q. Sure.

A. Some are much shorter.

Q. Sure.

A. Does it really matter? Because we're going to be talking about patents, specific patents.

Q. I think it matters because at least in terms of some of the questions I've been asking, I think there was some lack of clarity with respect to what I was asking and what you were providing us answer. So I'd like to get to some sort of definition.

A. Okay. We can try.

MR. MUKERJI: Let's take a break.

MR. CHEN: Thanks.

(Recess - 10:09 a.m. - 10:22 a.m.)

MR. CHEN: Back on.

BY MR. CHEN:

Q. All right. Dr. Rubloff, let me see if I can get some clarity on the terms that we've been using.

When I say "unit process," what does that mean to you?

A. I think of a unit process as a single -- a single modification of a sample, a wafer, a device, caused by a physical or a chemical -- let's see. That's not broad enough, actually, because I don't know what to do with metrology. You know, you have to do measurements in between etch, deposition, and so on.

But, generally speaking, unit process to me connotes an etch, a single etch step, a single deposition step, carried out in a tool.

Now, when I use the word "step," I realize there's some ambiguity with that because on

most, if not all, tools -- let's take an etch step. What will happen is, you have to etch at some power. You have to get some gas flow and so on. And when you look at the -- it would be the computer screen these days, but really the recipe for that step, that process, that unit process, you will see sometimes 20 different substeps.

You have to turn it on. You have to turn on the heating power if you're going to have a heated substrate. You have to wait a certain amount of time, some seconds, until it reaches temperature. Then some valve will open and some power, RF power will turn on, something like that.

So I keep getting into this dilemma of steps, but to me a unit process is probably one tool that may do some substeps to accomplish something.

Q. So unit process -- so if I use "unit process" to refer to an etching step, including all the substeps, or a deposition step, including all the substeps, you would understand what I mean?

MR. MUKERJI: Objection to form.

THE WITNESS: Well, if we decide

to agree upon that terminology. But in asking questions about the issues at hand, I reserve the right to --

BY MR. CHEN:

Q. Sure. If you have any --

A. -- to make it --

Q. Yeah.

A. -- more specific because there are subtleties in these substeps. And another place where it gets more complicated is, what do you call a cluster tool? If you have a cluster tool, is that a unit process or not?

Q. Sure.

A. So I'll have to maintain some flexibility.

MR. MUKERJI: I just want to remind you guys not to talk over each for the court reporter's benefit.

MR. CHEN: That was my fault. I interrupted you.

BY MR. CHEN:

Q. But a unit process would include, for

example, etching and deposition; correct?

A. It depends on the definition. So there are plenty of cases. If I look at how, let's say, a deposition is done today, it's in a cluster tool usually. And there will be a preheat cycle carried out in one chamber and there may be the deposition step in another chamber and then there may be another step where there's annealing or even an etchback step in another chamber.

So do I call the cluster tool a unit process? I don't know. It's ambiguous.

Q. Do you -- do you use "unit process" to refer to all those different -- different processes within the cluster tool?

A. You mean to each of the processes?

Q. No, to all of them combined.

A. I don't really have a rule for that. I'm not sure. I don't think -- I don't know of a convention that's broadly accepted for this.

I could -- I could understand the argument that if we -- if we go through a cluster tool and it's going to do several steps, there's a

chamber here, a chamber here, a chamber here, it goes through these three in sequence, you might say this is a cluster tool that carries out three unit processes. Each of which may have substeps.

Q. Okay. But then you refer to them as three separate unit processes?

A. We could refer to them.

Q. You --

A. I mean, the best --

Q. You said this cluster tool carries out three unit processes.

A. It could. I said it could be viewed that way.

Q. Okay.

A. And as long as we describe what's happening, then -- then I think it's -- it's not difficult.

Q. Okay. So for today when we say "unit process" and we use it to refer to etching or deposition or lithography, that's a fair way to use the term; correct?

MR. MUKERJI: Objection to form.

THE WITNESS: It may be a convenient one, but you will hear me giving the details.

BY MR. CHEN:

Q. Sure.

A. Not -- not just using a convenient word -- term like that. Because I want to know what's happening to the sample.

Q. Okay. Previously you had given an example, maybe a more practical example, of when you your students, for example, graduate and they get their first job.

And so your students, I think, are Ph.D. students; right?

A. Not exclusively but --

Q. Okay.

A. -- most of them are.

Q. All right.

A. I have -- I have sometimes master's and undergraduate.

Q. So let's just take, for example, your Ph.D. student who graduates and then he gets his

first job, and you said typically they enter in as a process engineer represent -- responsible for a unit process.

A. Okay.

Q. What is that process engineer who just graduated responsible for?

MR. MUKERJI: Objection to form.

BY MR. CHEN:

Q. What are their job responsibilities?

A. I'm sorry. The siren is distracting me.

Q. Okay. The new graduate student with his Ph.D., he gets his first job as a process engineer.

What is -- what are his initial job responsibilities?

MR. MUKERJI: Same objection.

THE WITNESS: Well, it certainly depends on his employer and the job to which he's hired, but it could involve doing -- tracking what the performance of a tool is or that process is in terms of yield of that process, if there's a way

that's measuring that right after. It could involve planning a design of experiments to optimize that process. At the Ph.D. level, it may involve a little more insight into the process chemistry and some of the subtleties of the way the process works.

It would likely involve interaction with the characterization lab where they look at depth profiling through the thin film to see if it's uniform and the right composition and things like that. But it's hard to be specific because every job is going to be a little different.

BY MR. CHEN:

Q. And their initial work is going to be on a specific unit process?

MR. MUKERJI: Objection to form.

THE WITNESS: Not necessarily. I mean, it could be in characterization and whether we call that a unit process, I don't know.

BY MR. CHEN:

Q. Let me -- let me explain a little bit of what I'm trying to understand and then maybe that will help you.

I want to understand for two different types of processes, like, for example, a deposition step and then an etching step. All right. I want to know how to distinguish between these two different types of processes so when I use the term "process," you know, we know whether we're talking about just a deposition or just an etching and not the two combined.

Is there a way to use the word "process" to distinguish between these two different things?

A. You could say etch process, deposition process.

Q. Okay. And the etch process, is that a unit process?

MR. MUKERJI: Objection to form.

THE WITNESS: It can be considered a unit process, but that's just making another term for something that's less precise than to say "an etch process."

BY MR. CHEN:

Q. All right.

A. So, for example, I have a former student who went to Applied Materials and -- I'm sorry -- to Novellus, now Lam, and he's responsible for a PECVD process. They have a PECVD tool. He's responsible for refining, improving that tool and its performance in carrying out PECVD on something. I don't know what material.

Q. What was that example of?

A. Oh.

Q. I don't understand why you gave that example. What were you trying to demonstrate?

A. I was just trying to clarify that it's easier to say that he's working on an etch -- a PECVD process than to say he's working on a unit process.

Q. Is the PECVD --

A. I don't think he ever would tell me, oh, I'm working on a unit process. That's kind of a weird term. It's okay, but it's not very specific, and I can much more easily say it's a PECVD process.

Q. But is there a term that you can use to refer generally to all these different types of

processes like, for example, a PECVD process or a reactive-ion etching process or a lithography process --

A. I think unit process --

Q. -- at that level?

A. I think unit process is about as good a term as I can -- as I know, and it's used traditionally by the chemical engineers.

Q. So we'll use unit process, and if you think in a specific situation where we need clarification or you need to --

A. Uh-huh.

Q. -- add some detail, we'll clarify in detail. Fair?

A. Thank you.

Q. Okay. Now, who is responsible for integrating multiple unit processes together?

MR. MUKERJI: Objection to form.

THE WITNESS: I don't know how to predict the answer to that. I mean, it depends on the situation and what does it mean to have responsibility.

These days -- I think it's a little bit off topic, but these days people tend to train to work in teams and they actually work in teams. And so it's not as if -- it's not as if there's one person that you always know is responsible for that, that I can look at the org chart of Intel and I can say, ah, that person is responsible for developing the thin factory time.

Maybe -- maybe it happens that way. I don't know, but I don't -- I don't really know how -- I guess I should just say, I don't know the answer to that.

BY MR. CHEN:

Q. Okay. How many years of experience working in the industry would you need before you're capable of understanding how different unit processes interact with each other?

A. I think you have to be in the industry for a couple of years or something like that. That's why I defined it that way.

And the basis for that is my experience with my students who have gone off to Intel, Applied

Materials, IBM, and so on, and when I see them a year afterwards at a conference or something like that, they have learned so much because they're in an environment which sees every day the process integration consequences, not the whole factory flow, but process integration consequences of what they're doing on a unit process.

Q. Previously you had mentioned the fourth level manager.

A. Okay.

Q. Yeah.

A. I don't remember it.

Q. When you were describing the hierarchy before you mentioned your students who entered in who worked as a unit process -- on the unit process initially. Then you mentioned the next level up the ladder, which is integrating the unit processes, and then you mentioned top level, you mentioned a fourth level manager. I don't know if you remember that.

A. It was a figure of speech.

Q. Okay.

A. Saying somewhere in this there must

be -- I don't know -- fourth level, third level, fifth level. I don't know.

Q. Okay. I was just wondering what you meant by that fourth level manager.

A. Well, fourth doesn't mean anything, but if -- if a company is trying to develop a next generation technology, then there has to be a concerted program. So somewhere in that organization, they find a way to do that, and there are many ways in an organization to move strategically.

So in the old-fashioned days, you know, you think, well, that person I'm giving -- I'm the CEO. I give that person the assignment to make this happen. These days it's more complicated than that because you have integrated interdisciplinary teams that come together, and sometimes those teams are led by people at lower levels who have a special capability for doing that and sometimes there's some at a bunch of higher levels.

Q. But is that management level person who's responsible for the general goals of

semiconductor processing that we talked about before?

A. Well, somebody is responsible, but I think it's kind of above my pay grade to -- to answer that question.

Q. So somebody very senior then?

MR. MUKERJI: Objection to form.

THE WITNESS: Not necessarily. Some of the key efforts that I was exposed to in IBM -- well, there was one -- there was one case where I was put on a team because there was a yield failure in IBM manufacturing and so I represented -- I was the liaison from the research division.

And that -- what do we call it? -- task force was led by a second level manager in Fishkill, not a fourth level manager, and there were different kind of skills brought together. So sometimes it's somebody young and -- and bold.

BY MR. CHEN:

Q. Okay. I was -- the only reason I thought it was somebody senior was because you said it was above your pay grade, and I assumed that

you're fairly senior. So above your pay grade would be very senior.

A. No, no. I said that because I think we're getting into the business school management discussion, and I don't kind of know -- know how to deal with that.

Q. Okay. Before when you were talking about, you know, your experience with your graduate students and after they graduated and had gone into industry and they come back and you're impressed with how much they've learned, which time frame are we talking about?

A. Well, that's happened since I've been in academia. So that's 1993. I had students while I was at NC State who went to -- well, they all went to work for Intel or Novellus at the time, or nearly all. So certainly then.

And then also when I was at IBM, I had people who reported to me. So these weren't all Ph.D.s who took jobs in Fishkill or Burlington, and I think they reported a very similar kind of thing. You know, you get into a new environment where

there's this -- there's a larger goal of the factory and the technology, and they start sampling how things are related.

Q. When did your first graduate student graduate?

A. I don't know the answer to that. I had -- when I was at IBM, Iqbal Sharif worked in my group and he was --

Q. Ah --

A. I'm sorry.

Q. I'm sorry to interrupt you. You can finish your answer.

A. Oh, and so I guess he was kind of my first graduate student. But I don't remember if I was the formal co-advisor. He had a formal advisor and an RPI, but he worked for me at IBM full time, and so it may be that I was a co-advisor. I just don't remember. Other than that, it would have been 1994 or so.

Q. After you had entered academics?

A. Right. Right.

Q. Are you familiar with the term "process

flow" as it's used in semiconductor manufacturing?

A. Yes.

Q. What is your understanding of the term "process flow"?

A. So if I know that there are a set of unit processes that need to be carried out to make a certain device, a three-dimensional transistor or an interconnect or a contact or something, it may be a short process flow, it may be many steps.

Process flow means I do this first, then I do this, then I do this.

Q. So a process flow is a sequence of unit processes with a specific order; is that a fair characterization?

MR. MUKERJI: Objection to form.

THE WITNESS: It's something like that. Sometimes you can have variants of the process flow that get a similar result or even the same result. So the order may change, but more often than not, you know, we've been doing this. We've been making this in the FAB for the last two years and here's what the process flow is. And it's

written down in this SOPs, standard operating procedures, or more likely it's implemented in some major computer system what's really in the factory.

BY MR. CHEN:

Q. If you have one process flow and then you change the order of the various unit processes within that flow, haven't you then created a new process flow?

MR. MUKERJI: Objection to form.

THE WITNESS: Strictly speaking, I suppose it would be fair to say that, or you've revised the flow process, or you've chosen alternative process flow. But one way or another, if you write down the steps and here's the A process flow and here's the changed version of it, something will be different in the two columns.

MR. MUKERJI: Mr. Chen, I've got to ask. Are we now going to move into the specific declarations or are you characterizing this as background?

MR. CHEN: This is going to be still background asking about, yeah, general

background information about some of the processes.

MR. MUKERJI: No. You're asking about a patent.

MR. CHEN: Actually, I'm not. I'm asking about general semiconductor processes. I didn't bring up the issue of the order. It was in his question -- answer.

MR. MUKERJI: Your question was, if you have one process flow and then you change the order of the various unit processes within that flow, so I think you are bringing up the notion of order.

MR. CHEN: The reason was because in his previous answer to what -- with respect to what a process flow is, he brought up order. I'm just trying to clarify his answer.

MR. MUKERJI: I understand and, look, I'm not trying to -- you can ask him whatever questions you want.

MR. CHEN: Sure.

MR. MUKERJI: What I want is a clear record as to which declaration you're going to

use this cross-examination testimony for.

So going through his background, his experience, that's fine, but it seems to me that you're moving now to more substantive areas. So I ask that you tie it to a declaration.

MR. CHEN: This is all just background knowledge about semiconductor manufacturing in general.

MR. MUKERJI: Well, then, can I get your representation this is not going to be used to cross-examine with regard to a specific declaration? It can't -- it's got to be one way or the other; right?

MR. CHEN: No. All the background general stuff can be used for any of these declarations, and then when I introduce his declaration in the specific patents, then I will limit that to the specific IPR.

MR. MUKERJI: So you're not asking about --

MR. CHEN: Should we go off the record for a second?

MR. MUKERJI: Sure. We can go off.

(10:49 a.m.)

(Off the stenographic record)

(Witness stepped out).

(Witness returned).

(11:05 a.m.)

MR. MUKERJI: We can go back on the record, I think.

MR. CHEN: So --

MR. MUKERJI: You want to make a statement or shall I?

MR. CHEN: Yeah, I mean.

MR. MUKERJI: So we took a break.

THE WITNESS: Instruction for me or what?

MR. MUKERJI: Well, I don't know if it's an instruction for you, but we took a break and counsel for respondent or HSC's counsel and I had a discussion about how to conduct this deposition, this cross-examination.

There are four declarations at

issue the witness has provided. Counsel previously agreed for efficiency's sake that we would cover all four declarations during the cross-examination over the span of two days. That leads to a bit of a procedural quandary as to when a question is within or outside the scope of a particular declaration.

After conferring with counsel at the break, we think we have an agreement in place, and we're going to give it a try. And that is that counsel will ask background questions as he's been doing throughout the morning and the witness will respond. If the question is meant to be tied to a specific patent, counsel will make that clear.

HSC's counsel reserves his right to use the background material for cross-examination on any particular declaration. We reserve our right to object to such use, as we believe such use may be outside the scope of direct. So would be improper cross-examination unless the witness is aware that he's testifying about his declaration.

But, again, we are feeling our way through -- through the issue. So with that

understanding in place, we can continue the deposition.

I don't know if that helps.

THE WITNESS: It doesn't help me a lot.

MR. MUKERJI: For you it's easy. Just tell the truth.

THE WITNESS: Right.

BY MR. CHEN:

Q. So, Dr. Rubloff, right now I'm asking you general information about the field of semiconductor manufacturing. I just want to get your understanding of some of the different processes or terms that are used in that field.

Previously before we took a break, we were talking about semiconductor process flow.

How is the semiconductor process flow used in semiconductor manufacturing?

A. Well, the process flow is a description of what -- what unit process do you do or what -- or what batch or whatever process you do and what process you do next. Then if you're going to do

lithography, what batch you're going to use. If you're going to insert a characterization step to qualify, if you think that means you screwed up, you're going to do that and so on. So you basically need a recipe for manufacturing.

Q. Is each unit process within the process flow important?

MR. MUKERJI: Objection to form.

THE WITNESS: I don't have an answer for that. Because there are many steps there and some of them may be more important than others, more critical. And if you ask -- if you use a term like "important," then I want to know, well, what's the metric by which you measure importance?

BY MR. CHEN:

Q. Are any of the steps extraneous?

MR. MUKERJI: Objection to form.

THE WITNESS: I guess the right way to look at that is that if people had a consensus they were extraneous, they wouldn't be doing them. So at the time it's happening, it doesn't appear to be extraneous, but it may be

someone will come up with a better idea and improve the process flow and take out some steps or replace them with other steps. But nobody would leave something in, unless -- if they knew it was extraneous, unless -- well, let me qualify that.

I could imagine -- this is very hypothetical. I could imagine a condition where you have steps 1, 2, 3 and you don't -- you realize you don't really need step 2, but it does something unintended and when you take it out, everything falls apart. So 1, 2, 3 doesn't work.

So, for example, if there was a delay in the wafer sitting out in the clean room too long because you're doing a characterization step, and somehow sitting out in the clean room caused it to be oxidized further and you didn't know it, but that was important. So if you were doing something with that seemingly unneeded step that you didn't know about, then that would be a deviation.

I mean, normally you say, if I don't think I need it for anything, I'll just take it out, but there are unintended consequences

sometimes. So that would be the occasional exception, I guess.

I find the question is difficult to deal with without specifics.

BY MR. CHEN:

Q. In the hypothetical that you just gave, was that a real-world example that you encountered?

A. I have no idea. It was hypothetical.

Q. So somebody running a process flow, would that person ever just take out a step and not run it or add in a new step?

MR. MUKERJI: Objection to form.

THE WITNESS: They would not do that in a manufacturing line, but they may be experimenting with the process integration issues of the sequence of a subsequence of steps and want to do some experiments to see if they could get rid of this one or replace it or something, something like that. But that would be kind of an off-line experiment.

It can be carried out certainly in development environments, sometimes in manufacturing

even, but they know they're doing it and it doesn't go to the same place where the product records go typically.

BY MR. CHEN:

Q. So maybe as part of the development process to try to improve or modify the process flow?

A. Yes, but --

MR. MUKERJI: Objection to form.

THE WITNESS: -- you have to be careful not to compartmentalize development versus manufacturing. It's not a solid wall between them.

One of the surprises you learn in manufacturing is that people are retuning unit processes, sequences of processes, to try to get the yield up or some other benefit from that. So they may do experiments with dummy wafers or with -- with some kinds of test wafers or sometimes even product wafers to see if they can get the yield up.

BY MR. CHEN:

Q. How are steps differentiated from each other within a process flow?

A. I don't know what differentiated. I mean, you could name them. You could number them. You could write a SOP, a standard operating procedure. You could write a tool recipe.

I think we're kind of in a discussion here which faces the obstacle that by trying to be general about this, we miss what's really happening. People want to be precise and say, we do this and we do this and here's how we do that and then we do this.

Q. Just so I understand, when you said that people want to be precise and say, we do this and we do this and here's how we do that and then we do this, what are you referring to?

A. I was referring to the disadvantage of trying to put kind of global terms on this.

Q. Okay.

A. You asked me -- in reference to your previous question.

Q. I thought maybe you were referring to what a process flow was, which is, you know, do this and then you do this and then you do that.

That's not what you were referring to?
A. I've lost the argument.
Q. Okay.
A. I don't know where we were.
Q. All right.
A. Sorry. I've lost the thread of the discussion already because it's a little bit vague.
Q. No problem.
A. That's what I meant by "lost the argument."
Q. Are you familiar with the term "chemical vapor deposition"?
A. Yes.
Q. And can we refer to it as CVD?
A. Yes.
Q. And you've had experience with CVD in your prior work?
A. Yes.
Q. What is CVD?
A. CVD is a materials modification process which uses chemically reactive gases to form new kinds of materials that are reaction products of

those reactive gases on a surface, resulting in a thin film of material being deposited.

Q. It is -- is it a deposition technique?

A. Yes.

Q. Are you familiar with the term "physical vapor deposition"?

A. Yes.

Q. Can we refer to it as PVD?

A. Yes.

Q. And what is PVD?

A. PVD is a different type of deposition technique which does not involve chemical reactions to an appreciable extent in contrast to CVD. So examples would be evaporation and sputtering in particular, and the P stands for physical as opposed to chemical.

Q. In PVD, do you have a target that then you bombard with some ions and that causes material to fall down onto where you want to make your deposition? I'm trying to understand the PVD process.

A. You said in PVD?

Q. Yeah.

A. There is -- there are several different styles of PVD. One of them is called sputtering, and I think that's what your referring to and that does use ions to unmark the target.

Q. So sputtering is a specific form of PVD?

A. Yes. Evaporation would be another one.

Q. How does the evaporation work?

A. In evaporation, you heat a target material -- there are different ways to do that -- to a temperature such that the atoms of that material jump off the surface. They evaporate. Some of them have enough thermal energy that they can leap the surface. And when they do that, they have some velocity going someplace and so they end up on some other surface. One example being that we care about is your wafer.

Q. Thank you.

Are you familiar with the term "rate of deposition"?

A. Yes.

Q. What does rate of deposition mean?

A. Well, typically we think of rate of deposition in units of nanometers per second, or angstroms per minute, or a certain amount of the deposited material coming onto the surface per unit time.

Q. So for a certain time period, the rate of deposition will determine how much material is deposited?

A. You mean a constant rate of deposition?

Q. Yes.

A. So if you have a constant deposition rate, then that -- and do you know how long you're doing that, that tells you how much you have left deposited at the end when you stop.

Q. When you're depositing material by CVD process, is there a difference between the rate of deposition on horizontal surfaces and vertical surfaces?

A. Yes and no. Mostly no because chemical vapor deposition can -- and is chosen for this -- can achieve essentially the same deposition rate on

horizontal and vertical surfaces. We call that phenomenon conformality, high conformality, or group step coverage and so on.

On the other hand, it's not perfect and it can depend on at least two fundamental factors. One of them is the process chemistry you use. Because there are regimes of process chemistry that are rate limited by kinetics and that's where you can get good conformality, and there are other regimes that are rate limited by transport.

And in that case, it depends on the geometry and specifics of gas flow distributions and three dimensions in your reactor as those gases are approaching your wafer.

So the second thing besides the individual process chemistry that's important is, you have to know something about -- well, as part of that, you have to know something about what regime you're in, kinetic or transport-limited, and what details are there.

But the other thing is the equipment design. Because as you enter a regime, which is

affected at all by transport, then the gas flows of bringing these reactive species to the surface are -- can be quite complicated and that has led to the challenge of designing good CVD reactors that can deposit uniformly over large wafers and into complicated three-dimensional micro- or nano-geometries which are the patterns you're trying to make.

Q. When you said "step coverage," what does step coverage mean?

A. Well, step coverage is a kind of legacy term from an earlier era when people would evaporate or sputter over structures where you might have a raised region compared to a lower region, like a plateau, and you'd want to have the sidewall covered with, if you can, the same thickness as you have on the top and on the lower plat -- lower level.

And so that's called step coverage. And so you asked, okay, if it's -- if it's a thousand angstroms on the top and away from the step, what is it on the side of the step?

Q. So good conformality and good step

coverage mean the same thing?

A. It means similar things. In my view, we now have the requirement in a DRAM capacitor or a stack capacitor or shallow trench isolation, whatever it is, we have very high-aspect-ratio structures in the devices we're making.

That means we have narrow trenches, for example, that are very deep and so in those cases, you really wouldn't talk about that as step coverage so much as you would conformality. I think that the term "step coverage" is not as -- not as current but legitimate.

Q. So if I were to say something had 50% step coverage, for example, that would mean that the thickness of the deposition on the horizontal surface is -- sorry -- I mean on the --

A. On the vertical surface.

Q. Right.

If I were to say that something had 50% step coverage, that means the thickness of the deposition on the vertical surface is half as much as the thickness of a deposition on the horizontal

surface; is that correct?

A. Partly, although there are different ways you can define it. Because typically when you have the vertical surface being covered, it won't be uniform coverage from the top to the bottom. So you may get thicker deposition near the top of the vertical step, the side of the step, than at the bottom. So you really should prescribe how you're measuring step coverage.

Q. Okay. How is step coverage typically measured?

A. I think people use what they -- what they are comfortable with for communicating results to their collaborators, colleagues, and so on.

Q. Okay.

A. I mean, you know, you could pick a simple measure like, what's the average over the vertical surface?

Q. Okay.

A. Something like that.

Q. Is the thickness at the top of the step always thicker than the bottom of the step?

A. Usually, but I wouldn't say always because I haven't conjured up reactor designs and gas flow consequences, particularly in a transport-limited CVD regime. So there might be exceptions.

Q. But in your experience, you haven't seen any?

A. Not typically, no.

Q. And so if somebody told you this process has 50% step coverage, what would that mean to you?

A. I think the only thing I could conclude from that, because they didn't tell me how they measured step coverage, is that you can't count on the layer being deposited on the vertical or side surface looking just like the layer on the top.

Q. It would be thinner; right?

A. Probably thinner.

The only exception I can think of right now is, suppose it's really rough. Sometimes you deposited material and it's a thin film material which has a grain structure or it's

nucleation-controlled, like I told the story earlier about finding a way to make rough silicon surfaces, and so there are exceptions that can happen. Then I would know. That would be a difference.

Q. Are you familiar with the term "anisotropic etching"?

A. Yes.

Q. What is anisotropic etching?

A. Anisotropic etching refers to etch rates such that the etch rate on a horizontal surface is different from that on a vertical surface. It's kind of the dry etching analogy to the CVD conformality question.

Q. How is -- how is the etch rate on the horizontal surface different than the etch rate on the vertical surface in anisotropic etching?

A. I'm sorry. I don't know what you're looking for here when you say "how is it." You mean why does it happen?

Q. What is the difference?

You said that anisotropic etching refers to etch rates such that the etch rate on the

horizontal surface is different than that on the vertical surface.

What do you mean how -- that the etch rates are different?

A. They're different numbers. If one is etching at a rate of 50 and the other is at 12, they're different.

Q. Is the etch rate of the horizontal surface higher than the etch rate of the vertical surface?

A. If it's anisotropic etching, yes.

Q. Is anisotropic etching the same thing as dry etching?

A. Not necessarily.

Q. So dry etching -- sorry. Let me ask you this.

What is isotropic etching?

A. Isotropic etching is a condition in which the rate at which a surface is removed is the same on all surfaces. So horizontal or vertical, substantially the same.

Q. So dry etching can be either

anisotropic or isotropic?

A. Yes.

Q. How about wet etching?

A. What about it?

Q. I'm sorry.

Can wet etching -- well, let me just start over.

What is wet etching?

A. Wet etching is the use of liquid chemicals, such as acids, for example, to remove material from a surface.

Q. And is wet etching anisotropic or isotropic?

A. It can be either.

Q. Okay. And I don't remember if I asked you before.

What is dry etching?

A. Dry etching is removal of material using a vapor environment. So there's no liquid involved. Typically a plasma is involved so that you have plasma species available to do the etching.

Q. Are you familiar with lithography

techniques?

A. Yes.

Q. What is lithography?

A. The word "lithography" can be used in at least two different contexts. One is the exposure of patterns, the transfer of -- the exposure of patterns of light typically, but could be electron or ion beams, into material so as to modify that material, typically a mask, and then to use that mask for other things.

So that use of the term "lithography" and they -- the two meanings kind of merge together. Sorry, but that's how I see it.

So one way to talk about lithography is the exposure of a patterned beam using a mask or direct light of a particle to form patterns in a -- in a material, and so it has to do with optics or electrons or photons in patterns.

The broader meaning is doing lithography to be able to typically remove material in some regions and not in others. So that combines typically something like the exposure part -- that's

the first version of the word that I used -- with etching of some kind so that that pattern that was made is transferred into the thin film material.

And I think those -- those two somewhat different versions are really used interchangeably.

Q. So let me see if I understand what you're saying.

There are two definitions of lithography which have kind of maybe bled into each other a little bit.

One is using lithography to strictly refer to the formation of the patterned mask; whereas, the other term refers to both the formation of the patterned mask as well as the etching process that is used to transfer that pattern onto the material below?

A. Yeah, and the reason I make the distinction is -- I mean, I teach this stuff; right? I've got slides on this. Is that if you're talking about how you make patterns by using masks and magnifying, demagnifying, and so on, you're really talking about optics or electron -- photon optics or

electron optics, ion beam optics, and so you're talking about a tool.

And there's a whole world of capital equipment vendors that make that their specialty. They don't necessarily do the etching and they don't necessarily develop the photoresistor or the resist that's sensitive to that pattern.

Most generally if I say typical lithographic process, I will mean I had something on the surface, I took a mask, I transferred the light from that mask into a photoresist layer that I put down and treated appropriately and developed so it had openings and closed parts, and then I used that to -- as a mask for etching.

So in that sense, lith -- the exposure, the lighting, and the etching are all part of the word lithography.

Q. All right.

A. I'm sorry, but I don't know how not to be a little bit vague on it. And it's not vague, but I need to explain that people use the term in different ways.

Q. Okay. And how is the photoresist used in lithography?

A. In optical lithography?

Q. Let's use the lithography to refer to both the optical aspect as well as the subsequent etching in photoresist.

A. No, that's not what I was distinguishing.

So if I want to make a pattern, I can do it by shining light or not shining light --

Q. Oh.

A. -- at these locations.

Q. As opposed to ions?

A. As opposed to ions and electrons.

Q. Sorry. All right.

And the photoresist is used with the light?

A. Right. But even in electron or ion beam lithography, particularly electron beam, some people would just say "photoresist" because they're so used to it, but it's an electron beam resist.

Q. Okay.

A. Or, for that matter, X-ray resist.

Q. In semiconductor manufacturing, do they typically use light or the ion beam?

A. Rarely ion beam because it doesn't have a high throughput. Usually light and these days it's ultraviolet light. But there are important uses for electron beam lithography as well in manufacturing and that's particularly to make the mask for optical lithography.

Q. Okay. For now let's talk about light.

A. Okay.

Q. Okay. Because that's the more common --

A. Yeah.

Q. -- form.

How is the photoresist used in lithography using light?

A. Yeah. You can say pattern --

Q. Okay.

A. -- so it's simple.

If I have a layer of material and I want to remove it from one region and leave it in

another, I put on a layer of photoresist, which is typically a polymer that is sensitive to light. So I make this -- this cover. I then take a mask, an optical mask, shine light through it, and image it one way or another on the photoresist. So the light hits this part of the photoresist, let's say the A part of the photoresist, but doesn't hit the B part of the photoresist.

The light causes photochemical changes in the resist and can transform that resist from being soluble to insoluble in the right chemical or insoluble to soluble. So it modifies the photoresist. That's why we call it photoresist.

And then you can remove one part or the other in a process that's called develop, where you basically dissolve one piece or the other. I'll hesitate to go into positive and negative photoresist and so on.

So that means that you now have the photoresist in one -- in one place A but not in B, and so if I have the photoresist on A on my material and I put it in an etching solution or a dry etching

environment, the mask is protecting the A region. So it won't -- the material under it won't be removed, but where the mask isn't present, the material will be removed.

Q. So the remaining portion of the photoresist acts as a mask?

A. Yes, and then, of course, you remove it at the end.

Q. When you say "remove it at the end," you mean remove it at the completion of the etching process?

A. Typically that's when you'd remove it, but not necessarily then. It depends what your next step is.

Q. Why do you -- how do you remove a photoresist?

A. Typically you dissolve it in liquid chemicals, but you could move it by dry processes as well. For example, by ashing.

Q. Why is it necessary to remove the photoresist?

A. The photoresist is just there to help

you do the patterning or to do lithography at that point. Now, I should be careful because there are exceptions.

So there are devices that use a photoresist called SU8, which can actually be used to make devices for microfluidics, for example. So sometimes you're going to continue to use it even as the device is completely finished, but in semiconductors typically you will remove it either after you've done one etching step with the mask, the photoresist mask in place or at some later time.

Q. When you are depositing the photoresist, does the surface that you're depositing it on have to be flat?

A. When you're depositing the photoresist? No, it does not have to be flat. I don't know how flat you mean, but if it had to be really flat, you wouldn't have a very good strategy for using lithography as a patterning technique to make three-dimensional devices.

Q. Okay.

A. But there is some tolerance too. There

are -- there are situations where you would have trouble making the profile of photoresist thickness versus position over underlying topography that's too demanding.

Q. You said if it had to be really flat, you wouldn't have a good strategy for using lithography as a patterning technique.

I'm sorry. I don't really understand.

A. So when we make devices, they're three-dimensional.

Q. Right.

A. They're also usually not very interesting usually; right? So if you make -- suppose you make a gate electrode.

Q. Right.

A. You know what a gate electrode is?

Q. Yeah.

A. And after that, you're going to have to make some other structures; right? Because a gate electrode in isolation doesn't do anything. You have to make contacts, the source/drain, and stuff. Those are going to be somewhere by lithography as a

pattern strategy, exposure and etch.

So if you couldn't put down a photoresist layer and use optical lithography, how would you make the rest of the device?

So lithography and photoresist have to be reasonably compatible with having a three-dimensional topography at some level underneath.

Q. So you can deposit a photoresist on a three-dimensional surface with topography?

A. Yeah, within limits.

Q. Okay. Are you familiar with chemical mechanical polishing?

A. Yes.

Q. And we can refer to chemical mechanical polishing as CMP; right?

A. Yes.

Q. Okay. And what is CMP?

A. CMP is a planarization technique. So as you make these layers --

Q. Right.

A. -- in three dimensions, the tendency is

for the topography of the surface to get more and more structure, higher aspect ratios and the like, and so sometimes you will want to planarize that surface. CMP was developed to deal with this problem in the interconnect domain.

It was actually done at IBM while I was there, and we weren't allowed to talk about it. But that was when people were trying to figure out, as you make a wire here, then a wire above it, then a wire above it, pretty soon you have a very rough surface. And so how are you going to do lithography on that? How are you going to make anything on that? It's too difficult.

So people developed strategies for planarization, and CMP was pivotal with that. It's one of the techniques, but it's probably the most advanced technique for doing a good job of planarization.

Q. You said you have a very rough surface, and how are you going to do lithography on that?

A. For example.

Q. Right. So CMP is used to planarize a

surface so that you can do lithography?

A. And -- and you can make reliable structures. So these days there are -- I don't know -- eight levels of interconnection wiring on a chip. And what's done now in the -- in the current generation of technology -- and CMP was part of developing that capability -- is at each level, you'll planarize the surface and then build another layer of wires that come up through an insulator and then do something in a horizontal direction, but it's planar.

Q. And are you using the CMP to planarize the -- the photoresist?

A. No. No. To planarize the materials that have been deposited.

Q. Okay. So you're using it to planarize the material upon which you would deposit the photoresist?

A. Or upon which you will deposit some other material.

Q. Okay. Would you ever use CMP to planarize the material that had a photoresist on top

of it?

MR. MUKERJI: Objection to form.

THE WITNESS: I don't understand the question. You don't -- I don't know of anyone and any attempts to use CMP on photoresist.

BY MR. CHEN:

Q. What are some other planarization techniques?

A. Well, another one is called etchback, which is a kind of ion beam plasma, and that was the standard before CMP was developed.

Q. Oh, okay. How does etchback work?

A. Etchback uses typically ions like you would use in sputtering to move material as uniformly as possible and be -- what it basically does, it homogenizes the surface. So if you've got a big bump someplace here, that will etch faster, be removed faster. So it does some planarization.

Q. Do you use a mask with etchback technique?

A. Well, people use masks for things like collimated sputtering, but I don't know of any

examples with etchback. That doesn't mean there aren't any. I just haven't seen it.

Q. I just have a few more of these background type of questions, probably take another 15 to 20 minutes, but I don't know how hungry you guys are, whether you want to stop.

MR. MUKERJI: Would you like to?

THE WITNESS: I'm all right.

MR. MUKERJI: Are you okay?

THE WITNESS: Yes.

MR. MUKERJI: So what I'd suggest is, why don't we do the 15 to 20 minutes questions and then take our lunch break.

MR. CHEN: Sure. That sounds good.

BY MR. CHEN:

Q. Are you familiar with the term "dielectric layer"?

A. Yes.

Q. Is it the same as an insulation layer?

A. The two terms are used pretty much interchangeably, but I'm not sure that that's a

universal valid way of looking -- to look at it. I'd have to think about whether there's some exceptions.

Q. What are some common materials used to form a dielectric layer or insulation layer?

A. In the sense?

MR. MUKERJI: Objection.

BY MR. CHEN:

Q. Actually, let me go back.

So for you, dielectric layer and insulation layer can be used interchangeably, but you're not sure whether that is universal?

A. Well, okay. So dielectrics should have a bandgap and be insulating, but they aren't always.

Q. Okay.

A. So with aluminum oxide I can tell you, it is metallic. So there are exceptions to this, but in the field of semiconductor electronics where the number of materials that are insulators or dielectrics, generally speaking, people casually use them, the terms interchangeably.

Q. Okay. Dielectric is more of a

characteristic of a material, whereas, insulation -- insulating might be more of a functional term; is that fair?

A. I haven't thought about this distinction.

Q. Okay. What is insulation layer?

A. Insulation layer to me means that if you have a voltage across that material, there can be a current passing through it. However, it's more complicated than that because most materials have leakage currents or means by which there can be a tiny current, and so we talk about what's the leakage current in this material under certain voltage conditions. Also, what's the breakdown field?

Because if you press high enough of voltage over a thin enough material, you can change the material, actually, and make it into a kind of conductor.

Q. Let's say I had a layer that was made of silicon oxide. Would that be an insulation layer?

A. Typically it should be, if the quality of the material is good and you're not stretching it to very high electric field strengths and if it's not too leaky.

For example, people used to do what's called sputtered quartz, which is you take a target for sputtering that's made of silicon dioxide and you sputter it onto your -- your wafer, and it makes rather inferior material compared to other -- other ways. So.

Q. What if I had a layer of silicon nitride? Would that be -- also be an insulation layer?

A. Yes, if it's decent quality material. Silicon oxide, silicon dioxide, silicon nitride are typically regarded as insulators, and people usually use them as insulators. I guess the caveat that you hear me making is, you can take a good material and mess it up.

Q. Okay. Are silicon nitride and silicon oxide largely interchangeable?

MR. MUKERJI: Objection to form.

THE WITNESS: For what metric do you have in mind?

BY MR. CHEN:

Q. In terms of their use as an insulating material.

A. Well, it depends -- it still depends on what you mean. If you want them to -- to just be insulators, well, they'll have different properties as insulators, different breakdown fields, different leakage currents. Even -- even silicon dioxide made by different techniques will have different properties. So you can't say they're really interchangeable from an electrical point of view.

And then when you recognize that you're going to have to do some kind of thin film deposition, all these things we do in semiconductor manufacturing, the properties of those materials can be very different in those processes.

Q. Okay. Are they formed differently?

A. Yes, typically. I mean, they have different atoms, so they certainly have to be made differently.

Q. All right. I meant like, are different deposition techniques used to deposit silicon nitride as opposed to silicon oxide?

A. Well, for both of them, there are a range of ways to do them. CVD processes, different precursors or reactants present in the CVD process. Growth of silicon dioxide from oxygen or water or N2O, nitrous oxide. There are many ways to make these, and the properties depend on how they're made.

Q. Are you familiar with the term "spacer"?

A. Yes.

Q. Okay. What is a spacer?

A. I think this gets into the domain of -- of how is it construed, and I think that could be different depending on the application you're talking about, and I think it also has to do with which patent we're talking about.

I don't think it's very helpful if I make up some kind of answer to that that's so generic that we don't know what it means.

Q. Is there a generally understood definition of spacer in the field of semiconductor manufacturing?

A. Generally understood? I'm not sure how specific it would be, and I certainly understand that there are different properties that one might want from a spacer. For example, I don't want alkali ions to be able to get through it or I don't want electrons to get through it.

A spacer is, you know, the common meaning -- the common thought one has from the word is something is kept a distance from something else. I can't be more specific than that. We really have to talk about an application.

Q. What are some of the functions of a spacer?

MR. MUKERJI: Objection to form.

THE WITNESS: I can't answer that without being specific about device structure, application or patent. That's far too general.

BY MR. CHEN:

Q. To you spacer doesn't have -- so, for

example, in the field of semiconductor manufacturing, if somebody used the term "spacer," you wouldn't know what they meant unless they referred to a specific patent?

MR. MUKERJI: Objection to form.

THE WITNESS: Of course I'd know what they meant if they asked the question in the context of a device structure or a patent or a process flow and device integration.

BY MR. CHEN:

Q. Okay. How about a spacer formed on the sidewall of a gate electrode?

MR. MUKERJI: Objection to form.

BY MR. CHEN:

Q. What are the functions of a spacer formed on the sidewall of a gate electrode?

A. I think that's too general a question. For example, it doesn't occur in main line silicon technology, but there's something called an ISFET, an ion-selective field-effect transistor, and the function of that, of anything that you might consider a spacer there might be very different from

that in a CMOS device.

You're asking a question which isn't specific enough for me to answer.

Q. So --

A. I'll be able to answer it when we get to the patents.

Q. Sure. I just want to understand what the roadblock is here.

You're saying a spacer has different definitions depending on context; is that what you're saying?

A. No. I'm saying that -- I'm saying that unless I understand an environment where the question is being asked, I don't know how to think about what properties it should have, which is, I think, the question you asked initially.

Q. Well, I'm asking generally what a spacer -- the definition of a spacer is in the field of semiconductor manufacturing and what type of functions a spacer might have.

You said that you needed specific, you know, application or a specific patent to be able to

answer that question.

I just want to understand whether you're saying that the reason you can't answer my question is because spacers have different definitions depending on the context.

MR. MUKERJI: Objection to form.

THE WITNESS: I don't think I can be helpful with this question. It's -- it's still too vague for me.

BY MR. CHEN:

Q. Okay.

A. Now, I already said that it could be something with regard to ion transport. It could be something with regard to electrical leakage current. It could be something to make sure that the field isn't too high. I don't know. I haven't thought hard about all the dimensions, but there are a lot.

But I certainly know what a spacer is in the context of a specific device application.

Q. So there's no one definition of spacer that can apply to multiple device applications; is that correct?

A. I don't know.

MR. MUKERJI: Objection to form.

THE WITNESS: I don't know. I haven't thought about it that way. That's too general.

I was asked to address specific patents and to -- and to make comparisons between prior art and patents at issue here, and that doesn't include my kind of dreaming up a generalization that should be applicable across a field as broad as semiconductor devices.

BY MR. CHEN:

Q. Yeah. Nobody is asking you to dream up a definition.

I'm just asking whether you're familiar with a definition of spacer as it's generally used in the field of semiconductor manufacturing.

A. Yes.

Q. And what is that definition?

A. It's a -- if there's a general way to do that, I'm trying to represent something general here, it has some function in ensuring that there's

a spatial separation between something and something else for properties which at this -- at this point in the discussion we're not specifying.

Q. Are you familiar with the term "isolation region"?

A. Yes.

Q. What is an isolation region?

A. Typically that term refers to the fact that if I want an active device, like a transistor, to operate correctly and I have more than one such on the surface, I don't want them connected to each other because then I can't wire circuits to use those various transistors. So I need some electrical isolation between them.

Q. Is STI a form of isolation region?

A. What do you mean by "STI"?

Q. Shallow trench isolation.

A. Yes, it is.

Q. Is field oxide a form of isolation region?

A. Yes.

Q. Are you familiar with the term "barrier

layer"?

A. Barrier layer?

Q. Uh-huh.

A. Yes.

Q. What is a barrier layer?

A. A barrier layer is a barrier to something moving, but I have to know the application to be able to say what that is.

Q. Okay.

A. It could be a barrier to transport a species. It could be a barrier to chemical reactivity. It's a lot.

Q. So the definition of barrier layer that you gave as a barrier to something moving, that's a more general high level definition; correct?

A. Compared to what?

Q. Compared to a definition that you might give which is more specific within a particular context.

MR. MUKERJI: Objection to form.

BY MR. CHEN:

Q. I just want to understand your answer

and kind of the difficulty in giving a more specific definition.

You said that:

A barrier layer is a barrier to something moving, but I have to know the application to be able to say what that is.

A. Well, let me give you an example. If I have a metal and then a layer of high quality insulator and then some other metal, and these two aren't shorted together and they don't leak very much, I could call that layer an insulating barrier for electron transport.

Q. Right.

A. Right? If I have dopants in silicon and I don't want them to leave the silicon, I could put a nitride layer or something there and then I have oxide or something above that, and that might serve -- I'm not sure, I haven't thought through that example -- that might serve to prevent diffusion of atoms or ions to it.

So that's a diffusion barrier and both are well known, but they're completely different.

Q. Right. Okay. So generally a barrier layer is a barrier to something moving, but depending on the application, there may be a more specific definition for barrier layer depending on its purpose such as a diffusion barrier?

A. Well, I think the way you've phrased it is too specific.

Q. Okay.

A. Because it doesn't include a chemical reaction barrier.

So if I have metal -- transition metal connected to silicon, it may -- it is likely to react at the interface and form a new material, a silicide. So if I don't want that to happen, then I need some kind of barrier layer to prevent it.

But I don't think characterizing that as a reaction -- what should I call it? -- chemical reaction barrier is encompassed in what you said about something moving.

Q. Okay.

A. Because nothing is moving from one side to the other if there's a chemical reaction.

Q. Okay. I was just using the definition that you gave.

A. I understand that.

Q. So is it fair to say that barrier layer is a term that, depending on its application or context, could have different meanings?

MR. MUKERJI: Objection to form.

THE WITNESS: Can have different functions.

BY MR. CHEN:

Q. Dr. Rubloff --

MR. MUKERJI: Mr. Chen, we're -- I'm sorry. We're past the 20-minute.

MR. CHEN: Sure. Just one more.

MR. MUKERJI: Do you have much more?

MR. CHEN: No, I have just a few more.

BY MR. CHEN:

Q. Is it also fair to say then that "spacer" is a term that, depending on its application or context, could have different

meanings?

MR. MUKERJI: Objection to form.

THE WITNESS: Could have different functions.

BY MR. CHEN:

Q. What is the distinction you're drawing between function and meaning?

A. I don't know what "meaning" means.

MR. CHEN: Okay. Why don't we break for lunch.

(Whereupon, at 12:15 p.m., a luncheon recess was taken.)

AFTERNOON SESSION

(1:09 p.m.)

GARY W. RUBLOFF, PHD

called for continued examination and, having been previously duly sworn, was examined and testified further as follows:

EXAMINATION (CONTINUED)

BY MR. CHEN:

Q. Welcome back, Dr. Rubloff.

THE REPORTER: Exhibit 2.

(Document marked, for identification purposes, as Rubloff Exhibit No. 2.)

MR. CHEN: We can mark his errata as Exhibit 3.

(Document marked, for identification purposes, as Rubloff Exhibit No. 3.)

MR. MUKERJI: This is 2?

MR. CHEN: Yeah.

MR. MUKERJI: And the errata is 3?

MR. CHEN: Right.

BY MR. CHEN:

Q. Dr. Rubloff, I've asked the court

reporter to mark as Exhibit No. 2 your declaration submitted in connection with Samsung's IPR of the '997 patent.

I've also asked the court reporter to mark as Exhibit No. 3 the errata to this declaration that you provided earlier this morning.

Just take a few quick moments to look over these documents.

A. (Reviewing document).

Q. Okay. Dr. Rubloff, is Exhibit No. 2 your declaration submitted in connection with the IPR of the '997 patent?

A. Yes.

Q. And Exhibit 3 is your errata to that declaration; correct?

A. Yeah.

Q. Does this declaration and the errata contain any and all relevant opinions you have regarding issues related to Samsung's petition for review of the '997 patent?

MR. MUKERJI: Objection to form.

THE WITNESS: Well, this looks

like my complete declaration, but I haven't read the petition that they made.

That's a different document; right?

I've looked -- I've looked at it, but I haven't studied.

BY MR. CHEN:

Q. You understand that you submitted your declaration to support Samsung's petition?

A. Yes, I understand that.

Q. All right. Do you have any opinions regarding issues relevant to Samsung's petition for review of the '997 patent that were not included in your declaration or your errata?

MR. MUKERJI: Objection to form.

THE WITNESS: The first part of that was? I'm sorry.

BY MR. CHEN:

Q. Do you have any opinions regarding issues relevant to Samsung's IPR of the '997 patent that were not included in your declaration or the errata?

MR. MUKERJI: Same objection.

THE WITNESS: Well, since I haven't paid attention to the petition that they submitted to the IPR board, I don't really know the answer to that.

But my -- my review is here in my declaration, and it covers all the conclusions that I drew.

BY MR. CHEN:

Q. Okay. So you don't have any other opinions related to the validity of the '997 patent that were not included in your declaration; correct?

A. I think I've got most of them right but, you know, that I've included everything that I intended to include. It may be there's something that will come up in discussion. I don't know.

Q. Sitting here today, you're not aware of any other opinions related to --

A. Oh.

Q. -- the '997 patent --

A. No.

Q. -- that you failed to include in your

errata --

A. No. No, I don't know of any I failed to include.

Q. -- or your declaration?

Okay. Other than the issues discussed in your errata, are you aware of any other errors or omissions in your declaration?

A. I don't think so.

Q. So your declaration and your errata contain a complete recitation of all the opinions that you have regarding the validity of the '997 patent; correct?

MR. MUKERJI: Objection to form.

THE WITNESS: Well, with the proviso that this is a summary of those. There certainly are more elucidation of detail to come from, but this is a good summary that I'm comfortable with of my opinions about the '997 validity.

BY MR. CHEN:

Q. Why didn't you include the additional detail when you were preparing your original

declaration?

A. It's not that I didn't include the additional. There's no substantial detail that I feel is necessary here to address the questions I was asked to look at, which is compare certain prior art references to the claims of the '997 and see if that prior art matches onto the claims of the '997.

So I think I've done an adequate job of that, but there's always more elucidation that could -- could be brought in, and I could make it 250 pages long. I don't think it's very useful.

Q. So you included all the relevant details; correct?

A. Well, depends what "relevant" means. The essential details maybe.

Q. Okay. You included all the essential details?

A. That's probably a fair statement.

MR. CHEN: Exhibit 4.

(Document marked, for identification purposes, as Rubloff Exhibit No. 4.)

BY MR. CHEN:

Q. So, Dr. Rubloff, I asked the court reporter to mark as Exhibit No. 4 a patent titled "Method For Forming Self-Aligned Contact Hole," which is the '997 patent.

If you can just take a quick moment to look over the document.

A. (Reviewing document).

Q. So as I ask you questions about your declaration, if you need to refer to the patent, you have it. If you need other documents, let me know, and we'll introduce them into the record so you can reference them.

Did you read the '997 patent?

A. Yes.

Q. When did you first read the '997 patent?

A. I guess it was at least six months ago.

Q. Is that when you were first engaged to work on the IPR directed at the '997 patent?

A. Yes.

Q. And you understand the contents of the '997 patent; correct?

A. Yes.

Q. Looking at Exhibit 2, which is your declaration, if you could go to paragraph 11, which is on page 8 of Exhibit 2.

A. Uh-huh.

Q. How did you arrive at your definition of a person of ordinary skill in the art?

A. Well, I think I said something about that earlier.

When I look at this patent, it involves process integration understanding, and I believe that a master's level training in the disciplines that I list here is pretty typical for people who work in this industry and would give them some idea about unit processes and maybe the relationship between them, but typically not so much insight into process integration.

So I included the two to three years of experience as what I see students developing in their first job in this industry that would be necessary to -- to really have the skill to deal with the process integration questions that are in

the '997 because the '997 deals with the sequence of steps and the structural consequences of that.

Q. Does the sequence of steps affect the structure that would form through the manufacturing process?

A. Do you mean the order in which one does it, or what the composition of the sequence is? What processes are in? What processes are out?

Q. Let's start with the order. Does the order of steps affect the structure that you are forming with the process?

A. It can.

Q. But not always?

A. Usually it would, but I don't like saying "always" unless I've thought really quite hard about the exceptions.

Q. I see. But in your experience, it usually does?

A. Yeah.

Q. And then the composition of the sequence will also affect the structure that is formed by the process as well; correct?

A. Yes. The elements that are -- if you mean composition, the elements that are in it, yes. And -- and the mask designs. Very important.

Q. Is there a difference between somebody with a master's degree in the relevant field and two to three years of experience in semiconductor processing with somebody who has a Ph.D. but no experience in industry?

A. Yes, I think so.

Q. The person with a Ph.D. and no experience would not be considered a person of ordinary skill in the art for the purposes of the '997 patent; correct?

A. No, I don't think they would be.

Q. Because they don't have the relevant industry experience to understand the integration aspects; is that --

A. I think primarily that, yes.

Q. So is it fair to say that it doesn't really matter what level of degree the person of ordinary skill in the art obtains, the important aspect is the two to three years of industry

experience?

MR. MUKERJI: Objection to form.

THE WITNESS: I think that's an overstatement. It's important to get a view of process integration somewhere. I'd like to think that my own students get it from me, but that's kind of a small sampling.

The -- I lost my train of thought. I'm sorry.

Oh. Your question was, is the industry experience what's really important here?

I would be reluctant to say that something less than a master's degree, a bachelor's degree, would be satisfactory because I teach undergraduates --

BY MR. CHEN:

Q. Sure.

A. -- junior level and some senior level. And I think the depth of their understanding of the process equipment and chemistry and vacuum technology and all that is rather shy, even if they've been in the semiconductor processing

industry for a couple of years.

By the same token, the Ph.D. will probably have that in good order and -- but I wouldn't say that a Ph.D. is required for this. So I think master's is the right, let me say, average educational level.

Q. Is a person who has a master's degree and two to three years of experience in semiconductor processing have the capability of modifying the process to add new or different steps?

A. Yes, usually. These people would be charged with doing design of experiments to optimize the performance of a particular process, to compare that to related processes and the process sequence, and start to actually work on understanding how those things fit together. So they're on their way to becoming process integration engineers.

Q. What do you mean "they're on their way to becoming process integration engineers"?

A. From most universities, if you get a master's degree, something will be missing. Typically it's process integration perspective. On

the other hand, for somebody in electrical engineering, it may not be that so much, but then the familiarity with equipment and materials and the way the process chemistry works is usually a little shortchanged. At least that's my -- that's my observation with all the students. I have -- I'm exposed to students in all of these disciplines.

Q. When you said two to three years of experience in the semiconductor processing industry, is there a specific part of semiconductor processing that they need to have experience in?

A. Something involving multiple steps to make a device. That's where the process integration expertise is developed.

If they were doing, let's say -- I don't know -- a single layer optical coating with a CVD tool --

Q. Right.

A. -- to put on car windows, that wouldn't teach process integration.

Q. So beginning at paragraph 15, you provide a brief overview of the '997 patent?

A. Uh-huh.

Q. On paragraph 19, you talk about the benefits of forming a thermal oxide layer after the formulation of a gate electrode.

You say that one of the benefits is to reduce the defect density?

A. Paragraph 19 on page 12 you mean?

Q. Yes. It begins on page 11 and continues onto page 12.

A. Uh-huh.

Q. How does thermal -- how does forming a thermal oxide reduce the defect density?

A. Well, as I said -- noted here, there are a number of reasons.

So, for example, you've made a layer structure, used lithography, and anisotropic etching to define the gate electrode. Okay. So when that happens, there are residues of the -- of the anisotropic plasma etching process that are left on the surface typically.

Thermal oxidation is one way to clean that up because things like carbon will be

volatilized and leave the surface because you make CO2 and maybe CO, things like that. So chemically it's an effective way to do that.

It may also yield any internal -- I'm not sure about this, but could conceivably influence the grain structure where the damage of vector ion etching had been at the surface by oxidizing just a little bit into the polysilicon. I'm not sure if that -- if that really happens, but there are a number of things that you might anticipate.

Q. Okay. So the primary effect of the thermal oxidation is a cleaning effect?

A. Well, it's certainly one of them, yes.

Q. Is there any benefit to the actual oxide layer that gets formed?

A. Benefit of the oxide layer or to the oxide layer?

Q. Of the -- well, when you perform thermal oxidation, don't you form an oxide layer?

A. Yes.

Q. Is there any specific benefit of the actual oxide layer that is formed?

A. You mean in the quality of the oxide layer? Or do you mean in having an oxide layer?

Q. In having the oxide layer.

A. Yes, there can be. It can serve as a protection layer because it's mask -- essentially masking the sidewall for chemical reaction, electrical transport, various things.

Q. But that benefit is not related to the reducing defect density?

A. Yes, they all could affect defect density.

Q. Okay. How does having the oxide layer reduce defect density?

A. Well, I think there are a number of ways that could happen. There's references to literature which shows that.

One way, for example, is it might affect the stress distribution at the corner of the gate electrode and the rapid thermal oxidation sidewall. I think that's the one I would -- I would highlight as an example.

Q. When you say "defect density," what

does that mean?

A. Well, okay. So let me -- let me add to that that at that corner -- so -- so the heart of these devices is the gate oxide, and the gate oxide was grown on a very smooth silicon surface, and then a polysilicon layer was applied by CVD on top of it.

So the gate oxide, which is the highest quality insulator we know, is fine at that point, until we make the gate electrode. The etching of the gate electrode is likely to damage the gate oxide right at the edge.

If one does this sidewall oxidation, one of the benefits could be -- I think is, but I haven't looked at this literature closely -- to heal some of the damage in the gate oxide at the periphery.

When you look at defects in these structures, one of the central features is to know, is this something characteristic of right in the middle of the gate electrode in the gate oxide or just following the periphery? And you can discern the difference between those by changing

perimeter-to-area ratios. That's how it's standardly done.

So I think that would be -- I think that's probably the thing that was targeted in the reference. I think I included a reference here.

Oh, I don't understand EX1009 page 3. I don't remember where that is.

Q. That's different.

A. That's one of the exhibits?

Q. Yeah, that's one of the exhibits.

A. I don't have the exhibits here.

Q. Yeah.

MR. CHEN: Exhibit 5.

(Document marked, for identification purposes, as Rubloff Exhibit No. 5.)

THE WITNESS: Thank you.

Oh, yeah. Right.

BY MR. CHEN:

Q. So I've asked the court reporter to introduce as Exhibit 5 a document titled "Process Induced Degradation of Thin Oxides."

You've referred to this as the Wong

reference in the IPR and your declaration?

A. Yeah. So this work, this is a technology group that I know, and it says here in the abstract:

"Polysilicon sidewall oxidation is also necessary to protect the thin oxide from degradation by source/drain ion implantation."

But before that it says:

"RIE to define polysilicon gate structure degrades the quality of thin oxide; nevertheless these defects can be substantially reduced by subsequent sidewall oxidation of polysilicon."

So the way they would measure defect density, I believe, would be to make a bunch of these devices and see what their performance characteristic is and see what the outlier tail of the distribution of performance looks like, and that's the basis on which they make that kind of statement.

Q. Does the defect -- do the defects occur to the gate oxide when the gate oxide is etched?

A. Yes.

Q. All right.

A. When the gate? When the reactive-ion etching to define the gate electrode reaches the level of the gate oxide. So right at that periphery, something bad is going to happen.

Q. Okay. But the gate oxide itself isn't necessarily etched?

A. No. No. Just the edge.

Oh, you mean do you etch all the way through the gate?

Q. Right.

A. It's pretty hard to stop on the gate oxide.

Q. Okay.

A. I mean, it's possible but, remember, that's the thinnest layer in any of these.

And -- and you have to -- you have to -- the etching has to reach the gate oxide.

Q. Right.

A. Because otherwise you've got still a remaining layer of polysilicon from this device to

another one.

Q. Okay.

A. And they're shorted.

Q. Right. So the damage occurs to the gate oxide as long as the etching reaches the gate oxide; right?

A. Right, but it has to reach the gate oxide.

Q. I'm moving to paragraph 27 and 28 of your declaration.

A. Uh-huh.

Q. So here you're talking about how the term "forming an oxide layer over the diffusion region" is construed in the context of the '997 patent.

I want to ask you: What is your understanding of the meaning of the word "over"?

A. So in the context of the semiconductor world that we're talking about, over usually means above but not necessarily in contact with.

Q. Okay.

A. Because if you think about nitride CVD

that we're talking about as an etch top layer, it has to go over topography. It would be very inconvenient if our terminology required everything to be in contact.

And then just the plain meaning of that. So the airplane is above the earth. So something like that.

Q. Does "over" include being in the same or overlapping vertical space?

A. Oh, you mean if I -- let me make sure I understand what the question is.

A piece here is over -- maybe you can say it.

Q. Sure. So --

A. I think I know what you're getting at.

Q. Maybe it will be easier if we use coordinates.

A. Okay.

Q. Like X coordinate being along --

A. Okay. Good.

Q. -- you know, be the typical X direction horizontal direction. A Y coordinate being a

vertical direction; right?

Does the term "over" mean that you're higher in the Y direction as well as being overlapping to some extent in the X direction?

A. Overlapping?

Q. I'm not sure if that's the right word.

If you have an object, right, and you -- when I say "vertical space," I mean the area above that object moving up at a 90-degree angle from the edges of an object.

A. Uh-huh.

Q. If another object is not within that vertical space, is that object still over the previous object?

MR. MUKERJI: Objection to form.

THE WITNESS: I find it difficult to answer that question without a kind of application to look at.

BY MR. CHEN:

Q. Okay.

A. Like if you want to -- would you mean some point of this part of the device structure, is

that over some point that's below it?

Q. Sure. Why don't we look at Figure 2B, which is --

A. Uh-huh.

Q. -- in your declaration right above paragraph 27.

You see that between the two gate electrodes there's a space; right?

A. Uh-huh.

Q. Is that -- if I had something that was within that space, would that be over the gate electrode?

A. Oh. So something between the two gate electrodes, can that be over a gate electrode? Is that your question?

Q. Yeah.

A. I wouldn't think so, except that the context of the description technically sometimes changes what the meaning is. So it's a little hard to make a blanket statement about that because often context defines that.

So, for example, it may be that in

context of a technical document tells you that the point you're asking about cannot be between the gate electrodes, and so if that makes no sense, then I can't say it's over.

Q. Okay. Just getting back to the general meanings of the word "over."

Is there a difference between the word -- the meaning of the word "over" and the meaning of the word "above" in the context of the '997 patent?

A. Let's see. Can you tell me where in the '997 you have in mind? There may be several places, but it would be very helpful to see an example of that.

Q. In looking at '997 patent, which is Exhibit 4, and we look at dependent claim 2, which is at column 4 line 5.

A. Yeah.

Q. And it says:

"The method as claimed in claim 1 further comprising a step of forming an oxide layer over the diffusion region and on the sidewalls of

the gate electrode by thermal oxidation prior to forming the barrier layer."

A. (Reviewing document). Yes, I think -- I think I address this. Let me see if I can find it. (Reviewing document).

So that says "over" but you said "above."

Q. Right. I wanted to know --

A. Where is "above"?

Q. Well, in paragraph 27 of your declaration, you say that you have considered whether a broadest reasonable interpretation of forming an oxide layer over the diffusion region would be broad enough to cover forming an oxide layer above the diffusion region, and then you say "I believe that it would."

A. Yes.

Q. All right.

A. Oh, I'm sorry. I thought I was asking whether -- I thought you had asked whether these two are essentially equivalent in terms of both words being used in the patent. That's not what you

meant.

Q. No. I want to know --

A. Okay.

Q. -- what your understanding of the two words are. Whether you think that the meaning of the word "over" is the same as the meaning of the word "above."

A. Yes. Yes.

Q. So, for example, if there is an object that is -- so let's say I have object A and it is higher in a higher plane than object B (indicating).

Object A is above object B; correct?

A. Okay.

Q. And if object A is in the same vertical space as object B (indicating), object A is over object B; correct?

A. Yes.

Q. But if object A is not in the same vertical space as object B (indicating), is object A still over object B?

A. Can you go through that one more time?

Q. Okay.

A. It is puzzling to follow.

Q. Well, let me ask you this.

Do you think there's a difference -- outside of the context of the '997 patent, do you think there's a difference in the meaning between the word "over" and "above"?

A. Well, my understanding of the -- of the IPR process is that once you choose the most reasonable broad interpretation of that. So I could -- I interpret this to mean that when you say "over the diffusion region," that could mean above, whether or not they're vertically aligned.

So if I'm here and I ask about that point (indicating), that's clearly over this, but this is also over it. It's in a higher altitude than this.

Q. Okay. So in your definition of "over" in the context of the '997 patent, they do -- the two objects do not have to be in the same vertical space?

A. Yes.

Q. So it's fair to say that in the context

of the '997 patent, you believe that the word "over" and the word "above" have the same meaning; correct?

A. (Pause). I think that's right.

Q. Okay. Let's move on to paragraph 29. 29 through 31 I believe is where you're addressing the construction of the term "spacer" as it's used in the '997 patent. So I just want to make sure I'm clear.

Your construction of the term "spacer" as it's used in the '997 patent is "a structure that spaces between two conductive structures"; correct?

A. Uh-huh. No, I'm sorry. Wait a minute.

You said my construction of spacer is "a structure that spaces between two conductive structures"?

Q. Yes.

A. Well, what this says is it's broad enough to cover that, but -- but there may be other definition of spacer.

Q. So spacer could be -- your construction of spacer is even broader than a structure that spaces between two --

A. No. No.
Q. No?
A. It's broad enough to cover that.
It could be broader. I don't know of an example, though.
Q. Do you have a specific construction of the term "spacer"?
A. Yes.
Q. And what is it?
A. Well, it's what's in 29 here.
Q. What's the difference between your construction being "a structure that spaces between two conductive structures" and simply being broad enough to cover "a structure that spaces between two conductive structures"?
A. Yeah, I guess -- I guess there isn't.
Q. Okay. So your --
A. Yeah. Okay.
Q. So just for clarity purposes, so your construction of spacer is "a structure that spaces between --
A. Yes.

Q. -- two conductive structures"?
A. Yeah.
Q. Okay. Does that construction cover the function of creating space during ion implantation?
A. I don't -- I don't understand what the "spacer" word has to do with ion implantation.
Q. In the context of, let's say you're implanting ions into the substrate area --
A. Uh-huh.
Q. -- next to a gate electrode --
A. Uh-huh.
Q. -- or close to a gate electrode.
Is one of the functions of the spacer to make sure there is space between the implanted area and the gate electrode?
A. In the lateral direction.
Q. Yes.
A. It can be, yes.
Q. And is that functionality included within your construction of spacer?
A. Well, the implanted region is marginally a conductive structure. So I'm not quite

sure how to think about the fact that here the interpretation has to do with spacing between conductive structures. Implanted region will have a reasonable conductivity. So, yes, I think so.

Q. What are some of the other functions of a spacer that are included within your construction?

A. Well, we went through this before. The construction doesn't say anything about the application. So it is very general.

A spacer can be used to prevent chemical reaction, to prevent diffusion, to prevent transport of electron charge. It can be many things, and I don't think it has anything to do with this general interpretation definition of spacer.

Q. Just for clarity purposes, you just said that a spacer can be used to prevent chemical reaction, to prevent diffusion, and to prevent transport of electron charge.

And I just want to make sure that you're referring to the function of a spacer and not the function of a barrier layer.

A. Well, a spacer can be a barrier layer.

Q. Okay. All right. Because they are very similar, and I wanted to make sure.

A. They can be, yes.

Q. Okay. Is your construction of spacer broad enough to cover all of those different functions of a spacer that you just mentioned?

A. Well, spacing between two conductive structures, which is what we're talking about here, doesn't tell anything about what function we're describing or measuring; right? So I don't think I can answer that question.

Q. Can you give me an example of a function of a spacer that would be covered by your construction of the term "spacer"?

A. Well, I think if a spacer spaces between two conductive structures, then if these conductive structures have in principle when intimately connected the ability to transport ions, to transport electrons, to undergo chemical reaction, then bringing them apart by putting something in between them may be able to suppress those phenomena, so serve those functions.

Q. Okay. Moving on to paragraph 32, in paragraph 32, you're giving your construction of the term or the phrase "etching an opening through the insulating layer self-aligned and borderless to the diffusion region."

What does the term "borderless" mean in the context of that phrase?

A. So borderless -- it would be interesting to know where the original term came from. But people speak of borderless context as situations where if I want to make contact to a diffusion region for -- as an example, I don't need to localize that hole within some larger structure that has a differential radius to make sure that I'm not shorting to something on the side.

So if I wanted to punch through a contact through an insulator and there's -- there's an electrode on one side or the other, I normally have to drill through but make sure that there's a border, a margin of error. So that when I put conducting material here, next to this is not touching.

So I think the term probably came from somebody looking at lithography masks and saying, well, we want to drill onto that contact. We've got another wire or gate electrode here and so when we define the mask for that hole, we have to leave a border, at least on this side and maybe on other sides.

So what these patents are talking about is borderless situations where the formation of the spacer during the etch protects against that happening so you can have a much larger lithographic hole to make that contact.

Q. All right. So the term is tied into the meaning of self-aligned?

A. Well, it may be used someplace else, but in the context of this patent and in the situations that I've known, yes, it has everything to do with self-aligned.

MR. CHEN: Exhibit 6.

(Document marked, for identification purposes, as Rubloff Exhibit No. 6.)

BY MR. CHEN:

Q. I've asked the court reporter to mark as Exhibit No. 6 patent number 6,277,720, which were referred to as the Doshi reference.

And this is one of the references -- Exhibit No. 6 is one of the references that was cited by Samsung in its IPR of the '997 patent; correct?

A. Uh-huh.

Q. Okay. Did you select this reference for -- as prior art for the '997 patent?

A. It is prior art.

Q. Okay. Did you find this reference?

A. Did I find it initially? No.

Q. You were provided with the patent?

A. Yes. I was provided a whole bunch of references, and I found and knew of a number myself, and so I looked at all of those and decided which ones to actually use here.

Q. Okay. So you -- you decided which ones to actually use --

A. Yes.

Q. -- in your declaration subsequently, I

guess, in the IPR then?

A. Yeah.

Q. Are you familiar with the term "sidewall filaments" as it's used in the Doshi reference?

A. Yes, I've read the Doshi.

Q. Okay. Are the sidewall filaments the same thing as spacers?

A. Sidewall filaments in the Doshi reference --

Q. Right.

A. -- serve one and possibly two functions. One is the sidewall filament is made partly by rapid thermal oxidation, which is similar to what is in the '997; but, more importantly, it has a component of conformal deposition anisotropic etching to form another component of that sidewall filament where the thickness of that determines a spacing between the edge of the gate electrode and where the ion implantation is done for the source/drain. So that's an adjustable parameter.

So the way to think about that and the

way to say it, I think, is that it serves the purposes of a doping spacer as well as potentially an electrical spacer.

Q. Okay. And is the function of a doping spacer a function that would be covered by your construction of the term "spacer" in the context of the '997 patent?

A. Yes.

Q. I want to take some time and walk through the process --

A. Uh-huh.

Q. -- that's described in the Doshi reference.

A. Okay.

Q. The process, I believe, begins at column 7 line 28.

Before we do that, we've been going for about an hour. Do you guys want to take a break?

MR. MUKERJI: Let's take a short break.

MR. CHEN: Yeah.

(Recess - 2:09 p.m. - 2:29 p.m.)

BY MR. CHEN:

Q. Okay. We were looking at the Doshi reference before we broke, and we're starting at Exhibit No. 6 column 7 line 28.

So the first step in the process described here in Doshi for fabricating an integrated circuit is to define the active regions and the isolation regions; correct?

A. Okay.

Q. And the next step is to form the gate electrode; correct?

A. Okay. That's going down to line 51 or something like that? All in 3a; is that where you're referring?

Q. Yeah. Yeah.

A. (Reviewing document). Okay.

Q. And then the next step it says:

"Following definition of gate structures 10, light 'reach-through' implants are performed in a self-aligned manner relative to gate structures to define source/drain extensions."

Do you see that at line column 7 lines

52 to 55?

A. Yeah. Are we still on 3a?

Q. In terms of figure?

A. Yeah.

Q. I think that's right. I think there's a lot of -- a lot of steps that are subsumed within 3a, but I'm looking at the text.

Then following -- well, first of all, what are the light reach-through implants?

A. Those are marked in 3a as 6' and 7'.

Q. What is their function?

A. Their function is to change the dopant profile of the source/drain regions to improve device performance.

Q. Are they part of the source/drain region?

A. Yeah. They're electrically connected to the source/drain region, but the point there is that people these days -- these days and in this time frame as well do substantial modeling on the performance of hard electrons and saturation velocities and all of that. And the detailed

three-dimensional distribution of dopant profiles, and not just profiles but concentrations, makes a substantial difference in the performance of the transistor devices.

So this is called source/drain engineering, trying to make it look a certain way. And I remember when I started, you know, in the '80s getting involved with some of the silicon technology people before I joined the department, there were people talking about source/drain extension and the source/drain connected to it and so on.

Q. So the source/drain extension is considered a part of the source/drain region; correct?

A. Yeah, it's part of the profile.

Q. Okay. And the dopant profile.

Well, what is a dopant profile?

A. You mean how did I define that?

Q. Yeah. How did you just use the term "dopant profile"?

A. Well, if you look in Figure 3a at the P device on the left.

Q. Right.

A. You see a profile that says "p+" and it has this little extension under the gate. It could be called source/drain extension sometimes.

And so when I say "dopant profile," what I really mean is concentration of dopants as a function of X, Y, and Z. Because I know it's drawn as if it's all p+, but it's not and, in fact, it can't be a boundary quite that sharp anyway. There's always a spread in how the P concentration goes down and the N concentration crosses over.

Q. And you said that the dopant profile for a device makes a substantial difference in the performance of that transistor device?

A. Yeah, it can.

Q. And what affects the dopant profile of the device?

A. Number one, how you make it. In this case, two implantation steps. Number two, the heat treatment that it sees in subsequent steps. And number three, how much dose you put into those places that are unmasked during ion implant.

Q. When you say "dose," you mean how much impurities are implanted --

A. Right.

Q. -- into the region?

A. Right.

Q. So changing the dosage would affect the dopant profile of the device?

A. Yeah. If you turn down the ion flux by a factor of 2 will probably change the performance. It may have the same shape. So that -- that C concentration of X, Y, Z --

Q. Right.

A. -- may become C over 2 but have the same shape.

Q. Right. The shape could be the same, but the concentration of impurities in that region would differ?

A. Yeah.

Q. Okay. And other things that could affect the dopant profile are, I think you said, the heat treatment as well; right?

A. Right.

Q. And the heat, how does the heat treatment affect the dopant profile?

A. Dopants diffuse in silicon and so the longer you heat the sample, the wafer, and the higher the temperature, the more diffusion you get. So what may have started out as a shallow doping profile, if you wait long enough, that -- that limited -- let me think of a fix for it -- will diffuse into something much broader and lower in concentration. Limited source diffusion.

Q. Okay. Does implantation energy also affect the doping profile?

A. Yes.

Q. Because that implantation energy will affect where the impurities are deposited in the substrate; right?

A. Right. How deep they penetrate.

Q. Okay. Looking at column 7 line 57 -- we briefly talked about this before -- it says:

"According to the preferred embodiment of the invention, sidewall filaments are formed."

You see where it says that?

A. Uh-huh. Uh-huh.

Q. And then it says:

"Sidewall filaments 11 are formed by first oxidizing the sides of polysilicon layer 22."

And then it goes on to talk about a subsequent step where silicon nitride is deposited and etched.

A. Uh-huh.

Q. So my question is: Are the oxidized sides of the polysilicon layer part of the sidewall filaments?

A. Yes.

Q. Why would you say that they are part of the sidewall?

A. Well, the sidewall -- what is described here as the sidewall filament is composed of oxidized polysilicon, which is silicon dioxide and nitride. So they both are insulators. So it would be hard to differentiate them except chemically, but functionally they're both insulators.

So I think, though it's not described in great detail here, I think what's intended here

is that 11 is a sidewall filament that's a composite of both components.

Q. Okay. Looking at -- I think we're still on Figure 3a.

The sidewall filament is a structure labeled 11 in the figure; correct?

A. Yes.

Q. Okay. And the polysilicon is the structure that's labeled 22; correct? The polysilicon portion of the gate?

A. Yes.

Q. And the oxidized portion of the polysilicon is just on the sidewalls of the structure that's labeled 22; correct?

A. Hold on. 24 is above 22.

Q. Right.

A. It's tungsten silicide.

Q. Right.

A. So the thermal oxidation of the sidewall of the polysilicon --

Q. Right.

A. -- will cause some oxidation of the

silicide as well.

Q. Oh, okay.

A. So, I mean, it's not really drawn here that way. This wasn't the point that was elucidated in detail.

Q. So the oxidized layer that was formed would cover 22, the sidewalls of 22, some of 24, but would not extend up to the silicon nitride layer 26; right?

A. Yeah. I don't think the silicon nitride will be oxidized.

Q. Okay.

A. And I don't know what the relative thickness of the rapid thermal oxidized on the silicide and on versus the polysilicon will be.

Q. Okay.

A. Probably more on the polysilicon, but I'm not sure.

Q. And you said that during the oxidation process, an oxide layer would also be formed over the diffusion regions; is that correct?

A. Yes.

Q. And this is true if the diffusion region is uncovered silicon; correct?

A. Well, if it's -- it's true if it's uncovered silicon, or if it's covered by thin oxide. Because thermal oxide has linear growth rate in the thin regime. So if you already have a thin layer of oxide and you go to oxidizing conditions, you make it thicker.

Q. But what you're doing there is you're thickening the existing oxide?

A. Yeah, which you're oxidizing it. It's the same oxidation chemistry as whatever formed it originally.

Q. Doshi only says oxidizing the sides of the polysilicon layer in column 7 line 59; correct?

A. Uh-huh.

Q. So Doshi doesn't specifically disclose thermal oxidation; correct?

MR. MUKERJI: Objection to form.

THE WITNESS: One of ordinary skill would interpret oxidizing any kind of silicon as thermal oxidation.

BY MR. CHEN:

Q. Is it --

A. Otherwise it would say CVD using such and such precursor.

Q. So is thermal oxidation the only method amenable to oxidize the polysilicon layer?

A. No.

I'm sorry. To oxidize polysilicon.

No, it's not. You could do anodic oxidation, which is a wet chemical electric chemical technique. I mean, I don't think anybody would do it here, but it could be done.

Q. Well, how do you know that Doshi, when it says oxidizing the sides of the polysilicon layer, is referring to thermal oxidation as opposed to the other form of oxidation using the wet chemical electrodes?

A. If it were wet chemical, it would have said anodization because it's a standard way of describing it. Poured silicon is made this way, for example. And in this technology domain, silicon, oxidizing means you use O2, or conceivably O2 with

some water, or conceivably N2O, but it's a gas-phase process. Oxidizing means that what used to be silicon becomes a new compound.

Q. Okay.

A. As opposed to CVD deposition of a silicon oxide, where both the silicon and the oxygen came from the vapor phase.

Q. So when you do CVD deposition of a silicon oxide, what you're doing is you are depositing new material onto, let's say, the substrate or wafer; correct?

A. That's right. All the source material comes from the gas-phase in CVD.

Q. Right. And when you're doing thermal oxidation, what you're doing is you're converting the existing material to a different compound?

A. Right.

Q. Right?

A. From silicon to SiO2.

Q. So if I have a layer of silicon and I perform thermal oxidation on that layer, part of that silicon gets converted to silicon dioxide;

correct?

A. Uh-huh.

Q. Is the overall thickness of the layer, which has both the original silicon and the converted silicon dioxide, the same thickness as the original layer of silicon prior to the thermal oxidation process?

A. No, it's different.

Q. How is it different?

A. Because the density of SiO2 is different from that of silicon, and so it turns out that when you oxidize, the thickness of the silicon which you started with gets smaller because you've consumed some. But if you look at the thickness from the bottom of the silicon to the top of the oxide, that grows.

Q. Okay.

A. And the ratio of how much is above and below the initial surface is something like 40/60 or 60/40. I don't know. I don't remember.

Q. The point is, it gets thicker?

A. It gets thicker.

Q. Okay. When you perform thermal oxidation -- oh, actually, never mind.

After the step of forming the sidewall filaments, then you form the source/drain implants. That's at column 7 beginning at line 66.

A. Uh-huh.

Q. Okay. And it's this step here where you discussed before that the sidewall filaments are used to create space between the implantation and the gate electrode; correct?

A. Right.

Q. The next step -- this is at the beginning of column 8 line 8 -- it talks about the formation of silicon nitride layer 30.

You see that?

A. Uh-huh.

Q. What is the function of the silicon nitride layer?

A. The silicon nitride layer is nominally an etch barrier for etching through the layer that will be on top of it, the ILD layer, interlayer dielectric, but it will also serve as the spacer at

the end of the process.

Q. Where does Doshi say that it will serve as a spacer at the end of the process?

A. Well -- (reviewing document). I'm not sure if I can find where it is explicitly stated, but the structure is identical to the spacer structure in the '997 patent and so it serves the same function.

I think he implies it. This would be at column 9 line 65 through 70.

"Figure 3g illustrates the construction of integrated circuit 20 after the completion of both etch steps, and the stripping of photoresist layer."

So I think he implies it there, but I don't know if I -- it's a long specification. So I don't know if I can --

Q. How does he imply it there? That paragraph that you just referenced doesn't even mention the silicon nitride layer 30.

A. Well, but he's prescribed that after the second etch, the silicon nitride is left on the

sidewall, and it's shown in the drawings. So I think it's very clear that there is a spacer there.

Q. Where does Doshi say that the silicon nitride layer is left on the sidewalls?

A. (Reviewing document). So Figure 3g shows the sidewall filament 11 and it shows silicon nitride 30 that's left on the sidewall next to the hole where the self-aligned contact goes in 3h.

Q. Other than Figure 3g, is there any place in the text of Doshi that says that the silicon nitride is left on the sidewall after the etch?

A. Well, I can't -- I don't remember exactly what he says about that, but it is very clear here, and I even identify that there was a minor error in the way the structure was drawn. But we know that that's what would happen, and the '997 builds on that afterwards and so I think it's -- it's very clear.

Q. Can you point to any place in the text of Doshi that says that the silicon nitride is left on the sidewalls after the etch?

A. Let me look some more. I don't remember. It's a long specification. (Reviewing document).

So I think it's implied in the paragraph in column 10 line 4.

"It has been observed, in connection with the present invention, that the two-step etch of BPSG layer 14 and nitride layer 30 is particularly beneficial, as damage to the corners of gate structure 10 and sidewall filaments is substantially minimized."

So if the corners -- if in the process of the second part of the etch through the nitride, which forms the sidewall spacer, the damage at the edge is minimal, then we know that there remains silicon nitride on the sidewall of the gate electrode.

And it goes on to say:

"In particular, sidewall corner locations NC illustrated in Figure 3g have been observed to be particularly susceptible to damage from conventional nitride etches. However, the

brief nitride etch used to clear nitride layer 30 from within plug contact locations" -- at the bottom because that's where the contact is going to be -- "PC has been observed to be highly anisotropic."

So he's reconfirming that that etch is highly anisotropic, and it doesn't etch that much from the corner. It should have -- my point was, it should have shown a little bit of change, but it's very little. And so that means that the sidewall nitride 30 is going to be there and that will serve as a spacer.

He doesn't say, this is a spacer. He doesn't say that. At least not here, and I haven't found where he says that, but it is very clear that it's a spacer. And it's the same thing that the '997 purports to use as a spacer.

Q. I understand that you have a, you know, interpretation of the Doshi reference, but that paragraph that you just read doesn't specifically say that the nitride 30 layer is left on the sidewalls after the etch; correct?

A. No, I think it says it. It doesn't say

it explicitly as you said it, but it makes it very clear to one of ordinary skill that if I haven't done much damage to the 30 at the top there and I use a highly anisotropic etch, I will have remaining a nitride sidewall spacer.

Q. Where does it say you will have remaining a nitride sidewall spacer?

A. It doesn't say it that way. It says it's a highly anisotropic etch, and it doesn't damage or remove much at the top at that corner above the sidewall filament. Therefore, one of ordinary skill would certainly conclude that that sidewall nitride structure remains --

Q. Well --

A. -- as a spacer.

Q. -- it doesn't say that it doesn't remove much of the nitride. It says it doesn't damage the corners of the gate structure as much; correct?

A. Well, the gate structure is underneath the photoresist.

Q. Right. But the gate structure is still

damaged. It's just not as much as before; correct?

A. Yeah. I think some of that nitride will be removed. That's what I tried to correct in this figure on page 37.

Q. So all that section says is that having the nitride there reduces the damage to the corner of the gate structure; correct?

A. Yes, but I describes the etching process in a way that's essentially identical to what the '997 purports to claim, and it forms what one of ordinary skill would recognize as a sidewall spacer made of nitride.

Q. In order to even damage the gate structure, you have to etch through the nitride layer protecting that gate structure; correct?

A. I'm not sure about that. (Reviewing document).

When you use reactive-ion etching to do highly anisotropic etching, you have on the wafer a large bias, several hundreds of volts. So the reactive-ion species that do the etching are very energetic, and that's why reactive-ion etching is

always a concern for damage to materials. It doesn't matter where. It happens all the time.

So it's reported that that region NC is particularly susceptible to damage from conventional nitride etches. That may be a mechanism where the energetic ions impact the top corner of the nitride and cause stress buildup, or something like that, that influences the properties of the gate electrode. It may be. I don't know. I mean, I didn't study that.

But I still come back to the fact that while I haven't yet found a place where Doshi makes it clear and simple that this nitride remains and forms a sidewall spacer, it's absolutely clear to -- for one of ordinary skill that it does remain because it's an anisotropic etch. And it hasn't modified much of that sidewall nitride, except perhaps at the top.

Q. And you're pointing to the Figure 3g; is that correct?

A. Yes, that's right.

Q. Are you relying on Figure 3g for your

understanding that the nitride layer remains on the sidewall of the gate electrode?

A. No. That confirms it to some extent, but I'm relying on my understanding and one that would be easy for one of ordinary skill to know that when you do the sequence of steps here, you will have a sidewall spacer.

Q. Even though Doshi doesn't actually say that you will have a sidewall spacer; correct?

A. But, remember, Doshi is a long patent with many embodiments and stack capacitors and all kinds of things in it, and he's talking about -- some -- sometimes the recognition of earlier invention in the prior art, as I understand it, can be found in things that are teaching the thing you're wondering about but not really making that the focus of what's there.

So I think Doshi covers a lot of things here.

Q. But Doshi doesn't specifically say that you will form sidewall spacers from nitride layer 30; correct?

MR. MUKERJI: Objection to form.

THE WITNESS: Well, I haven't reviewed the whole thing to look for where in one of the other applications he may have addressed that, but the process is very clear. There will be a sidewall spacer and everybody knows it.

BY MR. CHEN:

Q. Sitting here today, you cannot point to any specific portion in Doshi that says that sidewall spacers are formed from nitride layer 30; correct?

MR. MUKERJI: Objection to form.

THE WITNESS: I don't know the answer to that. I have to read the whole patent in detail.

BY MR. CHEN:

Q. You didn't read the whole patent in detail before?

A. Of course I did. I can't remember everything that's here.

Q. Okay. But you didn't cite to any portion of Doshi in your declaration?

A. No, I didn't.

Q. Right?

A. No, that's right.

Q. Do you think that Doshi might have said it somewhere, but you left it out of your declaration?

A. I have no idea. I did this six months ago, whatever it was. It's a long patent, and to me it was very clear.

In fact, the first time I encountered the teaching of the BPSG on top of the nitride serving as an etch-stop next to the gate electrode, the first time I encountered that was '997, which taught me after Doshi, prior art, that you make a sidewall spacer there. And I knew it before, and I think one of ordinary skill would know that.

Q. And so my question is and it's pretty simple question:

Sitting here today, can you point to any specific portion in Doshi that says that sidewall spacers are formed from nitride layer 30?

MR. MUKERJI: Objection to form.

THE WITNESS: I cannot yet do that, but I have not reread the patent to be able to answer your very explicit question.

BY MR. CHEN:

Q. Okay.

A. But I think this is not the issue, whether he says it or not. It forms the same structure as the '997 shows and it came before.

Q. In order for nitride layer 30 to act as a sidewall spacer, does it need to have a certain thickness?

A. Larger than zero. Yes.

Q. Just larger than zero?

A. No. I don't know. I don't know what number to put on it. Yes, it has to have a finite thickness.

Q. Should it have a relatively thick -- should it be a relatively thick layer to act as a sidewall spacer?

A. No, I don't think it needs to be very thick. We made essentially CVD, actually ALD, insulating layers 6 nanometers thick. They are

excellent insulators. So it doesn't have to be very thick.

Q. What does it depend on? How thick -- what determines how thick that layer needs to be in order to act as a sidewall spacer?

A. It depends on the quality of the material, and the thickness should be greater than a tunneling distance, but that's -- that's of order one nanometer or less. So that's kind of an irrelevant number. That's very thin. Tunneling distances I mean.

MR. MUKERJI: Can we go off the record for just one second?

(Off the stenographic record)

(Recess - 3:16 p.m. - 3:38 p.m.)

BY MR. CHEN:

Q. All right. Dr. Rubloff, before we went off the record, we were talking about --

A. Uh-huh.

Q. -- the nitride layer 30 --

A. Yes.

Q. -- as described in the Doshi reference.

I noticed that you were, you know, taking the time during the break to review the reference.

A. Uh-huh.

Q. Did you find -- in your time reviewing the reference, did you find any location where Doshi specifically says that nitride layer 30 is -- remains on the sidewalls of the gate electrode and acts as a spacer?

A. I haven't found anything explicit along the lines of the words that you just used. But the description, for example, in column 3 on 60, which is the description of how the sidewall filaments are made, talks to "silicon nitride sidewall filaments are conventionally formed by CVD of silicon nitride overall, followed by an anisotropic nitride etch to remove the nitride from the flat active regions, leaving sidewall filaments behind."

The structure of the sidewall filament is similar to the structure of the nitride layer 30 that is explicitly depicted in Figure 3g of Doshi and corresponds, I think, directly to what the '997

purports.

So while I have not found the explicit kind of wording that you are looking for, I think one of ordinary skill would recognize Doshi is doing the same thing that the '997 is doing.

Q. The sidewall filaments that are described in Doshi are actually explicitly described as having the spacer function; correct?

A. Having the doping spacer function; right.

Q. And in column 8 where Doshi is describing the nitride layer 30, it describes certain functions for that layer; correct?

A. Column 8 where?

Q. Column 8 beginning at line 8.

A. I'm sorry. Line?

Q. 8.

A. (Reviewing document). Well, that's a function -- the description you're referring to is the dopant barrier that 30 silicon nitride serves to prevent boron and phosphorous from the -- overlying BPSG from diffusing into the silicon.

So what -- what it basically says is the nitride serves as a diffusion barrier for that structure, but that's not addressing its sidewall function.

Q. Right.

A. It's addressing its chemical function.

Q. Right. It's specifically --

A. One of its functions.

Q. -- discloses a function for that layer and that function that is disclosed is acid diffusion barrier?

A. That's -- yes, but a layer like that can have multiple functions. Silicon nitride is a pretty good insulator, electrical insulator.

Q. All right. Following the formation of silicon nitride 30 -- layer 30 is the formation of the interlayer dielectric, and that's referred to at column 8 line 23; correct?

Oh, sorry. Actually --

A. Let's see.

Q. No, that's correct.

A. Yeah.

Q. So it begins at column 8 line 23; correct?

A. Uh-huh.

Q. Right. And that interlayer insulator is made of BPSG; correct?

A. Yes.

Q. And BPSG is a silicon oxide layer; correct?

A. It's a silicon-based oxide layer, but it's doped with boron and phosphorous.

Q. Okay.

A. That changes its mechanical properties significantly.

Q. And subsequent to the deposition of the BPSG layer, that layer is then planarized; correct?

A. Yes.

Q. All right. And then Doshi -- moving along, Doshi starts to talk about the formation of the contact openings.

A. I'm sorry. Can I go back to the BPSG question?

Q. Sure.

A. So this describes that after the layer 30 is put down over everything conformally --

Q. Right.

A. -- as the next top layer, the BPSG is put down and then it's planarized by high temperature annealing step.

What will happen during that annealing step is important for the understanding of the sidewall filaments function. Because it just described that nitride is a good barrier to boron and phosphorus diffusion -- diffusion, but referring only to the consequences for the crystalline silicon n+ region, the substrate; right?

So it's basically saying, what you just read, says that silicon nitride layer 30 when it's still on top of the n+ region will prevent boron and phosphorous diffusion into the silicon.

That -- that has a consequence that on the sidewall, the remaining nitride 30 will serve as a boron and phosphorus diffusion barrier. So that boron and phosphorous from the now present BPSG next to the nitride layer 30 can't get through 30 to get

to the polysilicon or tungsten silicide because the component of the sidewall filament, the thermal oxide, is not a good barrier.

So what I'm saying is the sidewall nitride structure 30 will play a role during the planarization step, which is annealing the BPSG, in preventing dopants from entering the polysilicon. And for that matter, it could be the gate oxide at that point.

Q. Okay. And what is the significance of that --

A. Well --

Q. -- point you just made?

A. -- the significance is that if the -- ah -- is that at least during that step, there is a function for that sidewall spacer of nitride. It's not the electrical barrier at that point because that hasn't been encountered yet until the structure is done.

Q. So you're saying then at the point of the BPSG formation, the nitride layer 30 covering the sidewalls of the gate electrode structure is

performing spacer function?

A. Yeah, and diffusion barrier function. It's not highlighted here because it's probably not as big a problem, but I noticed that a lot of attention is given to the diffusion barrier function of the nitride material with regard to the source region.

Q. Okay.

A. It's just a comment.

Q. Sure. So then, for example, looking at Figure 3f, which -- what figure are you looking at in your declaration?

A. Too many. I have Figure 3g in my declaration.

Q. Okay. Well, let's look at Figure 3f.

A. Okay.

Q. Or no. Sorry.

A. Yes.

Q. Figure 3 -- let's look at Figure 3d. All right? This is the figure before the contact openings are being etched, but you have the BPSG layer 14, I believe it is.

A. Uh-huh.

Q. Right. So looking at Figure 3d, a person of ordinary skill in the art would look at a portion of nitride layer 30 covering the sidewalls of the gate electrode and say that's a spacer right there?

A. Well, I would say it's a diffusion barrier during BPSG reflow, which is an annealing step.

Q. So it is not a spacer?

A. Well, a diffusion barrier is a kind of spacer.

Q. Okay. So it is a spacer?

A. Yes.

Q. Okay.

A. But that's not the spacer that's at issue here. I realize that.

Q. I don't follow you.

A. No. I think your question was, at this stage after both etches of BPSG and nitride is done, how do we know there's still a nitride sidewall spacer? And that's a different -- that's a

different question.

Q. That's a different.

A. I may have raised an irrelevant question. It was just an observation because there's been so much attention in what you read to the diffusion barrier properties of the nitride.

Q. Right.

A. Sorry if I got us off-track.

Q. No, no. I just want to understand. I mean, maybe it's an important point.

Because you are saying that during BPSG formation, that portion of the nitride layer that's on the sidewall is acting as a diffusion barrier in the --

A. Lateral.

Q. -- lateral direction?

A. Yes.

Q. Thank you.

And I think your point was, is that at that stage, that portion of the nitride layer, the portion that's on the sidewall of the gate, is functioning as a spacer; correct?

A. A diffusion barrier spacer.

Q. And that diffusion barrier spacer is within the definition of spacer that you provided in the context of the '997?

A. Yes.

Q. Now, one reason you said that that is needed to provide that function is because you said that the thermal oxide of the sidewall filament is not a good diffusion barrier; correct?

A. That's correct.

Q. Okay. But the sidewall filament is not just comprised of thermal oxide; correct?

A. That's correct.

Q. Okay. It actually has a layer of silicon nitride; correct?

A. Right, which was formed exactly the way that the sidewall fill -- the sidewall spacer 30 is formed during the two-step etch.

Q. Okay. And silicon nitride is a good diffusion barrier?

A. It is a good diffusion barrier.

Q. Okay. So in a sense, the sidewall

filament 11 will protect a gate from any boron or phosphorus diffusion?

A. It can, yes.

Q. And you don't really need the nitride layer 30 there to act as a diffusion barrier; correct?

A. I think that's correct. Well, it helps but --

Q. Okay. Okay. So we've talked about the formation of the BPSG layer, and I'd like to talk a little bit now about the formation of the contact openings and that begins at column 9 line 26.

A. (Reviewing document).

Q. Okay. I guess the first step of forming the contact opening is to form the patterned resist; correct?

A. Yes.

Q. All right. And the next step is to then etch through the BPSG layer stopping on the nitride layer; correct?

A. Yes.

Q. All right. And this is where the

nitride layer is behaving as an etch-stop?

A. Yes.

Q. And then what follows after the BPSG etch step is a nitride etch step; correct?

A. Uh-huh.

Q. And the purpose of that nitride etch step is to etch through the nitride layer; correct?

A. It's to etch through the nitride layer that's covering this source/drain region, the diffusion region, and at that point it forms the sidewall spacer.

Q. Looking at your declaration at paragraph A-12, you describe the second etch as "an anisotropic etching of the barrier layer underneath the opening."

You see that?

A. Uh-huh.

Q. Now, the part that you -- you quoted from the patent says:

"Contact openings (PC, BLC, CT) are etched through the BPSG layer (14) and the silicon nitride layer (30) using a two-step etch process."

What does the PC stand for?

A. Yeah. I don't remember which figure that is.

Q. I mean, is PC, BLC, and CT just different contact openings in different regions?

A. I'll have to think about that.

Q. Actually, maybe this will help you.

If you look at column 10?

A. Yeah.

Q. Line 3, for example. It says "within plug contact openings PC."

Is PC just plug contact?

A. Yeah, that's -- (reviewing document). Okay. In Figure 3g, PC is the plug -- excuse me -- plug contact. Because the PC is in the place where the opening through BPSG and nitride is.

And NC -- okay. That's different. That's the corner.

BLC is in Figure 3i.

Q. Right.

A. And I think 3i refers to a different structure, a different device. Plug oxide layer.

Q. Well, if you go to --
A. It's part of a DRAM circuit it appears. Bit line contact location is BLC.
Q. Right. So if you look at column 10 line 40, for example, it says:
"As in the formation of plug contact locations PC, bit line contact locations BLC."
So I assume that PC refers to plug contact and BLC refers to bit line contact?
A. Uh-huh.
Q. Is that right?
A. I think so.
Q. Okay. What is a CT?
A. (Reviewing document).
Q. Maybe that's not.
A. (Reviewing document).
Q. If you don't know, it's okay. We can move on.
A. I don't know. I think that those refer to other applications than the ones we've concentrated on --
Q. Okay.

A. -- and are relevant. So I think it's not a big deal.

Q. Okay. All right. Getting back to the nitride etch.

So the results of the nitride etch are shown in Figure 3g; correct?

Or the results of the nitride etch for the plug contact openings are shown in Figure 3g; correct?

A. Yes.

Q. And then you mention that you found an error in Figure 3g; correct?

A. Yes. I think it was a little misleading. I would have expected to see -- what page do I have this on? Yeah, on page 37.

I would have expected to see some of the top nitride etched away there.

Q. And that's not depicted in Figure 3g; right?

A. No. No. Figure 3g on page 37 of my declaration shows a little region in a rectangle where that top part of nitride 30, I think, should

have been shown removed, and that's an annotation to a blowup of the right part of Figure 3g near that plug contact.

Q. And the reason why that portion of the nitride layer 30 would have been removed is because it is within the exposed portion of the contact opening mask?

A. That's right. And so the thickness of that nitride as it meets the resist layer would be in conformal CVD the same as the thickness of the nitride that would be on top of the n+ region. So when you clear the n+ region, you'll lose some of that top part, but you'll still leave the sidewall nitride 30 because it's the standard way of making sidewall spacers.

Q. Other than the error that you pointed out in your declaration, are there other errors in Figure 3g of Doshi?

A. None that I know of, or I would have declared them.

Q. Previously you had mentioned that the diffusion region is covered by a thermal oxide

layer; correct?

A. Yeah, from the RTO.

Q. Right. Is that thermal oxide layer depicted here in Figure 3g?

A. No, because the etch that removes the nitride would have to remove any thermal oxide there in order to allow good contact to the n+ region.

Q. But isn't the etch to remove the nitride selective to nitride over oxide?

A. Right, but selectivity is never infinite. It's a certain number and nitride is significantly thicker than a little bit of thermal oxide --

Q. Okay.

A. -- that might have been present there.

Q. So it's your opinion that the etch that removes the nitride would also etch through any thermal oxide that is --

A. Yeah, and it wouldn't have to etch through all of it. Because when you make a contact like that, if there are a few patches of very thin oxide remaining, it doesn't change the

characteristics very much. You would like not to have that.

So the way -- the way to think about that is, if I make a contact here and there's some oxide here, but there are plenty of places where there is not oxide, that's really all I need to get the contact resistance lowered enough to make effectively contact.

I mean, I don't think every oxygen if there were thermal -- a little bit of thermal oxide here, I don't think it means that every single oxygen atom has to be gone after the etch for it to be a good contact to the material that fills this region.

Q. Wouldn't you want to clear off any oxide over the contact to make a good contact?

A. Yeah, of course. You'd like to clear off whatever you can and that means most of it, but it doesn't have to be every atom.

Q. Looking at Figure 3f of Doshi, this is before the nitride etch step.

The thermal oxide isn't shown in this

figure here; correct?

A. The thermal -- which thermal oxide?

Q. The thermal oxide over the diffusion region.

A. No.

Q. Okay. Is that another error in Doshi figures?

A. I don't think it's an error. It wasn't necessary.

Q. Wasn't Doshi --

A. It's not depicted in 11, the sidewall shown. Doshi says we do rapid thermal oxidation to make part of the sidewall filament, and we do nitride sidewall formation by CVD and anisotropic etch to make the other component of sidewall filament. But he doesn't break up -- despite having said that there are two components to 11, he doesn't attempt to draw that separately.

So I think it -- remember, as I said before, Doshi is trying to look at a much bigger picture than the '997 is. So he teaches the dual step, the two-step etch and the use of the nitride

and the BPSG to do a self-aligned contact. He teaches that as part of a much larger picture in the Doshi patent.

So leaving out some details which are in some of the places not put it in the figure, but it's explained in the text. Everything doesn't have to be in -- at least as I understand it, there is no need for the patent to show every detail of the specification in figures.

Q. So what you're saying is that some aspects of what Doshi disclosed in his text are not directly reflected in its figures?

A. Yes.

Q. The one error that you did find is the error in the etching of the nitride layer 30, which is what you pointed out in your declaration with respect to Figure 3g, though; correct?

A. Yeah. I guess I would say I'm a little uncomfortable with the notion of depicting that as an error because I think the description in the specification tells us what these shapes will look like, and they were known to one of ordinary skill.

So I would rather have seen it drawn differently, but error sounds like there's something fundamentally wrong. I think that's too strong a word.

Q. Okay. Well, you called it an error.

A. Yeah, I know. Maybe not the best choice of words.

Q. Are there other errors in the depiction of the etching of nitride layer 30 in the figures of the Doshi reference?

MR. MUKERJI: Objection to form.

THE WITNESS: It's possible, but I don't know of any. I mean, we could argue -- I think it's difficult. We could argue about exactly what the sidewall profile would look like after the nitride is etched to form the sidewall -- sidewall spacer, and that has to do with how anisotropic the etch is and so on there.

We could quibble about these details, but I know how these drawings are made. They're made by a draftsman who gets a sketch and tries to make it right, and they're not always

accurate.

BY MR. CHEN:

Q. Okay. So it's better to rely on the text of the reference as opposed to the figures; is that fair?

MR. MUKERJI: Objection to form.

THE WITNESS: I would like to look at both and -- and understand what was known at the time by one of ordinary skill and conclude from that that set of things.

BY MR. CHEN:

Q. All right. Following the etch of the plug contact openings, Doshi talks about the formation of plugs within those plug contact openings; correct?

A. Uh-huh.

Q. And then it says that if you were, for example, forming a DRAM circuit, you would also have to open up bit line contact openings; correct?

A. Which line are you at?

Q. Beginning at line column 10 line 31.

A. Uh-huh.

Q. And the formation of the bit line contact openings is effectively the same as the formation of the plug contact openings; correct?

A. Well, I'd have to look a little more closely at that because I didn't really concentrate on this part.

Q. Okay.

A. When I was studying this patent, I was more interested in the plug contact because that's really where the issue appears.

Q. So you don't have an opinion as to whether the formation of the bit line contact opening is the same as the formation of the plug contact opening; correct?

A. Give me just a minute, please. (Reviewing document).

I'm sorry. I'm taking some time to interpret the numbers in 3i. (Reviewing document).

Okay. I'm sorry. Can we come back to the question now about the bit line contact?

Q. My question was simply that whether you had provided any opinions about the formation of the

bit line contact opening.

A. No, I don't think so.

Q. Okay. And so you don't have an opinion as to whether the formation of the bit line contact opening is the same -- or you don't have any opinions as to whether the process used to form the bit line contact openings is the same as the process used to form the plug contact openings; correct?

A. I have not looked at the description of the bit line contact etch. I read it, but I didn't pay a lot of attention to it.

Q. Okay.

THE REPORTER: Exhibit 7.

(Document marked, for identification purposes, as Rubloff Exhibit No. 7.)

BY MR. CHEN:

Q. Okay. I've asked the court reporter to mark as Exhibit No. 7 patent number 5,770,498, which I believe is referred to as the Becker reference.

Dr. Rubloff, is Exhibit 7 one of the patents that you selected to be used in Samsung's IPR of the '997 patent?

A. Yes.

Q. And you did that selection yourself; right?

A. Yes.

Q. Which was about six months ago, roughly?

A. Whenever it was. (Laugh).

This is the one that was referenced by the IPR board somehow as not having the same stature as the Doshi. I don't -- I didn't quite understand that. But it was my selection, yes.

Q. All right. I also want to kind of do something similar to what we did with Doshi, kind of walk through the process that's disclosed in the Becker reference.

I believe the discussion of the process begins at column 4 line 9.

A. (Reviewing document).

Q. Again, I think the first step during the formation is to form the isolation regions; correct?

A. Right. The field oxide 16.

Q. And then Becker describes the formation of the gate electrode beginning at line or column 4 line -- roughly around line 22; correct?

A. Uh-huh.

Q. Does Becker describe the etch process used to form the gate electrode structure?

A. (Reviewing document). Well, line 22.

"Transistor gate electrode gate 18 is formed by successively depositing or 'stacking' layers of polysilicon 20, tungsten silicon 22 and silicon nitride 24 over thin gate insulating layer, and then patterning and etching those layers to expose substrate 12 at the desired locations of the source and drain for the access transistors."

That's polysilicon -- polysilicon gate.

Q. And my question was: Does Becker describe the specific etch process used to form the gate electrode structure?

A. Oh, you mean the etch gas and the power and all that stuff?

Q. Or even what type of etching process is used.

A. Well, what he says is these layers which are deposited and patterned and etched using conventional methods well known in the art.

Oh, I'm sorry. That, no.

"Then patterning and etching those layers to expose substrate." Yeah. Yeah. These layers. Yeah, this is line 25 to 29 or something.

Q. What are some of the conventional methods of etching known in the art in this time frame?

A. Reactive-ion etching would be most common, I think.

Q. Are there other types?

A. Well, you want to define the gate electrode by an anisotropic process. So it would be, in this time frame, reactive-ion etching would be common, but there are other configurations of equipment that could do that. Inductively coupled plasma, for a while ECR plasma, electron cyclotron resonance plasma, which are high density plasma etching techniques.

Q. And all of these other etching

techniques are considered conventional methods well known in the art?

A. Yes.

Q. After the formation of the gate electrode, Becker describes the next step as implantation of impurities into the substrate; correct?

A. Uh-huh.

Q. What is the purpose of this implantation step?

A. Well, the transistors require doped regions to make a PNP or an NPN transistor. So these regions 28 are the regions that with the gate electrode in place and the field oxide 16 in place, having cleared the gate stack material from the region between those two things, the ion implant 26 would form these doped regions 28. And to have an active device, you have to have doped regions.

Q. But those doped regions 28 are not the source/drain regions; correct?

A. Some of them will be.

Q. Well, the reason I say that is because

in the patent at column 4 line -- beginning at line 40 --

A. I'm sorry. Where?

Q. Column 4 beginning at line 40, the patent says:

"The resulting doped p-regions 28 extend into the channel area between the subsequently formed source and drain for each access transistor."

So I'm wondering whether that indicates that channel region or the doped p-region 28 is something that's different from the subsequently formed source/drain.

A. Well, notice that the regions 28 extend under the gate electrode; right? And so that's -- I think that's a design choice made for designing the dopant profile of the transistor in this case.

Q. So --

A. And that would be formed, I believe, by annealing to activate the dopants that were implanted.

Q. So is the region 28 different from the

source/drain region?

A. I don't think so. I don't recall if this is something atypical or unusual.

Q. But the source/drain region has not yet been formed at this step in the process; correct?

A. Yeah. I have to look at this more closely. I just don't remember how this part goes. It's not the part I was most interested in for the '997 patent.

(Reviewing document). It's a more complicated structure. I'm sorry. I hadn't remembered the details of that because I was focusing on other parts.

(Reviewing document). Okay. I'm sorry. I have lost the question.

Q. You know, it wasn't controversial.

I was just asking whether region 28 is part of this. Well, actually --

A. It's not --

Q. -- I'll ask you the exact question that I asked before the long pause.

At this particular step in the process

following the formation of region 28, the source/drain regions have not yet been formed; correct?

A. (Reviewing document). Yes, I think that's right.

Q. Okay.

A. 32a and b are the source/drain regions.

Q. Okay. Following the formation of the p-regions 28, the next step in the process is the deposition of the spacer insulating layer 30; correct?

A. Okay.

Q. What is the spacer insulating layer?

A. 30 is nitride; right?

Q. What is the function of that layer?

A. Well, the reason Becker was chosen is that the structure you see in Figure 4 corresponds to the way the '997 patent and the Doshi reference -- the Doshi patent etch a self-aligned contact through BPSG to an etch-stop layer of nitride in the second step going through that to make contact to the substrate, source/drain

contacts, and during that process leaving a sidewall spacer of nitride.

That was the part I considered relevant to the '997 patent here. The rest of the details of the dopant profiles and so on I didn't consider as relevant to '997.

Q. Okay. So when the spacer insulating area is first deposited, it is deposited, according to Becker, in the range of 600 to 2,000 angstroms; correct? That is at column 4 line 46.

A. Okay.

Q. And after it's deposited, that layer is then thinned in certain regions to the range of 50 angstroms to 400 angstroms; correct?

A. Yes.

Q. Okay. And the regions that are thinned are the portions of the spacer insulating layer above the gate electrode and above where the source/drain regions are to be formed between the gate electrode as shown in Figure 3; correct?

A. Uh-huh.

Q. The thickness of the spacer insulating

layer that is on the sidewalls of the gate are not thinned and remain close to the original deposition thickness of 600 to 2,000 angstroms; correct?

A. Uh-huh.

Q. I'm sorry. Uh-huh. Is that a yes?

A. Yes. I'm sorry.

Q. Why is the thickness of the spacer insulating layer over the -- what will later be the source/drain regions, why is that portion of the spacer insulating layer thinned?

A. (Reviewing document). Gee, I've looked at this, this aspect.

Q. Maybe it will help you. I can refer you to column 4 line 66 through column 5 line 5.

A. (Reviewing document). Well, as it says here -- thank you -- column 5:

"Under etching spacer insulating layer 30 to leave a thin layer of nitride material provides a diffusion barrier during subsequent processing."

Nitride is a good diffusion barrier.

Q. Now, following the formation of the

spacer insulating layer and then the subsequent thinning of that layer in certain regions, Becker describes a process where lightly doped drain implants are used to form the source and drain regions; correct?

A. Uh-huh.

Q. All right. And that --

A. Yes.

Q. -- begins at column 5 line 6; correct?

A. Yes.

Q. Okay. How are the impurities here implanted into the source/drain regions?

A. Through the nitride, the thinned nitride.

Q. So won't the thinned nitride interfere with implantation?

A. No.

Q. Why not?

A. In fact -- well, the implantation depth can certainly be greater than the thinned nitride thicknesses. You can adjust the implantation energy to get the penetration and compensate for the

presence of the nitride that's there.

In fact, these kinds of layers nitride used in them is not crystalline, it's amorphous. And so very often when you do an implantation, you want to make sure you're not channelling along the crystalline axis of the substrate. And so you want to put something that the -- that the implant ions go through which randomizes to some extent what their trajectory is so they don't channel deeply into the crystalline lattice.

Q. But the implantation parameters you use with the presence of the nitride layer there as opposed to the parameters used without the nitride will be different; correct?

A. Yeah, somewhat different.

Q. Because you have to compensate for your ability to penetrate through the nitride layer?

A. Yeah. The energy loss of the ion going through different materials is quite well understood.

Q. Okay.

A. So you would know, okay, I wanted the

peak position to be of the implant distribution, kind of Gaussian, to be so far below the silicon surface, but I'm going to lose this much energy going through the nitride. So I'll just change the implant energy.

Q. Okay. The thickness of that nitride layer will also affect the parameters of the implantation that you use to achieve your targeted dopant profile; correct?

A. Yeah. Unless it's thin enough it doesn't matter.

Q. And if you add another layer on top of the nitride layer, that too would affect the implantation parameters that you need to use to achieve your dopant profile; correct?

A. It could.

Q. In fact, the thicker the materials covering this substrate that is -- sorry.

The more material you have covering the substrate, the higher the implantation energy or impurity dosage you would need to use to achieve the same dopant profile; correct?

A. Not dose, but energy.
Q. Okay. Only energy?
A. Energy.
Q. Okay. So --
A. I'm sorry. Energy to get the right depth into the substrate, but you may lose some of that that gets buried in the thin layer on the top.
Q. Right.
A. And so you may have to change the dose a little too.
Q. Okay. So the material covering the substrate -- would the amount of material covering the substrate will affect both the implantation energy required as well as the impurity dosage required to achieve your targeted dopant profile for the source/drain region?
A. Yes, it could.
Q. Okay. In this step where Becker is performing the lightly doped drain implants, what is the function of the spacer insulating layer?
A. You're referring to which figure?
Q. Figure 3.

A. And you're talking about the spacer insulating layer --

Q. Yes.

A. -- which is 18 on the sidewall of the gate electrode?

Q. I think it's layer -- I think it's --

A. I'm sorry.

Q. -- 30.

A. 30. 18 --

Q. 18 is the gate electrode.

A. -- is the top of the gate electrode. 30. I'm sorry.

Q. Yes.

A. So 30 on the sidewall of the gate electrode will be an implant mask, part of an implant mask.

Q. Okay. So it's a doping spacer?

A. It's a doping spacer.

Q. Okay. Could you explain again how the portion of the spacer insulating layer 30 on the gate electrode -- on the sidewall of the gate electrode acts as a spacer during this step?

A. In Figure 3, so 40 are the ion implant trajectories.

Q. Right.

A. They are coming in a directional fashion into the substrate 12, and they will penetrate through the thinned nitride number 30, but they won't penetrate through the sidewall spacer 30 next to the gate electrode.

And the consequent dopant profiles that you get will be determined by that and by whatever annealing process and associated thermal diffusion the dopants happen during implant activation anneal.

Q. So it's creating space between where you're doing your implantation and the gate electrode?

A. Right.

Q. And so the spacer insulating layer 30 at this stage in the process is a spacer in the context of how you construed it for the '997 patent; correct?

A. Uh-huh.

Q. Is that a yes?

A. Yes.

Q. All right. Following the implantation step -- and, actually, you know, before we go on, I don't know how long we've been going.

MR. MUKERJI: It's been just a few minutes past an hour.

MR. CHEN: Okay. You want to take a quick break then?

MR. MUKERJI: Sure.

(Recess - 4:51 p.m. - 5:03 p.m.)

BY MR. CHEN:

Q. The Becker process does not disclose the thermal oxidation of the sidewalls of the polysilicon or the substrate for the diffusion regions; correct?

A. (Reviewing document). That's right.

Q. Okay. If you turn to Exhibit 5, which we introduced earlier in the day. This is the Wong reference --

A. Right.

Q. -- that you referred to on page 47 of your declaration.

A. Yeah.

Q. So the Wong reference is the one that teaches the use of thermal oxidation to repair damage created by reactive-ion etching; correct?

A. Yes.

Q. Does Wong address other forms of etching other than reactive-ion etching?

A. (Reviewing document). Not other forms of etching, but does address channel ion implantation as a source of defects, but that's not -- it's not really an etching process.

Q. Does Wong teach that thermal oxidation will also help repair defects created through channel ion implantation?

A. Yes.

Q. Where does it teach that?

A. At least in the abstract, polysilicon sidewall oxidation is also necessary to protect the thin oxide from degradation by source/drain ion implantation.

Q. Okay. But those are two different forms of protection; correct?

A. Which two?

Q. Well, the benefit of the thermal oxidation for repairing defects caused by reactive-ion etching is that -- well, let me rephrase that.

What Wong teaches is that thermal oxidation can be used to repair defects that are caused by reactive-ion etching; correct?

A. Uh-huh.

Q. What Wong teaches for the polysilicon sidewall oxidation is that it can help create a thin oxide that will then protect the source/drain region from subsequent damage by ion implantation; correct?

A. That certainly isn't how I read the abstract.

Q. Okay. Well, so then are you saying that the sidewall oxidation repairs damage to the source/drain regions that were created during ion implantation in the same way that it would repair damage created by reactive-ion etching?

A. I'm sorry. You said sidewall oxidation of a polysilicon to protect the thin oxide during

ion implantation.

Q. Right.

A. Is that what you said?

Q. Well, I was wondering whether the benefits of the thermal oxidation are different, I said, as applied to reactive-ion etching and --

A. Yes.

Q. -- as applied to ion implantation.

A. Well, according to the abstract, reactive-ion etching to define the polysilicon gate hurts the quality of the thin oxide. But if you then do sidewall oxidation to the polysilicon, you can reduce that problem.

Q. Because it will repair the damage --

A. Right.

Q. -- that had already occurred?

A. (Reviewing document). Yeah.

So -- so the conclusion, I don't remember the ion implantation part because it's not the part I focused on, but the conclusion in this abstract is that the sidewall oxidation does help protect the thin oxide, meaning the gate oxide, from

degradation during implantation where you're usually using the gate as a mask for ion implantation. So the ions are going straight at the edge of the gate oxide where the RIE damage could be. It's the same location.

Q. And that process isn't repairing damage that has already occurred but, rather, preventing damage from occurring; correct?

A. Yes.

Q. All right.

A. Or at least primarily so.

Q. Okay. Does Becker disclose the potential defects that will be created through reactive-ion etching of a gate electrode?

A. (Reviewing document). I don't think so. I'm just reviewing it again.

Q. Looking at Exhibit 5, the Wong reference, if you turn to page 12 and we look at Table 1 at the top of page 12.

A. I'm sorry. Can you hold just a minute --

Q. Sure thing.

A. -- while I finish scanning this?
(Reviewing document). I'm sorry.
Q. No problem.
A. Please go ahead.
Q. Okay. I was -- if you could turn to Exhibit 5, which is the Wong reference --
A. Uh-huh.
Q. -- page 12. And you look at Table 1 above.
Does Wong teach that the defect density for plasma etching is significantly lower than the defect density for reactive-ion etching?
A. Well, what she did was only RIE here. That's the only way you can make the gate. I don't know what process you'd be referring to as "plasma etching." RIE is a plasma etch process.
Q. Okay. Well, if you look at the table, the second line says:
"Polysilicon gate 60 mil dot plasma etched."
A. (Reviewing document). I'm sorry.
Q. So --

A. You're right. On page 158, she mentions "defined by RIE or plasma etching" and 60 mil dots are big. That's pretty big.

Okay. So the defect density in plasma etching is certainly higher than it is with RIE.

Q. Oh, it's higher than it is?

A. Oh, wait. I'm sorry. I was looking at aluminum gate. Which are you referring to: A general statement for aluminum or polysilicon gate?

Q. For the polysilicon gate.

Let me re-ask the question.

Does Wong teach that the defect density for plasma etching is significantly lower than the defect density for reactive-ion etching?

A. No.

Q. Why not?

A. Well, the plasma etch 60 mil dot on polysilicon gate is 26 per centimeters squared. If you look at the edge of the field oxide with RIE, it's 19, and if you look at the edge on the gate oxide, it's 88. I don't think that's a clear conclusion.

Q. Okay. If you turn to page 10 Figure 2, I think you can see the distinction between 2a, 2b, and 2c.

A. (Reviewing document). Yes.

Q. So is it fair then to say that the second line of Table 1 on page 12 describing plasma etching and Figure 2b, with reference to Figure 2b, is comparable to the fourth line in that table which is describing reactive-ion etching with reference to Figure 2b?

A. (Reviewing document). Well, the descriptors are a little confusing because it appears to compare RIE the fourth line to plasma the second line edge on gate oxide to 60 mil dot. I think they are the same thing. And the conclusion from that could be that 26 is notably less than 88.

Q. In your experience, does plasma etching cause fewer defects than reactive-ion etching?

A. I don't have any direct experience comparing them because most of the time people do, where I've -- where I've been involved, it's all RIE. So we don't look at plasma etching because you

can't define things with it.

Does it make sense that it would be less? The answer to that is yes because reactive-ion etching imparts tens or hundreds of volts of ion energy to the plasma species that are doing the etching and, therefore, they have a lot more kinetic energy to impart and do damage. Whereas, plasma etching is typically lower energy ions, considerably lower.

Q. What do you mean when you say you can't define things with plasma etching?

A. It's not directional. It's not an anisotropic.

Q. Oh.

A. By definition, plasma etching means you don't bias the substrate where the wafer is to accelerate DC the ions so they have hundreds of volts, for example, of energy when they do the etching. That's how you get anisotropy.

Q. Okay.

A. So basically plasma etching is irrelevant here. Irrelevant to the technology.

Q. Dr. Rubloff, did you draft the declaration by yourself?

A. The declaration was drafted by the attorneys and my specification. We had talked to all of these issues and -- well, part of it, part of the text was drafted and then I came in. And we sat for hours and looked through it and went through every line to decide, am I comfortable with that? But it was my decision what those statements were.

Q. And when were you --

A. I needed somebody to help write this thing.

Q. Sure. When were you first retained to work for Samsung on these IPRs?

A. My guess was six months ago, but I don't know.

Q. Okay.

A. Something like six months.

Q. Probably a little longer than six months since your declaration is dated December 16 --

A. Oh.

Q. -- 2014.

A. Yeah. Then I've -- then I've put it in the back of my memory.

Q. Okay. You don't remember what exact date you were retained?

A. No. No.

Q. Okay. I want to just --

A. For the drafting of the declaration, when I said that there was help coming from the attorneys to draft it, I'm talking about the typing. We had gone through all the arguments. I decided what it should say. I asked them to put it in the right order because otherwise from a legal point of view, it may be hard to follow. And then we went through it in great detail.

I guess I was confused by what you meant "drafting." I didn't type the first version.

Q. Sure.

A. But I directed it.

Q. I want to ask you another question, kind of returning back to Doshi. And this is about, you know, the issue of the nitride layer 30 and

whether it remains on the sidewalls of the gate electrode.

Let me refer to you the right section of the patent.

The step is described at column 9 beginning at around line 56, extending through column 10 line 3.

And I understand it's your opinion that the etch process described here would etch away certain portions of the nitride layer, but would leave some of the nitride layer on the sidewalls of the gate electrode; right? That's your opinion; correct?

A. Yeah. The etch process will remove the nitride from the horizontal regions and leave nitride on the sidewall.

Q. Okay. If you -- if the nitride -- does the amount of nitride that is removed depend on the specific parameters of the nitride etch process?

A. The nitride that's removed from the sidewall?

Q. Yes.

A. Well, the proper way to ask that question is to ask whether the anisotropy depends on the parameters of the process.

Q. Okay.

A. Right? Because you're going to remove from the -- from the horizontal areas at the source/drain and at the top of the gate, and you're going to remove a lesser amount from the sidewall because it's directional etching.

But directional by how much? So what's the etch rate ratio sideways compared to vertically? And that will depend to some extent on the details of the process you use.

For example, the possible -- the gas chemistry. So the ions that are involved. The voltage, the self-bias voltage that determines what the ion energies are when you're etching and pressures then and things like that.

Q. So it is possible to have an anisotropic etch that will remove the entire nitride layer including the portions that are on the sidewall of the gate electrode; correct?

A. That would be called an isotropic etch because the nitride was put down by a CVD process that puts the same thickness on the sidewall as on the top and the bottom. So if you say that it removes everything from the sidewall when you're clearing the bottom, that means the horizontal and vertical etch rates are the same. That's called an isotropic etch.

Q. But if you extend that -- if you were performing an anisotropic etch and you extended that etch for a longer period of time, wouldn't you remove then the material on the sidewalls?

A. Well, if you have a vertical etch rate of a hundred and you have a side -- a horizontal etch rate of one and you over-etch by a factor of a hundred, eventually you'll get there, but that's not a relevant condition. I mean, it's not -- it's not what people do.

People use timed etches in the worst-case and institute process sensors to tell when they're done with the etching. It's called endpoint detection in etching. You can measure

optical emission from the plasma that changes when you clear the nitride or other techniques to do that.

Q. When you're -- when you have a very thin layer of nitride, how do you control the amount of nitride material that's left on the sidewalls?

A. I don't understand the question.

Q. Well, when you're performing an etch, there's a certain amount of tolerance in the etch; correct?

A. Well, generically speaking, anything has that, but I still don't understand the question.

Q. So if you had a thin layer of nitride and your intent was to keep some of that nitride on the sidewall, are there certain precautions that you would need to take to make sure that the material left on the sidewall was intact?

A. Was in fact?

Q. Intact.

A. Intact. I don't -- this is a hypothetical example where, from what you asked, the only issue is, I start with thin layer nitride on

the sidewall.

Q. Right.

A. Can I prevent it from ever being etched? I just don't understand the context of the question.

Q. Is it your opinion that in every case where you have anisotropic etch of a nitride layer --

A. Isotropic.

Q. Anisotropic.

A. Okay.

Q. In every case where you're performing an anisotropic etch of a nitride layer covering a gate electrode structure and the diffusion regions to the sides of that gate electrode structure, that anisotropic etch of that nitride layer will leave some material on the sides of the gate electrode, some nitride material on the sides of the gate electrode?

A. If you have an anisotropic etch and you clear the horizontal surface, for example, at the diffusion region, then as long as you stop at about

the point where you've cleared it or 10% over-etch or something like that, you will have something, have nitride left on the sidewall.

Q. Okay. But if you continue to etch past the point of simply just removing the nitride on the horizontal regions, you potentially would remove the nitride material that's left on the sidewalls; correct?

A. The question was asked and answered already.

Q. And what was the answer?

A. The answer was that if you have an anisotropy of -- I gave the example of one to a hundred. So a hundred times faster on the vertical direction than on the sidewall, you would have to etch a very long time, a huge over-etch that is far beyond what anyone could possibly make the mistake of doing, in order for that low rate of one on the sidewall to remove the same initial thickness of film produced by the nitride CVD process.

Q. In your experience with anisotropic etches, what is the typical ratio of the vertical

etch as compared to the horizontal etch?

A. It depends very much on the process. Some processes are -- I mean, you can -- you can easily find, you know, two to five or 10 as an anisotropy ratio, but you have DRAM capacitor structures in all of these devices that have trans-capacitors that have aspect ratios of a hundred.

So now you're talking about very high anisotropy of order of a hundred or more.

Q. Okay.

A. So it can be very high, and it's not just a question of the distribution of impinging ions this way and this way. There's much more reactive-ion etching chemistry involved because a part of the etching in the vertical direction can lead to the formation of films on the sidewalls that further suppress the sideways etching. So it depends on the ion -- ion chemistry.

Q. Okay. But the range is -- there's a wide range?

A. There's a wide range.

Q. Okay. And that range that you gave is roughly two to five to one to one hundred?

A. Yeah, something of that order.

Q. If the range was two to five, then you would not need to extend your anisotropic etch that long to remove the material on the vertical sidewall; correct?

A. Well, you know that you need, let's say, a hundred seconds to do the etch on the diffusion region. So if it's five, you have to do 500; right? You're not going to make that kind of mistake. One of ordinary skill would never do that.

Q. I'm sorry. I'm not sure if I got the math right.

You said if you needed a hundred seconds and the ratio was two to five, you would need to do 500 seconds?

A. If the ratio was five.

Q. Right.

A. You'd need to do 500 seconds.

Q. Okay. If the ratio was two to five, how much time would you need?

A. 200 to 500.
Q. So --
A. But --
Q. -- 250 seconds?
A. Yeah, something like that. But no one is going to do this. You know you want a sidewall there. That's what the invention of Doshi is about and --
Q. But -- sorry.
A. -- in '997.
Q. Did you say that the invention in Doshi is about forming those sidewalls?
A. It's part of what's done.
Q. But it's not mentioned anywhere in the text of Doshi?
A. We talked about that already.
Q. Right.
A. I think it's very clear that that's what Doshi is doing.
Q. I know. I understand. But you said that that's what the invention of Doshi is about.
A. Right.

Q. And I just want to make sure I understand it because it's not actually mentioned anywhere in the text of Doshi; right?

MR. MUKERJI: Objection to form.

THE WITNESS: I'll have to continue to disagree about whether Doshi teaches it properly.

MR. CHEN: Okay. Okay. Let's take a quick break and then let me just review my notes a little bit. It shouldn't be long. Five minutes.

(Recess - 5:41 p.m. - 5:47 p.m.)

THE REPORTER: Exhibit 8.

(Document marked, for identification purposes, as Rubloff Exhibit No. 8.)

MR. MUKERJI: Are you moving to a different declaration?

MR. CHEN: I am.

MR. MUKERJI: Before you do that, I need to ask a couple questions of him.

MR. CHEN: Oh.

MR. MUKERJI: So, counsel, is your

cross on the '997 patent complete?

MR. CHEN: Yes.

MR. MUKERJI: Okay. I have just a couple of questions for him on that patent.

EXAMINATION

BY MR. MUKERJI:

Q. Dr. Rubloff, I'd like you to pull out what had been marked as Exhibit 3 earlier today, and it's titled "The Errata, Declaration of Gary W. Rubloff, Ph.D."

Mr. Chen had marked that earlier today, and I'm not sure if the discussion really got to it.

Can you just tell us what this errata is, please, sir?

A. There's a paragraph in the -- in my declaration for the '997 patent that we just talked about, and the paragraph mistakenly refers to the -- in paragraph 11 the '893 patent and the filing date in 1996, and it really should have been talking about the corresponding '997 patent with a 1999 filing date in that paragraph 11.

It was just a clerical error probably

because of copying from one to the other.

Q. In conducting your work on the '997 patent, did you apply this information about the '893 patent, or did you use the '997 patent information that you described in this paragraph?

A. No. I used the '997 information, but I can imagine, you know, having -- having talked about these issues and deciding what I thought was the appropriate position for me to take on these issues and which of the prior art publications to use in my declaration, I then needed help to -- to type these things in and give me something to work with.

And I can easily imagine that knowing there were three things, there's a lot of duplication of paragraphs between the three declarations, and I can easily imagine someone copied it. I don't know who typed this stuff. But copied it and didn't catch the change from that one. And looking through them took a long time and I just missed it.

MR. MUKERJI: Pass the witness.

EXAMINATION

BY MR. CHEN:

Q. So, Dr. Rubloff, I asked the court reporter to mark as Exhibit No. 8 your declaration submitted in connection with Samsung's IPR of the '244 patent.

Please take a brief moment to look over this document. I just want to make sure this is your declaration.

A. (Reviewing document).

MR. MUKERJI: Counsel, while he's doing that, just as a housekeeping matter, so are you restarting the exhibits for each different patent or are we -- what's the plan?

MR. CHEN: I'm continuing using. I mean, this is 8. So.

MR. MUKERJI: Okay.

MR. CHEN: I don't -- I mean, I only introduced one exhibit I think for his background, his CV. So.

MR. MUKERJI: That's fine. I just want to make sure everyone is on the same page.

THE WITNESS: (Reviewing

document). Okay.

BY MR. CHEN:

Q. And so this is your declaration submitted in connection with Samsung's IPR for the '244 patent; correct?

A. Yes, this is my declaration.

Q. And does this declaration contain any and all relevant opinions you have regarding the issues related to Samsung's IPR for '244 patent?

A. Yes.

Q. Do you have any opinions regarding issues relevant to Samsung's IPR of the '244 patent that were not included in your declaration?

MR. MUKERJI: Objection to form.

THE WITNESS: You're talking about Samsung's petition?

BY MR. CHEN:

Q. Yes.

A. So I think I've seen that, but I haven't really read it. I've concentrated on my declaration.

Q. Do you have any opinions regarding the

validity of the '244 patent that were not included in your declaration?

A. No.

Q. Are you aware of any errors or omissions in your declaration?

A. Not at this time.

Q. All right.

A. Unless we find one. Another typo. (Laugh).

THE REPORTER: Exhibit 9.

(Document marked, for identification purposes, as Rubloff Exhibit No. 9.)

BY MR. CHEN:

Q. Okay. I've asked the court reporter to mark as Exhibit 9 patent number 6,150,244 titled "Method For Fabricating MOS Transistor Having Raised Source and Drain."

You referred to this exhibit as the '244 patent for this deposition.

Did you read the '244 patent?

A. Yes.

Q. When did you first read the '244

patent?

A. Well, I guess it was more than six months ago. (Laugh). Maybe a year ago.

Q. After you were retained by Samsung to work on these IPRs?

A. Yes.

Q. And you understand the '244 patent?

A. Yes.

Q. Okay. What would you say is the point of novelty of the '244 patent?

A. Well, if I believe, as I do, that there is prior art which describes all the claims and invalidates the patent, then it's hard for me to call it novel, but the claim is and it's purported to be novel in the domain where the prior art would also be considered novel, I consider novel in prior art, and it's a prescription for how to form a shallow junction.

Q. A shallow junction. Is that the same thing as a raised source and drain?

A. It's the goal of a raised source and drain. A goal of a raised source and drain.

Q. What is a raised source and drain?

A. Well, I think what's more important is to understand what's the motivation for the shallow junction.

Ion implantation, the standard technique or conventional doping techniques, don't allow the design of source and drain profiles to be as shallow and, therefore, as high performance as one would like.

So for quite some time the community has been looking for ways to form very shallow junctions. We have conferences about that that have been going on for decades now.

And so I think that the raised source and drain provides a vehicle, as described in this patent and in the prior art, for producing dopant atoms above the crystalline silicon surface that can then be allowed with proper thermal treatment to diffuse shallowly into the crystalline silicon surface.

And so if you imagine that I look at what the drain and what the source look like, it's

silicon that's heavily doped or reasonably doped, and if I had some of that above the crystalline surface in the form of polysilicon with dopants, that would be a very nice source for essentially contact doping from that raised source/drain, looks like a raised source/drain -- looks like a source/drain material into the crystalline silicon.

Q. Okay. So what you're saying is that the raised source/drain refers to the dopant or impurities that are above the silicon substrate that are then subsequently diffused into the substrate to form the shallow junction following a heat treatment; is that --

A. Yes.

Q. So the raised source/drain doesn't actually refer to the source/drain that is then ultimately formed in the substrate; correct?

A. No. The raised source/drain is the source part -- I'm sorry for using "source" in two ways -- is the part which is above the crystalline silicon surface.

Q. Okay. And that is how you understand

the term "raised source/drain" as it is used in the '244 patent?

A. Yeah. It says -- it says here, for example, in '244.

"There is plenty of room for improvement in the fabrication of metal oxide devices having raised source and drain electrodes."

Q. Which paragraph are you looking at in your declaration?

A. Oh, that's the end of 17.

Q. And the '244 patent describes or claims a process for fabricating a semiconductor device; correct?

MR. MUKERJI: Objection to form.

BY MR. CHEN:

Q. Let me re-ask that.

The '244 patent claims a process for fabricating a semiconductor device comprising a raised source and drain; correct?

A. That's what claim 1 says. Introduction to claim 1.

Q. And claim 1 lays out a sequence of

steps for that process; correct?

A. No. It lays -- lays out a list of steps involved in that process, but not a sequence.

Q. Okay. So it's your --

A. Not necessarily a sequence.

Q. Okay. So is it your opinion then that claim 1 does not list a sequence of steps for that process?

A. It lists a set of steps that are part of that process, but it does not tell uniquely what the order of that is. So I can't say sequence.

Q. Is that true for every limitation of claim 1?

A. You mean for each of the forming, forming, forming --

Q. Yes.

A. -- when you say "limitation"?

Q. Yes.

A. No. There are some that you couldn't switch around. I mean, you couldn't randomly change these, but there is flexibility that would have been known to one of ordinary skill.

Q. Okay. Some of these steps or limitations have to be performed in a specific sequence; correct?

A. Well, normally would be performed in a specific sequence. I don't -- I don't at this point have alternative ways to move some of them around --

Q. Okay.

A. -- in mind.

Q. Your opinion that some of these limitations can be performed out of their listed order is limited to the limitation beginning with "removing a top portion of said fourth dielectric layer" and then the subsequent limitation "forming on the substrate a pattern second resist layer"; correct?

A. Yes.

Q. Okay. As far as you understand, the rest of the limitations or steps in claim 1 should be performed in their listed order; correct?

A. (Reviewing document). I'm just looking through it one more time to be sure. Yes.

Q. And generally when we're talking about

a semiconductor process, the order in which the different steps in the process are performed will affect the structure of the device that's being manufactured; correct?

MR. MUKERJI: Objection to form and also outside the scope.

THE WITNESS: Well, what you get depends on how you do it. In a general sense, yes.

BY MR. CHEN:

Q. So the sequence in which you perform a list of steps will affect the resulting structure that is being manufactured; correct?

MR. MUKERJI: Objection to form and also to scope.

THE WITNESS: There are cases where the order might be changed and changes in structure would be minimal. So I wouldn't make a blanket statement that you always change the structure by changing the order.

BY MR. CHEN:

Q. But in most cases, if you change the order, you will change the structure?

MR. MUKERJI: Same objections.

THE WITNESS: I don't know how to audit "most." I can think of cases where it won't change it.

BY MR. CHEN:

Q. Okay. For example? Could you give me an example?

A. A laminate structure. Suppose I want a laminate structure of -- I'm going to put a thin film structure in place maybe for optical interferometry applications, or something like that, and I have AB, AB, AB or ABC, ABC, ABC. And I could switch some of those, and it wouldn't make any difference.

Q. But the structure of what you're laminating would be different, though. Whether it makes a difference or not is a different issue; right?

A. Yeah. I need to think about this. I mean, a question like that --

Q. I'm not trying to --

A. -- asks for speculation that -- that

requires some dreaming to think about whether there are exceptions or there are examples that could be given.

Q. All right. Sitting here today then, can you -- you cannot think of a situation where changing the order of the steps in a semiconductor manufacturing process does not affect the ultimate structure of what you're manufacturing?

MR. MUKERJI: Objection. Outside the scope.

THE WITNESS: I don't agree with that because your suggestion is that I cannot think of that. I would need to think pretty hard to see if I can think of an example.

BY MR. CHEN:

Q. Okay.

A. And I probably could think of one.

Q. But you would need to -- let me ask it like this.

Have you provided an opinion in your declaration about whether changing the order of steps in a semiconductor process will change the

structure of a device that's being manufactured?

A. Well, how much change in structure should I use as the metric for answering yes or no?

Q. Any change in structure.

A. Well, does that mean an angstrom of change in the thickness of one of the layers? Does that mean what?

Q. Did you provide an opinion in your declaration about whether changing the structure -- order of steps in a process will change the structure of the manufactured device?

A. I don't think so. I think I provided an opinion that there are ways in which you can -- you can meet the claims here in the '244 patent with different orders of claim -- of the two components in claim 1.

Q. Okay.

A. I can make that structure and, whether it looks a little bit different or not, it satisfies all of the components of claim 1. So I can change the order.

MR. MUKERJI: Gentlemen, I don't

mean to interrupt this fascinating discussion, but I think we have hit seven hours. So we have sucked the marrow out of the day. Is that about right? We hit seven hours, Madam Court Reporter?

I don't want to deprive anyone of a minute, you know, but --

MR. CHEN: You know, it's okay. I don't want to put you on the spot. I think we're close. We'll continue this tomorrow. It's going to be just as fascinating tomorrow as it is this evening. So.

MR. MUKERJI: All right. Everyone have a good evening.

(Signature having not been waived, the taking of the deposition adjourned at 6:10 p.m., to reconvene Wednesday, August 19, 2015, at 9:00 a.m.)

* * *

CERTIFICATE OF COURT REPORTER

UNITED STATES OF AMERICA)

DISTRICT OF COLUMBIA)

I, DENISE D. VICKERY, the reporter before whom the foregoing deposition was taken, do hereby certify that the witness whose testimony appears in the foregoing deposition was sworn by me; that the testimony of said witness was taken by me in machine shorthand and thereafter transcribed by computer-aided transcription; that said deposition is a true record of the testimony given by said witness; that I am neither counsel for, related to, nor employed by any of the parties to the action in which this deposition was taken; and, further, that I am not a relative or employee of any attorney or counsel employed by the parties hereto, or financially or otherwise interested in the outcome of this action.

Denise D. Vickery

Notary Public in and for the
District of Columbia

My Commission expires February 14, 2018

DEPOSITION ERRATA SHEET

Our Assignment No. 173194

Case Caption: SAMSUNG ELECTRONICS CO. LTD. vs. HOME SEMICONDUCTOR CORPORATION

DECLARATION UNDER PENALTY OF PERJURY

I declare under penalty of perjury that I have read the entire transcript of my Deposition taken in the captioned matter or the same has been read to me, and the same is true and accurate, save and except for changes and/or corrections, if any, as indicated by me on the DEPOSITION ERRATA SHEET hereof, with the understanding that I offer these changes as if still under oath.

Signed on the _____ day of

_____, 2015.

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GARY W. RUBLOFF, PHD

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