

1 UNITED STATES PATENT AND TRADEMARK OFFICE

2 BEFORE THE PATENT TRIAL AND APPEAL BOARD

3 -----X

4 SAMSUNG ELECTRONICS CO. LTD.,

5 SAMSUNG ELECTRONICS AMERICA, INC.,

6 SAMSUNG SEMICONDUCTOR INC., and

7 SAMSUNG AUSTIN SEMICONDUCTOR LLC,

8 Petitioner,

9 V. Case IPR2015-00459

10 HOME SEMICONDUCTOR CORPORATION Patent 6,150,244

11 Patent Owner. Patent 6,146,997

12 -----X VOLUME I

13
14 DEPOSITION OF

15 GARY W. RUBLOFF, PHD

16
17 Washington, DC 20005

18 Tuesday, August 18, 2015

19
20
21 Reported by: Denise D. Vickery, RMR, CRR

22 Job No. 173194

Tuesday, August 18, 2015

9:04 a.m.

DEPOSITION OF GARY W. RUBLOFF, PHD, held at the
offices of:

FISH & RICHARDSON PC
1425 K Street NW, 11th Floor
Washington, DC 20005

Pursuant to notice, before Denise D. Vickery,
Registered Merit Reporter, Certified Realtime
Reporter, and Notary Public in and for the District
of Columbia.

A P P E A R A N C E S

For the Petitioner and the Witness:

FISH & RICHARDSON PC

1425 K Street NW, 11th Floor

Washington, DC 20005

202.783.5070

BY: INDRANIL MUKERJI, ESQ.

mukerji@fr.com

BY: DAVID L. HOLT, ESQ.

David.Holt@FR.com

For the Patent Owner:

TECHKNOWLEDGE LAW GROUP LLP

100 Marine Parkway, Suite 200

Redwood Shores, CA 94065

650.517.5200

BY: JERRY CHEN, ESQ.

jchen@tklg-llp.com

Also Present:

Ron Maltiel, RMG and Associates

I N D E X

EXAMINATION OF GARY W. RUBLOFF, PHD	PAGE
By Mr. Chen on 6,146,997	5
By Mr. Mukerji on 6,146,997	249
By Mr. Chen on 6,150,244	251

E X H I B I T S

RUBLOFF

EXHIBIT	DESCRIPTION	PAGE
No. 1	Curriculum Vitae	12
No. 2	Declaration of Dr. Gary W. Rubloff	125
	U.S. Patent No. 6,146,997	
No. 3	Errata Sheet	125
No. 4	U.S. Patent No. 6,146,997	130
No. 5	Process Induced Degradation of Thin	142
	Oxides, Wong	
No. 6	U.S. Patent No. 6,277,720 Doshi	159
No. 7	U.S. Patent No. 5,770,498 Becker	212
No. 8	Declaration of Dr. Gary W. Rubloff	248
	U.S. Patent No. 6,150,244	
No. 9	U.S. Patent No. 6,150,244	253

(Exhibits attached to transcript.)

P R O C E E D I N G S

- - -

GARY W. RUBLOFF, PHD

called for examination, and, after having been duly
sworn, was examined and testified as follows:

EXAMINATION

BY MR. CHEN:

Q. Good morning.

MR. MUKERJI: We should
probably -- I'm sorry to interrupt. We should
probably do introductions --

MR. CHEN: Sure.

MR. MUKERJI: -- since we don't
have a video camera and all that.

You want to go first?

MR. CHEN: Sure. Jerry Chen from
TechKnowledge Law Group representing respondent,
Home Semiconductor Corporation. With me is Ron
Maltiel, expert for Home Semiconductor Corporation.

MR. MUKERJI: Indranil Mukerji and
David Holt of Fish & Richardson representing the

1 petitioner and the witness here today. When I say
2 "petitioner," I mean petitioner in all four of the
3 RPIs that will be covered by this deposition or this
4 cross-examination.

5 I'll also note for the record
6 before we went on the record, counsel and I had a
7 discussion about apportioning the cross-examination
8 so it's clear which cross is for which declaration,
9 and I think we agreed to try to work together on
10 that.

11 BY MR. CHEN:

12 Q. Sure.

13 A. Am I supposed to introduce myself?

14 MR. MUKERJI: You'll be
15 introducing yourself all day.

16 THE WITNESS: Okay.

17 MR. MUKERJI: So we can get going.

18 BY MR. CHEN:

19 Q. Good morning, Dr. Rubloff.

20 A. Good morning.

21 Q. My name is Jerry Chen. I'm an attorney
22 with the firm of TechKnowledge Law Group. I

1 represent respondent, Home Semiconductor
2 Corporation. I'll be taking your deposition on
3 cross-examination today in connection with the IPRs
4 filed by Samsung against the Home patents.

5 In today's cross-examination, I'll ask
6 you questions related to the subject matter at issue
7 in those RPIs. You will need to answer my questions
8 truthfully and completely. The court reporter will
9 record my questions and your answers in writing.

10 As explained, if your attorney objects,
11 you may -- you must still answer all my questions.

12 You understand?

13 A. I understand.

14 Q. Okay. If you do not hear or understand
15 my questions, please ask me to repeat or clarify.
16 If you answer my questions, my assumption will be
17 that you understood the questions.

18 You understand?

19 A. Yes.

20 Q. And if you need a break, please let me
21 know and we'll take a break.

22 A. Thank you.

1 Q. Okay. Can you think of any reason that
2 might affect your ability to provide truthful and
3 complete answers to my questions today?

4 A. No.

5 Q. Okay. Do you have any questions before
6 we start?

7 A. No.

8 Q. Okay. Dr. Rubloff, could you please
9 state and spell your full name for the record?

10 A. Gary, G-a-r-y, Wayne, W-a-y-n-e,
11 Rubloff, R-u-b-l-o-f-f.

12 Q. Dr. Rubloff, are you being compensated
13 for your work on these matters?

14 A. Yes.

15 Q. What is your compensation?

16 A. For my time it's \$400 an hour, and I
17 think it's 600 an hour for deposition and testimony.
18 I'm not sure about that.

19 Q. Okay.

20 A. I don't really remember what our
21 agreement was.

22 Q. Okay.

1 A. But that's what it's been in
2 some previous times.

3 Q. Are you currently retained by Samsung
4 as an expert witness for other matters?

5 A. No, just the four things that are
6 today.

7 Q. Okay. Prior to these current matters,
8 these four IPRs, had you worked for Samsung on any
9 other matters?

10 A. No.

11 Q. How long have you worked as an expert
12 witness?

13 MR. MUKERJI: Objection to form.

14 THE WITNESS: You mean when was
15 the first date that I did anything like this? Is
16 that what the question is?

17 BY MR. CHEN:

18 Q. Sure. Yes. How long have you been
19 working as an expert witness?

20 A. You mean in general for -- for
21 different cases?

22 Q. For different cases, yes.

1 A. Yeah, I think -- I don't remember
2 exactly, but I think I did a small case in
3 California maybe in late '80s or early '90s. I
4 don't remember.

5 Q. Okay.

6 A. And just a few cases since then.

7 Q. Were they all patent matters?

8 A. When you say "patent matters," you mean
9 IP generally? I mean --

10 Q. Cases related to patents.

11 A. Yes. Yes.

12 Q. Were they all related to
13 semiconductors?

14 A. Depends what you mean by
15 "semiconductors."

16 Q. What was the subject matter of the
17 cases generally?

18 A. So one, a small first one I recall had
19 to do with semiconductor processing equipment, and
20 then the only two that have been really kind of
21 serious time consuming have been in LCD displays and
22 the electronics, control transistor electronics that

1 goes into LCDs.

2 Q. Okay. Do you know how many cases prior
3 to these matters you worked on as an expert witness?

4 A. Not offhand.

5 Q. Less than 10?

6 A. Yes, less than 10.

7 Q. Less than five?

8 A. I don't know.

9 Q. Okay. Do you remember in those prior
10 cases whether you represented the patent holder?

11 A. I don't remember about -- so there were
12 two large LE -- LCD cases, and I think I represented
13 the owner of the patent. It was an infringement.
14 No. I'm sorry. I'm sorry. Yes, I represented --
15 excuse me. I represented the holder of the patent
16 who was suing for infringement.

17 Is that the right way to say it?

18 Q. Yes.

19 A. And in the first case, I don't remember
20 who owned the patent.

21 And then for completeness, there were a
22 couple of little things where people needed my

1 advice or wanted me to go to the Patent Office where
2 they have -- they're having an informal hearing with
3 the examiner, some things like that, but that's it.

4 Q. All right. But these cases are the
5 first cases that you worked on that are related to a
6 petition for review before the Patent Trial and
7 Appeal Board?

8 A. You mean IPR cases?

9 Q. Yes.

10 A. I think so. I think I had one
11 opportunity where I was asked to go to the Patent
12 Office to talk with the examiners about the request
13 that had been made for reexamination, but I think
14 that's different from IPR.

15 Q. Do you remember when that case was?

16 A. I would guess three or four years ago,
17 but I'm not sure.

18 Q. And in that case, did you represent the
19 patent holder?

20 A. I don't know.

21 THE REPORTER: Exhibit 1.

22 (Document marked, for

1 identification purposes, as Rubloff Exhibit No. 1.)

2 BY MR. CHEN:

3 Q. Dr. Rubloff, I've asked the court
4 reporter to mark as Exhibit 1 your curriculum vitae.
5 I hope I pronounce that right. I'll just call it
6 CV.

7 A. (Laugh).

8 Q. Please take a moment to review this
9 document.

10 A. (Reviewing document). Okay.

11 Q. All right. Dr. Rubloff, is this your
12 CV?

13 A. This is my CV as of I don't know what
14 date, recent, fairly recent, but not completely up
15 to date.

16 Q. Up to date with respect to at least
17 this year, though?

18 A. Well, I don't know. I'd have to look
19 in detail at some of these. I'm sorry. I think
20 it's a fairly small matter, but I wouldn't like to
21 say that it's certainly up to date as of a year ago.
22 Because if you'll look at these conference

1 organization activities, you know, we're required --
2 not required but expected to have these long CVs.

3 Q. Right.

4 A. And, frankly, they're very hard to
5 keep, up -- up to date on. So conference
6 organization activities, I'm sure that there are
7 things now in that don't appear here --

8 Q. Okay.

9 A. -- and probably more than a year ago.

10 Q. Okay.

11 A. Very hard to keep this kind of thing up
12 to date.

13 Q. Sure. But largely current at least
14 through 2013/2014?

15 A. Mostly current.

16 I guess I should note one or two things
17 that have changed. I'm pleased to say that my
18 position as director of the Center for
19 Nanostructures for Electrical Energy Storage and my
20 role as -- where is it here -- founding director of
21 the Maryland NanoCenter have changed temporarily
22 because I have acting directors for both of these.

1 Q. Okay.

2 A. Since I'm on sabbatical.

3 Q. Okay.

4 A. I'm very pleased to report that.

5 And probably the number of publications
6 and stuff, that's changing on a weekly basis. So --

7 Q. Sure.

8 A. -- that won't be up to date.

9 Q. Okay. Now, Dr. Rubloff, have you
10 worked in the field of semiconductor manufacturing?

11 A. In -- yes. Yes. In the -- in the
12 research domain and in connection with people who
13 are actually doing manufacturing and the development
14 of manufacturing strategies.

15 Q. So you haven't worked directly yourself
16 in doing manufacturing or developing manufacturing
17 strategies; is that right?

18 MR. MUKERJI: Objection to form.

19 THE WITNESS: No, that's not the
20 case. No. I have worked in manufacturing strategy
21 development.

22 BY MR. CHEN:

1 Q. Oh.

2 A. I should mention, there's a publication
3 on the list here, which I think was 1992, in the IBM
4 journal, which is actually a summary of the work
5 that I had done in research and collaborated with
6 Don Bordonaro in IBM Burlington, who was in charge
7 of the Strategic Equipment Council -- I think that's
8 what it was called -- for the IBM Corporation.

9 So they were the ones central to making
10 decisions about what kinds of tools to buy, what
11 design changes are needed, and really driving the
12 move toward manufacturing cluster tools. So
13 that's -- that you can see in that publication.

14 And what was interesting about that is
15 that my research groups were doing the research
16 counterpart of cluster tools, which I'm sure we'll
17 get into, and so we put our heads together and wrote
18 a review paper about where this is actually going.

19 Q. When did you first start working with
20 semiconductor manufacturing?

21 A. I guess the right introduction to that,
22 it's a little cloudy how you would describe it

1 because I started out in as a kind of pure scientist
2 in materials surfaces, and I got interested in
3 electronic materials, which are relevant to
4 semiconductor manufacturing, in about 1977.

5 And that underwent continuous evolution
6 from kind of the science of interfaces of electronic
7 materials, to the processes and equipment, to the
8 integration of those schemes into process
9 integration flow. And so by -- let's see. It was
10 on silicide interfaces and then it went to CVD and
11 etching and so on, and I would say -- let's see.

12 I joined the Silicon Technology
13 Division in 1986 as a manager, and in 1985 I was a
14 technical staff person to the vice president for
15 logic and memory. So somewhere in there my science
16 evolved to the technology and, in particular, the
17 manufacturing aspects where -- where what I'm
18 talking about is: What kinds of equipment do you
19 use to make these kinds of devices? And how does
20 that equipment carry out what you want to make these
21 devices? And what are the manufacturability issues
22 that are associated with using those things? In

1 particular, both equipment and also the process
2 flow.

3 So I was very sensitized to that in
4 those days, and I guess I'd say that that certainly,
5 the time frame of around 1980, if you had asked me
6 then, I would say, yes, I'm interested in working on
7 aspects critical to semiconductor manufacturing.

8 Q. Okay. And was your work in research?

9 A. I was in the research division, but I
10 had collaborations and interactions and -- I don't
11 know -- partnerships with people at IBM Fishkill and
12 IBM Burlington. Don Bordonaro, who I mentioned, I
13 think his organization was central in helping and,
14 as I hear it, underwriting applied materials to
15 development of the 5000, which was the pioneering
16 cluster tool that was introduced, I think, in 1987.

17 MR. MUKERJI: Dr. Rubloff --
18 before you ask the next question -- I'll just remind
19 you. I don't know what confidentially --
20 confidentiality obligations you may have to your
21 prior employers and that sort of thing, just respect
22 that.

1 THE WITNESS: Yes.

2 MR. MUKERJI: This is a public
3 proceeding. So don't reveal anything confidential.
4 If you have a question about that, let us know.

5 THE WITNESS: Okay. Yeah. I
6 think that there isn't anything, but I've been gone
7 20 years from IBM.

8 So to finish that story, as I --
9 as I worked in silicon technology, I became
10 acquainted with the kinds of people who are doing
11 device integration strategy and interacting with
12 them and that was a nice residence because it
13 related our capabilities in process research to
14 their manufacturing considerations.

15 And then about the time -- let's
16 see. This would have been, I guess, probably in the
17 CV, of course.

18 Yes. So in 1992, I moved from a
19 management role in silicon technology to a
20 management role in manufacturing research
21 department, and that allowed me to get new
22 interactions and perspectives on particularly the

1 role of process modeling, logistics, factory flow,
2 things like that. And these I think -- and I moved
3 my niche in experimental research to process sensing
4 for advanced process control.

5 And so I kept -- I know this is a
6 slightly long-winded answer, but the fact is that I
7 kept evolving into manufacturing and in the first
8 technology roadmap, which was 1994 for the
9 semiconductor industry, I was involved in the
10 metrology section and we started the emphasis then
11 on advanced process control, which has since become
12 a reality.

13 So my research was in doing CVD
14 process and can we tell what's the chemistry
15 happening on the surface at that time by using
16 appropriate sensors, and how do you turn that into a
17 way of controlling those tools.

18 There are some very nice stories
19 actually to tell about that.

20 BY MR. CHEN:

21 Q. So let me see if I can -- you know,
22 correct me if I'm wrong in terms of how I summarize

1 your experience.

2 Your own work in the '80s was in
3 research, but you collaborated with individuals who
4 were more directly involved in manufacturing and
5 your research had applicability to semiconductor
6 manufacturing?

7 A. I think that's a reasonable
8 approximation to what I gave as a much longer
9 description.

10 Q. Did you work in the FAB?

11 A. Well, that's a complicated question.
12 In a manufacturing FAB, the answer is no. In a
13 development FAB, I had times when I would interact
14 with people occasionally in that environment. In
15 the research division, it's complicated because of
16 the structure of IBM.

17 In the research division, we had an
18 advanced clean room, which was a partnership with
19 the Fishkill development divisions and the
20 Burlington development and manufacturing divisions.
21 So it's really hard to say where the line is there.

22 And my -- I had a number of management

1 roles and then, in addition, I'm a research staff
2 member. I do research and that -- that research
3 included management responsibilities for what was
4 called -- yeah. Now, I can't remember the name of
5 it, but an exploratory clean room facility in
6 Yorktown research. So, and I was in that facility
7 on a fairly regular basis.

8 So I know what a clean room is.

9 Q. But -- okay. But you didn't work in a
10 manufacturing lab that was used to make commercial
11 product; right?

12 A. No, I was not in the FAB in Burlington
13 or Fishkill on a regular basis.

14 Q. Did you work in the field of thin
15 films?

16 A. Certainly.

17 Q. What was your experience with thin
18 films?

19 A. Let's see. My research in thin films,
20 I guess I would say, started in around 19 -- I
21 wonder if I can tell from here. It would have been
22 -- I started IBM in '73. I think it must have been

1 about '77 when I turned my attention from catalytic
2 surface science problems to the formation of metal
3 silicides at the metal silicon interface. So that
4 was depositing a thin film of metal, look at how it
5 reacts with the silicon underneath, how silicides
6 are formed, and all the implications that came from
7 that.

8 And the thin film work has continued to
9 this day and included the next generation of that
10 work was MOS structures, metal-oxide-semiconductor
11 structures, based largely on thermal oxidation. And
12 then chemical vapor deposition and that was aimed at
13 the silicon industry primarily, although later on we
14 had sojourns into gallium nitride since I've been at
15 Maryland, and so it's been continuously thin films
16 of one sort or another.

17 Today it's atomic layer deposition
18 which is a derivative or, let's say, the forefront
19 of CVD for building nanostructures.

20 Q. Okay. How about etching? Did you do
21 work with etching?

22 A. Yes, primarily dry etching or plasma

1 etching as you might call it. A little bit wet
2 etching. We use wet etching as a kind of, you know,
3 workhorse for simpler things.

4 Q. How about did you work with
5 lithography?

6 A. Yes.

7 Q. What type of work did you do with
8 lithography?

9 A. So most of our work didn't require high
10 resolution lithography because we were really
11 studying thin films and interfaces, but there have
12 been some cases where we've done that especially
13 more recently because we use -- so in the
14 NanoCenter, which I direct, or not this semester but
15 I direct, we have a clean room facility.

16 So I'm responsible ultimately for that,
17 and so there's plenty of lithography. And then the
18 program, which actually should be a CV correction
19 here, I'm no longer doing biomaterials and bioMEMS,
20 but for that we do lots of lithography as well as
21 for the energy devices.

22 Q. Did any of your work with lithography

1 relate to semiconductor manufacturing?

2 A. Indirectly I would say, not
3 principally.

4 Q. Did you do work with semiconductor
5 process integration?

6 A. Yes, in various flavors. In one case,
7 as one kind, the laboratory that I started in 1986
8 at IBM included capabilities for various kinds of
9 chemical growth and evaporation techniques for
10 deposition and also surface cleaning and -- let's
11 see -- some -- some ion beam plasma work, not a
12 major feature.

13 And there we were interested in looking
14 at: If I put down a layer of this material under
15 these conditions, what does that do to the next
16 layer of some other material? In other words, that
17 was the one embodiment of looking at the question of
18 process integration, which is a very critical
19 question.

20 But in another sense, the interactions
21 that -- that I had with various people in IBM in
22 research, particularly there were people that I

1 recall quite well interacting with, who would
2 present a problem like this. Actually, one of them
3 was: How do we make a self-aligned shallow trench
4 isolation? And what can your CVD process do for
5 that? And what's the dependency on etching?

6 And so I remember that in those days,
7 because we knew how to do some of these processes
8 and we were interested in semiconductor
9 manufacturing technology, I and the people in my
10 group had a lot of interaction with the device
11 integration people in the silicon technology
12 division who were working as part of what was called
13 the ASTL, Advanced Silicon Technology Lab, that
14 partnered our research division in Yorktown with IBM
15 Burlington and IBM Fishkill development and
16 manufacturing science.

17 So this notion of process integration
18 is one that I've been, I would say, far more close
19 to in kind of the strategic implications than how
20 much I could do in my own research lab.

21 Q. So you didn't do any direct research
22 with semiconductor process integration; is that

1 right?

2 MR. MUKERJI: Objection to form.

3 THE WITNESS: Would you restate
4 that, please?

5 BY MR. CHEN:

6 Q. I was just trying to clarify the last
7 statement you made.

8 You said that:

9 This notion of process integration is
10 one that I would say that I'm far more close to in
11 kind of the strategic implications and how I could
12 do in my own research lab.

13 And I so wanted to clarify whether you
14 meant that you didn't actually do any direct
15 research or direct work with semiconductor process
16 integration; is that right?

17 MR. MUKERJI: Same objection.

18 THE WITNESS: I don't think that's
19 a fair way to characterize it.

20 So I was referring primarily to my
21 discussions in the '80s --

22 BY MR. CHEN:

1 Q. Okay.

2 A. -- and early '90s with IBM technology
3 people in research and in other divisions --

4 Q. Okay.

5 A. -- when I made that statement.

6 In terms of how much my -- let's say my
7 publishable research has been in process
8 integration, I think it's been pretty substantial.

9 Q. Okay.

10 A. So, for example, at a certain point in
11 I think about late '80s, people were interested in
12 making high-density capacitor structures and the
13 question was: What can you do to make a high
14 surface area out of thin film technology? And the
15 answer to that we found was to use
16 nucleation-controlled growth that allows you to make
17 rough silicon surfaces.

18 Out of that I think we have a patent
19 and a number of publications. That certainly is a
20 process integration issue, although not the entire
21 line that you have for making the device.

22 And then moving to the present, our

1 work has been recognized in energy storage, which
2 uses the same thin film techniques as the
3 semiconductor world does, CVD, ALD, oxidation, etc.

4 And we've been nationally recognized
5 for building the world's smallest battery using
6 highly conformal deposition by a kind of CVD
7 technique called atomic layer deposition. Put two
8 electrodes at either end of a nanopore and make a
9 full-fledged battery. So that is certainly process
10 integration example.

11 So, I mean, the bottom line is that my
12 research students and the students who have to
13 listen to me in lecture know what process
14 integration is.

15 Q. Did you ever develop a semiconductor
16 process for making a device?

17 A. Now, that's a very broad question.
18 That's too broad a question for me to know how to
19 parse.

20 Q. Okay. Did you ever develop the
21 semiconductor process from beginning to end for
22 manufacturing a semiconductor device?

1 A. You mean where my hands or my head were
2 doing every single step and coming up with a
3 different device or a different process flow?

4 Q. Yes.

5 A. No.

6 Q. Did you ever develop semiconductor
7 processing --

8 A. Actually, I'm not sure anyone has done
9 the whole thing alone.

10 Q. Okay. Did you work on a portion of a
11 semiconductor process that was then used to
12 manufacture a device?

13 A. I certainly worked on processes that
14 are used in semiconductor device manufacturing and
15 trying to see ahead what are the things that control
16 that.

17 Yeah, I guess I could give an example.
18 Actually, it's an interesting one.

19 I had a program with Northrup Grumman,
20 which is interested in gallium nitride HEMT devices,
21 and the trick in the HEMT device is that there's a
22 capping layer of only 20 nanometers whose thickness

1 controls the performance of the HEMT device. And we
2 developed and my group, working with the engineers
3 at Northrup Grumman, we developed a realtime for
4 institute sensor that could determine in realtime
5 what the thickness and deposition rate of the CVD
6 process was as MOCVD, gallium nitride, aluminum
7 gallium nitride.

8 And we put in a process control so that
9 in realtime we could tell how many layers are on the
10 surface and then turn off the process when there's
11 just the right number, and they were able -- we were
12 able to control the aluminum gallium nitride cap
13 layer thickness to 1%.

14 Q. Did you ever develop portions of a
15 semiconductor process that was used to manufacture a
16 MOS semiconductor device?

17 A. An M-O-S?

18 Q. Yes.

19 A. The one example was that we did some
20 work on understanding the stability of the thermal
21 SiO₂ silicon interface high temperature annealing
22 and we looked at what are the degradation mechanisms

1 that happen. And we started in research with the
2 supposition that, well, if we can control the
3 cleanliness of the process environment, the kind of
4 thing cluster tube people worry about, we might be
5 able to make better structures. We found exactly
6 the reverse.

7 What happened was, there's a reaction
8 where the silicon and the SiO₂ form volatile silicon
9 monoxide, which comes off the surface and ends up
10 causing activation of existing defects, making them
11 electrically active, and then later on leads to
12 voids in the oxide film.

13 So this actually was the subject of
14 both a number of publications and a patent, and in a
15 sense that was adopted in manufacturing, but I'll
16 tell you how.

17 Gary Barner, who was at Yorktown, was
18 working with colleagues in Burlington. And they had
19 noticed that when they did annealing in what they
20 thought was a really good furnace, really clean,
21 that the devices failed too often, more often than
22 usual. And then he remembered our work and he said,

1 oh, they taught us what's going on there and all you
2 have to do is to put some little bit of water or
3 oxygen into the annealing environment. This problem
4 will go away, and it did.

5 So I don't know what it really led to
6 but --

7 Q. So --

8 A. -- that was gratifying.

9 Q. So your work, again, had applicability
10 to semiconductor manufacturing or the manufacturing
11 of semiconductor devices; is that what you're
12 saying?

13 A. I think it had some relevance to them.
14 You know, the people who work in development are
15 usually doing a more evolutionary approach and more
16 practical approach because you're trying to make
17 things work.

18 Q. Right.

19 A. We were doing research that had, I
20 think, a remarkable level of interaction and impact
21 compared to what most people do in research.

22 Q. But your work wasn't in development;

1 correct?

2 A. No, I was in the research division.

3 Q. Okay. And so you didn't ever develop a
4 semiconductor process or portion of a process that
5 was to be used directly in the manufacturing of a
6 semiconductor device; is that fair?

7 MR. MUKERJI: Objection to form.

8 THE WITNESS: It's hard for me to
9 measure that because we had a very integrated
10 environment in IBM across its divisions from
11 research to manufacturing, and part of my hesitation
12 is that the program that I started in 1986 at IBM
13 was in a sense pioneering.

14 We brought together ultraclean
15 process environments that could be coupled into
16 process integration sequence, and part of that work
17 was in low temperature epitaxy, which is sometimes
18 called UHV/CVD epitaxy.

19 Bernie Meyerson was primarily
20 responsible for that, but I think his ability to
21 make that happen came from the vision that I had and
22 that he and one or two other colleagues had in

1 creating this research -- special research
2 environment. We call it integrated processing, but
3 it's really a research version of cluster tool
4 manufacturing.

5 BY MR. CHEN:

6 Q. Did you ever develop semiconductor
7 processes for use in a commercial semiconductor
8 device?

9 A. Well, I'll give you kind of the same
10 example that this UHV/CVD epitaxy that Bernie
11 Meyerson was primarily responsible has been a huge
12 hit and certainly in manufacturing, but he was
13 really the driver of that. And he built on some of
14 the things that we together talked about and
15 realized in my lab and the example I gave you of
16 ultraclean annealing of MOS structures and so on.

17 Q. How would you distinguish between the
18 field of research that you worked in and the
19 development field?

20 A. In the research division, we had the
21 freedom to choose which processes, which devices,
22 which sequences of processes and structures and

1 devices we wanted to focus on. In development,
2 there's a technology roadmap where we know that the
3 industry has the -- it used to call it the national
4 technology roadmap for semiconductors, then the
5 international technology roadmap for semiconductors.

6 And then so this is pre-competitive
7 roadmap where people should be trying to move the
8 technology, and I would say that that roadmap
9 defines vectors of what people should work on and
10 that's what people in development largely do.

11 But now and then research can play a
12 role in changing which vectors are adopted or making
13 new vectors. So I think maybe a simple way to put
14 it is that development is really mission oriented.
15 Research has a mission, but it's an adjusted one.
16 It's more adjustable mission.

17 Q. Do you understand what are the general
18 goals in semiconductor manufacturing?

19 A. I think so.

20 Q. What are those general goals?

21 A. Well, very generally speaking, kind of
22 broad-brush perspective, they're interested in

1 increasing performance, increasing or at least not
2 hurting reliability, driving down costs, and those
3 are leveraged by other things such as factory
4 flexibility, process integration alternatives, and
5 so on. Oh, and availability of equipment, equipment
6 design.

7 Q. And these general goals are the typical
8 objectives that someone might have when they're
9 trying to develop a semiconductor process; correct?

10 MR. MUKERJI: Objection to form.

11 THE WITNESS: I think it depends
12 on who's developing a process. So you said "a
13 semiconductor process." Let's say I'm trying to
14 develop an MOS isotropic etching process. I'm
15 probably a process engineer, not a process
16 integration specialist. My task is to make that
17 single process work better.

18 So I really don't have as my
19 mission the larger system goal of improving
20 manufacturing costs and performance and so on. I
21 have one piece of the puzzle. So that's quite
22 different.

1 BY MR. CHEN:

2 Q. So the general goals that you had
3 mentioned before are goals for the larger system?

4 A. Yes.

5 Q. All right.

6 A. Somebody, somebody at the top of the
7 organization has to worry about those goals. Let me
8 give you an example what I'm talking about.

9 In something like the -- what would
10 have been the mid-'90s when I had been at North
11 Carolina State University and I came to Maryland,
12 where there were a different set of skills in the
13 institute that I directed, we had a National Science
14 Foundation program supported by also the
15 Semiconductor Research Program to understand the
16 interaction between an individual process model,
17 like for CVD or etch or probably both of them, and
18 the equipment models that carry out that process,
19 which may be cluster tools and have some number of
20 chambers on them that robots move things through.

21 And then you can have different numbers
22 of these cluster tools, and the numbers that you

1 have in the configuration of each tells you how
2 efficient your factory flow will be. And then the
3 factory has to look at the horizon of what is going
4 to be the demand for this product and that product.

5 So we had integrated models that went
6 all the way from a specific materials thin film
7 process to the horizon of changing demands and
8 factory flow optimization.

9 So at the end of that is where those
10 general goals lie, but those general goals depend on
11 what happens at each little process. And if you
12 make a process improvement, it will affect or may
13 not affect the flow of product through a cluster
14 tool or through a sector of the FAB.

15 So there's a whole hierarchy from
16 individual process to the kinds of general goals
17 that you're talking about.

18 Q. So I'm clear, when we talk about
19 overall system, we're talking about the entire
20 semiconductor process for manufacturing a device
21 from beginning to end; correct?

22 A. Yes, and the way that it's made. I

1 mean, that's -- that's a factory, that's all the
2 equipment in the factory, that's the sequence of
3 processes that individual tools in the factory have
4 to -- have to carry out.

5 Q. And then when you mention individual
6 process, that is a subset of that overall
7 semiconductor process, for example, you know,
8 etching?

9 A. Uh-huh.

10 Q. Or deposition?

11 A. Yes.

12 Q. Okay. Who's responsible for assembling
13 all the individual processes into a single overall
14 system or overall process?

15 A. So I guess the best way to address that
16 question is, this would typically involve a
17 significant number of people, maybe a couple hundred
18 or something like that. In IBM environment, only
19 one I can speak to, these would involve development,
20 probably manufacturing, probably equipment
21 engineering, and some research people. So that's a
22 team who wants to develop the next version of the

1 CMOS, or whatever it is, and so there will be some
2 management leader there who has that responsibility
3 of organizing the team and anticipating what it is
4 that they're going to get together. Right?

5 Ah, I'll give you a good example.

6 When I was working in the -- this would
7 have been in the '80s. When I was working on CVD,
8 PVD processes, etching processes and so on, IBM was
9 facing a huge transition. That transition was
10 interconnect. We were at four levels of metal
11 interconnect with aluminum as the conductor and
12 silicon dioxide as the insulator.

13 And those people who would have been on
14 such a team and the kind of strategic forecasters of
15 where things can go -- this is this technology
16 roadmapping environment -- identified the fact that
17 it can't keep going this way because the capacitants
18 between the wires is too large for the higher
19 speeds. We anticipate smaller devices to give.

20 The resistivity of the aluminum wires
21 is just too high, and so the desire was to replace
22 aluminum with copper, including diffusion barriers,

1 adhesion layers and so on that would be necessary,
2 and to replace the silicon dioxide insulator between
3 the wires with low K dielectrics. These would be
4 normally polymers or some kind of porous material.

5 And so there were teams of people and
6 leaders of those teams who spent huge amounts of
7 effort trying to figure out how do we get from
8 aluminum SiO₂ to copper polymer, and everybody was
9 involved in that. All the people in my group.

10 At that time, I was second level
11 manager, and so I had an etching group who worked
12 under me and a physical vapor deposition group and a
13 chemical vapor deposition group, which is kind of
14 mine, and characterizations group, and everybody was
15 focused on that problem.

16 So is there one person who's completely
17 responsible? I don't know the answer to that. But
18 it certainly is a hierarchal team that integrates a
19 lot of things or you can't address that kind of
20 problem.

21 And, incidentally, the change was
22 successful. Everybody uses copper wiring today.

1 Q. All right. Let me again see if I
2 understand what you're saying.

3 So for developing an overall
4 semiconductor process for manufacturing a device,
5 there will be individual team members or groups that
6 might have responsibility or will have
7 responsibility for a specific aspect of the process,
8 and specific aspects might be etching or another
9 aspect might be deposition or another aspect might
10 be lithography; is that fair characterization?

11 MR. MUKERJI: Objection to form.

12 THE WITNESS: Those three things
13 are essential to, let's say, changing the paradigm
14 of going to a next generation process flow, but
15 those are kind of at the bottom of the ladder and
16 then there are levels in between.

17 So, for example, there might be a
18 module of, well, how do we get this litho process to
19 work with this etch process? What are the
20 compatibilities and trade-offs between them?

21 BY MR. CHEN:

22 Q. Right.

1 A. It might be deposition and etchback,
2 you know, all kinds.

3 Q. Okay. Let me see if I can approach it
4 differently. I'm trying to understand the
5 hierarchy.

6 A. And -- and clearly the average process
7 engineer --

8 Q. Right.

9 A. -- who's working on one or two tools
10 and processors, doesn't have this whole picture in
11 mind.

12 Q. Right.

13 A. But most of them after a couple of
14 years will understand that that etch process they're
15 supposed to fix, the reason is it's linked to other
16 things. If that etch process drifts off to the
17 right, then the next thing is going to have to
18 compensate for that or it's going to fail.

19 Q. Sure. Okay.

20 So at the -- for the development of a
21 semiconductor process for manufacturing a device, at
22 the base level of the hierarchy are the individual

1 process engineers who are responsible for specific
2 aspects of the process like etching or deposition or
3 lithography; is that correct?

4 MR. MUKERJI: Objection to form.

5 THE WITNESS: Well, I don't know
6 about the base level, quite -- quite what you mean
7 by that.

8 BY MR. CHEN:

9 Q. Okay. Could you describe again the
10 general hierarchy for developing a semiconductor
11 manufacturing process beginning with the --

12 MR. MUKERJI: Objection to form.

13 BY MR. CHEN:

14 Q. -- lowest level and then moving up the
15 hierarchy to the individual who has the
16 responsibility or visibility of the overall process?

17 MR. MUKERJI: Objection to form.

18 THE WITNESS: So you depicted a
19 kind of vertical structure, a hierarchal structure.
20 In one way or another, the organization has to have
21 that, but you said developing a semiconductor
22 process.

1 To me, that can mean an individual
2 etch process. It can mean a kind of module etch
3 coupled with lithography and so on, and so the
4 people responsible for that are existing at all
5 levels.

6 BY MR. CHEN:

7 Q. I'm talking about developing the
8 process for manufacturing a device so it would
9 include all the different steps that are needed to
10 manufacture a device.

11 A. Well, remember that there's heritage
12 here. It's very rare, if ever, that you just make a
13 new -- a whole new structure.

14 Q. Sure.

15 A. Things evolve. If there are 25, 125
16 process steps to today's CMOS generation X, then
17 most of the changes will be evolutionary. They
18 might be in one process level, say etch, they might
19 be in a module level, and it's not very often that
20 it's something like I described with whole change in
21 the interconnect world.

22 Does that help you?

1 Q. Not really. I'm still a little bit
2 unclear. Maybe I'll try to approach it just another
3 way.

4 The process engineer that you mentioned
5 before who works on one of the specific aspects of
6 the process, like etching or deposition or
7 lithography or something of that nature, that
8 individual is responsible for improving or
9 developing a specific aspect of a process; correct?

10 A. How big did you mean the word "process"
11 to apply?

12 Q. All right. Okay. You know what? This
13 is --

14 A. I'm not trying to be difficult but --

15 Q. No, no. I understand. I want to make
16 sure that we're on the same page in terms of how we
17 use terms, and I think process is one of those that,
18 depending on context, might have different meaning.

19 What is the term that you feel most
20 comfortable with when I want to refer to the entire
21 process for manufacturing a device, the process that
22 includes, you know, multiple etch steps or multiple

1 deposition steps, and all those sort of individual
2 processes?

3 A. I don't know what term I'd use for
4 that. I mean, I don't think about it in that -- in
5 that sense.

6 Maybe I can suggest one thing, though.
7 So I tell my students --

8 Q. Sure.

9 A. -- if you go to work for Intel or some
10 company like that, first job is probably going to be
11 equipment engineer or process engineer with a Ph.D.
12 in this case, as my students do.

13 Q. Right.

14 A. And they are going to work with people
15 who are, for example, they would often be an
16 equipment engineer that has a master's degree or
17 something like that. And I tell them that your
18 first job is going to be kind of centered around a
19 unit process, meaning it's etch and it's a Lam,
20 whatever it is, etch tool.

21 And I tell them, what you should look
22 for in your career is start to understand what

1 everybody else is doing. What's the implication of
2 that etch process and that tool on other things in
3 the sequence in that region? If you're working on
4 interconnect, you're working on shallow trench
5 isolation, or DRAM capacitors.

6 Because the job you really want is
7 process integration engineer because then you're
8 looking at several steps, and I was -- I thought
9 about this hard when I was asked to define one of
10 ordinary skill in the art, and I chose that to be
11 actually for -- for all three patents at issue here.

12 Someone typically with a master's
13 degree and, importantly, a couple of years of
14 experience. Because when you come in with a
15 master's degree, you may know how to run an etch
16 tool, but what you really need to do is to
17 understand its relationship to things around it in
18 the process flow.

19 And so the only demarcation line I
20 could offer is process or equipment engineer,
21 process integration at some level, and then kind of
22 the big driver is fourth level management or

1 something like that, who are organizing people at
2 many levels if there's a major challenge to take on.

3 Q. Okay. So one of the terms you used was
4 "unit process"?

5 A. Yes.

6 Q. Okay. If I use the term "unit process"
7 to refer to, like, etching or deposition, like the
8 specific aspect of a process, is that a fair way to
9 use the term?

10 A. That's a good idea.

11 Q. All right.

12 A. That's actually what it's called.

13 Q. Okay.

14 A. Better idea. I didn't think to share
15 that earlier.

16 MR. MUKERJI: Mr. Chen? I'm
17 sorry. We've been going about an hour. You mind if
18 we take a short break?

19 MR. CHEN: Sure. Let me just
20 finish these definitions, and then we'll take a
21 break. I was thinking about that too.

22 BY MR. CHEN:

1 Q. Okay. And then if I use the term
2 "system process," can I use that to refer to the
3 overall process that's used to manufacture a device
4 that might include many unit processes?

5 A. I've never heard that term.

6 Q. Okay.

7 A. We'd be making it up.

8 Q. Well, I mean, I think it was used
9 previously before, but is there a term then that I
10 can use to refer to the overall process that
11 includes many unit processes?

12 A. I don't know what the term would be.
13 I'm trying to think what would be convenient for
14 that. I mean, from a manufacturing standpoint, it's
15 kind of factory flow. You go from this unit
16 process, to that unit process, to that unit process
17 and so on. But I'm not -- usually when you think
18 about factory -- factory flow, you're thinking about
19 the logistics of how you optimize getting stuff
20 through the FAB and particularly associated with
21 cost.

22 Q. How about integrated process?

1 A. This is troubling also because I've
2 published that term too many times at the level of a
3 short sequence of processes carried out in
4 essentially cluster tool-type environments.

5 Q. Okay. So an integrated process may
6 include multiple unit processes, but is not the full
7 process?

8 MR. MUKERJI: Objection to form.

9 THE WITNESS: That's a really hard
10 one because if you ask the director of IBM at
11 Fishkill or Applied Materials Santa Clara, or
12 something like that, what they call it, they
13 probably use a similar kind of term. So everybody
14 is trying to use the same term, but it's not the
15 same thing.

16 BY MR. CHEN:

17 Q. Okay. Well, we just need to find terms
18 so that when I'm asking you questions today in the
19 deposition, you understand what I'm asking about and
20 I understand what you're talking about.

21 So why don't we take a break, maybe you
22 can give it some thought, and then when we come

1 back, we'll try to find the right term, terminology
2 to use.

3 A. All right. Let me just ask a question,
4 though.

5 Q. Sure.

6 A. In the patents at issue, these are
7 different kinds of process steps in a certain
8 sequence of a certain life to do something, and I
9 don't -- some -- some go pretty far across the
10 spectrum of steps that are in the whole factory.

11 Q. Sure.

12 A. Some are much shorter.

13 Q. Sure.

14 A. Does it really matter? Because we're
15 going to be talking about patents, specific patents.

16 Q. I think it matters because at least in
17 terms of some of the questions I've been asking, I
18 think there was some lack of clarity with respect to
19 what I was asking and what you were providing us
20 answer. So I'd like to get to some sort of
21 definition.

22 A. Okay. We can try.

1 MR. MUKERJI: Let's take a break.

2 MR. CHEN: Thanks.

3 (Recess - 10:09 a.m. - 10:22 a.m.)

4 MR. CHEN: Back on.

5 BY MR. CHEN:

6 Q. All right. Dr. Rubloff, let me see if
7 I can get some clarity on the terms that we've been
8 using.

9 When I say "unit process," what does
10 that mean to you?

11 A. I think of a unit process as a single
12 -- a single modification of a sample, a wafer, a
13 device, caused by a physical or a chemical -- let's
14 see. That's not broad enough, actually, because I
15 don't know what to do with metrology. You know, you
16 have to do measurements in between etch, deposition,
17 and so on.

18 But, generally speaking, unit process
19 to me connotes an etch, a single etch step, a single
20 deposition step, carried out in a tool.

21 Now, when I use the word "step," I
22 realize there's some ambiguity with that because on

1 most, if not all, tools -- let's take an etch step.
2 What will happen is, you have to etch at some power.
3 You have to get some gas flow and so on. And when
4 you look at the -- it would be the computer screen
5 these days, but really the recipe for that step,
6 that process, that unit process, you will see
7 sometimes 20 different substeps.

8 You have to turn it on. You have to
9 turn on the heating power if you're going to have a
10 heated substrate. You have to wait a certain amount
11 of time, some seconds, until it reaches temperature.
12 Then some valve will open and some power, RF power
13 will turn on, something like that.

14 So I keep getting into this dilemma of
15 steps, but to me a unit process is probably one tool
16 that may do some substeps to accomplish something.

17 Q. So unit process -- so if I use "unit
18 process" to refer to an etching step, including all
19 the substeps, or a deposition step, including all
20 the substeps, you would understand what I mean?

21 MR. MUKERJI: Objection to form.

22 THE WITNESS: Well, if we decide

1 to agree upon that terminology. But in asking
2 questions about the issues at hand, I reserve the
3 right to --

4 BY MR. CHEN:

5 Q. Sure. If you have any --

6 A. -- to make it --

7 Q. Yeah.

8 A. -- more specific because there are
9 subtleties in these substeps. And another place
10 where it gets more complicated is, what do you call
11 a cluster tool? If you have a cluster tool, is that
12 a unit process or not?

13 Q. Sure.

14 A. So I'll have to maintain some
15 flexibility.

16 MR. MUKERJI: I just want to
17 remind you guys not to talk over each for the court
18 reporter's benefit.

19 MR. CHEN: That was my fault. I
20 interrupted you.

21 BY MR. CHEN:

22 Q. But a unit process would include, for

1 example, etching and deposition; correct?

2 A. It depends on the definition. So there
3 are plenty of cases. If I look at how, let's say, a
4 deposition is done today, it's in a cluster tool
5 usually. And there will be a preheat cycle carried
6 out in one chamber and there may be the deposition
7 step in another chamber and then there may be
8 another step where there's annealing or even an
9 etchback step in another chamber.

10 So do I call the cluster tool a unit
11 process? I don't know. It's ambiguous.

12 Q. Do you -- do you use "unit process" to
13 refer to all those different -- different processes
14 within the cluster tool?

15 A. You mean to each of the processes?

16 Q. No, to all of them combined.

17 A. I don't really have a rule for that.
18 I'm not sure. I don't think -- I don't know of a
19 convention that's broadly accepted for this.

20 I could -- I could understand the
21 argument that if we -- if we go through a cluster
22 tool and it's going to do several steps, there's a

1 chamber here, a chamber here, a chamber here, it
2 goes through these three in sequence, you might say
3 this is a cluster tool that carries out three unit
4 processes. Each of which may have substeps.

5 Q. Okay. But then you refer to them as
6 three separate unit processes?

7 A. We could refer to them.

8 Q. You --

9 A. I mean, the best --

10 Q. You said this cluster tool carries out
11 three unit processes.

12 A. It could. I said it could be viewed
13 that way.

14 Q. Okay.

15 A. And as long as we describe what's
16 happening, then -- then I think it's -- it's not
17 difficult.

18 Q. Okay. So for today when we say "unit
19 process" and we use it to refer to etching or
20 deposition or lithography, that's a fair way to use
21 the term; correct?

22 MR. MUKERJI: Objection to form.

1 THE WITNESS: It may be a
2 convenient one, but you will hear me giving the
3 details.

4 BY MR. CHEN:

5 Q. Sure.

6 A. Not -- not just using a convenient word
7 -- term like that. Because I want to know what's
8 happening to the sample.

9 Q. Okay. Previously you had given an
10 example, maybe a more practical example, of when you
11 your students, for example, graduate and they get
12 their first job.

13 And so your students, I think, are
14 Ph.D. students; right?

15 A. Not exclusively but --

16 Q. Okay.

17 A. -- most of them are.

18 Q. All right.

19 A. I have -- I have sometimes master's and
20 undergraduate.

21 Q. So let's just take, for example, your
22 Ph.D. student who graduates and then he gets his

1 first job, and you said typically they enter in as a
2 process engineer represent -- responsible for a unit
3 process.

4 A. Okay.

5 Q. What is that process engineer who just
6 graduated responsible for?

7 MR. MUKERJI: Objection to form.

8 BY MR. CHEN:

9 Q. What are their job responsibilities?

10 A. I'm sorry. The siren is distracting
11 me.

12 Q. Okay. The new graduate student with
13 his Ph.D., he gets his first job as a process
14 engineer.

15 What is -- what are his initial job
16 responsibilities?

17 MR. MUKERJI: Same objection.

18 THE WITNESS: Well, it certainly
19 depends on his employer and the job to which he's
20 hired, but it could involve doing -- tracking what
21 the performance of a tool is or that process is in
22 terms of yield of that process, if there's a way

1 that's measuring that right after. It could involve
2 planning a design of experiments to optimize that
3 process. At the Ph.D. level, it may involve a
4 little more insight into the process chemistry and
5 some of the subtleties of the way the process works.

6 It would likely involve
7 interaction with the characterization lab where they
8 look at depth profiling through the thin film to see
9 if it's uniform and the right composition and things
10 like that. But it's hard to be specific because
11 every job is going to be a little different.

12 BY MR. CHEN:

13 Q. And their initial work is going to be
14 on a specific unit process?

15 MR. MUKERJI: Objection to form.

16 THE WITNESS: Not necessarily. I
17 mean, it could be in characterization and whether we
18 call that a unit process, I don't know.

19 BY MR. CHEN:

20 Q. Let me -- let me explain a little bit
21 of what I'm trying to understand and then maybe that
22 will help you.

1 I want to understand for two different
2 types of processes, like, for example, a deposition
3 step and then an etching step. All right. I want
4 to know how to distinguish between these two
5 different types of processes so when I use the term
6 "process," you know, we know whether we're talking
7 about just a deposition or just an etching and not
8 the two combined.

9 Is there a way to use the word
10 "process" to distinguish between these two different
11 things?

12 A. You could say etch process, deposition
13 process.

14 Q. Okay. And the etch process, is that a
15 unit process?

16 MR. MUKERJI: Objection to form.

17 THE WITNESS: It can be considered
18 a unit process, but that's just making another term
19 for something that's less precise than to say "an
20 etch process."

21 BY MR. CHEN:

22 Q. All right.

1 A. So, for example, I have a former
2 student who went to Applied Materials and -- I'm
3 sorry -- to Novellus, now Lam, and he's responsible
4 for a PECVD process. They have a PECVD tool. He's
5 responsible for refining, improving that tool and
6 its performance in carrying out PECVD on something.
7 I don't know what material.

8 Q. What was that example of?

9 A. Oh.

10 Q. I don't understand why you gave that
11 example. What were you trying to demonstrate?

12 A. I was just trying to clarify that it's
13 easier to say that he's working on an etch -- a
14 PECVD process than to say he's working on a unit
15 process.

16 Q. Is the PECVD --

17 A. I don't think he ever would tell me,
18 oh, I'm working on a unit process. That's kind of a
19 weird term. It's okay, but it's not very specific,
20 and I can much more easily say it's a PECVD process.

21 Q. But is there a term that you can use to
22 refer generally to all these different types of

1 processes like, for example, a PECVD process or a
2 reactive-ion etching process or a lithography
3 process --

4 A. I think unit process --

5 Q. -- at that level?

6 A. I think unit process is about as good a
7 term as I can -- as I know, and it's used
8 traditionally by the chemical engineers.

9 Q. So we'll use unit process, and if you
10 think in a specific situation where we need
11 clarification or you need to --

12 A. Uh-huh.

13 Q. -- add some detail, we'll clarify in
14 detail. Fair?

15 A. Thank you.

16 Q. Okay. Now, who is responsible for
17 integrating multiple unit processes together?

18 MR. MUKERJI: Objection to form.

19 THE WITNESS: I don't know how to
20 predict the answer to that. I mean, it depends on
21 the situation and what does it mean to have
22 responsibility.

1 These days -- I think it's a
2 little bit off topic, but these days people tend to
3 train to work in teams and they actually work in
4 teams. And so it's not as if -- it's not as if
5 there's one person that you always know is
6 responsible for that, that I can look at the org
7 chart of Intel and I can say, ah, that person is
8 responsible for developing the thin factory time.

9 Maybe -- maybe it happens that
10 way. I don't know, but I don't -- I don't really
11 know how -- I guess I should just say, I don't know
12 the answer to that.

13 BY MR. CHEN:

14 Q. Okay. How many years of experience
15 working in the industry would you need before you're
16 capable of understanding how different unit
17 processes interact with each other?

18 A. I think you have to be in the industry
19 for a couple of years or something like that.
20 That's why I defined it that way.

21 And the basis for that is my experience
22 with my students who have gone off to Intel, Applied

1 Materials, IBM, and so on, and when I see them a
2 year afterwards at a conference or something like
3 that, they have learned so much because they're in
4 an environment which sees every day the process
5 integration consequences, not the whole factory
6 flow, but process integration consequences of what
7 they're doing on a unit process.

8 Q. Previously you had mentioned the fourth
9 level manager.

10 A. Okay.

11 Q. Yeah.

12 A. I don't remember it.

13 Q. When you were describing the hierarchy
14 before you mentioned your students who entered in
15 who worked as a unit process -- on the unit process
16 initially. Then you mentioned the next level up the
17 ladder, which is integrating the unit processes, and
18 then you mentioned top level, you mentioned a fourth
19 level manager. I don't know if you remember that.

20 A. It was a figure of speech.

21 Q. Okay.

22 A. Saying somewhere in this there must

1 be -- I don't know -- fourth level, third level,
2 fifth level. I don't know.

3 Q. Okay. I was just wondering what you
4 meant by that fourth level manager.

5 A. Well, fourth doesn't mean anything, but
6 if -- if a company is trying to develop a next
7 generation technology, then there has to be a
8 concerted program. So somewhere in that
9 organization, they find a way to do that, and there
10 are many ways in an organization to move
11 strategically.

12 So in the old-fashioned days, you know,
13 you think, well, that person I'm giving -- I'm the
14 CEO. I give that person the assignment to make this
15 happen. These days it's more complicated than that
16 because you have integrated interdisciplinary teams
17 that come together, and sometimes those teams are
18 led by people at lower levels who have a special
19 capability for doing that and sometimes there's some
20 at a bunch of higher levels.

21 Q. But is that management level person
22 who's responsible for the general goals of

1 semiconductor processing that we talked about
2 before?

3 A. Well, somebody is responsible, but I
4 think it's kind of above my pay grade to -- to
5 answer that question.

6 Q. So somebody very senior then?

7 MR. MUKERJI: Objection to form.

8 THE WITNESS: Not necessarily.

9 Some of the key efforts that I was exposed to in
10 IBM -- well, there was one -- there was one case
11 where I was put on a team because there was a yield
12 failure in IBM manufacturing and so I represented --
13 I was the liaison from the research division.

14 And that -- what do we call it? --
15 task force was led by a second level manager in
16 Fishkill, not a fourth level manager, and there were
17 different kind of skills brought together. So
18 sometimes it's somebody young and -- and bold.

19 BY MR. CHEN:

20 Q. Okay. I was -- the only reason I
21 thought it was somebody senior was because you said
22 it was above your pay grade, and I assumed that

1 you're fairly senior. So above your pay grade would
2 be very senior.

3 A. No, no. I said that because I think
4 we're getting into the business school management
5 discussion, and I don't kind of know -- know how to
6 deal with that.

7 Q. Okay. Before when you were talking
8 about, you know, your experience with your graduate
9 students and after they graduated and had gone into
10 industry and they come back and you're impressed
11 with how much they've learned, which time frame are
12 we talking about?

13 A. Well, that's happened since I've been
14 in academia. So that's 1993. I had students while
15 I was at NC State who went to -- well, they all went
16 to work for Intel or Novellus at the time, or nearly
17 all. So certainly then.

18 And then also when I was at IBM, I had
19 people who reported to me. So these weren't all
20 Ph.D.s who took jobs in Fishkill or Burlington, and
21 I think they reported a very similar kind of thing.
22 You know, you get into a new environment where

1 there's this -- there's a larger goal of the factory
2 and the technology, and they start sampling how
3 things are related.

4 Q. When did your first graduate student
5 graduate?

6 A. I don't know the answer to that. I had
7 -- when I was at IBM, Iqbal Sharif worked in my
8 group and he was --

9 Q. Ah --

10 A. I'm sorry.

11 Q. I'm sorry to interrupt you. You can
12 finish your answer.

13 A. Oh, and so I guess he was kind of my
14 first graduate student. But I don't remember if I
15 was the formal co-advisor. He had a formal advisor
16 and an RPI, but he worked for me at IBM full time,
17 and so it may be that I was a co-advisor. I just
18 don't remember. Other than that, it would have been
19 1994 or so.

20 Q. After you had entered academics?

21 A. Right. Right.

22 Q. Are you familiar with the term "process

1 flow" as it's used in semiconductor manufacturing?

2 A. Yes.

3 Q. What is your understanding of the term
4 "process flow"?

5 A. So if I know that there are a set of
6 unit processes that need to be carried out to make a
7 certain device, a three-dimensional transistor or an
8 interconnect or a contact or something, it may be a
9 short process flow, it may be many steps.

10 Process flow means I do this first,
11 then I do this, then I do this.

12 Q. So a process flow is a sequence of unit
13 processes with a specific order; is that a fair
14 characterization?

15 MR. MUKERJI: Objection to form.

16 THE WITNESS: It's something like
17 that. Sometimes you can have variants of the
18 process flow that get a similar result or even the
19 same result. So the order may change, but more
20 often than not, you know, we've been doing this.
21 We've been making this in the FAB for the last two
22 years and here's what the process flow is. And it's

1 written down in this SOPs, standard operating
2 procedures, or more likely it's implemented in some
3 major computer system what's really in the factory.

4 BY MR. CHEN:

5 Q. If you have one process flow and then
6 you change the order of the various unit processes
7 within that flow, haven't you then created a new
8 process flow?

9 MR. MUKERJI: Objection to form.

10 THE WITNESS: Strictly speaking, I
11 suppose it would be fair to say that, or you've
12 revised the flow process, or you've chosen
13 alternative process flow. But one way or another,
14 if you write down the steps and here's the A process
15 flow and here's the changed version of it, something
16 will be different in the two columns.

17 MR. MUKERJI: Mr. Chen, I've got
18 to ask. Are we now going to move into the specific
19 declarations or are you characterizing this as
20 background?

21 MR. CHEN: This is going to be
22 still background asking about, yeah, general

1 background information about some of the processes.

2 MR. MUKERJI: No. You're asking
3 about a patent.

4 MR. CHEN: Actually, I'm not. I'm
5 asking about general semiconductor processes. I
6 didn't bring up the issue of the order. It was in
7 his question -- answer.

8 MR. MUKERJI: Your question was,
9 if you have one process flow and then you change the
10 order of the various unit processes within that
11 flow, so I think you are bringing up the notion of
12 order.

13 MR. CHEN: The reason was because
14 in his previous answer to what -- with respect to
15 what a process flow is, he brought up order. I'm
16 just trying to clarify his answer.

17 MR. MUKERJI: I understand and,
18 look, I'm not trying to -- you can ask him whatever
19 questions you want.

20 MR. CHEN: Sure.

21 MR. MUKERJI: What I want is a
22 clear record as to which declaration you're going to

1 use this cross-examination testimony for.

2 So going through his background,
3 his experience, that's fine, but it seems to me that
4 you're moving now to more substantive areas. So I
5 ask that you tie it to a declaration.

6 MR. CHEN: This is all just
7 background knowledge about semiconductor
8 manufacturing in general.

9 MR. MUKERJI: Well, then, can I
10 get your representation this is not going to be used
11 to cross-examine with regard to a specific
12 declaration? It can't -- it's got to be one way or
13 the other; right?

14 MR. CHEN: No. All the background
15 general stuff can be used for any of these
16 declarations, and then when I introduce his
17 declaration in the specific patents, then I will
18 limit that to the specific IPR.

19 MR. MUKERJI: So you're not asking
20 about --

21 MR. CHEN: Should we go off the
22 record for a second?

1 MR. MUKERJI: Sure. We can go
2 off.

3 (10:49 a.m.)

4 (Off the stenographic record)

5 (Witness stepped out).

6 (Witness returned).

7 (11:05 a.m.)

8 MR. MUKERJI: We can go back on
9 the record, I think.

10 MR. CHEN: So --

11 MR. MUKERJI: You want to make a
12 statement or shall I?

13 MR. CHEN: Yeah, I mean.

14 MR. MUKERJI: So we took a break.

15 THE WITNESS: Instruction for me
16 or what?

17 MR. MUKERJI: Well, I don't know
18 if it's an instruction for you, but we took a break
19 and counsel for respondent or HSC's counsel and I
20 had a discussion about how to conduct this
21 deposition, this cross-examination.

22 There are four declarations at

1 issue the witness has provided. Counsel previously
2 agreed for efficiency's sake that we would cover all
3 four declarations during the cross-examination over
4 the span of two days. That leads to a bit of a
5 procedural quandary as to when a question is within
6 or outside the scope of a particular declaration.

7 After conferring with counsel at
8 the break, we think we have an agreement in place,
9 and we're going to give it a try. And that is that
10 counsel will ask background questions as he's been
11 doing throughout the morning and the witness will
12 respond. If the question is meant to be tied to a
13 specific patent, counsel will make that clear.

14 HSC's counsel reserves his right
15 to use the background material for cross-examination
16 on any particular declaration. We reserve our right
17 to object to such use, as we believe such use may be
18 outside the scope of direct. So would be improper
19 cross-examination unless the witness is aware that
20 he's testifying about his declaration.

21 But, again, we are feeling our way
22 through -- through the issue. So with that

1 understanding in place, we can continue the
2 deposition.

3 I don't know if that helps.

4 THE WITNESS: It doesn't help me a
5 lot.

6 MR. MUKERJI: For you it's easy.
7 Just tell the truth.

8 THE WITNESS: Right.

9 BY MR. CHEN:

10 Q. So, Dr. Rubloff, right now I'm asking
11 you general information about the field of
12 semiconductor manufacturing. I just want to get
13 your understanding of some of the different
14 processes or terms that are used in that field.

15 Previously before we took a break, we
16 were talking about semiconductor process flow.

17 How is the semiconductor process flow
18 used in semiconductor manufacturing?

19 A. Well, the process flow is a description
20 of what -- what unit process do you do or what -- or
21 what batch or whatever process you do and what
22 process you do next. Then if you're going to do

1 lithography, what batch you're going to use. If
2 you're going to insert a characterization step to
3 qualify, if you think that means you screwed up,
4 you're going to do that and so on. So you basically
5 need a recipe for manufacturing.

6 Q. Is each unit process within the process
7 flow important?

8 MR. MUKERJI: Objection to form.

9 THE WITNESS: I don't have an
10 answer for that. Because there are many steps there
11 and some of them may be more important than others,
12 more critical. And if you ask -- if you use a term
13 like "important," then I want to know, well, what's
14 the metric by which you measure importance?

15 BY MR. CHEN:

16 Q. Are any of the steps extraneous?

17 MR. MUKERJI: Objection to form.

18 THE WITNESS: I guess the right
19 way to look at that is that if people had a
20 consensus they were extraneous, they wouldn't be
21 doing them. So at the time it's happening, it
22 doesn't appear to be extraneous, but it may be

1 someone will come up with a better idea and improve
2 the process flow and take out some steps or replace
3 them with other steps. But nobody would leave
4 something in, unless -- if they knew it was
5 extraneous, unless -- well, let me qualify that.

6 I could imagine -- this is very
7 hypothetical. I could imagine a condition where you
8 have steps 1, 2, 3 and you don't -- you realize you
9 don't really need step 2, but it does something
10 unintended and when you take it out, everything
11 falls apart. So 1, 2, 3 doesn't work.

12 So, for example, if there was a
13 delay in the wafer sitting out in the clean room too
14 long because you're doing a characterization step,
15 and somehow sitting out in the clean room caused it
16 to be oxidized further and you didn't know it, but
17 that was important. So if you were doing something
18 with that seemingly unneeded step that you didn't
19 know about, then that would be a deviation.

20 I mean, normally you say, if I
21 don't think I need it for anything, I'll just take
22 it out, but there are unintended consequences

1 sometimes. So that would be the occasional
2 exception, I guess.

3 I find the question is difficult
4 to deal with without specifics.

5 BY MR. CHEN:

6 Q. In the hypothetical that you just gave,
7 was that a real-world example that you encountered?

8 A. I have no idea. It was hypothetical.

9 Q. So somebody running a process flow,
10 would that person ever just take out a step and not
11 run it or add in a new step?

12 MR. MUKERJI: Objection to form.

13 THE WITNESS: They would not do
14 that in a manufacturing line, but they may be
15 experimenting with the process integration issues of
16 the sequence of a subsequence of steps and want to
17 do some experiments to see if they could get rid of
18 this one or replace it or something, something like
19 that. But that would be kind of an off-line
20 experiment.

21 It can be carried out certainly in
22 development environments, sometimes in manufacturing

1 even, but they know they're doing it and it doesn't
2 go to the same place where the product records go
3 typically.

4 BY MR. CHEN:

5 Q. So maybe as part of the development
6 process to try to improve or modify the process
7 flow?

8 A. Yes, but --

9 MR. MUKERJI: Objection to form.

10 THE WITNESS: -- you have to be
11 careful not to compartmentalize development versus
12 manufacturing. It's not a solid wall between them.

13 One of the surprises you learn in
14 manufacturing is that people are retuning unit
15 processes, sequences of processes, to try to get the
16 yield up or some other benefit from that. So they
17 may do experiments with dummy wafers or with -- with
18 some kinds of test wafers or sometimes even product
19 wafers to see if they can get the yield up.

20 BY MR. CHEN:

21 Q. How are steps differentiated from each
22 other within a process flow?

1 A. I don't know what differentiated. I
2 mean, you could name them. You could number them.
3 You could write a SOP, a standard operating
4 procedure. You could write a tool recipe.

5 I think we're kind of in a discussion
6 here which faces the obstacle that by trying to be
7 general about this, we miss what's really happening.
8 People want to be precise and say, we do this and we
9 do this and here's how we do that and then we do
10 this.

11 Q. Just so I understand, when you said
12 that people want to be precise and say, we do this
13 and we do this and here's how we do that and then we
14 do this, what are you referring to?

15 A. I was referring to the disadvantage of
16 trying to put kind of global terms on this.

17 Q. Okay.

18 A. You asked me -- in reference to your
19 previous question.

20 Q. I thought maybe you were referring to
21 what a process flow was, which is, you know, do this
22 and then you do this and then you do that.

1 That's not what you were referring to?

2 A. I've lost the argument.

3 Q. Okay.

4 A. I don't know where we were.

5 Q. All right.

6 A. Sorry. I've lost the thread of the
7 discussion already because it's a little bit vague.

8 Q. No problem.

9 A. That's what I meant by "lost the
10 argument."

11 Q. Are you familiar with the term
12 "chemical vapor deposition"?

13 A. Yes.

14 Q. And can we refer to it as CVD?

15 A. Yes.

16 Q. And you've had experience with CVD in
17 your prior work?

18 A. Yes.

19 Q. What is CVD?

20 A. CVD is a materials modification process
21 which uses chemically reactive gases to form new
22 kinds of materials that are reaction products of

1 those reactive gases on a surface, resulting in a
2 thin film of material being deposited.

3 Q. It is -- is it a deposition technique?

4 A. Yes.

5 Q. Are you familiar with the term
6 "physical vapor deposition"?

7 A. Yes.

8 Q. Can we refer to it as PVD?

9 A. Yes.

10 Q. And what is PVD?

11 A. PVD is a different type of deposition
12 technique which does not involve chemical reactions
13 to an appreciable extent in contrast to CVD. So
14 examples would be evaporation and sputtering in
15 particular, and the P stands for physical as opposed
16 to chemical.

17 Q. In PVD, do you have a target that then
18 you bombard with some ions and that causes material
19 to fall down onto where you want to make your
20 deposition? I'm trying to understand the PVD
21 process.

22 A. You said in PVD?

1 Q. Yeah.

2 A. There is -- there are several different
3 styles of PVD. One of them is called sputtering,
4 and I think that's what your referring to and that
5 does use ions to unmark the target.

6 Q. So sputtering is a specific form of
7 PVD?

8 A. Yes. Evaporation would be another one.

9 Q. How does the evaporation work?

10 A. In evaporation, you heat a target
11 material -- there are different ways to do that --
12 to a temperature such that the atoms of that
13 material jump off the surface. They evaporate.
14 Some of them have enough thermal energy that they
15 can leap the surface. And when they do that, they
16 have some velocity going someplace and so they end
17 up on some other surface. One example being that we
18 care about is your wafer.

19 Q. Thank you.

20 Are you familiar with the term "rate of
21 deposition"?

22 A. Yes.

1 Q. What does rate of deposition mean?

2 A. Well, typically we think of rate of
3 deposition in units of nanometers per second, or
4 angstroms per minute, or a certain amount of the
5 deposited material coming onto the surface per unit
6 time.

7 Q. So for a certain time period, the rate
8 of deposition will determine how much material is
9 deposited?

10 A. You mean a constant rate of deposition?

11 Q. Yes.

12 A. So if you have a constant deposition
13 rate, then that -- and do you know how long you're
14 doing that, that tells you how much you have left
15 deposited at the end when you stop.

16 Q. When you're depositing material by CVD
17 process, is there a difference between the rate of
18 deposition on horizontal surfaces and vertical
19 surfaces?

20 A. Yes and no. Mostly no because chemical
21 vapor deposition can -- and is chosen for this --
22 can achieve essentially the same deposition rate on

1 horizontal and vertical surfaces. We call that
2 phenomenon conformality, high conformality, or group
3 step coverage and so on.

4 On the other hand, it's not perfect and
5 it can depend on at least two fundamental factors.

6 One of them is the process chemistry you use.

7 Because there are regimes of process chemistry that
8 are rate limited by kinetics and that's where you
9 can get good conformality, and there are other
10 regimes that are rate limited by transport.

11 And in that case, it depends on the
12 geometry and specifics of gas flow distributions and
13 three dimensions in your reactor as those gases are
14 approaching your wafer.

15 So the second thing besides the
16 individual process chemistry that's important is,
17 you have to know something about -- well, as part of
18 that, you have to know something about what regime
19 you're in, kinetic or transport-limited, and what
20 details are there.

21 But the other thing is the equipment
22 design. Because as you enter a regime, which is

1 affected at all by transport, then the gas flows of
2 bringing these reactive species to the surface are
3 -- can be quite complicated and that has led to the
4 challenge of designing good CVD reactors that can
5 deposit uniformly over large wafers and into
6 complicated three-dimensional micro- or
7 nano-geometries which are the patterns you're trying
8 to make.

9 Q. When you said "step coverage," what
10 does step coverage mean?

11 A. Well, step coverage is a kind of legacy
12 term from an earlier era when people would evaporate
13 or sputter over structures where you might have a
14 raised region compared to a lower region, like a
15 plateau, and you'd want to have the sidewall covered
16 with, if you can, the same thickness as you have on
17 the top and on the lower plat -- lower level.

18 And so that's called step coverage.
19 And so you asked, okay, if it's -- if it's a
20 thousand angstroms on the top and away from the
21 step, what is it on the side of the step?

22 Q. So good conformality and good step

1 coverage mean the same thing?

2 A. It means similar things. In my view,
3 we now have the requirement in a DRAM capacitor or a
4 stack capacitor or shallow trench isolation,
5 whatever it is, we have very high-aspect-ratio
6 structures in the devices we're making.

7 That means we have narrow trenches, for
8 example, that are very deep and so in those cases,
9 you really wouldn't talk about that as step coverage
10 so much as you would conformality. I think that the
11 term "step coverage" is not as -- not as current but
12 legitimate.

13 Q. So if I were to say something had 50%
14 step coverage, for example, that would mean that the
15 thickness of the deposition on the horizontal
16 surface is -- sorry -- I mean on the --

17 A. On the vertical surface.

18 Q. Right.

19 If I were to say that something had 50%
20 step coverage, that means the thickness of the
21 deposition on the vertical surface is half as much
22 as the thickness of a deposition on the horizontal

1 surface; is that correct?

2 A. Partly, although there are different
3 ways you can define it. Because typically when you
4 have the vertical surface being covered, it won't be
5 uniform coverage from the top to the bottom. So you
6 may get thicker deposition near the top of the
7 vertical step, the side of the step, than at the
8 bottom. So you really should prescribe how you're
9 measuring step coverage.

10 Q. Okay. How is step coverage typically
11 measured?

12 A. I think people use what they -- what
13 they are comfortable with for communicating results
14 to their collaborators, colleagues, and so on.

15 Q. Okay.

16 A. I mean, you know, you could pick a
17 simple measure like, what's the average over the
18 vertical surface?

19 Q. Okay.

20 A. Something like that.

21 Q. Is the thickness at the top of the step
22 always thicker than the bottom of the step?

1 A. Usually, but I wouldn't say always
2 because I haven't conjured up reactor designs and
3 gas flow consequences, particularly in a
4 transport-limited CVD regime. So there might be
5 exceptions.

6 Q. But in your experience, you haven't
7 seen any?

8 A. Not typically, no.

9 Q. And so if somebody told you this
10 process has 50% step coverage, what would that mean
11 to you?

12 A. I think the only thing I could conclude
13 from that, because they didn't tell me how they
14 measured step coverage, is that you can't count on
15 the layer being deposited on the vertical or side
16 surface looking just like the layer on the top.

17 Q. It would be thinner; right?

18 A. Probably thinner.

19 The only exception I can think of right
20 now is, suppose it's really rough. Sometimes you
21 deposited material and it's a thin film material
22 which has a grain structure or it's

1 nucleation-controlled, like I told the story earlier
2 about finding a way to make rough silicon surfaces,
3 and so there are exceptions that can happen. Then I
4 would know. That would be a difference.

5 Q. Are you familiar with the term
6 "anisotropic etching"?

7 A. Yes.

8 Q. What is anisotropic etching?

9 A. Anisotropic etching refers to etch
10 rates such that the etch rate on a horizontal
11 surface is different from that on a vertical
12 surface. It's kind of the dry etching analogy to
13 the CVD conformality question.

14 Q. How is -- how is the etch rate on the
15 horizontal surface different than the etch rate on
16 the vertical surface in anisotropic etching?

17 A. I'm sorry. I don't know what you're
18 looking for here when you say "how is it." You mean
19 why does it happen?

20 Q. What is the difference?

21 You said that anisotropic etching
22 refers to etch rates such that the etch rate on the

1 horizontal surface is different than that on the
2 vertical surface.

3 What do you mean how -- that the etch
4 rates are different?

5 A. They're different numbers. If one is
6 etching at a rate of 50 and the other is at 12,
7 they're different.

8 Q. Is the etch rate of the horizontal
9 surface higher than the etch rate of the vertical
10 surface?

11 A. If it's anisotropic etching, yes.

12 Q. Is anisotropic etching the same thing
13 as dry etching?

14 A. Not necessarily.

15 Q. So dry etching -- sorry. Let me ask
16 you this.

17 What is isotropic etching?

18 A. Isotropic etching is a condition in
19 which the rate at which a surface is removed is the
20 same on all surfaces. So horizontal or vertical,
21 substantially the same.

22 Q. So dry etching can be either

1 anisotropic or isotropic?

2 A. Yes.

3 Q. How about wet etching?

4 A. What about it?

5 Q. I'm sorry.

6 Can wet etching -- well, let me just
7 start over.

8 What is wet etching?

9 A. Wet etching is the use of liquid
10 chemicals, such as acids, for example, to remove
11 material from a surface.

12 Q. And is wet etching anisotropic or
13 isotropic?

14 A. It can be either.

15 Q. Okay. And I don't remember if I asked
16 you before.

17 What is dry etching?

18 A. Dry etching is removal of material
19 using a vapor environment. So there's no liquid
20 involved. Typically a plasma is involved so that
21 you have plasma species available to do the etching.

22 Q. Are you familiar with lithography

1 techniques?

2 A. Yes.

3 Q. What is lithography?

4 A. The word "lithography" can be used in
5 at least two different contexts. One is the
6 exposure of patterns, the transfer of -- the
7 exposure of patterns of light typically, but could
8 be electron or ion beams, into material so as to
9 modify that material, typically a mask, and then to
10 use that mask for other things.

11 So that use of the term "lithography"
12 and they -- the two meanings kind of merge together.
13 Sorry, but that's how I see it.

14 So one way to talk about lithography is
15 the exposure of a patterned beam using a mask or
16 direct light of a particle to form patterns in a --
17 in a material, and so it has to do with optics or
18 electrons or photons in patterns.

19 The broader meaning is doing
20 lithography to be able to typically remove material
21 in some regions and not in others. So that combines
22 typically something like the exposure part -- that's

1 the first version of the word that I used -- with
2 etching of some kind so that that pattern that was
3 made is transferred into the thin film material.

4 And I think those -- those two somewhat
5 different versions are really used interchangeably.

6 Q. So let me see if I understand what
7 you're saying.

8 There are two definitions of
9 lithography which have kind of maybe bled into each
10 other a little bit.

11 One is using lithography to strictly
12 refer to the formation of the patterned mask;
13 whereas, the other term refers to both the formation
14 of the patterned mask as well as the etching process
15 that is used to transfer that pattern onto the
16 material below?

17 A. Yeah, and the reason I make the
18 distinction is -- I mean, I teach this stuff; right?
19 I've got slides on this. Is that if you're talking
20 about how you make patterns by using masks and
21 magnifying, demagnifying, and so on, you're really
22 talking about optics or electron -- photon optics or

1 electron optics, ion beam optics, and so you're
2 talking about a tool.

3 And there's a whole world of capital
4 equipment vendors that make that their specialty.
5 They don't necessarily do the etching and they don't
6 necessarily develop the photoresistor or the resist
7 that's sensitive to that pattern.

8 Most generally if I say typical
9 lithographic process, I will mean I had something on
10 the surface, I took a mask, I transferred the light
11 from that mask into a photoresist layer that I put
12 down and treated appropriately and developed so it
13 had openings and closed parts, and then I used that
14 to -- as a mask for etching.

15 So in that sense, lith -- the exposure,
16 the lighting, and the etching are all part of the
17 word lithography.

18 Q. All right.

19 A. I'm sorry, but I don't know how not to
20 be a little bit vague on it. And it's not vague,
21 but I need to explain that people use the term in
22 different ways.

1 Q. Okay. And how is the photoresist used
2 in lithography?

3 A. In optical lithography?

4 Q. Let's use the lithography to refer to
5 both the optical aspect as well as the subsequent
6 etching in photoresist.

7 A. No, that's not what I was
8 distinguishing.

9 So if I want to make a pattern, I can
10 do it by shining light or not shining light --

11 Q. Oh.

12 A. -- at these locations.

13 Q. As opposed to ions?

14 A. As opposed to ions and electrons.

15 Q. Sorry. All right.

16 And the photoresist is used with the
17 light?

18 A. Right. But even in electron or ion
19 beam lithography, particularly electron beam, some
20 people would just say "photoresist" because they're
21 so used to it, but it's an electron beam resist.

22 Q. Okay.

1 A. Or, for that matter, X-ray resist.

2 Q. In semiconductor manufacturing, do they
3 typically use light or the ion beam?

4 A. Rarely ion beam because it doesn't have
5 a high throughput. Usually light and these days
6 it's ultraviolet light. But there are important
7 uses for electron beam lithography as well in
8 manufacturing and that's particularly to make the
9 mask for optical lithography.

10 Q. Okay. For now let's talk about light.

11 A. Okay.

12 Q. Okay. Because that's the more
13 common --

14 A. Yeah.

15 Q. -- form.

16 How is the photoresist used in
17 lithography using light?

18 A. Yeah. You can say pattern --

19 Q. Okay.

20 A. -- so it's simple.

21 If I have a layer of material and I
22 want to remove it from one region and leave it in

1 another, I put on a layer of photoresist, which is
2 typically a polymer that is sensitive to light. So
3 I make this -- this cover. I then take a mask, an
4 optical mask, shine light through it, and image it
5 one way or another on the photoresist. So the light
6 hits this part of the photoresist, let's say the A
7 part of the photoresist, but doesn't hit the B part
8 of the photoresist.

9 The light causes photochemical changes
10 in the resist and can transform that resist from
11 being soluble to insoluble in the right chemical or
12 insoluble to soluble. So it modifies the
13 photoresist. That's why we call it photoresist.

14 And then you can remove one part or the
15 other in a process that's called develop, where you
16 basically dissolve one piece or the other. I'll
17 hesitate to go into positive and negative
18 photoresist and so on.

19 So that means that you now have the
20 photoresist in one -- in one place A but not in B,
21 and so if I have the photoresist on A on my material
22 and I put it in an etching solution or a dry etching

1 environment, the mask is protecting the A region.
2 So it won't -- the material under it won't be
3 removed, but where the mask isn't present, the
4 material will be removed.

5 Q. So the remaining portion of the
6 photoresist acts as a mask?

7 A. Yes, and then, of course, you remove it
8 at the end.

9 Q. When you say "remove it at the end,"
10 you mean remove it at the completion of the etching
11 process?

12 A. Typically that's when you'd remove it,
13 but not necessarily then. It depends what your next
14 step is.

15 Q. Why do you -- how do you remove a
16 photoresist?

17 A. Typically you dissolve it in liquid
18 chemicals, but you could move it by dry processes as
19 well. For example, by ashing.

20 Q. Why is it necessary to remove the
21 photoresist?

22 A. The photoresist is just there to help

1 you do the patterning or to do lithography at that
2 point. Now, I should be careful because there are
3 exceptions.

4 So there are devices that use a
5 photoresist called SU8, which can actually be used
6 to make devices for microfluidics, for example. So
7 sometimes you're going to continue to use it even as
8 the device is completely finished, but in
9 semiconductors typically you will remove it either
10 after you've done one etching step with the mask,
11 the photoresist mask in place or at some later time.

12 Q. When you are depositing the
13 photoresist, does the surface that you're depositing
14 it on have to be flat?

15 A. When you're depositing the photoresist?
16 No, it does not have to be flat. I don't know how
17 flat you mean, but if it had to be really flat, you
18 wouldn't have a very good strategy for using
19 lithography as a patterning technique to make
20 three-dimensional devices.

21 Q. Okay.

22 A. But there is some tolerance too. There

1 are -- there are situations where you would have
2 trouble making the profile of photoresist thickness
3 versus position over underlying topography that's
4 too demanding.

5 Q. You said if it had to be really flat,
6 you wouldn't have a good strategy for using
7 lithography as a patterning technique.

8 I'm sorry. I don't really understand.

9 A. So when we make devices, they're
10 three-dimensional.

11 Q. Right.

12 A. They're also usually not very
13 interesting usually; right? So if you make --
14 suppose you make a gate electrode.

15 Q. Right.

16 A. You know what a gate electrode is?

17 Q. Yeah.

18 A. And after that, you're going to have to
19 make some other structures; right? Because a gate
20 electrode in isolation doesn't do anything. You
21 have to make contacts, the source/drain, and stuff.
22 Those are going to be somewhere by lithography as a

1 pattern strategy, exposure and etch.

2 So if you couldn't put down a
3 photoresist layer and use optical lithography, how
4 would you make the rest of the device?

5 So lithography and photoresist have to
6 be reasonably compatible with having a
7 three-dimensional topography at some level
8 underneath.

9 Q. So you can deposit a photoresist on a
10 three-dimensional surface with topography?

11 A. Yeah, within limits.

12 Q. Okay. Are you familiar with chemical
13 mechanical polishing?

14 A. Yes.

15 Q. And we can refer to chemical mechanical
16 polishing as CMP; right?

17 A. Yes.

18 Q. Okay. And what is CMP?

19 A. CMP is a planarization technique. So
20 as you make these layers --

21 Q. Right.

22 A. -- in three dimensions, the tendency is

1 for the topography of the surface to get more and
2 more structure, higher aspect ratios and the like,
3 and so sometimes you will want to planarize that
4 surface. CMP was developed to deal with this
5 problem in the interconnect domain.

6 It was actually done at IBM while I was
7 there, and we weren't allowed to talk about it. But
8 that was when people were trying to figure out, as
9 you make a wire here, then a wire above it, then a
10 wire above it, pretty soon you have a very rough
11 surface. And so how are you going to do lithography
12 on that? How are you going to make anything on
13 that? It's too difficult.

14 So people developed strategies for
15 planarization, and CMP was pivotal with that. It's
16 one of the techniques, but it's probably the most
17 advanced technique for doing a good job of
18 planarization.

19 Q. You said you have a very rough surface,
20 and how are you going to do lithography on that?

21 A. For example.

22 Q. Right. So CMP is used to planarize a

1 surface so that you can do lithography?

2 A. And -- and you can make reliable
3 structures. So these days there are -- I don't
4 know -- eight levels of interconnection wiring on a
5 chip. And what's done now in the -- in the current
6 generation of technology -- and CMP was part of
7 developing that capability -- is at each level,
8 you'll planarize the surface and then build another
9 layer of wires that come up through an insulator and
10 then do something in a horizontal direction, but
11 it's planar.

12 Q. And are you using the CMP to planarize
13 the -- the photoresist?

14 A. No. No. To planarize the materials
15 that have been deposited.

16 Q. Okay. So you're using it to planarize
17 the material upon which you would deposit the
18 photoresist?

19 A. Or upon which you will deposit some
20 other material.

21 Q. Okay. Would you ever use CMP to
22 planarize the material that had a photoresist on top

1 of it?

2 MR. MUKERJI: Objection to form.

3 THE WITNESS: I don't understand
4 the question. You don't -- I don't know of anyone
5 and any attempts to use CMP on photoresist.

6 BY MR. CHEN:

7 Q. What are some other planarization
8 techniques?

9 A. Well, another one is called etchback,
10 which is a kind of ion beam plasma, and that was the
11 standard before CMP was developed.

12 Q. Oh, okay. How does etchback work?

13 A. Etchback uses typically ions like you
14 would use in sputtering to move material as
15 uniformly as possible and be -- what it basically
16 does, it homogenizes the surface. So if you've got
17 a big bump someplace here, that will etch faster, be
18 removed faster. So it does some planarization.

19 Q. Do you use a mask with etchback
20 technique?

21 A. Well, people use masks for things like
22 collimated sputtering, but I don't know of any

1 examples with etchback. That doesn't mean there
2 aren't any. I just haven't seen it.

3 Q. I just have a few more of these
4 background type of questions, probably take another
5 15 to 20 minutes, but I don't know how hungry you
6 guys are, whether you want to stop.

7 MR. MUKERJI: Would you like to?

8 THE WITNESS: I'm all right.

9 MR. MUKERJI: Are you okay?

10 THE WITNESS: Yes.

11 MR. MUKERJI: So what I'd suggest
12 is, why don't we do the 15 to 20 minutes questions
13 and then take our lunch break.

14 MR. CHEN: Sure. That sounds
15 good.

16 BY MR. CHEN:

17 Q. Are you familiar with the term
18 "dielectric layer"?

19 A. Yes.

20 Q. Is it the same as an insulation layer?

21 A. The two terms are used pretty much
22 interchangeably, but I'm not sure that that's a

1 universal valid way of looking -- to look at it.

2 I'd have to think about whether there's some
3 exceptions.

4 Q. What are some common materials used to
5 form a dielectric layer or insulation layer?

6 A. In the sense?

7 MR. MUKERJI: Objection.

8 BY MR. CHEN:

9 Q. Actually, let me go back.

10 So for you, dielectric layer and
11 insulation layer can be used interchangeably, but
12 you're not sure whether that is universal?

13 A. Well, okay. So dielectrics should have
14 a bandgap and be insulating, but they aren't always.

15 Q. Okay.

16 A. So with aluminum oxide I can tell you,
17 it is metallic. So there are exceptions to this,
18 but in the field of semiconductor electronics where
19 the number of materials that are insulators or
20 dielectrics, generally speaking, people casually use
21 them, the terms interchangeably.

22 Q. Okay. Dielectric is more of a

1 characteristic of a material, whereas, insulation --
2 insulating might be more of a functional term; is
3 that fair?

4 A. I haven't thought about this
5 distinction.

6 Q. Okay. What is insulation layer?

7 A. Insulation layer to me means that if
8 you have a voltage across that material, there can
9 be a current passing through it. However, it's more
10 complicated than that because most materials have
11 leakage currents or means by which there can be a
12 tiny current, and so we talk about what's the
13 leakage current in this material under certain
14 voltage conditions. Also, what's the breakdown
15 field?

16 Because if you press high enough of
17 voltage over a thin enough material, you can change
18 the material, actually, and make it into a kind of
19 conductor.

20 Q. Let's say I had a layer that was made
21 of silicon oxide. Would that be an insulation
22 layer?

1 A. Typically it should be, if the quality
2 of the material is good and you're not stretching it
3 to very high electric field strengths and if it's
4 not too leaky.

5 For example, people used to do what's
6 called sputtered quartz, which is you take a target
7 for sputtering that's made of silicon dioxide and
8 you sputter it onto your -- your wafer, and it makes
9 rather inferior material compared to other -- other
10 ways. So.

11 Q. What if I had a layer of silicon
12 nitride? Would that be -- also be an insulation
13 layer?

14 A. Yes, if it's decent quality material.
15 Silicon oxide, silicon dioxide, silicon nitride are
16 typically regarded as insulators, and people usually
17 use them as insulators. I guess the caveat that you
18 hear me making is, you can take a good material and
19 mess it up.

20 Q. Okay. Are silicon nitride and silicon
21 oxide largely interchangeable?

22 MR. MUKERJI: Objection to form.

1 THE WITNESS: For what metric do
2 you have in mind?

3 BY MR. CHEN:

4 Q. In terms of their use as an insulating
5 material.

6 A. Well, it depends -- it still depends on
7 what you mean. If you want them to -- to just be
8 insulators, well, they'll have different properties
9 as insulators, different breakdown fields, different
10 leakage currents. Even -- even silicon dioxide made
11 by different techniques will have different
12 properties. So you can't say they're really
13 interchangeable from an electrical point of view.

14 And then when you recognize that you're
15 going to have to do some kind of thin film
16 deposition, all these things we do in semiconductor
17 manufacturing, the properties of those materials can
18 be very different in those processes.

19 Q. Okay. Are they formed differently?

20 A. Yes, typically. I mean, they have
21 different atoms, so they certainly have to be made
22 differently.

1 Q. All right. I meant like, are different
2 deposition techniques used to deposit silicon
3 nitride as opposed to silicon oxide?

4 A. Well, for both of them, there are a
5 range of ways to do them. CVD processes, different
6 precursors or reactants present in the CVD process.
7 Growth of silicon dioxide from oxygen or water or
8 N2O, nitrous oxide. There are many ways to make
9 these, and the properties depend on how they're
10 made.

11 Q. Are you familiar with the term
12 "spacer"?

13 A. Yes.

14 Q. Okay. What is a spacer?

15 A. I think this gets into the domain of --
16 of how is it construed, and I think that could be
17 different depending on the application you're
18 talking about, and I think it also has to do with
19 which patent we're talking about.

20 I don't think it's very helpful if I
21 make up some kind of answer to that that's so
22 generic that we don't know what it means.

1 Q. Is there a generally understood
2 definition of spacer in the field of semiconductor
3 manufacturing?

4 A. Generally understood? I'm not sure how
5 specific it would be, and I certainly understand
6 that there are different properties that one might
7 want from a spacer. For example, I don't want
8 alkali ions to be able to get through it or I don't
9 want electrons to get through it.

10 A spacer is, you know, the common
11 meaning -- the common thought one has from the word
12 is something is kept a distance from something else.
13 I can't be more specific than that. We really have
14 to talk about an application.

15 Q. What are some of the functions of a
16 spacer?

17 MR. MUKERJI: Objection to form.

18 THE WITNESS: I can't answer that
19 without being specific about device structure,
20 application or patent. That's far too general.

21 BY MR. CHEN:

22 Q. To you spacer doesn't have -- so, for

1 example, in the field of semiconductor
2 manufacturing, if somebody used the term "spacer,"
3 you wouldn't know what they meant unless they
4 referred to a specific patent?

5 MR. MUKERJI: Objection to form.

6 THE WITNESS: Of course I'd know
7 what they meant if they asked the question in the
8 context of a device structure or a patent or a
9 process flow and device integration.

10 BY MR. CHEN:

11 Q. Okay. How about a spacer formed on the
12 sidewall of a gate electrode?

13 MR. MUKERJI: Objection to form.

14 BY MR. CHEN:

15 Q. What are the functions of a spacer
16 formed on the sidewall of a gate electrode?

17 A. I think that's too general a question.
18 For example, it doesn't occur in main line silicon
19 technology, but there's something called an ISFET,
20 an ion-selective field-effect transistor, and the
21 function of that, of anything that you might
22 consider a spacer there might be very different from

1 that in a CMOS device.

2 You're asking a question which isn't
3 specific enough for me to answer.

4 Q. So --

5 A. I'll be able to answer it when we get
6 to the patents.

7 Q. Sure. I just want to understand what
8 the roadblock is here.

9 You're saying a spacer has different
10 definitions depending on context; is that what
11 you're saying?

12 A. No. I'm saying that -- I'm saying that
13 unless I understand an environment where the
14 question is being asked, I don't know how to think
15 about what properties it should have, which is, I
16 think, the question you asked initially.

17 Q. Well, I'm asking generally what a
18 spacer -- the definition of a spacer is in the field
19 of semiconductor manufacturing and what type of
20 functions a spacer might have.

21 You said that you needed specific, you
22 know, application or a specific patent to be able to

1 answer that question.

2 I just want to understand whether
3 you're saying that the reason you can't answer my
4 question is because spacers have different
5 definitions depending on the context.

6 MR. MUKERJI: Objection to form.

7 THE WITNESS: I don't think I can
8 be helpful with this question. It's -- it's still
9 too vague for me.

10 BY MR. CHEN:

11 Q. Okay.

12 A. Now, I already said that it could be
13 something with regard to ion transport. It could be
14 something with regard to electrical leakage current.
15 It could be something to make sure that the field
16 isn't too high. I don't know. I haven't thought
17 hard about all the dimensions, but there are a lot.

18 But I certainly know what a spacer is
19 in the context of a specific device application.

20 Q. So there's no one definition of spacer
21 that can apply to multiple device applications; is
22 that correct?

1 A. I don't know.

2 MR. MUKERJI: Objection to form.

3 THE WITNESS: I don't know. I
4 haven't thought about it that way. That's too
5 general.

6 I was asked to address specific
7 patents and to -- and to make comparisons between
8 prior art and patents at issue here, and that
9 doesn't include my kind of dreaming up a
10 generalization that should be applicable across a
11 field as broad as semiconductor devices.

12 BY MR. CHEN:

13 Q. Yeah. Nobody is asking you to dream up
14 a definition.

15 I'm just asking whether you're familiar
16 with a definition of spacer as it's generally used
17 in the field of semiconductor manufacturing.

18 A. Yes.

19 Q. And what is that definition?

20 A. It's a -- if there's a general way to
21 do that, I'm trying to represent something general
22 here, it has some function in ensuring that there's

1 a spatial separation between something and something
2 else for properties which at this -- at this point
3 in the discussion we're not specifying.

4 Q. Are you familiar with the term
5 "isolation region"?

6 A. Yes.

7 Q. What is an isolation region?

8 A. Typically that term refers to the fact
9 that if I want an active device, like a transistor,
10 to operate correctly and I have more than one such
11 on the surface, I don't want them connected to each
12 other because then I can't wire circuits to use
13 those various transistors. So I need some
14 electrical isolation between them.

15 Q. Is STI a form of isolation region?

16 A. What do you mean by "STI"?

17 Q. Shallow trench isolation.

18 A. Yes, it is.

19 Q. Is field oxide a form of isolation
20 region?

21 A. Yes.

22 Q. Are you familiar with the term "barrier

1 layer"?

2 A. Barrier layer?

3 Q. Uh-huh.

4 A. Yes.

5 Q. What is a barrier layer?

6 A. A barrier layer is a barrier to
7 something moving, but I have to know the application
8 to be able to say what that is.

9 Q. Okay.

10 A. It could be a barrier to transport a
11 species. It could be a barrier to chemical
12 reactivity. It's a lot.

13 Q. So the definition of barrier layer that
14 you gave as a barrier to something moving, that's a
15 more general high level definition; correct?

16 A. Compared to what?

17 Q. Compared to a definition that you might
18 give which is more specific within a particular
19 context.

20 MR. MUKERJI: Objection to form.

21 BY MR. CHEN:

22 Q. I just want to understand your answer

1 and kind of the difficulty in giving a more specific
2 definition.

3 You said that:

4 A barrier layer is a barrier to
5 something moving, but I have to know the application
6 to be able to say what that is.

7 A. Well, let me give you an example. If I
8 have a metal and then a layer of high quality
9 insulator and then some other metal, and these two
10 aren't shorted together and they don't leak very
11 much, I could call that layer an insulating barrier
12 for electron transport.

13 Q. Right.

14 A. Right? If I have dopants in silicon
15 and I don't want them to leave the silicon, I could
16 put a nitride layer or something there and then I
17 have oxide or something above that, and that might
18 serve -- I'm not sure, I haven't thought through
19 that example -- that might serve to prevent
20 diffusion of atoms or ions to it.

21 So that's a diffusion barrier and both
22 are well known, but they're completely different.

1 Q. Right. Okay. So generally a barrier
2 layer is a barrier to something moving, but
3 depending on the application, there may be a more
4 specific definition for barrier layer depending on
5 its purpose such as a diffusion barrier?

6 A. Well, I think the way you've phrased it
7 is too specific.

8 Q. Okay.

9 A. Because it doesn't include a chemical
10 reaction barrier.

11 So if I have metal -- transition metal
12 connected to silicon, it may -- it is likely to
13 react at the interface and form a new material, a
14 silicide. So if I don't want that to happen, then I
15 need some kind of barrier layer to prevent it.

16 But I don't think characterizing that
17 as a reaction -- what should I call it? -- chemical
18 reaction barrier is encompassed in what you said
19 about something moving.

20 Q. Okay.

21 A. Because nothing is moving from one side
22 to the other if there's a chemical reaction.

1 Q. Okay. I was just using the definition
2 that you gave.

3 A. I understand that.

4 Q. So is it fair to say that barrier layer
5 is a term that, depending on its application or
6 context, could have different meanings?

7 MR. MUKERJI: Objection to form.

8 THE WITNESS: Can have different
9 functions.

10 BY MR. CHEN:

11 Q. Dr. Rubloff --

12 MR. MUKERJI: Mr. Chen, we're --
13 I'm sorry. We're past the 20-minute.

14 MR. CHEN: Sure. Just one more.

15 MR. MUKERJI: Do you have much
16 more?

17 MR. CHEN: No, I have just a few
18 more.

19 BY MR. CHEN:

20 Q. Is it also fair to say then that
21 "spacer" is a term that, depending on its
22 application or context, could have different

1 meanings?

2 MR. MUKERJI: Objection to form.

3 THE WITNESS: Could have different
4 functions.

5 BY MR. CHEN:

6 Q. What is the distinction you're drawing
7 between function and meaning?

8 A. I don't know what "meaning" means.

9 MR. CHEN: Okay. Why don't we
10 break for lunch.

11 (Whereupon, at 12:15 p.m., a
12 luncheon recess was taken.)
13
14
15
16
17
18
19
20
21
22

AFTERNOON SESSION

(1:09 p.m.)

GARY W. RUBLOFF, PHD

called for continued examination and, having been
previously duly sworn, was examined and testified
further as follows:

EXAMINATION (CONTINUED)

BY MR. CHEN:

Q. Welcome back, Dr. Rubloff.

THE REPORTER: Exhibit 2.

(Document marked, for
identification purposes, as Rubloff Exhibit No. 2.)

MR. CHEN: We can mark his errata
as Exhibit 3.

(Document marked, for
identification purposes, as Rubloff Exhibit No. 3.)

MR. MUKERJI: This is 2?

MR. CHEN: Yeah.

MR. MUKERJI: And the errata is 3?

MR. CHEN: Right.

BY MR. CHEN:

Q. Dr. Rubloff, I've asked the court

1 reporter to mark as Exhibit No. 2 your declaration
2 submitted in connection with Samsung's IPR of the
3 '997 patent.

4 I've also asked the court reporter to
5 mark as Exhibit No. 3 the errata to this declaration
6 that you provided earlier this morning.

7 Just take a few quick moments to look
8 over these documents.

9 A. (Reviewing document).

10 Q. Okay. Dr. Rubloff, is Exhibit No. 2
11 your declaration submitted in connection with the
12 IPR of the '997 patent?

13 A. Yes.

14 Q. And Exhibit 3 is your errata to that
15 declaration; correct?

16 A. Yeah.

17 Q. Does this declaration and the errata
18 contain any and all relevant opinions you have
19 regarding issues related to Samsung's petition for
20 review of the '997 patent?

21 MR. MUKERJI: Objection to form.

22 THE WITNESS: Well, this looks

1 like my complete declaration, but I haven't read the
2 petition that they made.

3 That's a different document;
4 right?

5 I've looked -- I've looked at it,
6 but I haven't studied.

7 BY MR. CHEN:

8 Q. You understand that you submitted your
9 declaration to support Samsung's petition?

10 A. Yes, I understand that.

11 Q. All right. Do you have any opinions
12 regarding issues relevant to Samsung's petition for
13 review of the '997 patent that were not included in
14 your declaration or your errata?

15 MR. MUKERJI: Objection to form.

16 THE WITNESS: The first part of
17 that was? I'm sorry.

18 BY MR. CHEN:

19 Q. Do you have any opinions regarding
20 issues relevant to Samsung's IPR of the '997 patent
21 that were not included in your declaration or the
22 errata?

1 MR. MUKERJI: Same objection.

2 THE WITNESS: Well, since I
3 haven't paid attention to the petition that they
4 submitted to the IPR board, I don't really know the
5 answer to that.

6 But my -- my review is here in my
7 declaration, and it covers all the conclusions that
8 I drew.

9 BY MR. CHEN:

10 Q. Okay. So you don't have any other
11 opinions related to the validity of the '997 patent
12 that were not included in your declaration; correct?

13 A. I think I've got most of them right
14 but, you know, that I've included everything that I
15 intended to include. It may be there's something
16 that will come up in discussion. I don't know.

17 Q. Sitting here today, you're not aware of
18 any other opinions related to --

19 A. Oh.

20 Q. -- the '997 patent --

21 A. No.

22 Q. -- that you failed to include in your

1 errata --

2 A. No. No, I don't know of any I failed
3 to include.

4 Q. -- or your declaration?

5 Okay. Other than the issues discussed
6 in your errata, are you aware of any other errors or
7 omissions in your declaration?

8 A. I don't think so.

9 Q. So your declaration and your errata
10 contain a complete recitation of all the opinions
11 that you have regarding the validity of the '997
12 patent; correct?

13 MR. MUKERJI: Objection to form.

14 THE WITNESS: Well, with the
15 proviso that this is a summary of those. There
16 certainly are more elucidation of detail to come
17 from, but this is a good summary that I'm
18 comfortable with of my opinions about the '997
19 validity.

20 BY MR. CHEN:

21 Q. Why didn't you include the additional
22 detail when you were preparing your original

1 declaration?

2 A. It's not that I didn't include the
3 additional. There's no substantial detail that I
4 feel is necessary here to address the questions I
5 was asked to look at, which is compare certain prior
6 art references to the claims of the '997 and see if
7 that prior art matches onto the claims of the '997.

8 So I think I've done an adequate job of
9 that, but there's always more elucidation that could
10 -- could be brought in, and I could make it 250
11 pages long. I don't think it's very useful.

12 Q. So you included all the relevant
13 details; correct?

14 A. Well, depends what "relevant" means.
15 The essential details maybe.

16 Q. Okay. You included all the essential
17 details?

18 A. That's probably a fair statement.

19 MR. CHEN: Exhibit 4.

20 (Document marked, for
21 identification purposes, as Rubloff Exhibit No. 4.)

22 BY MR. CHEN:

1 Q. So, Dr. Rubloff, I asked the court
2 reporter to mark as Exhibit No. 4 a patent titled
3 "Method For Forming Self-Aligned Contact Hole,"
4 which is the '997 patent.

5 If you can just take a quick moment to
6 look over the document.

7 A. (Reviewing document).

8 Q. So as I ask you questions about your
9 declaration, if you need to refer to the patent, you
10 have it. If you need other documents, let me know,
11 and we'll introduce them into the record so you can
12 reference them.

13 Did you read the '997 patent?

14 A. Yes.

15 Q. When did you first read the '997
16 patent?

17 A. I guess it was at least six months ago.

18 Q. Is that when you were first engaged to
19 work on the IPR directed at the '997 patent?

20 A. Yes.

21 Q. And you understand the contents of the
22 '997 patent; correct?

1 A. Yes.

2 Q. Looking at Exhibit 2, which is your
3 declaration, if you could go to paragraph 11, which
4 is on page 8 of Exhibit 2.

5 A. Uh-huh.

6 Q. How did you arrive at your definition
7 of a person of ordinary skill in the art?

8 A. Well, I think I said something about
9 that earlier.

10 When I look at this patent, it involves
11 process integration understanding, and I believe
12 that a master's level training in the disciplines
13 that I list here is pretty typical for people who
14 work in this industry and would give them some idea
15 about unit processes and maybe the relationship
16 between them, but typically not so much insight into
17 process integration.

18 So I included the two to three years of
19 experience as what I see students developing in
20 their first job in this industry that would be
21 necessary to -- to really have the skill to deal
22 with the process integration questions that are in

1 the '997 because the '997 deals with the sequence of
2 steps and the structural consequences of that.

3 Q. Does the sequence of steps affect the
4 structure that would form through the manufacturing
5 process?

6 A. Do you mean the order in which one does
7 it, or what the composition of the sequence is?
8 What processes are in? What processes are out?

9 Q. Let's start with the order. Does the
10 order of steps affect the structure that you are
11 forming with the process?

12 A. It can.

13 Q. But not always?

14 A. Usually it would, but I don't like
15 saying "always" unless I've thought really quite
16 hard about the exceptions.

17 Q. I see. But in your experience, it
18 usually does?

19 A. Yeah.

20 Q. And then the composition of the
21 sequence will also affect the structure that is
22 formed by the process as well; correct?

1 A. Yes. The elements that are -- if you
2 mean composition, the elements that are in it, yes.
3 And -- and the mask designs. Very important.

4 Q. Is there a difference between somebody
5 with a master's degree in the relevant field and two
6 to three years of experience in semiconductor
7 processing with somebody who has a Ph.D. but no
8 experience in industry?

9 A. Yes, I think so.

10 Q. The person with a Ph.D. and no
11 experience would not be considered a person of
12 ordinary skill in the art for the purposes of the
13 '997 patent; correct?

14 A. No, I don't think they would be.

15 Q. Because they don't have the relevant
16 industry experience to understand the integration
17 aspects; is that --

18 A. I think primarily that, yes.

19 Q. So is it fair to say that it doesn't
20 really matter what level of degree the person of
21 ordinary skill in the art obtains, the important
22 aspect is the two to three years of industry

1 experience?

2 MR. MUKERJI: Objection to form.

3 THE WITNESS: I think that's an
4 overstatement. It's important to get a view of
5 process integration somewhere. I'd like to think
6 that my own students get it from me, but that's kind
7 of a small sampling.

8 The -- I lost my train of thought.
9 I'm sorry.

10 Oh. Your question was, is the
11 industry experience what's really important here?

12 I would be reluctant to say that
13 something less than a master's degree, a bachelor's
14 degree, would be satisfactory because I teach
15 undergraduates --

16 BY MR. CHEN:

17 Q. Sure.

18 A. -- junior level and some senior level.
19 And I think the depth of their understanding of the
20 process equipment and chemistry and vacuum
21 technology and all that is rather shy, even if
22 they've been in the semiconductor processing

1 industry for a couple of years.

2 By the same token, the Ph.D. will
3 probably have that in good order and -- but I
4 wouldn't say that a Ph.D. is required for this. So
5 I think master's is the right, let me say, average
6 educational level.

7 Q. Is a person who has a master's degree
8 and two to three years of experience in
9 semiconductor processing have the capability of
10 modifying the process to add new or different steps?

11 A. Yes, usually. These people would be
12 charged with doing design of experiments to optimize
13 the performance of a particular process, to compare
14 that to related processes and the process sequence,
15 and start to actually work on understanding how
16 those things fit together. So they're on their way
17 to becoming process integration engineers.

18 Q. What do you mean "they're on their way
19 to becoming process integration engineers"?

20 A. From most universities, if you get a
21 master's degree, something will be missing.
22 Typically it's process integration perspective. On

1 the other hand, for somebody in electrical
2 engineering, it may not be that so much, but then
3 the familiarity with equipment and materials and the
4 way the process chemistry works is usually a little
5 shortchanged. At least that's my -- that's my
6 observation with all the students. I have -- I'm
7 exposed to students in all of these disciplines.

8 Q. When you said two to three years of
9 experience in the semiconductor processing industry,
10 is there a specific part of semiconductor processing
11 that they need to have experience in?

12 A. Something involving multiple steps to
13 make a device. That's where the process integration
14 expertise is developed.

15 If they were doing, let's say -- I
16 don't know -- a single layer optical coating with a
17 CVD tool --

18 Q. Right.

19 A. -- to put on car windows, that wouldn't
20 teach process integration.

21 Q. So beginning at paragraph 15, you
22 provide a brief overview of the '997 patent?

1 A. Uh-huh.

2 Q. On paragraph 19, you talk about the
3 benefits of forming a thermal oxide layer after the
4 formulation of a gate electrode.

5 You say that one of the benefits is to
6 reduce the defect density?

7 A. Paragraph 19 on page 12 you mean?

8 Q. Yes. It begins on page 11 and
9 continues onto page 12.

10 A. Uh-huh.

11 Q. How does thermal -- how does forming a
12 thermal oxide reduce the defect density?

13 A. Well, as I said -- noted here, there
14 are a number of reasons.

15 So, for example, you've made a layer
16 structure, used lithography, and anisotropic etching
17 to define the gate electrode. Okay. So when that
18 happens, there are residues of the -- of the
19 anisotropic plasma etching process that are left on
20 the surface typically.

21 Thermal oxidation is one way to clean
22 that up because things like carbon will be

1 volatilized and leave the surface because you make
2 CO₂ and maybe CO, things like that. So chemically
3 it's an effective way to do that.

4 It may also yield any internal -- I'm
5 not sure about this, but could conceivably influence
6 the grain structure where the damage of vector ion
7 etching had been at the surface by oxidizing just a
8 little bit into the polysilicon. I'm not sure if
9 that -- if that really happens, but there are a
10 number of things that you might anticipate.

11 Q. Okay. So the primary effect of the
12 thermal oxidation is a cleaning effect?

13 A. Well, it's certainly one of them, yes.

14 Q. Is there any benefit to the actual
15 oxide layer that gets formed?

16 A. Benefit of the oxide layer or to the
17 oxide layer?

18 Q. Of the -- well, when you perform
19 thermal oxidation, don't you form an oxide layer?

20 A. Yes.

21 Q. Is there any specific benefit of the
22 actual oxide layer that is formed?

1 A. You mean in the quality of the oxide
2 layer? Or do you mean in having an oxide layer?

3 Q. In having the oxide layer.

4 A. Yes, there can be. It can serve as a
5 protection layer because it's mask -- essentially
6 masking the sidewall for chemical reaction,
7 electrical transport, various things.

8 Q. But that benefit is not related to the
9 reducing defect density?

10 A. Yes, they all could affect defect
11 density.

12 Q. Okay. How does having the oxide layer
13 reduce defect density?

14 A. Well, I think there are a number of
15 ways that could happen. There's references to
16 literature which shows that.

17 One way, for example, is it might
18 affect the stress distribution at the corner of the
19 gate electrode and the rapid thermal oxidation
20 sidewall. I think that's the one I would -- I would
21 highlight as an example.

22 Q. When you say "defect density," what

1 does that mean?

2 A. Well, okay. So let me -- let me add to
3 that that at that corner -- so -- so the heart of
4 these devices is the gate oxide, and the gate oxide
5 was grown on a very smooth silicon surface, and then
6 a polysilicon layer was applied by CVD on top of it.

7 So the gate oxide, which is the highest
8 quality insulator we know, is fine at that point,
9 until we make the gate electrode. The etching of
10 the gate electrode is likely to damage the gate
11 oxide right at the edge.

12 If one does this sidewall oxidation,
13 one of the benefits could be -- I think is, but I
14 haven't looked at this literature closely -- to heal
15 some of the damage in the gate oxide at the
16 periphery.

17 When you look at defects in these
18 structures, one of the central features is to know,
19 is this something characteristic of right in the
20 middle of the gate electrode in the gate oxide or
21 just following the periphery? And you can discern
22 the difference between those by changing

1 perimeter-to-area ratios. That's how it's
2 standardly done.

3 So I think that would be -- I think
4 that's probably the thing that was targeted in the
5 reference. I think I included a reference here.

6 Oh, I don't understand EX1009 page 3.
7 I don't remember where that is.

8 Q. That's different.

9 A. That's one of the exhibits?

10 Q. Yeah, that's one of the exhibits.

11 A. I don't have the exhibits here.

12 Q. Yeah.

13 MR. CHEN: Exhibit 5.

14 (Document marked, for
15 identification purposes, as Rubloff Exhibit No. 5.)

16 THE WITNESS: Thank you.

17 Oh, yeah. Right.

18 BY MR. CHEN:

19 Q. So I've asked the court reporter to
20 introduce as Exhibit 5 a document titled "Process
21 Induced Degradation of Thin Oxides."

22 You've referred to this as the Wong

1 reference in the IPR and your declaration?

2 A. Yeah. So this work, this is a
3 technology group that I know, and it says here in
4 the abstract:

5 "Polysilicon sidewall oxidation is also
6 necessary to protect the thin oxide from degradation
7 by source/drain ion implantation."

8 But before that it says:

9 "RIE to define polysilicon gate
10 structure degrades the quality of thin oxide;
11 nevertheless these defects can be substantially
12 reduced by subsequent sidewall oxidation of
13 polysilicon."

14 So the way they would measure defect
15 density, I believe, would be to make a bunch of
16 these devices and see what their performance
17 characteristic is and see what the outlier tail of
18 the distribution of performance looks like, and
19 that's the basis on which they make that kind of
20 statement.

21 Q. Does the defect -- do the defects occur
22 to the gate oxide when the gate oxide is etched?

1 A. Yes.

2 Q. All right.

3 A. When the gate? When the reactive-ion
4 etching to define the gate electrode reaches the
5 level of the gate oxide. So right at that
6 periphery, something bad is going to happen.

7 Q. Okay. But the gate oxide itself isn't
8 necessarily etched?

9 A. No. No. Just the edge.

10 Oh, you mean do you etch all the way
11 through the gate?

12 Q. Right.

13 A. It's pretty hard to stop on the gate
14 oxide.

15 Q. Okay.

16 A. I mean, it's possible but, remember,
17 that's the thinnest layer in any of these.

18 And -- and you have to -- you have to
19 -- the etching has to reach the gate oxide.

20 Q. Right.

21 A. Because otherwise you've got still a
22 remaining layer of polysilicon from this device to

1 another one.

2 Q. Okay.

3 A. And they're shorted.

4 Q. Right. So the damage occurs to the
5 gate oxide as long as the etching reaches the gate
6 oxide; right?

7 A. Right, but it has to reach the gate
8 oxide.

9 Q. I'm moving to paragraph 27 and 28 of
10 your declaration.

11 A. Uh-huh.

12 Q. So here you're talking about how the
13 term "forming an oxide layer over the diffusion
14 region" is construed in the context of the '997
15 patent.

16 I want to ask you: What is your
17 understanding of the meaning of the word "over"?

18 A. So in the context of the semiconductor
19 world that we're talking about, over usually means
20 above but not necessarily in contact with.

21 Q. Okay.

22 A. Because if you think about nitride CVD

1 that we're talking about as an etch top layer, it
2 has to go over topography. It would be very
3 inconvenient if our terminology required everything
4 to be in contact.

5 And then just the plain meaning of
6 that. So the airplane is above the earth. So
7 something like that.

8 Q. Does "over" include being in the same
9 or overlapping vertical space?

10 A. Oh, you mean if I -- let me make sure I
11 understand what the question is.

12 A piece here is over -- maybe you can
13 say it.

14 Q. Sure. So --

15 A. I think I know what you're getting at.

16 Q. Maybe it will be easier if we use
17 coordinates.

18 A. Okay.

19 Q. Like X coordinate being along --

20 A. Okay. Good.

21 Q. -- you know, be the typical X direction
22 horizontal direction. A Y coordinate being a

1 vertical direction; right?

2 Does the term "over" mean that you're
3 higher in the Y direction as well as being
4 overlapping to some extent in the X direction?

5 A. Overlapping?

6 Q. I'm not sure if that's the right word.

7 If you have an object, right, and
8 you -- when I say "vertical space," I mean the area
9 above that object moving up at a 90-degree angle
10 from the edges of an object.

11 A. Uh-huh.

12 Q. If another object is not within that
13 vertical space, is that object still over the
14 previous object?

15 MR. MUKERJI: Objection to form.

16 THE WITNESS: I find it difficult
17 to answer that question without a kind of
18 application to look at.

19 BY MR. CHEN:

20 Q. Okay.

21 A. Like if you want to -- would you mean
22 some point of this part of the device structure, is

1 that over some point that's below it?

2 Q. Sure. Why don't we look at Figure 2B,
3 which is --

4 A. Uh-huh.

5 Q. -- in your declaration right above
6 paragraph 27.

7 You see that between the two gate
8 electrodes there's a space; right?

9 A. Uh-huh.

10 Q. Is that -- if I had something that was
11 within that space, would that be over the gate
12 electrode?

13 A. Oh. So something between the two gate
14 electrodes, can that be over a gate electrode? Is
15 that your question?

16 Q. Yeah.

17 A. I wouldn't think so, except that the
18 context of the description technically sometimes
19 changes what the meaning is. So it's a little hard
20 to make a blanket statement about that because often
21 context defines that.

22 So, for example, it may be that in

1 context of a technical document tells you that the
2 point you're asking about cannot be between the gate
3 electrodes, and so if that makes no sense, then I
4 can't say it's over.

5 Q. Okay. Just getting back to the general
6 meanings of the word "over."

7 Is there a difference between the
8 word -- the meaning of the word "over" and the
9 meaning of the word "above" in the context of the
10 '997 patent?

11 A. Let's see. Can you tell me where in
12 the '997 you have in mind? There may be several
13 places, but it would be very helpful to see an
14 example of that.

15 Q. In looking at '997 patent, which is
16 Exhibit 4, and we look at dependent claim 2, which
17 is at column 4 line 5.

18 A. Yeah.

19 Q. And it says:

20 "The method as claimed in claim 1
21 further comprising a step of forming an oxide layer
22 over the diffusion region and on the sidewalls of

1 the gate electrode by thermal oxidation prior to
2 forming the barrier layer."

3 A. (Reviewing document). Yes, I think --
4 I think I address this. Let me see if I can find
5 it. (Reviewing document).

6 So that says "over" but you said
7 "above."

8 Q. Right. I wanted to know --

9 A. Where is "above"?

10 Q. Well, in paragraph 27 of your
11 declaration, you say that you have considered
12 whether a broadest reasonable interpretation of
13 forming an oxide layer over the diffusion region
14 would be broad enough to cover forming an oxide
15 layer above the diffusion region, and then you say
16 "I believe that it would."

17 A. Yes.

18 Q. All right.

19 A. Oh, I'm sorry. I thought I was asking
20 whether -- I thought you had asked whether these two
21 are essentially equivalent in terms of both words
22 being used in the patent. That's not what you

1 meant.

2 Q. No. I want to know --

3 A. Okay.

4 Q. -- what your understanding of the two
5 words are. Whether you think that the meaning of
6 the word "over" is the same as the meaning of the
7 word "above."

8 A. Yes. Yes.

9 Q. So, for example, if there is an object
10 that is -- so let's say I have object A and it is
11 higher in a higher plane than object B (indicating).

12 Object A is above object B; correct?

13 A. Okay.

14 Q. And if object A is in the same vertical
15 space as object B (indicating), object A is over
16 object B; correct?

17 A. Yes.

18 Q. But if object A is not in the same
19 vertical space as object B (indicating), is object A
20 still over object B?

21 A. Can you go through that one more time?

22 Q. Okay.

1 A. It is puzzling to follow.

2 Q. Well, let me ask you this.

3 Do you think there's a difference --
4 outside of the context of the '997 patent, do you
5 think there's a difference in the meaning between
6 the word "over" and "above"?

7 A. Well, my understanding of the -- of the
8 IPR process is that once you choose the most
9 reasonable broad interpretation of that. So I could
10 -- I interpret this to mean that when you say "over
11 the diffusion region," that could mean above,
12 whether or not they're vertically aligned.

13 So if I'm here and I ask about that
14 point (indicating), that's clearly over this, but
15 this is also over it. It's in a higher altitude
16 than this.

17 Q. Okay. So in your definition of "over"
18 in the context of the '997 patent, they do -- the
19 two objects do not have to be in the same vertical
20 space?

21 A. Yes.

22 Q. So it's fair to say that in the context

1 of the '997 patent, you believe that the word "over"
2 and the word "above" have the same meaning; correct?

3 A. (Pause). I think that's right.

4 Q. Okay. Let's move on to paragraph 29.
5 29 through 31 I believe is where you're addressing
6 the construction of the term "spacer" as it's used
7 in the '997 patent. So I just want to make sure I'm
8 clear.

9 Your construction of the term "spacer"
10 as it's used in the '997 patent is "a structure that
11 spaces between two conductive structures"; correct?

12 A. Uh-huh. No, I'm sorry. Wait a minute.

13 You said my construction of spacer is
14 "a structure that spaces between two conductive
15 structures"?

16 Q. Yes.

17 A. Well, what this says is it's broad
18 enough to cover that, but -- but there may be other
19 definition of spacer.

20 Q. So spacer could be -- your construction
21 of spacer is even broader than a structure that
22 spaces between two --

1 A. No. No.

2 Q. No?

3 A. It's broad enough to cover that.

4 It could be broader. I don't know of
5 an example, though.

6 Q. Do you have a specific construction of
7 the term "spacer"?

8 A. Yes.

9 Q. And what is it?

10 A. Well, it's what's in 29 here.

11 Q. What's the difference between your
12 construction being "a structure that spaces between
13 two conductive structures" and simply being broad
14 enough to cover "a structure that spaces between two
15 conductive structures"?

16 A. Yeah, I guess -- I guess there isn't.

17 Q. Okay. So your --

18 A. Yeah. Okay.

19 Q. So just for clarity purposes, so your
20 construction of spacer is "a structure that spaces
21 between --

22 A. Yes.

1 Q. -- two conductive structures"?

2 A. Yeah.

3 Q. Okay. Does that construction cover the
4 function of creating space during ion implantation?

5 A. I don't -- I don't understand what the
6 "spacer" word has to do with ion implantation.

7 Q. In the context of, let's say you're
8 implanting ions into the substrate area --

9 A. Uh-huh.

10 Q. -- next to a gate electrode --

11 A. Uh-huh.

12 Q. -- or close to a gate electrode.

13 Is one of the functions of the spacer
14 to make sure there is space between the implanted
15 area and the gate electrode?

16 A. In the lateral direction.

17 Q. Yes.

18 A. It can be, yes.

19 Q. And is that functionality included
20 within your construction of spacer?

21 A. Well, the implanted region is
22 marginally a conductive structure. So I'm not quite

1 sure how to think about the fact that here the
2 interpretation has to do with spacing between
3 conductive structures. Implanted region will have a
4 reasonable conductivity. So, yes, I think so.

5 Q. What are some of the other functions of
6 a spacer that are included within your construction?

7 A. Well, we went through this before. The
8 construction doesn't say anything about the
9 application. So it is very general.

10 A spacer can be used to prevent
11 chemical reaction, to prevent diffusion, to prevent
12 transport of electron charge. It can be many
13 things, and I don't think it has anything to do with
14 this general interpretation definition of spacer.

15 Q. Just for clarity purposes, you just
16 said that a spacer can be used to prevent chemical
17 reaction, to prevent diffusion, and to prevent
18 transport of electron charge.

19 And I just want to make sure that
20 you're referring to the function of a spacer and not
21 the function of a barrier layer.

22 A. Well, a spacer can be a barrier layer.

1 Q. Okay. All right. Because they are
2 very similar, and I wanted to make sure.

3 A. They can be, yes.

4 Q. Okay. Is your construction of spacer
5 broad enough to cover all of those different
6 functions of a spacer that you just mentioned?

7 A. Well, spacing between two conductive
8 structures, which is what we're talking about here,
9 doesn't tell anything about what function we're
10 describing or measuring; right? So I don't think I
11 can answer that question.

12 Q. Can you give me an example of a
13 function of a spacer that would be covered by your
14 construction of the term "spacer"?

15 A. Well, I think if a spacer spaces
16 between two conductive structures, then if these
17 conductive structures have in principle when
18 intimately connected the ability to transport ions,
19 to transport electrons, to undergo chemical
20 reaction, then bringing them apart by putting
21 something in between them may be able to suppress
22 those phenomena, so serve those functions.

1 Q. Okay. Moving on to paragraph 32, in
2 paragraph 32, you're giving your construction of the
3 term or the phrase "etching an opening through the
4 insulating layer self-aligned and borderless to the
5 diffusion region."

6 What does the term "borderless" mean in
7 the context of that phrase?

8 A. So borderless -- it would be
9 interesting to know where the original term came
10 from. But people speak of borderless context as
11 situations where if I want to make contact to a
12 diffusion region for -- as an example, I don't need
13 to localize that hole within some larger structure
14 that has a differential radius to make sure that I'm
15 not shorting to something on the side.

16 So if I wanted to punch through a
17 contact through an insulator and there's -- there's
18 an electrode on one side or the other, I normally
19 have to drill through but make sure that there's a
20 border, a margin of error. So that when I put
21 conducting material here, next to this is not
22 touching.

1 So I think the term probably came from
2 somebody looking at lithography masks and saying,
3 well, we want to drill onto that contact. We've got
4 another wire or gate electrode here and so when we
5 define the mask for that hole, we have to leave a
6 border, at least on this side and maybe on other
7 sides.

8 So what these patents are talking about
9 is borderless situations where the formation of the
10 spacer during the etch protects against that
11 happening so you can have a much larger lithographic
12 hole to make that contact.

13 Q. All right. So the term is tied into
14 the meaning of self-aligned?

15 A. Well, it may be used someplace else,
16 but in the context of this patent and in the
17 situations that I've known, yes, it has everything
18 to do with self-aligned.

19 MR. CHEN: Exhibit 6.

20 (Document marked, for
21 identification purposes, as Rubloff Exhibit No. 6.)

22 BY MR. CHEN:

1 Q. I've asked the court reporter to mark
2 as Exhibit No. 6 patent number 6,277,720, which were
3 referred to as the Doshi reference.

4 And this is one of the references --
5 Exhibit No. 6 is one of the references that was
6 cited by Samsung in its IPR of the '997 patent;
7 correct?

8 A. Uh-huh.

9 Q. Okay. Did you select this reference
10 for -- as prior art for the '997 patent?

11 A. It is prior art.

12 Q. Okay. Did you find this reference?

13 A. Did I find it initially? No.

14 Q. You were provided with the patent?

15 A. Yes. I was provided a whole bunch of
16 references, and I found and knew of a number myself,
17 and so I looked at all of those and decided which
18 ones to actually use here.

19 Q. Okay. So you -- you decided which ones
20 to actually use --

21 A. Yes.

22 Q. -- in your declaration subsequently, I

1 guess, in the IPR then?

2 A. Yeah.

3 Q. Are you familiar with the term
4 "sidewall filaments" as it's used in the Doshi
5 reference?

6 A. Yes, I've read the Doshi.

7 Q. Okay. Are the sidewall filaments the
8 same thing as spacers?

9 A. Sidewall filaments in the Doshi
10 reference --

11 Q. Right.

12 A. -- serve one and possibly two
13 functions. One is the sidewall filament is made
14 partly by rapid thermal oxidation, which is similar
15 to what is in the '997; but, more importantly, it
16 has a component of conformal deposition anisotropic
17 etching to form another component of that sidewall
18 filament where the thickness of that determines a
19 spacing between the edge of the gate electrode and
20 where the ion implantation is done for the
21 source/drain. So that's an adjustable parameter.

22 So the way to think about that and the

1 way to say it, I think, is that it serves the
2 purposes of a doping spacer as well as potentially
3 an electrical spacer.

4 Q. Okay. And is the function of a doping
5 spacer a function that would be covered by your
6 construction of the term "spacer" in the context of
7 the '997 patent?

8 A. Yes.

9 Q. I want to take some time and walk
10 through the process --

11 A. Uh-huh.

12 Q. -- that's described in the Doshi
13 reference.

14 A. Okay.

15 Q. The process, I believe, begins at
16 column 7 line 28.

17 Before we do that, we've been going for
18 about an hour. Do you guys want to take a break?

19 MR. MUKERJI: Let's take a short
20 break.

21 MR. CHEN: Yeah.

22 (Recess - 2:09 p.m. - 2:29 p.m.)

1 BY MR. CHEN:

2 Q. Okay. We were looking at the Doshi
3 reference before we broke, and we're starting at
4 Exhibit No. 6 column 7 line 28.

5 So the first step in the process
6 described here in Doshi for fabricating an
7 integrated circuit is to define the active regions
8 and the isolation regions; correct?

9 A. Okay.

10 Q. And the next step is to form the gate
11 electrode; correct?

12 A. Okay. That's going down to line 51 or
13 something like that? All in 3a; is that where
14 you're referring?

15 Q. Yeah. Yeah.

16 A. (Reviewing document). Okay.

17 Q. And then the next step it says:

18 "Following definition of gate
19 structures 10, light 'reach-through' implants are
20 performed in a self-aligned manner relative to gate
21 structures to define source/drain extensions."

22 Do you see that at line column 7 lines

1 52 to 55?

2 A. Yeah. Are we still on 3a?

3 Q. In terms of figure?

4 A. Yeah.

5 Q. I think that's right. I think there's
6 a lot of -- a lot of steps that are subsumed within
7 3a, but I'm looking at the text.

8 Then following -- well, first of all,
9 what are the light reach-through implants?

10 A. Those are marked in 3a as 6' and 7'.

11 Q. What is their function?

12 A. Their function is to change the dopant
13 profile of the source/drain regions to improve
14 device performance.

15 Q. Are they part of the source/drain
16 region?

17 A. Yeah. They're electrically connected
18 to the source/drain region, but the point there is
19 that people these days -- these days and in this
20 time frame as well do substantial modeling on the
21 performance of hard electrons and saturation
22 velocities and all of that. And the detailed

1 three-dimensional distribution of dopant profiles,
2 and not just profiles but concentrations, makes a
3 substantial difference in the performance of the
4 transistor devices.

5 So this is called source/drain
6 engineering, trying to make it look a certain way.
7 And I remember when I started, you know, in the '80s
8 getting involved with some of the silicon technology
9 people before I joined the department, there were
10 people talking about source/drain extension and the
11 source/drain connected to it and so on.

12 Q. So the source/drain extension is
13 considered a part of the source/drain region;
14 correct?

15 A. Yeah, it's part of the profile.

16 Q. Okay. And the dopant profile.

17 Well, what is a dopant profile?

18 A. You mean how did I define that?

19 Q. Yeah. How did you just use the term
20 "dopant profile"?

21 A. Well, if you look in Figure 3a at the P
22 device on the left.

1 Q. Right.

2 A. You see a profile that says "p+" and it
3 has this little extension under the gate. It could
4 be called source/drain extension sometimes.

5 And so when I say "dopant profile,"
6 what I really mean is concentration of dopants as a
7 function of X, Y, and Z. Because I know it's drawn
8 as if it's all p+, but it's not and, in fact, it
9 can't be a boundary quite that sharp anyway.
10 There's always a spread in how the P concentration
11 goes down and the N concentration crosses over.

12 Q. And you said that the dopant profile
13 for a device makes a substantial difference in the
14 performance of that transistor device?

15 A. Yeah, it can.

16 Q. And what affects the dopant profile of
17 the device?

18 A. Number one, how you make it. In this
19 case, two implantation steps. Number two, the heat
20 treatment that it sees in subsequent steps. And
21 number three, how much dose you put into those
22 places that are unmasked during ion implant.

1 Q. When you say "dose," you mean how much
2 impurities are implanted --

3 A. Right.

4 Q. -- into the region?

5 A. Right.

6 Q. So changing the dosage would affect the
7 dopant profile of the device?

8 A. Yeah. If you turn down the ion flux by
9 a factor of 2 will probably change the performance.
10 It may have the same shape. So that -- that C
11 concentration of X, Y, Z --

12 Q. Right.

13 A. -- may become C over 2 but have the
14 same shape.

15 Q. Right. The shape could be the same,
16 but the concentration of impurities in that region
17 would differ?

18 A. Yeah.

19 Q. Okay. And other things that could
20 affect the dopant profile are, I think you said, the
21 heat treatment as well; right?

22 A. Right.

1 Q. And the heat, how does the heat
2 treatment affect the dopant profile?

3 A. Dopants diffuse in silicon and so the
4 longer you heat the sample, the wafer, and the
5 higher the temperature, the more diffusion you get.
6 So what may have started out as a shallow doping
7 profile, if you wait long enough, that -- that
8 limited -- let me think of a fix for it -- will
9 diffuse into something much broader and lower in
10 concentration. Limited source diffusion.

11 Q. Okay. Does implantation energy also
12 affect the doping profile?

13 A. Yes.

14 Q. Because that implantation energy will
15 affect where the impurities are deposited in the
16 substrate; right?

17 A. Right. How deep they penetrate.

18 Q. Okay. Looking at column 7 line 57 --
19 we briefly talked about this before -- it says:

20 "According to the preferred embodiment
21 of the invention, sidewall filaments are formed."

22 You see where it says that?

1 A. Uh-huh. Uh-huh.

2 Q. And then it says:

3 "Sidewall filaments 11 are formed by
4 first oxidizing the sides of polysilicon layer 22."

5 And then it goes on to talk about a
6 subsequent step where silicon nitride is deposited
7 and etched.

8 A. Uh-huh.

9 Q. So my question is: Are the oxidized
10 sides of the polysilicon layer part of the sidewall
11 filaments?

12 A. Yes.

13 Q. Why would you say that they are part of
14 the sidewall?

15 A. Well, the sidewall -- what is described
16 here as the sidewall filament is composed of
17 oxidized polysilicon, which is silicon dioxide and
18 nitride. So they both are insulators. So it would
19 be hard to differentiate them except chemically, but
20 functionally they're both insulators.

21 So I think, though it's not described
22 in great detail here, I think what's intended here

1 is that 11 is a sidewall filament that's a composite
2 of both components.

3 Q. Okay. Looking at -- I think we're
4 still on Figure 3a.

5 The sidewall filament is a structure
6 labeled 11 in the figure; correct?

7 A. Yes.

8 Q. Okay. And the polysilicon is the
9 structure that's labeled 22; correct? The
10 polysilicon portion of the gate?

11 A. Yes.

12 Q. And the oxidized portion of the
13 polysilicon is just on the sidewalls of the
14 structure that's labeled 22; correct?

15 A. Hold on. 24 is above 22.

16 Q. Right.

17 A. It's tungsten silicide.

18 Q. Right.

19 A. So the thermal oxidation of the
20 sidewall of the polysilicon --

21 Q. Right.

22 A. -- will cause some oxidation of the

1 silicide as well.

2 Q. Oh, okay.

3 A. So, I mean, it's not really drawn here
4 that way. This wasn't the point that was elucidated
5 in detail.

6 Q. So the oxidized layer that was formed
7 would cover 22, the sidewalls of 22, some of 24, but
8 would not extend up to the silicon nitride layer 26;
9 right?

10 A. Yeah. I don't think the silicon
11 nitride will be oxidized.

12 Q. Okay.

13 A. And I don't know what the relative
14 thickness of the rapid thermal oxidized on the
15 silicide and on versus the polysilicon will be.

16 Q. Okay.

17 A. Probably more on the polysilicon, but
18 I'm not sure.

19 Q. And you said that during the oxidation
20 process, an oxide layer would also be formed over
21 the diffusion regions; is that correct?

22 A. Yes.

1 Q. And this is true if the diffusion
2 region is uncovered silicon; correct?

3 A. Well, if it's -- it's true if it's
4 uncovered silicon, or if it's covered by thin oxide.
5 Because thermal oxide has linear growth rate in the
6 thin regime. So if you already have a thin layer of
7 oxide and you go to oxidizing conditions, you make
8 it thicker.

9 Q. But what you're doing there is you're
10 thickening the existing oxide?

11 A. Yeah, which you're oxidizing it. It's
12 the same oxidation chemistry as whatever formed it
13 originally.

14 Q. Doshi only says oxidizing the sides of
15 the polysilicon layer in column 7 line 59; correct?

16 A. Uh-huh.

17 Q. So Doshi doesn't specifically disclose
18 thermal oxidation; correct?

19 MR. MUKERJI: Objection to form.

20 THE WITNESS: One of ordinary
21 skill would interpret oxidizing any kind of silicon
22 as thermal oxidation.

1 BY MR. CHEN:

2 Q. Is it --

3 A. Otherwise it would say CVD using such
4 and such precursor.

5 Q. So is thermal oxidation the only method
6 amenable to oxidize the polysilicon layer?

7 A. No.

8 I'm sorry. To oxidize polysilicon.

9 No, it's not. You could do anodic
10 oxidation, which is a wet chemical electric chemical
11 technique. I mean, I don't think anybody would do
12 it here, but it could be done.

13 Q. Well, how do you know that Doshi, when
14 it says oxidizing the sides of the polysilicon
15 layer, is referring to thermal oxidation as opposed
16 to the other form of oxidation using the wet
17 chemical electrodes?

18 A. If it were wet chemical, it would have
19 said anodization because it's a standard way of
20 describing it. Poured silicon is made this way, for
21 example. And in this technology domain, silicon,
22 oxidizing means you use O₂, or conceivably O₂ with

1 some water, or conceivably N₂O, but it's a gas-phase
2 process. Oxidizing means that what used to be
3 silicon becomes a new compound.

4 Q. Okay.

5 A. As opposed to CVD deposition of a
6 silicon oxide, where both the silicon and the oxygen
7 came from the vapor phase.

8 Q. So when you do CVD deposition of a
9 silicon oxide, what you're doing is you are
10 depositing new material onto, let's say, the
11 substrate or wafer; correct?

12 A. That's right. All the source material
13 comes from the gas-phase in CVD.

14 Q. Right. And when you're doing thermal
15 oxidation, what you're doing is you're converting
16 the existing material to a different compound?

17 A. Right.

18 Q. Right?

19 A. From silicon to SiO₂.

20 Q. So if I have a layer of silicon and I
21 perform thermal oxidation on that layer, part of
22 that silicon gets converted to silicon dioxide;

1 correct?

2 A. Uh-huh.

3 Q. Is the overall thickness of the layer,
4 which has both the original silicon and the
5 converted silicon dioxide, the same thickness as the
6 original layer of silicon prior to the thermal
7 oxidation process?

8 A. No, it's different.

9 Q. How is it different?

10 A. Because the density of SiO₂ is
11 different from that of silicon, and so it turns out
12 that when you oxidize, the thickness of the silicon
13 which you started with gets smaller because you've
14 consumed some. But if you look at the thickness
15 from the bottom of the silicon to the top of the
16 oxide, that grows.

17 Q. Okay.

18 A. And the ratio of how much is above and
19 below the initial surface is something like 40/60 or
20 60/40. I don't know. I don't remember.

21 Q. The point is, it gets thicker?

22 A. It gets thicker.

1 Q. Okay. When you perform thermal
2 oxidation -- oh, actually, never mind.

3 After the step of forming the sidewall
4 filaments, then you form the source/drain implants.
5 That's at column 7 beginning at line 66.

6 A. Uh-huh.

7 Q. Okay. And it's this step here where
8 you discussed before that the sidewall filaments are
9 used to create space between the implantation and
10 the gate electrode; correct?

11 A. Right.

12 Q. The next step -- this is at the
13 beginning of column 8 line 8 -- it talks about the
14 formation of silicon nitride layer 30.

15 You see that?

16 A. Uh-huh.

17 Q. What is the function of the silicon
18 nitride layer?

19 A. The silicon nitride layer is nominally
20 an etch barrier for etching through the layer that
21 will be on top of it, the ILD layer, interlayer
22 dielectric, but it will also serve as the spacer at

1 the end of the process.

2 Q. Where does Doshi say that it will serve
3 as a spacer at the end of the process?

4 A. Well -- (reviewing document). I'm not
5 sure if I can find where it is explicitly stated,
6 but the structure is identical to the spacer
7 structure in the '997 patent and so it serves the
8 same function.

9 I think he implies it. This would be
10 at column 9 line 65 through 70.

11 "Figure 3g illustrates the construction
12 of integrated circuit 20 after the completion of
13 both etch steps, and the stripping of photoresist
14 layer."

15 So I think he implies it there, but I
16 don't know if I -- it's a long specification. So I
17 don't know if I can --

18 Q. How does he imply it there? That
19 paragraph that you just referenced doesn't even
20 mention the silicon nitride layer 30.

21 A. Well, but he's prescribed that after
22 the second etch, the silicon nitride is left on the

1 sidewall, and it's shown in the drawings. So I
2 think it's very clear that there is a spacer there.

3 Q. Where does Doshi say that the silicon
4 nitride layer is left on the sidewalls?

5 A. (Reviewing document). So Figure 3g
6 shows the sidewall filament 11 and it shows silicon
7 nitride 30 that's left on the sidewall next to the
8 hole where the self-aligned contact goes in 3h.

9 Q. Other than Figure 3g, is there any
10 place in the text of Doshi that says that the
11 silicon nitride is left on the sidewall after the
12 etch?

13 A. Well, I can't -- I don't remember
14 exactly what he says about that, but it is very
15 clear here, and I even identify that there was a
16 minor error in the way the structure was drawn. But
17 we know that that's what would happen, and the '997
18 builds on that afterwards and so I think it's --
19 it's very clear.

20 Q. Can you point to any place in the text
21 of Doshi that says that the silicon nitride is left
22 on the sidewalls after the etch?

1 A. Let me look some more. I don't
2 remember. It's a long specification. (Reviewing
3 document).

4 So I think it's implied in the
5 paragraph in column 10 line 4.

6 "It has been observed, in connection
7 with the present invention, that the two-step etch
8 of BPSG layer 14 and nitride layer 30 is
9 particularly beneficial, as damage to the corners of
10 gate structure 10 and sidewall filaments is
11 substantially minimized."

12 So if the corners -- if in the process
13 of the second part of the etch through the nitride,
14 which forms the sidewall spacer, the damage at the
15 edge is minimal, then we know that there remains
16 silicon nitride on the sidewall of the gate
17 electrode.

18 And it goes on to say:

19 "In particular, sidewall corner
20 locations NC illustrated in Figure 3g have been
21 observed to be particularly susceptible to damage
22 from conventional nitride etches. However, the

1 brief nitride etch used to clear nitride layer 30
2 from within plug contact locations" -- at the bottom
3 because that's where the contact is going to be --
4 "PC has been observed to be highly anisotropic."

5 So he's reconfirming that that etch is
6 highly anisotropic, and it doesn't etch that much
7 from the corner. It should have -- my point was, it
8 should have shown a little bit of change, but it's
9 very little. And so that means that the sidewall
10 nitride 30 is going to be there and that will serve
11 as a spacer.

12 He doesn't say, this is a spacer. He
13 doesn't say that. At least not here, and I haven't
14 found where he says that, but it is very clear that
15 it's a spacer. And it's the same thing that the
16 '997 purports to use as a spacer.

17 Q. I understand that you have a, you know,
18 interpretation of the Doshi reference, but that
19 paragraph that you just read doesn't specifically
20 say that the nitride 30 layer is left on the
21 sidewalls after the etch; correct?

22 A. No, I think it says it. It doesn't say

1 it explicitly as you said it, but it makes it very
2 clear to one of ordinary skill that if I haven't
3 done much damage to the 30 at the top there and I
4 use a highly anisotropic etch, I will have remaining
5 a nitride sidewall spacer.

6 Q. Where does it say you will have
7 remaining a nitride sidewall spacer?

8 A. It doesn't say it that way. It says
9 it's a highly anisotropic etch, and it doesn't
10 damage or remove much at the top at that corner
11 above the sidewall filament. Therefore, one of
12 ordinary skill would certainly conclude that that
13 sidewall nitride structure remains --

14 Q. Well --

15 A. -- as a spacer.

16 Q. -- it doesn't say that it doesn't
17 remove much of the nitride. It says it doesn't
18 damage the corners of the gate structure as much;
19 correct?

20 A. Well, the gate structure is underneath
21 the photoresist.

22 Q. Right. But the gate structure is still

1 damaged. It's just not as much as before; correct?

2 A. Yeah. I think some of that nitride
3 will be removed. That's what I tried to correct in
4 this figure on page 37.

5 Q. So all that section says is that having
6 the nitride there reduces the damage to the corner
7 of the gate structure; correct?

8 A. Yes, but I describes the etching
9 process in a way that's essentially identical to
10 what the '997 purports to claim, and it forms what
11 one of ordinary skill would recognize as a sidewall
12 spacer made of nitride.

13 Q. In order to even damage the gate
14 structure, you have to etch through the nitride
15 layer protecting that gate structure; correct?

16 A. I'm not sure about that. (Reviewing
17 document).

18 When you use reactive-ion etching to do
19 highly anisotropic etching, you have on the wafer a
20 large bias, several hundreds of volts. So the
21 reactive-ion species that do the etching are very
22 energetic, and that's why reactive-ion etching is

1 always a concern for damage to materials. It
2 doesn't matter where. It happens all the time.

3 So it's reported that that region NC is
4 particularly susceptible to damage from conventional
5 nitride etches. That may be a mechanism where the
6 energetic ions impact the top corner of the nitride
7 and cause stress buildup, or something like that,
8 that influences the properties of the gate
9 electrode. It may be. I don't know. I mean, I
10 didn't study that.

11 But I still come back to the fact that
12 while I haven't yet found a place where Doshi makes
13 it clear and simple that this nitride remains and
14 forms a sidewall spacer, it's absolutely clear to --
15 for one of ordinary skill that it does remain
16 because it's an anisotropic etch. And it hasn't
17 modified much of that sidewall nitride, except
18 perhaps at the top.

19 Q. And you're pointing to the Figure 3g;
20 is that correct?

21 A. Yes, that's right.

22 Q. Are you relying on Figure 3g for your

1 understanding that the nitride layer remains on the
2 sidewall of the gate electrode?

3 A. No. That confirms it to some extent,
4 but I'm relying on my understanding and one that
5 would be easy for one of ordinary skill to know that
6 when you do the sequence of steps here, you will
7 have a sidewall spacer.

8 Q. Even though Doshi doesn't actually say
9 that you will have a sidewall spacer; correct?

10 A. But, remember, Doshi is a long patent
11 with many embodiments and stack capacitors and all
12 kinds of things in it, and he's talking about --
13 some -- sometimes the recognition of earlier
14 invention in the prior art, as I understand it, can
15 be found in things that are teaching the thing
16 you're wondering about but not really making that
17 the focus of what's there.

18 So I think Doshi covers a lot of things
19 here.

20 Q. But Doshi doesn't specifically say that
21 you will form sidewall spacers from nitride layer
22 30; correct?

1 MR. MUKERJI: Objection to form.

2 THE WITNESS: Well, I haven't
3 reviewed the whole thing to look for where in one of
4 the other applications he may have addressed that,
5 but the process is very clear. There will be a
6 sidewall spacer and everybody knows it.

7 BY MR. CHEN:

8 Q. Sitting here today, you cannot point to
9 any specific portion in Doshi that says that
10 sidewall spacers are formed from nitride layer 30;
11 correct?

12 MR. MUKERJI: Objection to form.

13 THE WITNESS: I don't know the
14 answer to that. I have to read the whole patent in
15 detail.

16 BY MR. CHEN:

17 Q. You didn't read the whole patent in
18 detail before?

19 A. Of course I did. I can't remember
20 everything that's here.

21 Q. Okay. But you didn't cite to any
22 portion of Doshi in your declaration?

1 A. No, I didn't.

2 Q. Right?

3 A. No, that's right.

4 Q. Do you think that Doshi might have said
5 it somewhere, but you left it out of your
6 declaration?

7 A. I have no idea. I did this six months
8 ago, whatever it was. It's a long patent, and to me
9 it was very clear.

10 In fact, the first time I encountered
11 the teaching of the BPSG on top of the nitride
12 serving as an etch-stop next to the gate electrode,
13 the first time I encountered that was '997, which
14 taught me after Doshi, prior art, that you make a
15 sidewall spacer there. And I knew it before, and I
16 think one of ordinary skill would know that.

17 Q. And so my question is and it's pretty
18 simple question:

19 Sitting here today, can you point to
20 any specific portion in Doshi that says that
21 sidewall spacers are formed from nitride layer 30?

22 MR. MUKERJI: Objection to form.

1 THE WITNESS: I cannot yet do
2 that, but I have not reread the patent to be able to
3 answer your very explicit question.

4 BY MR. CHEN:

5 Q. Okay.

6 A. But I think this is not the issue,
7 whether he says it or not. It forms the same
8 structure as the '997 shows and it came before.

9 Q. In order for nitride layer 30 to act as
10 a sidewall spacer, does it need to have a certain
11 thickness?

12 A. Larger than zero. Yes.

13 Q. Just larger than zero?

14 A. No. I don't know. I don't know what
15 number to put on it. Yes, it has to have a finite
16 thickness.

17 Q. Should it have a relatively thick --
18 should it be a relatively thick layer to act as a
19 sidewall spacer?

20 A. No, I don't think it needs to be very
21 thick. We made essentially CVD, actually ALD,
22 insulating layers 6 nanometers thick. They are

1 excellent insulators. So it doesn't have to be very
2 thick.

3 Q. What does it depend on? How thick --
4 what determines how thick that layer needs to be in
5 order to act as a sidewall spacer?

6 A. It depends on the quality of the
7 material, and the thickness should be greater than a
8 tunneling distance, but that's -- that's of order
9 one nanometer or less. So that's kind of an
10 irrelevant number. That's very thin. Tunneling
11 distances I mean.

12 MR. MUKERJI: Can we go off the
13 record for just one second?

14 (Off the stenographic record)

15 (Recess - 3:16 p.m. - 3:38 p.m.)

16 BY MR. CHEN:

17 Q. All right. Dr. Rubloff, before we went
18 off the record, we were talking about --

19 A. Uh-huh.

20 Q. -- the nitride layer 30 --

21 A. Yes.

22 Q. -- as described in the Doshi reference.

1 I noticed that you were, you know,
2 taking the time during the break to review the
3 reference.

4 A. Uh-huh.

5 Q. Did you find -- in your time reviewing
6 the reference, did you find any location where Doshi
7 specifically says that nitride layer 30 is --
8 remains on the sidewalls of the gate electrode and
9 acts as a spacer?

10 A. I haven't found anything explicit along
11 the lines of the words that you just used. But the
12 description, for example, in column 3 on 60, which
13 is the description of how the sidewall filaments are
14 made, talks to "silicon nitride sidewall filaments
15 are conventionally formed by CVD of silicon nitride
16 overall, followed by an anisotropic nitride etch to
17 remove the nitride from the flat active regions,
18 leaving sidewall filaments behind."

19 The structure of the sidewall filament
20 is similar to the structure of the nitride layer 30
21 that is explicitly depicted in Figure 3g of Doshi
22 and corresponds, I think, directly to what the '997

1 purports.

2 So while I have not found the explicit
3 kind of wording that you are looking for, I think
4 one of ordinary skill would recognize Doshi is doing
5 the same thing that the '997 is doing.

6 Q. The sidewall filaments that are
7 described in Doshi are actually explicitly described
8 as having the spacer function; correct?

9 A. Having the doping spacer function;
10 right.

11 Q. And in column 8 where Doshi is
12 describing the nitride layer 30, it describes
13 certain functions for that layer; correct?

14 A. Column 8 where?

15 Q. Column 8 beginning at line 8.

16 A. I'm sorry. Line?

17 Q. 8.

18 A. (Reviewing document). Well, that's a
19 function -- the description you're referring to is
20 the dopant barrier that 30 silicon nitride serves to
21 prevent boron and phosphorous from the -- overlying
22 BPSG from diffusing into the silicon.

1 So what -- what it basically says is
2 the nitride serves as a diffusion barrier for that
3 structure, but that's not addressing its sidewall
4 function.

5 Q. Right.

6 A. It's addressing its chemical function.

7 Q. Right. It's specifically --

8 A. One of its functions.

9 Q. -- discloses a function for that layer
10 and that function that is disclosed is acid
11 diffusion barrier?

12 A. That's -- yes, but a layer like that
13 can have multiple functions. Silicon nitride is a
14 pretty good insulator, electrical insulator.

15 Q. All right. Following the formation of
16 silicon nitride 30 -- layer 30 is the formation of
17 the interlayer dielectric, and that's referred to at
18 column 8 line 23; correct?

19 Oh, sorry. Actually --

20 A. Let's see.

21 Q. No, that's correct.

22 A. Yeah.

1 Q. So it begins at column 8 line 23;
2 correct?

3 A. Uh-huh.

4 Q. Right. And that interlayer insulator
5 is made of BPSG; correct?

6 A. Yes.

7 Q. And BPSG is a silicon oxide layer;
8 correct?

9 A. It's a silicon-based oxide layer, but
10 it's doped with boron and phosphorous.

11 Q. Okay.

12 A. That changes its mechanical properties
13 significantly.

14 Q. And subsequent to the deposition of the
15 BPSG layer, that layer is then planarized; correct?

16 A. Yes.

17 Q. All right. And then Doshi -- moving
18 along, Doshi starts to talk about the formation of
19 the contact openings.

20 A. I'm sorry. Can I go back to the BPSG
21 question?

22 Q. Sure.

1 A. So this describes that after the layer
2 30 is put down over everything conformally --

3 Q. Right.

4 A. -- as the next top layer, the BPSG is
5 put down and then it's planarized by high
6 temperature annealing step.

7 What will happen during that annealing
8 step is important for the understanding of the
9 sidewall filaments function. Because it just
10 described that nitride is a good barrier to boron
11 and phosphorus diffusion -- diffusion, but referring
12 only to the consequences for the crystalline silicon
13 n+ region, the substrate; right?

14 So it's basically saying, what you just
15 read, says that silicon nitride layer 30 when it's
16 still on top of the n+ region will prevent boron and
17 phosphorous diffusion into the silicon.

18 That -- that has a consequence that on
19 the sidewall, the remaining nitride 30 will serve as
20 a boron and phosphorus diffusion barrier. So that
21 boron and phosphorous from the now present BPSG next
22 to the nitride layer 30 can't get through 30 to get

1 to the polysilicon or tungsten silicide because the
2 component of the sidewall filament, the thermal
3 oxide, is not a good barrier.

4 So what I'm saying is the sidewall
5 nitride structure 30 will play a role during the
6 planarization step, which is annealing the BPSG, in
7 preventing dopants from entering the polysilicon.
8 And for that matter, it could be the gate oxide at
9 that point.

10 Q. Okay. And what is the significance of
11 that --

12 A. Well --

13 Q. -- point you just made?

14 A. -- the significance is that if the --
15 ah -- is that at least during that step, there is a
16 function for that sidewall spacer of nitride. It's
17 not the electrical barrier at that point because
18 that hasn't been encountered yet until the structure
19 is done.

20 Q. So you're saying then at the point of
21 the BPSG formation, the nitride layer 30 covering
22 the sidewalls of the gate electrode structure is

1 performing spacer function?

2 A. Yeah, and diffusion barrier function.

3 It's not highlighted here because it's probably not
4 as big a problem, but I noticed that a lot of
5 attention is given to the diffusion barrier function
6 of the nitride material with regard to the source
7 region.

8 Q. Okay.

9 A. It's just a comment.

10 Q. Sure. So then, for example, looking at
11 Figure 3f, which -- what figure are you looking at
12 in your declaration?

13 A. Too many. I have Figure 3g in my
14 declaration.

15 Q. Okay. Well, let's look at Figure 3f.

16 A. Okay.

17 Q. Or no. Sorry.

18 A. Yes.

19 Q. Figure 3 -- let's look at Figure 3d.
20 All right? This is the figure before the contact
21 openings are being etched, but you have the BPSG
22 layer 14, I believe it is.

1 A. Uh-huh.

2 Q. Right. So looking at Figure 3d, a
3 person of ordinary skill in the art would look at a
4 portion of nitride layer 30 covering the sidewalls
5 of the gate electrode and say that's a spacer right
6 there?

7 A. Well, I would say it's a diffusion
8 barrier during BPSG reflow, which is an annealing
9 step.

10 Q. So it is not a spacer?

11 A. Well, a diffusion barrier is a kind of
12 spacer.

13 Q. Okay. So it is a spacer?

14 A. Yes.

15 Q. Okay.

16 A. But that's not the spacer that's at
17 issue here. I realize that.

18 Q. I don't follow you.

19 A. No. I think your question was, at this
20 stage after both etches of BPSG and nitride is done,
21 how do we know there's still a nitride sidewall
22 spacer? And that's a different -- that's a

1 different question.

2 Q. That's a different.

3 A. I may have raised an irrelevant
4 question. It was just an observation because
5 there's been so much attention in what you read to
6 the diffusion barrier properties of the nitride.

7 Q. Right.

8 A. Sorry if I got us off-track.

9 Q. No, no. I just want to understand. I
10 mean, maybe it's an important point.

11 Because you are saying that during BPSG
12 formation, that portion of the nitride layer that's
13 on the sidewall is acting as a diffusion barrier in
14 the --

15 A. Lateral.

16 Q. -- lateral direction?

17 A. Yes.

18 Q. Thank you.

19 And I think your point was, is that at
20 that stage, that portion of the nitride layer, the
21 portion that's on the sidewall of the gate, is
22 functioning as a spacer; correct?

1 A. A diffusion barrier spacer.

2 Q. And that diffusion barrier spacer is
3 within the definition of spacer that you provided in
4 the context of the '997?

5 A. Yes.

6 Q. Now, one reason you said that that is
7 needed to provide that function is because you said
8 that the thermal oxide of the sidewall filament is
9 not a good diffusion barrier; correct?

10 A. That's correct.

11 Q. Okay. But the sidewall filament is not
12 just comprised of thermal oxide; correct?

13 A. That's correct.

14 Q. Okay. It actually has a layer of
15 silicon nitride; correct?

16 A. Right, which was formed exactly the way
17 that the sidewall fill -- the sidewall spacer 30 is
18 formed during the two-step etch.

19 Q. Okay. And silicon nitride is a good
20 diffusion barrier?

21 A. It is a good diffusion barrier.

22 Q. Okay. So in a sense, the sidewall

1 filament 11 will protect a gate from any boron or
2 phosphorus diffusion?

3 A. It can, yes.

4 Q. And you don't really need the nitride
5 layer 30 there to act as a diffusion barrier;
6 correct?

7 A. I think that's correct. Well, it helps
8 but --

9 Q. Okay. Okay. So we've talked about the
10 formation of the BPSG layer, and I'd like to talk a
11 little bit now about the formation of the contact
12 openings and that begins at column 9 line 26.

13 A. (Reviewing document).

14 Q. Okay. I guess the first step of
15 forming the contact opening is to form the patterned
16 resist; correct?

17 A. Yes.

18 Q. All right. And the next step is to
19 then etch through the BPSG layer stopping on the
20 nitride layer; correct?

21 A. Yes.

22 Q. All right. And this is where the

1 nitride layer is behaving as an etch-stop?

2 A. Yes.

3 Q. And then what follows after the BPSG
4 etch step is a nitride etch step; correct?

5 A. Uh-huh.

6 Q. And the purpose of that nitride etch
7 step is to etch through the nitride layer; correct?

8 A. It's to etch through the nitride layer
9 that's covering this source/drain region, the
10 diffusion region, and at that point it forms the
11 sidewall spacer.

12 Q. Looking at your declaration at
13 paragraph A-12, you describe the second etch as "an
14 anisotropic etching of the barrier layer underneath
15 the opening."

16 You see that?

17 A. Uh-huh.

18 Q. Now, the part that you -- you quoted
19 from the patent says:

20 "Contact openings (PC, BLC, CT) are
21 etched through the BPSG layer (14) and the silicon
22 nitride layer (30) using a two-step etch process."

1 What does the PC stand for?

2 A. Yeah. I don't remember which figure
3 that is.

4 Q. I mean, is PC, BLC, and CT just
5 different contact openings in different regions?

6 A. I'll have to think about that.

7 Q. Actually, maybe this will help you.
8 If you look at column 10?

9 A. Yeah.

10 Q. Line 3, for example. It says "within
11 plug contact openings PC."

12 Is PC just plug contact?

13 A. Yeah, that's -- (reviewing document).
14 Okay. In Figure 3g, PC is the plug -- excuse me --
15 plug contact. Because the PC is in the place where
16 the opening through BPSG and nitride is.

17 And NC -- okay. That's different.
18 That's the corner.

19 BLC is in Figure 3i.

20 Q. Right.

21 A. And I think 3i refers to a different
22 structure, a different device. Plug oxide layer.

1 Q. Well, if you go to --

2 A. It's part of a DRAM circuit it appears.
3 Bit line contact location is BLC.

4 Q. Right. So if you look at column 10
5 line 40, for example, it says:

6 "As in the formation of plug contact
7 locations PC, bit line contact locations BLC."

8 So I assume that PC refers to plug
9 contact and BLC refers to bit line contact?

10 A. Uh-huh.

11 Q. Is that right?

12 A. I think so.

13 Q. Okay. What is a CT?

14 A. (Reviewing document).

15 Q. Maybe that's not.

16 A. (Reviewing document).

17 Q. If you don't know, it's okay. We can
18 move on.

19 A. I don't know. I think that those refer
20 to other applications than the ones we've
21 concentrated on --

22 Q. Okay.

1 A. -- and are relevant. So I think it's
2 not a big deal.

3 Q. Okay. All right. Getting back to the
4 nitride etch.

5 So the results of the nitride etch are
6 shown in Figure 3g; correct?

7 Or the results of the nitride etch for
8 the plug contact openings are shown in Figure 3g;
9 correct?

10 A. Yes.

11 Q. And then you mention that you found an
12 error in Figure 3g; correct?

13 A. Yes. I think it was a little
14 misleading. I would have expected to see -- what
15 page do I have this on? Yeah, on page 37.

16 I would have expected to see some of
17 the top nitride etched away there.

18 Q. And that's not depicted in Figure 3g;
19 right?

20 A. No. No. Figure 3g on page 37 of my
21 declaration shows a little region in a rectangle
22 where that top part of nitride 30, I think, should

1 have been shown removed, and that's an annotation to
2 a blowup of the right part of Figure 3g near that
3 plug contact.

4 Q. And the reason why that portion of the
5 nitride layer 30 would have been removed is because
6 it is within the exposed portion of the contact
7 opening mask?

8 A. That's right. And so the thickness of
9 that nitride as it meets the resist layer would be
10 in conformal CVD the same as the thickness of the
11 nitride that would be on top of the n+ region. So
12 when you clear the n+ region, you'll lose some of
13 that top part, but you'll still leave the sidewall
14 nitride 30 because it's the standard way of making
15 sidewall spacers.

16 Q. Other than the error that you pointed
17 out in your declaration, are there other errors in
18 Figure 3g of Doshi?

19 A. None that I know of, or I would have
20 declared them.

21 Q. Previously you had mentioned that the
22 diffusion region is covered by a thermal oxide

1 layer; correct?

2 A. Yeah, from the RTO.

3 Q. Right. Is that thermal oxide layer
4 depicted here in Figure 3g?

5 A. No, because the etch that removes the
6 nitride would have to remove any thermal oxide there
7 in order to allow good contact to the n+ region.

8 Q. But isn't the etch to remove the
9 nitride selective to nitride over oxide?

10 A. Right, but selectivity is never
11 infinite. It's a certain number and nitride is
12 significantly thicker than a little bit of thermal
13 oxide --

14 Q. Okay.

15 A. -- that might have been present there.

16 Q. So it's your opinion that the etch that
17 removes the nitride would also etch through any
18 thermal oxide that is --

19 A. Yeah, and it wouldn't have to etch
20 through all of it. Because when you make a contact
21 like that, if there are a few patches of very thin
22 oxide remaining, it doesn't change the

1 characteristics very much. You would like not to
2 have that.

3 So the way -- the way to think about
4 that is, if I make a contact here and there's some
5 oxide here, but there are plenty of places where
6 there is not oxide, that's really all I need to get
7 the contact resistance lowered enough to make
8 effectively contact.

9 I mean, I don't think every oxygen if
10 there were thermal -- a little bit of thermal oxide
11 here, I don't think it means that every single
12 oxygen atom has to be gone after the etch for it to
13 be a good contact to the material that fills this
14 region.

15 Q. Wouldn't you want to clear off any
16 oxide over the contact to make a good contact?

17 A. Yeah, of course. You'd like to clear
18 off whatever you can and that means most of it, but
19 it doesn't have to be every atom.

20 Q. Looking at Figure 3f of Doshi, this is
21 before the nitride etch step.

22 The thermal oxide isn't shown in this

1 figure here; correct?

2 A. The thermal -- which thermal oxide?

3 Q. The thermal oxide over the diffusion
4 region.

5 A. No.

6 Q. Okay. Is that another error in Doshi
7 figures?

8 A. I don't think it's an error. It wasn't
9 necessary.

10 Q. Wasn't Doshi --

11 A. It's not depicted in 11, the sidewall
12 shown. Doshi says we do rapid thermal oxidation to
13 make part of the sidewall filament, and we do
14 nitride sidewall formation by CVD and anisotropic
15 etch to make the other component of sidewall
16 filament. But he doesn't break up -- despite having
17 said that there are two components to 11, he doesn't
18 attempt to draw that separately.

19 So I think it -- remember, as I said
20 before, Doshi is trying to look at a much bigger
21 picture than the '997 is. So he teaches the dual
22 step, the two-step etch and the use of the nitride

1 and the BPSG to do a self-aligned contact. He
2 teaches that as part of a much larger picture in the
3 Doshi patent.

4 So leaving out some details which are
5 in some of the places not put it in the figure, but
6 it's explained in the text. Everything doesn't have
7 to be in -- at least as I understand it, there is no
8 need for the patent to show every detail of the
9 specification in figures.

10 Q. So what you're saying is that some
11 aspects of what Doshi disclosed in his text are not
12 directly reflected in its figures?

13 A. Yes.

14 Q. The one error that you did find is the
15 error in the etching of the nitride layer 30, which
16 is what you pointed out in your declaration with
17 respect to Figure 3g, though; correct?

18 A. Yeah. I guess I would say I'm a little
19 uncomfortable with the notion of depicting that as
20 an error because I think the description in the
21 specification tells us what these shapes will look
22 like, and they were known to one of ordinary skill.

1 So I would rather have seen it drawn
2 differently, but error sounds like there's something
3 fundamentally wrong. I think that's too strong a
4 word.

5 Q. Okay. Well, you called it an error.

6 A. Yeah, I know. Maybe not the best
7 choice of words.

8 Q. Are there other errors in the depiction
9 of the etching of nitride layer 30 in the figures of
10 the Doshi reference?

11 MR. MUKERJI: Objection to form.

12 THE WITNESS: It's possible, but I
13 don't know of any. I mean, we could argue -- I
14 think it's difficult. We could argue about exactly
15 what the sidewall profile would look like after the
16 nitride is etched to form the sidewall -- sidewall
17 spacer, and that has to do with how anisotropic the
18 etch is and so on there.

19 We could quibble about these
20 details, but I know how these drawings are made.
21 They're made by a draftsman who gets a sketch and
22 tries to make it right, and they're not always

1 accurate.

2 BY MR. CHEN:

3 Q. Okay. So it's better to rely on the
4 text of the reference as opposed to the figures; is
5 that fair?

6 MR. MUKERJI: Objection to form.

7 THE WITNESS: I would like to look
8 at both and -- and understand what was known at the
9 time by one of ordinary skill and conclude from that
10 that set of things.

11 BY MR. CHEN:

12 Q. All right. Following the etch of the
13 plug contact openings, Doshi talks about the
14 formation of plugs within those plug contact
15 openings; correct?

16 A. Uh-huh.

17 Q. And then it says that if you were, for
18 example, forming a DRAM circuit, you would also have
19 to open up bit line contact openings; correct?

20 A. Which line are you at?

21 Q. Beginning at line column 10 line 31.

22 A. Uh-huh.

1 Q. And the formation of the bit line
2 contact openings is effectively the same as the
3 formation of the plug contact openings; correct?

4 A. Well, I'd have to look a little more
5 closely at that because I didn't really concentrate
6 on this part.

7 Q. Okay.

8 A. When I was studying this patent, I was
9 more interested in the plug contact because that's
10 really where the issue appears.

11 Q. So you don't have an opinion as to
12 whether the formation of the bit line contact
13 opening is the same as the formation of the plug
14 contact opening; correct?

15 A. Give me just a minute, please.
16 (Reviewing document).

17 I'm sorry. I'm taking some time to
18 interpret the numbers in 3i. (Reviewing document).

19 Okay. I'm sorry. Can we come back to
20 the question now about the bit line contact?

21 Q. My question was simply that whether you
22 had provided any opinions about the formation of the

1 bit line contact opening.

2 A. No, I don't think so.

3 Q. Okay. And so you don't have an opinion
4 as to whether the formation of the bit line contact
5 opening is the same -- or you don't have any
6 opinions as to whether the process used to form the
7 bit line contact openings is the same as the process
8 used to form the plug contact openings; correct?

9 A. I have not looked at the description of
10 the bit line contact etch. I read it, but I didn't
11 pay a lot of attention to it.

12 Q. Okay.

13 THE REPORTER: Exhibit 7.

14 (Document marked, for
15 identification purposes, as Rubloff Exhibit No. 7.)
16 BY MR. CHEN:

17 Q. Okay. I've asked the court reporter to
18 mark as Exhibit No. 7 patent number 5,770,498, which
19 I believe is referred to as the Becker reference.

20 Dr. Rubloff, is Exhibit 7 one of the
21 patents that you selected to be used in Samsung's
22 IPR of the '997 patent?

1 A. Yes.

2 Q. And you did that selection yourself;
3 right?

4 A. Yes.

5 Q. Which was about six months ago,
6 roughly?

7 A. Whenever it was. (Laugh).

8 This is the one that was referenced by
9 the IPR board somehow as not having the same stature
10 as the Doshi. I don't -- I didn't quite understand
11 that. But it was my selection, yes.

12 Q. All right. I also want to kind of do
13 something similar to what we did with Doshi, kind of
14 walk through the process that's disclosed in the
15 Becker reference.

16 I believe the discussion of the process
17 begins at column 4 line 9.

18 A. (Reviewing document).

19 Q. Again, I think the first step during
20 the formation is to form the isolation regions;
21 correct?

22 A. Right. The field oxide 16.

1 Q. And then Becker describes the formation
2 of the gate electrode beginning at line or column 4
3 line -- roughly around line 22; correct?

4 A. Uh-huh.

5 Q. Does Becker describe the etch process
6 used to form the gate electrode structure?

7 A. (Reviewing document). Well, line 22.

8 "Transistor gate electrode gate 18 is
9 formed by successively depositing or 'stacking'
10 layers of polysilicon 20, tungsten silicon 22 and
11 silicon nitride 24 over thin gate insulating layer,
12 and then patterning and etching those layers to
13 expose substrate 12 at the desired locations of the
14 source and drain for the access transistors."

15 That's polysilicon -- polysilicon gate.

16 Q. And my question was: Does Becker
17 describe the specific etch process used to form the
18 gate electrode structure?

19 A. Oh, you mean the etch gas and the power
20 and all that stuff?

21 Q. Or even what type of etching process is
22 used.

1 A. Well, what he says is these layers
2 which are deposited and patterned and etched using
3 conventional methods well known in the art.

4 Oh, I'm sorry. That, no.

5 "Then patterning and etching those
6 layers to expose substrate." Yeah. Yeah. These
7 layers. Yeah, this is line 25 to 29 or something.

8 Q. What are some of the conventional
9 methods of etching known in the art in this time
10 frame?

11 A. Reactive-ion etching would be most
12 common, I think.

13 Q. Are there other types?

14 A. Well, you want to define the gate
15 electrode by an anisotropic process. So it would
16 be, in this time frame, reactive-ion etching would
17 be common, but there are other configurations of
18 equipment that could do that. Inductively coupled
19 plasma, for a while ECR plasma, electron cyclotron
20 resonance plasma, which are high density plasma
21 etching techniques.

22 Q. And all of these other etching

1 techniques are considered conventional methods well
2 known in the art?

3 A. Yes.

4 Q. After the formation of the gate
5 electrode, Becker describes the next step as
6 implantation of impurities into the substrate;
7 correct?

8 A. Uh-huh.

9 Q. What is the purpose of this
10 implantation step?

11 A. Well, the transistors require doped
12 regions to make a PNP or an NPN transistor. So
13 these regions 28 are the regions that with the gate
14 electrode in place and the field oxide 16 in place,
15 having cleared the gate stack material from the
16 region between those two things, the ion implant 26
17 would form these doped regions 28. And to have an
18 active device, you have to have doped regions.

19 Q. But those doped regions 28 are not the
20 source/drain regions; correct?

21 A. Some of them will be.

22 Q. Well, the reason I say that is because

1 in the patent at column 4 line -- beginning at line
2 40 --

3 A. I'm sorry. Where?

4 Q. Column 4 beginning at line 40, the
5 patent says:

6 "The resulting doped p-regions 28
7 extend into the channel area between the
8 subsequently formed source and drain for each access
9 transistor."

10 So I'm wondering whether that indicates
11 that channel region or the doped p-region 28 is
12 something that's different from the subsequently
13 formed source/drain.

14 A. Well, notice that the regions 28 extend
15 under the gate electrode; right? And so that's -- I
16 think that's a design choice made for designing the
17 dopant profile of the transistor in this case.

18 Q. So --

19 A. And that would be formed, I believe, by
20 annealing to activate the dopants that were
21 implanted.

22 Q. So is the region 28 different from the

1 source/drain region?

2 A. I don't think so. I don't recall if
3 this is something atypical or unusual.

4 Q. But the source/drain region has not yet
5 been formed at this step in the process; correct?

6 A. Yeah. I have to look at this more
7 closely. I just don't remember how this part goes.
8 It's not the part I was most interested in for the
9 '997 patent.

10 (Reviewing document). It's a more
11 complicated structure. I'm sorry. I hadn't
12 remembered the details of that because I was
13 focusing on other parts.

14 (Reviewing document). Okay. I'm
15 sorry. I have lost the question.

16 Q. You know, it wasn't controversial.
17 I was just asking whether region 28 is
18 part of this. Well, actually --

19 A. It's not --

20 Q. -- I'll ask you the exact question that
21 I asked before the long pause.

22 At this particular step in the process

1 following the formation of region 28, the
2 source/drain regions have not yet been formed;
3 correct?

4 A. (Reviewing document). Yes, I think
5 that's right.

6 Q. Okay.

7 A. 32a and b are the source/drain regions.

8 Q. Okay. Following the formation of the
9 p-regions 28, the next step in the process is the
10 deposition of the spacer insulating layer 30;
11 correct?

12 A. Okay.

13 Q. What is the spacer insulating layer?

14 A. 30 is nitride; right?

15 Q. What is the function of that layer?

16 A. Well, the reason Becker was chosen is
17 that the structure you see in Figure 4 corresponds
18 to the way the '997 patent and the Doshi
19 reference -- the Doshi patent etch a self-aligned
20 contact through BPSG to an etch-stop layer of
21 nitride in the second step going through that to
22 make contact to the substrate, source/drain

1 contacts, and during that process leaving a sidewall
2 spacer of nitride.

3 That was the part I considered relevant
4 to the '997 patent here. The rest of the details of
5 the dopant profiles and so on I didn't consider as
6 relevant to '997.

7 Q. Okay. So when the spacer insulating
8 area is first deposited, it is deposited, according
9 to Becker, in the range of 600 to 2,000 angstroms;
10 correct? That is at column 4 line 46.

11 A. Okay.

12 Q. And after it's deposited, that layer is
13 then thinned in certain regions to the range of 50
14 angstroms to 400 angstroms; correct?

15 A. Yes.

16 Q. Okay. And the regions that are thinned
17 are the portions of the spacer insulating layer
18 above the gate electrode and above where the
19 source/drain regions are to be formed between the
20 gate electrode as shown in Figure 3; correct?

21 A. Uh-huh.

22 Q. The thickness of the spacer insulating

1 layer that is on the sidewalls of the gate are not
2 thinned and remain close to the original deposition
3 thickness of 600 to 2,000 angstroms; correct?

4 A. Uh-huh.

5 Q. I'm sorry. Uh-huh. Is that a yes?

6 A. Yes. I'm sorry.

7 Q. Why is the thickness of the spacer
8 insulating layer over the -- what will later be the
9 source/drain regions, why is that portion of the
10 spacer insulating layer thinned?

11 A. (Reviewing document). Gee, I've looked
12 at this, this aspect.

13 Q. Maybe it will help you. I can refer
14 you to column 4 line 66 through column 5 line 5.

15 A. (Reviewing document). Well, as it says
16 here -- thank you -- column 5:

17 "Under etching spacer insulating layer
18 30 to leave a thin layer of nitride material
19 provides a diffusion barrier during subsequent
20 processing."

21 Nitride is a good diffusion barrier.

22 Q. Now, following the formation of the

1 spacer insulating layer and then the subsequent
2 thinning of that layer in certain regions, Becker
3 describes a process where lightly doped drain
4 implants are used to form the source and drain
5 regions; correct?

6 A. Uh-huh.

7 Q. All right. And that --

8 A. Yes.

9 Q. -- begins at column 5 line 6; correct?

10 A. Yes.

11 Q. Okay. How are the impurities here
12 implanted into the source/drain regions?

13 A. Through the nitride, the thinned
14 nitride.

15 Q. So won't the thinned nitride interfere
16 with implantation?

17 A. No.

18 Q. Why not?

19 A. In fact -- well, the implantation depth
20 can certainly be greater than the thinned nitride
21 thicknesses. You can adjust the implantation energy
22 to get the penetration and compensate for the

1 presence of the nitride that's there.

2 In fact, these kinds of layers nitride
3 used in them is not crystalline, it's amorphous.
4 And so very often when you do an implantation, you
5 want to make sure you're not channelling along the
6 crystalline axis of the substrate. And so you want
7 to put something that the -- that the implant ions
8 go through which randomizes to some extent what
9 their trajectory is so they don't channel deeply
10 into the crystalline lattice.

11 Q. But the implantation parameters you use
12 with the presence of the nitride layer there as
13 opposed to the parameters used without the nitride
14 will be different; correct?

15 A. Yeah, somewhat different.

16 Q. Because you have to compensate for your
17 ability to penetrate through the nitride layer?

18 A. Yeah. The energy loss of the ion going
19 through different materials is quite well
20 understood.

21 Q. Okay.

22 A. So you would know, okay, I wanted the

1 peak position to be of the implant distribution,
2 kind of Gaussian, to be so far below the silicon
3 surface, but I'm going to lose this much energy
4 going through the nitride. So I'll just change the
5 implant energy.

6 Q. Okay. The thickness of that nitride
7 layer will also affect the parameters of the
8 implantation that you use to achieve your targeted
9 dopant profile; correct?

10 A. Yeah. Unless it's thin enough it
11 doesn't matter.

12 Q. And if you add another layer on top of
13 the nitride layer, that too would affect the
14 implantation parameters that you need to use to
15 achieve your dopant profile; correct?

16 A. It could.

17 Q. In fact, the thicker the materials
18 covering this substrate that is -- sorry.

19 The more material you have covering the
20 substrate, the higher the implantation energy or
21 impurity dosage you would need to use to achieve the
22 same dopant profile; correct?

1 A. Not dose, but energy.

2 Q. Okay. Only energy?

3 A. Energy.

4 Q. Okay. So --

5 A. I'm sorry. Energy to get the right
6 depth into the substrate, but you may lose some of
7 that that gets buried in the thin layer on the top.

8 Q. Right.

9 A. And so you may have to change the dose
10 a little too.

11 Q. Okay. So the material covering the
12 substrate -- would the amount of material covering
13 the substrate will affect both the implantation
14 energy required as well as the impurity dosage
15 required to achieve your targeted dopant profile for
16 the source/drain region?

17 A. Yes, it could.

18 Q. Okay. In this step where Becker is
19 performing the lightly doped drain implants, what is
20 the function of the spacer insulating layer?

21 A. You're referring to which figure?

22 Q. Figure 3.

1 A. And you're talking about the spacer
2 insulating layer --

3 Q. Yes.

4 A. -- which is 18 on the sidewall of the
5 gate electrode?

6 Q. I think it's layer -- I think it's --

7 A. I'm sorry.

8 Q. -- 30.

9 A. 30. 18 --

10 Q. 18 is the gate electrode.

11 A. -- is the top of the gate electrode.

12 30. I'm sorry.

13 Q. Yes.

14 A. So 30 on the sidewall of the gate
15 electrode will be an implant mask, part of an
16 implant mask.

17 Q. Okay. So it's a doping spacer?

18 A. It's a doping spacer.

19 Q. Okay. Could you explain again how the
20 portion of the spacer insulating layer 30 on the
21 gate electrode -- on the sidewall of the gate
22 electrode acts as a spacer during this step?

1 A. In Figure 3, so 40 are the ion implant
2 trajectories.

3 Q. Right.

4 A. They are coming in a directional
5 fashion into the substrate 12, and they will
6 penetrate through the thinned nitride number 30, but
7 they won't penetrate through the sidewall spacer 30
8 next to the gate electrode.

9 And the consequent dopant profiles that
10 you get will be determined by that and by whatever
11 annealing process and associated thermal diffusion
12 the dopants happen during implant activation anneal.

13 Q. So it's creating space between where
14 you're doing your implantation and the gate
15 electrode?

16 A. Right.

17 Q. And so the spacer insulating layer 30
18 at this stage in the process is a spacer in the
19 context of how you construed it for the '997 patent;
20 correct?

21 A. Uh-huh.

22 Q. Is that a yes?

1 A. Yes.

2 Q. All right. Following the implantation
3 step -- and, actually, you know, before we go on, I
4 don't know how long we've been going.

5 MR. MUKERJI: It's been just a few
6 minutes past an hour.

7 MR. CHEN: Okay. You want to take
8 a quick break then?

9 MR. MUKERJI: Sure.

10 (Recess - 4:51 p.m. - 5:03 p.m.)

11 BY MR. CHEN:

12 Q. The Becker process does not disclose
13 the thermal oxidation of the sidewalls of the
14 polysilicon or the substrate for the diffusion
15 regions; correct?

16 A. (Reviewing document). That's right.

17 Q. Okay. If you turn to Exhibit 5, which
18 we introduced earlier in the day. This is the Wong
19 reference --

20 A. Right.

21 Q. -- that you referred to on page 47 of
22 your declaration.

1 A. Yeah.

2 Q. So the Wong reference is the one that
3 teaches the use of thermal oxidation to repair
4 damage created by reactive-ion etching; correct?

5 A. Yes.

6 Q. Does Wong address other forms of
7 etching other than reactive-ion etching?

8 A. (Reviewing document). Not other forms
9 of etching, but does address channel ion
10 implantation as a source of defects, but that's not
11 -- it's not really an etching process.

12 Q. Does Wong teach that thermal oxidation
13 will also help repair defects created through
14 channel ion implantation?

15 A. Yes.

16 Q. Where does it teach that?

17 A. At least in the abstract, polysilicon
18 sidewall oxidation is also necessary to protect the
19 thin oxide from degradation by source/drain ion
20 implantation.

21 Q. Okay. But those are two different
22 forms of protection; correct?

1 A. Which two?

2 Q. Well, the benefit of the thermal
3 oxidation for repairing defects caused by
4 reactive-ion etching is that -- well, let me
5 rephrase that.

6 What Wong teaches is that thermal
7 oxidation can be used to repair defects that are
8 caused by reactive-ion etching; correct?

9 A. Uh-huh.

10 Q. What Wong teaches for the polysilicon
11 sidewall oxidation is that it can help create a thin
12 oxide that will then protect the source/drain region
13 from subsequent damage by ion implantation; correct?

14 A. That certainly isn't how I read the
15 abstract.

16 Q. Okay. Well, so then are you saying
17 that the sidewall oxidation repairs damage to the
18 source/drain regions that were created during ion
19 implantation in the same way that it would repair
20 damage created by reactive-ion etching?

21 A. I'm sorry. You said sidewall oxidation
22 of a polysilicon to protect the thin oxide during

1 ion implantation.

2 Q. Right.

3 A. Is that what you said?

4 Q. Well, I was wondering whether the
5 benefits of the thermal oxidation are different, I
6 said, as applied to reactive-ion etching and --

7 A. Yes.

8 Q. -- as applied to ion implantation.

9 A. Well, according to the abstract,
10 reactive-ion etching to define the polysilicon gate
11 hurts the quality of the thin oxide. But if you
12 then do sidewall oxidation to the polysilicon, you
13 can reduce that problem.

14 Q. Because it will repair the damage --

15 A. Right.

16 Q. -- that had already occurred?

17 A. (Reviewing document). Yeah.

18 So -- so the conclusion, I don't
19 remember the ion implantation part because it's not
20 the part I focused on, but the conclusion in this
21 abstract is that the sidewall oxidation does help
22 protect the thin oxide, meaning the gate oxide, from

1 degradation during implantation where you're usually
2 using the gate as a mask for ion implantation. So
3 the ions are going straight at the edge of the gate
4 oxide where the RIE damage could be. It's the same
5 location.

6 Q. And that process isn't repairing damage
7 that has already occurred but, rather, preventing
8 damage from occurring; correct?

9 A. Yes.

10 Q. All right.

11 A. Or at least primarily so.

12 Q. Okay. Does Becker disclose the
13 potential defects that will be created through
14 reactive-ion etching of a gate electrode?

15 A. (Reviewing document). I don't think
16 so. I'm just reviewing it again.

17 Q. Looking at Exhibit 5, the Wong
18 reference, if you turn to page 12 and we look at
19 Table 1 at the top of page 12.

20 A. I'm sorry. Can you hold just a
21 minute --

22 Q. Sure thing.

1 A. -- while I finish scanning this?

2 (Reviewing document). I'm sorry.

3 Q. No problem.

4 A. Please go ahead.

5 Q. Okay. I was -- if you could turn to

6 Exhibit 5, which is the Wong reference --

7 A. Uh-huh.

8 Q. -- page 12. And you look at Table 1

9 above.

10 Does Wong teach that the defect density
11 for plasma etching is significantly lower than the
12 defect density for reactive-ion etching?

13 A. Well, what she did was only RIE here.
14 That's the only way you can make the gate. I don't
15 know what process you'd be referring to as "plasma
16 etching." RIE is a plasma etch process.

17 Q. Okay. Well, if you look at the table,
18 the second line says:

19 "Polysilicon gate 60 mil dot plasma
20 etched."

21 A. (Reviewing document). I'm sorry.

22 Q. So --

1 A. You're right. On page 158, she
2 mentions "defined by RIE or plasma etching" and 60
3 mil dots are big. That's pretty big.

4 Okay. So the defect density in plasma
5 etching is certainly higher than it is with RIE.

6 Q. Oh, it's higher than it is?

7 A. Oh, wait. I'm sorry. I was looking at
8 aluminum gate. Which are you referring to: A
9 general statement for aluminum or polysilicon gate?

10 Q. For the polysilicon gate.

11 Let me re-ask the question.

12 Does Wong teach that the defect density
13 for plasma etching is significantly lower than the
14 defect density for reactive-ion etching?

15 A. No.

16 Q. Why not?

17 A. Well, the plasma etch 60 mil dot on
18 polysilicon gate is 26 per centimeters squared. If
19 you look at the edge of the field oxide with RIE,
20 it's 19, and if you look at the edge on the gate
21 oxide, it's 88. I don't think that's a clear
22 conclusion.

1 Q. Okay. If you turn to page 10 Figure 2,
2 I think you can see the distinction between 2a, 2b,
3 and 2c.

4 A. (Reviewing document). Yes.

5 Q. So is it fair then to say that the
6 second line of Table 1 on page 12 describing plasma
7 etching and Figure 2b, with reference to Figure 2b,
8 is comparable to the fourth line in that table which
9 is describing reactive-ion etching with reference to
10 Figure 2b?

11 A. (Reviewing document). Well, the
12 descriptors are a little confusing because it
13 appears to compare RIE the fourth line to plasma the
14 second line edge on gate oxide to 60 mil dot. I
15 think they are the same thing. And the conclusion
16 from that could be that 26 is notably less than 88.

17 Q. In your experience, does plasma etching
18 cause fewer defects than reactive-ion etching?

19 A. I don't have any direct experience
20 comparing them because most of the time people do,
21 where I've -- where I've been involved, it's all
22 RIE. So we don't look at plasma etching because you

1 can't define things with it.

2 Does it make sense that it would be
3 less? The answer to that is yes because
4 reactive-ion etching imparts tens or hundreds of
5 volts of ion energy to the plasma species that are
6 doing the etching and, therefore, they have a lot
7 more kinetic energy to impart and do damage.
8 Whereas, plasma etching is typically lower energy
9 ions, considerably lower.

10 Q. What do you mean when you say you can't
11 define things with plasma etching?

12 A. It's not directional. It's not an
13 anisotropic.

14 Q. Oh.

15 A. By definition, plasma etching means you
16 don't bias the substrate where the wafer is to
17 accelerate DC the ions so they have hundreds of
18 volts, for example, of energy when they do the
19 etching. That's how you get anisotropy.

20 Q. Okay.

21 A. So basically plasma etching is
22 irrelevant here. Irrelevant to the technology.

1 Q. Dr. Rubloff, did you draft the
2 declaration by yourself?

3 A. The declaration was drafted by the
4 attorneys and my specification. We had talked to
5 all of these issues and -- well, part of it, part of
6 the text was drafted and then I came in. And we sat
7 for hours and looked through it and went through
8 every line to decide, am I comfortable with that?
9 But it was my decision what those statements were.

10 Q. And when were you --

11 A. I needed somebody to help write this
12 thing.

13 Q. Sure. When were you first retained to
14 work for Samsung on these IPRs?

15 A. My guess was six months ago, but I
16 don't know.

17 Q. Okay.

18 A. Something like six months.

19 Q. Probably a little longer than six
20 months since your declaration is dated
21 December 16 --

22 A. Oh.

1 Q. -- 2014.

2 A. Yeah. Then I've -- then I've put it in
3 the back of my memory.

4 Q. Okay. You don't remember what exact
5 date you were retained?

6 A. No. No.

7 Q. Okay. I want to just --

8 A. For the drafting of the declaration,
9 when I said that there was help coming from the
10 attorneys to draft it, I'm talking about the typing.
11 We had gone through all the arguments. I decided
12 what it should say. I asked them to put it in the
13 right order because otherwise from a legal point of
14 view, it may be hard to follow. And then we went
15 through it in great detail.

16 I guess I was confused by what you
17 meant "drafting." I didn't type the first version.

18 Q. Sure.

19 A. But I directed it.

20 Q. I want to ask you another question,
21 kind of returning back to Doshi. And this is about,
22 you know, the issue of the nitride layer 30 and

1 whether it remains on the sidewalls of the gate
2 electrode.

3 Let me refer to you the right section
4 of the patent.

5 The step is described at column 9
6 beginning at around line 56, extending through
7 column 10 line 3.

8 And I understand it's your opinion that
9 the etch process described here would etch away
10 certain portions of the nitride layer, but would
11 leave some of the nitride layer on the sidewalls of
12 the gate electrode; right? That's your opinion;
13 correct?

14 A. Yeah. The etch process will remove the
15 nitride from the horizontal regions and leave
16 nitride on the sidewall.

17 Q. Okay. If you -- if the nitride -- does
18 the amount of nitride that is removed depend on the
19 specific parameters of the nitride etch process?

20 A. The nitride that's removed from the
21 sidewall?

22 Q. Yes.

1 A. Well, the proper way to ask that
2 question is to ask whether the anisotropy depends on
3 the parameters of the process.

4 Q. Okay.

5 A. Right? Because you're going to remove
6 from the -- from the horizontal areas at the
7 source/drain and at the top of the gate, and you're
8 going to remove a lesser amount from the sidewall
9 because it's directional etching.

10 But directional by how much? So what's
11 the etch rate ratio sideways compared to vertically?
12 And that will depend to some extent on the details
13 of the process you use.

14 For example, the possible -- the gas
15 chemistry. So the ions that are involved. The
16 voltage, the self-bias voltage that determines what
17 the ion energies are when you're etching and
18 pressures then and things like that.

19 Q. So it is possible to have an
20 anisotropic etch that will remove the entire nitride
21 layer including the portions that are on the
22 sidewall of the gate electrode; correct?

1 A. That would be called an isotropic etch
2 because the nitride was put down by a CVD process
3 that puts the same thickness on the sidewall as on
4 the top and the bottom. So if you say that it
5 removes everything from the sidewall when you're
6 clearing the bottom, that means the horizontal and
7 vertical etch rates are the same. That's called an
8 isotropic etch.

9 Q. But if you extend that -- if you were
10 performing an anisotropic etch and you extended that
11 etch for a longer period of time, wouldn't you
12 remove then the material on the sidewalls?

13 A. Well, if you have a vertical etch rate
14 of a hundred and you have a side -- a horizontal
15 etch rate of one and you over-etch by a factor of a
16 hundred, eventually you'll get there, but that's not
17 a relevant condition. I mean, it's not -- it's not
18 what people do.

19 People use timed etches in the
20 worst-case and institute process sensors to tell
21 when they're done with the etching. It's called
22 endpoint detection in etching. You can measure

1 optical emission from the plasma that changes when
2 you clear the nitride or other techniques to do
3 that.

4 Q. When you're -- when you have a very
5 thin layer of nitride, how do you control the amount
6 of nitride material that's left on the sidewalls?

7 A. I don't understand the question.

8 Q. Well, when you're performing an etch,
9 there's a certain amount of tolerance in the etch;
10 correct?

11 A. Well, generically speaking, anything
12 has that, but I still don't understand the question.

13 Q. So if you had a thin layer of nitride
14 and your intent was to keep some of that nitride on
15 the sidewall, are there certain precautions that you
16 would need to take to make sure that the material
17 left on the sidewall was intact?

18 A. Was in fact?

19 Q. Intact.

20 A. Intact. I don't -- this is a
21 hypothetical example where, from what you asked, the
22 only issue is, I start with thin layer nitride on

1 the sidewall.

2 Q. Right.

3 A. Can I prevent it from ever being
4 etched? I just don't understand the context of the
5 question.

6 Q. Is it your opinion that in every case
7 where you have anisotropic etch of a nitride
8 layer --

9 A. Isotropic.

10 Q. Anisotropic.

11 A. Okay.

12 Q. In every case where you're performing
13 an anisotropic etch of a nitride layer covering a
14 gate electrode structure and the diffusion regions
15 to the sides of that gate electrode structure, that
16 anisotropic etch of that nitride layer will leave
17 some material on the sides of the gate electrode,
18 some nitride material on the sides of the gate
19 electrode?

20 A. If you have an anisotropic etch and you
21 clear the horizontal surface, for example, at the
22 diffusion region, then as long as you stop at about

1 the point where you've cleared it or 10% over-etch
2 or something like that, you will have something,
3 have nitride left on the sidewall.

4 Q. Okay. But if you continue to etch past
5 the point of simply just removing the nitride on the
6 horizontal regions, you potentially would remove the
7 nitride material that's left on the sidewalls;
8 correct?

9 A. The question was asked and answered
10 already.

11 Q. And what was the answer?

12 A. The answer was that if you have an
13 anisotropy of -- I gave the example of one to a
14 hundred. So a hundred times faster on the vertical
15 direction than on the sidewall, you would have to
16 etch a very long time, a huge over-etch that is far
17 beyond what anyone could possibly make the mistake
18 of doing, in order for that low rate of one on the
19 sidewall to remove the same initial thickness of
20 film produced by the nitride CVD process.

21 Q. In your experience with anisotropic
22 etches, what is the typical ratio of the vertical

1 etch as compared to the horizontal etch?

2 A. It depends very much on the process.
3 Some processes are -- I mean, you can -- you can
4 easily find, you know, two to five or 10 as an
5 anisotropy ratio, but you have DRAM capacitor
6 structures in all of these devices that have
7 trans-capacitors that have aspect ratios of a
8 hundred.

9 So now you're talking about very high
10 anisotropy of order of a hundred or more.

11 Q. Okay.

12 A. So it can be very high, and it's not
13 just a question of the distribution of impinging
14 ions this way and this way. There's much more
15 reactive-ion etching chemistry involved because a
16 part of the etching in the vertical direction can
17 lead to the formation of films on the sidewalls that
18 further suppress the sideways etching. So it
19 depends on the ion -- ion chemistry.

20 Q. Okay. But the range is -- there's a
21 wide range?

22 A. There's a wide range.

1 Q. Okay. And that range that you gave is
2 roughly two to five to one to one hundred?

3 A. Yeah, something of that order.

4 Q. If the range was two to five, then you
5 would not need to extend your anisotropic etch that
6 long to remove the material on the vertical
7 sidewall; correct?

8 A. Well, you know that you need, let's
9 say, a hundred seconds to do the etch on the
10 diffusion region. So if it's five, you have to do
11 500; right? You're not going to make that kind of
12 mistake. One of ordinary skill would never do that.

13 Q. I'm sorry. I'm not sure if I got the
14 math right.

15 You said if you needed a hundred
16 seconds and the ratio was two to five, you would
17 need to do 500 seconds?

18 A. If the ratio was five.

19 Q. Right.

20 A. You'd need to do 500 seconds.

21 Q. Okay. If the ratio was two to five,
22 how much time would you need?

1 A. 200 to 500.

2 Q. So --

3 A. But --

4 Q. -- 250 seconds?

5 A. Yeah, something like that. But no one
6 is going to do this. You know you want a sidewall
7 there. That's what the invention of Doshi is about
8 and --

9 Q. But -- sorry.

10 A. -- in '997.

11 Q. Did you say that the invention in Doshi
12 is about forming those sidewalls?

13 A. It's part of what's done.

14 Q. But it's not mentioned anywhere in the
15 text of Doshi?

16 A. We talked about that already.

17 Q. Right.

18 A. I think it's very clear that that's
19 what Doshi is doing.

20 Q. I know. I understand. But you said
21 that that's what the invention of Doshi is about.

22 A. Right.

1 Q. And I just want to make sure I
2 understand it because it's not actually mentioned
3 anywhere in the text of Doshi; right?

4 MR. MUKERJI: Objection to form.

5 THE WITNESS: I'll have to
6 continue to disagree about whether Doshi teaches it
7 properly.

8 MR. CHEN: Okay. Okay. Let's
9 take a quick break and then let me just review my
10 notes a little bit. It shouldn't be long. Five
11 minutes.

12 (Recess - 5:41 p.m. - 5:47 p.m.)

13 THE REPORTER: Exhibit 8.

14 (Document marked, for
15 identification purposes, as Rubloff Exhibit No. 8.)

16 MR. MUKERJI: Are you moving to a
17 different declaration?

18 MR. CHEN: I am.

19 MR. MUKERJI: Before you do that,
20 I need to ask a couple questions of him.

21 MR. CHEN: Oh.

22 MR. MUKERJI: So, counsel, is your

1 cross on the '997 patent complete?

2 MR. CHEN: Yes.

3 MR. MUKERJI: Okay. I have just a
4 couple of questions for him on that patent.

5 EXAMINATION

6 BY MR. MUKERJI:

7 Q. Dr. Rubloff, I'd like you to pull out
8 what had been marked as Exhibit 3 earlier today, and
9 it's titled "The Errata, Declaration of Gary W.
10 Rubloff, Ph.D."

11 Mr. Chen had marked that earlier today,
12 and I'm not sure if the discussion really got to it.

13 Can you just tell us what this errata
14 is, please, sir?

15 A. There's a paragraph in the -- in my
16 declaration for the '997 patent that we just talked
17 about, and the paragraph mistakenly refers to the --
18 in paragraph 11 the '893 patent and the filing date
19 in 1996, and it really should have been talking
20 about the corresponding '997 patent with a 1999
21 filing date in that paragraph 11.

22 It was just a clerical error probably

1 because of copying from one to the other.

2 Q. In conducting your work on the '997
3 patent, did you apply this information about the
4 '893 patent, or did you use the '997 patent
5 information that you described in this paragraph?

6 A. No. I used the '997 information, but I
7 can imagine, you know, having -- having talked about
8 these issues and deciding what I thought was the
9 appropriate position for me to take on these issues
10 and which of the prior art publications to use in my
11 declaration, I then needed help to -- to type these
12 things in and give me something to work with.

13 And I can easily imagine that knowing
14 there were three things, there's a lot of
15 duplication of paragraphs between the three
16 declarations, and I can easily imagine someone
17 copied it. I don't know who typed this stuff. But
18 copied it and didn't catch the change from that one.
19 And looking through them took a long time and I just
20 missed it.

21 MR. MUKERJI: Pass the witness.

22 EXAMINATION

1 BY MR. CHEN:

2 Q. So, Dr. Rubloff, I asked the court
3 reporter to mark as Exhibit No. 8 your declaration
4 submitted in connection with Samsung's IPR of the
5 '244 patent.

6 Please take a brief moment to look over
7 this document. I just want to make sure this is
8 your declaration.

9 A. (Reviewing document).

10 MR. MUKERJI: Counsel, while he's
11 doing that, just as a housekeeping matter, so are
12 you restarting the exhibits for each different
13 patent or are we -- what's the plan?

14 MR. CHEN: I'm continuing using.
15 I mean, this is 8. So.

16 MR. MUKERJI: Okay.

17 MR. CHEN: I don't -- I mean, I
18 only introduced one exhibit I think for his
19 background, his CV. So.

20 MR. MUKERJI: That's fine. I just
21 want to make sure everyone is on the same page.

22 THE WITNESS: (Reviewing

1 document). Okay.

2 BY MR. CHEN:

3 Q. And so this is your declaration
4 submitted in connection with Samsung's IPR for the
5 '244 patent; correct?

6 A. Yes, this is my declaration.

7 Q. And does this declaration contain any
8 and all relevant opinions you have regarding the
9 issues related to Samsung's IPR for '244 patent?

10 A. Yes.

11 Q. Do you have any opinions regarding
12 issues relevant to Samsung's IPR of the '244 patent
13 that were not included in your declaration?

14 MR. MUKERJI: Objection to form.

15 THE WITNESS: You're talking about
16 Samsung's petition?

17 BY MR. CHEN:

18 Q. Yes.

19 A. So I think I've seen that, but I
20 haven't really read it. I've concentrated on my
21 declaration.

22 Q. Do you have any opinions regarding the

1 validity of the '244 patent that were not included
2 in your declaration?

3 A. No.

4 Q. Are you aware of any errors or
5 omissions in your declaration?

6 A. Not at this time.

7 Q. All right.

8 A. Unless we find one. Another typo.
9 (Laugh).

10 THE REPORTER: Exhibit 9.

11 (Document marked, for
12 identification purposes, as Rubloff Exhibit No. 9.)
13 BY MR. CHEN:

14 Q. Okay. I've asked the court reporter to
15 mark as Exhibit 9 patent number 6,150,244 titled
16 "Method For Fabricating MOS Transistor Having Raised
17 Source and Drain."

18 You referred to this exhibit as the
19 '244 patent for this deposition.

20 Did you read the '244 patent?

21 A. Yes.

22 Q. When did you first read the '244

1 patent?

2 A. Well, I guess it was more than six
3 months ago. (Laugh). Maybe a year ago.

4 Q. After you were retained by Samsung to
5 work on these IPRs?

6 A. Yes.

7 Q. And you understand the '244 patent?

8 A. Yes.

9 Q. Okay. What would you say is the point
10 of novelty of the '244 patent?

11 A. Well, if I believe, as I do, that there
12 is prior art which describes all the claims and
13 invalidates the patent, then it's hard for me to
14 call it novel, but the claim is and it's purported
15 to be novel in the domain where the prior art would
16 also be considered novel, I consider novel in prior
17 art, and it's a prescription for how to form a
18 shallow junction.

19 Q. A shallow junction. Is that the same
20 thing as a raised source and drain?

21 A. It's the goal of a raised source and
22 drain. A goal of a raised source and drain.

1 Q. What is a raised source and drain?

2 A. Well, I think what's more important is
3 to understand what's the motivation for the shallow
4 junction.

5 Ion implantation, the standard
6 technique or conventional doping techniques, don't
7 allow the design of source and drain profiles to be
8 as shallow and, therefore, as high performance as
9 one would like.

10 So for quite some time the community
11 has been looking for ways to form very shallow
12 junctions. We have conferences about that that have
13 been going on for decades now.

14 And so I think that the raised source
15 and drain provides a vehicle, as described in this
16 patent and in the prior art, for producing dopant
17 atoms above the crystalline silicon surface that can
18 then be allowed with proper thermal treatment to
19 diffuse shallowly into the crystalline silicon
20 surface.

21 And so if you imagine that I look at
22 what the drain and what the source look like, it's

1 silicon that's heavily doped or reasonably doped,
2 and if I had some of that above the crystalline
3 surface in the form of polysilicon with dopants,
4 that would be a very nice source for essentially
5 contact doping from that raised source/drain, looks
6 like a raised source/drain -- looks like a
7 source/drain material into the crystalline silicon.

8 Q. Okay. So what you're saying is that
9 the raised source/drain refers to the dopant or
10 impurities that are above the silicon substrate that
11 are then subsequently diffused into the substrate to
12 form the shallow junction following a heat
13 treatment; is that --

14 A. Yes.

15 Q. So the raised source/drain doesn't
16 actually refer to the source/drain that is then
17 ultimately formed in the substrate; correct?

18 A. No. The raised source/drain is the
19 source part -- I'm sorry for using "source" in two
20 ways -- is the part which is above the crystalline
21 silicon surface.

22 Q. Okay. And that is how you understand

1 the term "raised source/drain" as it is used in the
2 '244 patent?

3 A. Yeah. It says -- it says here, for
4 example, in '244.

5 "There is plenty of room for
6 improvement in the fabrication of metal oxide
7 devices having raised source and drain electrodes."

8 Q. Which paragraph are you looking at in
9 your declaration?

10 A. Oh, that's the end of 17.

11 Q. And the '244 patent describes or claims
12 a process for fabricating a semiconductor device;
13 correct?

14 MR. MUKERJI: Objection to form.

15 BY MR. CHEN:

16 Q. Let me re-ask that.

17 The '244 patent claims a process for
18 fabricating a semiconductor device comprising a
19 raised source and drain; correct?

20 A. That's what claim 1 says. Introduction
21 to claim 1.

22 Q. And claim 1 lays out a sequence of

1 steps for that process; correct?

2 A. No. It lays -- lays out a list of
3 steps involved in that process, but not a sequence.

4 Q. Okay. So it's your --

5 A. Not necessarily a sequence.

6 Q. Okay. So is it your opinion then that
7 claim 1 does not list a sequence of steps for that
8 process?

9 A. It lists a set of steps that are part
10 of that process, but it does not tell uniquely what
11 the order of that is. So I can't say sequence.

12 Q. Is that true for every limitation of
13 claim 1?

14 A. You mean for each of the forming,
15 forming, forming --

16 Q. Yes.

17 A. -- when you say "limitation"?

18 Q. Yes.

19 A. No. There are some that you couldn't
20 switch around. I mean, you couldn't randomly change
21 these, but there is flexibility that would have been
22 known to one of ordinary skill.

1 Q. Okay. Some of these steps or
2 limitations have to be performed in a specific
3 sequence; correct?

4 A. Well, normally would be performed in a
5 specific sequence. I don't -- I don't at this point
6 have alternative ways to move some of them around --

7 Q. Okay.

8 A. -- in mind.

9 Q. Your opinion that some of these
10 limitations can be performed out of their listed
11 order is limited to the limitation beginning with
12 "removing a top portion of said fourth dielectric
13 layer" and then the subsequent limitation "forming
14 on the substrate a pattern second resist layer";
15 correct?

16 A. Yes.

17 Q. Okay. As far as you understand, the
18 rest of the limitations or steps in claim 1 should
19 be performed in their listed order; correct?

20 A. (Reviewing document). I'm just looking
21 through it one more time to be sure. Yes.

22 Q. And generally when we're talking about

1 a semiconductor process, the order in which the
2 different steps in the process are performed will
3 affect the structure of the device that's being
4 manufactured; correct?

5 MR. MUKERJI: Objection to form
6 and also outside the scope.

7 THE WITNESS: Well, what you get
8 depends on how you do it. In a general sense, yes.

9 BY MR. CHEN:

10 Q. So the sequence in which you perform a
11 list of steps will affect the resulting structure
12 that is being manufactured; correct?

13 MR. MUKERJI: Objection to form
14 and also to scope.

15 THE WITNESS: There are cases
16 where the order might be changed and changes in
17 structure would be minimal. So I wouldn't make a
18 blanket statement that you always change the
19 structure by changing the order.

20 BY MR. CHEN:

21 Q. But in most cases, if you change the
22 order, you will change the structure?

1 MR. MUKERJI: Same objections.

2 THE WITNESS: I don't know how to
3 audit "most." I can think of cases where it won't
4 change it.

5 BY MR. CHEN:

6 Q. Okay. For example? Could you give me
7 an example?

8 A. A laminate structure. Suppose I want a
9 laminate structure of -- I'm going to put a thin
10 film structure in place maybe for optical
11 interferometry applications, or something like that,
12 and I have AB, AB, AB or ABC, ABC, ABC. And I could
13 switch some of those, and it wouldn't make any
14 difference.

15 Q. But the structure of what you're
16 laminating would be different, though. Whether it
17 makes a difference or not is a different issue;
18 right?

19 A. Yeah. I need to think about this. I
20 mean, a question like that --

21 Q. I'm not trying to --

22 A. -- asks for speculation that -- that

1 requires some dreaming to think about whether there
2 are exceptions or there are examples that could be
3 given.

4 Q. All right. Sitting here today then,
5 can you -- you cannot think of a situation where
6 changing the order of the steps in a semiconductor
7 manufacturing process does not affect the ultimate
8 structure of what you're manufacturing?

9 MR. MUKERJI: Objection. Outside
10 the scope.

11 THE WITNESS: I don't agree with
12 that because your suggestion is that I cannot think
13 of that. I would need to think pretty hard to see
14 if I can think of an example.

15 BY MR. CHEN:

16 Q. Okay.

17 A. And I probably could think of one.

18 Q. But you would need to -- let me ask it
19 like this.

20 Have you provided an opinion in your
21 declaration about whether changing the order of
22 steps in a semiconductor process will change the

1 structure of a device that's being manufactured?

2 A. Well, how much change in structure
3 should I use as the metric for answering yes or no?

4 Q. Any change in structure.

5 A. Well, does that mean an angstrom of
6 change in the thickness of one of the layers? Does
7 that mean what?

8 Q. Did you provide an opinion in your
9 declaration about whether changing the structure --
10 order of steps in a process will change the
11 structure of the manufactured device?

12 A. I don't think so. I think I provided
13 an opinion that there are ways in which you can --
14 you can meet the claims here in the '244 patent with
15 different orders of claim -- of the two components
16 in claim 1.

17 Q. Okay.

18 A. I can make that structure and, whether
19 it looks a little bit different or not, it satisfies
20 all of the components of claim 1. So I can change
21 the order.

22 MR. MUKERJI: Gentlemen, I don't

1 mean to interrupt this fascinating discussion, but I
2 think we have hit seven hours. So we have sucked
3 the marrow out of the day. Is that about right? We
4 hit seven hours, Madam Court Reporter?

5 I don't want to deprive anyone of
6 a minute, you know, but --

7 MR. CHEN: You know, it's okay. I
8 don't want to put you on the spot. I think we're
9 close. We'll continue this tomorrow. It's going to
10 be just as fascinating tomorrow as it is this
11 evening. So.

12 MR. MUKERJI: All right. Everyone
13 have a good evening.

14 (Signature having not been waived,
15 the taking of the deposition adjourned at 6:10 p.m.,
16 to reconvene Wednesday, August 19, 2015, at 9:00
17 a.m.)

18
19 * * *
20
21
22

CERTIFICATE OF COURT REPORTER

UNITED STATES OF AMERICA)

DISTRICT OF COLUMBIA)

I, DENISE D. VICKERY, the reporter before whom the foregoing deposition was taken, do hereby certify that the witness whose testimony appears in the foregoing deposition was sworn by me; that the testimony of said witness was taken by me in machine shorthand and thereafter transcribed by computer-aided transcription; that said deposition is a true record of the testimony given by said witness; that I am neither counsel for, related to, nor employed by any of the parties to the action in which this deposition was taken; and, further, that I am not a relative or employee of any attorney or counsel employed by the parties hereto, or financially or otherwise interested in the outcome of this action.

Denise D. Vickery

Notary Public in and for the
District of Columbia

My Commission expires February 14, 2018

DEPOSITION ERRATA SHEET

Our Assignment No. 173194

Case Caption: SAMSUNG ELECTRONICS CO. LTD. vs. HOME
SEMICONDUCTOR CORPORATION

DECLARATION UNDER PENALTY OF PERJURY

I declare under penalty of perjury
that I have read the entire transcript of
my Deposition taken in the captioned matter
or the same has been read to me, and
the same is true and accurate, save and
except for changes and/or corrections, if
any, as indicated by me on the DEPOSITION
ERRATA SHEET hereof, with the understanding
that I offer these changes as if still under
oath.

Signed on the _____ day of
_____, 2015.

GARY W. RUBLOFF, PHD

DEPOSITION ERRATA SHEET

Page No. _____ Line No. _____ Change to: _____

Reason for change: _____

Page No. _____ Line No. _____ Change to: _____

Reason for change: _____

Page No. _____ Line No. _____ Change to: _____

Reason for change: _____

Page No. _____ Line No. _____ Change to: _____

Reason for change: _____

Page No. _____ Line No. _____ Change to: _____

Reason for change: _____

Page No. _____ Line No. _____ Change to: _____

Reason for change: _____

SIGNATURE: _____ DATE: _____

GARY W. RUBLOFF, PHD

DEPOSITION ERRATA SHEET

Page No. _____ Line No. _____ Change to: _____

Reason for change: _____

Page No. _____ Line No. _____ Change to: _____

Reason for change: _____

Page No. _____ Line No. _____ Change to: _____

Reason for change: _____

Page No. _____ Line No. _____ Change to: _____

Reason for change: _____

Page No. _____ Line No. _____ Change to: _____

Reason for change: _____

Page No. _____ Line No. _____ Change to: _____

Reason for change: _____

SIGNATURE: _____ DATE: _____

GARY W. RUBLOFF, PHD

	10:09 a.m	17	79:8,9,11	244
\$	54:3	257:10	125:10,	251:5
	10:22 a.m	18	12,17	252:5,9,
\$400	54:3	214:8	126:1,10	12 253:1,
8:16	10:49 a.m	226:4,9,	132:2,4	19,20,22
	75:3	10	149:16	254:7,10
(11	19	167:9,13	257:2,4,
	132:3	22:20	235:1	11,17
(14)	138:8	138:2,7	2,000	263:14
200:21	169:3	234:20	220:9	25
(30)	170:1,6	264:16	221:3	46:15
200:22	178:6	1977	20	215:7
	199:1	17:4	19:7	250
1	207:11,17	1980	30:22	130:10
	249:18,21	18:5	55:7	247:4
	11:05 a.m	1985	108:5,12	26
1	75:7	17:13	177:12	171:8
12:21	12	1986	214:10	199:12
13:1,4	93:6	17:13	20-minute	216:16
79:8,11	138:7,9	25:7	123:13	234:18
149:20	214:13	34:12	200	235:16
232:19	227:5	1987	247:1	27
233:8	232:18,19	18:16	2013/2014	145:9
235:6	233:8	1992	14:14	148:6
257:20,	235:6	16:3	2014	150:10
21,22	125	19:18	238:1	28
258:7,13	46:15	1993	2015	145:9
259:18	12:15 p.m	69:14	264:16	162:16
263:16,20	124:11	1994	22	163:4
1%	14	20:8	169:4	216:13,
31:13	179:8	70:19	170:9,14,	17,19
10	195:22	1996	15 171:7	217:6,11,
11:5,6	15	249:19	214:3,7,	14,22
163:19	108:5,12	1999	10	218:17
179:5,10	137:21	249:20	23	219:1,9
201:8	158	1:09 p.m	191:18	29
202:4	234:1	125:2	192:1	153:4,5
210:21	16		24	154:10
235:1	213:22		170:15	215:7
239:7	216:14		171:7	2:09 p.m
245:4	237:21		214:11	162:22
10%		2		2:29 p.m
244:1				162:22
		2		

2a	198:17	189:21		5:41 p.m
235:2	199:5	195:13	5	248:12
	203:22	201:14		
2b	204:5,14	203:6,8,		5:47 p.m
148:2	208:15	12,18,20	5	248:12
235:2,7,	209:9	204:2,18	142:13,	
10	219:10,14	205:4	15,20	
	221:18	208:17	149:17	6
2c	226:8,9,		221:14,16	
235:3	12,14,20	3h	222:9	6
	227:6,7,	178:8	228:17	159:19,21
3	17 238:22	3i	232:17	160:2,5
		201:19,21	233:6	163:4
3	31	211:18	5,770,498	187:22
79:8,11	153:5		212:18	222:9
125:14,	210:21	4		6'
16,19	32		50	164:10
126:5,14	158:1,2	4	93:6	6,150,244
142:6	32a	130:19,21	220:13	253:15
189:12	219:7	131:2	50%	6,277,720
195:19	37	149:16,17	89:13,19	160:2
201:10	182:4	179:5	91:10	
220:20	203:15,20	213:17	500	60
225:22	3:16 p.m	214:2	246:11,	189:12
227:1	188:15	217:1,4	17,20	233:19
239:7	3:38 p.m	219:17	247:1	234:2,17
249:8	188:15	220:10	5000	235:14
30		221:14	18:15	60/40
176:14	3a	40	51	175:20
177:20	163:13	202:5	163:12	600
178:7	164:2,7,	217:2,4	52	8:17
179:8	10 165:21	227:1	164:1	220:9
180:1,10,	170:4	40/60	55	221:3
20 181:3	3d	175:19	164:1	65
184:22	195:19	400	56	177:10
185:10	196:2	220:14	239:6	66
186:21	3f	46	57	176:5
187:9	195:11,15	220:10	168:18	221:14
188:20	206:20	47	59	6:10 p.m
189:7,20	3g	228:21	172:15	264:15
190:12,20	177:11	4:51 p.m	5:03 p.m	
191:16	178:5,9	228:10	228:10	7
193:2,15,	179:20			
19,22	183:19,22			
194:5,21				
196:4				
				7

162:16		218:9	access	actual
163:4,22	9	219:18	214:14	139:14,22
168:18		220:4,6	217:8	add
172:15	9	227:19	accomplish	64:13
176:5	177:10	247:10	55:16	80:11
212:13,	199:12	249:1,16,	accurate	136:10
15,18,20	213:17	20 250:2,	210:1	141:2
7'	239:5	4,6	achieve	224:12
164:10	253:10,	9:00	86:22	addition
70	12,15	264:16	224:8,15,	22:1
177:10	90-degree		21 225:15	additional
73	147:9	A	acid	129:21
22:22	90s		191:10	130:3
77	10:3 28:2	A-12	acids	address
23:1	997	200:13	94:10	40:15
	126:3,12,	a.m.	acquainted	42:19
8	20	264:17	19:10	118:6
	127:13,20	AB	act	130:4
8	128:11,20	261:12	187:9,18	150:4
132:4	129:11,18	ABC	188:5	229:6,9
176:13	130:6,7	261:12	199:5	addressed
190:11,	131:4,13,	ability	acting	185:4
14,15,17	15,19,22	8:2 34:20	14:22	addressing
191:18	133:1	157:18	197:13	153:5
192:1	134:13	223:17	activate	191:3,6
248:13,15	137:22	absolutely	217:20	adequate
251:3,15	145:14	183:14	activation	130:8
80s	149:10,	abstract	32:10	adhesion
10:3 21:2	12,15	143:4	227:12	42:1
27:21	152:4,18	229:17	active	adjourned
28:11	153:1,7,	230:15	32:11	264:15
41:7	10 160:6,	231:9,21	119:9	adjust
165:7	10 161:15	academia	163:7	222:21
88	162:7	69:14	189:17	adjustable
234:21	177:7	academics	216:18	36:16
235:16	178:17	70:20	activities	161:21
893	180:16	accelerate	14:1,6	adjusted
249:18	182:10	236:17	acts	36:15
250:4	186:13	accepted	101:6	adopted
	187:8	57:19	189:9	32:15
	189:22		226:22	36:12
	190:5			
	198:4			
	207:21			
	212:22			

advanced	ALD	42:6	31:21	117:19
20:4,11	29:3		32:19	120:7
21:18	187:21	analogy	33:3	121:5
26:13		92:12	35:16	122:3
105:17	aligned	angle	57:8	123:5,22
	152:12	147:9	193:6,7	147:18
advice	alkali	angstrom	194:6	156:9
12:1	114:8	263:5	196:8	
advisor	allowed	angstroms	217:20	application
70:15	19:21	86:4	227:11	s
affect	105:7	88:20		117:21
8:2	255:18	220:9,14	annotation	185:4
39:12,13		221:3	204:1	202:20
133:3,10,	alternative			261:11
21	72:13	anisotropic	anodic	
140:10,18	259:6	92:6,8,9,	173:9	applied
167:6,20		16,21	anodization	18:14
168:2,12,	alternative	93:11,12	173:19	52:11
15 224:7,	s	94:1,12	answering	63:2
13 225:13	37:4	138:16,19	263:3	65:22
260:3,11	altitude	161:16	answers	141:6
262:7	152:15	180:4,6	7:9 8:3	231:6,8
affected	aluminum	181:4,9		apply
88:1	31:6,12	182:19	anticipate	47:11
affects	41:11,20,	183:16	41:19	117:21
166:16	22 42:8	189:16	139:10	250:3
AFTERNOON	109:16	200:14	anticipatin	apportionin
125:1	234:8,9	207:14	g	g
agree	ambiguity	209:17	41:3	6:7
56:1	54:22	215:15	Appeal	appreciable
262:11	ambiguous	236:13	12:7	84:13
agreed	57:11	240:20	appears	approach
6:9 76:2	amenable	241:10	202:2	33:15,16
agreement	amorphous	243:7,10,	211:10	44:3 47:2
8:21 76:8	223:3	13,16,20	235:13	approaching
ahead	amount	244:21	applicabili	87:14
30:15	55:10	246:5	ty	appropriately
233:4	86:4	anisotropy	21:5 33:9	97:12
aimed	225:12	240:2	applicable	approximati
23:12	239:18	244:13	118:10	on
airplane	240:8	245:5,10	application	21:8
146:6	242:5,9	anneal	113:17	area
	amounts	227:12	114:14,20	28:14
		annealing	116:22	

147:8	245:7	6:21 7:10	background	based
155:8,15	aspects	attorneys	72:20,22	23:11
217:7	17:17	237:4	73:1	basically
220:8	18:7 43:8	238:10	74:2,7,14	78:4
areas	45:2 47:5	atypical	76:10,15	100:16
74:4	134:17	218:3	108:4	107:15
240:6	208:11	audit	251:19	191:1
argue	assembling	261:3	bad	193:14
209:13,14	40:12	August	144:6	236:21
argument	assignment	264:16	bandgap	basis
57:21	67:14	availabilit	109:14	15:6
83:2,10	assume	y	Barner	22:7,13
arguments	202:8	37:5	32:17	65:21
238:11	assumed	average	barrier	143:19
arrive	68:22	44:6	119:22	batch
132:6	assumption	90:17	120:2,5,	77:21
art	7:16	136:5	6,10,11,	78:1
49:10	ASTL	aware	13,14	battery
118:8	26:13	76:19	121:4,11,	29:5,9
130:6,7	atom	128:17	21 122:1,	beam
132:7	206:12,19	129:6	2,4,5,10,	25:11
134:12,21	atomic	253:4	15,18	95:15
160:10,11	23:17	axis	123:4	97:1
184:14	29:7	223:6	150:2	98:19,21
186:14	atoms		156:21,22	99:3,4,7
196:3	85:12	B	176:20	107:10
215:3,9	112:21	bachelor's	190:20	beams
216:2	121:20	135:13	191:2,11	95:8
250:10	255:17	back	193:10,20	Becker
254:12,	attempt	53:1 54:4	194:3,17	212:19
15,17	207:18	69:10	195:2,5	213:15
255:16	attempts	75:8	196:8,11	214:1,5,
ashing	107:5	109:9	197:6,13	16 216:5
101:19	attention	125:9	198:1,2,	219:16
asks	23:1	149:5	9,20,21	220:9
261:22	128:3	183:11	199:5	222:2
aspect	195:5	192:20	200:14	225:18
43:7,9	197:5	203:3	221:19,21	228:12
47:9 50:8	212:11	211:19	barriers	232:12
98:5	attorney	238:3,21	41:22	beginning
105:2			base	29:21
134:22			44:22	39:21
221:12			45:6	45:11

137:21	bigger	bold	208:1	168:9
176:5,13	207:20	68:18	219:20	broadest
190:15	biomaterial	bombard	break	150:12
210:21	s	84:18	7:20,21	broadly
214:2	24:19	border	50:18,21	57:19
217:1,4	biomems	158:20	52:21	broke
239:6	24:19	159:6	54:1	163:3
259:11	bit	borderless	75:14,18	brought
begins	24:1 33:2	158:4,6,	76:8	34:14
138:8	47:1	8,10	77:15	68:17
162:15	61:20	159:9	108:13	73:15
192:1	65:2 76:4	Bordonaro	124:10	130:10
199:12	83:7	16:6	162:18,20	build
213:17	96:10	18:12	189:2	106:8
222:9	97:20	boron	207:16	building
behaving	139:8	190:21	228:8	23:19
200:1	180:8	192:10	248:9	29:5
beneficial	199:11	193:10,	breakdown	builds
179:9	202:3,7,9	16,20,21	110:14	178:18
benefit	205:12	199:1	112:9	buildup
56:18	206:10	bottom	briefly	183:7
81:16	210:19	29:11	168:19	built
139:14,	211:1,12,	43:15	bring	35:13
16,21	20 212:1,	90:5,8,22	73:6	bump
140:8	4,7,10	175:15	bringing	107:17
230:2	248:10	180:2	73:11	bunch
benefits	263:19	241:4,6	88:2	67:20
138:3,5	blanket	boundary	157:20	143:15
141:13	148:20	166:9	broad	160:15
231:5	260:18	BPSG	29:17,18	buried
Bernie	BLC	179:8	54:14	225:7
34:19	200:20	186:11	118:11	Burlington
35:10	201:4,19	190:22	150:14	16:6
bias	202:3,7,9	192:5,7,	152:9	18:12
182:20	bled	15,20	153:17	21:20
236:16	96:9	193:4,21	154:3,13	22:12
big	blowup	194:6,21	157:5	26:15
47:10	204:2	195:21	broad-brush	32:18
49:22	board	196:8,20	36:22	69:20
107:17	12:7	197:11	broader	business
195:4	128:4	199:10,19	95:19	
203:2	213:9	200:3,21	153:21	
234:3		201:16	154:4	

69:4	cap	54:20	causing	6,10,20
buy	31:12	57:5 71:6	32:10	changed
16:10	capabilitie	80:21	caveat	14:17,21
	s	carries	111:17	72:15
	19:13	58:3,10	Center	260:16
C	25:8	carry	14:18	changing
	capability	17:20	centered	15:6
California	67:19	38:18	48:18	36:12
10:3	106:7	40:4	centimeters	39:7
call	136:9	carrying	234:18	43:13
13:5 24:1	capable	63:6	central	141:22
35:2 36:3	65:16	case	16:9	167:6
52:12	capacitants	10:2	18:13	260:19
56:10	41:17	11:19	141:18	262:6,21
57:10	capacitor	12:15,18	CEO	263:9
61:18	28:12	15:20	67:14	channel
68:14	89:3,4	25:6	challenge	217:7,11
87:1	245:5	48:12	50:2 88:4	223:9
100:13	capacitors	68:10	chamber	229:9,14
121:11	49:5	87:11	57:6,7,9	channelling
122:17	184:11	166:19	58:1	223:5
254:14	capital	217:17	chambers	characteris
called	97:3	243:6,12	38:20	tic
5:5 16:8	capping	cases	change	110:1
22:4	30:22	9:21,22	42:21	141:19
26:12	car	10:6,10,	46:20	143:17
29:7	137:19	17 11:2,	71:19	characteris
34:18	carbon	10,12	72:6 73:9	tics
50:12	138:22	12:4,5,8	110:17	206:1
85:3	care	24:12	164:12	characteriz
88:18	85:18	57:3 89:8	167:9	ation
100:15	career	260:15,21	180:8	43:10
102:5	48:22	261:3	205:22	61:7,17
107:9	careful	casually	224:4	71:14
111:6	81:11	109:20	225:9	78:2
115:19	102:2	catalytic	250:18	79:14
125:4	Carolina	23:1	258:20	characteriz
165:5	38:11	catch	260:18,	ations
166:4	carried	250:18	21,22	42:14
209:5	52:3	caused	261:4	characteriz
241:1,7,		54:13	262:22	e
21		79:15	263:2,4,	27:19
camera		230:3,8		
5:15				

characteriz	240:15	13,18,20,	163:7	156:15
ing	245:15,19	21 127:7,	177:12	clean
72:19	Chen	18 128:9	202:2	21:18
122:16	5:8,13,17	129:20	210:18	22:5,8
charge	6:11,18,	130:19,22	circuits	24:15
16:6	21 9:17	135:16	119:12	32:20
156:12,18	13:2	142:13,18	cite	79:13,15
charged	15:22	147:19	185:21	138:21
136:12	20:20	159:19,22	cited	cleaning
chart	27:5,22	162:21	160:6	25:10
65:7	35:5 38:1	163:1	claim	139:12
chemical	43:21	173:1	149:16,20	cleanliness
23:12	45:8,13	185:7,16	182:10	32:3
25:9	46:6	187:4	254:14	clear
42:13	50:16,19,	188:16	257:20,	6:8 39:18
54:13	22 52:16	210:2,11	21,22	73:22
64:8	54:2,4,5	212:16	258:7,13	76:13
83:12	56:4,19,	228:7,11	259:18	153:8
84:12,16	21 59:4	248:8,18,	263:15,	178:2,15,
86:20	60:8	21 249:2,	16,20	19 180:1,
100:11	61:12,19	11 251:1,	claimed	14 181:2
104:12,15	62:21	14,17	149:20	183:13,14
120:11	65:13	252:2,17	claims	185:5
122:9,17,	68:19	253:13	130:6,7	186:9
22 140:6	72:4,17,	257:15	254:12	204:12
156:11,16	21 73:4,	260:9,20	257:11,17	206:15,17
157:19	13,20	261:5	263:14	234:21
173:10,	74:6,14,	262:15	Clara	242:2
17,18	21 75:10,	264:7	52:11	243:21
191:6	13 77:9	chip	clarificati	247:18
chemically	78:15	106:5	on	cleared
83:21	80:5	choice	64:11	216:15
139:2	81:4,20	209:7	clarify	244:1
169:19	107:6	217:16	7:15	clearing
chemicals	108:14,16	choose	27:6,13	241:6
94:10	109:8	35:21	63:12	clerical
101:18	112:3	152:8	64:13	249:22
chemistry	114:21	chose	73:16	close
20:14	115:10,14	49:10	clarity	26:18
61:4	117:10	chosen	53:18	27:10
87:6,7,16	118:12	72:12	54:7	155:12
135:20	120:21	86:21	154:19	221:2
137:4	123:10,	219:16	circuit	264:9
172:12	12,14,17,	characteriz		
	19 124:5,			
	9 125:8,			

closed 97:13	collaborato rs 90:14	129:18 237:8	compatibili ties 43:20	207:17 263:15,20
closely 141:14 211:5 218:7	colleagues 32:18 34:22 90:14	comment 195:9	compatible 104:6	composed 169:16
cloudy 16:22	collimated 107:22	commercial 22:10 35:7	compensate 44:18 222:22 223:16	composite 170:1
cluster 16:12,16 18:16 32:4 35:3 38:19,22 39:13 52:4 56:11 57:4,10, 14,21 58:3,10	column 149:17 162:16 163:4,22 168:18 172:15 176:5,13 177:10 179:5 189:12 190:11, 14,15 191:18 192:1 199:12 201:8 202:4 210:21 213:17 214:2 217:1,4 220:10 221:14,16 222:9 239:5,7	common 99:13 109:4 114:10,11 215:12,17	compensated 8:12	composition 61:9 133:7,20 134:2
CMOS 41:1 46:16 116:1		communicati ng 90:13	compensatio n 8:15	comprised 198:12
CMP 104:16, 18,19 105:4,15, 22 106:6, 12,21 107:5,11		community 255:10	complete 8:3 127:1 129:10 249:1	comprising 149:21 257:18
co-advisor 70:15,17		company 48:10 67:6	completely 7:8 13:14 42:16 102:8 121:22	computer 55:4 72:3
CO2 139:2	columns 72:16	comparable 235:8	completeness 11:21	conceivably 139:5 173:22 174:1
coating 137:16	combined 57:16 62:8	compare 130:5 136:13 235:13	completion 101:10 177:12	concentrate 211:5
collaborate d 16:5 21:3	combines 95:21	compared 33:21 88:14 111:9 120:16,17 240:11 245:1	complicated 21:11,15 56:10 67:15 88:3,6 110:10 218:11	concentrate d 202:21 252:20
collaborati ons 18:10	comfortable 47:20 90:13	comparisons 118:7	component 161:16,17 194:2 207:15	concentrati ons 165:2
		compartment alize 81:11	components 170:2	concern 183:1

concerted 67:8	conferences 255:12	119:11 122:12 157:18 164:17 165:11	constructio n 153:6,9, 13,20 154:6,12, 20 155:3, 20 156:6, 8 157:4, 14 158:2 162:6 177:11	20 212:1, 4,7,8,10 219:20,22 256:5
conclude 91:12 181:12 210:9	conferring 76:7			contacts 103:21 220:1
conclusion 231:18,20 234:22 235:15	confidential 19:3 confidentiality 18:20	connection 7:3 15:12 126:2,11 179:6 251:4 252:4		contents 131:21
conclusions 128:7	confidentially 18:19	connotes 54:19	construed 113:16 145:14 227:19	context 47:18 115:8 116:10 117:5,19 120:19
condition 79:7 93:18 241:17	configurati on 39:1	consensus 78:20	consumed 175:14	123:6,22 145:14,18 148:18,21 149:1,9 152:4,18, 22 155:7 158:7,10 159:16 162:6 198:4 227:19 243:4
conditions 25:15 110:14 172:7	configurati ons 215:17	consequence 193:18	consuming 10:21	
conduct 75:20	confirms 184:3	consequence s 66:5,6 79:22 91:3 133:2 193:12	contact 71:8 131:3 145:20 146:4 158:11,17 159:3,12 178:8 180:2,3 192:19 195:20 199:11,15 200:20 201:5,11, 12,15 202:3,6, 7,9 203:8 204:3,6 205:7,20 206:4,7, 8,13,16 208:1 210:13, 14,19 211:2,3, 9,12,14,	
conducting 158:21 250:2	conformal 29:6 161:16 204:10	consequent 227:9		
conductive 153:11,14 154:13,15 155:1,22 156:3 157:7,16, 17	conformaliti y 87:2,9 88:22 89:10 92:13	considerabl y 236:9		contexts 95:5
conductivit y 156:4	conformally 193:2	considerati ons 19:14		continue 77:1 102:7 244:4 248:6 264:9
conductor 41:11 110:19	confused 238:16	considered 62:17 134:11 150:11 165:13 216:1 220:3 254:16		continued 23:8 125:4,7
conference 13:22 14:5 66:2	confusing 235:12	constant 86:10,12		continues 138:9
	conjured 91:2			continuing 251:14
	connected			

continuous 17:5	coordinate 146:19,22	151:12,16 153:2,11 160:7 163:8,11 165:14 170:6,9, 14 171:21 172:2,15, 18 174:11 175:1 176:10 180:21 181:19 182:1,3, 7,15 183:20 184:9,22 185:11 190:8,13 191:18,21 192:2,5, 8,15 197:22 198:9,10, 12,13,15 199:6,7, 16,20 200:4,7 203:6,9, 12 205:1 207:1 208:17 210:15,19 211:3,14 212:8 213:21 214:3 216:7,20 218:5 219:3,11 220:10, 14,20 221:3 222:5,9 223:14 224:9,15, 22 227:20	228:15 229:4,22 230:8,13 232:8 239:13 240:22 242:10 244:8 246:7 252:5 256:17 257:13,19 258:1 259:3,15, 19 260:4, 12 correction 24:18 correctly 119:10 corresponds 189:22 219:17 cost 51:21 costs 37:2,20 Council 16:7 counsel 6:6 75:19 76:1,7, 10,13,14 248:22 251:10 count 91:14 counterpart 16:16 couple 11:22 40:17	44:13 49:13 65:19 136:1 248:20 249:4 coupled 34:15 46:3 215:18 court 7:8 13:3 56:17 125:22 126:4 131:1 142:19 160:1 212:17 251:2 253:14 264:4 cover 76:2 100:3 150:14 153:18 154:3,14 155:3 157:5 171:7 coverage 87:3 88:9,10, 11,18 89:1,9, 11,14,20 90:5,9,10 91:10,14 covered 6:3 88:15 90:4 157:13 162:5
continuousl y 23:15	coordinates 146:17 copied 250:17,18 copper 41:22 42:8,22 copying 250:1 corner 140:18 141:3 179:19 180:7 181:10 182:6 183:6 201:18 corners 179:9,12 181:18 Corporation 5:19,20 7:2 16:8 correct 20:22 34:1 37:9 39:21 45:3 47:9 57:1 58:21 90:1 117:22 120:15 126:15 128:12 129:12 130:13 131:22 133:22 134:13			
contrast 84:13				
control 10:22 20:4,11 30:15 31:8,12 32:2 242:5				
controlling 20:17				
controls 31:1				
controversi al 218:16				
convenient 51:13 59:2,6				
convention 57:19				
conventiona l 179:22 183:4 215:3,8 216:1 255:6				
conventiona lly 189:15				
converted 174:22 175:5				
converting 174:15				

172:4	166:11	113:5,6	238:5	250:8
204:22	crystalline	137:17	249:18,21	decision
covering	193:12	141:6	dated	237:9
194:21	223:3,6,	145:22	237:20	decisions
196:4	10	173:3	David	16:10
200:9	255:17,19	174:5,8,	5:22	declaration
224:18,19	256:2,7,	13 187:21	day	6:8 73:22
225:11,12	20	189:15	6:15 23:9	74:5,12,
243:13	CT	204:10	66:4	17 76:6,
covers	200:20	207:14	228:18	16,20
128:7	201:4	241:2	264:3	126:1,5,
184:18	202:13	244:20	days	11,15,17
create	current	CVS	18:4 26:6	127:1,9,
176:9	9:7	14:2	55:5	14,21
230:11	14:13,15	cycle	65:1,2	128:7,12
created	89:11	57:5	67:12,15	129:4,7,9
72:7	106:5	cyclotron	76:4 99:5	130:1
229:4,13	110:9,12,	215:19	106:3	131:9
230:18,20	13 117:14		164:19	132:3
232:13	currents	D	DC	143:1
creating	110:11		236:17	145:10
35:1	112:10	damage	deal	148:5
155:4	curriculum	139:6	69:6 80:4	150:11
227:13	13:4	141:10,15	105:4	160:22
critical	CV	145:4	132:21	185:22
18:7	13:6,12,	179:9,14,	203:2	186:6
25:18	13 19:17	21 181:3,	deals	195:12,14
78:12	24:18	10,18	133:1	200:12
cross	251:19	182:6,13	decades	203:21
6:8 249:1	CVD	183:1,4	255:13	204:17
cross-	17:10	229:4	December	208:16
examination	20:13	230:13,	237:21	228:22
6:4,7	23:19	17,20	decent	237:2,3,
7:3,5	26:4	231:14	111:14	20 238:8
74:1	29:3,6	232:4,6,8	decide	248:17
75:21	31:5	236:7	55:22	249:9,16
76:3,15,	38:17	damaged	237:8	250:11
19	41:7	182:1	decided	251:3,8
cross-	83:14,16,	date	160:17,19	252:3,6,
examine	19,20	9:15	238:11	7,13,21
74:11	84:13	13:14,15,	deciding	253:2,5
crosses	86:16	16,21		257:9
	88:4 91:4	14:5,12		262:21
	92:13	15:8		263:9

declaration	defines	demagnifyin	122:3,4	13,15
s	36:9	g	123:5,21	174:10
72:19	148:21	96:21		214:9
74:16			depends	
75:22	definition	demand	10:14	deposition
76:3	53:21	39:4	37:11	6:3 7:2
250:16	57:2	demanding	57:2	8:17
	114:2	103:4	60:19	23:12,17
declared	116:18		64:20	25:10
204:20	117:20	demands	87:11	29:6,7
	118:14,	39:7	101:13	31:5
deep	16,19	demarcation	112:6	40:10
89:8	120:13,	49:19	130:14	42:12,13
168:17	15,17		188:6	43:9 44:1
deeply	121:2	demonstrate	240:2	45:2 47:6
223:9	122:4	63:11	245:2,19	48:1 50:7
	123:1	density	260:8	52:19
defect	132:6	138:6,12		54:16,20
138:6,12	152:17	140:9,11,	depicted	55:19
140:9,10,	153:19	13,22	45:18	57:1,4,6
13,22	156:14	143:15	189:21	58:20
143:14,21	163:18	175:10	203:18	62:2,7,12
233:10,12	198:3	215:20	205:4	75:21
234:4,12,	236:15	233:10,12	207:11	77:2
14		234:4,12,	depicting	83:12
defects	definitions	14	208:19	84:3,6,
32:10	50:20			11,20
141:17	96:8	department	depiction	85:21
143:11,21	116:10	19:21	209:8	86:1,3,8,
229:10,13	117:5	165:9		10,12,18,
230:3,7	degradation	depend	deposit	21,22
232:13	31:22	39:10	88:5	89:15,21,
235:18	142:21	87:5	104:9	22 90:6
	143:6	113:9	106:17,19	112:16
define	229:19	188:3	113:2	113:2
49:9 90:3	232:1	239:18	deposited	161:16
138:17		240:12	84:2	174:5,8
143:9	degrades		86:5,9,15	192:14
144:4	143:10	dependency	91:15,21	219:10
159:5		26:5	106:15	221:2
163:7,21	degree	dependent	168:15	253:19
165:18	48:16	149:16	169:6	264:15
215:14	49:13,15		215:2	
231:10	134:5,20	depending	220:8,12	deprive
236:1,11	135:13,14	47:18		264:5
	136:7,21	113:17	depositing	
defined	delay	116:10	23:4	depth
65:20	79:13	117:5	86:16	61:8
234:2			102:12,	

135:19	designing	develop	14,21	165:4
222:19	88:4	29:15,20	31:1,16	245:6
225:6	217:16	30:6	34:6 35:8	257:7
derivative	designs	31:14	39:20	dielectric
23:18	91:2	34:3 35:6	43:4	108:18
describe	134:3	37:9,14	44:21	109:5,10,
16:22	desire	40:22	46:8,10	22 176:22
45:9	41:21	67:6 97:6	47:21	191:17
58:15	desired	100:15	51:3	259:12
200:13	214:13	developed	54:13	dielectrics
214:5,17	detail	31:2,3	71:7	42:3
describes	13:19	97:12	102:8	109:13,20
182:8	64:13,14	105:4,14	104:4	differ
190:12	129:16,22	107:11	114:19	167:17
193:1	130:3	137:14	115:8,9	difference
214:1	169:22	developing	116:1	86:17
216:5	171:5	15:16	117:19,21	92:4,20
222:3	185:15,18	37:12	119:9	134:4
254:12	208:8	43:3	137:13	141:22
257:11	238:15	45:10,21	144:22	149:7
describing	detailed	46:7 47:9	164:14	152:3,5
66:13	164:22	65:8	165:22	154:11
157:10	details	106:7	166:13,	165:3
173:20	59:3	132:19	14,17	166:13
190:12	87:20	development	167:7	261:14,17
235:6,9	130:13,	15:13,21	201:22	differentia
description	15,17	18:15	216:18	1
21:9	208:4	21:13,19,	257:12,18	158:14
77:19	209:20	20 26:15	260:3	differentia
148:18	218:12	33:14,22	263:1,11	te
189:12,13	220:4	35:19	devices	169:19
190:19	240:12	36:1,10,	17:19,21	differentia
208:20	detection	14 40:19	24:21	ted
212:9	241:22	44:20	30:20	81:21
descriptors	determine	80:22	32:21	82:1
235:12	31:4 86:8	81:5,11	33:11	differently
design	determined	deviation	35:21	44:4
16:11	227:10	79:19	36:1	112:19,22
37:6 61:2	determines	device	41:19	209:2
87:22	161:18	19:11	89:6	difficult
136:12	188:4	26:10	102:4,6,	47:14
217:16	240:16	28:21	20 103:9	58:17
255:7		29:16,22	118:11	80:3
		30:3,12,	141:4	
			143:16	

105:13	dimensions	directors	distance	13:9,10
147:16	87:13	14:22	114:12	125:11,15
209:14	104:22	disadvantage	188:8	126:9
difficulty	117:17	e	distances	127:3
121:1	dioxide	82:15	188:11	130:20
diffuse	41:12	disagree	distinction	131:6,7
168:3,9	42:2	248:6	96:18	142:14,20
255:19	111:7,15	discern	110:5	149:1
diffused	112:10	141:21	124:6	150:3,5
256:11	113:7	disciplines	235:2	159:20
diffusing	169:17	132:12	distinguish	163:16
190:22	174:22	137:7	35:17	177:4
diffusion	direct	disclose	62:4,10	178:5
41:22	24:14,15	172:17	distinguish	179:3
121:20,21	26:21	228:12	ing	182:17
122:5	27:14,15	232:12	98:8	190:18
145:13	76:18	disclosed	distracting	199:13
149:22	95:16	191:10	60:10	201:13
150:13,15	235:19	208:11	distributio	202:14,16
152:11	directed	213:14	n	211:16,18
156:11,17	38:13	discloses	140:18	212:14
158:5,12	131:19	191:9	143:18	213:18
168:5,10	238:19	discussed	165:1	214:7
171:21	direction	129:5	224:1	218:10,14
172:1	106:10	176:8	245:13	219:4
191:2,11	146:21,22	discussion	distributio	221:11,15
193:11,	147:1,3,4	6:7 69:5	ns	228:16
17,20	155:16	75:20	87:12	229:8
195:2,5	197:16	82:5 83:7	division	231:17
196:7,11	244:15	119:3	17:13	232:15
197:6,13	245:16	128:16	18:9	233:2,21
198:1,2,	directional	213:16	21:15,17	235:4,11
9,20,21	227:4	249:12	26:12,14	248:14
199:2,5	236:12	264:1	34:2	251:7,9
200:10	240:9,10	discussions	35:20	252:1
204:22	directly	27:21	68:13	253:11
207:3	15:15	displays	divisions	259:20
221:19,21	21:4 34:5	10:21	21:19,20	documents
227:11	189:22	dissolve	28:3	126:8
228:14	208:12	100:16	34:10	131:10
243:14,22	director	101:17	document	domain
246:10	14:18,20		12:22	15:12
dilemma	52:10			105:5
55:14				113:15
				173:21
				254:15

Don	225:14	draft	drew	10:3 28:2
16:6		237:1	128:8	
18:12	dose	238:10		earth
	166:21		drifts	146:6
dopant	167:1	drafted	44:16	easier
164:12	225:1,9	237:3,6		63:13
165:1,16,	Doshi	drafting	158:19	146:16
17,20	160:3	238:8,17	159:3	
166:5,12,	161:4,6,9			easily
16 167:7,	162:12	draftsman	driver	63:20
20 168:2	163:2,6	209:21	35:13	245:4
190:20	172:14,17	drain	49:22	250:13,16
217:17	173:13	214:14	driving	easy
220:5	177:2	217:8	16:11	77:6
224:9,15,	178:3,10,	222:3,4	37:2	184:5
22 225:15	21 180:18	225:19		
227:9	183:12	253:17	dry	ECR
255:16	184:8,10,	254:20,22	23:22	215:19
256:9	18,20	255:1,7,	92:12	
	185:9,22	15,22	93:13,15,	edge
dopants	186:4,14,	257:7,19	22 94:17,	141:11
121:14	20 188:22		18 100:22	144:9
166:6	189:6,21	DRAM	101:18	161:19
168:3	190:4,7,	49:5 89:3		179:15
194:7	11	202:2	dual	232:3
217:20	192:17,18	210:18	207:21	234:19,20
227:12	204:18	245:5	duly	235:14
256:3	206:20		5:5 125:5	edges
doped	207:6,10,	draw		147:10
192:10	12,20	207:18	dummy	
216:11,	208:3,11		81:17	educational
17,18,19	209:10	drawing		136:6
217:6,11	210:13	124:6	duplication	
222:3	213:10,13	drawings	250:15	effect
225:19	219:18,19	178:1		139:11,12
256:1	238:21	209:20	E	effective
		drawn		139:3
doping	247:7,11,	166:7	earlier	effectively
162:2,4	15,19,21	171:3	50:15	206:8
168:6,12	248:3,6	178:16	88:12	211:2
190:9	dot	209:1	92:1	
226:17,18	233:19		126:6	efficiency'
255:6	234:17	dream	132:9	s
256:5	235:14	118:13	184:13	76:2
		dreaming	228:18	efficient
dosage	dots	118:9	249:8,11	39:2
167:6	234:3	262:1	early	effort
224:21				

42:7	214:2,6,	elucidation	14:19	environment
efforts	8,18	129:16	24:21	21:14
68:9	215:15	130:9	29:1	32:3 33:3
electric	216:5,14	embodiment	85:14	34:10
111:3	217:15	25:17	168:11,14	35:2
173:10	220:18,20	168:20	222:21	40:18
electrical	226:5,10,	embodiments	223:18	41:16
14:19	11,15,21,	184:11	224:3,5,	66:4
112:13	22 227:8,	emission	20 225:1,	69:22
117:14	15 232:14	242:1	2,3,5,14	94:19
119:14	239:2,12	emphasis	236:5,7,	101:1
137:1	240:22	20:10	8,18	116:13
140:7	243:14,	employer	engaged	environment
162:3	15,17,19	60:19	131:18	s
191:14	electrodes	employers	engineer	34:15
194:17	29:8	18:21	37:15	52:4
electricall	148:8,14	encompassed	44:7 47:4	80:22
y	149:3	122:18	48:11,16	epitaxy
32:11	173:17	encountered	49:7,20	34:17,18
164:17	257:7	80:7	60:2,5,14	35:10
electrode	electron	186:10,13	engineering	equipment
103:14,	95:8	194:18	40:21	10:19
16,20	96:22	end	137:2	16:7
115:12,16	97:1	29:8,21	165:6	17:7,18,
138:4,17	98:18,19,	39:9,21	engineers	20 18:1
140:19	21 99:7	85:16	31:2 45:1	37:5
141:9,10,	121:12	86:15	64:8	38:18
20 144:4	156:12,18	101:8,9	136:17,19	40:2,20
148:12,14	215:19	177:1,3	ensuring	48:11,16
150:1	electronic	257:10	118:22	49:20
155:10,	17:3,6	endpoint	enter	87:21
12,15	electronics	241:22	60:1	97:4
158:18	10:22	ends	87:22	135:20
159:4	109:18	32:9	entered	137:3
161:19	electrons	energetic	66:14	215:18
163:11	95:18	182:22	70:20	equivalent
176:10	98:14	183:6	entering	150:21
179:17	114:9	energies	194:7	era
183:9	157:19	240:17	entire	88:12
184:2	164:21	energy	28:20	errata
186:12	elements	171:4	39:19	125:13,19
189:8	134:1,2		47:20	126:5,14,
194:22	elucidated		240:20	17
196:5				127:14,22

129:1,6,9	107:17	etchback	96:2,14	84:14
249:9,13	144:10	44:1 57:9	97:5,14,	85:8,9,10
error	146:1	107:9,12,	16 98:6	evening
158:20	159:10	13,19	100:22	264:11,13
178:16	176:20	108:1	101:10	eventually
203:12	177:13,22	etched	102:10	241:16
204:16	178:12,22	143:22	138:16,19	evolution
207:6,8	179:7,13	144:8	139:7	17:5
208:14,	180:1,5,	169:7	141:9	evolutionar
15,20	6,21	195:21	144:4,19	y
209:2,5	181:4,9	200:21	145:5	33:15
249:22	182:14	203:17	158:3	46:17
errors	183:16	209:16	161:17	evolve
129:6	189:16	215:2	176:20	46:15
204:17	198:18	233:20	182:8,18,	evolved
209:8	199:19	243:4	19,21,22	17:16
253:4	200:4,6,	etches	200:14	evolving
essential	7,8,13,22	179:22	208:15	20:7
43:13	203:4,5,7	183:5	209:9	EX1009
130:15,16	205:5,8,	196:20	214:12,21	142:6
essentially	16,17,19	241:19	215:5,9,	exact
52:4	206:12,21	244:22	11,16,21,	218:20
86:22	207:15,22	etching	22 221:17	238:4
140:5	209:18	17:11	229:4,7,	examination
150:21	210:12	23:20,21,	9,11	5:5,7
182:9	212:10	22 24:1,2	230:4,8,	125:4,7
187:21	214:5,17,	26:5	20 231:6,	249:5
256:4	19 219:19	37:14	10 232:14	250:22
etch	233:16	40:8 41:8	233:11,	examined
38:17	234:17	42:11	12,16	5:6 125:5
43:19	239:9,14,	43:8 45:2	234:2,5,	examiner
44:14,16	19	47:6 50:7	13,14	12:3
46:2,18	240:11,20	55:18	235:7,9,	examiners
47:22	241:1,7,	57:1	17,18,22	12:12
48:19,20	8,10,11,	58:19	236:4,6,	examples
49:2,15	13,15	62:3,7	8,11,15,	84:14
54:16,19	242:8,9	64:2	19,21	108:1
55:1,2	243:7,13,	92:6,8,9,	240:9,17	262:2
62:12,14,	16,20	12,16,21	241:21,22	excellent
20 63:13	244:4,16	93:6,11,	245:15,	188:1
92:9,10,	245:1	12,13,15,	16,18	
14,15,22	246:5,9	17,18,22	evaporate	
93:3,8,9	etch-stop	94:3,6,8,	85:13	
104:1	186:12	9,12,17,	88:12	
	200:1	18,21	evaporation	
	219:20		25:9	

exception	32:10	explain	extensions	223:2
80:2	46:4	61:20	163:21	224:17
91:19	172:10	97:21		242:18
	174:16	226:19	extent	84:13
exceptions			147:4	factor
91:5 92:3	expected	explained	184:3	167:9
102:3	14:2	7:10	223:8	241:15
109:3,17	203:14,16	208:6	240:12	factors
133:16	experience	explicit		87:5
262:2	21:1	187:3	extraneous	factory
exclusively	22:17	189:10	78:16,20,	20:1 37:3
59:15	49:14	190:2	22 79:5	39:2,3,8
	65:14,21			40:1,2,3
excuse	69:8 74:3	explicitly	F	51:15,18
11:15	83:16	177:5		53:10
201:14	91:6	181:1	FAB	65:8 66:5
exhibit	132:19	189:21	21:10,12,	70:1 72:3
12:21	133:17	190:7	13 22:12	fail
13:1,4	134:6,8,	exploratory	39:14	44:18
125:10,	11,16	22:5	51:20	failed
12,14,16	135:1,11	expose	71:21	32:21
126:1,5,	136:8	214:13	fabricating	128:22
10,14	137:9,11	215:6	163:6	129:2
130:19,21	235:17,19	exposed	253:16	failure
131:2	244:21	68:9	257:12,18	68:12
132:2,4	experiment	137:7	fabrication	fair
142:13,	80:20	204:6	257:6	27:19
15,20	experimenta	exposure	faces	34:6
149:16	l	95:6,7,	82:6	43:10
159:19,21	20:3	15,22	facility	50:8
160:2,5	experimenti	97:15	22:5,6	58:20
163:4	ng	104:1	24:15	64:14
212:13,	80:15	extend	facing	71:13
15,18,20	experiments	171:8	41:9	72:11
228:17	61:2	217:7,14	fact	110:3
232:17	80:17	241:9	20:6	123:4,20
233:6	81:17	246:5	41:16	130:18
248:13,15	136:12	extended	119:8	134:19
249:8	expert	241:10	156:1	152:22
251:3,18	5:20 9:4,	extending	166:8	210:5
253:10,	11,19	239:6	183:11	235:5
12,15,18	11:3	extension	186:10	fairly
exhibits	expertise	165:10,12	222:19	13:14,20
142:9,10,	137:14	166:3,4		22:7 69:1
11 251:12				
existing				

fall	22:14	208:5,17	28:14	6:22
84:19	35:18,19	219:17	29:2	Fish
falls	77:11,14	220:20	32:12	5:22
79:11	109:18	225:21,22	39:6 61:8	Fishkill
familiar	110:15	227:1	84:2	18:11
70:22	111:3	235:1,7,	91:21	21:19
83:11	114:2	10	96:3	22:13
84:5	115:1	figures	112:15	26:15
85:20	116:18	207:7	244:20	52:11
92:5	117:15	208:9,12	261:10	68:16
94:22	118:11,17	209:9	films	69:20
104:12	119:19	210:4	22:15,18,	fit
108:17	134:5	filament	19 23:15	136:16
113:11	213:22	161:13,18	24:11	fix
118:15	216:14	169:16	245:17	44:15
119:4,22	234:19	170:1,5	find	168:8
161:3	field-	178:6	52:17	flat
familiarity	effect	181:11	53:1 67:9	102:14,
137:3	115:20	189:19	80:3	16,17
fascinating	fields	194:2	147:16	103:5
264:1,10	112:9	198:8,11	150:4	189:17
fashion	figure	199:1	160:12,13	flavors
227:5	42:7	207:13,16	177:5	25:6
faster	66:20	filaments	189:5,6	flexibility
107:17,18	105:8	161:4,7,9	208:14	37:4
244:14	148:2	168:21	245:4	56:15
fault	164:3	169:3,11	253:8	258:21
56:19	165:21	176:4,8	finding	flow
feature	170:4,6	179:10	92:2	17:9 18:2
25:12	177:11	189:13,	fine	20:1 30:3
features	178:5,9	14,18	74:3	39:2,8,13
141:18	179:20	190:6	141:8	43:14
feel	182:4	193:9	251:20	49:18
47:19	183:19,22	filed	finish	51:15,18
130:4	189:21	7:4	19:8	55:3 66:6
feeling	195:11,	filing	50:20	71:1,4,9,
76:21	13,15,19,	249:18,21	70:12	10,12,18,
fewer	20 196:2	fill	233:1	22 72:5,
235:18	201:2,14,	198:17	finished	7,8,12,
field	19 203:6,	fills	102:8	13,15
15:10	8,12,18,	206:13	finite	73:9,11,
	20 204:2,	film	187:15	15 77:16,
	18 205:4	23:4,8	firm	17,19
	206:20			
	207:1			

78:7 79:2	62:16	248:4	214:9	fourth
80:9	64:18	252:14	217:8,13,	49:22
81:7,22	68:7	254:17	19 218:5	66:8,18
82:21	71:15	255:11	219:2	67:1,4,5
87:12	72:9	256:3,12	220:19	68:16
91:3	78:8,17	257:14	256:17	235:8,13
115:9	80:12	260:5,13		259:12
flows	81:9	formal	forming	
88:1	83:21	70:15	131:3	frame
flux	85:6	formation	133:11	18:5
167:8	95:16	23:2	138:3,11	69:11
focus	99:15	96:12,13	145:13	164:20
36:1	107:2	159:9	149:21	215:10,16
184:17	109:5	176:14	150:2,13,	frankly
focused	111:22	191:15,16	14 176:3	14:4
42:15	114:17	192:18	199:15	freedom
231:20	115:5,13	194:21	210:18	35:21
focusing	117:6	197:12	247:12	full
218:13	118:2	199:10,11	258:14,15	8:9 52:6
follow	119:15,19	202:6	259:13	70:16
152:1	120:20	207:14	forms	full-
196:18	122:13	210:14	179:14	fledged
238:14	123:7	211:1,3,	182:10	29:9
force	124:2	12,13,22	183:14	function
68:15	126:21	212:4	187:7	115:21
forecasters	127:15	213:20	200:10	118:22
41:14	129:13	214:1	229:6,8,	124:7
forefront	133:4	216:4	22	155:4
23:18	135:2	219:1,8	formulation	156:20,21
form	139:19	221:22	138:4	157:9,13
9:13	147:15	245:17	found	162:4,5
15:18	161:17	formed	28:15	164:11,12
27:2 32:8	163:10	23:6	32:5	166:7
34:7	172:19	112:19	160:16	176:17
37:10	173:16	115:11,16	180:14	177:8
43:11	176:4	133:22	183:12	190:8,9,
45:4,12,	184:21	139:15,22	184:15	19 191:4,
17 52:8	185:1,12	168:21	189:10	6,9,10
55:21	186:22	169:3	190:2	193:9
58:22	199:15	171:6,20	203:11	194:16
60:7	209:11,16	172:12	Foundation	195:1,2,5
61:15	210:6	185:10	38:14	198:7
	212:6,8	186:21	founding	219:15
	213:20	189:15	14:20	225:20
	214:6,17	198:16,18		
	216:17			
	222:4			

functional	249:9	186:12	45:10	give
110:2		189:8	67:22	30:17
	gas	194:8,22	72:22	35:9 38:8
functionali	55:3	196:5	73:5	41:5,19
ty	87:12	197:21	74:8,15	52:22
155:19	88:1 91:3	199:1	77:11	67:14
	214:19	214:2,6,	82:7	76:9
functionall	240:14	8,11,15,	114:20	120:18
y		18 215:14	115:17	121:7
169:20	gas-phase	216:4,13,	118:5,20,	132:14
	174:1,13	15 217:15	21 120:15	157:12
functioning		220:18,20	149:5	211:15
197:22	gases	221:1	156:9,14	250:12
	83:21	226:5,10,	234:9	261:6
functions	84:1	11,14,21	260:8	
114:15	87:13	227:8,14		giving
115:15		231:10,22	generalizat	59:2
116:20	gate	232:2,3,	ion	67:13
123:9	103:14,	14	118:10	121:1
124:4	16,19	233:14,19	generally	158:2
155:13	115:12,16	234:8,9,	10:9,17	global
156:5	138:4,17	10,18,20	36:21	82:16
157:6,22	140:19	235:14	54:18	
161:13	141:4,7,	239:1,12	63:22	goal
190:13	9,10,15,	240:7,22	97:8	37:19
191:8,13	20 143:9,	243:14,	109:20	70:1
	22 144:3,	15,17,18	114:1,4	254:21,22
fundamental	4,5,7,11,		116:17	goals
87:5	13,19	Gaussian	118:16	36:18,20
	145:5,7	224:2	122:1	37:7
fundamental	148:7,11,	gave	259:22	38:2,3,7
ly	13,14	21:8		39:10,16
209:3	149:2	35:15	generation	67:22
furnace	150:1	63:10	23:9	
32:20	155:10,	80:6	43:14	good
	12,15	120:14	46:16	5:9 6:19,
	159:4	123:2	67:7	20 32:20
G	161:19	244:13	106:6	41:5
	163:10,	246:1		50:10
G-a-r-y	18,20		generic	64:6 87:9
8:10	166:3	Gee	113:22	88:4,22
	170:10	221:11	generically	102:18
gallium	176:10		242:11	103:6
23:14	179:10,16	general		105:17
30:20	181:18,	9:20	Gentlemen	108:15
31:6,7,12	20,22	36:17,20	263:22	111:2,18
Gary	182:7,13,	37:7 38:2	geometry	129:17
5:4 8:10	15 183:8	39:10,16	87:12	
32:17	184:2			
125:3				

136:3	16:15	89:21	head	31:1
146:20	43:5		30:1	heritage
191:14		hand		
193:10	grown	56:2 87:4	heads	46:11
194:3	141:5	137:1	16:17	hesitate
198:9,19,	grows	hands	heal	100:17
21 205:7	175:16	30:1	141:14	hesitation
206:13,16	growth	happen	hear	34:11
221:21	25:9	32:1	7:14	
264:13	28:16	34:21	18:14	hierarchal
grade	113:7	55:2	59:2	42:18
68:4,22	172:5	67:15	111:18	45:19
69:1		92:3,19		hierarchy
	Grumman	122:14	heard	39:15
graduate	30:19	140:15	51:5	44:5,22
59:11	31:3	144:6	hearing	45:10,15
60:12	guess	178:17	12:2	66:13
69:8	12:16	193:7		
70:4,5,14	14:16	227:12	heart	high
graduated	16:21		141:3	24:9
60:6 69:9	18:4	happened	heat	28:13
graduates	19:16	32:7	85:10	31:21
59:22	22:20	69:13	166:19	41:21
grain	30:17	happening	167:21	87:2 99:5
91:22	40:15	20:15	168:1,4	110:16
139:6	65:11	58:16	256:12	111:3
gratifying	70:13	59:8		117:16
33:8	78:18	78:21	heated	120:15
	80:2	82:7	55:10	121:8
great	111:17	159:11	heating	193:5
169:22	131:17		55:9	215:20
238:15	154:16	hard		245:9,12
greater	161:1	14:4,11	heavily	255:8
188:7	199:14	21:21	256:1	
222:20	208:18	34:8 49:9	helpful	high-
group	237:15	52:9	113:20	aspect-
5:18 6:22	238:16	61:10	117:8	ratio
26:10	254:2	117:17	149:13	89:5
31:2		133:16		high-
42:9,11,	guys	144:13	helping	density
12,13,14	56:17	148:19	18:13	28:12
70:8 87:2	108:6	164:21	helps	higher
143:3	162:18	169:19	77:3	41:18
		238:14	199:7	67:20
groups		254:13	HEMT	93:9
	H	262:13	30:20,21	105:2
	half			147:3

151:11	107:16	15	182:9	226:15,16
152:15	hope	hundreds	identificat	227:1,12
168:5	13:5	182:20	ion	implantatio
224:20	horizon	236:4,17	13:1	n
234:5,6	39:3,7	hungry	125:12,16	143:7
highest	horizontal	108:5	130:21	155:4,6
141:7	86:18	hurting	142:15	161:20
highlight	87:1	37:2	159:21	166:19
140:21	89:15,22	hurts	212:15	168:11,14
highlighted	92:10,15	231:11	248:15	176:9
195:3	93:1,8,20	hypothetica	253:12	216:6,10
highly	106:10	l	identified	222:16,
29:6	146:22	79:7	41:16	19,21
180:4,6	239:15	80:6,8	identify	223:4,11
181:4,9	240:6	242:21	178:15	224:8,14,
182:19	241:6,14		ILD	20 225:13
hired	243:21		176:21	227:14
60:20	244:6	I	illustrated	228:2
	245:1		179:20	229:10,
hit	hour	IBM	illustrates	14,20
35:12	8:16,17	16:3,6,8	177:11	230:13,19
100:7	50:17	18:11,12	image	231:1,8,
264:2,4	162:18	19:7	100:4	19 232:1,
hits	228:6	21:16	imagine	2 255:5
100:6	hours	22:22	79:6,7	implanted
hold	237:7	25:8,21	250:7,13,	155:14,21
170:15	264:2,4	26:14,15	16 255:21	156:3
232:20	housekeepin	28:2	impact	167:2
holder	g	34:10,12	33:20	217:21
11:10,15	251:11	40:18	183:6	222:12
12:19	HSC'S	41:8	impart	implanting
hole	75:19	52:10	236:7	155:8
131:3	76:14	66:1	imparts	implants
158:13	huge	68:10,12	236:4	163:19
159:5,12	35:11	69:18	impinging	164:9
178:8	41:9 42:6	70:7,16	245:13	176:4
Holt	244:16	105:6	implant	222:4
5:22	hundred	idea	223:7	225:19
Home	40:17	50:10,14	224:1,5	implemented
5:19,20	241:14,16	79:1 80:8	166:22	72:2
7:1,4	244:14	132:14	216:16	implication
homogenizes	245:8,10	identical		49:1
	246:2,9,	177:6		

implication	168:15	37:1	influences	220:7,17,
s	216:6	indicating	183:8	22 221:8,
23:6	222:11	151:11,	informal	10,17
26:19	256:10	15,19	12:2	222:1
27:11	impurity	152:14	information	225:20
implied	224:21	Indirectly	73:1	226:2,20
179:4	225:14	25:2	77:11	227:17
implies	incidental	individual	250:3,5,6	insulation
177:9,15	y	38:16	infringemen	108:20
imply	42:21	39:16	t	109:5,11
177:18	include	40:3,5,13	11:13,16	110:1,6,
importance	46:9 51:4	43:5	initial	7,21
78:14	52:6	44:22	60:15	111:12
important	56:22	45:15	61:13	insulator
78:7,11,	118:9	46:1 47:8	175:19	41:12
13 79:17	122:9	48:1	244:19	42:2
87:16	128:15,22	87:16	initially	106:9
99:6	129:3,21	individuals	66:16	121:9
134:3,21	130:2	21:3	116:16	141:8
135:4,11	146:8	Indranil	160:13	158:17
193:8	included	5:21	insert	191:14
197:10	22:3 23:9	Induced	78:2	192:4
255:2	25:8	142:21	insight	insulators
importantly	127:13,21	Inductively	61:4	109:19
49:13	128:12,14	215:18	132:16	111:16,17
161:15	130:12,16	industry	insoluble	112:8,9
impressed	132:18	20:9	100:11,12	169:18,20
69:10	142:5	23:13	institute	188:1
improper	155:19	36:3	31:4	intact
76:18	156:6	65:15,18	38:13	242:17,
improve	252:13	69:10	241:20	19,20
79:1 81:6	253:1	132:14,20	instruction	integrated
164:13	includes	134:8,16,	75:15,18	34:9 35:2
improvement	51:11	22 135:11	insulating	39:5
39:12	including	136:1	109:14	51:22
257:6	41:22	137:9	110:2	52:5
improving	55:18,19	inferior	112:4	67:16
37:19	240:21	111:9	121:11	163:7
47:8 63:5	inconvenien	infinite	158:4	177:12
impurities	t	205:11	187:22	integrates
167:2,16	146:3	influence	214:11	42:18
increasing	increasing	139:5	219:10,13	integrating
				64:17
				66:17

integration	19:22	24:11	251:18	117:13
17:8,9	25:20			139:6
19:11	interchange	interfere	introducing	143:7
25:5,18	able	222:15	6:15	155:4,6
26:11,17,	111:21	interferome	introductio	161:20
22 27:9,	112:13	try	n	166:22
16 28:8,		261:11	16:21	167:8
20 29:10,	interchange	interlayer	257:20	216:16
14 34:16	ably	176:21	introductio	223:18
37:4,16	96:5	191:17	ns	227:1
49:7,21	108:22	192:4	5:12	229:9,14,
66:5,6	109:11,21			19
80:15	interconnec	internal	invalidates	230:13,18
115:9	t	139:4	254:13	231:1,8,
132:11,	41:10,11	internation	invention	19 232:2
17,22	46:21	al	168:21	236:5
134:16	49:4 71:8	36:5	179:7	240:17
135:5	105:5	interpret	184:14	245:19
136:17,	interconnec	152:10	247:7,11,	255:5
19,22	tion	172:21	21	ion-
137:13,20	106:4	211:18	involve	selective
Intel	interdiscip	interpretat	40:16,19	115:20
48:9	linary	ion	60:20	ions
65:7,22	67:16	150:12	61:1,3,6	84:18
69:16	interested	152:9	84:12	85:5
intended	17:2 18:6	156:2,14	involved	98:13,14
128:15	25:13	180:18	20:9 21:4	107:13
169:22	26:8	interrupt	42:9	114:8
intent	28:11	5:11	94:20	121:20
242:14	30:20	70:11	165:8	155:8
interact	36:22	264:1	235:21	157:18
21:13	211:9	interrupted	240:15	183:6
65:17	218:8	56:20	245:15	223:7
interacting	interesting	intimately	258:3	232:3
19:11	16:14	157:18	involves	236:9,17
26:1	30:18		132:10	240:15
	103:13	introduce	involving	245:14
interaction	158:9	6:13	137:12	IP
26:10	interface	74:16		10:9
33:20	23:3	131:11	ion	IPR
38:16	31:21	142:20	25:11	12:8,14
61:7	122:13	introduced	95:8 97:1	74:18
interaction	interfaces	18:16	98:18	126:2,12
s	17:6,10	228:18	99:3,4	127:20
18:10			107:10	128:4

131:19	211:10	junctions	135:6	61:7
143:1	238:22	255:12	143:19	labeled
152:8	242:22	junior	147:17	170:6,9,
160:6	261:17	135:18	172:21	14
161:1	issues		188:9	laboratory
212:22	17:21		190:3	25:7
213:9	56:2	K	196:11	lack
251:4	80:15		213:12,13	53:18
252:4,9,	126:19	key	224:2	ladder
12	127:12,20	68:9	238:21	43:15
IPRS	129:5	kind	246:11	66:17
7:3 9:8	237:5	10:20	kinds	Lam
237:14	250:8,9	14:11	16:10	48:19
254:5	252:9,12	17:1,6	17:18,19	63:3
Iqbal		24:2 25:7	19:10	laminate
70:7	J	26:19	25:8	261:8,9
irrelevant	Jerry	27:11	39:16	laminating
188:10	5:17 6:21	29:6 32:3	44:2 53:7	261:16
197:3	job	35:9	81:18	large
236:22	48:10,18	36:21	83:22	11:12
ISFET	49:6	41:14	184:12	41:18
115:19	59:12	42:4,13,	223:2	88:5
isolation	60:1,9,	19 43:15	kinetic	182:20
26:4 49:5	13,15,19	45:19	87:19	largely
89:4	61:11	46:2	236:7	14:13
103:20	105:17	48:18	kinetics	23:11
119:5,7,	130:8	49:21	87:8	36:10
14,15,17,	132:20	51:15	knew	111:21
19 163:8	jobs	52:13	26:7 79:4	larger
213:20	69:20	63:18	160:16	37:19
isotropic	joined	68:4,17	186:15	38:3 70:1
37:14	17:12	69:5,21	knowing	158:13
93:17,18	165:9	70:13	250:13	159:11
94:1,13	journal	80:19	knowledge	187:12,13
241:1,8	16:4	82:5,16	74:7	208:2
243:9	jump	88:11	L	late
issue	85:13	92:12		10:3
7:6 28:20	junction	95:12	lab	28:11
49:11	254:18,19	96:2,9	22:10	lateral
53:6 73:6	255:4	107:10	26:13,20	155:16
76:1,22	256:12	110:18	27:12	197:15,16
118:8		112:15	35:15	
187:6		113:21		
196:17		118:9		
		121:1		
		122:15		

lattice	156:21,22	221:1,8,	leak	11,21
223:10	158:4	10,17,18	121:10	180:20
Laugh	169:4,10	222:1,2	leakage	186:5
13:7	171:6,8,	223:12,17	110:11,13	242:6,17
213:7	20 172:6,	224:7,12,	112:10	244:3,7
253:9	15 173:6,	13 225:7,	117:14	legacy
254:3	15	20 226:2,	leaky	88:11
Law	174:20,21	6,20	111:4	legal
5:18 6:22	175:3,6	227:17	leap	238:13
layer	176:14,	238:22	85:15	legitimate
23:17	18,19,20,	239:10,11	learn	89:12
25:14,16	21	240:21	81:13	lesser
29:7	177:14,20	242:5,13,	learned	240:8
30:22	178:4	22 243:8,	66:3	level
31:13	179:8	13,16	69:11	33:20
91:15,16	180:1,20	259:13,14	leave	42:10
97:11	182:15	layers	79:3	44:22
99:21	184:1,21	31:9 42:1	99:22	45:6,14
100:1	185:10	104:20	121:15	46:18,19
104:3	186:21	187:22	139:1	49:21,22
106:9	187:9,18	214:10,12	159:5	52:2 61:3
108:18,20	188:4,20	215:1,6,7	204:13	64:5
109:5,10,	189:7,20	223:2	221:18	66:9,16,
11 110:6,	190:12,13	263:6	239:11,15	18,19
7,20,22	191:9,12,	lays	243:16	67:1,2,4,
111:11,13	16 192:7,	257:22	leaving	21 68:15,
120:1,2,	9,15	258:2	189:18	16 88:17
5,6,13	193:1,4,	LCD	208:4	104:7
121:4,8,	15,22	10:21	220:1	106:7
11,16	194:21	11:12	lecture	120:15
122:2,4,	195:22	LCDS	29:13	132:12
15 123:4	196:4	11:1	led	134:20
137:16	197:12,20	LE	33:5	135:18
138:3,15	198:14	11:12	67:18	136:6
139:15,	199:5,10,	lead	68:15	144:5
16,17,19,	19,20	245:17	88:3	levels
22 140:2,	200:1,7,	leader	left	41:10
3,5,12	8,14,21,	41:2	86:14	43:16
141:6	22 201:22	leaders	138:19	46:5 50:2
144:17,22	204:5,9	42:6	165:22	67:18,20
145:13	205:1,3	leads	177:22	106:4
146:1	208:15	32:11	178:4,7,	leveraged
149:21	209:9	76:4		37:3
150:2,13,	214:11			
15	219:10,			
	13,15,20			
	220:12,17			

liaison	44:15	102:1,19	long-winded	244:18
68:13		103:7,22	20:6	
	liquid	104:3,5		lower
lie	94:9,19	105:11,20	longer	67:18
39:10	101:17	106:1	21:8	88:14,17
		138:16	24:19	168:9
life	list	159:2	168:4	233:11
53:8	16:3		237:19	234:13
	132:13	localize	241:11	236:8,9
light	258:2,7	158:13		
95:7,16	260:11		looked	lowered
97:10		location	31:22	206:7
98:10,17	listed	189:6	127:5	
99:3,5,6,	259:10,19	202:3	141:14	lowest
10,17		232:5	160:17	45:14
100:2,4,	listen		212:9	
5,9	29:13	locations	221:11	lunch
163:19	lists	98:12	237:7	108:13
164:9	258:9	179:20		124:10
		180:2	lose	luncheon
lighting	literature	202:7	204:12	124:12
97:16	140:16	214:13	224:3	
	141:14		225:6	
lightly		logic		M
222:3	lith	17:15	loss	
225:19	97:15		223:18	M-o-s
		logistics		31:17
limit	litho	20:1	lost	
74:18	43:18	51:19	83:2,6,9	Madam
			135:8	264:4
limitation	lithographi	long	218:15	
258:12,17	c	9:11,18		made
259:11,13	97:9	14:2	lot	12:13
	159:11	58:15	26:10	27:7 28:5
limitations		79:14	42:19	39:22
259:2,10,	lithography	86:13	77:5	96:3
18	24:5,8,	130:11	117:17	110:20
	10,17,20,	145:5	120:12	111:7
limited	22 43:10	168:7	164:6	112:10,21
87:8,10	45:3 46:3	177:16	184:18	113:10
168:8,10	47:7	179:2	195:4	127:2
259:11	58:20	184:10	212:11	138:15
	64:2 78:1	186:8	236:6	161:13
limits	94:22	218:21	250:14	173:20
104:11	95:3,4,	228:4		182:12
	11,14,20	243:22	lots	187:21
linear	96:9,11	244:16	24:20	189:14
172:5	97:17	246:6		192:5
	98:2,3,4,	248:10	low	194:13
lines	19 99:7,	250:19	34:17	209:20,21
163:22	9,17		42:3	
189:11				
linked				

217:16	137:13	29:16	14,16,20	mark
magnifying	139:1	32:10	16:12,20	13:4
96:21	141:9	36:12	17:4,17	125:13
main	143:15,19	51:7	18:7	126:1,5
115:18	146:10	62:18	19:14,20	131:2
maintain	148:20	71:21	20:7	160:1
56:14	153:7	89:6	21:4,6,	212:18
major	155:14	103:2	12,20	251:3
25:12	156:19	111:18	22:10	253:15
50:2 72:3	157:2	184:16	25:1	marked
make	158:11,	204:14	26:9,16	12:22
17:19,20	14,19	Maltiel	29:22	125:11,15
22:10	159:12	5:20	30:14	130:20
26:3	165:6	management	32:15	142:14
28:13,16	166:18	19:19,20	33:10	159:20
29:8 32:5	172:7	21:22	34:5,11	164:10
33:16	186:14	22:3 41:2	35:4,12	212:14
34:21	205:20	49:22	36:18	248:14
37:16	206:4,7,	67:21	37:20	249:8,11
39:12	16	69:4	39:20	253:11
46:12	207:13,15	manager	40:20	marrow
47:15	209:22	17:13	43:4	264:3
56:6	216:12	42:11	44:21	Maryland
67:14	219:22	66:9,19	45:11	14:21
71:6	223:5	67:4	46:8	23:15
75:11	233:14	68:15,16	47:21	38:11
76:13	236:2	manner	51:14	mask
84:19	242:16	163:20	68:12	95:9,10,
88:8 92:2	244:17	manufactura	71:1 74:8	15 96:12,
96:17,20	246:11	bility	77:12,18	14 97:10,
97:4 98:9	248:1	17:21	78:5	11,14
99:8	251:7,21	manufacture	80:14,22	99:9
100:3	260:17	30:12	81:12,14	100:3,4
102:6,19	261:13	31:15	99:2,8	101:1,3,6
103:9,13,	263:18	46:10	112:17	102:10,11
14,19,21	makes	51:3	114:3	107:19
104:4,20	111:8	manufacture	115:2	134:3
105:9,12	149:3	d	116:19	140:5
106:2	165:2	260:4,12	118:17	159:5
110:18	166:13	263:1,11	133:4	204:7
113:8,21	181:1	manufacturi	262:7,8	226:15,16
117:15	183:12	ng	margin	232:2
118:7	261:17	15:10,13,	158:20	masking
130:10	making		marginally	140:6
	16:9		155:22	
	28:12,21			

masks	216:15	48:19	78:14	204:21
96:20	221:18	95:19	90:17	247:14
107:21	224:19	114:11	143:14	248:2
159:2	225:11,12	124:7,8	241:22	
	241:12	145:17		mentions
master's	242:6,16	146:5	measured	234:2
48:16	243:17,18	148:19	90:11	
49:12,15	244:7	149:8,9	91:14	merge
59:19	246:6	151:5,6		95:12
132:12	256:7	152:5	measurement	mess
134:5		153:2	s	111:19
135:13	materials	159:14	54:16	
136:5,7,	17:2,3,7	231:22	measuring	metal
21	18:14		61:1 90:9	23:2,3,4
	39:6	meanings	157:10	41:10
matches	52:11	95:12		121:8,9
130:7	63:2 66:1	123:6	mechanical	122:11
	83:20,22	124:1	104:13,15	257:6
material	106:14	149:6	192:12	
25:14,16	109:4,19		mechanism	metal-
42:4 63:7	110:10	means	183:5	oxide-
76:15	112:17	71:10		semiconduct
84:2,18	137:3	78:3	mechanisms	or
85:11,13	183:1	89:2,7,20	31:22	23:10
86:5,8,16	223:19	100:19		metallic
91:21	224:17	110:7,11	meet	109:17
94:11,18		113:22	263:14	
95:8,9,	math	124:8	meets	method
17,20	246:14	130:14	204:9	131:3
96:3,16		145:19		149:20
99:21	matter	173:22	member	173:5
100:21	7:6 10:16	174:2	22:2	253:16
101:2,4	13:20	180:9		
106:17,	53:14	206:11,18	members	methods
20,22	99:1	236:15	43:5	215:3,9
107:14	134:20	241:6	memory	216:1
110:1,8,	183:2		17:15	
13,17,18	194:8	meant	238:3	metric
111:2,9,	224:11	27:14		78:14
14,18	251:11	67:4	mention	112:1
112:5		76:12	16:2 40:5	263:3
122:13	matters	83:9	177:20	
158:21	8:13 9:4,	113:1	203:11	metrology
174:10,	7,9 10:7,	115:3,7		20:10
12,16	8 11:3	151:1	mentioned	54:15
188:7	53:16	238:17	18:12	
195:6			38:3 47:4	Meyerson
206:13	meaning	measure	66:8,14,	34:19
	47:18	34:9	16,18	35:11
			157:6	micro-

88:6	250:20	moments	122:2,19,	118:2
microfluidi	missing	126:7	21 145:9	120:20
cs	136:21	monoxide	147:9	123:7,12,
102:6	mission	32:9	158:1	15 124:2
mid-'90s	36:14,15,	months	192:17	125:17,19
38:10	16 37:19	131:17	248:16	126:21
middle	mistake	186:7	Mukerji	127:15
141:20	244:17	213:5	5:10,14,	128:1
mil	246:12	237:15,	21 6:14,	129:13
233:19	mistakenly	18,20	17 9:13	135:2
234:3,17	249:17	254:3	15:18	147:15
235:14	MOCVD	morning	18:17	162:19
mind	31:6	5:9 6:19,	19:2	172:19
44:11	model	20 76:11	27:2,17	185:1,12
50:17	38:16	126:6	34:7	186:22
112:2	modeling	MOS	37:10	188:12
149:12	20:1	23:10	43:11	209:11
176:2	164:20	31:16	45:4,12,	210:6
259:8	models	35:16	17 50:16	228:5,9
mine	38:18	37:14	52:8 54:1	248:4,16,
42:14	39:5	253:16	55:21	19,22
minimal	modificatio	motivation	56:16	249:3,6
179:15	n	255:3	58:22	250:21
260:17	54:12	move	60:7,17	251:10,
minimized	83:20	16:12	61:15	16,20
179:11	modified	36:7	62:16	252:14
minor	183:17	38:20	64:18	257:14
178:16	modifies	67:10	68:7	260:5,13
minute	100:12	72:18	71:15	261:1
86:4	modify	101:18	72:9,17	262:9
153:12	81:6 95:9	107:14	73:2,8,	263:22
211:15	modifying	153:4	17,21	264:12
232:21	136:10	202:18	74:9,19	multiple
264:6	module	259:6	75:1,8,	47:22
minutes	43:18	moved	11,14,17	52:6
108:5,12	46:2,19	19:18	77:6	64:17
228:6	moment	20:2	78:8,17	117:21
248:11	13:8	moving	80:12	137:12
misleading	131:5	28:22	81:9	191:13
203:14	251:6	45:14	107:2	
missed		74:4	108:7,9,	N
		120:7,14	11 109:7	
		121:5	111:22	
			114:17	n+
			115:5,13	193:13,16
			117:6	204:11,12

205:7	101:13	183:5,6,	11,15,16,	novelty
N2o	144:8	13,17	17,18,19,	254:10
113:8	145:20	184:1,21	20 240:20	NPN
174:1	258:5	185:10	241:2	216:12
nano-	needed	186:11,21	242:2,5,	nucleation-
geometries	11:22	187:9	6,13,14,	controlled
88:7	16:11	188:20	22 243:7,	28:16
Nanocenter	46:9	189:7,14,	13,16,18	92:1
14:21	116:21	15,16,17,	244:3,5,	number
24:14	198:7	20	7,20	15:5
nanometer	237:11	190:12,20	nitrous	21:22
188:9	246:15	191:2,13,	113:8	28:19
nanometers	250:11	16	nominally	31:11
30:22	negative	193:10,	176:19	32:14
86:3	100:17	15,19,22	North	38:19
187:22	nice	194:5,16,	38:10	40:17
nanoport	19:12	21 195:6	Northrup	82:2
29:8	20:18	196:4,20,	30:19	109:19
nanostructu	256:4	21 197:6,	31:3	138:14
res	niche	12,20	notably	139:10
14:19	20:3	198:15,19	235:16	140:14
23:19	nitride	199:4,20	note	160:2,16
narrow	23:14	200:1,4,	6:5 14:16	166:18,
89:7	30:20	6,7,8,22	noted	19,21
national	31:6,7,12	201:16	138:13	187:15
36:3	111:12,	203:4,5,	notes	188:10
38:13	15,20	7,17,22	248:10	205:11
nationally	113:3	204:5,9,	notice	212:18
29:4	121:16	11,14	217:14	227:6
nature	145:22	205:6,9,	noticed	253:15
47:7	169:6,18	11,17	32:19	numbers
NC	171:8,11	206:21	189:1	38:21,22
69:15	177:20,22	207:14,22	195:4	93:5
179:20	178:4,7,	208:15	notion	211:18
183:3	11,21	209:9,16	26:17	<hr/>
201:17	179:8,13,	214:11	27:9	O
necessarily	16,22	219:14,21	73:11	<hr/>
61:16	180:1,10,	220:2	208:19	O2
68:8	20 181:5,	221:18,21	Novellus	173:22
93:14	7,13,17	222:13,	63:3	object
97:5,6	182:2,6,	14,15,20	69:16	76:17
	12,14	223:1,2,		147:7,9,
		12,13,17		10,12,13,
		224:4,6,		14 151:9,
		13 227:6		
		238:22		
		239:10,		

10,11,12,	252:14	off-track	opinion	optimize
14,15,16,	257:14	197:8	205:16	51:19
18,19,20	260:5,13	offer	211:11	61:2
objection	262:9	49:20	212:3	136:12
9:13	objections	offhand	239:8,12	order
15:18	261:1	11:4	243:6	71:13,19
27:2,17	objectives	Office	258:6	72:6
34:7	37:8	12:1,12	259:9	73:6,10,
37:10	objects	old-	262:20	12,15
43:11	7:10	fashioned	263:8,13	133:6,9,
45:4,12,	152:19	67:12	opinions	10 136:3
17 52:8	obligations	omissions	126:18	182:13
55:21	18:20	129:7	127:11,19	187:9
58:22	observation	253:5	128:11,18	188:5,8
60:7,17	137:6	open	129:10,18	205:7
61:15	197:4	55:12	211:22	238:13
62:16	observed	210:19	212:6	244:18
64:18	179:6,21	opening	252:8,11,	245:10
68:7	180:4	158:3	22	246:3
71:15	obstacle	199:15	opportunity	258:11
72:9	82:6	200:15	12:11	259:11,19
78:8,17	obtains	201:16	opposed	260:1,16,
80:12	134:21	204:7	84:15	19,22
81:9	occasional	211:13,14	98:13,14	262:6,21
107:2	80:1	212:1,5	113:3	263:10,21
109:7	occasionally	openings	173:15	orders
111:22	21:14	97:13	174:5	263:15
114:17	occur	192:19	210:4	ordinary
115:5,13	115:18	195:21	223:13	49:10
117:6	143:21	199:12	optical	132:7
118:2	occurred	200:20	98:3,5	134:12,21
120:20	231:16	201:5,11	99:9	172:20
123:7	232:7	203:8	100:4	181:2,12
124:2	occurring	210:13,	104:3	182:11
126:21	232:8	15,19	137:16	183:15
127:15	occurs	211:2,3	242:1	184:5
128:1	145:4	212:7,8	261:10	186:16
129:13	off-line	operate	optics	190:4
135:2	80:19	119:10	95:17	196:3
147:15		operating	96:22	208:22
172:19		72:1 82:3	97:1	210:9
185:1,12			optimizatio	246:12
186:22			n	258:22
209:11			39:8	org
210:6				65:6
248:4				

organizatio	139:12,19	7,10	206:9,12	223:11,13
n	140:19	174:6,9		224:7,14
14:1,6	141:12	175:16		239:19
18:13	143:5,12	192:7,9	P	240:3
38:7	150:1	194:3,8		
45:20	161:14	198:8,12	p+	parse
67:9,10	170:19,22	201:22	166:2,8	29:19
	171:19	204:22		
organizing	172:12,	205:3,6,	p-region	part
41:3 50:1	18,22	9,13,18,	217:11	26:12
		22 206:5,		34:11,16
oriented	173:5,10,	6,10,16,	p-regions	81:5
36:14	15,16	22 207:2,	217:6	87:17
	174:15,21	3 213:22	219:9	95:22
original	175:7	216:14		97:16
129:22	176:2	229:19	pages	100:6,7,
158:9	207:12	230:12,22	130:11	14 106:6
175:4,6	228:13	231:11,22		127:16
221:2	229:3,12,	232:4	paid	137:10
	18 230:3,	234:19,21	128:3	147:22
originally	7,11,17,	235:14	paper	164:15
172:13	21 231:5,	257:6	16:18	165:13,15
outlier	12,21		paradigm	169:10,13
143:17			43:13	174:21
				179:13
over-etch	oxide	Oxides	paragraph	200:18
241:15	32:12	142:21	132:3	202:2
244:1,16	109:16		137:21	203:22
	110:21	oxidize	138:2,7	204:2,13
overlapping	111:15,21	173:6,8	145:9	207:13
146:9	113:3,8	175:12	148:6	208:2
147:4,5	119:19	oxidized	150:10	211:6
	121:17	79:16	153:4	218:7,8,
overlying	138:3,12	169:9,17	158:1,2	18 220:3
190:21	139:15,	170:12	177:19	226:15
	16,17,19,	171:6,11,	179:5	231:19,20
overstateme	22 140:1,	14	180:19	237:5
nt	2,3,12	oxidizing	200:13	245:16
	141:4,7,	139:7	249:15,	247:13
overview	11,15,20	169:4	17,18,21	256:19,20
137:22	143:6,10,	172:7,11,	250:5	258:9
	22 144:5,	14,21	257:8	
owned	7,14,19	173:14,22		
11:20	145:5,6,	174:2	paragraphs	particle
	8,13		250:15	95:16
owner	149:21	oxygen		
	150:13,14	33:3	parameter	partly
oxidation	171:20	113:7	161:21	90:2
23:11	172:4,5,	174:6	parameters	161:14
29:3				
138:21				

partnered	134:13	212:21	penetrate	87:4
26:14	137:22		168:17	
	145:15	pattern	223:17	perform
partnership	149:10,15	96:2,15	227:6,7	139:18
21:18	150:22	97:7 98:9		174:21
partnership	152:4,18	99:18	penetration	176:1
s	153:1,7,	104:1	222:22	260:10
18:11	10 159:16	259:14	people	performance
parts	160:2,6,	patterned	11:22	31:1
97:13	10,14	95:15	15:12	37:1,20
218:13	162:7	96:12,14	18:11	60:21
	177:7	199:15	19:10	63:6
Pass	184:10	215:2	21:14	136:13
250:21	185:14,17		25:21,22	143:16,18
passing	186:8	patterning	26:9,11	164:14,21
110:9	187:2	102:1,19	28:3,11	165:3
	200:19	103:7	32:4	166:14
past	208:3,8	214:12	33:14,21	167:9
123:13	211:8	215:5	36:7,9,10	255:8
228:6	212:18,22	patterns	40:17,21	
244:4	217:1,5	88:7	41:13	performed
patches	218:9	95:6,7,	42:5,9	163:20
205:21	219:18,19	16,18	46:4	259:2,4,
	220:4	96:20	48:14	10,19
patent	227:19		50:1 65:2	260:2
10:7,8	239:4	pause	67:18	performing
11:10,13,	249:1,4,	153:3	69:19	195:1
15,20	16,18,20	218:21	78:19	225:19
12:1,6,	250:3,4	pay	81:14	241:10
11,19	251:5,13	68:4,22	82:8,12	242:8
28:18	252:5,9,	69:1	88:12	243:12
32:14	12 253:1,	212:11	90:12	perimeter-
73:3	15,19,20	PC	97:21	to-area
76:13	254:1,7,	180:4	98:20	142:1
113:19	10,13	200:20	105:8,14	
114:20	255:16	201:1,4,	107:21	period
115:4,8	257:2,11,	11,12,14,	109:20	86:7
116:22	17 263:14	15 202:7,	111:5,16	241:11
126:3,12,		8	132:13	periphery
20	patents		136:11	141:16,21
127:13,20	7:4 10:10	peak	158:10	144:6
128:11,20	49:11	224:1	164:19	
129:12	53:6,15	PECVD	165:9,10	person
131:2,4,	74:17	63:4,6,	235:20	17:14
9,13,16,	116:6	14,16,20	241:18,19	42:16
19,22	118:7,8	64:1		65:5,7
132:10	159:8		perfect	67:13,14,

21 80:10	phosphorus	picture	106:8,12,	201:11,
132:7	193:11,20	44:10	14,16,22	12,14,15,
134:10,	199:2	207:21		22 202:6,
11,20		208:2	planarized	8 203:8
136:7	photochemic		192:15	204:3
196:3	al	piece	193:5	210:13,14
	100:9	37:21		211:3,9,
perspective	photon	100:16	plane	13 212:8
36:22	96:22	146:12	151:11	
136:22				
perspective	photons	pioneering	planning	plugs
s	95:18	18:15	61:2	210:14
19:22	photoresist	34:13	plasma	PNP
petition	97:11	pivotal	23:22	216:12
12:6	98:1,6,	105:15	25:11	point
126:19	16,20		94:20,21	28:10
127:2,9,	99:16	place	107:10	102:2
12 128:3	100:1,5,	56:9 76:8	138:19	112:13
252:16	6,7,8,13,	77:1 81:2	215:19,20	119:2
	18,20,21	100:20	233:11,	141:8
petitioner	101:6,16,	102:11	15,16,19	147:22
6:1,2	21,22	178:10,20	234:2,4,	148:1
	102:5,11,	183:12	13,17	149:2
Ph.d.	13,15	201:15	235:6,13,	152:14
48:11	103:2	216:14	17,22	164:18
59:14,22	104:3,5,9	261:10	236:5,8,	171:4
60:13	106:13,		11,15,21	175:21
61:3	18,22	places	242:1	178:20
134:7,10	107:5	149:13		180:7
136:2,4	177:13	166:22	plat	185:8
249:10	181:21	206:5	88:17	186:19
		208:5		194:9,13,
Ph.d.s	photoresist	plain	88:15	17,20
69:20	or	146:5		197:10,19
phase	97:6	plan	play	200:10
174:7		251:13	36:11	238:13
	phrase		194:5	244:1,5
PHD	158:3,7	planar	pleased	254:9
5:4 125:3		106:11	14:17	259:5
phenomena	phrased	planarizati	15:4	
157:22	122:6	on	plenty	pointed
	physical	104:19	24:17	204:16
phenomenon	42:12	105:15,18	57:3	208:16
87:2	54:13	107:7,18	206:5	
phosphorous	84:6,15	194:6	257:5	pointing
190:21	pick			183:19
192:10	90:16	planarize	plug	polishing
193:17,21		105:3,22	180:2	104:13,16

polymer	239:10	168:20	156:10,	254:12,
42:8	240:21	preheat	11,16,17	15,16
100:2	position	57:5	190:21	255:16
polymers	14:18	preparing	193:16	problem
42:4	103:3	129:22	243:3	26:2 33:3
polysilicon	224:1	prescribe	preventing	42:15,20
139:8	250:9	90:8	194:7	83:8
141:6	positive	prescribed	232:7	105:5
143:5,9,	100:17	177:21	previous	195:4
13 144:22	possibly	prescriptio	9:2 73:14	231:13
169:4,10,	161:12	n	82:19	233:3
17 170:8,	244:17	254:17	147:14	problems
10,13,20	potential	presence	previously	23:2
171:15,17	232:13	223:1,12	51:9 59:9	procedural
172:15	potentially	present	66:8 76:1	76:5
173:6,8,	162:2	26:2	77:15	procedure
14 194:1,	244:6	28:22	125:5	82:4
7 214:10,	Poured	101:3	204:21	procedures
15 228:14	173:20	113:6	primarily	72:2
229:17	power	179:7	23:13,22	proceeding
230:10,22	55:2,9,12	193:21	27:20	19:3
231:10,12	214:19	205:15	34:19	process
233:19	practical	president	35:11	17:8 18:1
234:9,10,	33:16	17:14	134:18	19:13
18 256:3	59:10	press	232:11	20:1,3,4,
porous	pre-	110:16	primary	11,14
42:4	competitive	pressures	139:11	25:5,18
portion	36:6	240:18	principally	26:4,17,
30:10	precautions	pretty	25:3	22 27:9,
34:4	242:15	28:8 53:9	principle	15 28:7,
101:5	precise	105:10	157:17	20 29:9,
170:10,12	62:19	108:21	prior	13,16,21
185:9,22	82:8,12	132:13	9:7 11:2,	30:3,11
186:20	precursor	144:13	9 18:21	31:6,8,
196:4	173:4	186:17	83:17	10,15
197:12,	precursors	191:14	118:8	32:3
20,21	113:6	234:3	130:5,7	34:4,15,
204:4,6	predict	262:13	150:1	16 37:4,
221:9	64:20	prevent	160:10,11	9,12,13,
226:20	preferred	121:19	175:6	14,15,17
259:12		122:15	184:14	38:16,18
portions			186:14	39:7,11,
31:14			250:10	12,16,20
220:17				40:6,7,14

43:4,7,	81:6,22	233:15,16	137:9,10	proper
14,18,19	82:21	239:9,14,	221:20	240:1
44:6,14,	83:20	19 240:3,		255:18
16,21	84:21	13 241:2,	processors	
45:1,2,	86:17	20 244:20	44:10	properly
11,16,22	87:6,7,16	245:2	produced	248:7
46:2,8,	91:10	257:12,17	244:20	properties
16,18	96:14	258:1,3,	producing	112:8,12,
47:4,6,9,	97:9	8,10	255:16	17 113:9
10,17,21	100:15	260:1,2	product	114:6
48:11,19	101:11	262:7,22	22:11	116:15
49:2,7,	113:6	263:10	39:4,13	119:2
18,20,21	115:9	processes	81:2,18	183:8
50:4,6,8	132:11,	17:7 26:7	products	192:12
51:2,3,	17,22	30:13	83:22	197:6
10,16,22	133:5,11,	35:7,21,	profile	protect
52:5,7	22 135:5,	22 40:3,	103:2	143:6
53:7	20	13 41:8	164:13	199:1
54:9,11,	136:10,	48:2	165:15,	229:18
18 55:6,	13,14,17,	51:4,11	16,17,20	230:12,22
15,17,18	19,22	52:3,6	166:2,5,	231:22
56:12,22	137:4,13,	57:13,15	12,16	protecting
57:11,12	20 138:19	58:4,6,11	167:7,20	101:1
58:19	142:20	62:2,5	168:2,7,	182:15
60:2,3,5,	152:8	64:1,17	12 209:15	protection
13,21,22	162:10,15	65:17	217:17	140:5
61:3,4,5,	163:5	66:17	224:9,15,	229:22
14,18	171:20	71:6,13	22 225:15	protects
62:6,10,	174:2	72:6	profiles	159:10
12,13,14,	175:7	73:1,5,10	165:1,2	provide
15,18,20	177:1,3	77:14	220:5	8:2
63:4,14,	179:12	81:15	227:9	137:22
15,18,20	182:9	101:18	255:7	198:7
64:1,2,3,	185:5	112:18	profiling	263:8
4,6,9	200:22	113:5	61:8	provided
66:4,6,7,	212:6,7	132:15	program	76:1
15 70:22	213:14,16	133:8	24:18	126:6
71:4,9,	214:5,17,	136:14	30:19	160:14,15
10,12,18,	21 215:15	245:3	34:12	198:3
22 72:5,	218:5,22	processing	38:14,15	211:22
8,12,13,	219:9	10:19	67:8	262:20
14 73:9,	220:1	30:7 35:2	pronounce	263:12
15 77:16,	222:3	68:1	13:5	providing
17,19,20,	227:11,18	134:7		53:19
21,22	228:12	135:22		
78:6 79:2	229:11	136:9		
80:9,15	232:6			

proviso	162:2	78:3 79:5	214:16	88:14
129:15	212:15	quality	218:15,20	197:3
public	248:15	111:1,14	234:11	253:16
19:2	253:12	121:8	238:20	254:20,
publication	put	140:1	240:2	21,22
16:2,13	16:17	141:8	242:7,12	255:1,14
publication	25:14	143:10	243:5	256:5,6,
s	29:7 31:8	188:6	244:9	9,15,18
15:5	33:2	231:11	245:13	257:1,7,
28:19	36:13	quandary	261:20	19
32:14	68:11	76:5	questions	randomizes
250:10	82:16	quartz	7:6,7,9,	223:8
publishable	97:11	111:6	11,15,16,	randomly
28:7	100:1,22	question	17 8:3,5	258:20
published	104:2	9:16	52:18	range
52:2	121:16	18:18	53:17	113:5
pull	137:19	19:4	56:2	220:9,13
249:7	158:20	21:11	73:19	245:20,
punch	166:21	25:17,19	76:10	21,22
158:16	187:15	28:13	108:4,12	246:1,4
pure	193:2,5	29:17,18	130:4	rapid
17:1	208:5	40:16	131:8	140:19
purported	223:7	53:3 68:5	132:22	161:14
254:14	238:2,12	73:7,8	248:20	171:14
purports	241:2	76:5,12	249:4	207:12
180:16	261:9	80:3	quibble	rare
182:10	264:8	82:19	209:19	46:12
190:1	puts	92:13	quick	Rarely
purpose	241:3	107:4	126:7	99:4
122:5	putting	115:7,17	131:5	rate
200:6	157:20	116:2,14,	228:8	31:5
216:9	puzzle	16 117:1,	248:9	85:20
purposes	37:21	4,8	quoted	86:1,2,7,
13:1	puzzling	135:10	200:18	10,13,17,
125:12,16	152:1	146:11		22 87:8,
130:21	PVD	147:17	R	10 92:10,
134:12	41:8	148:15		14,15,22
142:15	84:8,10,	157:11	R-u-b-l-o-	93:6,8,9,
154:19	11,17,20,	169:9	f-f	19 172:5
156:15	22 85:3,7	186:17,18	8:11	240:11
159:21		187:3	radius	241:13,15
	Q	192:21	158:14	244:18
		196:19	raised	rates
	qualify	197:1,4		
		211:20,21		

92:10,22	reactive	20:12	recipe	reexaminati
93:4	83:21	realize	55:5 78:5	on
241:7	84:1 88:2	54:22	82:4	12:13
ratio	reactive-	79:8	recitation	refer
175:18	ion	196:17	129:10	47:20
240:11	64:2	realized	recognition	50:7
244:22	144:3	35:15	184:13	51:2,10
245:5	182:18,	realtime	recognize	55:18
246:16,	21,22	31:3,4,9	112:14	57:13
18,21	215:11,16	reason	182:11	58:5,7,19
ratios	229:4,7	8:1 44:15	190:4	63:22
105:2	230:4,8,	68:20	recognized	83:14
142:1	20 231:6,	73:13	29:1,4	84:8
245:7	10 232:14	96:17	reconfirmin	96:12
re-ask	234:14	117:3	g	98:4
234:11	235:9,18	198:6	180:5	104:15
257:16	236:4	204:4	reconvene	131:9
reach	245:15	216:22	264:16	202:19
144:19	reactivity	219:16	record	221:13
145:7	120:12	reasonable	6:5,6 7:9	239:3
reach-	reactor	21:7	8:9 73:22	256:16
through	87:13	150:12	74:22	reference
163:19	91:2	152:9	75:4,9	82:18
164:9	reactors	156:4	131:11	131:12
reaches	88:4	reasons	188:13,	142:5
55:11	reacts	138:14	14,18	143:1
144:4	23:5	recall	records	160:3,9,
145:5	read	10:18	81:2	12 161:5,
react	127:1	26:1	rectangle	10 162:13
122:13	131:13,15	218:2	203:21	163:3
reactants	161:6	recent	reduce	180:18
113:6	180:19	13:14	138:6,12	188:22
reaction	185:14,17	recently	140:13	189:3,6
32:7	193:15	24:13	231:13	209:10
83:22	197:5	recess	reduced	210:4
122:10,	212:10	54:3	143:12	212:19
17,18,22	230:14	124:12	reduces	213:15
140:6	252:20	162:22	182:6	219:19
156:11,17	253:20,22	188:15	reducing	228:19
157:20	real-world	228:10	140:9	229:2
reactions	80:7	248:12	referenced	232:18
84:12	reality			233:6
				235:7,9
				177:19

213:8	117:13,14	246:10	171:13	remember
references	195:6	regions	relevance	8:20
130:6	regarded	95:21	33:13	10:1,4
140:15	111:16	163:7,8	relevant	11:9,11,
160:4,5,	regime	164:13	17:3	19 12:15
16	87:18,22	171:21	126:18	22:4 26:6
referred	91:4	189:17	127:12,20	46:11
115:4	172:6	201:5	130:12,14	66:12,19
142:22	regimes	213:20	134:5,15	70:14,18
160:3	87:7,10	216:12,	203:1	94:15
191:17	region	13,17,18,	220:3,6	142:7
212:19	49:3	19,20	241:17	144:16
228:21	88:14	217:14	252:8,12	165:7
253:18	99:22	219:2,7	reliability	175:20
referring	101:1	220:13,	37:2	178:13
27:20	119:5,7,	16,19	reliable	179:2
82:14,15,	15,20	221:9	106:2	184:10
20 83:1	145:14	222:2,5,	reluctant	185:19
85:4	149:22	12 228:15	135:12	201:2
156:20	150:13,15	230:18	rely	207:19
163:14	152:11	239:15	210:3	218:7
173:15	155:21	243:14	relying	231:19
190:19	156:3	244:6	183:22	238:4
193:11	158:5,12	regular	184:4	remembered
225:21	164:16,18	22:7,13	remain	32:22
233:15	165:13	relate	183:15	218:12
234:8	167:4,16	25:1	221:2	remind
refers	172:2	related	remaining	18:18
92:9,22	183:3	7:6	101:5	56:17
96:13	193:13,16	10:10,12	144:22	removal
119:8	195:7	12:5	181:4,7	94:18
201:21	200:9,10	19:13	193:19	remove
202:8,9	203:21	70:3	205:22	94:10
249:17	204:11,	126:19	remains	95:20
256:9	12,22	128:11,18	179:15	99:22
refining	205:7	136:14	181:13	100:14
63:5	206:14	140:8	183:13	101:7,9,
reflected	207:4	252:9	184:1	10,12,15,
208:12	216:16	relationshi	189:8	20 102:9
reflow	217:11,22	P	239:1	181:10,17
196:8	218:1,4,	49:17	remarkable	189:17
regard	17 219:1	132:15	33:20	205:6,8
74:11	225:16	relative		239:14
	230:12	163:20		240:5,8,
	243:22			20 241:12

244:6,19	126:1,4	research	resolution	restarting
246:6	131:2	15:12	24:10	251:12
removed	142:19	16:5,15	resonance	restate
93:19	160:1	18:8,9	215:20	27:3
101:3,4	212:13,17	19:13,20	respect	result
107:18	248:13	20:3,13	13:16	71:18,19
182:3	251:3	21:3,5,	18:21	resulting
204:1,5	253:10,14	15,17	53:18	84:1
239:18,20	264:4	22:1,2,6,	73:14	217:6
removes	reporter's	19 25:22	208:17	260:11
205:5,17	56:18	26:14,20,	respond	results
241:5	represent	21 27:12,	76:12	90:13
removing	7:1 12:18	15 28:3,7	respondent	203:5,7
244:5	60:2	29:12	5:18 7:1	retained
259:12	118:21	32:1	75:19	9:3
repair	representat	33:19,21	responsibil	237:13
229:3,13	ion	34:2,11	ities	238:5
230:7,19	74:10	35:1,3,	22:3	254:4
231:14	represented	18,20	60:9,16	retuning
repairing	11:10,12,	36:11,15	responsibil	81:14
230:3	14,15	38:15	ity	returned
232:6	68:12	40:21	41:2	75:6
repairs	representin	68:13	43:6,7	returning
230:17	g	reserve	45:16	238:21
repeat	5:18,22	56:2	64:22	reveal
7:15	request	76:16	responsible	19:3
rephrase	12:12	reserves	24:16	reverse
230:5	require	76:14	34:20	32:6
replace	24:9	residence	35:11	review
41:21	216:11	19:12	40:12	12:6 13:8
42:2 79:2	required	residues	42:17	16:18
80:18	14:1,2	138:18	45:1 46:4	126:20
report	136:4	resist	47:8	127:13
15:4	146:3	97:6	60:2,6	128:6
reported	225:14,15	98:21	63:3,5	189:2
69:19,21	requirement	99:1	64:16	248:9
183:3	89:3	100:10	65:6,8	reviewed
reporter	requires	199:16	67:22	185:3
7:8 12:21	262:1	204:9	68:3	reviewing
13:4	reread	259:14	rest	13:10
125:10	187:2	resistance	104:4	126:9
		206:7	220:4	
		resistivity	259:18	
		41:20		

131:7	roadmap	8:8,11,12	Samsung	55:4
150:3,5	20:8	13:1,3,11	7:4 9:3,8	screwed
163:16	36:2,4,5,	15:9	160:6	78:3
177:4	7,8	18:17	237:14	
178:5	roadmapping	54:6	254:4	seconds
179:2	41:16	77:10		55:11
182:16		123:11	Samsung's	246:9,16,
189:5	robots	125:3,9,	126:2,19	17,20
190:18	38:20	12,16,22	127:9,12,	247:4
199:13		126:10	20 212:21	
201:13	role	130:21	251:4	section
202:14,16	14:20	131:1	252:4,9,	20:10
211:16,18	19:19,20	142:15	12,16	182:5
213:18	20:1	159:21		239:3
214:7	36:12	188:17	Santa	
218:10,14	194:5	212:15,20	52:11	sector
219:4	roles	237:1	sat	39:14
221:11,15	22:1	248:15	237:6	seemingly
228:16	Ron	249:7,10	satisfactor	79:18
229:8	5:19	251:2	y	sees
231:17		253:12	135:14	66:4
232:15,16	room		satisfies	166:20
233:2,21	21:18	rule	263:19	select
235:4,11	22:5,8	57:17		160:9
251:9,22	24:15	run	saturation	
259:20	79:13,15	49:15	164:21	selected
	257:5	80:11	scanning	212:21
revised			233:1	selection
72:12	rough	running		213:2,11
RF	28:17	80:9	schemes	
55:12	91:20		17:8	selective
Richardson	92:2	S	school	205:9
5:22	105:10,19		69:4	selectivity
rid	roughly	sabbatical	science	205:10
80:17	213:6	15:2	17:6,15	self-
RIE	214:3	sake	23:2	aligned
143:9	246:2	76:2	26:16	26:3
232:4	RPI		38:13	131:3
233:13,16	70:16	sample		158:4
234:2,5,	RPIS	54:12	scientist	159:14,18
19	6:3 7:7	59:8	17:1	163:20
235:13,22	RTO	168:4	scope	178:8
roadblock	205:2	sampling	76:6,18	208:1
116:8	Rubloff	70:2	260:6,14	219:19
	5:4 6:19	135:7	262:10	self-bias
			screen	240:16

semester	semiconduct	58:2	255:3,8,	206:22
24:14	ors	71:12	11 256:12	207:12
	10:13,15	80:16		220:20
semiconduct	36:4,5	133:1,3,	shallowly	
or	102:9	7,21	255:19	shows
5:19,20		136:14	shape	140:16
7:1 10:19	senior	184:6	167:10,	178:6
15:10	68:6,21	257:22	14,15	187:8
16:20	69:1,2	258:3,5,	shapes	203:21
17:4 18:7	135:18	7,11	208:21	shy
20:9 21:5	sense	259:3,5	share	135:21
25:1,4	25:20	260:10	50:14	side
26:8,22	32:15	sequences		88:21
27:15	34:13	35:22	Sharif	90:7
29:3,15,	48:5	81:15	70:7	91:15
21,22	97:15	serve	sharp	122:21
30:6,11,	109:6	121:18,19	166:9	158:15,18
14 31:15,	149:3	140:4	shine	159:6
16 33:10,	198:22	157:22	100:4	241:14
11 34:4,6	236:2	161:12	shining	sides
35:6,7	260:8	176:22	98:10	159:7
36:18	sensing	177:2	short	169:4,10
37:9,13	20:3	180:10	50:18	172:14
38:15	sensitive	193:19	52:3 71:9	173:14
39:20	97:7	serves	162:19	243:15,
40:7 43:4	100:2	162:1	shortchange	17,18
44:21	sensitized	177:7	d	sidewall
45:10,21	18:3	190:20	137:5	88:15
68:1 71:1	sensor	191:2	shorted	115:12,16
73:5 74:7	31:4	serving	121:10	140:6,20
77:12,16,	sensors	186:12	145:3	141:12
17,18	20:16	SESSION	shorter	143:5,12
99:2	241:20	125:1	53:12	161:4,7,
109:18	separate	set	shorting	9,13,17
112:16	58:6	38:12	158:15	168:21
114:2	separately	71:5	show	169:3,10,
115:1	207:18	210:10	208:8	14,15,16
116:19	separation	258:9	shown	170:1,5,
118:11,17	119:1	shallow	178:1	20 176:3,
134:6	sequence	26:3 49:4	180:8	8 178:1,
135:22	34:16	89:4	203:6,8	6,7,11
136:9	40:2 49:3	119:17	204:1	179:10,
137:9,10	52:3 53:8	168:6		14,16,19
145:18		254:18,19		180:9
257:12,18				181:5,7,
260:1				
262:6,22				

11,13	194:22	42:2 92:2	69:21	262:5
182:11	196:4	110:21	71:18	situations
183:14,17	221:1	111:7,11,	89:2	103:1
184:2,7,	228:13	15,20	157:2	158:11
9,21	239:1,11	112:10	161:14	159:9,17
185:6,10	241:12	113:2,3,7	189:20	sketch
186:15,21	242:6	115:18	213:13	209:21
187:10,19	244:7	121:14,15	simple	skill
188:5	245:17	122:12	36:13	49:10
189:13,	247:12	141:5	90:17	132:7,21
14,18,19	sideways	165:8	99:20	134:12,21
190:6	240:11	168:3	183:13	172:21
191:3	245:18	169:6,17	186:18	181:2,12
193:9,19	signature	171:8,10	simpler	182:11
194:2,4,	264:14	172:2,4,	24:3	183:15
16 196:21	significanc	21	simply	184:5
197:13,21	e	173:20,21	154:13	186:16
198:8,11,	194:10,14	174:3,6,	211:21	190:4
17,22	significant	9,19,20,	244:5	196:3
200:11	40:17	22 175:4,	single	208:22
204:13,15	significant	5,6,11,	30:2	210:9
207:11,	ly	12,15	37:17	246:12
13,14,15	significant	176:14,	40:13	258:22
209:15,16	ly	17,19	54:11,12,	skills
220:1	192:13	177:20,22	19 137:16	38:12
226:4,14,	205:12	178:3,6,	206:11	68:17
21 227:7	233:11	11,21	Sio2	slides
229:18	234:13	179:16	31:21	96:19
230:11,	silicide	189:14,15	32:8 42:8	slightly
17,21	17:10	190:20,22	174:19	20:6
231:12,21	122:14	191:13,16	175:10	small
239:16,21	170:17	192:7	sir	10:2,18
240:8,22	171:1,15	193:12,	249:14	13:20
241:3,5	194:1	15,17	siren	135:7
242:15,17	silicides	198:15,19	60:10	smaller
243:1	23:3,5	200:21	sitting	41:19
244:3,15,	silicon	214:10,11	79:13,15	175:13
19 246:7	17:12	224:2	128:17	smallest
247:6	19:9,19	255:17,19	185:8	29:5
sidewalls	23:3,5,13	256:1,7,	186:19	smooth
149:22	26:11,13	10,21	262:4	141:5
170:13	28:17	silicon-	situation	64:10,21
171:7	31:21	based		
178:4,22	32:8	192:9		
180:21	41:12	similar		
189:8		52:13		

sojourns	143:7	13,19,20,	spacers	236:5
23:14	161:21	21 154:7,	117:4	specific
solid	163:21	20 155:6,	161:8	39:6
81:12	164:13,	13,20	184:21	43:7,8
soluble	15,18	156:6,10,	185:10	45:1
100:11,12	165:5,10,	14,16,20,	186:21	47:5,9
solution	11,12,13	22 157:4,	204:15	50:8
100:22	166:4	6,13,14,	spaces	53:15
someplace	176:4	15 159:10	153:11,	56:8
85:16	200:9	162:2,3,	14,22	61:10,14
107:17	216:20	5,6	154:12,	63:19
159:15	217:13	176:22	14,20	64:10
SOP	218:1,4	177:3,6	157:15	71:13
82:3	219:2,7,	178:2	spacing	72:18
SOPS	22 220:19	179:14	156:2	74:11,17,
72:1	221:9	180:11,	157:7	18 76:13
sort	222:12	12,15,16	161:19	85:6
18:21	225:16	181:5,7,	span	114:5,13,
23:16	229:19	15 182:12	76:4	19 115:4
48:1	230:12,18	183:14	spatial	116:3,21,
53:20	240:7	184:7,9	119:1	22 117:19
sounds	256:5,6,	185:6	speak	118:6
108:14	7,9,15,	186:15	40:19	120:18
209:2	16,18	187:10,19	158:10	121:1
source	257:1	188:5	speaking	122:4,7
168:10	space	189:9	36:21	137:10
174:12	146:9	190:8,9	54:18	139:21
195:6	147:8,13	194:16	72:10	154:6
214:14	148:8,11	195:1	109:20	185:9
217:8	151:15,19	196:5,10,	242:11	186:20
222:4	152:20	12,13,16,	special	214:17
229:10	155:4,14	22 197:22	35:1	239:19
253:17	176:9	198:1,2,	67:18	259:2,5
254:20,	227:13	3,17	specialist	specificall
21,22	spacer	200:11	37:16	y
255:1,7,	113:12,14	209:17	specialty	172:17
14,22	114:2,7,	219:10,13	97:4	180:19
256:4,19	10,16,22	220:2,7,	species	184:20
257:7,19	115:2,11,	17,22	88:2	189:7
source/	15,22	221:7,10,	94:21	191:7
drain	116:9,18,	17 222:1	120:11	specificati
103:21	20	225:20	182:21	on
	117:18,20	226:1,17,		
	118:16	18,20,22		
	123:21	227:7,17,		
	153:6,9,	18		

237:4	staff	state	12 193:6,	stop
specifics	17:14	8:9 38:11	8 194:6,	86:15
80:4	22:1	69:15	15 196:9	108:6
87:12	stage	stated	199:14,18	144:13
spectrum	196:20	177:5	200:4,7	243:22
53:10	197:20	statement	206:21	stopping
speculation	227:18	27:7 28:5	207:22	199:19
261:22	stand	75:12	213:19	storage
speech	201:1	130:18	216:5,10	14:19
66:20	standard	143:20	218:5,22	29:1
speeds	72:1 82:3	148:20	219:9,21	stories
41:19	107:11	234:9	225:18	20:18
spell	173:19	260:18	226:22	story
8:9	204:14	statements	228:3	19:8 92:1
spent	255:5	237:9	239:5	stepped
42:6	standardly	stature	75:5	straight
spot	142:2	213:9	steps	232:3
264:8	standpoint	stenographi	46:9,16	strategic
spread	51:14	c	47:22	16:7
166:10	stands	75:4	48:1 49:8	26:19
sputter	84:15	step	53:7,10	27:11
88:13	start	30:2	55:15	41:14
111:8	8:6 16:19	54:19,20,	57:22	strategical
sputtered	48:22	21 55:1,	71:9	ly
111:6	70:2 94:7	5,18,19	72:14	67:11
sputtering	133:9	57:7,8,9	78:10,16	strategies
84:14	136:15	62:3 78:2	79:2,3,8	15:14,17
85:3,6	242:22	79:9,14,	80:16	105:14
107:14,22	started	18 80:10,	81:21	strategy
111:7	17:1	11 87:3	133:2,3,	15:20
squared	20:10	88:9,10,	10 136:10	19:11
234:18	22:20,22	11,18,21,	137:12	102:18
stability	25:7 32:1	22 89:9,	164:6	103:6
31:20	34:12	11,14,20	166:19,20	104:1
stack	165:7	90:7,9,	177:13	strengths
89:4	168:6	10,21,22	184:6	111:3
184:11	175:13	91:10,14	258:1,3,	stress
216:15	starting	101:14	7,9	140:18
stacking	163:3	102:10	259:1,18	183:7
214:9	starts	149:21	260:2,11	stretching
	192:18	163:5,10,	262:6,22	111:2
		17 169:6	263:10	strictly
		176:3,7,	STI	
			119:15,16	

72:10	261:8,9,	211:8	28:8	214:9
96:11	10,15	stuff	130:3	sucked
stripping	262:8	15:6	164:20	264:2
177:13	263:1,2,	51:19	165:3	suggest
strong	4,9,11,18	74:15	166:13	48:6
209:3	structures	96:18	substantial	108:11
structural	23:10,11	103:21	ly	suggestion
133:2	28:12	214:20	93:21	262:12
structure	32:5	250:17	143:11	suing
21:16	35:16,22	styles	179:11	11:16
45:19	88:13	85:3	substantive	summarize
46:13	89:6	SU8	74:4	20:22
91:22	103:19	102:5	substeps	summary
105:2	106:3	subject	55:7,16,	16:4
114:19	141:18	7:6 10:16	19,20	129:15,17
115:8	153:11,15	32:13	56:9 58:4	support
133:4,10,	154:13,15	submitted	substrate	127:9
21 138:16	155:1	126:2,11	55:10	supported
139:6	156:3	127:8	155:8	38:14
143:10	157:8,16,	128:4	168:16	suppose
147:22	17	251:4	174:11	72:11
153:10,	163:19,21	252:4	193:13	91:20
14,21	245:6	subsequence	214:13	103:14
154:12,	student	80:16	215:6	261:8
14,20	59:22	subsequent	216:6	supposed
155:22	60:12	98:5	219:22	6:13
158:13	63:2	143:12	223:6	44:15
170:5,9,	70:4,14	166:20	224:18,20	supposition
14 177:6,	students	169:6	225:6,12,	32:2
7 178:16	29:12	192:14	13 227:5	suppress
179:10	48:7,12	221:19	228:14	157:21
181:13,	59:11,13,	222:1	236:16	245:18
18,20,22	14 65:22	230:13	256:10,	surface
182:7,14,	66:14	259:13	11,17	20:15
15 187:8	69:9,14	subsequent1	259:14	23:2
189:19,20	132:19	y	subsumed	25:10
191:3	135:6	160:22	164:6	28:14
194:5,18,	137:6,7	217:8,12	subtleties	31:10
22 201:22	studied	256:11	56:9 61:5	32:9 84:1
214:6,18	127:6	subset	successful	85:13,15,
218:11	study	40:6	42:22	17 86:5
219:17	183:10	substantial	successivel	
243:14,15	studying		y	
260:3,11,	24:11			
17,19,22				

88:2	38:3	46:7	229:12,16	105:16
89:16,17,	39:19	52:20	233:10	107:8
21 90:1,	40:14	53:15	234:12	112:11
4,18	51:2 72:3	62:6	teaches	113:2
91:16		69:7,12	207:21	215:21
92:11,12,	T	77:16	208:2	216:1
15,16		96:19,22	229:3	242:2
93:1,2,9,		97:2	230:6,10	255:6
10,19	table	113:18,19	248:6	technology
94:11	232:19	145:12,19	teaching	17:12,16
97:10	233:8,17	146:1	184:15	19:9,19
102:13	235:6,8	157:8	186:11	20:8
104:10	tail	159:8	team	26:9,11,
105:1,4,	143:17	165:10	40:22	13 28:2,
11,19	taking	184:12	41:3,14	14 36:2,
106:1,8	7:2 189:2	188:18	42:18	4,5,8
107:16	211:17	226:1	43:5	41:15
119:11	264:15	238:10	68:11	67:7 70:2
138:20	talk	245:9	teams	106:6
139:1,7	12:12	249:19	42:5,6	115:19
141:5	39:18	252:15	65:3,4	135:21
175:19	56:17	259:22	67:16,17	143:3
224:3	89:9	talks	Techknowled	165:8
243:21	95:14	176:13	ge	173:21
255:17,20	99:10	189:14	5:18 6:22	236:22
256:3,21	105:7	210:13	technical	tells
surfaces	110:12	target	17:14	39:1
17:2	114:14	84:17	149:1	86:14
28:17	138:2	85:5,10	technically	149:1
86:18,19	169:5	111:6	148:18	208:21
87:1 92:2	192:18	targeted	technique	temperature
93:20	199:10	142:4	29:7	31:21
surprises	talked	224:8	84:3,12	34:17
81:13	35:14	225:15	102:19	55:11
susceptible	68:1	task	103:7	85:12
179:21	168:19	37:16	104:19	168:5
183:4	199:9	68:15	105:17	193:6
switch	237:4	taught	107:20	temporarily
258:20	247:16	33:1	173:11	14:21
261:13	249:16	186:14	255:6	tend
sworn	250:7	teach	techniques	65:2
5:6 125:5	talking	96:18	25:9 29:2	tendency
system	17:18	135:14	95:1	104:22
37:19	38:8	137:20		
	39:17,19			

tens	146:3	171:14	204:8,10	89:1
236:4		172:5,18,	220:22	91:12
	terms	22 173:5,	221:3,7	93:12
term	20:22	15	224:6	142:4
47:19	28:6	174:14,21	241:3	161:8
48:3	47:16,17	175:6	244:19	180:15
50:6,9	50:3	176:1	263:6	184:15
51:1,5,9,	52:17	194:2		185:3
12 52:2,	53:17	198:8,12	thicknesses	190:5
13,14	54:7	204:22	222:21	232:22
53:1	60:22	205:3,6,	thin	235:15
58:21	77:14	12,18	22:14,17,	237:12
59:7	82:16	206:10,22	19 23:4,	254:20
62:5,18	108:21	207:2,3,	8,15	
63:19,21	109:21	12 227:11	24:11	things
64:7	112:4	228:13	28:14	9:5 11:22
70:22	150:21	229:3,12	29:2 39:6	12:3
71:3	164:3	230:2,6	61:8 65:8	14:7,16
78:12		231:5	84:2	17:22
83:11	test	255:18	91:21	20:2 24:3
84:5	81:18		96:3	30:15
85:20	testified	thick	110:17	33:17
88:12	5:6 125:5	187:17,	112:15	35:14
89:11	testifying	18,21,22	142:21	37:3
92:5	76:20	188:2,3,4	143:6,10	38:20
95:11			172:4,6	41:15
96:13	testimony	thickening	188:10	42:19
97:21	8:17 74:1	172:10	205:21	43:12
108:17	text	thicker	214:11	44:16
110:2	164:7	90:6,22	221:18	46:15
113:11	178:10,20	172:8	224:10	49:2,17
115:2	208:6,11	175:21,22	225:7	61:9
119:4,8,	210:4	205:12	229:19	62:11
22 123:5,	237:6	224:17	230:11,22	70:3 89:2
21 145:13	247:15	thickness	231:11,22	95:10
147:2	248:3	30:22	242:5,13,	107:21
153:6,9		31:5,13	22 261:9	112:16
154:7	thermal	88:16		136:16
157:14	23:11	89:15,20,	thing	138:22
158:3,6,9	31:20	22 90:21	14:11	139:2,10
159:1,13	85:14	103:2	18:21	140:7
161:3	138:3,11,	161:18	30:9 32:4	156:13
162:6	12,21	171:14	44:17	167:19
165:19	139:12,19	175:3,5,	48:6	184:12,
257:1	140:19	12,14	52:15	15,18
	150:1	187:11,16	69:21	210:10
terminology	161:14	188:7	87:15,21	216:16
53:1 56:1	170:19			

236:1,11	165:1	244:14	58:3,10	touching
240:18	throughput	tiny	60:21	158:22
250:12,14	99:5	110:12	63:4,5	tracking
thinking	tie	titled	82:4 97:2	60:20
50:21	74:5	131:2	137:17	trade-offs
51:18	tied	142:20	tool-type	43:20
thinned	76:12	249:9	52:4	traditional
220:13,16	159:13	253:15	tools	ly
221:2,10	time	today	16:10,12,	64:8
222:13,	8:16	6:1 7:3	16 20:17	train
15,20	10:21	8:3 9:6	38:19,22	65:3
227:6	18:5	23:17	40:3 44:9	135:8
thinner	19:15	42:22	55:1	training
91:17,18	20:15	52:18	top	132:12
thinnest	42:10	57:4	38:6	trajectorie
144:17	55:11	58:18	66:18	s
thinning	65:8	128:17	88:17,20	227:2
222:2	69:11,16	185:8	90:5,6,21	trajectory
thought	70:16	186:19	91:16	223:9
32:20	78:21	249:8,11	106:22	trans-
49:8	86:6,7	262:4	141:6	capacitors
52:22	102:11	today's	146:1	245:7
68:21	151:21	7:5 46:16	175:15	transfer
82:20	162:9	token	176:21	95:6
110:4	164:20	136:2	181:3,10	96:15
114:11	183:2	told	183:6,18	transferred
117:16	186:10,13	91:9 92:1	186:11	96:3
118:4	189:2,5	tolerance	193:4,16	97:10
121:18	210:9	102:22	203:17,22	transform
133:15	211:17	242:9	204:11,13	100:10
135:8	215:9,16	tomorrow	224:12	transistor
150:19,20	235:20	264:9,10	225:7	10:22
250:8	241:11	tool	226:11	71:7
thousand	244:16	18:16	232:19	115:20
88:20	246:22	35:3	240:7	119:9
thread	250:19	39:14	241:4	165:4
83:6	253:6	48:20	259:12	166:14
three-	255:10	49:2,16	topic	214:8
dimensional	259:21	54:20	65:2	216:12
71:7 88:6	timed	55:15	topography	217:9,17
102:20	241:19	56:11	103:3	253:16
103:10	times	57:4,10,	104:7,10	
104:7,10	9:2 21:13	14,22	105:1	
	52:2		146:2	

transistors	true	250:11	64:12	47:2
119:13	172:1,3		120:3	
214:14	258:12	typed	132:5	uncomfortable
216:11		250:17	138:1,10	208:19
	truth	types	145:11	
transition	77:7	62:2,5	147:11	uncovered
41:9	truthful	63:22	148:4,9	172:2,4
122:11	8:2	215:13	153:12	undergo
transport	truthfully	typical	155:9,11	157:19
87:10	7:8	37:7 97:8	160:8	
88:1		132:13	162:11	undergraduate
117:13	tube	146:21	169:1,8	te
120:10	32:4	244:22	172:16	59:20
121:12	tungsten		175:2	undergraduate
140:7	170:17	typically	176:6,16	tes
156:12,18	194:1	40:16	188:19	135:15
157:18,19	214:10	49:12	189:4	
		60:1 81:3	192:3	underlying
transport-	tunneling	86:2	196:1	103:3
limited	188:8,10	90:3,10	200:5,17	underneath
87:19		91:8	202:10	23:5
91:4	turn	94:20	210:16,22	104:8
	20:16	95:7,9,	214:4	181:20
treated	31:10	20,22	216:8	200:14
97:12	55:8,9,13	99:3	220:21	
treatment	167:8	100:2	221:4,5	understand
166:20	228:17	101:12,17	222:6	7:12,13,
167:21	232:18	102:9	227:21	14,18
168:2	233:5	107:13	230:9	36:17
255:18	235:1	111:1,16	233:7	38:15
256:13	turned	112:20		43:2
trench	23:1	119:8	UHV/CVD	44:4,14
26:3 49:4		132:16	34:18	47:15
89:4	turns	136:22	35:10	48:22
119:17	175:11	138:20	ultimate	49:17
	two-step	236:8	262:7	52:19,20
trenches	179:7			55:20
89:7	198:18	typing	ultimately	57:20
Trial	200:22	238:10	24:16	61:21
12:6	207:22	typo	256:17	62:1
trick	type	253:8	ultraclean	63:10
30:21	24:7		34:14	73:17
	84:11		35:16	82:11
trouble	108:4	U		84:20
103:2	116:19		ultraviolet	96:6
	214:21	Uh-huh	99:6	103:8
troubling	238:17	40:9	unclear	107:3
52:1				

114:5	17:5	universal	94:19	152:19
116:7,13	underwritin	109:1,12	174:7	241:7,13
117:2	g	universitie	variants	244:14,22
120:22	18:14	s	71:17	245:16
123:3	uniform	136:20	vector	246:6
127:8,10	61:9 90:5	University	139:6	vertically
131:21	uniformly	38:11	vectors	152:12
134:16	88:5	unmark	36:9,12,	240:11
142:6	107:15	85:5	13	vice
146:11	unintended	unmasked	vehicle	17:14
155:5	79:10,22	166:22	255:15	video
180:17	uniquely	unneeded	velocities	5:15
184:14	258:10	79:18	164:22	view
197:9	unit	unusual	velocity	89:2
208:7	48:19	218:3	85:16	112:13
210:8	50:4,6	usual	vendors	135:4
213:10	51:4,11,	32:22	97:4	238:14
239:8	15,16		version	viewed
242:7,12	52:6		35:3	58:12
243:4	54:9,11,	v	40:22	visibility
247:20	18 55:6,		72:15	45:16
248:2	15,17	vacuum	96:1	vision
254:7	56:12,22	135:20	238:17	34:21
255:3	57:10,12	vague	versions	vitae
256:22	58:3,6,	83:7	96:5	13:4
259:17	11,18	97:20	versus	voids
understandi	60:2	117:9	81:11	32:12
ng	61:14,18	valid	103:3	volatile
31:20	62:15,18	109:1	171:15	32:8
65:16	63:14,18	validity	vertical	volatilized
71:3	64:4,6,9,	128:11	45:19	139:1
77:1,13	17 65:16	129:11,19	86:18	voltage
132:11	17 71:6,	253:1	87:1	110:8,14,
135:19	12 72:6	valve	89:17,21	17 240:16
136:15	73:10	55:12	90:4,7,18	volts
145:17	77:20	vapor	91:15	182:20
151:4	78:6	23:12	92:11,16	236:5,18
152:7	81:14	42:12,13	93:2,9,20	
184:1,4	86:5	83:12	146:9	W
193:8	132:15	84:6	147:1,8,	
understood	units	86:21	13	
7:17	86:3		151:14,19	W-a-y-n-e
114:1,4				
223:20				
underwent				

8:10	85:11	Wong	33:9,14,	works
wafer	90:3	142:22	17,22	47:5 61:5
54:12	97:22	228:18	34:16	137:4
79:13	111:10	229:2,6,	36:9	world
85:18	113:5,8	12 230:6,	37:17	29:3
87:14	140:15	10 232:17	43:19	46:21
111:8	255:11	233:6,10	48:9,14	97:3
168:4	256:20	234:12	61:13	145:19
174:11	259:6	word	65:3	world's
182:19	263:13	47:10	69:16	29:5
236:16	Wednesday	54:21	79:11	worry
wafers	264:16	59:6 62:9	83:17	32:4 38:7
81:17,18,	weekly	95:4 96:1	85:9	worst-case
19 88:5	15:6	97:17	107:12	241:20
wait	weird	114:11	131:19	write
55:10	63:19	145:17	132:14	72:14
153:12	wet	147:6	136:15	82:3,4
168:7	24:1,2	149:6,8,9	143:2	237:11
234:7	94:3,6,8,	151:6,7	237:14	writing
waived	9,12	152:6	250:2,12	7:9
264:14	173:10,	153:1,2	254:5	written
walk	16,18	155:6	worked	72:1
162:9	wide	209:4	9:8,11	wrong
213:14	245:21,22	wording	11:3 12:5	20:22
wall	windows	190:3	15:10,15,	209:3
81:12	137:19	words	20 19:9	wrote
wanted	wire	25:16	30:13	16:17
12:1	105:9,10	150:21	35:18	
27:13	119:12	151:5	42:11	X
36:1	159:4	189:11	66:15	
150:8	wires	209:7	70:7,16	X-ray
157:2	41:18,20	work	workhorse	99:1
158:16	42:3	6:9 8:13	24:3	
223:22	106:9	16:4 18:8	working	Y
water	wiring	21:2,10	9:19	
33:2	42:22	22:9,14	16:19	year
113:7	106:4	23:8,10,	18:6	13:17,21
174:1	wondering	21 24:4,	26:12	14:9 66:2
Wayne	67:3	7,9,22	31:2	254:3
8:10	184:16	25:4,11	32:18	years
ways	217:10	27:15	41:6,7	
67:10	231:4	29:1	44:9	
		30:10	49:3,4	
		31:20	63:13,14,	
		32:22	18 65:15	

12:16
19:7
44:14
49:13
65:14,19
71:22
132:18
134:6,22
136:1,8
137:8

yield

60:22
68:11
81:16,19
139:4

Yorktown

22:6
26:14
32:17

young

68:18