UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Case IPR 2015-00459

Patent No. 6,150,244

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Samsung Electronics Co. LTD.,
Samsung Electronics America, Inc.
Samsung Semiconductor Inc. and
Samsung Austin Semiconductor LLC, Volume 2 of 2

Petitioner, Pages 263 - 465

vs

Home Semiconductor Corporation,

Patent Owner

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DEPOSITION OF GARY W. RUBLOFF, PH.D.

Washington, D.C.

Wednesday, August 19, 2015

9:00 a.m.

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Whereupon, this is the deposition of GARY W. RUBLOFF, PH.D.who appeared as a witness called by the RESPONDENT in the above-styled caption, was called and was examined on Wednesday, August 19, 2015, conducted at the offices of Fish & Richardson, P.C., 1425 K Street Northwest, Washington, DC 20005 Virginia, commencing at 9:00 a.m., and was reported and transcribed by T. S. Hubbard, Jr. a notary public for the District of Columbia.

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P R O C E E D I N G S

MR. MUKERJI: The witness remains under oath from yesterday.

BY MR. CHEN:

Q Good morning, Dr.~Rubloff.

A Good morning.

Q Dr. Rubloff, did you speak with your attorneys last night?

MR. MUKERJI: That is a yes or no question.

THE WITNESS: It is a yes or no question?

MR. MUKERJI: About anything?

BY MR. CHEN:

Q Did you speak with your attorneys about the subject matter about your deposition last night?

A No, I spoke with him about a restaurant.

Q And this morning you did not speak with him about the subject matter of your deposition either, is that correct?

MR. MUKERJI: That would breach the privilege.

THE WITNESS: I am sorry?

BY MR. CHEN:

Q And this morning you also did not speak with him about the subject matter?
A No.
Q Can we look at Exhibit 8 which is your declaration submitted in connection with the Samsung IPR '224 patent, and if we could go to paragraph 12.
Paragraph 12 is where you state what you believe is the person of ordinary skill in the art for the '244 patent, correct?
A Yes.
Q You have given the same definition of "person of ordinary skill in the art for the '244 patent as you did for the '997 patent, correct?
A Yes.
Q Did you come up with your definition of a person of ordinary skill in the art for '224 patent separately from the '997 patent?
A Yes.
Q What did you consider when coming up with your definition for a person of ordinary skill in the art for the '224 patent?
A I considered what the '224 patent teaches, what the time frame of the '224 patent was.

What the state-of-the art at the time was like and what skill sets are coming with the degrees in universities that people are trained with, and the things that they will have to master beyond that or at least --

Well, not master this necessarily, but to become familiar with by working in the environment.

Q The two to three years of experience in semiconductor processing industry that a person of ordinary skill would need to have, is that also experience in process integration?

A Yes, it would certainly include that.

Q Why is it important for them to have experience in processing integration with respect to the '244 patent?

A The '224 patent goes through a number of process steps to achieve a certain result.

In this case, the raised source drain structure and so one really has to understand sequences of steps, something about the process consequences of each of those steps and what the motivation in the architecture of the device really is.

Q When you say that a person of ordinary

skill in the art needs to understand the sequence of steps, why is that important?

A The fabrication of a specific device, the kinds that are treated in the '244 patent will have one or another paths to realization, so these will be sequences or possibly different alternative sequences to achieve the result.

Q The sequence of steps will affect the result?

A Yes, the sequence of the steps will affect the result and the details of those steps and the substeps will affect the result, some more than others, and depending on which result we are talking about because there are numerous properties of the resulting device and its constituents that are important, less important, and so on.

Q You also said that a person of ordinary skill in the art would need to understand the process consequences of each of those steps.

What did you mean by that?

A If you will look at a single process, a unit process, let's say, you can characterize its consequences usually by multiple metrics.

For example, what is the resistivity of

the material? What is the breakdown field if it is an insulator? What is a deposition rate? What is the conformality and the like?

Those are all consequences of how the process works and how the equipment carries out that process.

Q Then you also said that a person of ordinary skill in the art would need to understand what is the motivation in the architecture of the device, what did you mean by motivation in the architectural or in the motivation of the architecture?

A If you are looking at the target of the '244 patent, the goal of the '244 patent, or if you're looking at the prior art which is very similar to that of the '224 patent, there is a goal in mind, and the way you would like to have the structure look when you are done is part of the thing that would need to be understood, and the different ways in which you might get to that result which things can be substituted for which things, and the like, there are lots of considerations there.

And in general when I was talking here about what would be the characteristics of one of

one of ordinary skill whether it is the goal of the '244 patent or any other patent of this type looking at a device structure and function, you would need to have some familiarity with how those things play together.

Q How would one of ordinary skill in the art achieve the goal or the motivation of their architecture?

MR. CHEN: Let me reask that.

BY MR. CHEN:

Q How would one of ordinary skill in the art design a process to achieve a specific goal or motivation of the architecture?

MR. MUKERJI: Object to the form.

THE WITNESS: What architecture would you like to talk about? What function?

BY MR. CHEN:

Q When I asked you why a person of ordinary skill in the art would need to understand the motivation of the architecture, you stated that a person of ordinary skill in the art would have certain goals in mind and you used the '244 patent as an example?

A Yes.

Q How would a person of ordinary skill in

the art design a process to achieve the goal that they have for the specific device?

MR. MUKERJI: Objection to form.

THE WITNESS: That's a very broad question. Your answer would be, the technology is here, I want something to change, I look at what constraints are there, I look at what processes I have available, my understanding of those processes and their consequences for subsequent processes and the like, and I try to dream up a solution.

BY MR. CHEN:

Q Is part of achieving the goal the selection of specific steps and arranging those steps in a specific sequence?

MR. MUKERJI: Objection to the form.

THE WITNESS: We are still speaking in gross generality here.

BY MR. CHEN:

Q Sure.

A But given that in parting some innovative function to a technology that already has a kind of existing shell, certainly means understanding what will change and what will stay the same, so what processes are there and what

order they can be carried out or alternative ways in which those steps and sequences can be arranged to achieve a similar result.

Q You are of the opinion that with a specific result in mind that there are multiple ways that a process could be constructed to achieve that result, correct?

A There may be multiple ways.

Q For example, you could have a process with a certain sequence of steps, that would achieve a result and you could have another process with those same steps arranged in a different order that would achieve the same result, correct?

MR. MUKERJI: Objection to the form.

THE WITNESS: I mean in principle this could happen. More typically there would be some level of change.

If you're talking about rearranging steps, I have, let's say, eight steps that achieves a result.

In a very general sense you're asking me, as I understand it, could I exchange Steps 6 and 8, right, in the cases where I could achieve approximately the same result

by doing that there would be other changes that I might make to the details of 6 and 8 or to the details of the final structure for that matter, and the question whether it is worthwhile is a different question because you still have to ask the question, "What things are different from the manufacturing point of view?"

If the resulting structure has somewhat different properties, they may be better or they may be worse.

The costs and complexity and the yield price you pay by doing it differently they could all be different.

You cannot predict without going through an exercise here, a real exercise, not the kind of hypothetical one which way would be the preferred way to do it.

BY MR. CHEN:

Q When you say a real exercise, are you referring to an actual experimentation with equipment and a wafer, actually building the device with the different processes?

A I think there would be two stages at least of looking at this.

The first one would be, I have a certain body of knowledge as one of ordinary skill about what these steps will do and what modifications and processes each can make and what the consequences will be for those steps.

Then what the consequences are for the way in which I arrange these steps and make modifications to each of those steps in any new arrangement if needed.

That is the kind of thing of "one of ordinary skill" would be sitting around the kitchen table or at their desk at work thinking through and trying to see from their body of knowledge what they expect is credible and what is not, so they will go through and I have seen many people doing exactly this.

That is where innovation comes from and they look at the scenarios and sometimes talk to colleagues about it, work on the blackboard, erase things, and so on, it is actually one of the more interesting exercises, to see whether conceptually it makes sense.

These days they also have significant tools, modeling tools, computational tools at hand so they can actually predict whether this is going

to work with some degree of accuracy never complete and then ultimately if you get through the first stage of conceptualization, the person of ordinary skill and you may do some modeling after that, the next stage would be to prototype it experimentally so you would have to find a way to use the facilities in a different fashion.

From a manufacturing plant you are going to detract from throughput because you're going to use the tools for your little experiment, so you have to do that as a prototype, and then if it is serious, make a decision whether to commit to the experiment to determine whether this works at reasonably high volume.

BY MR. CHEN:

Q What you just described is part of the real exercise that would need to be done in order to determine whether a process step sequence could be rearranged, correct?

MR. MUKERJI: Objection to form.

THE WITNESS: I described multiple levels at which this assessment can be done starting from a very basic one which is a blackboard exercise to larger commitments of resources that usually would only be pursued

if the earlier investigations indicated sufficient benefit to justify the costs of pursuing it further.

BY MR. CHEN:

Q I want to make sure I understand, that this is the assessment or the real exercise that would need to be done in order to determine whether the process step sequence could be rearranged, correct?

MR. MUKERJI: Objection.

THE WITNESS: It depends on what you mean by determination. I can look at a sequence of steps and the result and I can play with that on the blackboard and I can determine, "This is credible. I think this will work."

But I don't know how well it will work, right, because I haven't done it, right.

On the other hand, one of ordinary skill or above could look at that and at least say, "This is very credible," and often what that will lead to is something kind of in between in the sense that I see I could restructure the process, even move steps around or replace steps or take out steps or add steps

or something like that, and I could look at that carefully and I can analyze it and I can conclude, "This is doable."

I haven't done it yet. I haven't looked at the process regime specifically for each of those steps that I need, but I can say that this is credible.

Often the judgment at that point is, "Is it worth the experimentation to do that?"

Very often people decide it is going to take us weeks, months, something like that to really test it out or even to refine it because it may require computational studies and so decide not to pursue it because there is a cost in trying anything.

BY MR. CHEN:

Q Previously, I asked you whether you could have a process with a certain sequence of steps that would achieve a particular result and that you could have another process with those same steps arranged in a different order that would achieve the same result.

As part of your answer you said, "In principle this could happen," but said that you could not predict what would happen without going

through the real exercise, not a hypothetical one in which way would be the preferred way to do it. That is what you said, correct?

MR. MUKERJI: Objection to the form.

THE WITNESS: Are you reading from the transcript or are you paraphrasing?

BY MR. CHEN:

Q I am reading from the transcript, but it's a rough right now.

You said more. I am trying to shorten it. Does that sound a fair characterization of what you said? I can just reask the question.

MR. MUKERJI: Objection to the form.

THE WITNESS: I don't want to leave the impression that you only know the answer after all of this experimentation and prototyping and manufacturing environment because that is not the case.

BY MR. CHEN:

Q Right?

A There are plenty very good innovative ideas that come from that kind of exercise and appear in patents and are certainly patentable that may never have seen the manufacturing floor.

The problem we are having is you're

asking questions in great generality and I don't understand the relevance to the patent at hand.

And I think I'm having trouble making it sufficiently clear to you that this exercise you are asking about is hypothetical and it is not a single level.

There is a level that can be done on the blackboard in an hour's discussion with a couple of people.

There is a level that actually maps it out and looks at what each step's parameters will be and maybe into some modeling of that, and then there are various levels of experimentation, some of them just on subsets of that sequence that are seen as the most likely to control what the change and the result is.

BY MR. CHEN:

Q What you have described then, are various levels of analysis that might need to be done in order to determine whether a process sequence could be rearranged to achieve a particular result, correct?

A Say the last part again?

Q What you described are various levels of analysis that might need to be done in order to

determine whether a process sequence could be rearranged to achieve a particular result, correct?

A I wouldn't say might. I would say may or may not be needed to make an assessment of whether the result could be achieved by a different arrangement of the process flow.

There are modifications and rearrangements as we are talking about that would certainly be credible if built upon what one of ordinary skill understands an etch process does, what a deposition process does, lithography constraints, and so on, and for the most part the people of ordinary skill will be able to determine whether it is credible, right, but that does not mean manufacturable because manufacturable has to do with costs and reliability and yield and all of these things.

But when people do that initial level of investigation, if they are of ordinary skill or above, I think they can make a pretty good guess as to whether it is possible. It doesn't mean it is practical yet because they haven't done all of the experiments, but they certainly know what is credible.

Put it another way.

I have heard and I have said it any number of times the statement, "This makes sense. This is something that ultimately would work or it is very likely to work," meaning, I don't know, a high likelihood of doing it.

But that doesn't mean we will pursue it because to actually bring it to manufacturing entails a substantial cost.

That is a situation that is likely to be possible, but a decision was made not to bring it into manufacturing so it remains in the category, "Yes, that is workable."

The question is: Are we going to follow that or not? Does it give us enough advantage to bother pursuing?

Unless you are in research. If you're in research you can do any of these things.

MR. CHEN: Let me make sure I understand.

BY MR. CHEN:

Q Is there a difference between something that is possible and something that is credible?

A You're looking for a semantic response here?

Q You used both terms and I wasn't sure whether you were using them interchangeably or whether you were referring to two different levels of assessment?

A I was trying to talk like an ordinary person. Excuse me.

MR. CHEN: I appreciate your effort.

BY MR. CHEN:

Q You were just using them interchangeably, then, possible and credible?

MR. MUKERJI: Objection to the form.

THE WITNESS: I think you are putting too much into my choice of words.

One of ordinary skill considering various arrangements of structures and processes and their sequences and the details thereof come up with something that looks interesting.

If I call it possible that means, and I haven't demonstrated it, then is it really possible, that is a semantic thing that I haven't thought about, so I don't know how to deal with that.

If I call it credible I know how to deal with that because I or a group of us have

gone through using what we know about the art, and we think, "Yes, that should work," so it is credible. If it weren't credible we would say, "That is a dumb idea, so let forget it."

BY MR. CHEN:

Q When you come up with something that is credible, that does not mean it is manufacturable, correct?

MR. CHEN: Let me reask the question. I can see where that might be a little bit difficult for you to answer.

BY MR. CHEN:

Q When you have done this assessment and you and your team come up with a solution that you believe is credible, that does not mean you have determined whether it is manufacturable, correct?

MR. MUKERJI: Objection to the form.

THE WITNESS: It depends what you mean by manufacturable. If it is credible, then I believe if a group of ordinary skill has determined that this is credible, it is extremely likely that it is manufacturable as a structure.

Whether you would put it into

manufacturing given costs and yield and other considerations, that is a different question.

There is a difference between, "Can I fabricate it?" which is what credibility says, "Yes, I can fabricate that," and, "Is it cost effective at the higher levels to actually manufacture it?"

BY MR. CHEN:

Q So the performance of those real exercises that you had discussed earlier that was to determine whether something is manufacturable in the sense that you would actually manufacture it?

A No.

Q No? Where do all of those real exercises come in?

A Let me give you an example. I think it is a good example. We use thin film processes of the kind that you see here to make device structures which are essentially electro chemical batteries.

I think I mentioned this earlier, so we use these processes in the sequence and we had the idea that if we use amortization of aluminum and we make pore structures out of that and then use a

variant of CVD which is called ALD, we could cut very thin layers inside these tiny pores at each end and we can put active layers of ion storage materials at each end and then fill it with electrolite we can make a working nano-battery.

And we did.

We talked about it. We were not sure we could make it, but we were pretty sure, so it was credible, right, and we knew it well.

It may not be a really good battery because this is a pretty speculative domain. It turns out it is really a good battery, so we did the research experimentation, but we were pretty sure we could make this structure and so that is a level of credibility, the performance would have to have some way of estimating what that might be and we got that right as well.

But that doesn't mean it is manufacturable at high volume and it doesn't mean that it is doing going to be cost effective which probably it will not be in this example.

Another example would be something closer to the subject at hand because the prior art in the '244 patent shows more than one way of making a structure for a raised source drain like

the '244 is amended at, and in that case the steps that are involved and the differences in sequence of those substeps in the different embodiments that we address, as I wrote in my declaration, that is very credible because these steps are well understood and they have been practiced in combinations like that in other parts of very same technology.

It is all there in my declaration. One of ordinary skill would know that one can embody the innovation of the '244 patent in more than one way.

It is much easier to talk about that than the generalities that we have spent, I don't know, the last 40 minutes on?

Q When those of ordinary skill have analyzed the process and determined that it is credible to rearrange the process sequence to achieve the same innovation --

MR. CHEN: Let me give you a specific example and start over.

BY MR. CHEN:

Q When those of ordinary skill in the art have analyzed the process disclosed in the '244 patent, and determined that it is credible to

rearrange the process sequence to achieve the same innovation as the '224 patent, is that rearranged sequence a new innovation?

MR. MUKERJI: Objection to the form.

THE WITNESS: You are stating things incorrectly. The '244 patent was invented, disclosed, after the ones we are talking about in the prior art.

There were multiple ways to achieve the raised source drain structure disclosed in the prior art I have cited here before the '224 patent, so nobody had to have or look at the '244 patent to do that, it was already done.

BY MR. CHEN:

Q What I'm asking you is, persons of ordinary skill in the art analyzing the '224 patent, and looking at the '244 process, if they look at that process and determine that it is credible to rearrange the process sequence in the '244 patent, to achieve the same goal or results that are stated in the '244 patent, have those of ordinary skill in the art then created a new innovation?

MR. MUKERJI: Objection to the form.

THE WITNESS: I can't answer that question because prior art value in innovation as I understand it from the patent law you cannot invent something in hindsight.

The '244 wasn't there.

I don't want to speculate on what somebody would learn from the '244 patent to go back and invent something else.

The '244 patent says what it says, but what it says has been already disclosed in the prior art so I can't answer your question.

It's a hypothetical.

It has got the order of the times wrong or something.

I will clarify.

I went through the exercise in all three of these patents of responding to what I was asked to do which is to look at the prior art, identify if in the prior art there were teachings for each of the claims and the substeps of each of the claims in these patents, that is what I did.

In doing that to note whether one of ordinary skill might put together different

things that were known at the time and be motivated to put them together to achieve a result.

The result was not to be, "Can we match what is in the '244 patent?"

My question is: Would people understand from the prior art I have cited that you could achieve raised source drain structure which is shallow doping, that is what it is all about, in one way or another.

BY MR. CHEN:

Q Did the prior art you analyzed for the '244 patent provide a process for achieving raised source drain structure that had the same process steps and in the same sequence as disclosed in the '244 patent?

A You said same process steps and sequence. Some of the prior art had a similar sequence to that in the specification of the '244 patent and more than one embodiment in the prior art met the requirements of the claims in the '244.

Q Did the embodiments in the prior art disclose a process with the same sequence as that disclosed in the '244 patent?

MR. MUKERJI: Objection to form.

THE WITNESS: I think it is time to look at the '244 and make sure I understand what sequence you are referring to.

BY MR. CHEN:

Q Sure.

A Because the claims indicate a set of steps, but not necessarily a sequence, and there are a certain number of embodiments, but each embodiment will have some sequence, so I wanted to make sure I understand which sequence you are talking about.

Q If you look at Exhibit 9, which is the '244 patent.

A Right.

Q The '244 patent provides a description of a preferred embodiment and this is beginning at Column 3 Line 50 and continues to Column 6 Line 8.

A Right.

Q In preparing your declaration, did you find any prior art that disclosed a process for fabricating the device with a raised source drain that had the same sequence of process steps as disclosed in the '244 patent?

A Yes.

Q Which prior art disclosed the same sequence of process steps?

A Nakamura third embodiment, I think it is. There is the planarization of the insulated dielectric down to the etch stop layer on the gate electrode similar to this and so the sequence is essentially the same.

Q Nakamura first embodiment does not disclose the same sequence, correct?

A Nakamura first embodiment has sort of a different sequence. Let me think about whether I would properly describe that as a different sequence.

Yes, it is a different sequence, the first embodiment. Sorry. It is a different sequence than the '244 specification shows. Let me make sure I clarify that.

Q Is it a different sequence than the '244 Claim 1 if the limitations of Claim 1 were interpreted to have the listed order of steps?

MR. MUKERJI: Objection to the form.

THE WITNESS: Claim 1 does not specify sequence of steps.

BY MR. CHEN:

Q If Claim 1 were to be performed in the

listed order of steps, would Nakamura Embodiment 1 disclose that same order of steps?

MR. MUKERJI: Objection to form.

THE WITNESS: Wait a minute. I would like to see the Nakamura reference. I don't think it has been entered yet.

MR. CHEN: I think you are right. Give me a minute.

(Whereupon, Respondent's Exhibit Number 10 was marled for Identification.)

THE WITNESS: Your question is which embodiment?

BY MR. CHEN:

Q Embodiment 1.

A One.

Q Yes.

A Let's repeat the question. I believe your question is: Does Embodiment 1 of Nakamura represent an equivalent sequence of steps as Claim 1 would be interpreted if it literally said it has to be this sequence? And the answer is no.

Q Yesterday you provided a definition of raised source and drain and you said that the raised source drain was the area that was above the substrate surface.

Do you recall that?

A I think that is what I said. That is most of where the material is, the dopants that were in it are no longer all the way in it.

Q So the raised source and drain refers to the dopant in the source material before that dopant has been diffused into the substrate after heat treatment. That was your definition yesterday, is that correct?

A I don't remember exactly what I said.

Q Would you stand by that definition?

A My recollection is we were talking about what structure is the raised source drain, and I said, "I think it is called raised source drain because it is above the crystalline silicon and the function which is the important thing is to supply in communication with the crystalline silicon a source of dopants that could then diffuse and form a shallow junction in the crystalline silicon."

Q Is that the understanding of raised source drain that you used to conduct your analysis of the '244 patent and the prior art?

A I think substantially so. The motive of a raised source drain is to produce a shallow

junction by out diffusion from a structure in intimate contact with crystalline silicon in the source and drain regions.

So the semantics and we can debate for a long time about whether one should define the raised source drain is only the part above the crystalline silicon surface or the part above the crystalline silicon surface plus the shallow junction the dopants that wandered out by diffusion.

I think that is a distinction that is inconsequential. The point of a raised source drain is you make a structure which allows shallow doping by diffusion into the crystalline silicon.

Q But you define the raised source drain as the material above the crystalline silicon, correct?

A I think I did. I think I referred to it as that. I didn't think I was being asked to make some kind of formal definition of that.

Anyone who looks at these structures one of ordinary skill in the art knows that the function is to make shallow doping which you cannot do the same way by ion implantation, conventional means and that somewhere along the

lines somebody calls it a raised source drain because there was dope polysilicon above the crystalline silicon.

I didn't find in my investigation an irrefutable historical statement of who started the term and precisely what they defined that to mean if they did define it to mean something and particularly when I was at North Carolina State University we had people working on various versions of shallow junctions and raised source drain and they used the term pretty loosely.

I don't want to pose as if I know more than they do about a formal definition because it is the function that matters. I am sorry. The function and how that function is achieved.

Q Did you contact a formal construction of the term raised source drain when you were providing your analysis of the '244 patent and the prior art?

A I was asked to look at a number of terms and I don't recall which ones, so give me a minute to look for that.

In the brief overview in my paragraph 17, I said, "The '244 compares two different methods of forming the shallow junctions, ion

implantation, and the use of a raised source drain technique.

"According to the patent the method solely using, ... blah, blah, blah.

As an alternative, the '244 patent describes various advantages to the use of raised source and drain technique to create shallow junctions and describe their raised source and raised drained are performed by diffusing dopant ions into a substrate surface by dope material formed at the surface regions of a substrate where the source and drain are to be formed."

So this doesn't make a definition. This is paraphrasing the essence of the '244.

Oh, here, terminology. Sorry. Yes, paragraph 21: "I have considered whether a broadest reasonable interpretation of the raised source and raised drain is recited in Claims 1, 5, 6, 14, and 16 is broad enough to encompass a source and drain formed at least in part by diffusing dopant ions into a substrate surface by a dope material formed at the surface regions of a substrate whether the source and drain are to be formed," and I believe that a is reasonable interpretation.

This tells me that what I was saying is that the function is to diffuse dopant ions into the crystalline silicon surface.

Whether that means that I call the raised source and drain a little shallow doping region, or shallow doping region, and the polysilicon source above it, or just the polysilicon source above it, I think, is not the important issue here. It is the function that matters.

Q The function of the raised source and drain is to diffuse dopant into the substrate, correct?

A Right.

Q And the reason why the dopants should be diffused into substrate is to form the shallow junction, correct?

A That is correct.

Q It is the shallow junction that is actually the source and drain of the device, correct?

A Yes.

Q The raised source and drain is not the source and drain of the device, correct?

A I haven't made a formal definition of

which three dimensional volume is the raised source and drain.

I said earlier yesterday that I think of the raised source and drain as the source there and I really wasn't thinking about a definition of which volume we are talking about.

What is important here is the function and the structure that has used that function, I could conceive of other structures which will achieve shallow junctions that do not look like what they are in the '244 or in the embodiments in the prior art.

So raised source and drain means I made a shallow junction by diffusion into crystalline silicon and the architecture of structures that can do that would include various things.

I don't think it matters whether I am talking about defining this volume or the little piece under it or both of them together as the raised source and drain.

Q I am trying to understand the definition you used when you did the analysis of the '244 patent and the prior art?

A Yes.

Q The reason why I am trying to understand

it is because raised source and drain is a term that is used in the '244 patent.

A Yes.

Q Let me try to go through this again. You stated that what is important for the definition of the raised source drain is its function, correct?

A Yes.

Q And that the function of the raised source and drain is to provide dopants that will then be diffused into the substrate, correct?

A Shallow, yes.

Q And the reason why they want to diffuse those dopants into the substrate is to create the source and drain for the device, correct?

A That is correct.

Q So the raised source and drain which is the source of the dopants that will then be diffused into the substrate to create the source and drain of the device is different than the source and drain of the device, correct?

MR. MUKERJI: Objection to form.

THE WITNESS: I am sorry. Say that again. I was looking at this.

BY MR. CHEN:

Q The raised source and drain which is the source of the dopants that will be diffused into the substrate in order to create the source and drain of the device is different than the actual source and drain of the device, correct?

A Structurally that is different, yes. The structure that is the source of the dopant diffused and the source and drain that follows, that is right.

I think it would be exaggerating the significance of what I said yesterday which was saying, "I think the term came from looking", you have got the source of the dopants above the crystalline silicon surface to exaggerate the significance of that into a formal definition. I stand by the definition here which is the definition of function.

MR. MUKERJI: We have been going for more than a hour. Dr. Rubloff, do you need a break?

THE WITNESS: I think we should take break about every hour.

MR. CHEN: Let's take a break.

(Whereupon, a break in the proceedings commenced at 10:30 a.m. and on resuming at 10:40 a.m.)

BY MR. CHEN:

Q Why not turn to the '244 patent, that is Exhibit 9. I want to direct your attention to Column 2, the "Summary of Invention"?

A Yes.

Q There in the "Summary of Invention," starting at Line 30 ending at Line 64.

A Yes.

Q It describes a process for forming a device with a raised source drain, correct?

A Yes.

Q Looking at the sequence here as it is described in "Summary of Invention," do you see the step of "exposing the portion of the third dielectric layer covering the gate electrode structure by planarizing the top portion of the fourth dielectric," do you see that, it is at Line 47?

A Yes.

Q Do you see following that there is another step, "forming on the substrate a pattern second resist layer, masking portions of the fourth dielectric layer," do you see that?

A Yes.

Q Is it your opinion that those two steps

could be performed in the reverse sequence?
A Yes.
Q It is your opinion that you could form a patterned resist layer masking portions of the fourth dielectric layer and then follow that with a planarization of the fourth dielectric layer?
A Planarization usually means all the way across the wafer, right, so if you had a resist you really could not planarize another layer underneath it without losing the resist.
But the clause which starts exposing would be achieved by using the resist to etch the fourth dielectric layer, and embodiment, I have to make sure I get the right one, Embodiment 1 of Nakamura does precisely that.
Q Let's focus on the '244 for now. We will get to Nakamura later.
A But it says "exposing". It doesn't say "planarizing".
Q If you look at the limitation, it says, "Exposing the portion of the third dielectric layer covering the gate electrode structure by planarizing the top portion."
A Yes, but etching with a resist in place, a region of the fourth dielectric layer between

where the resist masks are would be equivalent to planarizing that portion because the resist is here, between whether resist is you are etching and the etching is a uniform process, so in that sense it is planarizing it.

Q Is it your opinion that any time you etch with a mask you effectively are also planarizing, is that correct?

A Unless your etch is highly nonuniform and nobody wants that you are planarizing portions between the resist mask components because you are etching uniformly.

Q Could you perform chemical mechanical polishing to planarize with a resist in place?

A I think that's unlikely. I don't know if there are configurations that people might think about, such as if you wanted to remove the resist at the same time you might be able to do that.

Q If you want to keep the resist, if you could?

A If you want to keep resist, I think it is dubious, but I haven't thought about how I might invent a way to do that.

Q You would have to invent a new way?

A I think you would have to invent a new way. On the other hand, it could happen. There are plenty of scanning actuation devices that people think of all kinds of applications for.

Q You stated that planarization usually means all the way across the wafer. Is that how a person of ordinary still in the art would generally understand the term planarization?

A I think someone of ordinary skill, if you say, "How is planarization done, does it mean across the wafer?" they would first think of the cross-wafer embodiments of planarization, such as etchback and CMP, but I think that you also think about what are the consequences of etching, dry etching when you have a resist mask in place? I don't think it is a stretch for them to think about that.

Q In your experience have you ever used the term planarization to refer to the consequences of etching with a resist mask?

A Probably not because it is assumed that you have uniformity of the etching process for the way the top surface evolves when you are etching between the regions between the mask.

The criterion for a reasonable dry etch

process and an anisotropic etch process is that it is uniform across a millimeter, if not larger dimensions, or you wouldn't be using it, so it means between the features it is uniform etching which means that it is planarization as well as etching.

Q Are you saying that the dry etch process is only used where the distance between the masked regions has to be either a millimeter or larger?

A No, no, of course not.

Q You said the criteria of a reasonable dry etch process is uniform across a milliliter if not larger dimensions. What did you mean by that?

A Yes, but that doesn't mean that the spacing between the photoresist piece is millimeters, by no means, it is much smaller than that.

It means if I have a substrate, let's say a large wafer, and I measure the etch rate in different places across many millimeters, then I should get essentially the same number.

Q If you could turn to your declaration. It is Exhibit 8, page 32.

A Yes.

Q If you would look at the bottom of page

32, you have referenced a couple figures from the Nakamura reference, do you see that?

A Yes.

Q Do you see Fig. 2A?

A Yes.

Q And do you see that Fig. 2A is the result of the etch process using the resist mask 28, correct?

A It is the initial part of the etch process.

Q But here Layer 26 has been etched using the resist 28 as a mask, correct?

A Yes.

Q Is this etch a planarization?

A Let me say it this way and I will repeat what I said before. A dry etch an anisotropic etch is a local planarization where local means where the resist mask is not and that may be a small dimension or larger dimension.

Q I don't understand what you just said. You said a dry etch is a local planarization where the resist mask is not. What do you mean by resist mask is not?

A A resist mask, I have photoresist in certain locations, and no photoresist in other

locations, between the photoresist components that are left, during anisotropic etching the etch takes place of the material underneath, that is what the purpose of that kind of step is.

No one would use a highly non-uniform etch rate in that process to remove the material that this patterning is intended to do, so that is why I am saying that any such etch processes will locally maintain a planar form, so it is a planarization step as well as an etch step.

In that sense think about etchback, tungsten etchback, which we will probably talk about sometime today, in that case, you sputter the layer that has been deposited away and that is the same thing that happens, essentially the chemistry is different, but the same thing that happens in anisotropic etching and it better be uniform or it will not be planarizing.

Q It is your opinion here that in Fig. 2A the top portion of Layer 26 has been planarized by the etching process?

A Yes.

Q Which part has been planarized by the etching process?

A The part between the Elements 28.

Q Even though all of the Layer 26 between Elements 27 has been etched away?

A Even though.

Q All of the portions of Layer 26 between Elements 28 has been etched away?

A What I was trying to depict in this particular portion is the first part of that etch step which etches the top surface of the Layer 26 uniformly and therefore planarizing down to the exposed part of the etch stopper Layer 24 that is on the top of the gate electrode.

That is why it corresponds to the words that you mentioned exposing the portion of the third dielectric layer covering the gate electrode structure by planarizing, which I do by anisotropic etching, the top portion of the fourth dielectric layer, so I think it matches correctly. It meets the language of '244.

Q How does it match? What portion of the Layer 26 has been planarized as shown in Fig. 2A?

A How does it match? I thought I said that.

Q I don't think it is clear. Could you explain again how has Layer 26 been planarized as shown in Fig. 2A?

MR. MUKERJI: Objection to the form.

THE WITNESS: It has been planarized by etching. The etching process maintains, removes the surface and leaves a planar surface when it does that.

BY MR. CHEN:

Q Where is the planar surface?

A There are several of them because it keeps moving, but you see the shaded region between the combination of photoresist, and ILD materials, the shaded portion there, if you take the top piece of that, draw a horizontal line, then take the next one further down from that, and further down from that, that material that is being etched is being planarized.

Q The etch process that removed Layer 26 here, does it stop in the middle of the shaded region?

A No, the etch process starts from the top of 26, and with the photoresist mask in place and it moves down and after a while it encounters the top surface of Layer 24 on the gate electrode and it keeps moving down and ultimately gets down to the top of the etch stop Layer 24.

It then has removed all of the ILD and

then the succeeding part of that etch goes through the Layer 24, the etch stop layer leaving the side wall spacer in place opening the contact to the diffusion region to what will be the diffusion region for the raised source drain.

Q Is it your opinion that a person of ordinary skill in the art would understand the phrase, "planarizing the top portion of the fourth dielectric layer," to mean etching the fourth dielectric layer using a resist mask?

A That would not be the first thing they think of. If they hear the word "in isolation" as you have hypothesized, they would normally think of tungsten etchback as an example or CMP, of course.

But in the context of the considerations here, trying to achieve in different ways the raised source drain function, they would recognize that as that surface evolves and moves down during etching, it will remain planar and it is making a new surface as it etches and that surface is planar and then follow it down and then it will contact then start evolving at the silicon nitride stop layer.

It is not the first thing they would

think about, but in the context of what is described here or in the prior art that I have cited, they will be perfectly comfortable, recognizing, "Oh, yes, duh, when we developed the etched process, the first thing we look at is the uniform and what is the etch rate."

And by uniform, I want to know it does the same thing every place and they realized, "Yes, that is a planarization."

Q The ordinary understanding of the term planarization as it is used in semiconductor fabrication is to create a planar or flat surface across the wafer using techniques like CPM or etchback, correct?

MR. MUKERJI: Objection, outside the scope. Also as to form.

THE WITNESS: I think it is important to understand the historical context planarization.

For many years it wasn't important because aspect ratios were small, so when people started thinking about planarization, first in etchback techniques, then in CMP they started thinking about, "Oh, we have to keep it flat and here are the techniques to

do it." That is what people normally think of first.

BY MR. CHEN:

Q You agree then that the ordinary understanding of the term planarization as used in semiconductor fabrication is to create a planar or flat surface across the wafer using techniques like CMP or etchback, right?

A No, I do not agree.

MR. MUKERJI: Objection, scope and form.

THE WITNESS: No, I do not agree.

BY MR. CHEN:

Q What is the ordinary understanding of the term planarization?

MR. MUKERJI: Objection to form. Hang on. Let's not talk over each other, that is first, and secondly, please don't interrupt his response.

MR. CHEN: I thought he was finished.

MR. MUKERJI: Were you finished? Complete your response and Mr. Chen will ask his next question.

THE WITNESS: I didn't get started actually.

BY MR. CHEN:

Q I thought you said you did not agree and then I thought you were done, so please continue.

A I do not agree. As I said a minute ago, the first thought that most people would have of ordinary skill would be something like etchback or CMP because that is when people started thinking about planarization as a term.

But I could point to the discussion in the prior art that I have cited - Nakamura - where they distinguish that there are reasons to try to make different levels of different structures at the same height and it has to do with lithographic depth of focus, so people also think of planarity alignment in-depth as an important function for lithography and it is used in the Nakamura Reference as one of the criteria for weighing which of the embodiments of a raised source drain might be more effective and more valuable.

People do think about planarity on the local level that I am talking about here.

May I add something to that? There's a really interesting example here. If someone hires my student to run a deposition tool or an etch tool and they talk about planarization they would probably think what most people would think first

from that term which is CMP or etchback and planarity and uniformity across a whole wafer, a long distance.

But if one of ordinary skill, as I have defined it here, has had enough experience to be exposed to these kinds of issues where lithography, etching, and deposition change the profile, the vertical profile, and the height of different structures, they won't be very sensitive to planarity as an issue as well.

That one of ordinary skill in the art would think about CMP, and etchback, but also about planarity and that's the issue that is important here.

Q Would a person of ordinary skill in the art reading the phrase "planarizing the top portion of the fourth dielectric layer," in the context of the '244 patent, think of the planarization term to mean forming a planar flat layer across layer, across the wafer?

A If someone were only looking at '244 and had not looked at prior art, for example, the prior art that I have cited here they would look at something like Fig. 4, absent the Resist 30, and they would think, "What '244 is trying to show

here is a global planarization," which is one way, as '244 shows, and is one of the embodiments in Nakamura show of achieving the raised source drain structure.

So I agree. They would think about CMP or etchback.

But that is if they are only looking at this one. If they were doing that blackboard exercise that we talked at length about earlier and trying to imagine there is another way to make this, maybe there is a better way to make it, maybe there is a way we can even ensure that things are planar at the end so we can do lithography properly, they could easily come up with the other descriptors of planarization that talk about local planarity associated with etching through using a resist mask.

Q What you said was, if a person of ordinary skill in the art is looking only at the '244 patent, that person of ordinary skill in the art would understand the term planarization to refer to creating the planar surface across the entire wafer, correct?

MR. MUKERJI: Objection to the form.

THE WITNESS: I think what I said was,

that would be the natural first thing to think about because the word planarization got popular before people started worrying about depth of field for fine line focusing in lithography.

If you were to ask the same person, "I have a resist mask in place. You have qualified the uniformity, the etch rate, so an anisotropic etch process, is it also planarizing the surface?" I think they would say yes because it does.

BY MR. CHEN:

Q It is your opinion that a person of ordinary skill in the art, looking at the '244 patent, would understand the term "planarizing the top portion of the fourth dielectric layer" to refer to etching the fourth dielectric layer using a resist mask, is that correct?

MR. MUKERJI: Objection to the form.

THE WITNESS: No.

BY MR. CHEN:

Q That is not correct, is it? It's your opinion that a person of ordinary skill in the art reading the '244 patent would understand the term "planarizing the top portion of the fourth

dielectric layer," to refer to creating a planar surface for the fourth dielectric layer across the wafer, correct?

MR. MUKERJI: Objection to the m.

THE WITNESS: Well, the '244 patent as you see in, what was it, Fig. 4, if you look at Fig. 4 and Figure 3, so the scope of what the '244 was considering, and they only read that, and they haven't read any of the prior art or thought about it, they would see in this case you start with a non-planar surface, you are going to planarize down and remove material that is an etching of some kind, down to the F-stop layer on the gate electrode, they would think of CMP or straight etchback across the wafer.

That is the first thing because the word "planarization" as used here, it is only in the context that doesn't involve the considerations that an alternative embodiment gets to the same function of raised source drain in prior art literature specifies.

BY MR. CHEN:

Q But is your opinion that if a person of ordinary skill looked at the prior art like

Nakamura, for example, they would then understand planarization to refer to etching using a resist mask?

A It depends on which embodiment they look at. Embodiment 3 looks a lot more like the '244.

Q A person of ordinary skill in the art looking at the prior art like Nakamura specifically looking at Embodiment 1, would then understand planarization to refer to etching using a resist mask, is that correct?

A I think this is somehow not the right order to look at this issue.

The people who developed the prior art were trying to achieve a certain result, a raised source drain structure, and to be consistent with the formation of the gate electrode, and all the constraints that one has if you do not want to totally change the technology, they are looking for a way to make this structure and to make it efficient.

They go to a blackboard. They start drawing these structures and the sequence of steps that would get them to the right structure and they would come to the situation which I depict on page 32 which includes an annotated version of

Fig. 2A of Nakamura, and they would talk about that, and they would say, "That will get us there."

That's the important thing because this is prior art.

If someone were to ask the question, "My guess is that if someone else is going to have another disclosure or patent later, and they are going to say it is important to planarize it, "Does this planarize it?' and their answer would be, yes, because it is a uniform etch process.

I am not trying to say that the first thought in the mind of such people would be uniformity of an etch process between pieces of resists.

I'm not trying to say that.

The first thought would be CMP and etchback, but when you're designing the prior art and you have no idea about '244, you could come up with this - and Nakamura did - one or more embodiments that will get there.

And if you ask, "What is really happening?" and what you think is a credible way to make the raised source drain structure, you would recognize that in the step of etching the

top of ILD Layer 26, you are also keeping it planar.

Q You're saying that a person of ordinary skill in the art looking at Nakamura Embodiment 1 would understand the term planarization or planarizing would refer to the etching process using the resist mask, correct?

MR. MUKERJI: Objection to the form.

THE WITNESS: You are looking at the summary of the invention, that is what we are talking about here, right, the language that you are trying to get to, is taken from summary of the invention.

BY MR. CHEN:

Q My question is about the term planarization?

A But you introduced exposing the portion of the third dielectic layer covering the gate electrode structure by planarizing the top portion of the fourth dielectric layer, right?

Q Yes.

A And we have now been talking about the meaning and context of the word planarizing.

Q Yes.

A Right?

Q Right.
A Sorry, so could you repeat your question.
Q You said that a person looking at Nakamura without reference to the '224 patent would understand that planarizing would encompass etching using a resist mask.
A That is not what I said. What I said was, if someone walked into that room where they are developing the ideas in Nakamura or people of ordinary skill were talking about the Nakamura, if someone walked in, and said, "What does planarization mean?" they would say, "Tungsten etchback, CMP, why do you ask?"
Someone on the team that has been talking to me about the Nakamura innovation, would say, "Oh, well, someone wondered whether we are planarizing here?" Someone would say, "Of course you are. You are etching." Right?
That is what they would say. But this is off track, I think, to what my job in the declaration is and outside the scope of my declaration because I was asked to determine whether I believe Nakamura teaching matches all of the claims, specifications --

I don't get these words right.

All of the claims in the '244, and if I look at Claim 1, for example, in the '224, it says, "removing the top portion of said fourth dielectric layer to expose a portion of said third dielectric layer covering said gate electrode structure."

I don't understand why we are having all of this discussion about the term planarization in the context of Nakamura Embodiment 1.

Q If the claim read, "Planarizing the fourth dielectric layer," would Nakamura Embodiment 1 meet that requirement?

MR. MUKERJI: Object to the form and outside the scope.

THE WITNESS: If it had the word planarize, yes, it would meet it, but it doesn't say that. So it is outside the scope.

BY MR. CHEN:

Q The reason you believe it would meet that limitation is because you believe that etching using the resist mask is a form of planarization?

A It is not because I believe. It is

because I know.

Q You know that because Nakamura teaches that?

A No. If someone had asked me in class when I am talking about lithography and etching and I am describing uniformity, they would ask me, "Is this local planarization what you're talking about, that region between the resist pieces?" I say, "Of course it is because we have to have etches that are uniform."

Q Do they have to say local planarization?

A They would ask the question. You have to say local because you are not talking about the horizon of the earth, or the 12-inches diameter of the wafer. You are talking about what happens between the resist pieces and that's the only place that is being etched.

Q They have to specifically tell you that they are referring to the portion between the resists?

A I don't think so. They would say, "When you're doing etching and you have a resist mask in place so you can make the etch cause patterning, is it planarizing?'.

I would think about it, and I would say,

"It is uniform, so it must be planarizing wherever things are not covered by resist," so between the resist and from this hole in the resist to that hole in the resist.

Q Does Nakamura use the term planarizing or planarization to refer to etching using a resist?

A I don't know. Do you want me to look? I just don't remember. I don't have a computer to do a search.

Q I will help you out. If you will look at Nakamura which is Exhibit 10, and you look at Column 10, which is a description, a continuation of the description of the first embodiment.

A Yes, of course, the word is used. It is a different part of first embodiment.

Q And it says there at Column 10, Line 16, "The surface of the insulation film may be planarized by CMP."

Do you see that?

A Right.

Q Is Nakamura using the term planarized in the more ordinary sense to refer to creating a flat surface across the entire wafer?

A Yes.

Q Does Nakamura use the term planarize to refer to the etching process where resist is used?

A I don't know the answer to that, I haven't looked for that. I would doubt it because people do not usually ask the question that way.

The only reason the question is being asked is that one embodiment which is shown in '244, describes the inclusion of a planarizing step, and in that case, that planarizing step can be global.

But if people were thinking about alternatives to make a raised source drain as they were in the invention of Nakamura, they think of other ways to do this, and if you get to that stage and then someone asks you a question, "Is that step planarizing?" you realize, yes, it is planarizing.

This is the kind of superfluous effort to understand whether the Nakamura teaching lines up with a piece of the specification in '244, that is really not the issue here, it is outside the scope.

I was asked to see if Nakamura teaches all the things that are in the claims.

Q You did not analyze whether Nakamura

teaches the claim which recites planarization of the fourth dielectric layer, correct?

A No, that is not true. I was asked whether to look carefully at the prior art and to look at the claims of the '244 and determine whether the prior art teaches all the things that are in the claims.

Q Did you determine? Did you provide an opinion whether Nakamura teaches a claim which recites the step of planarizing the top portion of the fourth dielectric layer?

A Yes, of course, because that is part of '244.

Q Then what were you saying about my question as being "outside the scope"?

A Let's look at the claims. Taking Claim 1 as an example, what Claim 1 says is: "Removing a top portion of said fourth dielectric layer to expose a portion of said third dielectric layer covering said gate electrode."

Well, you analyzed whether there is an embodiment in Nakamura that meets this for Embodiment 1, I realize, yes, it does that, and there is no requirement in this phrase that I just read for anything to be planarizing.

Q You did not analyze Nakamura to determine whether it meets a claim which requires the planarization of the fourth dielectric?

A Of course, I did. Wait. Where are you referring to in the Nakamura claim? I want to find it so I'm sure about this where it says "planarization of the fourth dielectric."

Q It doesn't say it in Nakamura.

A I'm sorry. In '244, that was the question.

Q I am asking you questions about planarization and you are saying that you think it is irrelevant because it is "outside the scope," correct?

MR. MUKERJI: Objection to the form.

THE WITNESS: I am saying that my task was to look at the claims in the '244 and determine whether prior art meets all of these claim limitations and that's what I did. If I look at these claims which part of '244 says planarization?

BY MR. CHEN:

Q Do you believe that the questions regarding planarization are outside the scope of your analysis of the '244 patent?

MR. MUKERJI: Objection to the form.

THE WITNESS: No, because they are embodiments that use planarization, global planarization with resist mask in place as part of an etch process.

BY MR. CHEN:

Q The '244 patent uses a term planarization or planarizing to refer to the ordinary understanding of planarizing which is to create a flat surface across the wafer, correct?

A In the specification, that is right.

Q And Nakamura also uses a term planarization or planarizing to refer to the ordinary understanding which is to create the flat surface across the wafer, correct?

A In large part, yes.

Q You agree that the ordinary understanding of planarization includes processes like CMP or etchback, correct?

MR. MUKERJI: Objection to the form.

THE WITNESS: In the absence of context, the first thing that that word would suggest to someone is global planarization, I agree with that.

BY MR. CHEN:

Q Global planarization would be performed by techniques like CMP or etchback, correct?
A Yes.
Q And you would not conduct global planarization with a resist mask in place, correct?
A No, that is not true.
MR. MUKERJI: Objection to the form.
THE WITNESS: No, that is not true. If I am doing etching, and I have qualified the etch process as being uniform across the wafer, which I need to do in manufacturing, then the etching is also going to be planarizing the surface that is being removed.
BY MR. CHEN:
Q But that is not global planarization, correct?
A Sure it is. It goes from one side of the wafer to another.
Q Where is your resist?
A The etch process to first order doesn't affect the resist, so wherever the etch process happens is the same, so it is globally planar.
Q Is that creating a flat surface across

the wafer?

A The new surface is a flat surface. What is the right word for that? Island? Something like that. I mean it doesn't cover the entire. The new surface does not cover the entire surface.

Q You used the term "global planarization" to refer to the ordinary understanding.

A Yes.

Q Which is to create the flat surface across the wafer?

A Across all of the wafer?

Q Yes.

A Yes.

Q That's how I was using the term.

A Oh, okay. Let's call it Global 1, meaning, each and every place on the wafer, and Global 2 means is it uniform across the wafer wherever it exists and I will say that that is what etching does.

Q You have used another term, "local planarization" to refer to etching with a mask, do you recall that?

A Yes, it was for convenience. I am talking about an etch process in the presence of a photoresist.

Q Let's just use global planarization to mean the ordinary understanding which is to create the flat surface across the wafer and then we can use "local planarization" to refer to "etching using a resist," is that fair?

A But the local planarization can be uniform at the appropriate points across the wafer.

Q Between the resists?

A Yes.

Q For global planarization you would not perform that with a resist in place, correct?

A Global planarization by the standard techniques for "across wafer" process would not be done nor aligned with resist in place.

MR. CHEN: Why don't we take a break.

(Whereupon, a break in the proceedings commenced at 11:35 a.m. and on resuming at 11:48 a.m.)

BY MR. CHEN:

Q Dr. Rubloff, I have a question regarding the etch process using a resist as a mask.

When you are performing etching with a resist and the resist has a pattern in it, let's take for example it has a pattern, it as a hole, and you're etching within the hole, is the etch

rate at the center of that hole the same as the etch rate towards the edges of the hole close to the resist?

MR. MUKERJI: Objection to the form.

THE WITNESS: You are speaking in generality about anisotropic etching?

BY MR. CHEN:

Q Let's talk about anisotropic etching, yes.

A The ideal situation is certainly a worthy goal of someone doing process development on etch or equipment design, for etch is to make that happen to make it uniform.

But when you look at the chemistry and physics of the etch process, it is always more complicated than that.

I mentioned I think yesterday that these chemistries lead to reaction products that are deposited on sidewalls, that changes the profile of essentially the mask as you go down, as you transfer the mask down through the material you are etching, if you are depositing on the side wall, then now you have made a new mask and so these things are a lot more complicated in reality.

Then the question I should also add is what do you mean when you say "same rate at the edge of the hole," as compared to the center?

You need a quantitative expression of that. I mean, what would it take to say, yes, it is the same. One percent uniformity? 10 percent? Do you have a number in mind?

Q No, I mean "the same" as in "exactly the same."

A That is a word I never use, not in real life.

Q So the rate is different, but within a range. Is that what you're saying?

A Think about how the etch process works, it is different on different length scales for different reasons, so if it were varying by a factor of 20 percent or 100 percent or 1,000 percent, you probably would not find it very useful.

Then there is another scale at which you realize that every time atoms are removed they happen essentially one at a time, an ion hits this location, that atom leaves, so there is statistical distribution as well. These things are part of the context of your question.

Q The problem that you are having with answering the question, is it the word "same" or is it "etch rate"?

MR. MUKERJI: Objection.

BY MR. CHEN:

Q I want to understand. What is your difficulty in providing an answer?

MR. MUKERJI: Objection to the form.

THE WITNESS: Are you asking if the etch rate at the center and at the edge is the same?

BY MR. CHEN:

Q Yes.

A And therefore the vertical profile of the bottom would be flat?

Q Yes.

A And "same" means "exactly the same"?

Q Yes.

A On average the same. What does it mean?

Q Exactly the same.

A To how many decimal points?

Q (No response.)

A As I said, I never use the word exact because it doesn't work that day.

Q To measurable decimal points.

A Of the order of what? One percent?
Q Is it one percent different?
A No, I am asking you.
Q I am asking you about the etch rate. Is it one percent different?
A It depends on the process and without being specific, I can't make an estimate and I don't have a comprehensive knowledge of every process and, I am sorry to say, the situation is even more complicated and worse than that because etching, anisotropic etching whichever process you are talking about, bromine based, chlorine based, fluorine based, and so on, typically use several gases, they are a very complex chemistry and the performance depends on the equipment you are using.

In the worst case, if I buy a Lam Etcher Model XXX and I buy another Lam Etcher Model XXX, I probably will not get exactly the same result in those two tools.

Q Are you saying that without knowing all of those specifics, the type of tool, the type of etching, the number of decimal places, all of these specific parameters you cannot answer whether etching using a resist mask will have a

different etch rate within the spaces in the resist as opposed to near the edges of the resist?

A I can answer it. It's just a broader answer than what I think you're trying to ask from me.

Q What is your answer?

A What you would like to have in practice is the ability to etch down through a single material and have at essentially the same etch rate across that region from center to edge, to within you would like to have a percent or something like that, you might end up with, I don't know, 10 percent or something like that.

That is going through the same material and that is for a goal, that is what you would like to have.

If you're actually going to use it in practice that is probably what you need but it depends a little bit on the application.

Q The etch rate in the center is roughly 10 percent faster than the etch rate towards the edges of the hole?

A That is not what I said.

Q What did you mean when you said 10 percent?

A I don't know how much you have looked at what are called SEM cross-sections, so when you're trying to understand an etch process you are developing what is called a vertical profile.

Imagine you take the sample and you etch a hole down into it, and then you cut it vertically, you take that half of the sample, and you put it in an electron microscope, you look at the profile of the material you have just etched, and as I said, it may taper because there is sidewall deposition and all kinds of other stuff, it may have a flat bottom, but it will probably have some distribution.

It can be concave up. It can be concave down. It can have corners that are features that you didn't expect where it gets a little bit wider.

There are many different variations that are observed in the practice of etching like that. That's why it is so difficult to give you simple answers to the questions you are posing about etch.

Q What did you mean when you said in response to my question about whether the etch rate in the center is the same as the etch rate

near the edge, what did you mean when you said you might end with, "I don't know, 10 percent," or something like that?

A I am just trying to give a ballpark estimate.

Q What did that 10 percent refer to?

A For example, if I did an SEM cross-section measurement, and I quantify what the shape of the vertical profile is and I look at the two edges and then I make a depth measurement across from one etch to the other, and if I were to take the RMS value of deviation from the exact same number from the average, let's say it might be something like 10 percent or it could be 2 percent, or I guess there are configurations that could be 20 percent, I don't know.

I mean, I have seen a lot of SEM cross-sections and none of them look like the pictures we draw, but on average they look like what you want them to or we wouldn't have the technology.

Q Are you saying that in practice the result of the etch at the bottom of the hole will always have some contour?

A Well, it always has some shape and it

may be flatter and more ideal looking or it may be more deviation from that.

Q That depends on the process you used and the number of other parameters?

A Yes, and the equipment, and the gases and the temperature.

I assume there is a specific application that you have in mind for wanting to understand how I think about that question.

Q We were talking about etching with a mask previously before the break and I just wanted to understand some more details about that process.

We can turn back to the '244 patent, Exhibit 9.

A You said Column 9?

Q No, Exhibit 9. We are going to look at Column 6. Look at Claim 1 that begins at Column 6, Line 28.

A Yes.

Q We covered this a little bit before. It is your opinion that the step of removing a top portion of said fourth dielectric layer to expose a portion of said third dielectric layer covering said gate electrode structure, and the step of

forming on the substrate a pattern second resist layer to mask portions of the fourth dielectric layer," it is your opinion that those two steps could be performed in a different order from how they are listed in the Claim 1?

MR. MUKERJI: Objection to the form.

BY MR. CHEN:

Q Is that correct?

A It is my opinion as I described in the declaration, that prior art of Nakamura Embodiment 1, meets the limitations of Claim 1 and actually does use a different order of those two.

Q I'm asking you about your interpretation of Claim 1. Is it your opinion that Claim 1 can be interpreted so that the step that begins with removing a top portion of said fourth dielectric layer can be performed after the step of forming on the substrate a pattern resist layer?

A Yes, it can be done that way and I was taught that by Nakamura.

Q So the reason that you have that understanding of Claim 1 is because you referenced Nakamura?

MR. MUKERJI: Objection to the form.

THE WITNESS: I wouldn't have any reason

to think about it or to knock Nakamura if I hadn't been asked to compare prior art to '244 so I wouldn't have thought about it and unless I had been interested in making the raised source drain, developing a process flow, and structure to make a raised source drain, and spent some time thinking about that and having a blackboard and making little drawings and musing about it, of course, I wouldn't have thought about what order in which to do these and I work in different things. I don't do this.

BY MR. CHEN:

Q So you came up with your understanding that those two steps could be performed in reverse from the order in which they are listed in a claim based on your understanding of the Nakamura reference, is that correct?

MR. MUKERJI: Objection to form.

THE WITNESS: In part at least, maybe in total, I haven't thought about that. But certainly that possibility comes out clearly from Nakamura.

BY MR. CHEN:

Q If you were to perform the steps listed

in Claim 1, and you performed the step of forming on the substrate a pattern second resist layer to mask portions of the fourth dielectric layer, before you performed the step of removing a top portion of said fourth dielectric layer to expose a portion of said third dielectric layer covering said gate electrode structure, would you end up with a structure that is different from the structure you would have if you performed the steps in the order in which they are listed?

A Yes. That is shown in my paragraph 121 which compares Figs. 2C and 6B from Nakamura.

Q Which paragraph are you referring to?

A 121, page 40.

Q I think that is paragraph A-28.

A Oh, I'm sorry.

Q Moving down to Claim 1, if you will look at the step that begins at Column 6, Line 53.

A We are on '244 now.

Q Yes.

A Column 6, Line 53.

Q Yes.

A Yes.

Q You see it says, "Removing said fourth dielectric layer other than said portions masked

by said second resist layer to form a plurality of trenches adjacent to said gate electrode structure," do you see where it says that?

A Yes.

Q Would you agree that that clause recites the specific step for "removing said fourth dielectric layer using the resist mask?"

A Well, it uses the second resist layer as a mask to etch away the fourth dielectric layer.

Q You see following that clause there is the phrase, "Wherein portions of the substrate are exposed."

A Yes.

Q What is your understanding of that clause where it says, "Wherein portions of the substrate are exposed"?

A Yes, that's all in my disclosure in my declaration. I thought hard about this question because I knew the interpretation is important.

Starting in paragraph 23, I was asked what would be the broadest reasonable interpretation of "at the same time" here to understand what this means.

I will just read you what I said and I can then embellish as you need.

"At the same time it would be broad enough to cover the same measured to measurable period during which an etching process continues.

"I believe it would because it is not inconsistent with '244 specifications and one of ordinary skill would understand it this way."

Then there is more about time as in a dictionary. "Time is the measured to measurable period during which an action process or condition exists or continues."

So "at the same time" is construable to mean the same period in which something is happening.

I consider that the clause that you read is the clause that is where the etch process is taking place.

"In considering what the measured or measurable period and action process or condition are, a person of ordinary skill in the art would turn to the claims and the specification for context.

"The specification of the '244 patent does not use the term 'at the same time' and the only recitations of 'at the same time' are in Claims, 1, 14, and 16 where the term comes after

the phrase, 'wherein spacers are formed on sidewalls of the gate electrode structure.'

"This phrase is separated --

Now this part is confusing because you have to parse the punctuation, but I have gone through that in detail and reviewed it recently.

"This phrase is separated by a comma from other phrases that are listed between the two; so removing said fourth dielectric layer other than said portions masked by said resist layer to form a plurality of trenches adjacent to said gate electrode and wherein portions of the substrate are exposed.

"Based on the language of the claim, it appears to me that the term 'at the same time' could only refer to, (1), the phrase 'wherein spacers are formed on the side walls of the gate electrode,' okay, and that means all of the spacers, "or to refer to all three of the phrases listed between the successive semicolons.

"However, the term 'at the same time' would not appear to refer to only the phrases wherein spacers are formed on sidewalls of the gate electrode structure and wherein portions of the substrate are exposed to additional

punctuation or other indication that distinguishes these two phrases from the phrase removing said fourth dielectric layer' other than said portions masked by said second resist layer to form a plurality of trenches adjacent to said gate electrode structure.

"Thus, the term 'at same the time' would appear in either the last phrase of the list or all three.

"In the case that the term 'at the same time' refers only to the phrase 'wherein spacers are formed on sidewalls of the gate electrode structure' the term 'at the same time' would require that each of the spacers be formed on sidewalls of the gate electrode structure during the same measured or measurable period during which an action process or condition exists or continues.'"

I am sorry, but I need to get a drink.

"Alternatively, in the case of the term 'at the same time' refers to all three of the phrases listed between the successive semicolons, the term 'at the same time' would require that during the same measured or measurable period during which an action, process, or condition

exists or continues; (1), said fourth dielectric layer other than said portions masked by said second resist layer be removed to form a plurality of trenches adjacent to gate electrode structure.

"(2), portions of the substrate be exposed.

"And (3), spacers be formed on the sidewalls of the gate electrode structure.

"In either case the '244 patent describes an anisotropic etching process is utilized to remove the unmasked fourth dielectric Layer 28 located under Areas 31A and 31B.

"This anisotropic process also removes the portion of the third dielectric Layer 26 on top of the gate electrode structure 27."

Exhibit 1001, paragraph 5, Lines 25 to 30, emphasis is added.

"According to the '244 patent, the entire duration of this anisotropic etching process is required to remove the said fourth dielectric layer other than said portions masked by said second resist layer to exposed portions of the substrate.

And (3), form spacers on sidewalls of the gate electrode structure.

"In fact, as illustrated in the following annotation of the '244 patent's Fig. 4, no portion of the substrate is exposed until the very end of the anisotropic process, i.e., after the fourth dielectric layer and then the third dielectric layer are removed."

Let me see if I need to go further. Yes, this gets long. But I would like to have it specific in the record.

"29. Moreover, etching occurs at a certain rate due to the exposure of a material to an etchant. See Exhibit 1006 pages 77 to 79.

"By its very nature any anisotropic etching process would eat away at a certain rate the fourth dielectric and then the third dielectric layer starting from the exposed areas 31A and 31B showing Fig. 4 and working vertically downward to the surface of the Substrate 10.

"Thus, as shown in the following annotation of Fig. 5 of the '244 patent, the formation of the sidewalls highlighted in yellow would occur through this anisotropic etching process because they would be exposed as the etching process worked vertically downward.

"30, the '244 patent does not indicate

the number of actions that are operations that are part of the above described anisotropic etching process or the amount of time over which it takes."

THE WITNESS: If you are going to look at this anyway later, I can probably skip the dictionary and pages stuff. Is everybody okay with that?

THE REPORTER: Counsel is nodding?

MR. CHEN: Yes, I am okay with him skipping the citations.

THE WITNESS: The reporter would be happy for me to skip through them. Me too.

"Moreover, independent Claims 1, 14, and 16, do not appear to limit the removing of said fourth dielectric layer to anisotropic etching.

"Thus the action process or condition that defines the period during which the above noted claim phrases are considered to occur is an etching process which may include multiple actions or operations."

Parenthetically, let me add that we had this discussion earlier about a process step typically has substeps in it as well.

Going back to the text.

"31, in view of the foregoing, I believe the broadest reasonable interpretation of 'at the same time' is the same measured to measurable period during which an etching process continues.

"When applied to the claims in which is resided the term 'at the same time' is broad enough to encompass either that, (1), that each of the spacers are formed on sidewalls of the gate electrode structure during the same etching process, or (2), that during the same etching process,

"(a), said fourth dielectric layer, other than said portions masked by said second resist layer is removed to form a plurality of trenches adjacent to said gate electrodes.

"(b) portions of the substrate are exposed.

"And (c), spacers are formed on the sidewalls of the gate electrode structure.

"32, I have considered whether a broadest reasonable interpretation of the claims would require the steps of 'removing a

top portion of said second or fourth, depending on which claim we are talking about, dielectric layer to expose a portion of said first or third dielectric layer covering gate electrode structure and 'forming on the substrate a patterned second resist layer to masked portions of said the second fourth dielectric be performed in that particular order.

"In light of the claim language, I do not believe one of ordinary skill in the art would ascribe a specific order to these steps."

BY MR. CHEN:

Q Dr. Rubloff, if I might interrupt you for a second.

A Yes.

Q I think the portion of your declaration that relates to the construction of 'at the same time' ended with paragraph 31. I believe paragraph 32 you have moved on to a different topic.

That is not correct.

A But I was trying to deal with the fact that part of the claim that you asked me to

address includes the 'at the same time' part, but it also includes the question of what happens during a process.

Q I am sorry, I did not know what --

A I was trying to get to the right thing.

Q Please continue. You already read 32.

A Thank you. "33, in Claims 1, 14, and 16, the step of forming on the substrate a patterned second resist layer does not include any language that it would imply, it should be performed after the step of removing a top portion of said dielectric layer, the second fourth dielectric layer.

"For example, the forming step does not mention details recited in the removing steps such as removed top portion or the exposed portion of said first third dielectric layer.

"Rather the forming step simply recites that the patterned second or second resist layer is formed on the substrate."

I think we are almost there.

"Moreover, Claims 4 and 15 explicitly use temporal language wherein said step comprises two consecutive steps of which the independent claims do not.

"In fact the independent claims themselves use the word sequentially to define a temporal relationship between the deposition of dielectric layers, i.e., depositing sequentially a first third dielectric layer and a second fourth dielectric layer on said substrate and said gate electrode structure.

"The above noted removing in forming steps do not contain any temporal language of this kind.

"35, accordingly, I do not believe that the broadest reasonable interpretation of the claims would require that the steps of 'removing a top portion of said second or fourth dielectric layer to expose a portion of said first or third dielectric layer recovering said gate electrode structure' and 'forming on the substrate a patterned second resist layer to masked portions of said the second fourth dielectric layer to be performed in the particular order."

Q Are you finished?

A I am finished reading. Did I answer your question?

Q Not to my understanding. I will repeat the question with a copy of that. The answer is

simply a recitation of a number of pages from your declaration.

You can just say, "I have nothing more to say than what is in my declaration," without just reading it all into the record, if that helps you.

If you want to read it all again, that is up to you. So my question was: Looking at the limitation that begins with removing said fourth dielectric layer other than said portions masked by the second resist layer," do you see that?

A Yes.

Q We agree that that clause there recites a step for removing the fourth dielectric layer using the resist mask, correct?

A The clause up to the comma?

Q Yes.

A Yes.

Q My question was: Following the comma, there is another phrase that says, "Wherein portions of the substrate are exposed." Do you see that?

A Yes.

Q My question was: "What is your understanding of that clause wherein portions of

the substrate are exposed?"

A My understanding of, is it a paragraph of three things are with two "whereins" and 'at the same time' this is describing what happens in a single etch step using the resist layer to drill through the two layers of dielectric.

Q The clause, "Wherein portions of the substrate are exposed," is something that has to occur during the step of "removing said fourth dielectric layer other than said portions masked by the said second resist layer," correct?

A Yes.

Q And this next clause, "Wherein spacers are formed on the side walls of the gate electrode structure at the same time," isn't something else that also has to occur during the step of "removing said fourth dielectric layer other than said portions masked by said second resist layer," correct?

A As in all three of those things should be part of the etch step.

Q The etch step where you use the resist as a mask, correct?

A Yes.

Q Before you had stated that it is your

opinion that Nakamura Embodiment 1 satisfies all the limitations of Claim 1, correct?

A Yes.

Q In Nakamura you believe Nakamura Embodiment 1 satisfies all the limitations of Claim 1 because it performs all of the steps listed in Claim 1, correct?

A That is correct.

Q Would Nakamura Embodiment 1 satisfy all the limitations of Claim 1 if it did not perform the step of "removing a top portion of said fourth dielectric layer to expose a portion of said third dielectric layer covering said gate electrode structure?"

MR. MUKERJI: Objection to form.

THE WITNESS: You are asking whether if it didn't meet part of this paragraph, the removing part, it will not meet that claim, is that right?

BY MR. CHEN:

Q Yes.

A Well, the question is: Does Nakamura do what is said here which is to do three things in a single etch step, right, and so if it doesn't do the three things, it does not need it.

Q Sorry. Were you finished?
A Did you want to rephrase the question?
Q I was referring to a different limitation. I think you were looking at the --
A Which one are you referring to?
Q I was referring to the one above it, "removing a top portion of said fourth dielectric layer to expose a portion of said third dielectric layer covering said gate electrode structure," so I will reask the question.

Would Nakamura Embodiment 1 meet all the limitations of Claim 1 if it did not perform that step which begins with "removing a top portion of said fourth dielectric layer"?

MR. MUKERJI: Objection to the form.

THE WITNESS: Nakamura Embodiment 1 you are asking about?

BY MR. CHEN:

Q Yes.
A Just this one? It has to meet the claim limitations, so if it doesn't meet one of the claim limitations then it doesn't meet it.
Q So if it did not perform that step then it would not meet all the limitations of Claim 1, correct?

A If it didn't achieve what it wanted the claim limitations specifies, then it wouldn't meet the claim. Sounds a bit like a cytology.

Q Are you drawing a distinction between achieving and performing?

A (No answer.)

Q My question was: If it did not perform all the steps listed in the claim, then it would not meet the claim limitation, correct?

A The claim limitation is what is written there, so Nakamura Embodiment 1 either does all of these things or it doesn't.

Q If Nakamura Embodiment 1 did not perform the step of "removing a top portion of said fourth dielectric layer to expose a portion of said fourth dielectric layer covering said gate electrode structure," then it would not meet all the limitations of Claim 1, correct?

A The way you phrased it made it sound like this is a separate step. The function is what is important.

But the claim limitation says is, you have to have a process and process flow which removes "the top portion of said fourth dielectric layer to expose a portion of said third dielectric

layer covering the gate electrode structure."

That may be accomplished while other things are being accomplished, so I wouldn't call it "the steps of."

Q Is it your opinion that the limitations in Claim 1 do not recite steps?

A I did not say that. They recite functions. It could be accomplished in steps. They say what they say. I can ask the question, did I do in removing the second dielectric layer, did I deposit sequentially a third dielectric layer, and so on, it either meets or it doesn't whether you call it a step or not.

Q I want to understand how you understand Claim 1. Are each of those limitations steps or just functions?

MR. MUKERJI: Objection, form.

THE WITNESS: They are what they are. I don't know what else to say. It either does what the language says or it doesn't.

BY MR. CHEN:

Q Right.

A I don't want to try to classify steps or functions or something because this prescribes what the Claim is talking about.

Q Does the Claim require certain steps to be performed or does it only require that certain functions are achieved?

MR. MUKERJI: Objection to the form.

THE WITNESS: It requires what the words say. I have no other answer for you.

BY MR. CHEN:

Q You don't have an opinion whether the claims require steps or functions?

A I don't think that is a relevant question that I need to have an opinion about in order to make the judgment as to whether the prior art meets the Claim limitations of '244.

Q Did you form an opinion as to whether the Claim requires a series of steps or just functions?

MR. MUKERJI: Objection to the form.

THE WITNESS: Everything in this domain is carried out in steps. How they are organized give different functions may cloud the distinction between those two terms, but the language of the claim is what is at issue here and that is the only thing I am looking at.

BY MR. CHEN:

Q Right, and so the language of the Claim, and let's look specifically at one limitation within Claim 1, the language, "Removing a top portion of said fourth dielectric layer to expose a portion of said third dielectric layer covering said gate electrode structure," does that limitation recite a step?

A I think I have answered that question.

Q What is your answer?

A My answer is I can't answer it because it is irrelevant to the question at hand. It is outside the scope of my investigation. There was no reason I needed to go through --

In order to determine whether there was prior art which meets all the Claim limitations of '244, I did not have to invent a categorization of the Claim limitations as steps or functions or anything like that. I only have to answer the plain question.

Q In determining whether the prior art met all the limitations you did not determine whether the prior art performed all the steps listed in Claim 1?

MR. MUKERJI: Objection to the form.

THE WITNESS: That's kind of a trick

question because you inserted "step" in the middle of a description of a Claim limitation and I already said that I analyzed whether all the things here have been done and taught in the prior art.

BY MR. CHEN:

Q Right.

A But I did not go through a categorization of steps.

Q What I want to understand is how you read the Claim. When you were reading the Claim in the '244 patent, did you make a determination as to whether the limitations recited steps or not?

A As to whether the limitations recited steps, no, I don't consider except in situations like the clause which has at the same time, that tells me these things have to happen as part of something together, but other than that, I did not go through a classification of steps.

I went through to see, "Does it do what the words say?"

Q You did not determine whether the limitation "removing a top portion of said fourth dielectric layer to expose a portion of said third

dielectric layer covering said gate electrode structure," is a step in a process or not?

A I know exactly what the words say. I know what it means whether it is happening or not.

But I didn't worry about whether it is a step, a separate step, a substep of a process.

As I said, I have not attempted to make a hierarchical categorization like it seems you are looking for.

Q But you would agree that the limitations refer to something that must be performed in the process, correct?

A Yes, or achieved or a function. If I remove material, I have achieved something. If I removed material, I have carried out a function, whether it is a step or a separate step, or a substep, that is not what the Claims talk about because they do not have this temporal character except as the ones I have pointed out in my declaration.

Q If Nakamura Embodiment 1 did not perform, "removing a top portion of said fourth dielectric layer to expose a portion of said third dielectric layer covering said gate electrode structure," then it would not have met all the

limitations of Claim 1, correct?
A Yes.
MR. MUKERJI: Objection to the form.
THE WITNESS: It has to do what it says in each limitation.
And it does.
BY MR. CHEN:
Q If you look at the top of Claim 1.
A Claim 1.
Q Claim 1, yes, do you see the first clause, it is typically called the preamble. This is at Column 6, Line 28.
You see how it says, "A process of fabricating on a substrate a semiconductor device having a raised source, a raised drain, and a gate electrode structure comprising the steps of:" Do you see that?
A Yes.
Q Did you read that clause?
A Yes.
Q When you were coming up with your understanding of Claim 1?
A Yes.
Q What is your understanding of the phrase "comprising the steps of"?

A Well, at "forming, forming, forming, removing, depositing," and so on, all have to be in therein whatever is the prior art if it is to meet this claim limitation.

Q Does the phrase "comprising the steps of" mean that each of those limitations in Claim 1 are separate steps?

MR. MUKERJI: Objection to the form.

THE WITNESS: That would depend on how to interpret the word steps, and as I have said before, its process is typically having substeps and we already recognized that the order here is not important.

It is in the constraint of the claims and that in some cases things have to happen together, that comes later at the same time, but I do not take "comprising the steps of" as a formal designation of separate steps. It is the function that has to be met for the result.

BY MR. CHEN:

Q It is your opinion that each of those limitations that came with forming, forming, forming, removing, depositing, removing, forming, removing, filling, doping, driving, each of those

limitations are not separate steps?

MR. MUKERJI: Objection to form.

THE WITNESS: You can call them steps, but this doesn't tell me if they are separate steps.

BY MR. CHEN:

Q Does the Claim call them steps?

A The Claim calls them steps, but I think that is a convenient way of saying they could have easily have said "comprising the following functions."

The following actions.

I don't read it as literally requiring that these be "separate steps."

Q When you were interpreting the claim, even though the Claim said "comprising the steps of," you did not read the limitations that each be separate steps?

A I look at them as requirements. I am not an attorney. I am a researcher and I am only trying to see whether prior art matches on to achieving all of these things.

Q Before you analyzed whether the prior art matched up with achieving all of these things, you did form an understanding of what the Claim

meant, correct?

A Sure.

Q When you formed your understanding of what the Claim meant you did not interpret each of the limitations within the claim as being separate steps, correct?

A Where I have dealt with patents and the claims in patents, I usually see a list like this and the question that comes up immediately, this is a listing of the pieces that have to be in that claim and where I see that, the question that immediately comes up, "Is there a sequence that is required here?" And I never read the steps as anything as a formal designation.

Q Ignoring the issue of whether they need to be in a specific sequence, did you interpret each of the limitations as each being a separate step?

MR. MUKERJI: Objection to form.

THE WITNESS: I interpreted each one of these as a descriptor for what has to happen according to the prescription of the authors of the claim, and so whatever it says, my question is, "Does prior art do the same thing?" That is all.

BY MR. CHEN:
Q Even though the claim says "comprising the steps of."
A Yes.
Q You would not interpret each of the limitations as being separate steps within a process?
MR. MUKERJI: Objection to the form.
THE WITNESS: I don't think that is relevant or necessary to do that in order to understand whether the claim limitations are being met.
BY MR. CHEN:
Q So you did not do that?
MR. MUKERJI: Objection to the form.
BY MR. CHEN:
Q Correct?
A No, I don't know. I do not have an answer to that.
Q You must know whether you interpreted each of the limitations as separate steps or not, right?
MR. MUKERJI: Objection to form.
THE WITNESS: I read the claims as they are written. That is really all I have to

say about this.
BY MR. CHEN:
Q You cannot answer yes or no whether you interpreted the Claims limitations to each refer to a separate step?
MR. MUKERJI: This is now bordering on harassing the witness. I have been sitting here counting. This is the seventh time. He has answered the question. I think we need to move on.
MR. CHEN: Let me read you his answer because it is a yes or no question of whether he interpreted the limitations in a certain way.
He can either say yes or he can say no and he is not saying any of those things. He is providing other.
MR. MUKERJI: You view it as a yes or no question. He may not view it the same way. He gave you his answer. Let's move on.
BY MR. CHEN:
Q Is it your response that you cannot provide a yes or no answer to my question?
A I can't provide a yes or no answer because the question is irrelevant to the exercise

that I did.

I analyzed the Claim. I looked at the prior art. I asked whether things taught in the prior art accomplish the things that are listed here.

Whether these are separate steps or not doesn't matter because there is nothing which tells me that they have to be separate steps.

You can call them steps, but "separate steps" is a different issue. I can't answer your question.

MR. CHEN: Why not we break for lunch. It is 12:35.

(Whereupon, a break in the proceedings commenced at 12:35 p.m. And on resuming at 1:30 p.m.)

AFTERNOON SESSION

BY MR. CHEN:

Q Dr. Rubloff, let's look at the Nakamura reference, Exhibit 10. Now you rely on the Nakamura reference to support your opinion that the '244 patent is invalid, correct?

A Yes.

Q Nakamura describes a number of different embodiments, correct?

A Yes.

Q And you provided opinions related to the first and third embodiments, correct?
A That is correct.
Q You are not relying on any of the other embodiments in Nakamura to form the basis of your opinion that the '244 patent is invalid, correct?
A No.
Q No, as in that is not correct, or no, you are not relying on any other embodiments?
A Sorry. It is not correct. No.
Q You are relying on other embodiments?
A On some others.
Q What other embodiments are you relying on?
A Most specifically, Embodiment 4 is where the Diopine distribution and diffusion to form the raised source drain is described.
Q Where is your reliance on Embodiment 4 disclosed in your declaration?
A It is quoted. Here we are. I think it is, for example, Column 15.
Q Paragraph 15 or what are you referring to?
A The Nakamura patent.
Q Where in your declaration are you

looking at?

A A-30. If you start at Line 31 or 32. "The electrodes 42, 44 are formed of the conducting film material having a large Diopine impurity diffusion coefficient, e.g., polycrystalline silicon, morphosilicon, metalsilicide that is subjected to suitable thermal treatment to diffuse the Diopine impurity from the electrodes 42, 44 into the silicon substrate to thereby form the source drain diffused layer," and so on.

Q Is that portion specific to Embodiment 4 or is that just a portion in the patent that is referring to all of the embodiments that are described?

A Well, the wording at the start of the fourth embodiment builds on the third embodiment, but I haven't looked closely recently at where it applies to the other embodiments.

I think it is fairly general.

The whole specification does have a number of embodiments, but the structure is made and the raised source drain diffusion part is described in the fourth embodiment.

Q In paragraph A-30 that you just

referenced, the first line.

A Sorry.

Q A-30 in your declaration.

A Yes.

Q This is the portion that you said is referring to Embodiment 4, correct?

A No, it is listed under Embodiment 4. Embodiment 4 starts its discussion, "The same numbers of the embodiment is a method for fabricating semiconductor device according to the first and third embodiments are represented by the same reference numbers, not to repeat or to simplify their explanation.

"Figs. 7A and 7B are sectional views," and then it goes on to describe, "and the method for fabricating a semiconductor device according to third embodiment, the electrodes are formed," et cetera," and then gets down to the diffusion of dopants.

Q But referring to your declaration.

A Yes.

Q Paragraph A-30, you are quoting from a portion of the patent which I believe you just read a portion of, and you have added the annotation after, "in the above described

embodiments," you added, "e.g. the first and third embodiments."

A Yes.

Q Does that mean that you believe that the quoted portion from the patent, from Column 15, Lines 25 to 31 should be applied to the first and third embodiments?

A Yes.

Q In your declaration you only discuss the first and third embodiments with reference to meeting the limitations of the Claims of the '244 patent, correct?

A That is right.

Q You did not provide an opinion as to whether the fourth embodiment in Nakamura meets the limitations of the Claims of the '244 patent, correct?

A Embodiment 1 and Embodiment 3 meet most of the limitations of Claim 1, for example, and taken together with the fourth embodiment that describes the formation of the source drain diffusion area, together those meet, 1 and 4 or 3 and 4, meet the Claim limitations.

Q You are not relying on Embodiment 2 to support your opinion that the limitations of the

'244 patent, the limitations of the claims of the '224 patent are met, correct?

A I don't know the answer to that unless I look carefully at Embodiment 2.

I read it earlier, but decided that 1 and 3 and the quote from 4 is all that is necessary.

Q In your declaration you did not provide an opinion regarding whether Embodiment 2 meets the limitations of the claims of the '224 patent, correct?

A Yes, I didn't address Embodiment 2.

Q Do you believe that the quoted portion of the Nakamura specification, the portion that you quoted in paragraph A-30, that portion is actually a description specifically directed at Embodiment 4?

A That's a description of the teaching which lines up with the last limitation of Claim 1, for example, "Driving said dopants into the substrate underneath said trenches to form said raised source and raised drain. "

Q You are referring to the '224 patent?

A Yes, right, I am sorry.

Q My question was: Whether that portion

in the Nakamura specification is talking about Embodiment 4 or was it talking about all of the other embodiments listed above, 1, 2, 3 or 4?

A In Nakamura?

Q In Nakamura.

A It is clear that that is a concise description of the formation of the shallow layer would be applicable to any region that allows for a doped material to reside just above the crystalline silicon surface and in particular Embodiment 1 and Embodiment 3 and there may be other places where it is applicable as well.

Q So that portion is applicable to all of the embodiments that were listed in Nakamura, correct?

A I haven't concentrated on that recently. I would have to look in detail.

Q But that portion of the specification is definitely applicable to Nakamura Embodiments 1 and 3, correct?

A Yes.

Q Other than the portion that we are just talking about, where it is describing the diffusion of the source drain regions, you did not analyze ...

MR. CHEN: Let me start over.

BY MR. CHEN:

Q Other than the portion that we just mentioned which begins at Column 15, Line 25, and extends down through Column 15, Line 46, you did not analyze any other part of Embodiment 4 to determine whether it meets the limitations of the claims of the '244 patent, correct?

A Let me re-read the fourth embodiment to see if I can say that or not. I mean I have read it all.

Q The reason I ask is because you did not mention Embodiment 4 specifically in your declaration?

A I didn't say Embodiment 4. But the quote was clearly in Embodiment 4.

Q I understand that the quote you believe is applicable to both Embodiments 1 and 3?

A Yes.

Q But you did not rely on any other portion of Embodiment 4 to form the basis of the opinion that you provided in your declaration?

A I have to look at that.

Q If it will help you to refer to your declaration, I believe all the discussion of

Nakamura begins on page 25 at A-1 and extends through page 42, the last paragraph in A-31.

A I am sorry, the question was if there is any other part of Embodiment 4 that I relied upon?

Q Yes, to form the basis of the opinion that you included in your declaration.

A I think that describes it, yes. Would you like to repeat the question?

Q Other than the portions of the Nakamura specification which begin at Column 15, Line 25, and extend through Column 15, Line 46, you did not analyze or rely on any other portion of Embodiment 4 to form the basis of your opinion that is included in your declaration, correct?

A I don't think there is anything else in Embodiment 4 that I relied on, but there is some repetition of things like the use of the stopper film and so on here that may be worded differently than in Embodiments 1 and 3, so I would say, yes, to your question with that kind of caveat that there may be things that could be interpreted as important there.

Q But for your declaration you relied on Embodiments 1 and 3 and then the other portion?

A That is right.

Q Let's talk about the first embodiment in Nakamura.

A First embodiment?

Q The first embodiment, yes, and I believe that begins at Column 9, Line 24. I think you also begin that discussion at paragraph A-6 of your declaration.

The first step in the process of the first embodiment is the formation of the isolation regions, correct?

A Yes.

Q Then the next step, starting at around Column 9, Line 37, is the formation of the gate electrode?

A No, there is a gate insulator that is needed first.

Q Is the gate insulation film part of the gate electrode?

A That is another semantics question. Do you really want to go through this?

Q I don't think it is critical, but fine, let's just say that the next step after formation of the isolation region is the formation of the gate insulation film, right?

A Yes.

Q Then subsequently there is gate electrodes that are formed on the gate insulation film, correct?
A Yes.
Q What is the structure of the gate electrode?
A It is described on the first embodiment dope polysilicon which is the electrical component and then a silicon oxide film on the top.
Q The silicon oxide film on the top, what is the purpose of that component?
A I think it protects the polysilicon from exposure and oxidation during the different process steps that follow and in between the process steps, that is exposed to air.
Q It is for protection purposes?
A Yes. In some configurations it serves as an etch stop as well, but I'm not sure that it does here, I just don't remember.
Q Do you know why Nakamura chose to use oxide as the material for that insulation film?
A No, I don't recall. I don't know if he said why.
Q Would a person of ordinary skill in the art understand why oxide was chosen as the

material?

A There are many reasons that people choose one or the other of insulating film like that, usually oxide or nitride.

Q After the formation of the gate electrode, if you will look at Column 9, Line 45, to 53, the next step is the formation, the next step is to use the gate electrode as a mask to implant ions to form impurity dope regions, correct?

A Yes.

Q And the impurity doped regions are to be an LDD structure?

A Yes, or it describes here also MOD structure and I believe that is the one that enables or allows anisotropic diffusion of the implant during an anneal so that it may go a little bit under the gate electron and I think that is depicted as 22 in Fig. 1B.

Q What is the LDD structure?

A LDD is called lightly doped drain.

Q Is that the same thing as lightly doped well?

A No.

Q What is the difference?

A A well is a larger region, so when you do CMOS technology which this all is you need to make p-channel and n-channel devices, so you start with a substrate that has one doping site, so some of the devices have to be in the region, on the bulk silicon, but once I have to be in a p-region, you have to make a deeper region not too far from the surface of the silicon, that is "P" in which you make the other polarity of the device.

Q Is the MOD structure a lightly doped well?

A I am not sure. I don't think this is relevant to the questions here.

I haven't spent MY attention on the implantation dope file, naming conventions or all the different permutations that can be used to make them particularly because here we are trying to concentrate on the raised source drain.

Q So I'm clear. You are not sure whether MOD structure is a lightly doped well, but you are sure that an LDD structure is not a lightly doped well, is that correct?

A I didn't say that. LDD stands for a lightly doped drain. Oh, I'm sorry. Well? No.

A well is different from a source or a

drain or a source drain extension or any permutation thereof. A well is a deeper thing.

Q So an LDD structure is not a lightly doped well, correct?

A Right.

Q But you do not know whether an MOD structure is a lightly doped well or not?

A Oh, well, no, it is a drain, minimum overlapped source of drain.

Q An MOD structure is also not a lightly doped well, right?

A Right.

Q If we can move on down to Line 62, Column 9, "the next step is the formation of a silicon nitride etching stopper film," correct?

A Yes.

Q The purpose of this etching stopper film is to be used as a stopper for etching the interlayer insulation film in a later step and a sidewall insulation film is to be formed on the sidewalls of the gate electrode, correct?

A Yes.

Q The sidewall insulation film formed on the sidewalls of the gate electrode the same thing as a spacer?

A It serves the role of an electrical spacer.

Q The next step is beginning at Column 10, Line 6, is the formation of the interlayer insulation film, correct?

A Yes.

Q The next step, subsequent to the formation of the interlayer insulation film is a planarization of that film, correct?

A Yes.

Q Nakamura describes that planarization using the process of CMP, correct?

A Yes.

Q The next step is the formation of patterned photoresist, correct?

A Yes.

Q What does Nakamura say about the pattern in that photoresist?

A Down on Line 30, it says, "Anisotropic etching is further conducted with the photoresist 28 as a patterned the etching stopper film 24, below the interlayer insulation film 26, and as a result because of the etching stopper film 24 deposit the sidewalls of the gate electrodes 18 and the insulation film 20, even when the etching

goes on until a silicon substrate 10 is exposed in the regions where the source drain diffused layer are to be formed the etching stopper film on the sidewall says not removed, to remain as the sidewall insulation films 30.

So the pattern is chosen to be able to etch ultimately down to the source drain contact regions and to etch the sidewall region of the gate electrode such as to form side wall spacers.

Then this embodiment, it protects the center region of the gate electrodes in this embodiment.

Q When you say it protects the central region of the gate electrodes are you saying that the mask --

A Yes.

Q -- covers the gate electrodes so that they are not etched in the etching process?

A It covers part of the gate electrode, the central part. You can see that in Fig. 2A.

Q It says Nakamura in its description, in its actual description, states that its objective is to protect only the central part of the gate electrode?

A I don't think it says that, but it

certainly says that the etching will produce the sidewall spacers, so if you do not leave some opening near the edge of gate electrode for the etch to take place in forming the resist mask, then you will not form the sidewall spacer and it clearly says it will form the side wall spacer.

That is down at Column 10, Line 37 or something like that.

It says, "Silicon substrate 10 is exposed in the regions where the source drain diffused layer are to be formed.

"The etching stopper films 24 are on the sidewalls is not removed to remain as the sidewall insulation films 30."

Q After the pattern resist form then you perform your etching process, correct?

A Yes.

Q That etches the interlayer insulator film and then it etches the etching stopper film, correct?

A Yes.

Q Then the step after that -- well, actually, Nakamura in terms of a description of Embodiment 1, says that the step after you finish your etching is to then do ion implantation,

correct?

A As you see in Line 40, Nakamura also says, "that concurrent to that etch contact holes 34, 36 are open in alignment with the gate electrodes 18 on the regions where the source drained diffused layer is formed.

Q The contact holes are open as a result of the etching process.

A Yes, it is part of the etching process, right, I just wanted to note that because it is quite critical here.

It is also noteworthy in the paragraph starting at 43, it basically points out that the etching stopper film 24 leads to the sidewall insulation film without requiring a separate one which sounds very much like the motivation in the '244 patent.

Q If we look at Embodiment 1, Column 11, this is Nakamura, Column 11, beginning at Line 9, that is the portion where it is describing the formation of the conducting film for Embodiment 1, correct?

A Yes.

Q You discuss in your declaration at paragraph A-28 which is on page 39 of your

declaration, you say, "With regard to both the first --

A Hold on just a second. A-29?

Q A-28, it begins on page 39 of your declaration and it continues through page 40.

In your declaration you say, "With regard to both the first and third embodiments," although we are talking specifically about the first embodiment right, now, you say, "Nakamura teaches that a conducting film is deposited on the entire surface in patterned form electrodes," do you see that?

A Yes.

Q Then you provide annotated versions of Fig. 2C for Embodiment 1 and Fig. 6B for Embodiment 3, correct?

A Yes.

Q Then you say, "As is well known in the art patterning by definition involves removal of a layer."

A Yes, you may remember my discussion yesterday when we were talking about the definition of lithography and its relationship to patterning and I said, "Some people think of lithography as the optical exposure patterned

definition part to clearly those people built tools for lithography and other people think of lithography as really the synonym for patterning where you have to have a waveform image making the photoresist mask and then using the etch."

Q Continuing on at paragraph A-29, you say, "In summary, because Nakamura is teaching this patterning process, Nakamura teaches two consecutive steps of depositing a conductor layer on a substrate and removing the conductor layer other than portions filling trenches."

Do you see that?

A Yes.

Q You reference Fig. 2C and I suppose Fig. 6B as well to show that?

A Yes.

Q It is your opinion that Figs. 2C and 6B show conductive material only in the trenches, correct?

A I don't know what you mean by "only in the trenches." They are within the etched regions through the interlayer dielectric and the sidewall insulating film and in some areas 24 which was the etch stopper film, so if that is what you mean by trenches that is what is shown there.

Q Do those images also show conducting film or some of the conducting film outside of the trenches?

A What do you call a trench?

Q Do you have an understanding of the term trench as it is used in the '244 patent?

A Yes, and let me find where that is used. Yes, "moving said fourth dielectric layer," blah blah, "to form plurality of trenches adjacent to said gate electrode structure." So that would be the pieces 42 and 44 in Fig. 2C.

Yes, I agree.

Q So the images, Fig 2C and Fig. 6B, do show some of the conducting film outside of the trenches, correct?

A I don't think that the 2 and 4 is specific about whether in --

The answer to your question is yes or no because it doesn't really define the vertical profile of the trench.

For example, 42 in Fig 2C, part of that goes all the way down to the silicon substrate. Part of it is over the spacer and adjacent to the ILD and the edge stopper layer.

It depends what you call a trench. Then

there is a little bit of that that is over the ILD, layer 26.

Q Would you consider the portion of the conducting film that is over the ILD within the trench?

A I don't know why this is a question. Is this just a hypothetical question?

Q It is not hypothetical. I am asking you with reference to the figure whether you would consider a portion of the conducting film that is over the ILD within the trench?

A In the context of '244, I assume that's where your question is aimed, Claim 1, the clause, the limitation, "removing said fourth dielectric layer," says, "to form a plurality of trenches adjacent to said gate electrode structure."

In that sense, '244 is defining the trench to be that part of it that is adjacent to gate electrode.

It is not specific about whether that includes the cap layer over the polysilicon. If I take that definition, then some of the conducting layer is outside of the trench if I take that definition as inferred from the '244 claim.

Q What if the definition of trench

included the portion formed by the cap layer?

A The cap layer, the ILD layer?

Q The ILD layer, in that case, would some of the conducting film still be outside of the trench as shown in Fig 2C and Fig 6B?

A If the trench went all the way up to the top of 26?

Q Yes.

A And then the question is part of the conducting film outside of that?

Q Yes.

A This is a very hypothetical question. I don't understand the relevance of this question because it is a semantics question. It does not bear on what the content of the patents at issue are.

Q I'm asking you about Fig 2C and Fig 6B. Looking at the figures, do those figures show some of the conducting film outside of the trench if the trench went all the way up to the top of the ILD which is labeled 26.

A If I look at that figure and I look at the profile of 42, the shape of 42, it is the case that some of 42 appears above 26, but I don't see any significance whatsoever to that.

Q The same is true for both Fig. 2C and Fig 6B, correct?

A Yes. The definition of the 42 structure and the 44 was the patterning function that was carried out after deposition of the material into these trenches, so it would have a different shape.

Q What do you mean so it would have a different shape? What are you referring to there?

A I said it here. I can go to this, A-28. "With respect to the first and third Embodiments, Nakamura teaches, "A conducting film is deposited on the entire surface and patterned to form electrodes 42, 44." Then it refers to those two figures.

"As is well known in the art, patterning by definition involves removal of a layer, therefore Nakamura's disclosure of patterning the conducting film necessarily teaches removing some of the conducting film."

There would have been, being able to create these shapes.

Blanket deposition of the polysilicon into these trenches or whatever you call trenches, and then a photoresist layer put on top of that,

it is patterned and then that pattern is used to etch out the uncovered regions and the periphery of those regions would be outside of the trench dimension at the top of the ILD that was created in the previous etched sequence.

I think one of ordinary skill would try to make the edges outside the inside edges of the holes in 26, because otherwise, you may have a seam and that is a reliability concern.

MR. CHEN: Let's move on to the discussion of the third embodiment.

MR. MUKERJI: Mr. Chen, it sounds like you are switching topics slightly. It has been about an hour, could we take a short break?

MR. CHEN: Sure, if you need one, that is fine.

(Whereupon, a break in the proceedings commenced at 2:26 p.m. and on resuming at 2:46 p.m.)

BY MR. CHEN:

Q Dr. Rubloff, we were about to start talking about the third embodiment in Nakamura.

A Yes.

Q I believe that begins at Column 12, Line 60.

A Yes.
Q A lot of the steps in the third embodiment are similar to first embodiment, so we will skip it all the way up to --
Let's move to Column 13, Line 23. I think that's where after they form the gate electrode in the third embodiment, correct?
A Correct.
Q After they form the gate electrode then they deposit the etching stopper film, correct?
A Yes, that is Line 26.
Q Right and that is shown in Fig. 5A on the Nakamura patent?
A Right.
Q Then after they deposit etching stopper film, they deposit the interlayer insulation film, correct?
A Yes.
Q Then a planarization removes the interlayer insulation film all the way down onto the etching stopper film over the gate, correct?
A Yes.
Q Then planarization removes interlayer insulation film all the way down to etching stopper film over the gate, correct?

A Yes.
Q Do you know why they planarized the interlayer insulation film all the way down to the etching stopper film over the gate?
A I think there is a figure which denotes some benefits of that on page 40 of my declaration. I think what you can see is that the structure is shorter, the resulting structure would be shorter and more planar.
I think one of the embodiments, and I don't recall which one, speaks to this question that I described earlier, the depth of field, focusing on lithography and more planar things can be across the various required structures, the easier it is to do lithography well.
I don't know if that is only motivation, but that certainly is one.
Q I believe you're talking about this specific planarization at page 35 of your declaration and continuing on to page 36.
A Yes.
Q Following the planarization step, there is the formation of a photoresist, the pattern resist?
A Yes.

Q After the form pattern resist, then after the formation of the pattern resist, Nakamura Embodiment 3 teaches the beginning of the etching process, correct?
A Yes.
Q In the first stage of the etch process the unmasked portions of the interlayer insulation film are removed, correct?
A Yes.
Q What happens after that etch is completed?
A In the description of the third Embodiment the photoresist is then removed. This is Line 39.
Q Of Column?
A I am sorry, no, it is later than that. Sorry, Column 13, Line 47.
Q How is the photoresist removed?
A It does not specify.
Q How would a person of ordinary skill in the art understand would be needed --
MR. CHEN: Let me rephrase that.
BY MR. CHEN:
Q What would a person of ordinary skill in the art understand is the process to remove the

photoresist?

A The simplest one is by wet chemical techniques to dissolve the photoresist.

There are other techniques that can be used depending on conditions, more specifically ashing, any organic can be ashed which means volatilize it in a oxygen containing plasma.

Q Is the removal of the photoresist done in the same tool as the etching process?

A The specification doesn't really tell us that.

Q Typically, is the removal of the photoresist done in the same tool as the tool used to perform an etch?

A No.

Q Typically the wafer would need to be moved from the tool that does the etch to the tool that will remove the photoresist, correct?

A Most typically, but there are situations where it could be done in situ, whether it is advisable or not depends on the situation.

Q What do you mean "advisable or not"?

A These etching tools are chemically temperamental sometimes, and particularly dry etching, so in principle one could do the etch,

change the gases, use a similar power in the plasma, change the bias probably on the electrodes and use oxygen to remove the photoresist in the form of CO and CO2 and then change back.

I think that would be possible but it is not clear if it would be workable in this configuration.

It probably depends on how sensitive the etch is in this case. To summarize, the natural way to do it is to remove it from the tool, do wet etch or wet dissolution of the photoresist and then go back in the tool to finish the etch.

Q Is it important to remove all of the photoresist material?

A Yes, I think it is certainly advisable.

Q Why is that?

A If you didn't remove all of it, then when you continue the etch it will be etched away by the etch that you are using to finish the intended etch and that is probably not a great idea. Unless you develop the special process.

Q How long does it usually take to remove the photoresist? How long does the process of removing the photoresist usually take?

A I am not quite sure which parts. If you

want to go from the photoresist on the wafer you can take the wafer out of the etch tool and put in another tool you will dissolve away the photoresist and then you are going to take it out and put it back in etch tool, I would guess it is some minutes, a few minutes, I don't really know.

Q In Nakamura Embodiment 3 after the photoresist has been removed, then more etching is performed, correct?

A Yes.

Q This second stage is different than the first stage, correct?

A Yes, I think that is right, but let me look again .... yes.

Q The etch chemistry is adjusted?

A Yes.

Q What is being etched during the second stage?

A The ILD film 26, and etch stopper film 24, have to be removed.

Q Why are both materials removed?

A The material 24, the etch stopper film in the Fig. 6A, had been over the source drain region, so you don't want a piece of silicon nitride covering the region where you are going to

form the resource drain and in that process you complete the formation of the side wall film.

Q Why is the material 26 removed during the second stage etch?

A 26 is being removed that substantially is the same rate as the etch stopper film, so it serves kind of as a sacrificial mask for defining the edge of the etch.

Q Look at Nakamura Column 13, Line 58, it says there, "On the other hand the interlayer insulation film 26 is etched by a film thickness substantially equal to a film thickness of the etching stopper film 24 and the interlayer insulation film 26 has a height substantially equal to a height of the insulation film 20 exposed on the surface.

"Thus contact host 34 and 36 can be opened with the surface maintained plain."

Do you see that?

A Yes.

Q Does that help explain why in the Nakamura third Embodiment the interlayer insulation film is etched during the second stage etch?

A Yes, because it is desirable to have as

much a planar surface as is possible for lithography purposes s.

Q They wanted to have the height of the interlayer insulation film 26 be substantially equal to the height of the gate, correct?

A It is a desirable benefit if you can do it.

Q If Nakamura Embodiment 3 did not remove the mask --

A The photoresist mask?

Q Yes, and continued with the second stage etch, would it have been able to achieve the goals that are described in Column 13, Line 57, through 64?

MR. MUKERJI: Objection to form and scope.

THE WITNESS: The etch stopper film 24 is pretty thin. It shouldn't take a very long etch to clear that over the diffusion region, over the source drain region.

I don't really know the answer whether the planarity can be achieved in the same way because I don't know where the relative etch rates will be and so on.

That planarity is a nice benefit, if you

can get it, but it is not essential and particular, it is not essential for considering the extent to which Nakamura meets the claim limitations in the '244 patent.

BY MR. CHEN:

Q But achieving that planarity is one of the goals stated for Nakamura Embodiment 3, correct?

A Yes, the way Nakamura Embodiment 3 does it.

Q If the resist was in place when you performed the second stage of the etch, then the interlayer insulation film 26 would not be etched, correct?

A Correct.

MR. MUKERJI: Objection to form and scope.

BY MR. CHEN:

Q By removing the resist mask, the portions of the interlayer insulation film that were previously masked are then subsequently etched during the second stage each, correct?

A Correct.

(Whereupon, Exhibit Number 11 is marked for

Identification.)
BY MR. CHEN:
Q I have asked the court reporter to mark as Exhibit No. 11, a document with the title "Introduction to NMOS and CMOS VLSI System designs by M.R. Mukherjee, and I am hoping that I have pronounced that correctly?
MR. MUKERJI: It is pretty good.
MR. CHEN: Thanks.
BY MR. CHEN:
Q This is another one of the references that you relied on to support your declaration on the '244 patent, correct?
A Yes, I think that is right.
Q I want to turn your attention to page 19 of Exhibit 11. If you need to refer to other portions of the exhibit, just let me know what you are looking at.
If you also need to refer to your declaration, I believe the Mukherjee reference discussed is paragraphs C1 through C3.
A Yes.
Q I would like to walk through to what is being described in the paragraph of page 19 of Exhibit 11 and understand what is happening at

each of these different stages beginning at the upper left-hand corner with the image marked A.

A Yes.

Q What is happening at that stage?

A There has been presumably a thermal oxide, it only says oxide, if deposited or grown, if it is thermal oxide, it is grown on an antisubstrate and that has been covered by silicon nitride presumably by thermal CVD process.

Q What is happening at the next stage in the image marked B?

A I haven't looked at this in months, but it looks as if the silicon nitride has been patterned.

Q What is the meaning of the label "active areas"?

A I don't know. I will have to re-read this to know what we are talking about here. Do you want me to take the time to re-read it?

Q It's a pretty long reference.

A Yes, it is.

Q The reason why I am referring you to this particular page is because you actually cite to it. Maybe not.

A I do? I don't know why I would do that

except --

Q I am sorry. I looked at the 4.3 at the top and I thought you were referencing this portion.

A Some of these combinations that you see in my declaration, they are only to substantiate what everyone of ordinary skill would already know.

I am advised that for patent purposes like this you really have to have a reference even though everyone knows that is the case.

A At the end of paragraph C1, I say, "However, it would have been obvious to a person of ordinary skill in the art to form a well in Substrate 10 of Nakamura."

Anybody who is doing any of these technologies is doing something related to CMOS and CMOS processes have been known for decades and for the purposes of innovation in comparing Nakamura to '244 to whatever is involved I think these are not really important.

Q Just again looking at Fig. 4.3.

A 4.4?

Q Page 7 of Nakamura, this is the figure that you are --

A I'm sorry? In Nakamura?
Q Sorry. Mukherjee, Exhibit 11. This, I believe, is the figure you are referencing in your declaration?
A 4.3D.
Q Yes, I hope that is right. I would like to understand what is happening here in this figure. In the portion of the figure at the upper left that is labeled A.
A Yes.
Q There's a substrate, do you see that, p-substrate?
A Yes.
Q On top of the p-substrate is an oxide?
A Yes.
Q Is that oxide the gate oxide?
A I don't think that is the point. The point of my referencing this and from the little that is depicted here it's just trying to prove the point there is a photoresist sequence using optical lithography and leading to patterning capability that involves etching that can allow you to take a continuous fill like oxide and break it up into islands whose shape you defined in the original optical mask. This is just straight

optical lithography.

Q I thought you were using this to demonstrate the formation of lightly doped wells.

A It's the first step in doing that subsequently so what I say here is you can form islands of base materials such as silicon dioxide which turn out then to be masks for implantation, or for the fusion, so subsequently the diffusion process using ion implantation techniques and then performed with dry ions and create p-well in an antisubstrate.

In "D" here, I could take that sample, go to an ion implantar, implant antidopants or put that surface in contact with some other source of antidopants and anneal the result and I would have p-wells underneath the opening.

Q So the oxide there is really just being used as a mask?

A The oxide, I am just going from the demonstration in Fig. 4.3 that you could make a patterned island structure, right? And let's see, page -- I don't understand. The pages are on the upper right?

Q Yes, there are two different page numbering schemes.

A Yes, it's kind of confusing. So thus Mukherjee describes MLS certification technique in which a well is formed between the steps of forming islands which correspond to isolation, regions, and the step of forming a protective oxide layer which is understood in the art corresponds to dielectric layer.

The whole point here as stated in C3 is one of ordinary skill would recognize that the way it is describing Mukherjee to make MLS devices could be used to detail the steps for MLS fabrication that are kind of left out and not described in detail in Nakamura.

Q Right, so are the oxide islands the isolation regions, is that what Mukherjee is saying?

A I have to re-read what he says. This Fig. 4.3. in the text of Mukherjee is speaking to the general process of lithography.

From that one can control where implantation goes. I would say this is pretty general, but in Nakamura there are Regions 22 in Figure 5C, and 6A and 6B, for example, which could be formed by ion implantation and that can be done before the gate electrode is formed.

That is one of the things that is needed to realize the structure. Like it is very well known.

Q I'm trying to understand what you're saying about the Mukherjee reference specifically. Is it your opinion that the oxide islands shown in Fig. 4.3D are equivalent to isolation regions?

A Sorry 4.3?

MR. MUKERJI: Objection to the form.

THE WITNESS: Would you repeat the question.

BY MR. CHEN:

Q Is it your opinion that the oxide islands shown in Fig 4.3D correspond to isolation regions?

A They could be the definition of where the isolation -- they could be isolation regions and they also define where the active regions will be formed by some combination of either diffusion or ion implantation doping to form wells or to form source drain regions.

Q Are isolation regions typically very thin?

A You mean the oxide isolation regions?

Q Yes.

A What does "very thin" mean? Compared to what? Compared to wells or compared to the structures that we are talking about in the patents at hand?

Q If you turn to page 120, the previous page of the reference.

A Yes.

Q In paragraph 4.2.2, it talks about oxidation.

A Yes.

Q Then it talks about growing a thin layer of protective silicon dioxide on the silicon oxide.

A Where does say that?

Q Paragraph 4.2.2.

A It doesn't make sense to me. You grow silicon dioxide. That is the form that silicon creates when it is oxidized in oxygen or in water. Wet oxidation, dry oxidation.

I don't know why he says, "to grow a thin layer of protected silicon dioxide on the silicon oxide." That means grow thicker, right, so this thermal oxidation step, if it is dry, the growth rate is fairly small, so you slowly grow linearly in time thicker and thicker oxide.

If you keep going it will eventually slow down the growth rate mechanism and what that happens to switch from what is called linear to parabolic growth is well understood.

You can accelerate those growth rates if you add some water to the environment, but this is the "Classic Homer" problem you give to students, you have got this thickness of oxide, here are the oxidation conditions, how long does it take to increase the thickness by a certain amount?

But I don't know why it says "grow a thin layer of protective silicon dioxide on the silicon oxide." That doesn't grow on. It grows at the interface.

So I don't understand this sentence. Sorry.

The reference was chosen because it is a very general reference for all of the things, not all, but for some of the things that Nakamura left a little bit vague, but everybody in this field knows.

Q In your declaration in paragraph C2 at the back end of that paragraph, in the last sentence you say, "Thus, Mukherjee describes a MOS fabrication technique in which a well is formed

between the steps of forming islands which correspond to isolation regions and the step of forming a protective oxide layer which as is understood in the art corresponds a dielectric layer."

A Yes.

Q Where is the description of forming the protective oxide layer?

A My statement here is that an ion implantation of diffusion step is used to form a well after island regions like the LOCOS regions that we talked about, LOCOS I think is explained to you, right? Remember, the patterning can be done over and over again.

I can use the technique that is outlined in Fig. 4.3, as just a general description of lithography to produce an island pattern as you see in D and then to use that as an implant mask to deposit to inject dopants to make a well.

I can do that after --

Let's see, after or before?

I can do LOCOS first, then form the well, using the LOCOS even as an ion implantation process, and then clean the silicon surface by known chemical techniques, HF, for example, and

then I can grow a thermal oxide.

Q Looking on page 122 of the reference in the paragraph 4.2.4 in the diffusion?

A Yes.

Q The second to last sentence of that paragraph, it says, "It is possible to grow an oxide layer right after the drive-in process thereby providing a thin protective oxide layer."

A Yes.

Q Is it your opinion that that thin protective oxide layer corresponds to the gate oxide?

A It could. It need not be as described here.

Q So it doesn't specifically say that that's the gate oxide, correct?

A No. You put layers down. You pattern them, you do something, you remove the layers. Often, even if they are oxide or nitride, they are sacrificial, they are there for a purpose of modifying the substrate as in making wells and making the implant more diffusion regions.

Q Similarly, with respect to the oxide islands that are shown in Fig. 4.3D, Mukherjee doesn't specifically say that those oxide islands

are isolation regions, correct?

A Clearly they could be. I mean this is showing general lithography. This is teaching lithography 101.

They could be isolation regions. They could be silicon nitride pads so that you can then oxidize between the silicon nitride pads to form those LOCOS structures that you saw in some of the -- yes, here, for example, in 5A, Number 12, that is a LOCOS isolation region typically formed by nitride patterned local oxidation.

Q Fig. 4.3 really is just focused on the patterning steps, correct? Yes. Fig. 4.3 is really just focused on the patterning steps, correct?

A 4.3 is what I would call introduction to lithography. How do you pattern islands where you want them? They can almost be removed? They can be used to pattern things in the substrate.

It enables many things. It enables LOCOS relevant, enables diffusion, or implantation, in patterns and so on.

Q But it doesn't teach the implantation steps, correct?

A Well, the other parts of this mention

the various to make n-wells and p-wells and the like. I think it is all here.

Q But not in the specific figure, correct?

A This figure is in an enabler of these other things.

MR. CHEN: I will move on to a different declaration.

MR. MUKERJI: Then I have a few questions on the '244, so if we could do that.

EXAMINATION BY MR. MUKERJI:

Q Professor Rubloff, you considered all the claims of '244 in doing the work in this case, correct?

A Yes.

Q That includes Claim 16 of the '244 patent, right?

A Yes.

Q Would you look at the '244 patent please which I think is Exhibit 9, half way down is Claim 16, there is a word that appears and it says "planarizing" do you see that?

A Yes.

Q Earlier today there was considerable discussion on planarization, do you recall that?

A Yes.
Q Just so I'm clear. Can you tell us whether or not you considered the issue of planarizing in connection with your study of Nakamura?
A Yes, I certainly did.
Q And you stand by the opinions that you have expressed in your declaration on that issue?
A Yes.
MR. MUKERJI: Thank you. Pass the witness.
(Whereupon, Respondent's Exhibit Number 12 was marled for Identification.)
EXAMINATION BY MR. CHEN:
Q I asked the court reporter to mark as Exhibit No. 12, your declaration that was submitted in connection with Samsung's IPR of the '893 patent. Is this your declaration? Is Exhibit 12 your declaration?
A I would have to look at this. The print is too big in that one. Yes.
Q And does this declaration contain any and all relevant opinions you have regarding issues related to Samsung's petition for review of the '893 patent?

A Well, yes, related to my input to the petition process that they have done.

MR. MUKERJI: Counsel, before you ask your next question, for clarity of the record, there are two proceedings pending on the '893. This declaration is 466 or 467.

MR. CHEN: Thank you for clarifying that issue. I believe it is the same declaration that was submitted in both proceedings.

MR. MUKERJI: Can we stipulate then that this is declaration in both the '466 and the '467?

MR. CHEN: Yes.

MR. MUKERJI: Sorry for the interruption.

MR. CHEN: No problem.

BY MR. CHEN:

Q Does this declaration contain any and all relevant opinions you have regarding issues related to Samsung's two petitions for review of the '893 patent?

MR. MUKERJI: Objection to form.

THE WITNESS: This represents my conclusions in addressing the questions I was asked to address whether prior art meets the

claim limitations in the '893 patent.

BY MR. CHEN:

Q Do you have any opinions regarding the issues relevant to Samsung's two petitions for review of the '893 patent that were not included in this declaration?

MR. MUKERJI: Objection to the form.

THE WITNESS: I haven't read those two petitions so I'm not qualified to answer that.

BY MR. CHEN:

Q Do you have any opinions regarding the validity of '893 patent that were not included in this declaration?

MR. MUKERJI: Objection to the form.

THE WITNESS: In the opinions that are --

BY MR. CHEN:

Q Regarding the validity of the '893 patent?

MR. MUKERJI: Same objection.

THE WITNESS: Yes. I'm not a patent attorney, so what I looked at was whether what is taught in prior art references and in particular the ones I put in my declaration

map onto or cover the teaching of the '893 patent. Validity is a legal question.

BY MR. CHEN:

Q So you did not provide an opinion as to whether the '893 patent is valid or invalid, correct?

A No, I did not provide. I have concerns about it because it is not enabling, but I don't think that is an issue here. It is not supposed to be an issue.

Q Do you have any opinions regarding the '893 patent or any prior art to the '893 patent that are not included in your declaration?

A I don't think so. This is a summary of what I believe.

Q Are you aware of any errors or omissions in your declaration?

A I don't think so.

(Whereupon, Respondent's Exhibit Number 13 was marled for Identification.)

BY MR. CHEN:

Q Dr. Rubloff, I have asked the court reporter to mark Exhibit 13, which is Patent No. 6,030,893.

We will be referring to this exhibit as

the '893 patent for the rest of this deposition. Have you read the '893 patent?

A Certainly.

Q When did you first read the '893 patent?

A Thank you. You asked me yesterday when I started working on these and it was humorous that I had it wrong so I went back and looked and it must have been in October 2014, ten months ago.

Q That was when you were first engaged in these matters?

A Yes, but then I think I was told that the '893, the '244, "These are the ones they want you to look at."

Q Turning to your declaration, which is Exhibit 12, if we can look at paragraph 19, it begins on page 12 of your declaration.

A Yes.

Q You stated here that you believe that the '893 patent is not enabled, correct?

A That is right.

Q Why do you think that the '893 patent is not enabled?

MR. MUKERJI: Objection, outside the scope. You can answer.

THE WITNESS: I can answer?

MR. MUKERJI: You can, yes.

THE WITNESS: I was actually quite surprised to find this. The '893 patent talks about a constant CVD process using tungsten hexafluoride.

To deposit, to use tungsten hexafluoride to deposit tungsten, you have to have a way to remove the fluorine.

If the fluorine is in the tungsten film it will not be a good film. You need a reducing agent to do that.

The conventional one, the most popular one is hydrogen. Hydrogen then bonds to the fluorine which makes HF, that is a volatile product that leaves the surface and then only the tungsten atom is left behind to deposit. That is the basic idea.

But there is no mention of hydrogen as a reducing agent in the CVD process.

There are two or at least two other reducing agents which can be lead to tungsten deposition. Well, actually more than two.

An example is Silane, SiH4, and that can be used. It makes a much faster growth rate. So a WF6, plus Silane, will produce tungsten

as a deposited film, and SiF4 and HF that leaves the surface, and finally you can use silicon.

If you use the WF6 and hydrogen it can react with the silicon substrate and produce silicon fluoride products that leave the surface but unfortunately etch and therefore rough on the silicon surface.

People have used all of these and there are different trade-offs between using them. But the effect is that if you have a CVD reactor and the only thing you put into it is WF6 you will not get a tungsten film.

What is surprising was, and this is all very well known in this time frame, and the prior art references cite that, they talk about hydrogen reductor.

They talk about the silicon substrate doing the reducing and they talk about Silane as a reducing agent and they talk about it in the context of well understood chemical trends that relate gas ratios of the reductant to the WF6, temperature, dependencies of these and really lay out the state of the art which was there.

I say that this is not enabling primarily because it doesn't even tell you what molecules are being used.

BY MR. CHEN:

Q It is your opinion that a person of ordinary skill in the art would not be able to implement the teachings of the '893 patent without the specific mention of the reducing agents like hydrogen or Silane or silicon, correct?

A Yes, what would happen is that the person, or processor, the equipment engineer, whoever it is, goes through the tool and you tell them this is the tool and if they are supposed to hook up the gases they don't know what gas to put on the tool.

Q Without the specific instruction of what reducing agents to use a person of ordinary skill in the art wouldn't be able to implement the teachings of the '893 patent?

A If all they had was '893, no, they wouldn't know what to do, but the prior art would have told them not only what gases to use, but how the different process parameters work together to change conformalities, stress, growth rate, et cetera.

Q Looking at the '893, would a person of ordinary skill in the art have been able to modify the teachings of the '893 patent to implement those teachings?

MR. MUKERJI: Objection to the form.

THE WITNESS: I don't know what they do to figure out what the reactant is without looking at prior art literature.

MR. CHEN: Let me reask the question.

BY MR. CHEN:

Q Looking at the '893 patent, would a person of ordinary skill in the art have been able to modify the process described in the '893 patent to implement the teachings of the '893 patent?

A This hypothetical person has access to what information? The literature?

Q You would have access to whatever the hypothetical person of ordinary skill in the art that you define for the '893 patent has access to?

A I think a person of ordinary skill in the art will read this patent, and say, "I have to know how this process works so I know what gas bottles to hook up and so on," so they would be able to get that from prior art information, by locations, patents, and so on, some of the patents

I cited and some of the references, and then to actually implement the two-layered deposition and to know what process parameters to choose, they would look beyond the teachings of the '893 to, "How does the mechanism work? Why does temperature change something this way? What is the role of the gas flow ratio?" which is very critical here.

And that is not found in the '893 and it is important for actually knowing how to do the design of experiments to determine the process parameter point.

And it is available in the prior art literature. It was all known.

I happen to know it because I worked in this and I know other people who have worked in it, so I concentrated on it.

MR. CHEN: Let's take a quick break. Ron has to catch a flight.

(Whereupon, a break in the proceedings commenced at 3:46 p.m. and on resuming at 4:02 p.m.)

(Whereupon, Respondent's Exhibit Number 14 was marked for Identification.)

BY MR. CHEN:

Q Dr. Rubloff, I have asked the court

reporter to mark as Exhibit 14, Patent No. 5,843,840, which I believe we were referring to say Miyazaki Reference.

A Yes.

Q The Miyazaki Reference is one of the primary references that you discuss in your declaration which is Exhibit 12, correct?

A Yes.

Q I believe your discussion of the Miyazaki Reference begins on page 23 of your declaration paragraph A1?

A Yes.

Q Miyazaki describes six different Embodiments, correct?

A I guess they number that, but I don't remember.

Q I could refer to you the Miyazaki Reference, Column 5, Line 44, that is where it begins the description of the preferred embodiments and then it concludes at Column 9.

A Fifth, sixth. Yes.

Q Which embodiments in Miyazaki were you relying on to support the opinions provided in your declaration?

A I don't remember if I put that into my

declaration. I will have to look for that.

I am glad to look through them, but I think the distinguishing feature is that some of them are related to ion implantation, and some related to CVD tungsten.

Q Right.

A So changing process parameters from CVD tungsten as opposed to using ion implantation to change stress and so on.

Q One of the key features of the '893 patent is the use, depositing two layers of CVD tungsten doing the deposition in two different chambers and then modifying the temperature between those depositions, correct?

A Yes.

Q Then we will walk through each of the embodiments and ask you whether this is one embodiment that you are relying on. I believe Embodiment 1 begins at Column 5, Line 43.

A Yes.

Q And then continues on to Column 6, Line 37. I believe Embodiment 1 describes a process where only a single layer of CVD tungsten is deposited, correct?

A Yes.

Q You are not relying on Embodiment 2 to support the opinions that are provided in your declaration, right?

A Some of the independent claims in the '893 speak to two layers of tungsten under different conditions, so Embodiment 1 of what we are talking about here, Miyazaki, is not what I relied upon.

Q Looking at Embodiment 2, that begins at Column 6, Line 38, and continues through Column 7, Line 24, the second embodiment of Miyazaki also deposits only a single layer of CVD tungsten and so you are not relying on Embodiment 2 to support your opinions in your declaration?

A No, I don't think either one of those, although it may be that there are aspects of the tungsten CVD process described in there that may not be easily found in the ones that I did rely upon. I don't recall if there are any such examples.

Q That's fine. If we come across that, or if it is, it is probably in your declaration?

A Yes, I think so.

Q The third Embodiment, which begins at Column 7, Line 26, continuing all the way through

Column 8, Line 14, the third Embodiment in Miyazaki does deposit two layers of CVD tungsten, correct?

A Yes.

Q As disclosed in Miyazaki, the temperature used for the deposition of the first layer of CVD tungsten in Embodiment 3 and the second layer of CVD tungsten in Embodiment 3 is the same, correct?

A Yes, that is right.

Q You are also not relying on Embodiment 3 to support the opinions that you provided in your declaration, correct?

A I am relying on it in part because it is supportive of that. The Miyazaki provides the reductant species and it provides teaching as to how the process works.

It is important in trying to practice this kind of a technology to know what are the things that changed the conformality via a filling capability and one of the things changed is stress and Miyazaki teaches at least two very significant points.

One of them is temperature.

As you go up in temperature you tend to

get into a transport limited regime which has lower stress and better via trench filling capability, void free.

As you go down in temperature you enter a kinetically limited regime which is very good for void free filling but creates higher stress and Miyazaki teaches how this works.

This is a very fundamental point about these kinds of CVD processes. I have many lectures on this actually at this point. Temperature is one thing.

The other thing that is important is the ratio of the reductant in this case is hydrogen to tungsten hexafluoride, and so in reference in Embodiment 3, the two layers differ by that ratio.

If it turns out where if you have a higher ratio of hydrogen to tungsten hexafluoride then you tend to be weight limited by the tungsten hexafluoride arrival and that does not give good conformality, but hydrogen, if you go to a low ratio you are then weight limited by hydrogen and that is a nice strongly kinetic limitation which gives good conformality.

Q All the claims in the '893 patent require that the temperature of the second CVD

deposition is different from the temperature of the first CVD deposition, right?

A Yes, that is true.

Q And Miyazaki Embodiment 3 specifically teaches that the temperature between the two depositions is the same, correct?

A Yes, the sense in which I say, I relied upon is related to my concern about enablement.

But in the '893 patent there are numerous claim limitations that have to do with either time or flow rate of one, the only species mentioned, or thickness, and gas flow rate of the tungsten hexafluoride.

In order to understand how those are related to each other you have to understand two things.

One is the chemistry of the reaction at least to the level that the hydrogen to tungsten hexafluoride ratio is critical and changing that ratio can differentiate between the two characteristic films that the '893 is talking about.

Secondly, you have to understand what the role of texture is in transforming the situation from kinetically transport limited

domains which also is a way to differentiate these two.

In that sense, and I am sure we will come back to this, interpreting the way in which the Miyazaki or the Emesh teachings map onto the claims in '893, really depends on translating that.

Q We will come back to that, but my point is that you said that you do rely on aspects of Embodiment 3 to support your opinions in the declaration, correct?

A Certainly to support my contention that '893 is not enabling.

Q How about to support your contention that Miyazaki teaches all the limitations of '893 claims?

A This is really difficult because of enablement. I talk to enablement because of the processed chemistry. There is another enablement issue buried in this problem so you have to understand how deposition works.

The thickness you get is generally proportional to the time and the impingement rate of the molecule on the surface, the impingement rate on the molecules on the surface depends on

the pressure, the higher pressure, higher impingement rate.

Time is nothing very special in isolation and that's what the claims in the '893, some of them, are directed to.

There is another factor here which is the pressure of the hydrogen and the tungsten hexafluoride that will be used in the process can be associated with different flow rates.

If I have a certain pressure and I change the flow rate, I can change the pumping speed of the equipment and still get the same pressure.

In that sense the gas flow rate is not a variable which tells very much, so that's the second sense in which I have the concern of enablement.

Q If we look at the fourth embodiment in Miyazaki, this begins at Column 8, Line 15, and continues down to Line 46.

A Yes.

Q The fourth embodiment of Miyazaki teaches that the two depositions are done with the same gas flow rate, but different temperatures, correct?

A Yes.

Q You do rely on Embodiment 4 to support your contention that Miyazaki alone or in combination with other references teaches all the limitations of the '893 patent, correct?

A In a significant sense I will say yes to that, but as I tried to explain when we talk about thickness and processed time and flow rates those are not the determining factors for the process.

In more or less any case one can move the process into the regime of those parameters here, and say, "It meets the claim conditions," but it is a little bit phony because it is not enabling to tell us what is really happening.

Q When you're saying it is not annealing to tell us what is really happening, are you now to the teachings of Miyazaki?

A No, '893, it says 10 to 100 seconds, for example, well, there are plenty of Miyazaki and Emesh References that arrive at those numbers.

We can arrive at them, but those numbers are not particularly unique given that I can change the deposition rate by changing the pressure by just changing the gas flow and the pumping speed.

Q Would you consider the teachings Miyazaki enabling?

A Yes.

Q Do you think Miyazaki provides enough details so that a person of ordinary skill could implement whatever?

A Absolutely and in fact what it really gives is an understanding of, if it said 10 to 100 seconds, and my current process is at 150, I know which knobs to turn to get from 10 to 100, and if you want me to I can get to 350.

Q Let's look at Miyazaki and Embodiment 5 or the fifth embodiment that begins at Column 8, Line 47 and continues on to Column 9, Line 7.

Miyazaki's fifth embodiment again teaches two separate CVD tungsten depositions, only this time both the flow rate and the temperature are varied between the two deposition steps, correct?

A Yes.

Q You are also relying on Miyazaki Embodiment 5 to support your conclusions or your opinions in your declaration that Miyazaki alone or in combination with other references teaches all the limitations of the claims of the '893

patent, correct?
A Yes.
Q Miyazaki Embodiments 3, 4, and 5 all teach specific CVD deposition parameters, correct?
A Yes, they give examples of parameters.
Q Those parameters include, for example, the temperature for the deposition and the gas flow rate for the deposition, correct?
A Right. Yes. Oh, sorry correct that. Gas flow rates for the two species and therefore the gas flow ratios.
Q Because of those teachings you also believe that a person of ordinary skill in the art looking at Embodiments 3, 4, and 5 of Miyazaki would be able to implement the teachings of Miyazaki, correct?
A Yes, and in fact, from those as well as from some of the other things which Miyazaki describes about how the stress balance will work that is in some of the figures and how the competition between transport and kinetic limitation plays out, those would also be helpful to one of ordinary skill.
Q Then looking at the sixth embodiment that begins at Column 9, Line 8, and continues

through Column 9, Line 51, or Column 9, Line 58, the fifth Embodiment doesn't specifically teach process parameters used for two CVD tungsten depositions, correct?

A No, that's right. It has taught already how you can change the chemical and mechanical properties of the film to change the stress and then it goes through the excise, I think that is Fig. 13.

It goes through the exercise of asking, well, I have chosen process parameters for the two films that gives stresses of 5 of the 9 for the upper film and 10 of the 9 for the lower film, how will the stress vary as I have changed the relative thickness of those two films, that is what the sixth embodiment is teaching.

Q Embodiment 6 is focused on how to achieve a specific targeted stress level for your film by varying the thicknesses of the two different films, correct?

A Yes and the implication from that is that it gives you a road map for understanding how the resistance of the upper wire which is an interconnect wire will change because it changes with thickness and you have to trade off how

important that is as compared to the stress in your particular technology.

Q Embodiment 6 is agnostic about the specific process parameters that are used to form the two tungsten films, correct?

A That is right. It is a kind of demonstration example.

Q Did you rely on Embodiment 6 to support the opinions that you provided in your declaration?

A Yes, it supports the description of variables that is taught in Miyazaki.

Q When you say description of variables what are you referring to?

A Miyazaki tells you a number of times that if you change the hydrogen to tungsten ratio, between kinetic and transport regimes, and as you lower that ratio you will get a better filling and higher stress and as you increase that ratio you get lower stress and not as good a filling, things like that.

You are trying to say I am going to use two films of tungsten here whereon with Fig. 12, the one to operate, Fig. 12, the consequences are in Fig. 13, but Fig. 12 is perhaps even more

interesting.

Q Were you still answering?

A No, I am done.

Q Fig. 12 shows the overall stress of your tungsten film?

A Yes.

Q Based on the ratio of the stress level between the two tungsten films?

A The ratio of the thickness.

Q Sorry, the ratio of the thickness.

A Yes, you see film thickness ratio. It is a little strange the word composition, but on the left side you see the thickness of the high stress film on the lower level..

Oh, yes, yes.

I think this is a typo here actually. I remember knowing that earlier. Let me see. The high stress film which is the one on the lower level -- Yes, I know what is wrong. The axis is mislabeled.

The high stress, this is just a simple mathematical exercise. It presumes, as you see --

Yes, if you will look at Column 9, Line 40, if you have the high stress as 10 over the 9, and the low stress is 5 over the 9, that means the

bottom one which is high stress should be 10, so on the right-hand side of this curve you see the stress is 10.

So that should be high stress film as comprising all of the thickness and on the left side where the stress is 5, it should be the low-stress film, the upper-layer film as comprising 100 percent of the thickness.

It is mislabeled. I guess I should have remembered to put that in somewhere.

Q The labeling of high-stress film and the low-stress film should be flipped?

A Yes, exactly.

Q Isn't the lower film, the lower-level layer, the one that fills the contact?

A Yes.

Q Isn't that the low-stress film?

A No, that is the high-stress film. You see the words, high-stress film, lower-level layer, low-stress film, upper-level layer.

I would offer to explain why. but I don't think you need my verbiage anymore.

Q You never know. I might ask. I think I was confusing stress and pressure.

So you deposit the lower level film at a

low pressure to achieve high-step ratio or good conductive hole filling, but you will result in a high-stress film?

A You get a high-stress film because you are depositing under conditions that are kinetically limited, that is the hydrogen to tungsten hexafluoride ratio.

Q Right.

A But it is not tied to the pressure in a direct sense.

Q Sorry, I said type of temperature lower?

A We usually think of stress and pressure.

Q Yes. Tied to temperature though.

A Yes.

Q Lower temperature leads to a higher-stress film. Higher temperature leads to a lower-stress film?

A Right.

Q Let's turn back to Embodiment 3. If we look at Column 7, Line 51, beginning at 51.

A Yes.

Q It talks about filling the contact hole with a diameter of 0.5 microns with a thickness of film at 0.2 microns or more and that the tungsten film has a film thickness not smaller than 40

percent of the diameter of contact hole.

If you deposited a layer of .2 microns into the .5 micron diameter hole, would the entire hole be filled?

MR. MUKERJI: Objection, outside the scope.

THE WITNESS: That would require me to speculate on details of profile evolution in this process and that is a tough one to answer. Note that it prescribes not smaller than 40 percent.

BY MR. CHEN:

Q Sure.

A And the way these processes work can get harder to predict as the remaining space closes. Sometimes they form a seam in the microstructure of the film, sometimes they don't. I think what you are getting at is the 50 percent is the right number.

But remember it is growing from the bottom as well, so exactly how that material goes away, I think this is not so clear how the void goes away, but I do not have complete explanation for that question.

(Whereupon, Respondent's Exhibit Number 15 was

marled for Identification.)
(Whereupon, Respondent's Exhibit Number 16 was marled for Identification.)
BY MR. CHEN:
Q I have asked the court reporter to mark as Exhibit 15, a document titled "Silicon Processing for the VLSI Era," the authors are Stanley Wolf and Richard Tauber.
I think we referred to this as the Wolf Reference and I believe that is how you referred to it in your declaration.
A Yes.
Q And I asked the court reporter to mark as Exhibit 16 a document titled "Volume 5, Introduction to Microelectronic Fabrication," authored by Richard C. Jaeger.
I believe we referred to this as the Jaeger Reference as it is referenced in your declaration.
A Okay.
Q Taking a look at Exhibit 16, first.
A 16. Jaeger.
Q Yes, Jaeger. Look at page 5 of Jaeger, Fig. 7.3, it shows aluminum contacts, correct?
A Yes.

Q I just have a question about the formation of aluminum contacts. Is aluminum typically deposited using CVD or PVD?

A Usually PVD.

Q Why is that?

A Because it has been developed for many years. It has a sputtering process. I'm not sure what Aluminum CVD processes are available. There may be some. I haven't looked at that.

Q At least in your experience you haven't encountered Aluminum CVD processes?

A No. CVD processes would be wonderful if they were all available, but they are not so that is a limitation because it depends on what precursor molecules you can actually buy or at least make.

Q In general are CVD processes preferred over PVD processes?

A Well, preferred it depends on what metric you have for that. If you're dealing high aspect ratios in deposition you really typically like to have a CVD process because PVD processes can have high-aspect ratio trenches and increasingly that is what you need to do, but if you want to be able to do something less demanding

in that sense, keep the high rate and do it cheaply and PVD is the choice.

Q Turning now to Exhibit 15 which is the Wolf Reference. I believe you discussed this in paragraphs A-22 to A-31 of your declaration.

A Right.

Q You used the combination of Miyazaki and Wolf to arrive at the particular timing of the depositions, correct?

A Yes, to see if the teaching of Miyazaki with what is known in Wolf about the kinetics of the processes is consistent with some of the claim limitations in the '893, for example, the time required for a certain thickness.

Q If you look at paragraph A-29 of your declaration which is on page 40.

A Yes.

Q I think you did a few calculations and then you arrived at the conclusion that for a .35 micron diameter hole you would deposit a tungsten layer of 1,400 angstroms or less, and at the temperature of 450 degrees it would take 80 seconds to deposit that 14 angstrom layer of tungsten, correct?

A Yes.

Q But that is specific for a .35 micron hole, correct?
A Yes.
Q If few had a .5 micron hole, what layer of thickness of tungsten would you need to use?
A Let's see,.5 micron would be something like 2,000 to 2,500 angstroms.
Q How long would it take then to deposit that 2,000 to 2,500 angstrom thickness at 450 degrees?
A I don't know if I gave that number, but it would be something greater than 100 seconds and the point I was trying to explain earlier is that that is a bit of a fictitious number because under exactly the same conditions, I can change the deposition rate by increasing the flow rates and thereby achieving a higher pressure which is not expressed at all in the teachings of the '893, and as I said, the higher the pressure the higher the impeachment rate, the higher the growth rate, so I will get down below the 100 seconds pretty straight forward and I think anyone of ordinary skill in the art would know how to do that.
Q But if you changed the other conditions like the temperature or the flow rates, it is

possible that those conditions would then be out of the range that is claimed in the '893 patent. correct?

A But remember, I have several knobs I can change and the temperature range is specified in '893, are about 50 degrees broad. That is a lot.

If you look at Fig. 16 on page 37, that I took from the reference we are talking about, this is the Wolf Reference you can see --

Take a look at any one of those parallel curves and recognize that the Y axis is the long plot, and you can see, if I go from 400 to 450, I change the deposition rate a lot, so temperature can accommodate many changes.

Q So lowering the temperature significantly reduces the deposition rate?

A Yes, and for the first level, the via filling -- I am sorry -- the trench filling part, that is the part which is kinectically limited, so that is the part that is most sensitive to temperature and that is why these curves are quite steep.

Q But if you lowered the temperature and you decreased the deposition rate, it would take even longer to deposit the same thickness of

tungsten, correct?

A Right, but I can always increase the temperature as well. It depends on where I start, where are we starting from, and in terms of staying within the range that is specified in '893.

Q I think the range of temperature that is specified for the '893 for the first tungsten layer is between 400 and 450 degrees C?

A Yes.

Q And the calculation that you provided in your declaration was for 450 degrees C?

A Yes.

Q If we were to reduce the temperature within the range provided in the '893 patent, the timing that you calculated in your declaration would only increase?

A That is true. The other variable is the pressure though, so if I wanted a higher rate than 1050, as you see in that chart, the 1050 number comes from the highest pressure of 2 TOR, I know it is a little hard to read, but the one below it is 1 TOR, and if I were go to 4 TOR, I think I would get a big increase in rate again because is the well plot being shown.

I believe I could accommodate the half micron diameter with the width of a trench within the range of parameters consistent with the specification in '893.

Q 4 TOR is not plotted on the Fig. 16 from the Wolf Reference, correct?

A That is right.

Q They did not conduct any experiments at 4 TOR in order to get data points for Fig. 16, correct?

A That is true, but I give two answers. There are many other references for tungsten CVD so probably somebody has done it and if nobody had done it, it would be a very simple exercise to just try it.

The CVD processes are done up to 10 or even 100 TOR. For example there are ozone POS processes which is plasma system CVD that I remember run to 100 TOR. So there is plenty of lending space available.

Q Would 100 TOR be considered a low-pressure process?

A Yes.

Q Where is the dividing line between low pressure and high pressure?

A That's hard. Typically low pressure means you need a pump so there is atmospheric pressure CVD and then you don't need a pump and low pressure is going to be less than that, but requires a pump and all the equipment and baggage that that brings with it.

In fairness most low pressure is of order 1 to 10 TOR or in the milli-TOR range.

MR. CHEN: I will move on to Emesh which is part of a different IPR, so let's just take a quick break.

(Whereupon, a break in the proceedings commenced at 4:53 p.m.and on resuming at 5:09 p.m.)

(Whereupon, Respondent Exhibit Number 17 is marked for Identification.)

(Whereupon, Respondent Exhibit Number 18 is marked for Identification.)

BY MR. CHEN:

Q Dr. Rubloff, I have asked the court reporter to mark as Exhibit 17, Patent No. 5,407,698 which is the Emesh Reference.

I have also asked the court reporter to mark Exhibit 18, a document entitled Integrated Tungsten Plug Fabrication Process," authored by a number of people, the first author being A. Mak

and we will refer to this as the Mak Reference.

Turning to Exhibit 17, the Emesh Reference, does Emesh disclose depositing two layers of tungsten in two different chambers?

A I think I had written about this in my declaration, so let me look for that.

Q I can direct you.

A I think I know the answer.

Q I was just going to direct you to page 45 of your declaration which is where I think you start the discussion of Emesh.

A That doesn't answer the question. I know that Emesh doesn't talk explicitly about describing the use of two chambers, but it does say that it could be done.

Let me find where that is.

B-27 of my declaration, page 62, "Although Emesh doesn't expressly disclose the deposition process in two separate chambers Mak discloses an integrated system.

No, that is not the place I am looking for. Maybe I did not put it there. I don't recall if I am confusing Miyazaki with Emesh.

At any rate, I wrote it in my declaration but it doesn't explicitly disclose

that, so why don't we go from there.

Q I think it is possible that maybe there's some confusion there.

A One of those references says, though we did it in one chamber. It could be done in two separate chambers.

I am used to looking at these that I have annotated and I can find things for you.

Q Emesh doesn't teach explicitly the use of two chambers and that's why you combined Emesh with the Mak Reference, correct?

A Yes.

Q Because you are of the opinion that Mak discloses a multichamber deposition system, correct?

A Yes.

Q Is the reason that Emesh doesn't teach two chamber deposition because Emesh teaches specifically the use of the Varian --

A 5101.

Q Thank you, the Varian 5101?

A I got some of it right. I will not take time to look for which one of these references mentions it, it's pretty brief, but I suspect that Emesh doesn't mention it because they had a 5101

to work with.

The assignee is Northern Telecom, this is an R&D activity, it is not a high-volume manufacturing environment, so they probably wouldn't have had access to the resources to purchase and use a multichamber cluster tool.

The issue is about whether this scheme or using two different deposition conditions for the filling and for the interconnect above it could be sorted out in a single tool. It is not ideal for high volume manufacturing, but to do the R&D it is okay.

Q Varian 5101 is a single chamber CVD reactor system, correct?

A That is right.

Q Turning to Exhibit 18 which is the Mak Reference.

A Yes.

Q What is the specific process taught by the Mak Reference?

A It describes the use of the equipment for CVD tungsten and tungsten etchback.

On page 2, "Blanket tungsten depositions performed in the cold wall single wafer CVD chamber," and then later it talks in the next

paragraph about the etchback process which is the planarized deposition of tungsten.

Q Subsequent to that deposition of tungsten and then the etchback, the next layer that is deposited in Mak is an aluminum layer, correct?

A Yes. I think that is right. Tungsten deposition. Tungsten etchback.

Q If you look at the first page under "Introduction," I think it talks about forming tungsten plugs?

A Yes.

Q And then having aluminum deposit subsequently.

A Yes, okay.

Q So Mak teaches the deposition of a single layer of tungsten, correct?

A Yes.

Q It does not teach the deposition of two layers of tungsten, correct?

A Not explicitly, but by implication. If one of these chambers, the CVD chamber can do tungsten CVD, then the one that looks exactly like it could also do that and have different process deposition conditions.

Q But the specific process that is taught by Mak teaches the deposition of a single layer of tungsten to form plugs followed by an etchback, which is then followed by a deposition of an aluminum layer to form the interconnects, correct?

A Yes, that was, I think, then motivated by the era when all the lateral interconnects were aluminum.

Q Because Mak only teaches the deposition of a single tungsten layer, Mak does not teach two CVD tungsten depositions performed in two different chambers, correct?

A It teaches it by implication, I think. Note that this is a publication from applied materials which is our equipment company and the discussion here, while it mentions some of the process conditions, it doesn't mention very many.

It talks about rates and it talks about equipment-related issues because this is really explaining how the P-5000 is being used for multistep deposition in etching in a single-cluster tool.

So one of ordinary skill in the art would have recognized several things. One is, in the time frame of the '893 patent, which is 96, or

so, the whole world knew about cluster tools, the P-5000 and everyone was moving toward the adoption of this cluster manufacturing techniques.

The demonstration that one of the CVD chambers can do tungsten would make it obvious to any of those skilled in the art that they could use two chambers for tungsten, and I can tell you that applied materials was at Semicon to sell you as many of these as you wanted to do whichever they qualified as processes.

If the tungsten CVD process and tungsten etchback process were qualified at that time, it would have been very obvious to adopt this to do precisely what is taught in the Emesh reference, the Miyazaki Reference, and the '893 Reference.

Q Looking at the Mak Reference at the bottom of page one, then continuing on to page 2, under the heading "Experimental"?

A Yes.

Q There it's kind of describing the use of the applied materials 5000, right?

A Yes.

Q Sorry, the AMAT P-5000?

A The last sentence starting on page 1, it says, "Since the throughput of the etchback

chamber is twice that of the deposition chamber, two deposition chambers CVD, and Watten etchback chamber are typically used." What does that sentence mean? That actually is a very significant sentence in explaining why these tools have been so successful.

If you look at the Cassette IO at the bottom of Fig. 1, there is a load station, you put the initial wafers there, a robot takes them into the cluster tool, puts them in one chamber, processes one, takes it out of there and puts in another chamber, and the process is run, so when you look at factory utilization and efficiency, you want to get wafers through these tools as far as possible. It has a huge effect on what is called cost of ownership.

What that means is, if I want to load balance my ability to get wafers through, I like the CVD process that is half the speed takes twice as long, they have two chambers in the etchback which is twice as fast, they want a chamber and what that means is that throughput through the tool is much better.

In the case of applied to the teaching of Emesh, Miyazaki and '893, what you would do is

you would use two CVD chambers for the slower process, the lower process because that would be slower because it is lower temperature and one chamber for the faster process if the two-to-one ratio is what you ended up arriving at for the filling step of a process and the interconnect step that follows.

That is assuming they have a factor of two difference in throughput.

Q What that sentence that we just read teaches is that you could increase the throughput of your process by running two parallel processes, each process using a different CVD chamber, but sharing the etchback chamber?

A Yes, if you need the etchback chamber. There are four stations here you could use for processes, right, so where it says, I think, expansion, you could make the expansion be in another CVD chamber, devote two of these to the slower of the two layers, one of them to the faster one and not use the etch back chamber, it just depends how you want to configure it, but it is a throughput issue.

Q But specifically for Mak because it only needs to deposit a single layer of CVD tungsten.

They use two separate CVD chambers each chamber for a different process, correct?

A Right, for a different material and this tells us something about an earlier discussion which is it's an aluminum CVD chamber.

You will recall we had the discussion, you asked me about whether aluminum is likely to be deposited by PVD or CVD.

Q Right.

A I had forgotten here is an example of aluminum CVD.

Q Where is this teaching aluminum?

A In the previous declaration.

Q No, no. I mean where does this teach aluminum CVD?

A Does it not? I guess I am making an assumption here, tungsten plugs, no, it doesn't say it explicitly here. I take it back.

Q Are there potential downsides of using two chambers for your tungsten CVD deposition as opposed to a single chamber?

A Yes, downsize to using two. I don't think significant ones unless you're in a cluster tool like this. Well, are you assuming it would be done in a cluster tool?

Q Why don't we start with doing it in a cluster tool.

A In a cluster tool, the only downside is the robot breaks and you cannot get it from one chamber to another.

But for cleanliness control and throughput it is very efficient.

That is much of the reason why people are using these.

If you have two chambers running the lower level and the upper level in a clean room and you have to remove the wafer from the first one and take it to the second one, that requires time because you have to cool down, open the system, take the wafer out maybe through a load lock and then go through that again so there are delays there.

And other than if you use a single chamber, time to change and stabilize the temperature are substantial.

If you were worried about real manufacturing you would probably be quite worried about throughput and so you would probably look very closely at trying not to change the temperature, but rather change the flow rate

conditions for the two levels.

MR. CHEN: I don't have anymore questions.

MR. MUKERJI: I have no questions. I think we are done.

(Whereupon, the deposition concluded at 5:25 p.m. with the witness to read and sign and Mr. Mukerji to make arrangements for the witness to read.)

UNITED STATES OF AMERICA)
ss:
DISTRICT OF COLUMBIA)

I, T. S. HUBBARD, JR., a Notary Public within and for the District of Columbia do hereby certify that the witness whose deposition is hereinbefore set forth was duly sworn and that the within transcript is a true record of the testimony given by such witness.

I further certify that I am not related to any of the parties to this action by blood or marriage and that I am in no way interested in the outcome of this matter.

IN WITNESS WHEREOF, I have hereunto set my hand this 24th day of August 2015.

_____

Thomas S. Hubbard, Jr.
Notary Public District of Columbia
Commission Identification 237435
Sworn in on June 12, 2006
Commission Expires April 30, 2018

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