

1 UNITED STATES PATENT AND TRADEMARK OFFICE

2 BEFORE THE PATENT TRIAL AND APPEAL BOARD

3 Case IPR 2015-00459

4 Patent No. 6,150,244

5 - - - - - x

6 Samsung Electronics Co. LTD.,

7 Samsung Electronics America, Inc.

8 Samsung Semiconductor Inc. and

9 Samsung Austin Semiconductor LLC,

Volume 2 of 2

10 Petitioner,

Pages 263 - 465

11 vs

12 Home Semiconductor Corporation,

13 Patent Owner

14 -----x

15 DEPOSITION OF GARY W. RUBLOFF, PH.D.

16 Washington, D.C.

17 Wednesday, August 19, 2015

18 9:00 a.m.

19 \* \* \* \* \*

\* \* \* 8

Whereupon, this is the deposition of GARY W. RUBLOFF, PH.D. who appeared as a witness called by the RESPONDENT in the above-styled caption, was called and was examined on Wednesday, August 19, 2015, conducted at the offices of Fish & Richardson, P.C., 1425 K Street Northwest, Washington, DC 20005 Virginia, commencing at 9:00 a.m., and was reported and transcribed by T. S. Hubbard, Jr. a notary public for the District of Columbia.

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P R O C E E D I N G S

MR. MUKERJI: The witness remains under  
oath from yesterday.

BY MR. CHEN:

Q Good morning, Dr.~Rubloff.

A Good morning.

Q Dr. Rubloff, did you speak with your  
attorneys last night?

MR. MUKERJI: That is a yes or no  
question.

THE WITNESS: It is a yes or no  
question?

MR. MUKERJI: About anything?

BY MR. CHEN:

Q Did you speak with your attorneys about  
the subject matter about your deposition last  
night?

A No, I spoke with him about a restaurant.

Q And this morning you did not speak with  
him about the subject matter of your deposition  
either, is that correct?

MR. MUKERJI: That would breach the  
privilege.

THE WITNESS: I am sorry?

BY MR. CHEN:

1 Q And this morning you also did not speak  
2 with him about the subject matter?

3 A No.

4 Q Can we look at Exhibit 8 which is your  
5 declaration submitted in connection with the  
6 Samsung IPR '224 patent, and if we could go to  
7 paragraph 12.

8 Paragraph 12 is where you state what you  
9 believe is the person of ordinary skill in the art  
10 for the '244 patent, correct?

11 A Yes.

12 Q You have given the same definition of  
13 "person of ordinary skill in the art for the '244  
14 patent as you did for the '997 patent, correct?

15 A Yes.

16 Q Did you come up with your definition of  
17 a person of ordinary skill in the art for '224  
18 patent separately from the '997 patent?

19 A Yes.

20 Q What did you consider when coming up  
21 with your definition for a person of ordinary  
22 skill in the art for the '224 patent?

23 A I considered what the '224 patent  
24 teaches, what the time frame of the '224 patent  
25 was.

1                   What the state-of-the art at the time  
2                   was like and what skill sets are coming with the  
3                   degrees in universities that people are trained  
4                   with, and the things that they will have to master  
5                   beyond that or at least --

6                   Well, not master this necessarily, but  
7                   to become familiar with by working in the  
8                   environment.

9                   Q     The two to three years of experience in  
10                   semiconductor processing industry that a person of  
11                   ordinary skill would need to have, is that also  
12                   experience in process integration?

13                  A     Yes, it would certainly include that.

14                  Q     Why is it important for them to have  
15                   experience in processing integration with respect  
16                   to the '244 patent?

17                  A     The '224 patent goes through a number of  
18                   process steps to achieve a certain result.

19                         In this case, the raised source drain  
20                   structure and so one really has to understand  
21                   sequences of steps, something about the process  
22                   consequences of each of those steps and what the  
23                   motivation in the architecture of the device  
24                   really is.

25                  Q     When you say that a person of ordinary

1 skill in the art needs to understand the sequence  
2 of steps, why is that important?

3 A The fabrication of a specific device,  
4 the kinds that are treated in the '244 patent will  
5 have one or another paths to realization, so these  
6 will be sequences or possibly different  
7 alternative sequences to achieve the result.

8 Q The sequence of steps will affect the  
9 result?

10 A Yes, the sequence of the steps will  
11 affect the result and the details of those steps  
12 and the substeps will affect the result, some more  
13 than others, and depending on which result we are  
14 talking about because there are numerous  
15 properties of the resulting device and its  
16 constituents that are important, less important,  
17 and so on.

18 Q You also said that a person of ordinary  
19 skill in the art would need to understand the  
20 process consequences of each of those steps.

21 What did you mean by that?

22 A If you will look at a single process, a  
23 unit process, let's say, you can characterize its  
24 consequences usually by multiple metrics.

25 For example, what is the resistivity of



1 the material? What is the breakdown field if it  
2 is an insulator? What is a deposition rate? What  
3 is the conformality and the like?

4 Those are all consequences of how the  
5 process works and how the equipment carries out  
6 that process.

7 Q Then you also said that a person of  
8 ordinary skill in the art would need to understand  
9 what is the motivation in the architecture of the  
10 device, what did you mean by motivation in the  
11 architectural or in the motivation of the  
12 architecture?

13 A If you are looking at the target of the  
14 '244 patent, the goal of the '244 patent, or if  
15 you're looking at the prior art which is very  
16 similar to that of the '224 patent, there is a  
17 goal in mind, and the way you would like to have  
18 the structure look when you are done is part of  
19 the thing that would need to be understood, and  
20 the different ways in which you might get to that  
21 result which things can be substituted for which  
22 things, and the like, there are lots of  
23 considerations there.

24 And in general when I was talking here  
25 about what would be the characteristics of one of

1 one of ordinary skill whether it is the goal of  
2 the '244 patent or any other patent of this type  
3 looking at a device structure and function, you  
4 would need to have some familiarity with how those  
5 things play together.

6 Q How would one of ordinary skill in the  
7 art achieve the goal or the motivation of their  
8 architecture?

9 MR. CHEN: Let me reask that.

10 BY MR. CHEN:

11 Q How would one of ordinary skill in the  
12 art design a process to achieve a specific goal or  
13 motivation of the architecture?

14 MR. MUKERJI: Object to the form.

15 THE WITNESS: What architecture would  
16 you like to talk about? What function?

17 BY MR. CHEN:

18 Q When I asked you why a person of  
19 ordinary skill in the art would need to understand  
20 the motivation of the architecture, you stated  
21 that a person of ordinary skill in the art would  
22 have certain goals in mind and you used the '244  
23 patent as an example?

24 A Yes.

25 Q How would a person of ordinary skill in

1 the art design a process to achieve the goal that  
2 they have for the specific device?

3 MR. MUKERJI: Objection to form.

4 THE WITNESS: That's a very broad  
5 question. Your answer would be, the  
6 technology is here, I want something to  
7 change, I look at what constraints are there,  
8 I look at what processes I have available, my  
9 understanding of those processes and their  
10 consequences for subsequent processes and the  
11 like, and I try to dream up a solution.

12 BY MR. CHEN:

13 Q Is part of achieving the goal the  
14 selection of specific steps and arranging those  
15 steps in a specific sequence?

16 MR. MUKERJI: Objection to the form.

17 THE WITNESS: We are still speaking in  
18 gross generality here.

19 BY MR. CHEN:

20 Q Sure.

21 A But given that in parting some  
22 innovative function to a technology that already  
23 has a kind of existing shell, certainly means  
24 understanding what will change and what will stay  
25 the same, so what processes are there and what

1 order they can be carried out or alternative ways  
2 in which those steps and sequences can be arranged  
3 to achieve a similar result.

4 Q You are of the opinion that with a  
5 specific result in mind that there are multiple  
6 ways that a process could be constructed to  
7 achieve that result, correct?

8 A There may be multiple ways.

9 Q For example, you could have a process  
10 with a certain sequence of steps, that would  
11 achieve a result and you could have another  
12 process with those same steps arranged in a  
13 different order that would achieve the same  
14 result, correct?

15 MR. MUKERJI: Objection to the form.

16 THE WITNESS: I mean in principle this  
17 could happen. More typically there would be  
18 some level of change.

19 If you're talking about rearranging  
20 steps, I have, let's say, eight steps that  
21 achieves a result.

22 In a very general sense you're asking  
23 me, as I understand it, could I exchange  
24 Steps 6 and 8, right, in the cases where I  
25 could achieve approximately the same result

1 by doing that there would be other changes  
2 that I might make to the details of 6 and 8  
3 or to the details of the final structure for  
4 that matter, and the question whether it is  
5 worthwhile is a different question because  
6 you still have to ask the question, "What  
7 things are different from the manufacturing  
8 point of view?"

9 If the resulting structure has somewhat  
10 different properties, they may be better or  
11 they may be worse.

12 The costs and complexity and the yield  
13 price you pay by doing it differently they  
14 could all be different.

15 You cannot predict without going through  
16 an exercise here, a real exercise, not the  
17 kind of hypothetical one which way would be  
18 the preferred way to do it.

19 BY MR. CHEN:

20 Q When you say a real exercise, are you  
21 referring to an actual experimentation with  
22 equipment and a wafer, actually building the  
23 device with the different processes?

24 A I think there would be two stages at  
25 least of looking at this.

1           The first one would be, I have a certain  
2 body of knowledge as one of ordinary skill about  
3 what these steps will do and what modifications  
4 and processes each can make and what the  
5 consequences will be for those steps.

6           Then what the consequences are for the  
7 way in which I arrange these steps and make  
8 modifications to each of those steps in any new  
9 arrangement if needed.

10           That is the kind of thing of "one of  
11 ordinary skill" would be sitting around the  
12 kitchen table or at their desk at work thinking  
13 through and trying to see from their body of  
14 knowledge what they expect is credible and what is  
15 not, so they will go through and I have seen many  
16 people doing exactly this.

17           That is where innovation comes from and  
18 they look at the scenarios and sometimes talk to  
19 colleagues about it, work on the blackboard, erase  
20 things, and so on, it is actually one of the more  
21 interesting exercises, to see whether conceptually  
22 it makes sense.

23           These days they also have significant  
24 tools, modeling tools, computational tools at hand  
25 so they can actually predict whether this is going

1 to work with some degree of accuracy never  
2 complete and then ultimately if you get through  
3 the first stage of conceptualization, the person  
4 of ordinary skill and you may do some modeling  
5 after that, the next stage would be to prototype  
6 it experimentally so you would have to find a way  
7 to use the facilities in a different fashion.

8 From a manufacturing plant you are going  
9 to detract from throughput because you're going to  
10 use the tools for your little experiment, so you  
11 have to do that as a prototype, and then if it is  
12 serious, make a decision whether to commit to the  
13 experiment to determine whether this works at  
14 reasonably high volume.

15 BY MR. CHEN:

16 Q What you just described is part of the  
17 real exercise that would need to be done in order  
18 to determine whether a process step sequence could  
19 be rearranged, correct?

20 MR. MUKERJI: Objection to form.

21 THE WITNESS: I described multiple  
22 levels at which this assessment can be done  
23 starting from a very basic one which is a  
24 blackboard exercise to larger commitments of  
25 resources that usually would only be pursued

1           if the earlier investigations indicated  
2           sufficient benefit to justify the costs of  
3           pursuing it further.

4       BY MR. CHEN:

5           Q     I want to make sure I understand, that  
6           this is the assessment or the real exercise that  
7           would need to be done in order to determine  
8           whether the process step sequence could be  
9           rearranged, correct?

10               MR. MUKERJI:  Objection.

11               THE WITNESS:  It depends on what you  
12           mean by determination.  I can look at a  
13           sequence of steps and the result and I can  
14           play with that on the blackboard and I can  
15           determine, "This is credible.  I think this  
16           will work."

17               But I don't know how well it will work,  
18           right, because I haven't done it, right.

19               On the other hand, one of ordinary skill  
20           or above could look at that and at least say,  
21           "This is very credible," and often what that  
22           will lead to is something kind of in between  
23           in the sense that I see I could restructure  
24           the process, even move steps around or  
25           replace steps or take out steps or add steps



1 or something like that, and I could look at  
2 that carefully and I can analyze it and I can  
3 conclude, "This is doable."

4 I haven't done it yet. I haven't looked  
5 at the process regime specifically for each  
6 of those steps that I need, but I can say  
7 that this is credible.

8 Often the judgment at that point is, "Is  
9 it worth the experimentation to do that?"

10 Very often people decide it is going to  
11 take us weeks, months, something like that to  
12 really test it out or even to refine it  
13 because it may require computational studies  
14 and so decide not to pursue it because there  
15 is a cost in trying anything.

16 BY MR. CHEN:

17 Q Previously, I asked you whether you  
18 could have a process with a certain sequence of  
19 steps that would achieve a particular result and  
20 that you could have another process with those  
21 same steps arranged in a different order that  
22 would achieve the same result.

23 As part of your answer you said, "In  
24 principle this could happen," but said that you  
25 could not predict what would happen without going

1 through the real exercise, not a hypothetical one  
2 in which way would be the preferred way to do it.  
3 That is what you said, correct?

4 MR. MUKERJI: Objection to the form.

5 THE WITNESS: Are you reading from the  
6 transcript or are you paraphrasing?

7 BY MR. CHEN:

8 Q I am reading from the transcript, but  
9 it's a rough right now.

10 You said more. I am trying to shorten  
11 it. Does that sound a fair characterization of  
12 what you said? I can just reask the question.

13 MR. MUKERJI: Objection to the form.

14 THE WITNESS: I don't want to leave the  
15 impression that you only know the answer  
16 after all of this experimentation and  
17 prototyping and manufacturing environment  
18 because that is not the case.

19 BY MR. CHEN:

20 Q Right?

21 A There are plenty very good innovative  
22 ideas that come from that kind of exercise and  
23 appear in patents and are certainly patentable  
24 that may never have seen the manufacturing floor.

25 The problem we are having is you're

1 asking questions in great generality and I don't  
2 understand the relevance to the patent at hand.

3 And I think I'm having trouble making it  
4 sufficiently clear to you that this exercise you  
5 are asking about is hypothetical and it is not a  
6 single level.

7 There is a level that can be done on the  
8 blackboard in an hour's discussion with a couple  
9 of people.

10 There is a level that actually maps it  
11 out and looks at what each step's parameters will  
12 be and maybe into some modeling of that, and then  
13 there are various levels of experimentation, some  
14 of them just on subsets of that sequence that are  
15 seen as the most likely to control what the change  
16 and the result is.

17 BY MR. CHEN:

18 Q What you have described then, are  
19 various levels of analysis that might need to be  
20 done in order to determine whether a process  
21 sequence could be rearranged to achieve a  
22 particular result, correct?

23 A Say the last part again?

24 Q What you described are various levels of  
25 analysis that might need to be done in order to

1 determine whether a process sequence could be  
2 rearranged to achieve a particular result,  
3 correct?

4 A I wouldn't say might. I would say may  
5 or may not be needed to make an assessment of  
6 whether the result could be achieved by a  
7 different arrangement of the process flow.

8 There are modifications and  
9 rearrangements as we are talking about that would  
10 certainly be credible if built upon what one of  
11 ordinary skill understands an etch process does,  
12 what a deposition process does, lithography  
13 constraints, and so on, and for the most part the  
14 people of ordinary skill will be able to determine  
15 whether it is credible, right, but that does not  
16 mean manufacturable because manufacturable has to  
17 do with costs and reliability and yield and all of  
18 these things.

19 But when people do that initial level of  
20 investigation, if they are of ordinary skill or  
21 above, I think they can make a pretty good guess  
22 as to whether it is possible. It doesn't mean it  
23 is practical yet because they haven't done all of  
24 the experiments, but they certainly know what is  
25 credible.

1 Put it another way.

2 I have heard and I have said it any  
3 number of times the statement, "This makes sense.  
4 This is something that ultimately would work or it  
5 is very likely to work," meaning, I don't know, a  
6 high likelihood of doing it.

7 But that doesn't mean we will pursue it  
8 because to actually bring it to manufacturing  
9 entails a substantial cost.

10 That is a situation that is likely to be  
11 possible, but a decision was made not to bring it  
12 into manufacturing so it remains in the category,  
13 "Yes, that is workable."

14 The question is: Are we going to follow  
15 that or not? Does it give us enough advantage to  
16 bother pursuing?

17 Unless you are in research. If you're  
18 in research you can do any of these things.

19 MR. CHEN: Let me make sure I  
20 understand.

21 BY MR. CHEN:

22 Q Is there a difference between something  
23 that is possible and something that is credible?

24 A You're looking for a semantic response  
25 here?

1           Q     You used both terms and I wasn't sure  
2 whether you were using them interchangeably or  
3 whether you were referring to two different levels  
4 of assessment?

5           A     I was trying to talk like an ordinary  
6 person. Excuse me.

7                     MR. CHEN: I appreciate your effort.

8 BY MR. CHEN:

9           Q     You were just using them  
10 interchangeably, then, possible and credible?

11                     MR. MUKERJI: Objection to the form.

12                     THE WITNESS: I think you are putting  
13 too much into my choice of words.

14                     One of ordinary skill considering  
15 various arrangements of structures and  
16 processes and their sequences and the details  
17 thereof come up with something that looks  
18 interesting.

19                     If I call it possible that means, and I  
20 haven't demonstrated it, then is it really  
21 possible, that is a semantic thing that I  
22 haven't thought about, so I don't know how to  
23 deal with that.

24                     If I call it credible I know how to deal  
25 with that because I or a group of us have

1           gone through using what we know about the  
2           art, and we think, "Yes, that should work,"  
3           so it is credible. If it weren't credible we  
4           would say, "That is a dumb idea, so let  
5           forget it."

6 BY MR. CHEN:

7           Q       When you come up with something that is  
8           credible, that does not mean it is manufacturable,  
9           correct?

10           MR. CHEN: Let me reask the question. I  
11           can see where that might be a little bit  
12           difficult for you to answer.

13 BY MR. CHEN:

14           Q       When you have done this assessment and  
15           you and your team come up with a solution that you  
16           believe is credible, that does not mean you have  
17           determined whether it is manufacturable, correct?

18           MR. MUKERJI: Objection to the form.

19           THE WITNESS: It depends what you mean  
20           by manufacturable. If it is credible, then I  
21           believe if a group of ordinary skill has  
22           determined that this is credible, it is  
23           extremely likely that it is manufacturable as  
24           a structure.

25           Whether you would put it into

1 manufacturing given costs and yield and other  
2 considerations, that is a different question.

3 There is a difference between, "Can I  
4 fabricate it?" which is what credibility  
5 says, "Yes, I can fabricate that," and, "Is  
6 it cost effective at the higher levels to  
7 actually manufacture it?"

8 BY MR. CHEN:

9 Q So the performance of those real  
10 exercises that you had discussed earlier that was  
11 to determine whether something is manufacturable  
12 in the sense that you would actually manufacture  
13 it?

14 A No.

15 Q No? Where do all of those real  
16 exercises come in?

17 A Let me give you an example. I think it  
18 is a good example. We use thin film processes of  
19 the kind that you see here to make device  
20 structures which are essentially electro chemical  
21 batteries.

22 I think I mentioned this earlier, so we  
23 use these processes in the sequence and we had the  
24 idea that if we use amortization of aluminum and  
25 we make pore structures out of that and then use a



1 variant of CVD which is called ALD, we could cut  
2 very thin layers inside these tiny pores at each  
3 end and we can put active layers of ion storage  
4 materials at each end and then fill it with  
5 electrolyte we can make a working nano-battery.

6 And we did.

7 We talked about it. We were not sure we  
8 could make it, but we were pretty sure, so it was  
9 credible, right, and we knew it well.

10 It may not be a really good battery  
11 because this is a pretty speculative domain. It  
12 turns out it is really a good battery, so we did  
13 the research experimentation, but we were pretty  
14 sure we could make this structure and so that is a  
15 level of credibility, the performance would have  
16 to have some way of estimating what that might be  
17 and we got that right as well.

18 But that doesn't mean it is  
19 manufacturable at high volume and it doesn't mean  
20 that it is doing going to be cost effective which  
21 probably it will not be in this example.

22 Another example would be something  
23 closer to the subject at hand because the prior  
24 art in the '244 patent shows more than one way of  
25 making a structure for a raised source drain like

1 the '244 is amended at, and in that case the steps  
2 that are involved and the differences in sequence  
3 of those substeps in the different embodiments  
4 that we address, as I wrote in my declaration,  
5 that is very credible because these steps are well  
6 understood and they have been practiced in  
7 combinations like that in other parts of very same  
8 technology.

9 It is all there in my declaration. One  
10 of ordinary skill would know that one can embody  
11 the innovation of the '244 patent in more than one  
12 way.

13 It is much easier to talk about that  
14 than the generalities that we have spent, I don't  
15 know, the last 40 minutes on?

16 Q When those of ordinary skill have  
17 analyzed the process and determined that it is  
18 credible to rearrange the process sequence to  
19 achieve the same innovation --

20 MR. CHEN: Let me give you a specific  
21 example and start over.

22 BY MR. CHEN:

23 Q When those of ordinary skill in the art  
24 have analyzed the process disclosed in the '244  
25 patent, and determined that it is credible to

1 rearrange the process sequence to achieve the same  
2 innovation as the '224 patent, is that rearranged  
3 sequence a new innovation?

4 MR. MUKERJI: Objection to the form.

5 THE WITNESS: You are stating things  
6 incorrectly. The '244 patent was invented,  
7 disclosed, after the ones we are talking  
8 about in the prior art.

9 There were multiple ways to achieve the  
10 raised source drain structure disclosed in  
11 the prior art I have cited here before the  
12 '224 patent, so nobody had to have or look at  
13 the '244 patent to do that, it was already  
14 done.

15 BY MR. CHEN:

16 Q What I'm asking you is, persons of  
17 ordinary skill in the art analyzing the '224  
18 patent, and looking at the '244 process, if they  
19 look at that process and determine that it is  
20 credible to rearrange the process sequence in the  
21 '244 patent, to achieve the same goal or results  
22 that are stated in the '244 patent, have those of  
23 ordinary skill in the art then created a new  
24 innovation?

25 MR. MUKERJI: Objection to the form.

1 THE WITNESS: I can't answer that  
2 question because prior art value in  
3 innovation as I understand it from the patent  
4 law you cannot invent something in hindsight.

5 The '244 wasn't there.

6 I don't want to speculate on what  
7 somebody would learn from the '244 patent to  
8 go back and invent something else.

9 The '244 patent says what it says, but  
10 what it says has been already disclosed in  
11 the prior art so I can't answer your  
12 question.

13 It's a hypothetical.

14 It has got the order of the times wrong  
15 or something.

16 I will clarify.

17 I went through the exercise in all three  
18 of these patents of responding to what I was  
19 asked to do which is to look at the prior  
20 art, identify if in the prior art there were  
21 teachings for each of the claims and the  
22 substeps of each of the claims in these  
23 patents, that is what I did.

24 In doing that to note whether one of  
25 ordinary skill might put together different

1 things that were known at the time and be  
2 motivated to put them together to achieve a  
3 result.

4 The result was not to be, "Can we match  
5 what is in the '244 patent?"

6 My question is: Would people understand  
7 from the prior art I have cited that you  
8 could achieve raised source drain structure  
9 which is shallow doping, that is what it is  
10 all about, in one way or another.

11 BY MR. CHEN:

12 Q Did the prior art you analyzed for the  
13 '244 patent provide a process for achieving raised  
14 source drain structure that had the same process  
15 steps and in the same sequence as disclosed in the  
16 '244 patent?

17 A You said same process steps and  
18 sequence. Some of the prior art had a similar  
19 sequence to that in the specification of the '244  
20 patent and more than one embodiment in the prior  
21 art met the requirements of the claims in the  
22 '244.

23 Q Did the embodiments in the prior art  
24 disclose a process with the same sequence as that  
25 disclosed in the '244 patent?

1 MR. MUKERJI: Objection to form.

2 THE WITNESS: I think it is time to look  
3 at the '244 and make sure I understand what  
4 sequence you are referring to.

5 BY MR. CHEN:

6 Q Sure.

7 A Because the claims indicate a set of  
8 steps, but not necessarily a sequence, and there  
9 are a certain number of embodiments, but each  
10 embodiment will have some sequence, so I wanted to  
11 make sure I understand which sequence you are  
12 talking about.

13 Q If you look at Exhibit 9, which is the  
14 '244 patent.

15 A Right.

16 Q The '244 patent provides a description  
17 of a preferred embodiment and this is beginning at  
18 Column 3 Line 50 and continues to Column 6 Line 8.

19 A Right.

20 Q In preparing your declaration, did you  
21 find any prior art that disclosed a process for  
22 fabricating the device with a raised source drain  
23 that had the same sequence of process steps as  
24 disclosed in the '244 patent?

25 A Yes.

1 Q Which prior art disclosed the same  
2 sequence of process steps?

3 A Nakamura third embodiment, I think it  
4 is. There is the planarization of the insulated  
5 dielectric down to the etch stop layer on the gate  
6 electrode similar to this and so the sequence is  
7 essentially the same.

8 Q Nakamura first embodiment does not  
9 disclose the same sequence, correct?

10 A Nakamura first embodiment has sort of a  
11 different sequence. Let me think about whether I  
12 would properly describe that as a different  
13 sequence.

14 Yes, it is a different sequence, the  
15 first embodiment. Sorry. It is a different  
16 sequence than the '244 specification shows. Let  
17 me make sure I clarify that.

18 Q Is it a different sequence than the '244  
19 Claim 1 if the limitations of Claim 1 were  
20 interpreted to have the listed order of steps?

21 MR. MUKERJI: Objection to the form.

22 THE WITNESS: Claim 1 does not specify  
23 sequence of steps.

24 BY MR. CHEN:

25 Q If Claim 1 were to be performed in the

1 listed order of steps, would Nakamura Embodiment 1  
2 disclose that same order of steps?

3 MR. MUKERJI: Objection to form.

4 THE WITNESS: Wait a minute. I would  
5 like to see the Nakamura reference. I don't  
6 think it has been entered yet.

7 MR. CHEN: I think you are right. Give  
8 me a minute.

9 (Whereupon, Respondent's Exhibit Number 10 was  
10 marled for Identification.)

11 THE WITNESS: Your question is which  
12 embodiment?

13 BY MR. CHEN:

14 Q Embodiment 1.

15 A One.

16 Q Yes.

17 A Let's repeat the question. I believe  
18 your question is: Does Embodiment 1 of Nakamura  
19 represent an equivalent sequence of steps as Claim  
20 1 would be interpreted if it literally said it has  
21 to be this sequence? And the answer is no.

22 Q Yesterday you provided a definition of  
23 raised source and drain and you said that the  
24 raised source drain was the area that was above  
25 the substrate surface.



1 Do you recall that?

2 A I think that is what I said. That is  
3 most of where the material is, the dopants that  
4 were in it are no longer all the way in it.

5 Q So the raised source and drain refers to  
6 the dopant in the source material before that  
7 dopant has been diffused into the substrate after  
8 heat treatment. That was your definition  
9 yesterday, is that correct?

10 A I don't remember exactly what I said.

11 Q Would you stand by that definition?

12 A My recollection is we were talking about  
13 what structure is the raised source drain, and I  
14 said, "I think it is called raised source drain  
15 because it is above the crystalline silicon and  
16 the function which is the important thing is to  
17 supply in communication with the crystalline  
18 silicon a source of dopants that could then  
19 diffuse and form a shallow junction in the  
20 crystalline silicon."

21 Q Is that the understanding of raised  
22 source drain that you used to conduct your  
23 analysis of the '244 patent and the prior art?

24 A I think substantially so. The motive of  
25 a raised source drain is to produce a shallow

1 junction by out diffusion from a structure in  
2 intimate contact with crystalline silicon in the  
3 source and drain regions.

4 So the semantics and we can debate for a  
5 long time about whether one should define the  
6 raised source drain is only the part above the  
7 crystalline silicon surface or the part above the  
8 crystalline silicon surface plus the shallow  
9 junction the dopants that wandered out by  
10 diffusion.

11 I think that is a distinction that is  
12 inconsequential. The point of a raised source  
13 drain is you make a structure which allows shallow  
14 doping by diffusion into the crystalline silicon.

15 Q But you define the raised source drain  
16 as the material above the crystalline silicon,  
17 correct?

18 A I think I did. I think I referred to it  
19 as that. I didn't think I was being asked to make  
20 some kind of formal definition of that.

21 Anyone who looks at these structures one  
22 of ordinary skill in the art knows that the  
23 function is to make shallow doping which you  
24 cannot do the same way by ion implantation,  
25 conventional means and that somewhere along the

1 lines somebody calls it a raised source drain  
2 because there was dope polysilicon above the  
3 crystalline silicon.

4 I didn't find in my investigation an  
5 irrefutable historical statement of who started  
6 the term and precisely what they defined that to  
7 mean if they did define it to mean something and  
8 particularly when I was at North Carolina State  
9 University we had people working on various  
10 versions of shallow junctions and raised source  
11 drain and they used the term pretty loosely.

12 I don't want to pose as if I know more  
13 than they do about a formal definition because it  
14 is the function that matters. I am sorry. The  
15 function and how that function is achieved.

16 Q Did you contact a formal construction of  
17 the term raised source drain when you were  
18 providing your analysis of the '244 patent and the  
19 prior art?

20 A I was asked to look at a number of terms  
21 and I don't recall which ones, so give me a minute  
22 to look for that.

23 In the brief overview in my paragraph  
24 17, I said, "The '244 compares two different  
25 methods of forming the shallow junctions, ion

1 implantation, and the use of a raised source drain  
2 technique.

3 "According to the patent the method  
4 solely using, ... blah, blah, blah.

5 As an alternative, the '244 patent  
6 describes various advantages to the use of raised  
7 source and drain technique to create shallow  
8 junctions and describe their raised source and  
9 raised drained are performed by diffusing dopant  
10 ions into a substrate surface by dope material  
11 formed at the surface regions of a substrate where  
12 the source and drain are to be formed."

13 So this doesn't make a definition. This  
14 is paraphrasing the essence of the '244.

15 Oh, here, terminology. Sorry. Yes,  
16 paragraph 21: "I have considered whether a  
17 broadest reasonable interpretation of the raised  
18 source and raised drain is recited in Claims 1, 5,  
19 6, 14, and 16 is broad enough to encompass a  
20 source and drain formed at least in part by  
21 diffusing dopant ions into a substrate surface by  
22 a dope material formed at the surface regions of a  
23 substrate whether the source and drain are to be  
24 formed," and I believe that a is reasonable  
25 interpretation.

1                   This tells me that what I was saying is  
2                   that the function is to diffuse dopant ions into  
3                   the crystalline silicon surface.

4                   Whether that means that I call the  
5                   raised source and drain a little shallow doping  
6                   region, or shallow doping region, and the  
7                   polysilicon source above it, or just the  
8                   polysilicon source above it, I think, is not the  
9                   important issue here. It is the function that  
10                  matters.

11                 Q     The function of the raised source and  
12                   drain is to diffuse dopant into the substrate,  
13                   correct?

14                 A     Right.

15                 Q     And the reason why the dopants should be  
16                   diffused into substrate is to form the shallow  
17                   junction, correct?

18                 A     That is correct.

19                 Q     It is the shallow junction that is  
20                   actually the source and drain of the device,  
21                   correct?

22                 A     Yes.

23                 Q     The raised source and drain is not the  
24                   source and drain of the device, correct?

25                 A     I haven't made a formal definition of

1     which three dimensional volume is the raised  
2     source and drain.

3                 I said earlier yesterday that I think of  
4     the raised source and drain as the source there  
5     and I really wasn't thinking about a definition of  
6     which volume we are talking about.

7                 What is important here is the function  
8     and the structure that has used that function, I  
9     could conceive of other structures which will  
10    achieve shallow junctions that do not look like  
11    what they are in the '244 or in the embodiments in  
12    the prior art.

13                So raised source and drain means I made  
14    a shallow junction by diffusion into crystalline  
15    silicon and the architecture of structures that  
16    can do that would include various things.

17                I don't think it matters whether I am  
18    talking about defining this volume or the little  
19    piece under it or both of them together as the  
20    raised source and drain.

21                Q     I am trying to understand the definition  
22    you used when you did the analysis of the '244  
23    patent and the prior art?

24                A     Yes.

25                Q     The reason why I am trying to understand

1 it is because raised source and drain is a term  
2 that is used in the '244 patent.

3 A Yes.

4 Q Let me try to go through this again.  
5 You stated that what is important for the  
6 definition of the raised source drain is its  
7 function, correct?

8 A Yes.

9 Q And that the function of the raised  
10 source and drain is to provide dopants that will  
11 then be diffused into the substrate, correct?

12 A Shallow, yes.

13 Q And the reason why they want to diffuse  
14 those dopants into the substrate is to create the  
15 source and drain for the device, correct?

16 A That is correct.

17 Q So the raised source and drain which is  
18 the source of the dopants that will then be  
19 diffused into the substrate to create the source  
20 and drain of the device is different than the  
21 source and drain of the device, correct?

22 MR. MUKERJI: Objection to form.

23 THE WITNESS: I am sorry. Say that  
24 again. I was looking at this.

25 BY MR. CHEN:

1           Q     The raised source and drain which is the  
2     source of the dopants that will be diffused into  
3     the substrate in order to create the source and  
4     drain of the device is different than the actual  
5     source and drain of the device, correct?

6           A     Structurally that is different, yes.  
7     The structure that is the source of the dopant  
8     diffused and the source and drain that follows,  
9     that is right.

10                I think it would be exaggerating the  
11     significance of what I said yesterday which was  
12     saying, "I think the term came from looking", you  
13     have got the source of the dopants above the  
14     crystalline silicon surface to exaggerate the  
15     significance of that into a formal definition. I  
16     stand by the definition here which is the  
17     definition of function.

18               MR. MUKERJI: We have been going for  
19     more than a hour. Dr. Rubloff, do you need a  
20     break?

21               THE WITNESS: I think we should take  
22     break about every hour.

23               MR. CHEN: Let's take a break.  
24     (Whereupon, a break in the proceedings commenced  
25     at 10:30 a.m. and on resuming at 10:40 a.m.)



1 BY MR. CHEN:

2 Q Why not turn to the '244 patent, that is  
3 Exhibit 9. I want to direct your attention to  
4 Column 2, the "Summary of Invention"?

5 A Yes.

6 Q There in the "Summary of Invention,"  
7 starting at Line 30 ending at Line 64.

8 A Yes.

9 Q It describes a process for forming a  
10 device with a raised source drain, correct?

11 A Yes.

12 Q Looking at the sequence here as it is  
13 described in "Summary of Invention," do you see  
14 the step of "exposing the portion of the third  
15 dielectric layer covering the gate electrode  
16 structure by planarizing the top portion of the  
17 fourth dielectric," do you see that, it is at Line  
18 47?

19 A Yes.

20 Q Do you see following that there is  
21 another step, "forming on the substrate a pattern  
22 second resist layer, masking portions of the  
23 fourth dielectric layer," do you see that?

24 A Yes.

25 Q Is it your opinion that those two steps

1 could be performed in the reverse sequence?

2 A Yes.

3 Q It is your opinion that you could form a  
4 patterned resist layer masking portions of the  
5 fourth dielectric layer and then follow that with  
6 a planarization of the fourth dielectric layer?

7 A Planarization usually means all the way  
8 across the wafer, right, so if you had a resist  
9 you really could not planarize another layer  
10 underneath it without losing the resist.

11 But the clause which starts exposing  
12 would be achieved by using the resist to etch the  
13 fourth dielectric layer, and embodiment, I have to  
14 make sure I get the right one, Embodiment 1 of  
15 Nakamura does precisely that.

16 Q Let's focus on the '244 for now. We  
17 will get to Nakamura later.

18 A But it says "exposing". It doesn't say  
19 "planarizing".

20 Q If you look at the limitation, it says,  
21 "Exposing the portion of the third dielectric  
22 layer covering the gate electrode structure by  
23 planarizing the top portion."

24 A Yes, but etching with a resist in place,  
25 a region of the fourth dielectric layer between

1 where the resist masks are would be equivalent to  
2 planarizing that portion because the resist is  
3 here, between whether resist is you are etching  
4 and the etching is a uniform process, so in that  
5 sense it is planarizing it.

6 Q Is it your opinion that any time you  
7 etch with a mask you effectively are also  
8 planarizing, is that correct?

9 A Unless your etch is highly nonuniform  
10 and nobody wants that you are planarizing portions  
11 between the resist mask components because you are  
12 etching uniformly.

13 Q Could you perform chemical mechanical  
14 polishing to planarize with a resist in place?

15 A I think that's unlikely. I don't know  
16 if there are configurations that people might  
17 think about, such as if you wanted to remove the  
18 resist at the same time you might be able to do  
19 that.

20 Q If you want to keep the resist, if you  
21 could?

22 A If you want to keep resist, I think it  
23 is dubious, but I haven't thought about how I  
24 might invent a way to do that.

25 Q You would have to invent a new way?

1           A     I think you would have to invent a new  
2     way. On the other hand, it could happen. There  
3     are plenty of scanning actuation devices that  
4     people think of all kinds of applications for.

5           Q     You stated that planarization usually  
6     means all the way across the wafer. Is that how a  
7     person of ordinary skill in the art would  
8     generally understand the term planarization?

9           A     I think someone of ordinary skill, if  
10    you say, "How is planarization done, does it mean  
11    across the wafer?" they would first think of the  
12    cross-wafer embodiments of planarization, such as  
13    etchback and CMP, but I think that you also think  
14    about what are the consequences of etching, dry  
15    etching when you have a resist mask in place? I  
16    don't think it is a stretch for them to think  
17    about that.

18          Q     In your experience have you ever used  
19    the term planarization to refer to the  
20    consequences of etching with a resist mask?

21          A     Probably not because it is assumed that  
22    you have uniformity of the etching process for the  
23    way the top surface evolves when you are etching  
24    between the regions between the mask.

25                   The criterion for a reasonable dry etch

1 process and an anisotropic etch process is that it  
2 is uniform across a millimeter, if not larger  
3 dimensions, or you wouldn't be using it, so it  
4 means between the features it is uniform etching  
5 which means that it is planarization as well as  
6 etching.

7 Q Are you saying that the dry etch process  
8 is only used where the distance between the masked  
9 regions has to be either a millimeter or larger?

10 A No, no, of course not.

11 Q You said the criteria of a reasonable  
12 dry etch process is uniform across a milliliter if  
13 not larger dimensions. What did you mean by that?

14 A Yes, but that doesn't mean that the  
15 spacing between the photoresist piece is  
16 millimeters, by no means, it is much smaller than  
17 that.

18 It means if I have a substrate, let's  
19 say a large wafer, and I measure the etch rate in  
20 different places across many millimeters, then I  
21 should get essentially the same number.

22 Q If you could turn to your declaration.  
23 It is Exhibit 8, page 32.

24 A Yes.

25 Q If you would look at the bottom of page

1 32, you have referenced a couple figures from the  
2 Nakamura reference, do you see that?

3 A Yes.

4 Q Do you see Fig. 2A?

5 A Yes.

6 Q And do you see that Fig. 2A is the  
7 result of the etch process using the resist mask  
8 28, correct?

9 A It is the initial part of the etch  
10 process.

11 Q But here Layer 26 has been etched using  
12 the resist 28 as a mask, correct?

13 A Yes.

14 Q Is this etch a planarization?

15 A Let me say it this way and I will repeat  
16 what I said before. A dry etch an anisotropic  
17 etch is a local planarization where local means  
18 where the resist mask is not and that may be a  
19 small dimension or larger dimension.

20 Q I don't understand what you just said.  
21 You said a dry etch is a local planarization where  
22 the resist mask is not. What do you mean by  
23 resist mask is not?

24 A A resist mask, I have photoresist in  
25 certain locations, and no photoresist in other

1 locations, between the photoresist components that  
2 are left, during anisotropic etching the etch  
3 takes place of the material underneath, that is  
4 what the purpose of that kind of step is.

5 No one would use a highly non-uniform  
6 etch rate in that process to remove the material  
7 that this patterning is intended to do, so that is  
8 why I am saying that any such etch processes will  
9 locally maintain a planar form, so it is a  
10 planarization step as well as an etch step.

11 In that sense think about etchback,  
12 tungsten etchback, which we will probably talk  
13 about sometime today, in that case, you sputter  
14 the layer that has been deposited away and that is  
15 the same thing that happens, essentially the  
16 chemistry is different, but the same thing that  
17 happens in anisotropic etching and it better be  
18 uniform or it will not be planarizing.

19 Q It is your opinion here that in Fig. 2A  
20 the top portion of Layer 26 has been planarized by  
21 the etching process?

22 A Yes.

23 Q Which part has been planarized by the  
24 etching process?

25 A The part between the Elements 28.

1 Q Even though all of the Layer 26 between  
2 Elements 27 has been etched away?

3 A Even though.

4 Q All of the portions of Layer 26 between  
5 Elements 28 has been etched away?

6 A What I was trying to depict in this  
7 particular portion is the first part of that etch  
8 step which etches the top surface of the Layer 26  
9 uniformly and therefore planarizing down to the  
10 exposed part of the etch stopper Layer 24 that is  
11 on the top of the gate electrode.

12 That is why it corresponds to the words  
13 that you mentioned exposing the portion of the  
14 third dielectric layer covering the gate electrode  
15 structure by planarizing, which I do by  
16 anisotropic etching, the top portion of the fourth  
17 dielectric layer, so I think it matches correctly.  
18 It meets the language of '244.

19 Q How does it match? What portion of the  
20 Layer 26 has been planarized as shown in Fig. 2A?

21 A How does it match? I thought I said  
22 that.

23 Q I don't think it is clear. Could you  
24 explain again how has Layer 26 been planarized as  
25 shown in Fig. 2A?



1 MR. MUKERJI: Objection to the form.

2 THE WITNESS: It has been planarized by  
3 etching. The etching process maintains,  
4 removes the surface and leaves a planar  
5 surface when it does that.

6 BY MR. CHEN:

7 Q Where is the planar surface?

8 A There are several of them because it  
9 keeps moving, but you see the shaded region  
10 between the combination of photoresist, and ILD  
11 materials, the shaded portion there, if you take  
12 the top piece of that, draw a horizontal line,  
13 then take the next one further down from that, and  
14 further down from that, that material that is  
15 being etched is being planarized.

16 Q The etch process that removed Layer 26  
17 here, does it stop in the middle of the shaded  
18 region?

19 A No, the etch process starts from the top  
20 of 26, and with the photoresist mask in place and  
21 it moves down and after a while it encounters the  
22 top surface of Layer 24 on the gate electrode and  
23 it keeps moving down and ultimately gets down to  
24 the top of the etch stop Layer 24.

25 It then has removed all of the ILD and

1 then the succeeding part of that etch goes through  
2 the Layer 24, the etch stop layer leaving the side  
3 wall spacer in place opening the contact to the  
4 diffusion region to what will be the diffusion  
5 region for the raised source drain.

6 Q Is it your opinion that a person of  
7 ordinary skill in the art would understand the  
8 phrase, "planarizing the top portion of the fourth  
9 dielectric layer," to mean etching the fourth  
10 dielectric layer using a resist mask?

11 A That would not be the first thing they  
12 think of. If they hear the word "in isolation" as  
13 you have hypothesized, they would normally think  
14 of tungsten etchback as an example or CMP, of  
15 course.

16 But in the context of the considerations  
17 here, trying to achieve in different ways the  
18 raised source drain function, they would recognize  
19 that as that surface evolves and moves down during  
20 etching, it will remain planar and it is making a  
21 new surface as it etches and that surface is  
22 planar and then follow it down and then it will  
23 contact then start evolving at the silicon nitride  
24 stop layer.

25 It is not the first thing they would

1 think about, but in the context of what is  
2 described here or in the prior art that I have  
3 cited, they will be perfectly comfortable,  
4 recognizing, "Oh, yes, duh, when we developed the  
5 etched process, the first thing we look at is the  
6 uniform and what is the etch rate."

7 And by uniform, I want to know it does  
8 the same thing every place and they realized,  
9 "Yes, that is a planarization."

10 Q The ordinary understanding of the term  
11 planarization as it is used in semiconductor  
12 fabrication is to create a planar or flat surface  
13 across the wafer using techniques like CPM or  
14 etchback, correct?

15 MR. MUKERJI: Objection, outside the  
16 scope. Also as to form.

17 THE WITNESS: I think it is important to  
18 understand the historical context  
19 planarization.

20 For many years it wasn't important  
21 because aspect ratios were small, so when  
22 people started thinking about planarization,  
23 first in etchback techniques, then in CMP  
24 they started thinking about, "Oh, we have to  
25 keep it flat and here are the techniques to

1 do it." That is what people normally think  
2 of first.

3 BY MR. CHEN:

4 Q You agree then that the ordinary  
5 understanding of the term planarization as used in  
6 semiconductor fabrication is to create a planar or  
7 flat surface across the wafer using techniques  
8 like CMP or etchback, right?

9 A No, I do not agree.

10 MR. MUKERJI: Objection, scope and form.

11 THE WITNESS: No, I do not agree.

12 BY MR. CHEN:

13 Q What is the ordinary understanding of  
14 the term planarization?

15 MR. MUKERJI: Objection to form. Hang  
16 on. Let's not talk over each other, that is  
17 first, and secondly, please don't interrupt  
18 his response.

19 MR. CHEN: I thought he was finished.

20 MR. MUKERJI: Were you finished?

21 Complete your response and Mr. Chen will ask  
22 his next question.

23 THE WITNESS: I didn't get started  
24 actually.

25 BY MR. CHEN:

1           Q     I thought you said you did not agree and  
2 then I thought you were done, so please continue.

3           A     I do not agree. As I said a minute ago,  
4 the first thought that most people would have of  
5 ordinary skill would be something like etchback or  
6 CMP because that is when people started thinking  
7 about planarization as a term.

8                     But I could point to the discussion in  
9 the prior art that I have cited - Nakamura - where  
10 they distinguish that there are reasons to try to  
11 make different levels of different structures at  
12 the same height and it has to do with lithographic  
13 depth of focus, so people also think of planarity  
14 alignment in-depth as an important function for  
15 lithography and it is used in the Nakamura  
16 Reference as one of the criteria for weighing  
17 which of the embodiments of a raised source drain  
18 might be more effective and more valuable.

19                    People do think about planarity on the  
20 local level that I am talking about here.

21                    May I add something to that? There's a  
22 really interesting example here. If someone hires  
23 my student to run a deposition tool or an etch  
24 tool and they talk about planarization they would  
25 probably think what most people would think first

1 from that term which is CMP or etchback and  
2 planarity and uniformity across a whole wafer, a  
3 long distance.

4 But if one of ordinary skill, as I have  
5 defined it here, has had enough experience to be  
6 exposed to these kinds of issues where  
7 lithography, etching, and deposition change the  
8 profile, the vertical profile, and the height of  
9 different structures, they won't be very sensitive  
10 to planarity as an issue as well.

11 That one of ordinary skill in the art  
12 would think about CMP, and etchback, but also  
13 about planarity and that's the issue that is  
14 important here.

15 Q Would a person of ordinary skill in the  
16 art reading the phrase "planarizing the top  
17 portion of the fourth dielectric layer," in the  
18 context of the '244 patent, think of the  
19 planarization term to mean forming a planar flat  
20 layer across layer, across the wafer?

21 A If someone were only looking at '244 and  
22 had not looked at prior art, for example, the  
23 prior art that I have cited here they would look  
24 at something like Fig. 4, absent the Resist 30,  
25 and they would think, "What '244 is trying to show

1 here is a global planarization," which is one way,  
2 as '244 shows, and is one of the embodiments in  
3 Nakamura show of achieving the raised source drain  
4 structure.

5 So I agree. They would think about CMP  
6 or etchback.

7 But that is if they are only looking at  
8 this one. If they were doing that blackboard  
9 exercise that we talked at length about earlier  
10 and trying to imagine there is another way to make  
11 this, maybe there is a better way to make it,  
12 maybe there is a way we can even ensure that  
13 things are planar at the end so we can do  
14 lithography properly, they could easily come up  
15 with the other descriptors of planarization that  
16 talk about local planarity associated with etching  
17 through using a resist mask.

18 Q What you said was, if a person of  
19 ordinary skill in the art is looking only at the  
20 '244 patent, that person of ordinary skill in the  
21 art would understand the term planarization to  
22 refer to creating the planar surface across the  
23 entire wafer, correct?

24 MR. MUKERJI: Objection to the form.

25 THE WITNESS: I think what I said was,

1           that would be the natural first thing to  
2           think about because the word planarization  
3           got popular before people started worrying  
4           about depth of field for fine line focusing  
5           in lithography.

6           If you were to ask the same person, "I  
7           have a resist mask in place. You have  
8           qualified the uniformity, the etch rate, so  
9           an anisotropic etch process, is it also  
10          planarizing the surface?" I think they would  
11          say yes because it does.

12 BY MR. CHEN:

13          Q     It is your opinion that a person of  
14          ordinary skill in the art, looking at the '244  
15          patent, would understand the term "planarizing the  
16          top portion of the fourth dielectric layer" to  
17          refer to etching the fourth dielectric layer using  
18          a resist mask, is that correct?

19               MR. MUKERJI: Objection to the form.

20               THE WITNESS: No.

21 BY MR. CHEN:

22          Q     That is not correct, is it? It's your  
23          opinion that a person of ordinary skill in the art  
24          reading the '244 patent would understand the term  
25          "planarizing the top portion of the fourth



1 dielectric layer," to refer to creating a planar  
2 surface for the fourth dielectric layer across the  
3 wafer, correct?

4 MR. MUKERJI: Objection to the m.

5 THE WITNESS: Well, the '244 patent as  
6 you see in, what was it, Fig. 4, if you look  
7 at Fig. 4 and Figure 3, so the scope of what  
8 the '244 was considering, and they only read  
9 that, and they haven't read any of the prior  
10 art or thought about it, they would see in  
11 this case you start with a non-planar  
12 surface, you are going to planarize down and  
13 remove material that is an etching of some  
14 kind, down to the F-stop layer on the gate  
15 electrode, they would think of CMP or  
16 straight etchback across the wafer.

17 That is the first thing because the word  
18 "planarization" as used here, it is only in  
19 the context that doesn't involve the  
20 considerations that an alternative embodiment  
21 gets to the same function of raised source  
22 drain in prior art literature specifies.

23 BY MR. CHEN:

24 Q But is your opinion that if a person of  
25 ordinary skill looked at the prior art like

1 Nakamura, for example, they would then understand  
2 planarization to refer to etching using a resist  
3 mask?

4 A It depends on which embodiment they look  
5 at. Embodiment 3 looks a lot more like the '244.

6 Q A person of ordinary skill in the art  
7 looking at the prior art like Nakamura  
8 specifically looking at Embodiment 1, would then  
9 understand planarization to refer to etching using  
10 a resist mask, is that correct?

11 A I think this is somehow not the right  
12 order to look at this issue.

13 The people who developed the prior art  
14 were trying to achieve a certain result, a raised  
15 source drain structure, and to be consistent with  
16 the formation of the gate electrode, and all the  
17 constraints that one has if you do not want to  
18 totally change the technology, they are looking  
19 for a way to make this structure and to make it  
20 efficient.

21 They go to a blackboard. They start  
22 drawing these structures and the sequence of steps  
23 that would get them to the right structure and  
24 they would come to the situation which I depict on  
25 page 32 which includes an annotated version of

1 Fig. 2A of Nakamura, and they would talk about  
2 that, and they would say, "That will get us  
3 there."

4 That's the important thing because this  
5 is prior art.

6 If someone were to ask the question, "My  
7 guess is that if someone else is going to have  
8 another disclosure or patent later, and they are  
9 going to say it is important to planarize it,  
10 "Does this planarize it?" and their answer would  
11 be, yes, because it is a uniform etch process.

12 I am not trying to say that the first  
13 thought in the mind of such people would be  
14 uniformity of an etch process between pieces of  
15 resists.

16 I'm not trying to say that.

17 The first thought would be CMP and  
18 etchback, but when you're designing the prior art  
19 and you have no idea about '244, you could come up  
20 with this - and Nakamura did - one or more  
21 embodiments that will get there.

22 And if you ask, "What is really  
23 happening?" and what you think is a credible way  
24 to make the raised source drain structure, you  
25 would recognize that in the step of etching the

1 top of ILD Layer 26, you are also keeping it  
2 planar.

3 Q You're saying that a person of ordinary  
4 skill in the art looking at Nakamura Embodiment 1  
5 would understand the term planarization or  
6 planarizing would refer to the etching process  
7 using the resist mask, correct?

8 MR. MUKERJI: Objection to the form.

9 THE WITNESS: You are looking at the  
10 summary of the invention, that is what we are  
11 talking about here, right, the language that  
12 you are trying to get to, is taken from  
13 summary of the invention.

14 BY MR. CHEN:

15 Q My question is about the term  
16 planarization?

17 A But you introduced exposing the portion  
18 of the third dielectric layer covering the gate  
19 electrode structure by planarizing the top portion  
20 of the fourth dielectric layer, right?

21 Q Yes.

22 A And we have now been talking about the  
23 meaning and context of the word planarizing.

24 Q Yes.

25 A Right?

1 Q Right.

2 A Sorry, so could you repeat your  
3 question.

4 Q You said that a person looking at  
5 Nakamura without reference to the '224 patent  
6 would understand that planarizing would encompass  
7 etching using a resist mask.

8 A That is not what I said. What I said  
9 was, if someone walked into that room where they  
10 are developing the ideas in Nakamura or people of  
11 ordinary skill were talking about the Nakamura, if  
12 someone walked in, and said, "What does  
13 planarization mean?" they would say, "Tungsten  
14 etchback, CMP, why do you ask?"

15 Someone on the team that has been  
16 talking to me about the Nakamura innovation, would  
17 say, "Oh, well, someone wondered whether we are  
18 planarizing here?" Someone would say, "Of course  
19 you are. You are etching." Right?

20 That is what they would say. But this  
21 is off track, I think, to what my job in the  
22 declaration is and outside the scope of my  
23 declaration because I was asked to determine  
24 whether I believe Nakamura teaching matches all of  
25 the claims, specifications --

1 I don't get these words right.

2 All of the claims in the '244, and if I  
3 look at Claim 1, for example, in the '224, it  
4 says, "removing the top portion of said fourth  
5 dielectric layer to expose a portion of said third  
6 dielectric layer covering said gate electrode  
7 structure."

8 I don't understand why we are having all  
9 of this discussion about the term planarization in  
10 the context of Nakamura Embodiment 1.

11 Q If the claim read, "Planarizing the  
12 fourth dielectric layer," would Nakamura  
13 Embodiment 1 meet that requirement?

14 MR. MUKERJI: Object to the form and  
15 outside the scope.

16 THE WITNESS: If it had the word  
17 planarize, yes, it would meet it, but it  
18 doesn't say that. So it is outside the  
19 scope.

20 BY MR. CHEN:

21 Q The reason you believe it would meet  
22 that limitation is because you believe that  
23 etching using the resist mask is a form of  
24 planarization?

25 A It is not because I believe. It is

1 because I know.

2 Q You know that because Nakamura teaches  
3 that?

4 A No. If someone had asked me in class  
5 when I am talking about lithography and etching  
6 and I am describing uniformity, they would ask me,  
7 "Is this local planarization what you're talking  
8 about, that region between the resist pieces?" I  
9 say, "Of course it is because we have to have  
10 etches that are uniform."

11 Q Do they have to say local planarization?

12 A They would ask the question. You have  
13 to say local because you are not talking about the  
14 horizon of the earth, or the 12-inches diameter of  
15 the wafer. You are talking about what happens  
16 between the resist pieces and that's the only  
17 place that is being etched.

18 Q They have to specifically tell you that  
19 they are referring to the portion between the  
20 resists?

21 A I don't think so. They would say, "When  
22 you're doing etching and you have a resist mask in  
23 place so you can make the etch cause patterning,  
24 is it planarizing?'.  
25

I would think about it, and I would say,

1 "It is uniform, so it must be planarizing wherever  
2 things are not covered by resist," so between the  
3 resist and from this hole in the resist to that  
4 hole in the resist.

5 Q Does Nakamura use the term planarizing  
6 or planarization to refer to etching using a  
7 resist?

8 A I don't know. Do you want me to look?  
9 I just don't remember. I don't have a computer to  
10 do a search.

11 Q I will help you out. If you will look  
12 at Nakamura which is Exhibit 10, and you look at  
13 Column 10, which is a description, a continuation  
14 of the description of the first embodiment.

15 A Yes, of course, the word is used. It is  
16 a different part of first embodiment.

17 Q And it says there at Column 10, Line 16,  
18 "The surface of the insulation film may be  
19 planarized by CMP."

20 Do you see that?

21 A Right.

22 Q Is Nakamura using the term planarized in  
23 the more ordinary sense to refer to creating a  
24 flat surface across the entire wafer?

25 A Yes.



1 Q Does Nakamura use the term planarize to  
2 refer to the etching process where resist is used?

3 A I don't know the answer to that, I  
4 haven't looked for that. I would doubt it because  
5 people do not usually ask the question that way.

6 The only reason the question is being  
7 asked is that one embodiment which is shown in  
8 '244, describes the inclusion of a planarizing  
9 step, and in that case, that planarizing step can  
10 be global.

11 But if people were thinking about  
12 alternatives to make a raised source drain as they  
13 were in the invention of Nakamura, they think of  
14 other ways to do this, and if you get to that  
15 stage and then someone asks you a question, "Is  
16 that step planarizing?" you realize, yes, it is  
17 planarizing.

18 This is the kind of superfluous effort  
19 to understand whether the Nakamura teaching lines  
20 up with a piece of the specification in '244, that  
21 is really not the issue here, it is outside the  
22 scope.

23 I was asked to see if Nakamura teaches  
24 all the things that are in the claims.

25 Q You did not analyze whether Nakamura

1 teaches the claim which recites planarization of  
2 the fourth dielectric layer, correct?

3 A No, that is not true. I was asked  
4 whether to look carefully at the prior art and to  
5 look at the claims of the '244 and determine  
6 whether the prior art teaches all the things that  
7 are in the claims.

8 Q Did you determine? Did you provide an  
9 opinion whether Nakamura teaches a claim which  
10 recites the step of planarizing the top portion of  
11 the fourth dielectric layer?

12 A Yes, of course, because that is part of  
13 '244.

14 Q Then what were you saying about my  
15 question as being "outside the scope"?

16 A Let's look at the claims. Taking Claim  
17 1 as an example, what Claim 1 says is: "Removing  
18 a top portion of said fourth dielectric layer to  
19 expose a portion of said third dielectric layer  
20 covering said gate electrode."

21 Well, you analyzed whether there is an  
22 embodiment in Nakamura that meets this for  
23 Embodiment 1, I realize, yes, it does that, and  
24 there is no requirement in this phrase that I just  
25 read for anything to be planarizing.

1 Q You did not analyze Nakamura to  
2 determine whether it meets a claim which requires  
3 the planarization of the fourth dielectric?

4 A Of course, I did. Wait. Where are you  
5 referring to in the Nakamura claim? I want to  
6 find it so I'm sure about this where it says  
7 "planarization of the fourth dielectric."

8 Q It doesn't say it in Nakamura.

9 A I'm sorry. In '244, that was the  
10 question.

11 Q I am asking you questions about  
12 planarization and you are saying that you think it  
13 is irrelevant because it is "outside the scope,"  
14 correct?

15 MR. MUKERJI: Objection to the form.

16 THE WITNESS: I am saying that my task  
17 was to look at the claims in the '244 and  
18 determine whether prior art meets all of  
19 these claim limitations and that's what I  
20 did. If I look at these claims which part of  
21 '244 says planarization?

22 BY MR. CHEN:

23 Q Do you believe that the questions  
24 regarding planarization are outside the scope of  
25 your analysis of the '244 patent?

1 MR. MUKERJI: Objection to the form.

2 THE WITNESS: No, because they are  
3 embodiments that use planarization, global  
4 planarization with resist mask in place as  
5 part of an etch process.

6 BY MR. CHEN:

7 Q The '244 patent uses a term  
8 planarization or planarizing to refer to the  
9 ordinary understanding of planarizing which is to  
10 create a flat surface across the wafer, correct?

11 A In the specification, that is right.

12 Q And Nakamura also uses a term  
13 planarization or planarizing to refer to the  
14 ordinary understanding which is to create the flat  
15 surface across the wafer, correct?

16 A In large part, yes.

17 Q You agree that the ordinary  
18 understanding of planarization includes processes  
19 like CMP or etchback, correct?

20 MR. MUKERJI: Objection to the form.

21 THE WITNESS: In the absence of context,  
22 the first thing that that word would suggest  
23 to someone is global planarization, I agree  
24 with that.

25 BY MR. CHEN:

1 Q Global planarization would be performed  
2 by techniques like CMP or etchback, correct?

3 A Yes.

4 Q And you would not conduct global  
5 planarization with a resist mask in place,  
6 correct?

7 A No, that is not true.

8 MR. MUKERJI: Objection to the form.

9 THE WITNESS: No, that is not true. If  
10 I am doing etching, and I have qualified the  
11 etch process as being uniform across the  
12 wafer, which I need to do in manufacturing,  
13 then the etching is also going to be  
14 planarizing the surface that is being  
15 removed.

16 BY MR. CHEN:

17 Q But that is not global planarization,  
18 correct?

19 A Sure it is. It goes from one side of  
20 the wafer to another.

21 Q Where is your resist?

22 A The etch process to first order doesn't  
23 affect the resist, so wherever the etch process  
24 happens is the same, so it is globally planar.

25 Q Is that creating a flat surface across

1 the wafer?

2 A The new surface is a flat surface. What  
3 is the right word for that? Island? Something  
4 like that. I mean it doesn't cover the entire.  
5 The new surface does not cover the entire surface.

6 Q You used the term "global planarization"  
7 to refer to the ordinary understanding.

8 A Yes.

9 Q Which is to create the flat surface  
10 across the wafer?

11 A Across all of the wafer?

12 Q Yes.

13 A Yes.

14 Q That's how I was using the term.

15 A Oh, okay. Let's call it Global 1,  
16 meaning, each and every place on the wafer, and  
17 Global 2 means is it uniform across the wafer  
18 wherever it exists and I will say that that is  
19 what etching does.

20 Q You have used another term, "local  
21 planarization" to refer to etching with a mask, do  
22 you recall that?

23 A Yes, it was for convenience. I am  
24 talking about an etch process in the presence of a  
25 photoresist.

1 Q Let's just use global planarization to  
2 mean the ordinary understanding which is to create  
3 the flat surface across the wafer and then we can  
4 use "local planarization" to refer to "etching  
5 using a resist," is that fair?

6 A But the local planarization can be  
7 uniform at the appropriate points across the  
8 wafer.

9 Q Between the resists?

10 A Yes.

11 Q For global planarization you would not  
12 perform that with a resist in place, correct?

13 A Global planarization by the standard  
14 techniques for "across wafer" process would not be  
15 done nor aligned with resist in place.

16 MR. CHEN: Why don't we take a break.  
17 (Whereupon, a break in the proceedings commenced  
18 at 11:35 a.m. and on resuming at 11:48 a.m.)

19 BY MR. CHEN:

20 Q Dr. Rubloff, I have a question regarding  
21 the etch process using a resist as a mask.

22 When you are performing etching with a  
23 resist and the resist has a pattern in it, let's  
24 take for example it has a pattern, it as a hole,  
25 and you're etching within the hole, is the etch

1 rate at the center of that hole the same as the  
2 etch rate towards the edges of the hole close to  
3 the resist?

4 MR. MUKERJI: Objection to the form.

5 THE WITNESS: You are speaking in  
6 generality about anisotropic etching?

7 BY MR. CHEN:

8 Q Let's talk about anisotropic etching,  
9 yes.

10 A The ideal situation is certainly a  
11 worthy goal of someone doing process development  
12 on etch or equipment design, for etch is to make  
13 that happen to make it uniform.

14 But when you look at the chemistry and  
15 physics of the etch process, it is always more  
16 complicated than that.

17 I mentioned I think yesterday that these  
18 chemistries lead to reaction products that are  
19 deposited on sidewalls, that changes the profile  
20 of essentially the mask as you go down, as you  
21 transfer the mask down through the material you  
22 are etching, if you are depositing on the side  
23 wall, then now you have made a new mask and so  
24 these things are a lot more complicated in  
25 reality.



1                   Then the question I should also add is  
2                   what do you mean when you say "same rate at the  
3                   edge of the hole," as compared to the center?

4                   You need a quantitative expression of  
5                   that. I mean, what would it take to say, yes, it  
6                   is the same. One percent uniformity? 10 percent?  
7                   Do you have a number in mind?

8               Q       No, I mean "the same" as in "exactly the  
9               same."

10             A       That is a word I never use, not in real  
11             life.

12             Q       So the rate is different, but within a  
13             range. Is that what you're saying?

14             A       Think about how the etch process works,  
15             it is different on different length scales for  
16             different reasons, so if it were varying by a  
17             factor of 20 percent or 100 percent or 1,000  
18             percent, you probably would not find it very  
19             useful.

20                   Then there is another scale at which you  
21                   realize that every time atoms are removed they  
22                   happen essentially one at a time, an ion hits this  
23                   location, that atom leaves, so there is  
24                   statistical distribution as well. These things  
25                   are part of the context of your question.

1 Q The problem that you are having with  
2 answering the question, is it the word "same" or  
3 is it "etch rate"?

4 MR. MUKERJI: Objection.

5 BY MR. CHEN:

6 Q I want to understand. What is your  
7 difficulty in providing an answer?

8 MR. MUKERJI: Objection to the form.

9 THE WITNESS: Are you asking if the etch  
10 rate at the center and at the edge is the  
11 same?

12 BY MR. CHEN:

13 Q Yes.

14 A And therefore the vertical profile of  
15 the bottom would be flat?

16 Q Yes.

17 A And "same" means "exactly the same"?

18 Q Yes.

19 A On average the same. What does it mean?

20 Q Exactly the same.

21 A To how many decimal points?

22 Q (No response.)

23 A As I said, I never use the word exact  
24 because it doesn't work that day.

25 Q To measurable decimal points.

1           A       Of the order of what? One percent?

2           Q       Is it one percent different?

3           A       No, I am asking you.

4           Q       I am asking you about the etch rate. Is  
5 it one percent different?

6           A       It depends on the process and without  
7 being specific, I can't make an estimate and I  
8 don't have a comprehensive knowledge of every  
9 process and, I am sorry to say, the situation is  
10 even more complicated and worse than that because  
11 etching, anisotropic etching whichever process you  
12 are talking about, bromine based, chlorine based,  
13 fluorine based, and so on, typically use several  
14 gases, they are a very complex chemistry and the  
15 performance depends on the equipment you are  
16 using.

17                   In the worst case, if I buy a Lam Etcher  
18 Model XXX and I buy another Lam Etcher Model XXX,  
19 I probably will not get exactly the same result in  
20 those two tools.

21           Q       Are you saying that without knowing all  
22 of those specifics, the type of tool, the type of  
23 etching, the number of decimal places, all of  
24 these specific parameters you cannot answer  
25 whether etching using a resist mask will have a

1 different etch rate within the spaces in the  
2 resist as opposed to near the edges of the resist?

3 A I can answer it. It's just a broader  
4 answer than what I think you're trying to ask from  
5 me.

6 Q What is your answer?

7 A What you would like to have in practice  
8 is the ability to etch down through a single  
9 material and have at essentially the same etch  
10 rate across that region from center to edge, to  
11 within you would like to have a percent or  
12 something like that, you might end up with, I  
13 don't know, 10 percent or something like that.

14 That is going through the same material  
15 and that is for a goal, that is what you would  
16 like to have.

17 If you're actually going to use it in  
18 practice that is probably what you need but it  
19 depends a little bit on the application.

20 Q The etch rate in the center is roughly  
21 10 percent faster than the etch rate towards the  
22 edges of the hole?

23 A That is not what I said.

24 Q What did you mean when you said 10  
25 percent?

1           A       I don't know how much you have looked at  
2 what are called SEM cross-sections, so when you're  
3 trying to understand an etch process you are  
4 developing what is called a vertical profile.

5                   Imagine you take the sample and you etch  
6 a hole down into it, and then you cut it  
7 vertically, you take that half of the sample, and  
8 you put it in an electron microscope, you look at  
9 the profile of the material you have just etched,  
10 and as I said, it may taper because there is  
11 sidewall deposition and all kinds of other stuff,  
12 it may have a flat bottom, but it will probably  
13 have some distribution.

14                   It can be concave up. It can be concave  
15 down. It can have corners that are features that  
16 you didn't expect where it gets a little bit  
17 wider.

18                   There are many different variations that  
19 are observed in the practice of etching like that.  
20 That's why it is so difficult to give you simple  
21 answers to the questions you are posing about  
22 etch.

23           Q       What did you mean when you said in  
24 response to my question about whether the etch  
25 rate in the center is the same as the etch rate

1 near the edge, what did you mean when you said you  
2 might end with, "I don't know, 10 percent," or  
3 something like that?

4 A I am just trying to give a ballpark  
5 estimate.

6 Q What did that 10 percent refer to?

7 A For example, if I did an SEM  
8 cross-section measurement, and I quantify what the  
9 shape of the vertical profile is and I look at the  
10 two edges and then I make a depth measurement  
11 across from one etch to the other, and if I were  
12 to take the RMS value of deviation from the exact  
13 same number from the average, let's say it might  
14 be something like 10 percent or it could be 2  
15 percent, or I guess there are configurations that  
16 could be 20 percent, I don't know.

17 I mean, I have seen a lot of SEM  
18 cross-sections and none of them look like the  
19 pictures we draw, but on average they look like  
20 what you want them to or we wouldn't have the  
21 technology.

22 Q Are you saying that in practice the  
23 result of the etch at the bottom of the hole will  
24 always have some contour?

25 A Well, it always has some shape and it

1 may be flatter and more ideal looking or it may be  
2 more deviation from that.

3 Q That depends on the process you used and  
4 the number of other parameters?

5 A Yes, and the equipment, and the gases  
6 and the temperature.

7 I assume there is a specific application  
8 that you have in mind for wanting to understand  
9 how I think about that question.

10 Q We were talking about etching with a  
11 mask previously before the break and I just wanted  
12 to understand some more details about that  
13 process.

14 We can turn back to the '244 patent,  
15 Exhibit 9.

16 A You said Column 9?

17 Q No, Exhibit 9. We are going to look at  
18 Column 6. Look at Claim 1 that begins at Column  
19 6, Line 28.

20 A Yes.

21 Q We covered this a little bit before. It  
22 is your opinion that the step of removing a top  
23 portion of said fourth dielectric layer to expose  
24 a portion of said third dielectric layer covering  
25 said gate electrode structure, and the step of

1 forming on the substrate a pattern second resist  
2 layer to mask portions of the fourth dielectric  
3 layer," it is your opinion that those two steps  
4 could be performed in a different order from how  
5 they are listed in the Claim 1?

6 MR. MUKERJI: Objection to the form.

7 BY MR. CHEN:

8 Q Is that correct?

9 A It is my opinion as I described in the  
10 declaration, that prior art of Nakamura Embodiment  
11 1, meets the limitations of Claim 1 and actually  
12 does use a different order of those two.

13 Q I'm asking you about your interpretation  
14 of Claim 1. Is it your opinion that Claim 1 can  
15 be interpreted so that the step that begins with  
16 removing a top portion of said fourth dielectric  
17 layer can be performed after the step of forming  
18 on the substrate a pattern resist layer?

19 A Yes, it can be done that way and I was  
20 taught that by Nakamura.

21 Q So the reason that you have that  
22 understanding of Claim 1 is because you referenced  
23 Nakamura?

24 MR. MUKERJI: Objection to the form.

25 THE WITNESS: I wouldn't have any reason



1 to think about it or to knock Nakamura if I  
2 hadn't been asked to compare prior art to  
3 '244 so I wouldn't have thought about it and  
4 unless I had been interested in making the  
5 raised source drain, developing a process  
6 flow, and structure to make a raised source  
7 drain, and spent some time thinking about  
8 that and having a blackboard and making  
9 little drawings and musing about it, of  
10 course, I wouldn't have thought about what  
11 order in which to do these and I work in  
12 different things. I don't do this.

13 BY MR. CHEN:

14 Q So you came up with your understanding  
15 that those two steps could be performed in reverse  
16 from the order in which they are listed in a claim  
17 based on your understanding of the Nakamura  
18 reference, is that correct?

19 MR. MUKERJI: Objection to form.

20 THE WITNESS: In part at least, maybe in  
21 total, I haven't thought about that. But  
22 certainly that possibility comes out clearly  
23 from Nakamura.

24 BY MR. CHEN:

25 Q If you were to perform the steps listed

1 in Claim 1, and you performed the step of forming  
2 on the substrate a pattern second resist layer to  
3 mask portions of the fourth dielectric layer,  
4 before you performed the step of removing a top  
5 portion of said fourth dielectric layer to expose  
6 a portion of said third dielectric layer covering  
7 said gate electrode structure, would you end up  
8 with a structure that is different from the  
9 structure you would have if you performed the  
10 steps in the order in which they are listed?

11 A Yes. That is shown in my paragraph 121  
12 which compares Figs. 2C and 6B from Nakamura.

13 Q Which paragraph are you referring to?

14 A 121, page 40.

15 Q I think that is paragraph A-28.

16 A Oh, I'm sorry.

17 Q Moving down to Claim 1, if you will look  
18 at the step that begins at Column 6, Line 53.

19 A We are on '244 now.

20 Q Yes.

21 A Column 6, Line 53.

22 Q Yes.

23 A Yes.

24 Q You see it says, "Removing said fourth  
25 dielectric layer other than said portions masked

1 by said second resist layer to form a plurality of  
2 trenches adjacent to said gate electrode  
3 structure," do you see where it says that?

4 A Yes.

5 Q Would you agree that that clause recites  
6 the specific step for "removing said fourth  
7 dielectric layer using the resist mask?"

8 A Well, it uses the second resist layer as  
9 a mask to etch away the fourth dielectric layer.

10 Q You see following that clause there is  
11 the phrase, "Wherein portions of the substrate are  
12 exposed."

13 A Yes.

14 Q What is your understanding of that  
15 clause where it says, "Wherein portions of the  
16 substrate are exposed"?

17 A Yes, that's all in my disclosure in my  
18 declaration. I thought hard about this question  
19 because I knew the interpretation is important.

20 Starting in paragraph 23, I was asked  
21 what would be the broadest reasonable  
22 interpretation of "at the same time" here to  
23 understand what this means.

24 I will just read you what I said and I  
25 can then embellish as you need.

1 "At the same time it would be broad  
2 enough to cover the same measured to measurable  
3 period during which an etching process continues.

4 "I believe it would because it is not  
5 inconsistent with '244 specifications and one of  
6 ordinary skill would understand it this way."

7 Then there is more about time as in a  
8 dictionary. "Time is the measured to measurable  
9 period during which an action process or condition  
10 exists or continues."

11 So "at the same time" is construable to  
12 mean the same period in which something is  
13 happening.

14 I consider that the clause that you read  
15 is the clause that is where the etch process is  
16 taking place.

17 "In considering what the measured or  
18 measurable period and action process or condition  
19 are, a person of ordinary skill in the art would  
20 turn to the claims and the specification for  
21 context.

22 "The specification of the '244 patent  
23 does not use the term 'at the same time' and the  
24 only recitations of 'at the same time' are in  
25 Claims, 1, 14, and 16 where the term comes after

1 the phrase, 'wherein spacers are formed on  
2 sidewalls of the gate electrode structure.'

3 "This phrase is separated --

4 Now this part is confusing because you  
5 have to parse the punctuation, but I have gone  
6 through that in detail and reviewed it recently.

7 "This phrase is separated by a comma  
8 from other phrases that are listed between the  
9 two; so removing said fourth dielectric layer  
10 other than said portions masked by said resist  
11 layer to form a plurality of trenches adjacent to  
12 said gate electrode and wherein portions of the  
13 substrate are exposed.

14 "Based on the language of the claim, it  
15 appears to me that the term 'at the same time'  
16 could only refer to, (1), the phrase 'wherein  
17 spacers are formed on the side walls of the gate  
18 electrode,' okay, and that means all of the  
19 spacers, "or to refer to all three of the phrases  
20 listed between the successive semicolons.

21 "However, the term 'at the same time'  
22 would not appear to refer to only the phrases  
23 wherein spacers are formed on sidewalls of the  
24 gate electrode structure and wherein portions of  
25 the substrate are exposed to additional

1 punctuation or other indication that distinguishes  
2 these two phrases from the phrase removing said  
3 fourth dielectric layer' other than said portions  
4 masked by said second resist layer to form a  
5 plurality of trenches adjacent to said gate  
6 electrode structure.

7 "Thus, the term 'at same the time' would  
8 appear in either the last phrase of the list or  
9 all three.

10 "In the case that the term 'at the same  
11 time' refers only to the phrase 'wherein spacers  
12 are formed on sidewalls of the gate electrode  
13 structure' the term 'at the same time' would  
14 require that each of the spacers be formed on  
15 sidewalls of the gate electrode structure during  
16 the same measured or measurable period during  
17 which an action process or condition exists or  
18 continues.'"

19 I am sorry, but I need to get a drink.

20 "Alternatively, in the case of the term  
21 'at the same time' refers to all three of the  
22 phrases listed between the successive semicolons,  
23 the term 'at the same time' would require that  
24 during the same measured or measurable period  
25 during which an action, process, or condition

1 exists or continues; (1), said fourth dielectric  
2 layer other than said portions masked by said  
3 second resist layer be removed to form a plurality  
4 of trenches adjacent to gate electrode structure.

5 "(2), portions of the substrate be  
6 exposed.

7 "And (3), spacers be formed on the  
8 sidewalls of the gate electrode structure.

9 "In either case the '244 patent  
10 describes an anisotropic etching process is  
11 utilized to remove the unmasked fourth dielectric  
12 Layer 28 located under Areas 31A and 31B.

13 "This anisotropic process also removes  
14 the portion of the third dielectric Layer 26 on  
15 top of the gate electrode structure 27."

16 Exhibit 1001, paragraph 5, Lines 25 to  
17 30, emphasis is added.

18 "According to the '244 patent, the  
19 entire duration of this anisotropic etching  
20 process is required to remove the said fourth  
21 dielectric layer other than said portions masked  
22 by said second resist layer to exposed portions of  
23 the substrate.

24 And (3), form spacers on sidewalls of  
25 the gate electrode structure.

1                    "In fact, as illustrated in the  
2 following annotation of the '244 patent's Fig. 4,  
3 no portion of the substrate is exposed until the  
4 very end of the anisotropic process, i.e., after  
5 the fourth dielectric layer and then the third  
6 dielectric layer are removed."

7                    Let me see if I need to go further.  
8 Yes, this gets long. But I would like to have it  
9 specific in the record.

10                   "29. Moreover, etching occurs at a  
11 certain rate due to the exposure of a material to  
12 an etchant. See Exhibit 1006 pages 77 to 79.

13                   "By its very nature any anisotropic  
14 etching process would eat away at a certain rate  
15 the fourth dielectric and then the third  
16 dielectric layer starting from the exposed areas  
17 31A and 31B showing Fig. 4 and working vertically  
18 downward to the surface of the Substrate 10.

19                   "Thus, as shown in the following  
20 annotation of Fig. 5 of the '244 patent, the  
21 formation of the sidewalls highlighted in yellow  
22 would occur through this anisotropic etching  
23 process because they would be exposed as the  
24 etching process worked vertically downward.

25                   "30, the '244 patent does not indicate



1 the number of actions that are operations that are  
2 part of the above described anisotropic etching  
3 process or the amount of time over which it  
4 takes."

5 THE WITNESS: If you are going to look  
6 at this anyway later, I can probably skip the  
7 dictionary and pages stuff. Is everybody  
8 okay with that?

9 THE REPORTER: Counsel is nodding?

10 MR. CHEN: Yes, I am okay with him  
11 skipping the citations.

12 THE WITNESS: The reporter would be  
13 happy for me to skip through them. Me too.

14 "Moreover, independent Claims 1, 14, and  
15 16, do not appear to limit the removing of  
16 said fourth dielectric layer to anisotropic  
17 etching.

18 "Thus the action process or condition  
19 that defines the period during which the  
20 above noted claim phrases are considered to  
21 occur is an etching process which may include  
22 multiple actions or operations."

23 Parenthetically, let me add that we had  
24 this discussion earlier about a process step  
25 typically has substeps in it as well.

1           Going back to the text.

2           "31, in view of the foregoing, I believe  
3           the broadest reasonable interpretation of 'at  
4           the same time' is the same measured to  
5           measurable period during which an etching  
6           process continues.

7           "When applied to the claims in which is  
8           resided the term 'at the same time' is broad  
9           enough to encompass either that, (1), that  
10          each of the spacers are formed on sidewalls  
11          of the gate electrode structure during the  
12          same etching process, or (2), that during the  
13          same etching process,

14          "(a), said fourth dielectric layer,  
15          other than said portions masked by said  
16          second resist layer is removed to form a  
17          plurality of trenches adjacent to said gate  
18          electrodes.

19          "(b) portions of the substrate are  
20          exposed.

21          "And (c), spacers are formed on the  
22          sidewalls of the gate electrode structure.

23          "32, I have considered whether a  
24          broadest reasonable interpretation of the  
25          claims would require the steps of 'removing a

1 top portion of said second or fourth,  
2 depending on which claim we are talking  
3 about, dielectric layer to expose a portion  
4 of said first or third dielectric layer  
5 covering gate electrode structure and  
6 'forming on the substrate a patterned second  
7 resist layer to masked portions of said the  
8 second fourth dielectric be performed in that  
9 particular order.

10 "In light of the claim language, I do  
11 not believe one of ordinary skill in the art  
12 would ascribe a specific order to these  
13 steps."

14 BY MR. CHEN:

15 Q Dr. Rubloff, if I might interrupt you  
16 for a second.

17 A Yes.

18 Q I think the portion of your declaration  
19 that relates to the construction of 'at the same  
20 time' ended with paragraph 31. I believe  
21 paragraph 32 you have moved on to a different  
22 topic.

23 That is not correct.

24 A But I was trying to deal with the fact  
25 that part of the claim that you asked me to

1 address includes the 'at the same time' part, but  
2 it also includes the question of what happens  
3 during a process.

4 Q I am sorry, I did not know what --

5 A I was trying to get to the right thing.

6 Q Please continue. You already read 32.

7 A Thank you. "33, in Claims 1, 14, and  
8 16, the step of forming on the substrate a  
9 patterned second resist layer does not include any  
10 language that it would imply, it should be  
11 performed after the step of removing a top portion  
12 of said dielectric layer, the second fourth  
13 dielectric layer.

14 "For example, the forming step does not  
15 mention details recited in the removing steps such  
16 as removed top portion or the exposed portion of  
17 said first third dielectric layer.

18 "Rather the forming step simply recites  
19 that the patterned second or second resist layer  
20 is formed on the substrate."

21 I think we are almost there.

22 "Moreover, Claims 4 and 15 explicitly  
23 use temporal language wherein said step comprises  
24 two consecutive steps of which the independent  
25 claims do not.

1                    "In fact the independent claims  
2 themselves use the word sequentially to define a  
3 temporal relationship between the deposition of  
4 dielectric layers, i.e., depositing sequentially a  
5 first third dielectric layer and a second fourth  
6 dielectric layer on said substrate and said gate  
7 electrode structure.

8                    "The above noted removing in forming  
9 steps do not contain any temporal language of this  
10 kind.

11                   "35, accordingly, I do not believe that  
12 the broadest reasonable interpretation of the  
13 claims would require that the steps of 'removing a  
14 top portion of said second or fourth dielectric  
15 layer to expose a portion of said first or third  
16 dielectric layer recovering said gate electrode  
17 structure' and 'forming on the substrate a  
18 patterned second resist layer to masked portions  
19 of said the second fourth dielectric layer to be  
20 performed in the particular order."

21            Q        Are you finished?

22            A        I am finished reading. Did I answer  
23 your question?

24            Q        Not to my understanding. I will repeat  
25 the question with a copy of that. The answer is

1 simply a recitation of a number of pages from your  
2 declaration.

3 You can just say, "I have nothing more  
4 to say than what is in my declaration," without  
5 just reading it all into the record, if that helps  
6 you.

7 If you want to read it all again, that  
8 is up to you. So my question was: Looking at the  
9 limitation that begins with removing said fourth  
10 dielectric layer other than said portions masked  
11 by the second resist layer," do you see that?

12 A Yes.

13 Q We agree that that clause there recites  
14 a step for removing the fourth dielectric layer  
15 using the resist mask, correct?

16 A The clause up to the comma?

17 Q Yes.

18 A Yes.

19 Q My question was: Following the comma,  
20 there is another phrase that says, "Wherein  
21 portions of the substrate are exposed." Do you  
22 see that?

23 A Yes.

24 Q My question was: "What is your  
25 understanding of that clause wherein portions of

1 the substrate are exposed?"

2 A My understanding of, is it a paragraph  
3 of three things are with two "whereins" and 'at  
4 the same time' this is describing what happens in  
5 a single etch step using the resist layer to drill  
6 through the two layers of dielectric.

7 Q The clause, "Wherein portions of the  
8 substrate are exposed," is something that has to  
9 occur during the step of "removing said fourth  
10 dielectric layer other than said portions masked  
11 by the said second resist layer," correct?

12 A Yes.

13 Q And this next clause, "Wherein spacers  
14 are formed on the side walls of the gate electrode  
15 structure at the same time," isn't something else  
16 that also has to occur during the step of  
17 "removing said fourth dielectric layer other than  
18 said portions masked by said second resist layer,"  
19 correct?

20 A As in all three of those things should  
21 be part of the etch step.

22 Q The etch step where you use the resist  
23 as a mask, correct?

24 A Yes.

25 Q Before you had stated that it is your

1 opinion that Nakamura Embodiment 1 satisfies all  
2 the limitations of Claim 1, correct?

3 A Yes.

4 Q In Nakamura you believe Nakamura  
5 Embodiment 1 satisfies all the limitations of  
6 Claim 1 because it performs all of the steps  
7 listed in Claim 1, correct?

8 A That is correct.

9 Q Would Nakamura Embodiment 1 satisfy all  
10 the limitations of Claim 1 if it did not perform  
11 the step of "removing a top portion of said fourth  
12 dielectric layer to expose a portion of said third  
13 dielectric layer covering said gate electrode  
14 structure?"

15 MR. MUKERJI: Objection to form.

16 THE WITNESS: You are asking whether if  
17 it didn't meet part of this paragraph, the  
18 removing part, it will not meet that claim,  
19 is that right?

20 BY MR. CHEN:

21 Q Yes.

22 A Well, the question is: Does Nakamura do  
23 what is said here which is to do three things in a  
24 single etch step, right, and so if it doesn't do  
25 the three things, it does not need it.



1 Q Sorry. Were you finished?

2 A Did you want to rephrase the question?

3 Q I was referring to a different  
4 limitation. I think you were looking at the --

5 A Which one are you referring to?

6 Q I was referring to the one above it,  
7 "removing a top portion of said fourth dielectric  
8 layer to expose a portion of said third dielectric  
9 layer covering said gate electrode structure," so  
10 I will reask the question.

11 Would Nakamura Embodiment 1 meet all the  
12 limitations of Claim 1 if it did not perform that  
13 step which begins with "removing a top portion of  
14 said fourth dielectric layer"?

15 MR. MUKERJI: Objection to the form.

16 THE WITNESS: Nakamura Embodiment 1 you  
17 are asking about?

18 BY MR. CHEN:

19 Q Yes.

20 A Just this one? It has to meet the claim  
21 limitations, so if it doesn't meet one of the  
22 claim limitations then it doesn't meet it.

23 Q So if it did not perform that step then  
24 it would not meet all the limitations of Claim 1,  
25 correct?

1           A     If it didn't achieve what it wanted the  
2     claim limitations specifies, then it wouldn't meet  
3     the claim. Sounds a bit like a cytology.

4           Q     Are you drawing a distinction between  
5     achieving and performing?

6           A     (No answer.)

7           Q     My question was: If it did not perform  
8     all the steps listed in the claim, then it would  
9     not meet the claim limitation, correct?

10          A     The claim limitation is what is written  
11     there, so Nakamura Embodiment 1 either does all of  
12     these things or it doesn't.

13          Q     If Nakamura Embodiment 1 did not perform  
14     the step of "removing a top portion of said fourth  
15     dielectric layer to expose a portion of said  
16     fourth dielectric layer covering said gate  
17     electrode structure," then it would not meet all  
18     the limitations of Claim 1, correct?

19          A     The way you phrased it made it sound  
20     like this is a separate step. The function is  
21     what is important.

22                 But the claim limitation says is, you  
23     have to have a process and process flow which  
24     removes "the top portion of said fourth dielectric  
25     layer to expose a portion of said third dielectric

1 layer covering the gate electrode structure."

2 That may be accomplished while other  
3 things are being accomplished, so I wouldn't call  
4 it "the steps of."

5 Q Is it your opinion that the limitations  
6 in Claim 1 do not recite steps?

7 A I did not say that. They recite  
8 functions. It could be accomplished in steps.  
9 They say what they say. I can ask the question,  
10 did I do in removing the second dielectric layer,  
11 did I deposit sequentially a third dielectric  
12 layer, and so on, it either meets or it doesn't  
13 whether you call it a step or not.

14 Q I want to understand how you understand  
15 Claim 1. Are each of those limitations steps or  
16 just functions?

17 MR. MUKERJI: Objection, form.

18 THE WITNESS: They are what they are. I  
19 don't know what else to say. It either does  
20 what the language says or it doesn't.

21 BY MR. CHEN:

22 Q Right.

23 A I don't want to try to classify steps or  
24 functions or something because this prescribes  
25 what the Claim is talking about.

1 Q Does the Claim require certain steps to  
2 be performed or does it only require that certain  
3 functions are achieved?

4 MR. MUKERJI: Objection to the form.

5 THE WITNESS: It requires what the words  
6 say. I have no other answer for you.

7 BY MR. CHEN:

8 Q You don't have an opinion whether the  
9 claims require steps or functions?

10 A I don't think that is a relevant  
11 question that I need to have an opinion about in  
12 order to make the judgment as to whether the prior  
13 art meets the Claim limitations of '244.

14 Q Did you form an opinion as to whether  
15 the Claim requires a series of steps or just  
16 functions?

17 MR. MUKERJI: Objection to the form.

18 THE WITNESS: Everything in this domain  
19 is carried out in steps. How they are  
20 organized give different functions may cloud  
21 the distinction between those two terms, but  
22 the language of the claim is what is at issue  
23 here and that is the only thing I am looking  
24 at.

25 BY MR. CHEN:

1           Q     Right, and so the language of the Claim,  
2     and let's look specifically at one limitation  
3     within Claim 1, the language, "Removing a top  
4     portion of said fourth dielectric layer to expose  
5     a portion of said third dielectric layer covering  
6     said gate electrode structure," does that  
7     limitation recite a step?

8           A     I think I have answered that question.

9           Q     What is your answer?

10          A     My answer is I can't answer it because  
11     it is irrelevant to the question at hand. It is  
12     outside the scope of my investigation. There was  
13     no reason I needed to go through --

14                 In order to determine whether there was  
15     prior art which meets all the Claim limitations of  
16     '244, I did not have to invent a categorization of  
17     the Claim limitations as steps or functions or  
18     anything like that. I only have to answer the  
19     plain question.

20          Q     In determining whether the prior art met  
21     all the limitations you did not determine whether  
22     the prior art performed all the steps listed in  
23     Claim 1?

24                 MR. MUKERJI: Objection to the form.

25                 THE WITNESS: That's kind of a trick

1 question because you inserted "step" in the  
2 middle of a description of a Claim limitation  
3 and I already said that I analyzed whether  
4 all the things here have been done and taught  
5 in the prior art.

6 BY MR. CHEN:

7 Q Right.

8 A But I did not go through a  
9 categorization of steps.

10 Q What I want to understand is how you  
11 read the Claim. When you were reading the Claim  
12 in the '244 patent, did you make a determination  
13 as to whether the limitations recited steps or  
14 not?

15 A As to whether the limitations recited  
16 steps, no, I don't consider except in situations  
17 like the clause which has at the same time, that  
18 tells me these things have to happen as part of  
19 something together, but other than that, I did not  
20 go through a classification of steps.

21 I went through to see, "Does it do what  
22 the words say?"

23 Q You did not determine whether the  
24 limitation "removing a top portion of said fourth  
25 dielectric layer to expose a portion of said third

1 dielectric layer covering said gate electrode  
2 structure," is a step in a process or not?

3 A I know exactly what the words say. I  
4 know what it means whether it is happening or not.

5 But I didn't worry about whether it is a  
6 step, a separate step, a substep of a process.

7 As I said, I have not attempted to make  
8 a hierarchical categorization like it seems you  
9 are looking for.

10 Q But you would agree that the limitations  
11 refer to something that must be performed in the  
12 process, correct?

13 A Yes, or achieved or a function. If I  
14 remove material, I have achieved something. If I  
15 removed material, I have carried out a function,  
16 whether it is a step or a separate step, or a  
17 substep, that is not what the Claims talk about  
18 because they do not have this temporal character  
19 except as the ones I have pointed out in my  
20 declaration.

21 Q If Nakamura Embodiment 1 did not  
22 perform, "removing a top portion of said fourth  
23 dielectric layer to expose a portion of said third  
24 dielectric layer covering said gate electrode  
25 structure," then it would not have met all the

1 limitations of Claim 1, correct?

2 A Yes.

3 MR. MUKERJI: Objection to the form.

4 THE WITNESS: It has to do what it says  
5 in each limitation.

6 And it does.

7 BY MR. CHEN:

8 Q If you look at the top of Claim 1.

9 A Claim 1.

10 Q Claim 1, yes, do you see the first  
11 clause, it is typically called the preamble. This  
12 is at Column 6, Line 28.

13 You see how it says, "A process of  
14 fabricating on a substrate a semiconductor device  
15 having a raised source, a raised drain, and a gate  
16 electrode structure comprising the steps of:" Do  
17 you see that?

18 A Yes.

19 Q Did you read that clause?

20 A Yes.

21 Q When you were coming up with your  
22 understanding of Claim 1?

23 A Yes.

24 Q What is your understanding of the phrase  
25 "comprising the steps of"?



1           A       Well, at "forming, forming, forming,  
2       removing, depositing," and so on, all have to be  
3       in therein whatever is the prior art if it is to  
4       meet this claim limitation.

5           Q       Does the phrase "comprising the steps  
6       of" mean that each of those limitations in Claim 1  
7       are separate steps?

8                   MR. MUKERJI:   Objection to the form.

9                   THE WITNESS:   That would depend on how  
10       to interpret the word steps, and as I have  
11       said before, its process is typically having  
12       substeps and we already recognized that the  
13       order here is not important.

14                   It is in the constraint of the claims  
15       and that in some cases things have to happen  
16       together, that comes later at the same time,  
17       but I do not take "comprising the steps of"  
18       as a formal designation of separate steps.  
19       It is the function that has to be met for the  
20       result.

21       BY MR. CHEN:

22           Q       It is your opinion that each of those  
23       limitations that came with forming, forming,  
24       forming, removing, depositing, removing, forming,  
25       removing, filling, doping, driving, each of those

1 limitations are not separate steps?

2 MR. MUKERJI: Objection to form.

3 THE WITNESS: You can call them steps,  
4 but this doesn't tell me if they are separate  
5 steps.

6 BY MR. CHEN:

7 Q Does the Claim call them steps?

8 A The Claim calls them steps, but I think  
9 that is a convenient way of saying they could have  
10 easily have said "comprising the following  
11 functions."

12 The following actions.

13 I don't read it as literally requiring  
14 that these be "separate steps."

15 Q When you were interpreting the claim,  
16 even though the Claim said "comprising the steps  
17 of," you did not read the limitations that each be  
18 separate steps?

19 A I look at them as requirements. I am  
20 not an attorney. I am a researcher and I am only  
21 trying to see whether prior art matches on to  
22 achieving all of these things.

23 Q Before you analyzed whether the prior  
24 art matched up with achieving all of these things,  
25 you did form an understanding of what the Claim

1     meant, correct?

2             A     Sure.

3             Q     When you formed your understanding of  
4     what the Claim meant you did not interpret each of  
5     the limitations within the claim as being separate  
6     steps, correct?

7             A     Where I have dealt with patents and the  
8     claims in patents, I usually see a list like this  
9     and the question that comes up immediately, this  
10    is a listing of the pieces that have to be in that  
11    claim and where I see that, the question that  
12    immediately comes up, "Is there a sequence that is  
13    required here?" And I never read the steps as  
14    anything as a formal designation.

15            Q     Ignoring the issue of whether they need  
16    to be in a specific sequence, did you interpret  
17    each of the limitations as each being a separate  
18    step?

19                   MR. MUKERJI: Objection to form.

20                   THE WITNESS: I interpreted each one of  
21    these as a descriptor for what has to happen  
22    according to the prescription of the authors  
23    of the claim, and so whatever it says, my  
24    question is, "Does prior art do the same  
25    thing?" That is all.

1 BY MR. CHEN:

2 Q Even though the claim says "comprising  
3 the steps of."

4 A Yes.

5 Q You would not interpret each of the  
6 limitations as being separate steps within a  
7 process?

8 MR. MUKERJI: Objection to the form.

9 THE WITNESS: I don't think that is  
10 relevant or necessary to do that in order to  
11 understand whether the claim limitations are  
12 being met.

13 BY MR. CHEN:

14 Q So you did not do that?

15 MR. MUKERJI: Objection to the form.

16 BY MR. CHEN:

17 Q Correct?

18 A No, I don't know. I do not have an  
19 answer to that.

20 Q You must know whether you interpreted  
21 each of the limitations as separate steps or not,  
22 right?

23 MR. MUKERJI: Objection to form.

24 THE WITNESS: I read the claims as they  
25 are written. That is really all I have to

1 say about this.

2 BY MR. CHEN:

3 Q You cannot answer yes or no whether you  
4 interpreted the Claims limitations to each refer  
5 to a separate step?

6 MR. MUKERJI: This is now bordering on  
7 harassing the witness. I have been sitting  
8 here counting. This is the seventh time. He  
9 has answered the question. I think we need  
10 to move on.

11 MR. CHEN: Let me read you his answer  
12 because it is a yes or no question of whether  
13 he interpreted the limitations in a certain  
14 way.

15 He can either say yes or he can say no  
16 and he is not saying any of those things. He  
17 is providing other.

18 MR. MUKERJI: You view it as a yes or no  
19 question. He may not view it the same way.  
20 He gave you his answer. Let's move on.

21 BY MR. CHEN:

22 Q Is it your response that you cannot  
23 provide a yes or no answer to my question?

24 A I can't provide a yes or no answer  
25 because the question is irrelevant to the exercise

1     that I did.

2                 I analyzed the Claim. I looked at the  
3     prior art. I asked whether things taught in the  
4     prior art accomplish the things that are listed  
5     here.

6                 Whether these are separate steps or not  
7     doesn't matter because there is nothing which  
8     tells me that they have to be separate steps.

9                 You can call them steps, but "separate  
10    steps" is a different issue. I can't answer your  
11    question.

12                MR. CHEN: Why not we break for lunch.

13                It is 12:35.

14    (Whereupon, a break in the proceedings commenced  
15    at 12:35 p.m. And on resuming at 1:30 p.m.)

16    AFTERNOON SESSION

17    BY MR. CHEN:

18                Q     Dr. Rubloff, let's look at the Nakamura  
19    reference, Exhibit 10. Now you rely on the  
20    Nakamura reference to support your opinion that  
21    the '244 patent is invalid, correct?

22                A     Yes.

23                Q     Nakamura describes a number of different  
24    embodiments, correct?

25                A     Yes.

1 Q And you provided opinions related to the  
2 first and third embodiments, correct?

3 A That is correct.

4 Q You are not relying on any of the other  
5 embodiments in Nakamura to form the basis of your  
6 opinion that the '244 patent is invalid, correct?

7 A No.

8 Q No, as in that is not correct, or no,  
9 you are not relying on any other embodiments?

10 A Sorry. It is not correct. No.

11 Q You are relying on other embodiments?

12 A On some others.

13 Q What other embodiments are you relying  
14 on?

15 A Most specifically, Embodiment 4 is where  
16 the Diopine distribution and diffusion to form the  
17 raised source drain is described.

18 Q Where is your reliance on Embodiment 4  
19 disclosed in your declaration?

20 A It is quoted. Here we are. I think it  
21 is, for example, Column 15.

22 Q Paragraph 15 or what are you referring  
23 to?

24 A The Nakamura patent.

25 Q Where in your declaration are you

1 looking at?

2 A A-30. If you start at Line 31 or 32.

3 "The electrodes 42, 44 are formed of the

4 conducting film material having a large Diopine

5 impurity diffusion coefficient, e.g.,

6 polycrystalline silicon, morphosilicon,

7 metalsilicide that is subjected to suitable

8 thermal treatment to diffuse the Diopine impurity

9 from the electrodes 42, 44 into the silicon

10 substrate to thereby form the source drain

11 diffused layer," and so on.

12 Q Is that portion specific to Embodiment 4

13 or is that just a portion in the patent that is

14 referring to all of the embodiments that are

15 described?

16 A Well, the wording at the start of the

17 fourth embodiment builds on the third embodiment,

18 but I haven't looked closely recently at where it

19 applies to the other embodiments.

20 I think it is fairly general.

21 The whole specification does have a

22 number of embodiments, but the structure is made

23 and the raised source drain diffusion part is

24 described in the fourth embodiment.

25 Q In paragraph A-30 that you just



1       referenced, the first line.

2           A       Sorry.

3           Q       A-30 in your declaration.

4           A       Yes.

5           Q       This is the portion that you said is  
6       referring to Embodiment 4, correct?

7           A       No, it is listed under Embodiment 4.  
8       Embodiment 4 starts its discussion, "The same  
9       numbers of the embodiment is a method for  
10       fabricating semiconductor device according to the  
11       first and third embodiments are represented by the  
12       same reference numbers, not to repeat or to  
13       simplify their explanation.

14                 "Figs. 7A and 7B are sectional views,"  
15       and then it goes on to describe, "and the method  
16       for fabricating a semiconductor device according  
17       to third embodiment, the electrodes are formed,"  
18       et cetera," and then gets down to the diffusion of  
19       dopants.

20          Q       But referring to your declaration.

21          A       Yes.

22          Q       Paragraph A-30, you are quoting from a  
23       portion of the patent which I believe you just  
24       read a portion of, and you have added the  
25       annotation after, "in the above described

1     embodiments," you added, "e.g. the first and third  
2     embodiments."

3             A       Yes.

4             Q       Does that mean that you believe that the  
5     quoted portion from the patent, from Column 15,  
6     Lines 25 to 31 should be applied to the first and  
7     third embodiments?

8             A       Yes.

9             Q       In your declaration you only discuss the  
10    first and third embodiments with reference to  
11    meeting the limitations of the Claims of the '244  
12    patent, correct?

13            A       That is right.

14            Q       You did not provide an opinion as to  
15    whether the fourth embodiment in Nakamura meets  
16    the limitations of the Claims of the '244 patent,  
17    correct?

18            A       Embodiment 1 and Embodiment 3 meet most  
19    of the limitations of Claim 1, for example, and  
20    taken together with the fourth embodiment that  
21    describes the formation of the source drain  
22    diffusion area, together those meet, 1 and 4 or 3  
23    and 4, meet the Claim limitations.

24            Q       You are not relying on Embodiment 2 to  
25    support your opinion that the limitations of the

1 '244 patent, the limitations of the claims of the  
2 '224 patent are met, correct?

3 A I don't know the answer to that unless I  
4 look carefully at Embodiment 2.

5 I read it earlier, but decided that 1  
6 and 3 and the quote from 4 is all that is  
7 necessary.

8 Q In your declaration you did not provide  
9 an opinion regarding whether Embodiment 2 meets  
10 the limitations of the claims of the '224 patent,  
11 correct?

12 A Yes, I didn't address Embodiment 2.

13 Q Do you believe that the quoted portion  
14 of the Nakamura specification, the portion that  
15 you quoted in paragraph A-30, that portion is  
16 actually a description specifically directed at  
17 Embodiment 4?

18 A That's a description of the teaching  
19 which lines up with the last limitation of Claim  
20 1, for example, "Driving said dopants into the  
21 substrate underneath said trenches to form said  
22 raised source and raised drain. "

23 Q You are referring to the '224 patent?

24 A Yes, right, I am sorry.

25 Q My question was: Whether that portion

1 in the Nakamura specification is talking about  
2 Embodiment 4 or was it talking about all of the  
3 other embodiments listed above, 1, 2, 3 or 4?

4 A In Nakamura?

5 Q In Nakamura.

6 A It is clear that that is a concise  
7 description of the formation of the shallow layer  
8 would be applicable to any region that allows for  
9 a doped material to reside just above the  
10 crystalline silicon surface and in particular  
11 Embodiment 1 and Embodiment 3 and there may be  
12 other places where it is applicable as well.

13 Q So that portion is applicable to all of  
14 the embodiments that were listed in Nakamura,  
15 correct?

16 A I haven't concentrated on that recently.  
17 I would have to look in detail.

18 Q But that portion of the specification is  
19 definitely applicable to Nakamura Embodiments 1  
20 and 3, correct?

21 A Yes.

22 Q Other than the portion that we are just  
23 talking about, where it is describing the  
24 diffusion of the source drain regions, you did not  
25 analyze ...

1 MR. CHEN: Let me start over.

2 BY MR. CHEN:

3 Q Other than the portion that we just  
4 mentioned which begins at Column 15, Line 25, and  
5 extends down through Column 15, Line 46, you did  
6 not analyze any other part of Embodiment 4 to  
7 determine whether it meets the limitations of the  
8 claims of the '244 patent, correct?

9 A Let me re-read the fourth embodiment to  
10 see if I can say that or not. I mean I have read  
11 it all.

12 Q The reason I ask is because you did not  
13 mention Embodiment 4 specifically in your  
14 declaration?

15 A I didn't say Embodiment 4. But the  
16 quote was clearly in Embodiment 4.

17 Q I understand that the quote you believe  
18 is applicable to both Embodiments 1 and 3?

19 A Yes.

20 Q But you did not rely on any other  
21 portion of Embodiment 4 to form the basis of the  
22 opinion that you provided in your declaration?

23 A I have to look at that.

24 Q If it will help you to refer to your  
25 declaration, I believe all the discussion of

1 Nakamura begins on page 25 at A-1 and extends  
2 through page 42, the last paragraph in A-31.

3 A I am sorry, the question was if there is  
4 any other part of Embodiment 4 that I relied upon?

5 Q Yes, to form the basis of the opinion  
6 that you included in your declaration.

7 A I think that describes it, yes. Would  
8 you like to repeat the question?

9 Q Other than the portions of the Nakamura  
10 specification which begin at Column 15, Line 25,  
11 and extend through Column 15, Line 46, you did not  
12 analyze or rely on any other portion of Embodiment  
13 4 to form the basis of your opinion that is  
14 included in your declaration, correct?

15 A I don't think there is anything else in  
16 Embodiment 4 that I relied on, but there is some  
17 repetition of things like the use of the stopper  
18 film and so on here that may be worded differently  
19 than in Embodiments 1 and 3, so I would say, yes,  
20 to your question with that kind of caveat that  
21 there may be things that could be interpreted as  
22 important there.

23 Q But for your declaration you relied on  
24 Embodiments 1 and 3 and then the other portion?

25 A That is right.

1 Q Let's talk about the first embodiment in  
2 Nakamura.

3 A First embodiment?

4 Q The first embodiment, yes, and I believe  
5 that begins at Column 9, Line 24. I think you  
6 also begin that discussion at paragraph A-6 of  
7 your declaration.

8 The first step in the process of the  
9 first embodiment is the formation of the isolation  
10 regions, correct?

11 A Yes.

12 Q Then the next step, starting at around  
13 Column 9, Line 37, is the formation of the gate  
14 electrode?

15 A No, there is a gate insulator that is  
16 needed first.

17 Q Is the gate insulation film part of the  
18 gate electrode?

19 A That is another semantics question. Do  
20 you really want to go through this?

21 Q I don't think it is critical, but fine,  
22 let's just say that the next step after formation  
23 of the isolation region is the formation of the  
24 gate insulation film, right?

25 A Yes.

1 Q Then subsequently there is gate  
2 electrodes that are formed on the gate insulation  
3 film, correct?

4 A Yes.

5 Q What is the structure of the gate  
6 electrode?

7 A It is described on the first embodiment  
8 dope polysilicon which is the electrical component  
9 and then a silicon oxide film on the top.

10 Q The silicon oxide film on the top, what  
11 is the purpose of that component?

12 A I think it protects the polysilicon from  
13 exposure and oxidation during the different  
14 process steps that follow and in between the  
15 process steps, that is exposed to air.

16 Q It is for protection purposes?

17 A Yes. In some configurations it serves  
18 as an etch stop as well, but I'm not sure that it  
19 does here, I just don't remember.

20 Q Do you know why Nakamura chose to use  
21 oxide as the material for that insulation film?

22 A No, I don't recall. I don't know if he  
23 said why.

24 Q Would a person of ordinary skill in the  
25 art understand why oxide was chosen as the



1 material?

2 A There are many reasons that people  
3 choose one or the other of insulating film like  
4 that, usually oxide or nitride.

5 Q After the formation of the gate  
6 electrode, if you will look at Column 9, Line 45,  
7 to 53, the next step is the formation, the next  
8 step is to use the gate electrode as a mask to  
9 implant ions to form impurity dope regions,  
10 correct?

11 A Yes.

12 Q And the impurity doped regions are to be  
13 an LDD structure?

14 A Yes, or it describes here also MOD  
15 structure and I believe that is the one that  
16 enables or allows anisotropic diffusion of the  
17 implant during an anneal so that it may go a  
18 little bit under the gate electron and I think  
19 that is depicted as 22 in Fig. 1B.

20 Q What is the LDD structure?

21 A LDD is called lightly doped drain.

22 Q Is that the same thing as lightly doped  
23 well?

24 A No.

25 Q What is the difference?

1           A     A well is a larger region, so when you  
2     do CMOS technology which this all is you need to  
3     make p-channel and n-channel devices, so you start  
4     with a substrate that has one doping site, so some  
5     of the devices have to be in the region, on the  
6     bulk silicon, but once I have to be in a p-region,  
7     you have to make a deeper region not too far from  
8     the surface of the silicon, that is "P" in which  
9     you make the other polarity of the device.

10          Q     Is the MOD structure a lightly doped  
11     well?

12          A     I am not sure. I don't think this is  
13     relevant to the questions here.

14                I haven't spent MY attention on the  
15     implantation dope file, naming conventions or all  
16     the different permutations that can be used to  
17     make them particularly because here we are trying  
18     to concentrate on the raised source drain.

19          Q     So I'm clear. You are not sure whether  
20     MOD structure is a lightly doped well, but you are  
21     sure that an LDD structure is not a lightly doped  
22     well, is that correct?

23          A     I didn't say that. LDD stands for a  
24     lightly doped drain. Oh, I'm sorry. Well? No.

25                A well is different from a source or a

1 drain or a source drain extension or any  
2 permutation thereof. A well is a deeper thing.

3 Q So an LDD structure is not a lightly  
4 doped well, correct?

5 A Right.

6 Q But you do not know whether an MOD  
7 structure is a lightly doped well or not?

8 A Oh, well, no, it is a drain, minimum  
9 overlapped source of drain.

10 Q An MOD structure is also not a lightly  
11 doped well, right?

12 A Right.

13 Q If we can move on down to Line 62,  
14 Column 9, "the next step is the formation of a  
15 silicon nitride etching stopper film," correct?

16 A Yes.

17 Q The purpose of this etching stopper film  
18 is to be used as a stopper for etching the  
19 interlayer insulation film in a later step and a  
20 sidewall insulation film is to be formed on the  
21 sidewalls of the gate electrode, correct?

22 A Yes.

23 Q The sidewall insulation film formed on  
24 the sidewalls of the gate electrode the same thing  
25 as a spacer?

1           A       It serves the role of an electrical  
2 spacer.

3           Q       The next step is beginning at Column 10,  
4 Line 6, is the formation of the interlayer  
5 insulation film, correct?

6           A       Yes.

7           Q       The next step, subsequent to the  
8 formation of the interlayer insulation film is a  
9 planarization of that film, correct?

10          A       Yes.

11          Q       Nakamura describes that planarization  
12 using the process of CMP, correct?

13          A       Yes.

14          Q       The next step is the formation of  
15 patterned photoresist, correct?

16          A       Yes.

17          Q       What does Nakamura say about the pattern  
18 in that photoresist?

19          A       Down on Line 30, it says, "Anisotropic  
20 etching is further conducted with the photoresist  
21 28 as a patterned the etching stopper film 24,  
22 below the interlayer insulation film 26, and as a  
23 result because of the etching stopper film 24  
24 deposit the sidewalls of the gate electrodes 18  
25 and the insulation film 20, even when the etching

1 goes on until a silicon substrate 10 is exposed in  
2 the regions where the source drain diffused layer  
3 are to be formed the etching stopper film on the  
4 sidewall says not removed, to remain as the  
5 sidewall insulation films 30.

6 So the pattern is chosen to be able to  
7 etch ultimately down to the source drain contact  
8 regions and to etch the sidewall region of the  
9 gate electrode such as to form side wall spacers.

10 Then this embodiment, it protects the  
11 center region of the gate electrodes in this  
12 embodiment.

13 Q When you say it protects the central  
14 region of the gate electrodes are you saying that  
15 the mask --

16 A Yes.

17 Q -- covers the gate electrodes so that  
18 they are not etched in the etching process?

19 A It covers part of the gate electrode,  
20 the central part. You can see that in Fig. 2A.

21 Q It says Nakamura in its description, in  
22 its actual description, states that its objective  
23 is to protect only the central part of the gate  
24 electrode?

25 A I don't think it says that, but it

1 certainly says that the etching will produce the  
2 sidewall spacers, so if you do not leave some  
3 opening near the edge of gate electrode for the  
4 etch to take place in forming the resist mask,  
5 then you will not form the sidewall spacer and it  
6 clearly says it will form the side wall spacer.

7 That is down at Column 10, Line 37 or  
8 something like that.

9 It says, "Silicon substrate 10 is  
10 exposed in the regions where the source drain  
11 diffused layer are to be formed.

12 "The etching stopper films 24 are on the  
13 sidewalls is not removed to remain as the sidewall  
14 insulation films 30."

15 Q After the pattern resist form then you  
16 perform your etching process, correct?

17 A Yes.

18 Q That etches the interlayer insulator  
19 film and then it etches the etching stopper film,  
20 correct?

21 A Yes.

22 Q Then the step after that -- well,  
23 actually, Nakamura in terms of a description of  
24 Embodiment 1, says that the step after you finish  
25 your etching is to then do ion implantation,

1 correct?

2 A As you see in Line 40, Nakamura also  
3 says, "that concurrent to that etch contact holes  
4 34, 36 are open in alignment with the gate  
5 electrodes 18 on the regions where the source  
6 drained diffused layer is formed.

7 Q The contact holes are open as a result  
8 of the etching process.

9 A Yes, it is part of the etching process,  
10 right, I just wanted to note that because it is  
11 quite critical here.

12 It is also noteworthy in the paragraph  
13 starting at 43, it basically points out that the  
14 etching stopper film 24 leads to the sidewall  
15 insulation film without requiring a separate one  
16 which sounds very much like the motivation in the  
17 '244 patent.

18 Q If we look at Embodiment 1, Column 11,  
19 this is Nakamura, Column 11, beginning at Line 9,  
20 that is the portion where it is describing the  
21 formation of the conducting film for Embodiment 1,  
22 correct?

23 A Yes.

24 Q You discuss in your declaration at  
25 paragraph A-28 which is on page 39 of your

1 declaration, you say, "With regard to both the  
2 first --

3 A Hold on just a second. A-29?

4 Q A-28, it begins on page 39 of your  
5 declaration and it continues through page 40.

6 In your declaration you say, "With  
7 regard to both the first and third embodiments,"  
8 although we are talking specifically about the  
9 first embodiment right, now, you say, "Nakamura  
10 teaches that a conducting film is deposited on the  
11 entire surface in patterned form electrodes," do  
12 you see that?

13 A Yes.

14 Q Then you provide annotated versions of  
15 Fig. 2C for Embodiment 1 and Fig. 6B for  
16 Embodiment 3, correct?

17 A Yes.

18 Q Then you say, "As is well known in the  
19 art patterning by definition involves removal of a  
20 layer."

21 A Yes, you may remember my discussion  
22 yesterday when we were talking about the  
23 definition of lithography and its relationship to  
24 patterning and I said, "Some people think of  
25 lithography as the optical exposure patterned



1 definition part to clearly those people built  
2 tools for lithography and other people think of  
3 lithography as really the synonym for patterning  
4 where you have to have a waveform image making the  
5 photoresist mask and then using the etch."

6 Q Continuing on at paragraph A-29, you  
7 say, "In summary, because Nakamura is teaching  
8 this patterning process, Nakamura teaches two  
9 consecutive steps of depositing a conductor layer  
10 on a substrate and removing the conductor layer  
11 other than portions filling trenches."

12 Do you see that?

13 A Yes.

14 Q You reference Fig. 2C and I suppose Fig.  
15 6B as well to show that?

16 A Yes.

17 Q It is your opinion that Figs. 2C and 6B  
18 show conductive material only in the trenches,  
19 correct?

20 A I don't know what you mean by "only in  
21 the trenches." They are within the etched regions  
22 through the interlayer dielectric and the sidewall  
23 insulating film and in some areas 24 which was the  
24 etch stopper film, so if that is what you mean by  
25 trenches that is what is shown there.

1           Q     Do those images also show conducting  
2 film or some of the conducting film outside of the  
3 trenches?

4           A     What do you call a trench?

5           Q     Do you have an understanding of the term  
6 trench as it is used in the '244 patent?

7           A     Yes, and let me find where that is used.  
8 Yes, "moving said fourth dielectric layer," blah  
9 blah, "to form plurality of trenches adjacent to  
10 said gate electrode structure." So that would be  
11 the pieces 42 and 44 in Fig. 2C.

12                     Yes, I agree.

13          Q     So the images, Fig 2C and Fig. 6B, do  
14 show some of the conducting film outside of the  
15 trenches, correct?

16          A     I don't think that the 2 and 4 is  
17 specific about whether in --

18                     The answer to your question is yes or no  
19 because it doesn't really define the vertical  
20 profile of the trench.

21                     For example, 42 in Fig 2C, part of that  
22 goes all the way down to the silicon substrate.  
23 Part of it is over the spacer and adjacent to the  
24 ILD and the edge stopper layer.

25                     It depends what you call a trench. Then

1     there is a little bit of that that is over the  
2     ILD, layer 26.

3           Q     Would you consider the portion of the  
4     conducting film that is over the ILD within the  
5     trench?

6           A     I don't know why this is a question. Is  
7     this just a hypothetical question?

8           Q     It is not hypothetical. I am asking you  
9     with reference to the figure whether you would  
10    consider a portion of the conducting film that is  
11    over the ILD within the trench?

12          A     In the context of '244, I assume that's  
13    where your question is aimed, Claim 1, the clause,  
14    the limitation, "removing said fourth dielectric  
15    layer," says, "to form a plurality of trenches  
16    adjacent to said gate electrode structure."

17                In that sense, '244 is defining the  
18    trench to be that part of it that is adjacent to  
19    gate electrode.

20                It is not specific about whether that  
21    includes the cap layer over the polysilicon. If I  
22    take that definition, then some of the conducting  
23    layer is outside of the trench if I take that  
24    definition as inferred from the '244 claim.

25          Q     What if the definition of trench

1 included the portion formed by the cap layer?

2 A The cap layer, the ILD layer?

3 Q The ILD layer, in that case, would some  
4 of the conducting film still be outside of the  
5 trench as shown in Fig 2C and Fig 6B?

6 A If the trench went all the way up to the  
7 top of 26?

8 Q Yes.

9 A And then the question is part of the  
10 conducting film outside of that?

11 Q Yes.

12 A This is a very hypothetical question. I  
13 don't understand the relevance of this question  
14 because it is a semantics question. It does not  
15 bear on what the content of the patents at issue  
16 are.

17 Q I'm asking you about Fig 2C and Fig 6B.  
18 Looking at the figures, do those figures show some  
19 of the conducting film outside of the trench if  
20 the trench went all the way up to the top of the  
21 ILD which is labeled 26.

22 A If I look at that figure and I look at  
23 the profile of 42, the shape of 42, it is the case  
24 that some of 42 appears above 26, but I don't see  
25 any significance whatsoever to that.

1 Q The same is true for both Fig. 2C and  
2 Fig 6B, correct?

3 A Yes. The definition of the 42 structure  
4 and the 44 was the patterning function that was  
5 carried out after deposition of the material into  
6 these trenches, so it would have a different  
7 shape.

8 Q What do you mean so it would have a  
9 different shape? What are you referring to there?

10 A I said it here. I can go to this, A-28.  
11 "With respect to the first and third Embodiments,  
12 Nakamura teaches, "A conducting film is deposited  
13 on the entire surface and patterned to form  
14 electrodes 42, 44." Then it refers to those two  
15 figures.

16 "As is well known in the art, patterning  
17 by definition involves removal of a layer,  
18 therefore Nakamura's disclosure of patterning the  
19 conducting film necessarily teaches removing some  
20 of the conducting film."

21 There would have been, being able to  
22 create these shapes.

23 Blanket deposition of the polysilicon  
24 into these trenches or whatever you call trenches,  
25 and then a photoresist layer put on top of that,

1 it is patterned and then that pattern is used to  
2 etch out the uncovered regions and the periphery  
3 of those regions would be outside of the trench  
4 dimension at the top of the ILD that was created  
5 in the previous etched sequence.

6 I think one of ordinary skill would try  
7 to make the edges outside the inside edges of the  
8 holes in 26, because otherwise, you may have a  
9 seam and that is a reliability concern.

10 MR. CHEN: Let's move on to the  
11 discussion of the third embodiment.

12 MR. MUKERJI: Mr. Chen, it sounds like  
13 you are switching topics slightly. It has  
14 been about an hour, could we take a short  
15 break?

16 MR. CHEN: Sure, if you need one, that  
17 is fine.

18 (Whereupon, a break in the proceedings commenced  
19 at 2:26 p.m. and on resuming at 2:46 p.m.)

20 BY MR. CHEN:

21 Q Dr. Rubloff, we were about to start  
22 talking about the third embodiment in Nakamura.

23 A Yes.

24 Q I believe that begins at Column 12, Line  
25 60.

1 A Yes.

2 Q A lot of the steps in the third  
3 embodiment are similar to first embodiment, so we  
4 will skip it all the way up to --

5 Let's move to Column 13, Line 23. I  
6 think that's where after they form the gate  
7 electrode in the third embodiment, correct?

8 A Correct.

9 Q After they form the gate electrode then  
10 they deposit the etching stopper film, correct?

11 A Yes, that is Line 26.

12 Q Right and that is shown in Fig. 5A on  
13 the Nakamura patent?

14 A Right.

15 Q Then after they deposit etching stopper  
16 film, they deposit the interlayer insulation film,  
17 correct?

18 A Yes.

19 Q Then a planarization removes the  
20 interlayer insulation film all the way down onto  
21 the etching stopper film over the gate, correct?

22 A Yes.

23 Q Then planarization removes interlayer  
24 insulation film all the way down to etching  
25 stopper film over the gate, correct?

1           A     Yes.

2           Q     Do you know why they planarized the  
3     interlayer insulation film all the way down to the  
4     etching stopper film over the gate?

5           A     I think there is a figure which denotes  
6     some benefits of that on page 40 of my  
7     declaration. I think what you can see is that the  
8     structure is shorter, the resulting structure  
9     would be shorter and more planar.

10           I think one of the embodiments, and I  
11     don't recall which one, speaks to this question  
12     that I described earlier, the depth of field,  
13     focusing on lithography and more planar things can  
14     be across the various required structures, the  
15     easier it is to do lithography well.

16           I don't know if that is only motivation,  
17     but that certainly is one.

18           Q     I believe you're talking about this  
19     specific planarization at page 35 of your  
20     declaration and continuing on to page 36.

21           A     Yes.

22           Q     Following the planarization step, there  
23     is the formation of a photoresist, the pattern  
24     resist?

25           A     Yes.



1 Q After the form pattern resist, then  
2 after the formation of the pattern resist,  
3 Nakamura Embodiment 3 teaches the beginning of the  
4 etching process, correct?

5 A Yes.

6 Q In the first stage of the etch process  
7 the unmasked portions of the interlayer insulation  
8 film are removed, correct?

9 A Yes.

10 Q What happens after that etch is  
11 completed?

12 A In the description of the third  
13 Embodiment the photoresist is then removed. This  
14 is Line 39.

15 Q Of Column?

16 A I am sorry, no, it is later than that.  
17 Sorry, Column 13, Line 47.

18 Q How is the photoresist removed?

19 A It does not specify.

20 Q How would a person of ordinary skill in  
21 the art understand would be needed --

22 MR. CHEN: Let me rephrase that.

23 BY MR. CHEN:

24 Q What would a person of ordinary skill in  
25 the art understand is the process to remove the

1 photoresist?

2 A The simplest one is by wet chemical  
3 techniques to dissolve the photoresist.

4 There are other techniques that can be  
5 used depending on conditions, more specifically  
6 ashing, any organic can be ashed which means  
7 volatilize it in a oxygen containing plasma.

8 Q Is the removal of the photoresist done  
9 in the same tool as the etching process?

10 A The specification doesn't really tell us  
11 that.

12 Q Typically, is the removal of the  
13 photoresist done in the same tool as the tool used  
14 to perform an etch?

15 A No.

16 Q Typically the wafer would need to be  
17 moved from the tool that does the etch to the tool  
18 that will remove the photoresist, correct?

19 A Most typically, but there are situations  
20 where it could be done in situ, whether it is  
21 advisable or not depends on the situation.

22 Q What do you mean "advisable or not"?

23 A These etching tools are chemically  
24 temperamental sometimes, and particularly dry  
25 etching, so in principle one could do the etch,

1 change the gases, use a similar power in the  
2 plasma, change the bias probably on the electrodes  
3 and use oxygen to remove the photoresist in the  
4 form of CO and CO2 and then change back.

5 I think that would be possible but it is  
6 not clear if it would be workable in this  
7 configuration.

8 It probably depends on how sensitive the  
9 etch is in this case. To summarize, the natural  
10 way to do it is to remove it from the tool, do wet  
11 etch or wet dissolution of the photoresist and  
12 then go back in the tool to finish the etch.

13 Q Is it important to remove all of the  
14 photoresist material?

15 A Yes, I think it is certainly advisable.

16 Q Why is that?

17 A If you didn't remove all of it, then  
18 when you continue the etch it will be etched away  
19 by the etch that you are using to finish the  
20 intended etch and that is probably not a great  
21 idea. Unless you develop the special process.

22 Q How long does it usually take to remove  
23 the photoresist? How long does the process of  
24 removing the photoresist usually take?

25 A I am not quite sure which parts. If you

1 want to go from the photoresist on the wafer you  
2 can take the wafer out of the etch tool and put in  
3 another tool you will dissolve away the  
4 photoresist and then you are going to take it out  
5 and put it back in etch tool, I would guess it is  
6 some minutes, a few minutes, I don't really know.

7 Q In Nakamura Embodiment 3 after the  
8 photoresist has been removed, then more etching is  
9 performed, correct?

10 A Yes.

11 Q This second stage is different than the  
12 first stage, correct?

13 A Yes, I think that is right, but let me  
14 look again .... yes.

15 Q The etch chemistry is adjusted?

16 A Yes.

17 Q What is being etched during the second  
18 stage?

19 A The ILD film 26, and etch stopper film  
20 24, have to be removed.

21 Q Why are both materials removed?

22 A The material 24, the etch stopper film  
23 in the Fig. 6A, had been over the source drain  
24 region, so you don't want a piece of silicon  
25 nitride covering the region where you are going to

1 form the resource drain and in that process you  
2 complete the formation of the side wall film.

3 Q Why is the material 26 removed during  
4 the second stage etch?

5 A 26 is being removed that substantially  
6 is the same rate as the etch stopper film, so it  
7 serves kind of as a sacrificial mask for defining  
8 the edge of the etch.

9 Q Look at Nakamura Column 13, Line 58, it  
10 says there, "On the other hand the interlayer  
11 insulation film 26 is etched by a film thickness  
12 substantially equal to a film thickness of the  
13 etching stopper film 24 and the interlayer  
14 insulation film 26 has a height substantially  
15 equal to a height of the insulation film 20  
16 exposed on the surface.

17 "Thus contact host 34 and 36 can be  
18 opened with the surface maintained plain."

19 Do you see that?

20 A Yes.

21 Q Does that help explain why in the  
22 Nakamura third Embodiment the interlayer  
23 insulation film is etched during the second stage  
24 etch?

25 A Yes, because it is desirable to have as

1 much a planar surface as is possible for  
2 lithography purposes s.

3 Q They wanted to have the height of the  
4 interlayer insulation film 26 be substantially  
5 equal to the height of the gate, correct?

6 A It is a desirable benefit if you can do  
7 it.

8 Q If Nakamura Embodiment 3 did not remove  
9 the mask --

10 A The photoresist mask?

11 Q Yes, and continued with the second stage  
12 etch, would it have been able to achieve the goals  
13 that are described in Column 13, Line 57, through  
14 64?

15 MR. MUKERJI: Objection to form and  
16 scope.

17 THE WITNESS: The etch stopper film 24  
18 is pretty thin. It shouldn't take a very  
19 long etch to clear that over the diffusion  
20 region, over the source drain region.

21 I don't really know the answer whether  
22 the planarity can be achieved in the same way  
23 because I don't know where the relative etch  
24 rates will be and so on.

25 That planarity is a nice benefit, if you

1           can get it, but it is not essential and  
2           particular, it is not essential for  
3           considering the extent to which Nakamura  
4           meets the claim limitations in the '244  
5           patent.

6       BY MR. CHEN:

7           Q       But achieving that planarity is one of  
8           the goals stated for Nakamura Embodiment 3,  
9           correct?

10          A       Yes, the way Nakamura Embodiment 3 does  
11          it.

12          Q       If the resist was in place when you  
13          performed the second stage of the etch, then the  
14          interlayer insulation film 26 would not be etched,  
15          correct?

16          A       Correct.

17                   MR. MUKERJI:  Objection to form and  
18          scope.

19       BY MR. CHEN:

20          Q       By removing the resist mask, the  
21          portions of the interlayer insulation film that  
22          were previously masked are then subsequently  
23          etched during the second stage each, correct?

24          A       Correct.

25          (Whereupon, Exhibit Number 11 is marked for

1 Identification.)

2 BY MR. CHEN:

3 Q I have asked the court reporter to mark  
4 as Exhibit No. 11, a document with the title  
5 "Introduction to NMOS and CMOS VLSI System designs  
6 by M.R. Mukherjee, and I am hoping that I have  
7 pronounced that correctly?

8 MR. MUKERJI: It is pretty good.

9 MR. CHEN: Thanks.

10 BY MR. CHEN:

11 Q This is another one of the references  
12 that you relied on to support your declaration on  
13 the '244 patent, correct?

14 A Yes, I think that is right.

15 Q I want to turn your attention to page 19  
16 of Exhibit 11. If you need to refer to other  
17 portions of the exhibit, just let me know what you  
18 are looking at.

19 If you also need to refer to your  
20 declaration, I believe the Mukherjee reference  
21 discussed is paragraphs C1 through C3.

22 A Yes.

23 Q I would like to walk through to what is  
24 being described in the paragraph of page 19 of  
25 Exhibit 11 and understand what is happening at



1 each of these different stages beginning at the  
2 upper left-hand corner with the image marked A.

3 A Yes.

4 Q What is happening at that stage?

5 A There has been presumably a thermal  
6 oxide, it only says oxide, if deposited or grown,  
7 if it is thermal oxide, it is grown on an  
8 antistructure and that has been covered by silicon  
9 nitride presumably by thermal CVD process.

10 Q What is happening at the next stage in  
11 the image marked B?

12 A I haven't looked at this in months, but  
13 it looks as if the silicon nitride has been  
14 patterned.

15 Q What is the meaning of the label "active  
16 areas"?

17 A I don't know. I will have to re-read  
18 this to know what we are talking about here. Do  
19 you want me to take the time to re-read it?

20 Q It's a pretty long reference.

21 A Yes, it is.

22 Q The reason why I am referring you to  
23 this particular page is because you actually cite  
24 to it. Maybe not.

25 A I do? I don't know why I would do that

1     except --

2           Q     I am sorry. I looked at the 4.3 at the  
3     top and I thought you were referencing this  
4     portion.

5           A     Some of these combinations that you see  
6     in my declaration, they are only to substantiate  
7     what everyone of ordinary skill would already  
8     know.

9                     I am advised that for patent purposes  
10    like this you really have to have a reference even  
11    though everyone knows that is the case.

12          A     At the end of paragraph C1, I say,  
13    "However, it would have been obvious to a person  
14    of ordinary skill in the art to form a well in  
15    Substrate 10 of Nakamura."

16                    Anybody who is doing any of these  
17    technologies is doing something related to CMOS  
18    and CMOS processes have been known for decades and  
19    for the purposes of innovation in comparing  
20    Nakamura to '244 to whatever is involved I think  
21    these are not really important.

22          Q     Just again looking at Fig. 4.3.

23          A     4.4?

24          Q     Page 7 of Nakamura, this is the figure  
25    that you are --

1 A I'm sorry? In Nakamura?

2 Q Sorry. Mukherjee, Exhibit 11. This, I  
3 believe, is the figure you are referencing in your  
4 declaration?

5 A 4.3D.

6 Q Yes, I hope that is right. I would like  
7 to understand what is happening here in this  
8 figure. In the portion of the figure at the upper  
9 left that is labeled A.

10 A Yes.

11 Q There's a substrate, do you see that,  
12 p-substrate?

13 A Yes.

14 Q On top of the p-substrate is an oxide?

15 A Yes.

16 Q Is that oxide the gate oxide?

17 A I don't think that is the point. The  
18 point of my referencing this and from the little  
19 that is depicted here it's just trying to prove  
20 the point there is a photoresist sequence using  
21 optical lithography and leading to patterning  
22 capability that involves etching that can allow  
23 you to take a continuous fill like oxide and break  
24 it up into islands whose shape you defined in the  
25 original optical mask. This is just straight

1 optical lithography.

2 Q I thought you were using this to  
3 demonstrate the formation of lightly doped wells.

4 A It's the first step in doing that  
5 subsequently so what I say here is you can form  
6 islands of base materials such as silicon dioxide  
7 which turn out then to be masks for implantation,  
8 or for the fusion, so subsequently the diffusion  
9 process using ion implantation techniques and then  
10 performed with dry ions and create p-well in an  
11 antistructure.

12 In "D" here, I could take that sample,  
13 go to an ion implantar, implant antidopants or put  
14 that surface in contact with some other source of  
15 antidopants and anneal the result and I would have  
16 p-wells underneath the opening.

17 Q So the oxide there is really just being  
18 used as a mask?

19 A The oxide, I am just going from the  
20 demonstration in Fig. 4.3 that you could make a  
21 patterned island structure, right? And let's see,  
22 page -- I don't understand. The pages are on the  
23 upper right?

24 Q Yes, there are two different page  
25 numbering schemes.

1           A     Yes, it's kind of confusing. So thus  
2 Mukherjee describes MLS certification technique in  
3 which a well is formed between the steps of  
4 forming islands which correspond to isolation,  
5 regions, and the step of forming a protective  
6 oxide layer which is understood in the art  
7 corresponds to dielectric layer.

8                     The whole point here as stated in C3 is  
9 one of ordinary skill would recognize that the way  
10 it is describing Mukherjee to make MLS devices  
11 could be used to detail the steps for MLS  
12 fabrication that are kind of left out and not  
13 described in detail in Nakamura.

14           Q     Right, so are the oxide islands the  
15 isolation regions, is that what Mukherjee is  
16 saying?

17           A     I have to re-read what he says. This  
18 Fig. 4.3. in the text of Mukherjee is speaking to  
19 the general process of lithography.

20                     From that one can control where  
21 implantation goes. I would say this is pretty  
22 general, but in Nakamura there are Regions 22 in  
23 Figure 5C, and 6A and 6B, for example, which could  
24 be formed by ion implantation and that can be done  
25 before the gate electrode is formed.

1                   That is one of the things that is needed  
2                   to realize the structure. Like it is very well  
3                   known.

4           Q       I'm trying to understand what you're  
5                   saying about the Mukherjee reference specifically.  
6                   Is it your opinion that the oxide islands shown in  
7                   Fig. 4.3D are equivalent to isolation regions?

8           A       Sorry 4.3?

9                   MR. MUKERJI: Objection to the form.

10                  THE WITNESS: Would you repeat the  
11                   question.

12           BY MR. CHEN:

13           Q       Is it your opinion that the oxide  
14                   islands shown in Fig 4.3D correspond to isolation  
15                   regions?

16           A       They could be the definition of where  
17                   the isolation -- they could be isolation regions  
18                   and they also define where the active regions will  
19                   be formed by some combination of either diffusion  
20                   or ion implantation doping to form wells or to  
21                   form source drain regions.

22           Q       Are isolation regions typically very  
23                   thin?

24           A       You mean the oxide isolation regions?

25           Q       Yes.

1           A       What does "very thin" mean? Compared to  
2 what? Compared to wells or compared to the  
3 structures that we are talking about in the  
4 patents at hand?

5           Q       If you turn to page 120, the previous  
6 page of the reference.

7           A       Yes.

8           Q       In paragraph 4.2.2, it talks about  
9 oxidation.

10          A       Yes.

11          Q       Then it talks about growing a thin layer  
12 of protective silicon dioxide on the silicon  
13 oxide.

14          A       Where does say that?

15          Q       Paragraph 4.2.2.

16          A       It doesn't make sense to me. You grow  
17 silicon dioxide. That is the form that silicon  
18 creates when it is oxidized in oxygen or in water.  
19 Wet oxidation, dry oxidation.

20                 I don't know why he says, "to grow a  
21 thin layer of protected silicon dioxide on the  
22 silicon oxide." That means grow thicker, right,  
23 so this thermal oxidation step, if it is dry, the  
24 growth rate is fairly small, so you slowly grow  
25 linearly in time thicker and thicker oxide.

1                   If you keep going it will eventually  
2                   slow down the growth rate mechanism and what that  
3                   happens to switch from what is called linear to  
4                   parabolic growth is well understood.

5                   You can accelerate those growth rates if  
6                   you add some water to the environment, but this is  
7                   the "Classic Homer" problem you give to students,  
8                   you have got this thickness of oxide, here are the  
9                   oxidation conditions, how long does it take to  
10                  increase the thickness by a certain amount?

11                  But I don't know why it says "grow a  
12                  thin layer of protective silicon dioxide on the  
13                  silicon oxide." That doesn't grow on. It grows  
14                  at the interface.

15                  So I don't understand this sentence.  
16                  Sorry.

17                  The reference was chosen because it is a  
18                  very general reference for all of the things, not  
19                  all, but for some of the things that Nakamura left  
20                  a little bit vague, but everybody in this field  
21                  knows.

22                  Q       In your declaration in paragraph C2 at  
23                  the back end of that paragraph, in the last  
24                  sentence you say, "Thus, Mukherjee describes a MOS  
25                  fabrication technique in which a well is formed



1 between the steps of forming islands which  
2 correspond to isolation regions and the step of  
3 forming a protective oxide layer which as is  
4 understood in the art corresponds a dielectric  
5 layer."

6 A Yes.

7 Q Where is the description of forming the  
8 protective oxide layer?

9 A My statement here is that an ion  
10 implantation of diffusion step is used to form a  
11 well after island regions like the LOCOS regions  
12 that we talked about, LOCOS I think is explained  
13 to you, right? Remember, the patterning can be  
14 done over and over again.

15 I can use the technique that is outlined  
16 in Fig. 4.3, as just a general description of  
17 lithography to produce an island pattern as you  
18 see in D and then to use that as an implant mask  
19 to deposit to inject dopants to make a well.

20 I can do that after --

21 Let's see, after or before?

22 I can do LOCOS first, then form the  
23 well, using the LOCOS even as an ion implantation  
24 process, and then clean the silicon surface by  
25 known chemical techniques, HF, for example, and

1 then I can grow a thermal oxide.

2 Q Looking on page 122 of the reference in  
3 the paragraph 4.2.4 in the diffusion?

4 A Yes.

5 Q The second to last sentence of that  
6 paragraph, it says, "It is possible to grow an  
7 oxide layer right after the drive-in process  
8 thereby providing a thin protective oxide layer."

9 A Yes.

10 Q Is it your opinion that that thin  
11 protective oxide layer corresponds to the gate  
12 oxide?

13 A It could. It need not be as described  
14 here.

15 Q So it doesn't specifically say that  
16 that's the gate oxide, correct?

17 A No. You put layers down. You pattern  
18 them, you do something, you remove the layers.  
19 Often, even if they are oxide or nitride, they are  
20 sacrificial, they are there for a purpose of  
21 modifying the substrate as in making wells and  
22 making the implant more diffusion regions.

23 Q Similarly, with respect to the oxide  
24 islands that are shown in Fig. 4.3D, Mukherjee  
25 doesn't specifically say that those oxide islands

1 are isolation regions, correct?

2 A Clearly they could be. I mean this is  
3 showing general lithography. This is teaching  
4 lithography 101.

5 They could be isolation regions. They  
6 could be silicon nitride pads so that you can then  
7 oxidize between the silicon nitride pads to form  
8 those LOCOS structures that you saw in some of  
9 the -- yes, here, for example, in 5A, Number 12,  
10 that is a LOCOS isolation region typically formed  
11 by nitride patterned local oxidation.

12 Q Fig. 4.3 really is just focused on the  
13 patterning steps, correct? Yes. Fig. 4.3 is  
14 really just focused on the patterning steps,  
15 correct?

16 A 4.3 is what I would call introduction to  
17 lithography. How do you pattern islands where you  
18 want them? They can almost be removed? They can  
19 be used to pattern things in the substrate.

20 It enables many things. It enables  
21 LOCOS relevant, enables diffusion, or  
22 implantation, in patterns and so on.

23 Q But it doesn't teach the implantation  
24 steps, correct?

25 A Well, the other parts of this mention

1 the various to make n-wells and p-wells and the  
2 like. I think it is all here.

3 Q But not in the specific figure, correct?

4 A This figure is in an enabler of these  
5 other things.

6 MR. CHEN: I will move on to a different  
7 declaration.

8 MR. MUKERJI: Then I have a few  
9 questions on the '244, so if we could do  
10 that.

11 EXAMINATION BY MR. MUKERJI:

12 Q Professor Rubloff, you considered all  
13 the claims of '244 in doing the work in this case,  
14 correct?

15 A Yes.

16 Q That includes Claim 16 of the '244  
17 patent, right?

18 A Yes.

19 Q Would you look at the '244 patent please  
20 which I think is Exhibit 9, half way down is Claim  
21 16, there is a word that appears and it says  
22 "planarizing" do you see that?

23 A Yes.

24 Q Earlier today there was considerable  
25 discussion on planarization, do you recall that?

1 A Yes.

2 Q Just so I'm clear. Can you tell us  
3 whether or not you considered the issue of  
4 planarizing in connection with your study of  
5 Nakamura?

6 A Yes, I certainly did.

7 Q And you stand by the opinions that you  
8 have expressed in your declaration on that issue?

9 A Yes.

10 MR. MUKERJI: Thank you. Pass the  
11 witness.

12 (Whereupon, Respondent's Exhibit Number 12 was  
13 marked for Identification.)

14 EXAMINATION BY MR. CHEN:

15 Q I asked the court reporter to mark as  
16 Exhibit No. 12, your declaration that was  
17 submitted in connection with Samsung's IPR of the  
18 '893 patent. Is this your declaration? Is  
19 Exhibit 12 your declaration?

20 A I would have to look at this. The print  
21 is too big in that one. Yes.

22 Q And does this declaration contain any  
23 and all relevant opinions you have regarding  
24 issues related to Samsung's petition for review of  
25 the '893 patent?

1           A       Well, yes, related to my input to the  
2       petition process that they have done.

3           MR. MUKERJI: Counsel, before you ask  
4       your next question, for clarity of the  
5       record, there are two proceedings pending on  
6       the '893. This declaration is 466 or 467.

7           MR. CHEN: Thank you for clarifying that  
8       issue. I believe it is the same declaration  
9       that was submitted in both proceedings.

10          MR. MUKERJI: Can we stipulate then that  
11       this is declaration in both the '466 and the  
12       '467?

13          MR. CHEN: Yes.

14          MR. MUKERJI: Sorry for the  
15       interruption.

16          MR. CHEN: No problem.

17       BY MR. CHEN:

18          Q       Does this declaration contain any and  
19       all relevant opinions you have regarding issues  
20       related to Samsung's two petitions for review of  
21       the '893 patent?

22          MR. MUKERJI: Objection to form.

23          THE WITNESS: This represents my  
24       conclusions in addressing the questions I was  
25       asked to address whether prior art meets the

1 claim limitations in the '893 patent.

2 BY MR. CHEN:

3 Q Do you have any opinions regarding the  
4 issues relevant to Samsung's two petitions for  
5 review of the '893 patent that were not included  
6 in this declaration?

7 MR. MUKERJI: Objection to the form.

8 THE WITNESS: I haven't read those two  
9 petitions so I'm not qualified to answer  
10 that.

11 BY MR. CHEN:

12 Q Do you have any opinions regarding the  
13 validity of '893 patent that were not included in  
14 this declaration?

15 MR. MUKERJI: Objection to the form.

16 THE WITNESS: In the opinions that are  
17 --

18 BY MR. CHEN:

19 Q Regarding the validity of the '893  
20 patent?

21 MR. MUKERJI: Same objection.

22 THE WITNESS: Yes. I'm not a patent  
23 attorney, so what I looked at was whether  
24 what is taught in prior art references and in  
25 particular the ones I put in my declaration

1 map onto or cover the teaching of the '893  
2 patent. Validity is a legal question.

3 BY MR. CHEN:

4 Q So you did not provide an opinion as to  
5 whether the '893 patent is valid or invalid,  
6 correct?

7 A No, I did not provide. I have concerns  
8 about it because it is not enabling, but I don't  
9 think that is an issue here. It is not supposed  
10 to be an issue.

11 Q Do you have any opinions regarding the  
12 '893 patent or any prior art to the '893 patent  
13 that are not included in your declaration?

14 A I don't think so. This is a summary of  
15 what I believe.

16 Q Are you aware of any errors or omissions  
17 in your declaration?

18 A I don't think so.

19 (Whereupon, Respondent's Exhibit Number 13 was  
20 marled for Identification.)

21 BY MR. CHEN:

22 Q Dr. Rubloff, I have asked the court  
23 reporter to mark Exhibit 13, which is Patent No.  
24 6,030,893.

25 We will be referring to this exhibit as



1 the '893 patent for the rest of this deposition.

2 Have you read the '893 patent?

3 A Certainly.

4 Q When did you first read the '893 patent?

5 A Thank you. You asked me yesterday when  
6 I started working on these and it was humorous  
7 that I had it wrong so I went back and looked and  
8 it must have been in October 2014, ten months ago.

9 Q That was when you were first engaged in  
10 these matters?

11 A Yes, but then I think I was told that  
12 the '893, the '244, "These are the ones they want  
13 you to look at."

14 Q Turning to your declaration, which is  
15 Exhibit 12, if we can look at paragraph 19, it  
16 begins on page 12 of your declaration.

17 A Yes.

18 Q You stated here that you believe that  
19 the '893 patent is not enabled, correct?

20 A That is right.

21 Q Why do you think that the '893 patent is  
22 not enabled?

23 MR. MUKERJI: Objection, outside the  
24 scope. You can answer.

25 THE WITNESS: I can answer?

1 MR. MUKERJI: You can, yes.

2 THE WITNESS: I was actually quite  
3 surprised to find this. The '893 patent  
4 talks about a constant CVD process using  
5 tungsten hexafluoride.

6 To deposit, to use tungsten hexafluoride  
7 to deposit tungsten, you have to have a way  
8 to remove the fluorine.

9 If the fluorine is in the tungsten film  
10 it will not be a good film. You need a  
11 reducing agent to do that.

12 The conventional one, the most popular  
13 one is hydrogen. Hydrogen then bonds to the  
14 fluorine which makes HF, that is a volatile  
15 product that leaves the surface and then only  
16 the tungsten atom is left behind to deposit.  
17 That is the basic idea.

18 But there is no mention of hydrogen as a  
19 reducing agent in the CVD process.

20 There are two or at least two other  
21 reducing agents which can be lead to tungsten  
22 deposition. Well, actually more than two.

23 An example is Silane,  $\text{SiH}_4$ , and that can  
24 be used. It makes a much faster growth rate.  
25 So a  $\text{WF}_6$ , plus Silane, will produce tungsten

1 as a deposited film, and SiF<sub>4</sub> and HF that  
2 leaves the surface, and finally you can use  
3 silicon.

4 If you use the WF<sub>6</sub> and hydrogen it can  
5 react with the silicon substrate and produce  
6 silicon fluoride products that leave the  
7 surface but unfortunately etch and therefore  
8 rough on the silicon surface.

9 People have used all of these and there  
10 are different trade-offs between using them.  
11 But the effect is that if you have a CVD  
12 reactor and the only thing you put into it is  
13 WF<sub>6</sub> you will not get a tungsten film.

14 What is surprising was, and this is all  
15 very well known in this time frame, and the  
16 prior art references cite that, they talk  
17 about hydrogen reductor.

18 They talk about the silicon substrate  
19 doing the reducing and they talk about Silane  
20 as a reducing agent and they talk about it in  
21 the context of well understood chemical  
22 trends that relate gas ratios of the  
23 reductant to the WF<sub>6</sub>, temperature,  
24 dependencies of these and really lay out the  
25 state of the art which was there.

1 I say that this is not enabling  
2 primarily because it doesn't even tell you  
3 what molecules are being used.

4 BY MR. CHEN:

5 Q It is your opinion that a person of  
6 ordinary skill in the art would not be able to  
7 implement the teachings of the '893 patent without  
8 the specific mention of the reducing agents like  
9 hydrogen or Silane or silicon, correct?

10 A Yes, what would happen is that the  
11 person, or processor, the equipment engineer,  
12 whoever it is, goes through the tool and you tell  
13 them this is the tool and if they are supposed to  
14 hook up the gases they don't know what gas to put  
15 on the tool.

16 Q Without the specific instruction of what  
17 reducing agents to use a person of ordinary skill  
18 in the art wouldn't be able to implement the  
19 teachings of the '893 patent?

20 A If all they had was '893, no, they  
21 wouldn't know what to do, but the prior art would  
22 have told them not only what gases to use, but how  
23 the different process parameters work together to  
24 change conformalities, stress, growth rate, et  
25 cetera.

1 Q Looking at the '893, would a person of  
2 ordinary skill in the art have been able to modify  
3 the teachings of the '893 patent to implement  
4 those teachings?

5 MR. MUKERJI: Objection to the form.

6 THE WITNESS: I don't know what they do  
7 to figure out what the reactant is without  
8 looking at prior art literature.

9 MR. CHEN: Let me reask the question.

10 BY MR. CHEN:

11 Q Looking at the '893 patent, would a  
12 person of ordinary skill in the art have been able  
13 to modify the process described in the '893 patent  
14 to implement the teachings of the '893 patent?

15 A This hypothetical person has access to  
16 what information? The literature?

17 Q You would have access to whatever the  
18 hypothetical person of ordinary skill in the art  
19 that you define for the '893 patent has access to?

20 A I think a person of ordinary skill in  
21 the art will read this patent, and say, "I have to  
22 know how this process works so I know what gas  
23 bottles to hook up and so on," so they would be  
24 able to get that from prior art information, by  
25 locations, patents, and so on, some of the patents

1 I cited and some of the references, and then to  
2 actually implement the two-layered deposition and  
3 to know what process parameters to choose, they  
4 would look beyond the teachings of the '893 to,  
5 "How does the mechanism work? Why does  
6 temperature change something this way? What is  
7 the role of the gas flow ratio?" which is very  
8 critical here.

9 And that is not found in the '893 and it  
10 is important for actually knowing how to do the  
11 design of experiments to determine the process  
12 parameter point.

13 And it is available in the prior art  
14 literature. It was all known.

15 I happen to know it because I worked in  
16 this and I know other people who have worked in  
17 it, so I concentrated on it.

18 MR. CHEN: Let's take a quick break.

19 Ron has to catch a flight.

20 (Whereupon, a break in the proceedings commenced  
21 at 3:46 p.m. and on resuming at 4:02 p.m.)

22 (Whereupon, Respondent's Exhibit Number 14 was  
23 marked for Identification.)

24 BY MR. CHEN:

25 Q Dr. Rubloff, I have asked the court

1 reporter to mark as Exhibit 14, Patent No.  
2 5,843,840, which I believe we were referring to  
3 say Miyazaki Reference.

4 A Yes.

5 Q The Miyazaki Reference is one of the  
6 primary references that you discuss in your  
7 declaration which is Exhibit 12, correct?

8 A Yes.

9 Q I believe your discussion of the  
10 Miyazaki Reference begins on page 23 of your  
11 declaration paragraph A1?

12 A Yes.

13 Q Miyazaki describes six different  
14 Embodiments, correct?

15 A I guess they number that, but I don't  
16 remember.

17 Q I could refer to you the Miyazaki  
18 Reference, Column 5, Line 44, that is where it  
19 begins the description of the preferred  
20 embodiments and then it concludes at Column 9.

21 A Fifth, sixth. Yes.

22 Q Which embodiments in Miyazaki were you  
23 relying on to support the opinions provided in  
24 your declaration?

25 A I don't remember if I put that into my

1 declaration. I will have to look for that.

2 I am glad to look through them, but I  
3 think the distinguishing feature is that some of  
4 them are related to ion implantation, and some  
5 related to CVD tungsten.

6 Q Right.

7 A So changing process parameters from CVD  
8 tungsten as opposed to using ion implantation to  
9 change stress and so on.

10 Q One of the key features of the '893  
11 patent is the use, depositing two layers of CVD  
12 tungsten doing the deposition in two different  
13 chambers and then modifying the temperature  
14 between those depositions, correct?

15 A Yes.

16 Q Then we will walk through each of the  
17 embodiments and ask you whether this is one  
18 embodiment that you are relying on. I believe  
19 Embodiment 1 begins at Column 5, Line 43.

20 A Yes.

21 Q And then continues on to Column 6, Line  
22 37. I believe Embodiment 1 describes a process  
23 where only a single layer of CVD tungsten is  
24 deposited, correct?

25 A Yes.



1           Q     You are not relying on Embodiment 2 to  
2     support the opinions that are provided in your  
3     declaration, right?

4           A     Some of the independent claims in the  
5     '893 speak to two layers of tungsten under  
6     different conditions, so Embodiment 1 of what we  
7     are talking about here, Miyazaki, is not what I  
8     relied upon.

9           Q     Looking at Embodiment 2, that begins at  
10    Column 6, Line 38, and continues through Column 7,  
11    Line 24, the second embodiment of Miyazaki also  
12    deposits only a single layer of CVD tungsten and  
13    so you are not relying on Embodiment 2 to support  
14    your opinions in your declaration?

15          A     No, I don't think either one of those,  
16    although it may be that there are aspects of the  
17    tungsten CVD process described in there that may  
18    not be easily found in the ones that I did rely  
19    upon. I don't recall if there are any such  
20    examples.

21          Q     That's fine. If we come across that, or  
22    if it is, it is probably in your declaration?

23          A     Yes, I think so.

24          Q     The third Embodiment, which begins at  
25    Column 7, Line 26, continuing all the way through

1 Column 8, Line 14, the third Embodiment in  
2 Miyazaki does deposit two layers of CVD tungsten,  
3 correct?

4 A Yes.

5 Q As disclosed in Miyazaki, the  
6 temperature used for the deposition of the first  
7 layer of CVD tungsten in Embodiment 3 and the  
8 second layer of CVD tungsten in Embodiment 3 is  
9 the same, correct?

10 A Yes, that is right.

11 Q You are also not relying on Embodiment 3  
12 to support the opinions that you provided in your  
13 declaration, correct?

14 A I am relying on it in part because it is  
15 supportive of that. The Miyazaki provides the  
16 reductant species and it provides teaching as to  
17 how the process works.

18 It is important in trying to practice  
19 this kind of a technology to know what are the  
20 things that changed the conformality via a filling  
21 capability and one of the things changed is stress  
22 and Miyazaki teaches at least two very significant  
23 points.

24 One of them is temperature.

25 As you go up in temperature you tend to

1 get into a transport limited regime which has  
2 lower stress and better via trench filling  
3 capability, void free.

4 As you go down in temperature you enter  
5 a kinetically limited regime which is very good  
6 for void free filling but creates higher stress  
7 and Miyazaki teaches how this works.

8 This is a very fundamental point about  
9 these kinds of CVD processes. I have many  
10 lectures on this actually at this point.  
11 Temperature is one thing.

12 The other thing that is important is the  
13 ratio of the reductant in this case is hydrogen to  
14 tungsten hexafluoride, and so in reference in  
15 Embodiment 3, the two layers differ by that ratio.

16 If it turns out where if you have a  
17 higher ratio of hydrogen to tungsten hexafluoride  
18 then you tend to be weight limited by the tungsten  
19 hexafluoride arrival and that does not give good  
20 conformality, but hydrogen, if you go to a low  
21 ratio you are then weight limited by hydrogen and  
22 that is a nice strongly kinetic limitation which  
23 gives good conformality.

24 Q All the claims in the '893 patent  
25 require that the temperature of the second CVD

1 deposition is different from the temperature of  
2 the first CVD deposition, right?

3 A Yes, that is true.

4 Q And Miyazaki Embodiment 3 specifically  
5 teaches that the temperature between the two  
6 depositions is the same, correct?

7 A Yes, the sense in which I say, I relied  
8 upon is related to my concern about enablement.

9 But in the '893 patent there are  
10 numerous claim limitations that have to do with  
11 either time or flow rate of one, the only species  
12 mentioned, or thickness, and gas flow rate of the  
13 tungsten hexafluoride.

14 In order to understand how those are  
15 related to each other you have to understand two  
16 things.

17 One is the chemistry of the reaction at  
18 least to the level that the hydrogen to tungsten  
19 hexafluoride ratio is critical and changing that  
20 ratio can differentiate between the two  
21 characteristic films that the '893 is talking  
22 about.

23 Secondly, you have to understand what  
24 the role of texture is in transforming the  
25 situation from kinetically transport limited

1 domains which also is a way to differentiate these  
2 two.

3 In that sense, and I am sure we will  
4 come back to this, interpreting the way in which  
5 the Miyazaki or the Emesh teachings map onto the  
6 claims in '893, really depends on translating  
7 that.

8 Q We will come back to that, but my point  
9 is that you said that you do rely on aspects of  
10 Embodiment 3 to support your opinions in the  
11 declaration, correct?

12 A Certainly to support my contention that  
13 '893 is not enabling.

14 Q How about to support your contention  
15 that Miyazaki teaches all the limitations of '893  
16 claims?

17 A This is really difficult because of  
18 enablement. I talk to enablement because of the  
19 processed chemistry. There is another enablement  
20 issue buried in this problem so you have to  
21 understand how deposition works.

22 The thickness you get is generally  
23 proportional to the time and the impingement rate  
24 of the molecule on the surface, the impingement  
25 rate on the molecules on the surface depends on

1 the pressure, the higher pressure, higher  
2 impingement rate.

3 Time is nothing very special in  
4 isolation and that's what the claims in the '893,  
5 some of them, are directed to.

6 There is another factor here which is  
7 the pressure of the hydrogen and the tungsten  
8 hexafluoride that will be used in the process can  
9 be associated with different flow rates.

10 If I have a certain pressure and I  
11 change the flow rate, I can change the pumping  
12 speed of the equipment and still get the same  
13 pressure.

14 In that sense the gas flow rate is not a  
15 variable which tells very much, so that's the  
16 second sense in which I have the concern of  
17 enablement.

18 Q If we look at the fourth embodiment in  
19 Miyazaki, this begins at Column 8, Line 15, and  
20 continues down to Line 46.

21 A Yes.

22 Q The fourth embodiment of Miyazaki  
23 teaches that the two depositions are done with the  
24 same gas flow rate, but different temperatures,  
25 correct?

1           A     Yes.

2           Q     You do rely on Embodiment 4 to support  
3 your contention that Miyazaki alone or in  
4 combination with other references teaches all the  
5 limitations of the '893 patent, correct?

6           A     In a significant sense I will say yes to  
7 that, but as I tried to explain when we talk about  
8 thickness and processed time and flow rates those  
9 are not the determining factors for the process.

10                   In more or less any case one can move  
11 the process into the regime of those parameters  
12 here, and say, "It meets the claim conditions,"  
13 but it is a little bit phony because it is not  
14 enabling to tell us what is really happening.

15           Q     When you're saying it is not annealing  
16 to tell us what is really happening, are you now  
17 to the teachings of Miyazaki?

18           A     No, '893, it says 10 to 100 seconds, for  
19 example, well, there are plenty of Miyazaki and  
20 Emesh References that arrive at those numbers.

21                   We can arrive at them, but those numbers  
22 are not particularly unique given that I can  
23 change the deposition rate by changing the  
24 pressure by just changing the gas flow and the  
25 pumping speed.

1           Q     Would you consider the teachings  
2 Miyazaki enabling?

3           A     Yes.

4           Q     Do you think Miyazaki provides enough  
5 details so that a person of ordinary skill could  
6 implement whatever?

7           A     Absolutely and in fact what it really  
8 gives is an understanding of, if it said 10 to 100  
9 seconds, and my current process is at 150, I know  
10 which knobs to turn to get from 10 to 100, and if  
11 you want me to I can get to 350.

12          Q     Let's look at Miyazaki and Embodiment 5  
13 or the fifth embodiment that begins at Column 8,  
14 Line 47 and continues on to Column 9, Line 7.

15                 Miyazaki's fifth embodiment again  
16 teaches two separate CVD tungsten depositions,  
17 only this time both the flow rate and the  
18 temperature are varied between the two deposition  
19 steps, correct?

20          A     Yes.

21          Q     You are also relying on Miyazaki  
22 Embodiment 5 to support your conclusions or your  
23 opinions in your declaration that Miyazaki alone  
24 or in combination with other references teaches  
25 all the limitations of the claims of the '893



1 patent, correct?

2 A Yes.

3 Q Miyazaki Embodiments 3, 4, and 5 all  
4 teach specific CVD deposition parameters, correct?

5 A Yes, they give examples of parameters.

6 Q Those parameters include, for example,  
7 the temperature for the deposition and the gas  
8 flow rate for the deposition, correct?

9 A Right. Yes. Oh, sorry correct that.  
10 Gas flow rates for the two species and therefore  
11 the gas flow ratios.

12 Q Because of those teachings you also  
13 believe that a person of ordinary skill in the art  
14 looking at Embodiments 3, 4, and 5 of Miyazaki  
15 would be able to implement the teachings of  
16 Miyazaki, correct?

17 A Yes, and in fact, from those as well as  
18 from some of the other things which Miyazaki  
19 describes about how the stress balance will work  
20 that is in some of the figures and how the  
21 competition between transport and kinetic  
22 limitation plays out, those would also be helpful  
23 to one of ordinary skill.

24 Q Then looking at the sixth embodiment  
25 that begins at Column 9, Line 8, and continues

1 through Column 9, Line 51, or Column 9, Line 58,  
2 the fifth Embodiment doesn't specifically teach  
3 process parameters used for two CVD tungsten  
4 depositions, correct?

5 A No, that's right. It has taught already  
6 how you can change the chemical and mechanical  
7 properties of the film to change the stress and  
8 then it goes through the exercise, I think that is  
9 Fig. 13.

10 It goes through the exercise of asking,  
11 well, I have chosen process parameters for the two  
12 films that gives stresses of 5 of the 9 for the  
13 upper film and 10 of the 9 for the lower film, how  
14 will the stress vary as I have changed the  
15 relative thickness of those two films, that is  
16 what the sixth embodiment is teaching.

17 Q Embodiment 6 is focused on how to  
18 achieve a specific targeted stress level for your  
19 film by varying the thicknesses of the two  
20 different films, correct?

21 A Yes and the implication from that is  
22 that it gives you a road map for understanding how  
23 the resistance of the upper wire which is an  
24 interconnect wire will change because it changes  
25 with thickness and you have to trade off how

1 important that is as compared to the stress in  
2 your particular technology.

3 Q Embodiment 6 is agnostic about the  
4 specific process parameters that are used to form  
5 the two tungsten films, correct?

6 A That is right. It is a kind of  
7 demonstration example.

8 Q Did you rely on Embodiment 6 to support  
9 the opinions that you provided in your  
10 declaration?

11 A Yes, it supports the description of  
12 variables that is taught in Miyazaki.

13 Q When you say description of variables  
14 what are you referring to?

15 A Miyazaki tells you a number of times  
16 that if you change the hydrogen to tungsten ratio,  
17 between kinetic and transport regimes, and as you  
18 lower that ratio you will get a better filling and  
19 higher stress and as you increase that ratio you  
20 get lower stress and not as good a filling, things  
21 like that.

22 You are trying to say I am going to use  
23 two films of tungsten here whereon with Fig. 12,  
24 the one to operate, Fig. 12, the consequences are  
25 in Fig. 13, but Fig. 12 is perhaps even more

1 interesting.

2 Q Were you still answering?

3 A No, I am done.

4 Q Fig. 12 shows the overall stress of your  
5 tungsten film?

6 A Yes.

7 Q Based on the ratio of the stress level  
8 between the two tungsten films?

9 A The ratio of the thickness.

10 Q Sorry, the ratio of the thickness.

11 A Yes, you see film thickness ratio. It  
12 is a little strange the word composition, but on  
13 the left side you see the thickness of the high  
14 stress film on the lower level..

15 Oh, yes, yes.

16 I think this is a typo here actually. I  
17 remember knowing that earlier. Let me see. The  
18 high stress film which is the one on the lower  
19 level -- Yes, I know what is wrong. The axis is  
20 mislabeled.

21 The high stress, this is just a simple  
22 mathematical exercise. It presumes, as you see --

23 Yes, if you will look at Column 9, Line  
24 40, if you have the high stress as 10 over the 9,  
25 and the low stress is 5 over the 9, that means the

1 bottom one which is high stress should be 10, so  
2 on the right-hand side of this curve you see the  
3 stress is 10.

4 So that should be high stress film as  
5 comprising all of the thickness and on the left  
6 side where the stress is 5, it should be the  
7 low-stress film, the upper-layer film as  
8 comprising 100 percent of the thickness.

9 It is mislabeled. I guess I should have  
10 remembered to put that in somewhere.

11 Q The labeling of high-stress film and the  
12 low-stress film should be flipped?

13 A Yes, exactly.

14 Q Isn't the lower film, the lower-level  
15 layer, the one that fills the contact?

16 A Yes.

17 Q Isn't that the low-stress film?

18 A No, that is the high-stress film. You  
19 see the words, high-stress film, lower-level  
20 layer, low-stress film, upper-level layer.

21 I would offer to explain why. but I  
22 don't think you need my verbiage anymore.

23 Q You never know. I might ask. I think I  
24 was confusing stress and pressure.

25 So you deposit the lower level film at a

1 low pressure to achieve high-step ratio or good  
2 conductive hole filling, but you will result in a  
3 high-stress film?

4 A You get a high-stress film because you  
5 are depositing under conditions that are  
6 kinetically limited, that is the hydrogen to  
7 tungsten hexafluoride ratio.

8 Q Right.

9 A But it is not tied to the pressure in a  
10 direct sense.

11 Q Sorry, I said type of temperature lower?

12 A We usually think of stress and pressure.

13 Q Yes. Tied to temperature though.

14 A Yes.

15 Q Lower temperature leads to a  
16 higher-stress film. Higher temperature leads to a  
17 lower-stress film?

18 A Right.

19 Q Let's turn back to Embodiment 3. If we  
20 look at Column 7, Line 51, beginning at 51.

21 A Yes.

22 Q It talks about filling the contact hole  
23 with a diameter of 0.5 microns with a thickness of  
24 film at 0.2 microns or more and that the tungsten  
25 film has a film thickness not smaller than 40

1 percent of the diameter of contact hole.

2 If you deposited a layer of .2 microns  
3 into the .5 micron diameter hole, would the entire  
4 hole be filled?

5 MR. MUKERJI: Objection, outside the  
6 scope.

7 THE WITNESS: That would require me to  
8 speculate on details of profile evolution in  
9 this process and that is a tough one to  
10 answer. Note that it prescribes not smaller  
11 than 40 percent.

12 BY MR. CHEN:

13 Q Sure.

14 A And the way these processes work can get  
15 harder to predict as the remaining space closes.  
16 Sometimes they form a seam in the microstructure  
17 of the film, sometimes they don't. I think what  
18 you are getting at is the 50 percent is the right  
19 number.

20 But remember it is growing from the  
21 bottom as well, so exactly how that material goes  
22 away, I think this is not so clear how the void  
23 goes away, but I do not have complete explanation  
24 for that question.

25 (Whereupon, Respondent's Exhibit Number 15 was

1 marled for Identification.)

2 (Whereupon, Respondent's Exhibit Number 16 was  
3 marled for Identification.)

4 BY MR. CHEN:

5 Q I have asked the court reporter to mark  
6 as Exhibit 15, a document titled "Silicon  
7 Processing for the VLSI Era," the authors are  
8 Stanley Wolf and Richard Tauber.

9 I think we referred to this as the Wolf  
10 Reference and I believe that is how you referred  
11 to it in your declaration.

12 A Yes.

13 Q And I asked the court reporter to mark  
14 as Exhibit 16 a document titled "Volume 5,  
15 Introduction to Microelectronic Fabrication,"  
16 authored by Richard C. Jaeger.

17 I believe we referred to this as the  
18 Jaeger Reference as it is referenced in your  
19 declaration.

20 A Okay.

21 Q Taking a look at Exhibit 16, first.

22 A 16. Jaeger.

23 Q Yes, Jaeger. Look at page 5 of Jaeger,  
24 Fig. 7.3, it shows aluminum contacts, correct?

25 A Yes.



1 Q I just have a question about the  
2 formation of aluminum contacts. Is aluminum  
3 typically deposited using CVD or PVD?

4 A Usually PVD.

5 Q Why is that?

6 A Because it has been developed for many  
7 years. It has a sputtering process. I'm not sure  
8 what Aluminum CVD processes are available. There  
9 may be some. I haven't looked at that.

10 Q At least in your experience you haven't  
11 encountered Aluminum CVD processes?

12 A No. CVD processes would be wonderful if  
13 they were all available, but they are not so that  
14 is a limitation because it depends on what  
15 precursor molecules you can actually buy or at  
16 least make.

17 Q In general are CVD processes preferred  
18 over PVD processes?

19 A Well, preferred it depends on what  
20 metric you have for that. If you're dealing high  
21 aspect ratios in deposition you really typically  
22 like to have a CVD process because PVD processes  
23 can have high-aspect ratio trenches and  
24 increasingly that is what you need to do, but if  
25 you want to be able to do something less demanding

1 in that sense, keep the high rate and do it  
2 cheaply and PVD is the choice.

3 Q Turning now to Exhibit 15 which is the  
4 Wolf Reference. I believe you discussed this in  
5 paragraphs A-22 to A-31 of your declaration.

6 A Right.

7 Q You used the combination of Miyazaki and  
8 Wolf to arrive at the particular timing of the  
9 depositions, correct?

10 A Yes, to see if the teaching of Miyazaki  
11 with what is known in Wolf about the kinetics of  
12 the processes is consistent with some of the claim  
13 limitations in the '893, for example, the time  
14 required for a certain thickness.

15 Q If you look at paragraph A-29 of your  
16 declaration which is on page 40.

17 A Yes.

18 Q I think you did a few calculations and  
19 then you arrived at the conclusion that for a .35  
20 micron diameter hole you would deposit a tungsten  
21 layer of 1,400 angstroms or less, and at the  
22 temperature of 450 degrees it would take 80  
23 seconds to deposit that 14 angstrom layer of  
24 tungsten, correct?

25 A Yes.

1 Q But that is specific for a .35 micron  
2 hole, correct?

3 A Yes.

4 Q If few had a .5 micron hole, what layer  
5 of thickness of tungsten would you need to use?

6 A Let's see, .5 micron would be something  
7 like 2,000 to 2,500 angstroms.

8 Q How long would it take then to deposit  
9 that 2,000 to 2,500 angstrom thickness at 450  
10 degrees?

11 A I don't know if I gave that number, but  
12 it would be something greater than 100 seconds and  
13 the point I was trying to explain earlier is that  
14 that is a bit of a fictitious number because under  
15 exactly the same conditions, I can change the  
16 deposition rate by increasing the flow rates and  
17 thereby achieving a higher pressure which is not  
18 expressed at all in the teachings of the '893, and  
19 as I said, the higher the pressure the higher the  
20 impeachment rate, the higher the growth rate, so I  
21 will get down below the 100 seconds pretty  
22 straight forward and I think anyone of ordinary  
23 skill in the art would know how to do that.

24 Q But if you changed the other conditions  
25 like the temperature or the flow rates, it is

1 possible that those conditions would then be out  
2 of the range that is claimed in the '893 patent.  
3 correct?

4 A But remember, I have several knobs I can  
5 change and the temperature range is specified in  
6 '893, are about 50 degrees broad. That is a lot.

7 If you look at Fig. 16 on page 37, that  
8 I took from the reference we are talking about,  
9 this is the Wolf Reference you can see --

10 Take a look at any one of those parallel  
11 curves and recognize that the Y axis is the long  
12 plot, and you can see, if I go from 400 to 450, I  
13 change the deposition rate a lot, so temperature  
14 can accommodate many changes.

15 Q So lowering the temperature  
16 significantly reduces the deposition rate?

17 A Yes, and for the first level, the via  
18 filling -- I am sorry -- the trench filling part,  
19 that is the part which is kinectically limited, so  
20 that is the part that is most sensitive to  
21 temperature and that is why these curves are quite  
22 steep.

23 Q But if you lowered the temperature and  
24 you decreased the deposition rate, it would take  
25 even longer to deposit the same thickness of

1 tungsten, correct?

2 A Right, but I can always increase the  
3 temperature as well. It depends on where I start,  
4 where are we starting from, and in terms of  
5 staying within the range that is specified in  
6 '893.

7 Q I think the range of temperature that is  
8 specified for the '893 for the first tungsten  
9 layer is between 400 and 450 degrees C?

10 A Yes.

11 Q And the calculation that you provided in  
12 your declaration was for 450 degrees C?

13 A Yes.

14 Q If we were to reduce the temperature  
15 within the range provided in the '893 patent, the  
16 timing that you calculated in your declaration  
17 would only increase?

18 A That is true. The other variable is the  
19 pressure though, so if I wanted a higher rate than  
20 1050, as you see in that chart, the 1050 number  
21 comes from the highest pressure of 2 TOR, I know  
22 it is a little hard to read, but the one below it  
23 is 1 TOR, and if I were go to 4 TOR, I think I  
24 would get a big increase in rate again because is  
25 the well plot being shown.

1 I believe I could accommodate the half  
2 micron diameter with the width of a trench within  
3 the range of parameters consistent with the  
4 specification in '893.

5 Q 4 TOR is not plotted on the Fig. 16 from  
6 the Wolf Reference, correct?

7 A That is right.

8 Q They did not conduct any experiments at  
9 4 TOR in order to get data points for Fig. 16,  
10 correct?

11 A That is true, but I give two answers.  
12 There are many other references for tungsten CVD  
13 so probably somebody has done it and if nobody had  
14 done it, it would be a very simple exercise to  
15 just try it.

16 The CVD processes are done up to 10 or  
17 even 100 TOR. For example there are ozone POS  
18 processes which is plasma system CVD that I  
19 remember run to 100 TOR. So there is plenty of  
20 lending space available.

21 Q Would 100 TOR be considered a  
22 low-pressure process?

23 A Yes.

24 Q Where is the dividing line between low  
25 pressure and high pressure?

1           A       That's hard. Typically low pressure  
2 means you need a pump so there is atmospheric  
3 pressure CVD and then you don't need a pump and  
4 low pressure is going to be less than that, but  
5 requires a pump and all the equipment and baggage  
6 that that brings with it.

7                   In fairness most low pressure is of  
8 order 1 to 10 TOR or in the milli-TOR range.

9                   MR. CHEN: I will move on to Emesh which  
10 is part of a different IPR, so let's just  
11 take a quick break.

12 (Whereupon, a break in the proceedings commenced  
13 at 4:53 p.m. and on resuming at 5:09 p.m.)

14 (Whereupon, Respondent Exhibit Number 17 is marked  
15 for Identification.)

16 (Whereupon, Respondent Exhibit Number 18 is marked  
17 for Identification.)

18 BY MR. CHEN:

19           Q       Dr. Rubloff, I have asked the court  
20 reporter to mark as Exhibit 17, Patent No.  
21 5,407,698 which is the Emesh Reference.

22                   I have also asked the court reporter to  
23 mark Exhibit 18, a document entitled Integrated  
24 Tungsten Plug Fabrication Process," authored by a  
25 number of people, the first author being A. Mak

1 and we will refer to this as the Mak Reference.

2 Turning to Exhibit 17, the Emesh  
3 Reference, does Emesh disclose depositing two  
4 layers of tungsten in two different chambers?

5 A I think I had written about this in my  
6 declaration, so let me look for that.

7 Q I can direct you.

8 A I think I know the answer.

9 Q I was just going to direct you to page  
10 45 of your declaration which is where I think you  
11 start the discussion of Emesh.

12 A That doesn't answer the question. I  
13 know that Emesh doesn't talk explicitly about  
14 describing the use of two chambers, but it does  
15 say that it could be done.

16 Let me find where that is.

17 B-27 of my declaration, page 62,  
18 "Although Emesh doesn't expressly disclose the  
19 deposition process in two separate chambers Mak  
20 discloses an integrated system.

21 No, that is not the place I am looking  
22 for. Maybe I did not put it there. I don't  
23 recall if I am confusing Miyazaki with Emesh.

24 At any rate, I wrote it in my  
25 declaration but it doesn't explicitly disclose



1     that, so why don't we go from there.

2           Q     I think it is possible that maybe  
3     there's some confusion there.

4           A     One of those references says, though we  
5     did it in one chamber. It could be done in two  
6     separate chambers.

7                     I am used to looking at these that I  
8     have annotated and I can find things for you.

9           Q     Emesh doesn't teach explicitly the use  
10    of two chambers and that's why you combined Emesh  
11    with the Mak Reference, correct?

12          A     Yes.

13          Q     Because you are of the opinion that Mak  
14    discloses a multichamber deposition system,  
15    correct?

16          A     Yes.

17          Q     Is the reason that Emesh doesn't teach  
18    two chamber deposition because Emesh teaches  
19    specifically the use of the Varian --

20          A     5101.

21          Q     Thank you, the Varian 5101?

22          A     I got some of it right. I will not take  
23    time to look for which one of these references  
24    mentions it, it's pretty brief, but I suspect that  
25    Emesh doesn't mention it because they had a 5101

1 to work with.

2 The assignee is Northern Telecom, this  
3 is an R&D activity, it is not a high-volume  
4 manufacturing environment, so they probably  
5 wouldn't have had access to the resources to  
6 purchase and use a multichamber cluster tool.

7 The issue is about whether this scheme  
8 or using two different deposition conditions for  
9 the filling and for the interconnect above it  
10 could be sorted out in a single tool. It is not  
11 ideal for high volume manufacturing, but to do the  
12 R&D it is okay.

13 Q Varian 5101 is a single chamber CVD  
14 reactor system, correct?

15 A That is right.

16 Q Turning to Exhibit 18 which is the Mak  
17 Reference.

18 A Yes.

19 Q What is the specific process taught by  
20 the Mak Reference?

21 A It describes the use of the equipment  
22 for CVD tungsten and tungsten etchback.

23 On page 2, "Blanket tungsten depositions  
24 performed in the cold wall single wafer CVD  
25 chamber," and then later it talks in the next

1 paragraph about the etchback process which is the  
2 planarized deposition of tungsten.

3 Q Subsequent to that deposition of  
4 tungsten and then the etchback, the next layer  
5 that is deposited in Mak is an aluminum layer,  
6 correct?

7 A Yes. I think that is right. Tungsten  
8 deposition. Tungsten etchback.

9 Q If you look at the first page under  
10 "Introduction," I think it talks about forming  
11 tungsten plugs?

12 A Yes.

13 Q And then having aluminum deposit  
14 subsequently.

15 A Yes, okay.

16 Q So Mak teaches the deposition of a  
17 single layer of tungsten, correct?

18 A Yes.

19 Q It does not teach the deposition of two  
20 layers of tungsten, correct?

21 A Not explicitly, but by implication. If  
22 one of these chambers, the CVD chamber can do  
23 tungsten CVD, then the one that looks exactly like  
24 it could also do that and have different process  
25 deposition conditions.

1           Q     But the specific process that is taught  
2 by Mak teaches the deposition of a single layer of  
3 tungsten to form plugs followed by an etchback,  
4 which is then followed by a deposition of an  
5 aluminum layer to form the interconnects, correct?

6           A     Yes, that was, I think, then motivated  
7 by the era when all the lateral interconnects were  
8 aluminum.

9           Q     Because Mak only teaches the deposition  
10 of a single tungsten layer, Mak does not teach two  
11 CVD tungsten depositions performed in two  
12 different chambers, correct?

13          A     It teaches it by implication, I think.  
14 Note that this is a publication from applied  
15 materials which is our equipment company and the  
16 discussion here, while it mentions some of the  
17 process conditions, it doesn't mention very many.

18                It talks about rates and it talks about  
19 equipment-related issues because this is really  
20 explaining how the P-5000 is being used for  
21 multistep deposition in etching in a  
22 single-cluster tool.

23                So one of ordinary skill in the art  
24 would have recognized several things. One is, in  
25 the time frame of the '893 patent, which is 96, or

1 so, the whole world knew about cluster tools, the  
2 P-5000 and everyone was moving toward the adoption  
3 of this cluster manufacturing techniques.

4 The demonstration that one of the CVD  
5 chambers can do tungsten would make it obvious to  
6 any of those skilled in the art that they could  
7 use two chambers for tungsten, and I can tell you  
8 that applied materials was at Semicon to sell you  
9 as many of these as you wanted to do whichever  
10 they qualified as processes.

11 If the tungsten CVD process and tungsten  
12 etchback process were qualified at that time, it  
13 would have been very obvious to adopt this to do  
14 precisely what is taught in the Emesh reference,  
15 the Miyazaki Reference, and the '893 Reference.

16 Q Looking at the Mak Reference at the  
17 bottom of page one, then continuing on to page 2,  
18 under the heading "Experimental"?

19 A Yes.

20 Q There it's kind of describing the use of  
21 the applied materials 5000, right?

22 A Yes.

23 Q Sorry, the AMAT P-5000?

24 A The last sentence starting on page 1, it  
25 says, "Since the throughput of the etchback

1 chamber is twice that of the deposition chamber,  
2 two deposition chambers CVD, and Watten etchback  
3 chamber are typically used." What does that  
4 sentence mean? That actually is a very  
5 significant sentence in explaining why these tools  
6 have been so successful.

7 If you look at the Cassette IO at the  
8 bottom of Fig. 1, there is a load station, you put  
9 the initial wafers there, a robot takes them into  
10 the cluster tool, puts them in one chamber,  
11 processes one, takes it out of there and puts in  
12 another chamber, and the process is run, so when  
13 you look at factory utilization and efficiency,  
14 you want to get wafers through these tools as far  
15 as possible. It has a huge effect on what is  
16 called cost of ownership.

17 What that means is, if I want to load  
18 balance my ability to get wafers through, I like  
19 the CVD process that is half the speed takes twice  
20 as long, they have two chambers in the etchback  
21 which is twice as fast, they want a chamber and  
22 what that means is that throughput through the  
23 tool is much better.

24 In the case of applied to the teaching  
25 of Emesh, Miyazaki and '893, what you would do is

1 you would use two CVD chambers for the slower  
2 process, the lower process because that would be  
3 slower because it is lower temperature and one  
4 chamber for the faster process if the two-to-one  
5 ratio is what you ended up arriving at for the  
6 filling step of a process and the interconnect  
7 step that follows.

8 That is assuming they have a factor of  
9 two difference in throughput.

10 Q What that sentence that we just read  
11 teaches is that you could increase the throughput  
12 of your process by running two parallel processes,  
13 each process using a different CVD chamber, but  
14 sharing the etchback chamber?

15 A Yes, if you need the etchback chamber.  
16 There are four stations here you could use for  
17 processes, right, so where it says, I think,  
18 expansion, you could make the expansion be in  
19 another CVD chamber, devote two of these to the  
20 slower of the two layers, one of them to the  
21 faster one and not use the etch back chamber, it  
22 just depends how you want to configure it, but it  
23 is a throughput issue.

24 Q But specifically for Mak because it only  
25 needs to deposit a single layer of CVD tungsten.

1 They use two separate CVD chambers each chamber  
2 for a different process, correct?

3 A Right, for a different material and this  
4 tells us something about an earlier discussion  
5 which is it's an aluminum CVD chamber.

6 You will recall we had the discussion,  
7 you asked me about whether aluminum is likely to  
8 be deposited by PVD or CVD.

9 Q Right.

10 A I had forgotten here is an example of  
11 aluminum CVD.

12 Q Where is this teaching aluminum?

13 A In the previous declaration.

14 Q No, no. I mean where does this teach  
15 aluminum CVD?

16 A Does it not? I guess I am making an  
17 assumption here, tungsten plugs, no, it doesn't  
18 say it explicitly here. I take it back.

19 Q Are there potential downsides of using  
20 two chambers for your tungsten CVD deposition as  
21 opposed to a single chamber?

22 A Yes, downsize to using two. I don't  
23 think significant ones unless you're in a cluster  
24 tool like this. Well, are you assuming it would  
25 be done in a cluster tool?



1           Q     Why don't we start with doing it in a  
2 cluster tool.

3           A     In a cluster tool, the only downside is  
4 the robot breaks and you cannot get it from one  
5 chamber to another.

6                     But for cleanliness control and  
7 throughput it is very efficient.

8                     That is much of the reason why people  
9 are using these.

10                    If you have two chambers running the  
11 lower level and the upper level in a clean room  
12 and you have to remove the wafer from the first  
13 one and take it to the second one, that requires  
14 time because you have to cool down, open the  
15 system, take the wafer out maybe through a load  
16 lock and then go through that again so there are  
17 delays there.

18                    And other than if you use a single  
19 chamber, time to change and stabilize the  
20 temperature are substantial.

21                    If you were worried about real  
22 manufacturing you would probably be quite worried  
23 about throughput and so you would probably look  
24 very closely at trying not to change the  
25 temperature, but rather change the flow rate

1 conditions for the two levels.

2 MR. CHEN: I don't have anymore  
3 questions.

4 MR. MUKERJI: I have no questions. I  
5 think we are done.

6  
7 (Whereupon, the deposition concluded at 5:25 p.m.  
8 with the witness to read and sign and Mr. Mukerji  
9 to make arrangements for the witness to read.)  
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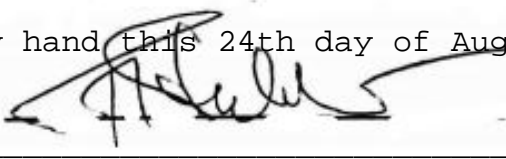
1  
2 UNITED STATES OF AMERICA )

3 ss:  
4 DISTRICT OF COLUMBIA )

5  
6 I, T. S. HUBBARD, JR., a Notary Public  
7 within and for the District of Columbia do hereby  
8 certify that the witness whose deposition is  
9 hereinbefore set forth was duly sworn and that the  
10 within transcript is a true record of the testimony  
11 given by such witness.

12  
13 I further certify that I am not related  
14 to any of the parties to this action by blood or  
15 marriage and that I am in no way interested in the  
16 outcome of this matter.

17  
18 IN WITNESS WHEREOF, I have hereunto set  
19 my hand this 24th day of August 2015.

20  
21   
22 Thomas S. Hubbard, Jr.  
23 Notary Public District of Columbia  
24 Commission Identification 237435  
25 Sworn in on June 12, 2006  
Commission Expires April 30, 2018

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