

1 UNITED STATES PATENT AND TRADEMARK OFFICE

2 BEFORE THE PATENT TRIAL AND APPEAL BOARD

3 Case IPR2015-00460 Patent 6,146,997

4 Case IPR2015-00459 Patent 6,150,244

5 -----X

6 SAMSUNG ELECTRONICS CO. LTD.,

7 SAMSUNG ELECTRONICS AMERICA, INC., Volume 1 of 2

8 SAMSUNG SEMICONDUCTOR INC., and

9 SAMSUNG AUSTIN SEMICONDUCTOR LLC

10 Petitioner,

11 vs

12 HOME SEMICONDUCTOR CORPORATION

13 Patent Owner.

14 -----X

15
16 VIDEOTAPED DEPOSITION OF GARY W. RUBLOFF, PH.D.

17
18 Washington, DC 20005

19 Wednesday, December 16, 2015

20
21
22 By: Denise D. Vickery, RMR, CRR Job No. J0254984

Wednesday, December 16, 2015

9:09 a.m.

VIDEOTAPED DEPOSITION OF GARY W. RUBLOFF, PH.D.,
held at the offices of:

FISH & RICHARDSON PC
1425 K Street NW, 11th Floor
Washington, DC 20005

Pursuant to notice, before Denise D. Vickery,
Registered Merit Reporter, Certified Realtime
Reporter, and Notary Public in and for the District
of Columbia.

A P P E A R A N C E S

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Also Present: Patrick Graham, Videographer

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(Exhibits attached to transcript.)

P R O C E E D I N G S

- - -

THE VIDEOGRAPHER: Here begins
disk 1 in the video deposition of Gary Rubloff taken
in the matter of Samsung Electronics Company
Limited, et al. v. Home Semiconductor Corporation,
before the Patent Trial and Appeal Board, Patent
Case Number IPR 2015-00460.

Today's date is December 16, 2015.
The time on the video monitor is 9:09. This
deposition is being held at 1425 K Street,
Northwest, Washington, DC 20005.

The court reporter is Denise
Vickery on behalf of Esquire. The video camera
operator is Patrick Graham on behalf of Esquire.

Will counsel please introduce
themselves and state whom they represent, beginning
with the party noticing the deposition.

MR. CHEN: Jerry Chen from
TechKnowledge Law Group for Home Semiconductor
Corporation.

MR. COLAIANNI: Joseph Colaianni

1 of Fish & Richardson on behalf of the Samsung
2 Petitioners.

3 MR. HSIEH: Andy Hsieh, Fish &
4 Richardson, on behalf of Samsung Petitioners.

5 THE VIDEOGRAPHER: Will the court
6 reporter please swear in the witness.

7 - - -

8 GARY W. RUBLOFF, PH.D.
9 called for examination, and, after having been duly
10 sworn, was examined and testified as follows:

11 CROSS-EXAMINATION

12 BY MR. CHEN:

13 Q. Good morning, Dr. Rubloff.

14 A. Good morning.

15 Q. Good to see you again.

16 A. (Laugh). Just before Christmas.

17 Q. Right. So as you know, I'm an attorney
18 with the law firm of TechKnowledge Law Group, and I
19 represent the Respondent Home Semiconductor
20 Corporation and the patent holder.

21 I'll be cross-examining you today
22 regarding your reply declaration submitted in

1 connection with the IPRs filed by the Samsung
2 entities against the Home patents.

3 I will ask you questions related to the
4 subject matter disclosed or discussed in those reply
5 declarations. You will need to answer my questions
6 truthfully and completely. The court reporter will
7 record my questions and your answers in writing.

8 Do you understand?

9 A. Yes.

10 Q. Okay. If your attorney objects, you
11 still must answer all my questions, unless your
12 attorney instructs you not to answer.

13 You understand?

14 A. Yes.

15 Q. Okay. If you do not hear or understand
16 my question, please ask me to repeat or clarify. If
17 you answer my questions, my assumption will be that
18 you understood the questions.

19 Do you understand?

20 A. Yes.

21 Q. Okay. And, of course, if you need a
22 break, please let me know and we'll take one.

1 A. I certainly will.

2 Q. Okay. Can you think of any reason that
3 might affect your ability to provide truthful and
4 complete answers to my questions today?

5 A. No, unless I don't know the answer.

6 Q. Do you have any questions before we
7 start?

8 A. No.

9 Q. Okay. Dr. Rubloff, could you and
10 please state and spell your full name for the
11 record.

12 A. Gary, G-a-r-y, Wayne, W-a-y-n-e,
13 Rubloff, R-u-b-l-o-f-f.

14 Q. Okay. Dr. Rubloff, you were previously
15 deposed in connection with the Samsung IPR case
16 number for IPR 2015-00460; correct?

17 A. I don't remember the number of it, but
18 there was a Samsung case, yes.

19 Q. Okay. And this was the IPR filed in
20 connection with the Home '997 patent; correct?

21 A. Yes.

22 Q. Okay. And in that prior deposition, I

1 asked you to let me know if you didn't understand my
2 questions; correct?

3 A. I think -- I think so.

4 Q. Okay. And I told you in that prior
5 deposition that if you did not understand my
6 questions, you could ask me to repeat or clarify;
7 correct?

8 A. I would assume so. I don't -- I don't
9 remember that --

10 Q. Okay.

11 A. -- precisely.

12 MR. CHEN: All right. So we'll
13 mark this as two transcripts for two days of
14 deposition. So we'll mark it Exhibit 1 and 2.

15 (Document marked, for
16 identification purposes, as Rubloff Exhibit No. 1.)

17 (Document marked, for
18 identification purposes, as Rubloff Exhibit No. 2.)

19 MR. COLAIANNI: Is this one
20 exhibit or two?

21 MR. CHEN: Two.

22 MR. COLAIANNI: Okay.

1 BY MR. CHEN:

2 Q. All right. Dr. Rubloff, I asked the
3 court reporter to mark as Exhibits 1 and 2 the
4 deposition transcripts from your prior deposition in
5 the IPRs filed by Samsung.

6 Exhibit 1 is the transcript from the
7 first day of your deposition and Exhibit 2 is a
8 transcript from the second day of your deposition.

9 You have those now in front of you;
10 correct?

11 A. Yeah.

12 Q. Okay. If you look at Exhibit 1, if you
13 look at page 7 of the transcript.

14 A. Question. The way this is laid out,
15 there are four pages per page. So when you say
16 "page 7," you mean this one?

17 Q. Right. I mean page 7 of the
18 transcript, which refers to --

19 A. Okay. I think I understand.

20 Q. -- the upper right-hand corner --

21 A. Right.

22 Q. -- of each small section as opposed to

1 the physical page.

2 A. Yes.

3 Q. Okay. If you look at page 7 of the
4 transcript.

5 A. Yes.

6 Q. You see there at line 14 --

7 A. Yes.

8 Q. -- I ask you:

9 "If you do not hear or understand my
10 questions, please ask me to repeat or clarify. If
11 you answer my questions, my assumptions will be that
12 you understood the questions. You understand?"

13 And you replied: "Yes."

14 Do you see that?

15 A. Yes.

16 Q. Okay. So does that refresh your memory
17 as to whether in your previous deposition I asked
18 you to let me know whether you didn't understand any
19 of my questions?

20 A. Yes. Sure.

21 Q. Okay.

22 A. I mean, I expected what you just did

1 you would have done last time. I just didn't
2 remember exactly.

3 Q. Right. And so I told you in that prior
4 deposition that if you did not understand my
5 questions, you could ask me to repeat or clarify;
6 correct?

7 A. Yes.

8 Q. Okay. And I told you that if you
9 answered my questions, my assumptions would be that
10 you understood my questions; correct?

11 A. Yes.

12 Q. And barring circumstances where you
13 asked me to repeat or clarify my -- the question,
14 you understood my questions in those -- that prior
15 deposition; correct?

16 A. I thought I did at the time.

17 Q. Okay. And you were truthful in that
18 prior deposition; correct?

19 A. Of course.

20 Q. And you gave complete answers to my
21 questions; correct?

22 A. As complete as I could.

1 Q. And you stand by the answers you
2 provided in that prior deposition; correct?

3 A. There was a clarification in my
4 reply -- is it called reply declaration? -- about at
5 least one of the questions and my answer to it, and
6 I'm sure you know which one that is.

7 And I stand by what is in my reply
8 declaration, which was an explanation that I was not
9 catching the significance of the legal terms you
10 used because I think, on retrospect, I realized that
11 from the transcript and from discussions later that
12 went into my reply declaration that your question
13 really meant, as I understand it now, the nature of
14 the claims language.

15 And when I gave a comment at that
16 point, I was thinking about a specification, a
17 preferred embodiment of the specification.

18 I think it's important to understand
19 that I am not an attorney. I'm a practicing
20 scientist every day and so it's easy for me to --
21 well, hopefully not easy, but it's possible for me
22 to miss the subtlety of the question with regard to

1 issues which I would call legal in nature. You're
2 talking about the claims, not a specification, and I
3 think you asked me to summarize what the situation
4 was. And I gave the example, as explained in my
5 declaration, of -- of what -- what was in this
6 preferred specification. This is how a scientist
7 thinks.

8 Q. Dr. Rubloff, do you stand by the
9 answers provided in your prior deposition?

10 A. Well, I've indicated clarification in
11 my declaration, my reply declaration. So that
12 qualifies and, in some cases, may change the -- the
13 tone of what's in the dec -- in the deposition. So
14 consider my declaration -- my reply declaration to
15 be an amendment to the deposition testimony.

16 Q. So is it correct then that you do not
17 stand by the answers provided in your prior dec --
18 deposition?

19 A. I think that's the wrong way to word
20 it. I think the way to word it is that I had a
21 declaration. It's before the court. I had a
22 deposition. I had a reply declaration. And taken

1 together, that expresses what I -- what my opinion
2 is.

3 Q. My question is very simple.

4 Do you or do you not stand by the
5 answers that you provided in your prior deposition?

6 A. As amended by the declaration.

7 Q. Are you retracting the answers that you
8 provided in your prior deposition?

9 A. I don't want to address the question in
10 generality.

11 I cited one example that I recall from
12 my reply declaration, and I don't want to make grand
13 statements about every single word that's in my
14 prior deposition or in a declaration.

15 If there is some that -- if -- I stand
16 by the fact that my two declarations and my
17 deposition constitute testimony up to this point.

18 Q. As we covered a few minutes ago, in the
19 previous deposition you were asked to provide
20 truthful and complete answers to my questions;
21 correct?

22 A. Of course.

1 Q. And you stated that you provided
2 truthful and complete answers to my questions;
3 correct?

4 A. Certainly.

5 Q. And you also stated that you understood
6 my questions; correct?

7 A. I stated that. That's correct, but it
8 is only a reality of human nature and it's the case
9 for a scientist because these issues are complex,
10 and it's particularly the case for a scientist who's
11 dealing with a legal matter to be able to discern
12 very carefully what the legal specifications of that
13 question are.

14 MR. CHEN: This is Exhibit 3.

15 (Document marked, for
16 identification purposes, as Rubloff Exhibit No. 3.)

17 MR. COLAIANNI: Thank you.

18 BY MR. CHEN:

19 Q. All right. Dr. Rubloff, I've asked the
20 court reporter to mark as Exhibit No. 3 your reply
21 declaration submitted in connection with the Samsung
22 IPR 460, which is the IPR filed in connection --

1 filed regarding the Home '997 patent.

2 You have that now before you?

3 A. Yes.

4 Q. Did you draft this declaration?

5 A. Yes.

6 Q. Are you aware of any errors in this
7 declaration?

8 A. Not at this point.

9 Q. So there are no corrections you would
10 like to make to this declaration?

11 A. I have no corrections at this time.

12 Q. Okay. How did you arrive at the
13 opinions included in this declaration?

14 A. Well, I looked at the -- the
15 declaration of Ron Maltiel and the patent owner
16 response, and looked at what some of the remaining
17 issues were that were raised by Maltiel, and had
18 discussions with the attorneys about which of the
19 issues are of significant enough to put into this
20 reply because I didn't want to document -- I
21 certainly didn't want to write a document of a
22 hundred or 200 pages, and -- and picked the issues

1 and constructed the arguments and wrote them.

2 Q. Did you arrive at the conclusions in
3 this declaration based on your own analysis?

4 A. Of course.

5 Q. Do some of these conclusions in this
6 declaration relate to legal issues?

7 MR. COLAIANNI: Objection to form.

8 THE WITNESS: Well, I'm not sure
9 what you mean by "legal issues."

10 BY MR. CHEN:

11 Q. For example, interpretation of
12 terminology that might have legal significance.

13 A. I'm not a lawyer.

14 MR. COLAIANNI: I'm going to
15 object.

16 THE WITNESS: I'm sorry.

17 MR. COLAIANNI: No, that's okay.

18 THE WITNESS: I'm not a lawyer. I
19 don't know what -- I wouldn't know how to explain
20 what legal significance has. I know there's
21 discussions of things in the claims and in the
22 specifications.

1 BY MR. CHEN:

2 Q. Okay. Did you discuss, for example,
3 the interpretation of claim terms?

4 A. I don't remember -- for this
5 declaration? Let me look and see if there's a
6 specific discussion of claim terms. Of course,
7 things rely on what -- on what the terms in the
8 claim mean. So I guess that's implicit.

9 (Reviewing document).

10 I don't find anything here that is a
11 discussion or debate over the meaning of a claim
12 term, but there certainly are claim terms used in
13 this.

14 Does that answer your question?

15 Q. Sure.

16 So there is content or opinions in your
17 declaration that relate to claim terms?

18 A. Yeah, I think that's -- that's probably
19 always the case.

20 Q. Okay. Were you able to understand
21 those claim terms as they were used in your
22 declaration?

1 MR. COLAIANNI: Objection to form.

2 THE WITNESS: I think so.

3 BY MR. CHEN:

4 Q. Okay.

5 A. Generally speaking.

6 Q. Previously when I asked you whether you
7 stood by the answers provided in your prior
8 deposition, you stated that there were instances
9 where you could not catch the significance of the
10 legal terms that were used.

11 Do you recall that?

12 A. Yes.

13 Q. And then you also stated that because
14 you are not an attorney and that you're a practicing
15 scientist, it's very easy for you to miss the
16 subtlety of a question with regard to issues that
17 you call legal in nature.

18 Do you recall that?

19 A. I said that.

20 Q. Okay.

21 A. That was a fairly strong statement.
22 That's probably stronger than it needed to be.

1 I mean, usually I don't miss these
2 things, but there are -- there are situations where
3 a question may be asked. There may be a long
4 discussion as -- as in the case I referred to where
5 basically I then get a question that asks for a very
6 simple answer, and I give an overview that is not
7 going to the specific legal undercurrents of the
8 words in the claims.

9 The example I have in mind, I think, is
10 for a different patent.

11 Q. So is it your answer then that you
12 generally can understand questions that might be
13 legal in nature at least in connection with these
14 Samsung IPRs?

15 MR. COLAIANNI: Objection to form.

16 THE WITNESS: I think I generally
17 understand what I need to about the meaning of the
18 claims and about what's said in the specification
19 and the relationship of the specification to the
20 claims and what has been decided or not about the
21 interpretation of terms in the claims, and I think
22 that's adequate to do my job as a technical expert.

1 BY MR. CHEN:

2 Q. But sometimes you are unable to catch
3 the significance of legal terms that are used;
4 correct?

5 A. No, I don't think that's correct.

6 Q. Isn't that what you said?

7 A. That may have been what I said.

8 What I -- what I meant was that there
9 is so much in these cases that -- I'm -- I'm
10 thinking of a very specific case that happened in a
11 previous deposition and I was asked a question that
12 I think, having looked at it in retrospect, was
13 specifically about the language in the claims.

14 And I gave an answer, which was after a
15 long discussion over whatever the topic was, I gave
16 an answer which was a very simple explanation, kind
17 of bottom line statement, using as an example for
18 that answer the preferred embodiment of that patent,
19 and that was a simplification where I was thinking
20 about the specification, not about the specific --
21 specifics of the claims.

22 So I guess I just missed something

1 important that you had said when you referred to the
2 claim language, and so I thought I'm talking about
3 the patent as a whole and the example I have to
4 understand what the intellectual contribution, the
5 intellectual property is here in this patent, and I
6 thought of and described a specific preferred
7 embodiment.

8 Q. Is it true then that sometimes you miss
9 the subtlety of a question with regards to issues
10 that you consider legal in nature?

11 MR. COLAIANNI: Objection to form.

12 THE WITNESS: Well, I try not to
13 do that. I don't think it happens very often but,
14 you know, I think people are like this. Normal
15 human beings are like this.

16 If my wife asks me a question and
17 I don't listen quite right and understand why she's
18 asking it or where the question is coming from, I
19 may give an answer that is -- is incorrect in
20 getting to exactly what she asked. And I think
21 that's human nature. And I don't think it's correct
22 to make a big deal of it if there's a clarification

1 in place, which in the case I have in mind there is.

2 BY MR. CHEN:

3 Q. And so this misunderstanding that you
4 might have with regards to issues that are legal in
5 nature, this is true with response -- with regard to
6 your response to questions in your deposition;
7 correct?

8 MR. COLAIANNI: Objection. Lacks
9 foundation.

10 THE WITNESS: Well, I'm sure we'll
11 come to the question, the question that we're
12 talking around and I -- I would be much more
13 effective in addressing that if we did that in --
14 with some specifics. I don't like making such
15 generalities.

16 I think the possibility of
17 spending a day in deposition, of not -- not
18 understanding, not getting exactly what the question
19 was, is not dependent on it being a legal situation
20 or not. I think it's part of human nature and
21 clarifications are warranted in cases like that.
22 That's what I've done in the case at hand.

1 The legal aspect of it is the
2 sophistication of the legal system of what makes it
3 more likely this can happen.

4 BY MR. CHEN:

5 Q. So are you then saying that your
6 questions in deposition are unreliable until you've
7 had a chance to then clarify your responses?

8 A. Of course not. My questions and my
9 answers and discussion in deposition are 99.9
10 percent what I -- what I meant, what I think, what I
11 want to say, but once in a while on reflection, I
12 realize -- I mean, it's happened before.

13 I've been in other cases, depositions
14 before, and I may walk out for a break and say,
15 wait, I wonder if that question should have been
16 interpreted a little bit differently? And if that
17 were -- that were the case, I probably would have
18 answered it differently. This happens, but it
19 doesn't happen often.

20 Look, look, let me make it very clear.
21 I'm confident that I can address these technical
22 issues and their interaction with the claim language

1 in a perfectly accurate manner, with the caveat that
2 once in a while a subtlety of the way the question
3 was -- was -- was raised may require some
4 clarification, and we all know that we're not here
5 in depositions to ask questions that are very, very
6 precise like I would when I'm working with
7 scientists.

8 Q. When you drafted your reply
9 declaration, you did so in consultation with your
10 attorneys; correct?

11 A. Yes.

12 Q. Okay. Was it your attorneys who
13 pointed out the potential misunderstanding in your
14 prior deposition?

15 A. Hmm. I don't remember.

16 I remember reading the transcript and
17 saying, boy, that was kind of a cavalier, quick
18 answer to a complicated situation. And then I guess
19 in discussions with my attorneys, they pointed out,
20 yeah, this is -- this is really misleading
21 because -- I think because you asked about the claim
22 language, not about the specification, and I gave a

1 sweeping very brief statement about what the patent
2 is doing, and -- and we decided, you know, it's
3 worth putting that into the declaration -- reply
4 declaration.

5 Q. After you were deposed last time, you
6 were given an opportunity following the deposition
7 to review your transcript; correct?

8 A. Right.

9 Q. And you were given opportunity to
10 submit any errata that might be -- that you might
11 have to the transcript; correct?

12 A. Actually, I saw only -- I think I -- I
13 think I was sent only one -- I think I was sent only
14 one of the days' transcripts. I think you sent it
15 to me, actually. I'm not sure I got the second one.
16 So I really don't remember.

17 Q. Okay. But you didn't submit any errata
18 to your prior deposition transcripts; correct?

19 A. No, but in those cases, I would have
20 been looking for things that are more like wording
21 corrections and stuff like that.

22 Q. Okay.

1 A. I didn't pay a lot of attention to
2 that, frankly, because that's what I thought their
3 job was. Somehow I figured my attorneys could do
4 that. They'd find things like that because I guess
5 they look at the transcripts.

6 MR. CHEN: 4.

7 (Document marked, for
8 identification purposes, as Rubloff Exhibit No. 4.)

9 BY MR. CHEN:

10 Q. Dr. Rubloff, I've asked the court
11 reporter to mark as Exhibit No. 4 a document titled
12 "VLSI Handbook" edited by Norman S. Einspruch.

13 A. G. Einspruch.

14 Q. G. Sorry. Norman G. Einspruch.

15 This exhibit was submitted by you in
16 connection with your reply declaration; correct?

17 A. Yes.

18 Q. All right. If you need to -- I'm going
19 to ask you some questions about the VLSI Handbook
20 exhibit, Exhibit No. 4. If you need to refer to
21 your reply declaration, which is Exhibit No. 3,
22 please feel free to do so.

1 I believe you start the discussion of
2 this exhibit at paragraph 2B.

3 A. Uh-huh. (Reviewing document).

4 Q. So the VLSI Handbook, you state in your
5 declaration that the VLSI Handbook is a well-known
6 textbook in the area of semiconductor processing;
7 correct?

8 A. Yes.

9 Q. All right. And so it is your opinion
10 that the information in this VLSI Handbook is
11 reliable; correct?

12 A. Yes, at least as of the date that it
13 was written and published. I don't -- I don't
14 remember. Oh, this says 1985. Right.

15 Q. Is it reliable at least as through the
16 filing date of the '997 patent?

17 MR. COLAIANNI: Objection to form.

18 THE WITNESS: The filing date. I
19 don't -- I don't recall the filing date of the '997.
20 It's '96 or something like that.

21 BY MR. CHEN:

22 Q. Yeah.

1 A. Yeah, I think it would be a reasonable
2 representation of what was known at the time.

3 Q. Okay. I mean, you rely on the VLSI
4 Handbook in your reply declaration to describe what
5 a person of ordinary skill in the art would have
6 understood at the time of the filing of the '997
7 patent; correct?

8 A. Well, I rely on it as one of many
9 sources that -- I mean, I just chose this as an
10 example to fortify. I think the issue here was
11 anisotropic versus isotropic etching, but there are
12 countless such sources and -- and much shared
13 knowledge --

14 Q. Sure.

15 A. -- that I and many others have at the
16 time.

17 Q. Sure. And you selected this one as an
18 example of some of many reliable sources of the
19 information that was known at the time?

20 A. Yeah. Yeah.

21 Q. If you look at page 7 of Exhibit No. 4.
22 Well, actually, if you look at pages 7 and 8.

1 You see that there are three tables
2 there?

3 A. Yes.

4 Q. What are those tables describing at a
5 high level? We don't need to get into detailed
6 specifics. I'm just trying to understand what those
7 tables show.

8 A. Well, these are some examples of plasma
9 etching capabilities that are for different
10 materials you'd have in semiconductor technology.
11 So silicon, oxygen, titanium, lithium, tantalum,
12 things like that, that can be etched in plasma using
13 various kinds of gases. So gases containing
14 fluorine, chlorine, bromine, which are halogens that
15 are important for the removal of all the species,
16 and also oxygen and hydrogen and so on, these gases.

17 And it's an attempt to give a
18 demonstration of examples for isotropic etching and
19 anisotropic etching and selectivity, which are the
20 kinds of differentiators that you use in choosing a
21 plasma process -- etch process recipe.

22 So very often you want to be able to

1 have isotropic or anisotropic etching or you want to
2 have selectivity of one material compared to
3 another, which means different etch rates,
4 distinctly different etch rates for one material
5 compared to another.

6 And the tables are arranged by
7 categories, it appears, associated with whether
8 they're bromine, chlorine containing, or
9 fluorine-based, or unsat -- unsaturated fluorocarbon
10 versions of the fluorine-based.

11 Q. And when you say select -- when the
12 table says "Selectivity," what does that mean?

13 A. Oh. If you have a chemical process to
14 remove or, for that matter, to deposit and react on
15 a surface of some material, it will have some kind
16 of reaction rate. In this case, an etch rate.

17 So you may have a chemistry for the
18 plasma which etches, let's say, for example, silicon
19 dioxide at a considerably higher rate, maybe a
20 factor of 5 or 10, than a nitride, silicon nitride
21 or then silicon. So that's what selectivity means.

22 Q. So if the table says "High over

1 silicon," for example, it means that the etching
2 reactant will etch the targeted material at a rate
3 much higher than it will etch silicon?

4 A. Yes.

5 Q. Is that correct?

6 A. I think that's right. The terminology
7 is -- the terminology that's used -- used in many
8 cases is, it's X is high over Y. And so yes, I
9 think that means X -- the ratio of etch rate in X
10 divided by the etch rate for Y is a large number,
11 not a small number, compared to Y.

12 I always do a double-take with the
13 "over" and -- and where that comes from, I think,
14 the use of the word "over," why is it so natural to
15 say "over" is because usually you want to etch a
16 material, and then when you get to the bottom of
17 that material and now there's another material, you
18 want the second material underneath to have a low
19 etch rate so it acts as an etch stop.

20 I always use etch rate ratio.

21 Q. So if you look at, for example, the
22 first entry in Table I, the target material is

1 silicon; correct?

2 A. Uh-huh.

3 Q. And then it lists a number of different
4 gases that can be used to etch the silicon?

5 A. Yes.

6 Q. Over there on the -- in the column that
7 says "Gases."

8 And under "Anisotropy," it says it's
9 isotropic; is that --

10 A. Uh-huh.

11 Q. And then for "Selectivity," it says
12 "High over silicon oxide, silicon nitride, metals
13 and silicides."

14 You see that?

15 A. Yes.

16 Q. So that means that when you're using
17 these listed etching materials to etch silicon, they
18 should be able to etch through the silicon, but then
19 they would stop and not etch the silicon oxide or
20 silicon nitride or metals or silicides that might be
21 below the silicon; is that correct?

22 A. In a very approximate sense, that's

1 true. We use the word "stop" and that's because the
2 etch rate decreases dramatically. The caveat to
3 that is that the etch rate is rarely, if ever, zero,
4 precisely zero. So we're always talking about an
5 etch rate ratio --

6 Q. Right.

7 A. -- of one to the other.

8 Q. Right.

9 A. And if you get an etch rate ratio of 5
10 to 100 --

11 Q. Right.

12 A. -- we call that an etch stop.

13 Q. Okay. So there might be some etching,
14 but it's minimal?

15 A. Yeah. As a scientist, you know, the
16 rate of anything you should not assume can be
17 exactly zero.

18 Q. Okay.

19 A. It's like the two words never to use
20 are "always" and "never."

21 Q. Okay. Okay. So maybe a few atoms, for
22 example, of the materials at the bottom; is that

1 correct?

2 A. I mean, this is the way you do this in
3 practice is you measure the etch rate, and then you
4 can get a real etch rate ratio.

5 Q. Okay. Turning to page 8, looking at
6 Table II. Table II describes the etching properties
7 of unsaturated fluorocarbon plasmas; correct?

8 A. Yeah, that's what it says.

9 Q. All right. And if you look at the
10 second row, the materials to be etched are listed as
11 silicon oxide and silicon nitride; correct?

12 A. Yes.

13 Q. Okay. And for etching silicon oxide
14 and silicon nitride, Table II lists a number of
15 different of these unsaturated fluorocarbon plasma
16 compounds; correct?

17 A. Uh-huh.

18 Q. Okay.

19 A. Yes. Sorry.

20 Q. It lists the same compounds for both
21 silicon oxide and silicon nitride; correct?

22 A. Yes.

1 Q. Is this because these compounds will
2 typically etch both silicon oxide and silicon
3 nitride?

4 A. At -- at different rates, certainly,
5 and usually these gas -- gases are used as mixtures
6 of more than one gas. Not always, but often. So
7 the results you get in terms of degree of anisotropy
8 and selectivity would depend on exactly what the
9 process recipe is, and the temperature.

10 Q. But these plasmas can be used to etch
11 both silicon oxide and silicon nitride; correct?

12 A. Yes.

13 Q. Okay. And then in the next column on
14 anisotropy, it says "Anisotropic at high ion
15 energies"?

16 A. Yes.

17 Q. Okay. And for "Selectivity," it says
18 "High over silicon and III-V compounds"; correct?

19 A. Yes.

20 Q. All right. And that "high over
21 silicon" means that when using these plasmas to etch
22 silicon oxide and silicon nitride, the etching --

1 once it etches through the target material, the
2 etching will tend to stop on silicon; correct?

3 A. Yes, it will certainly slow down
4 substantially.

5 Q. Enough -- it would slow down enough so
6 that from a technical perspective you would consider
7 the etching to stop on the silicon; correct?

8 A. From an applications perspective, in
9 some important applications, it would be
10 functionally equivalent to stopping.

11 Q. Okay.

12 A. But there are numbers that you have to
13 look at. When -- when people design a resist mask
14 or a hard mask, to be able to do the etching, you
15 know, you'd want to know.

16 So, for example, that ratio may require
17 because it's not a perfect selectivity that you
18 adjust the thickness of the photoresist layer
19 because the photoresist also has an etch rate --
20 etch rate ratio, and you don't want it to be gone
21 before you finish the pattern.

22 That's not the best example, but it's

1 those kinds of considerations.

2 Q. In any case, these plasmas that are
3 listed in the row we were just talking about will
4 etch silicon oxide and silicon nitride at a much
5 higher rate than they will etch silicon; correct?

6 A. Yes. Right.

7 Q. Are -- I want to ask you about the --
8 the term "anisotropy" or "anisotropic."

9 In the column -- I mean, in the column
10 or in this row in the column "Anisotropy," the table
11 says "Anisotropic at high ion energies."

12 Do all etches have the same -- well,
13 let me ask you this.

14 Are there different levels of
15 anisotropy?

16 A. Sure.

17 Q. So some etches could be more
18 anisotropic than others; is that correct?

19 A. Yes.

20 Q. Okay. And how anisotropic an etch is
21 depends on certain parameters; correct?

22 A. Yes.

1 Q. What type of parameters would affect
2 the anisotropy of an etch?

3 A. So clearly the -- the materials that
4 are involved. The gas species that are present.
5 The relative concentration of the gas species. The
6 way in which the tool is set up to provide for high
7 ion energies because that's really what decides the
8 direction of the anisotropy.

9 You know, there's a -- there's a sheath
10 which surrounds all surfaces in a plasma and that
11 sheath has a voltage typically across it. It may be
12 small. It may be large. And if you hook up the
13 electrodes in the plasma one way or another, you can
14 arrange that the electrode is biased to, I believe,
15 at hundreds of volts to accelerate the ions towards
16 the surface you're trying to etch, and so the
17 bombardment energy plays into that.

18 There's a background chemical etching,
19 which is largely isotropic. It may mean, you know,
20 you can't get rid of that, but you can increase the
21 directional etching that's associated with the ion
22 charge and its acceleration to the surface.

1 So -- so the parameters that matter
2 are, unfortunately, many. It's what you put into
3 the reactor. It's how you wire it up to provide the
4 plasma energy and the voltages across the sheath and
5 such things.

6 And it's -- it has to do with the
7 consequences of etching in that system because there
8 will be reaction products which are volatile or
9 partially volatile that may end up on the sidewalls
10 of the feature you're etching down through, and they
11 also end up on the walls of the chamber and that --
12 that can sometimes affect what the actual
13 composition of gases in the chamber is compared to
14 what you intentionally put in.

15 Q. So here in this table where it says
16 "Anisotropic at high ion energies," just saying
17 something is anisotropic really doesn't tell you
18 about the level of anisotropy that would be involved
19 because you would need to know the specifics about
20 all these other parameters; correct?

21 A. Well, I think that in this table, it
22 appears to me they are not trying to distinguish how

1 much anisotropy the etching gives. And it certainly
2 can't be considering to do that here because if you
3 look at how many permutations of oxide and nitride
4 are with all these gases, there are dozens. All
5 right? So you really couldn't say it there.

6 I think a statement that may be useful
7 is that usually, usually you would like to have
8 anisotropic etching and to make it quite anisotropic
9 for the very simple reason that the miniaturization
10 of semiconductors attempts to make smaller and
11 smaller devices much more dense. And to be able to
12 pattern those structures properly, you really need
13 to be able to control things with -- to have and
14 exploit a relatively high anisotropy.

15 So it used to be the world was -- of
16 semiconductors was filled with wet etching, which is
17 in almost every case isotropic, and you lived with
18 the fact that if you wanted to etch down one micron,
19 you're going to etch one micron sideways and now you
20 don't have as much space.

21 So usually when we talk about
22 anisotropy here, we're talking about trying to get a

1 significant number, like 10 or maybe 50, something
2 like that. And maybe I should tell you an example.

3 In a DRAM memory chip, there's a
4 capacitor which is formed by etching down into the
5 silicon about a hundred times as deep as it is wide.
6 So that would require very high anisotropy.

7 Q. For a process engineer to determine the
8 level of anisotropy for a particular etch, the
9 process engineer would need to know about the
10 parameters that you had previously described, for
11 example, the gas species that are present, the
12 relative concentration of the gases, the way the
13 tool is set up, and other parameters; correct? The
14 voltages, for example?

15 A. Yeah, but usually the process engineer
16 arrives to the new job assigned to a tool which is
17 running one of these processes. So he can see,
18 okay, well, this part of the etch process I'm going
19 at a step where the flow rate of this is this and
20 the flow rate of that is that and we're running at
21 200 watts, or whatever it is. And so he has a
22 starting point and probably some documentation from

1 other experiments that people using that tool have
2 done.

3 So it's not guesswork. There's a track
4 record there. Then there are plenty of publications
5 and, for that matter, in the tools and
6 manufacturing, usually they -- they would come with
7 preprogrammed recipes.

8 So, oh, I want to do at least a factor
9 of 10 anisotropy of nitride over silicon. Let's see
10 what recipes the tool has, or maybe they have it in,
11 you know, a data brochure something like that. Let
12 me try that one and then do a design of experiments
13 in that vicinity of parameters.

14 Q. But for a process engineer to determine
15 the level of anisotropy for a particular etch, that
16 process engineer would need to understand the
17 specifics of all the parameters that you had
18 previously described; correct?

19 A. The specifics? And to understand?

20 I mean, to determine the anisotropy
21 degree, there are a couple ways to do that. One is
22 to look at the notes for that tool. Another would

1 be to do a few experiments where you build a mask
2 with a certain opening, let's say to make a trench,
3 and you just run the process. Then you take it out
4 and you cross-section it and look at an SEM, and you
5 measure, you know, what's the vertical profile.
6 It's coming down like this and then it's this at the
7 bottom.

8 And you see is it straight walls? Is
9 it tapered a little bit or not? And you ask how
10 deep did it get and how wide did it get. How much
11 wider than the mask did it get? And that would be a
12 simple estimate of anisotropy. How much did my
13 pattern widen after going how deep?

14 Q. So are you saying that in order to
15 determine how anisotropic an etch is, you actually
16 have to do the etch and measure the results?

17 A. Well, it may be already documented.

18 Q. Well, let's say you were developing a
19 new process.

20 A. Yeah, then you'd measure it. Sure.

21 Q. Okay.

22 A. But it is done all the time.

1 Q. Sure.

2 A. The pathway in the fab from the etch
3 tool to the SEM is probably well-worn.

4 Q. Just knowing what gas you're using is
5 not going to tell you how anisotropic the etch is
6 going to be; correct?

7 A. You mean just what gas?

8 Q. If all you know is the gas, for
9 example.

10 A. No. No. It will depend on power. It
11 will depend on what additive gases are included in
12 that and so on.

13 Q. Okay.

14 A. But these are well-defined recipes.

15 Q. Okay. If you look at --

16 A. You know, it's very much like the
17 kitchen. You have cookbooks and they give you
18 recipes to do things. And you can get variations on
19 that that are mild variations on a theme, depending
20 on which cookbook, and then depending on who the
21 cook is, they may make some adjustments to that.

22 Q. Okay.

1 A. But, I mean, basically people know
2 about what will happen.

3 Q. Right, but all of those factors that
4 you mentioned could affect the anisotropy of an
5 etch?

6 MR. COLAIANNI: Objection to form.
7 BY MR. CHEN:

8 Q. Is that what you're saying?

9 A. Well, I mean, I listed the factors that
10 can influence the anisotropy, yeah.

11 Q. If you look at page 6 of Exhibit 4,
12 under the heading "Parameters Affecting Anisotropy
13 and Selectivity."

14 A. Uh-huh.

15 Q. And you see it there says:

16 "Many parameters affect the anisotropy
17 and selectivity of a plasma-assisted etch. Most
18 important are the chemical nature of the reacting
19 gas or gases, the reactor type, gas pressure, and
20 applied RF power and frequency. The gas flow
21 electromaterials and spacing, wafer temperature, and
22 number of wafers etched at one time (loading) can

1 also have significant effects."

2 You see that?

3 A. Yes.

4 Q. And you agree with that statement?

5 A. Sure. There are many subtleties to
6 many of these processes, and plasma etching probably
7 has the most subtlety because it's so -- because the
8 mechanisms that are operative can be complicated,
9 quite complicated. And, I mean, this -- this
10 loading is -- is one of the more interesting ones
11 because if you put -- I mean, if you'll think about
12 it this way.

13 You put more wafers in, you're removing
14 more material. You can only remove material by
15 making volatile products that can land on the walls
16 and -- and land on other parts of the wafer, and --
17 and it also depends on there's something called
18 ARDE, aspect ratio dependent etching. So the rate
19 at which you can etch a very narrow feature deeply
20 is a different rate than if you have a wide feature.

21 So people have dealt with this -- this
22 kind of thing for a long time.

1 Q. Anisotropic etching will etch in the
2 vertical direction faster than the lateral
3 direction; correct?

4 A. Yes.

5 Q. Okay. So if all the parameters are the
6 same, an anisotropic etch will etch more material on
7 a flat horizontal surface than material that is on a
8 vertical surface; correct?

9 A. Yes.

10 Q. Okay. What if the surface is sloped?

11 MR. COLAIANNI: Objection to form.

12 THE WITNESS: So when you say
13 "sloped," do you mean the sidewalls look like this?
14 (Indicating). Or you just have like a sliding board
15 like this? (Indicating).

16 BY MR. CHEN:

17 Q. Sure. Let's say you have some --
18 instead of being perfectly vertical, you have some
19 angle to the surface.

20 MR. COLAIANNI: Objection. Vague.
21 Incomplete hypothetical.

22 THE WITNESS: I haven't thought

1 about that one. That's a complicated one if the --
2 if the tilt is significant because if you're trying
3 to do the usual anisotropic etching, you have a flux
4 of ions that have been accelerated to the electrode
5 in this direction.

6 But typically that only happens or
7 it happens primarily in the sheath region which
8 surrounds the -- which exists right up against the
9 electrode. That's where most of the voltage drop
10 is.

11 So I'd have to think hard about
12 that one because it -- if it's a substantial tilt,
13 it mixes the mechanisms in a funny way. I'd have to
14 think more about that.

15 BY MR. CHEN:

16 Q. Okay. So you can't say whether an
17 anisotropic etch process will etch more material on
18 a sloped surface than if the surface was a perfect
19 vertical?

20 MR. COLAIANNI: Objection. Vague.
21 Incomplete hypothetical.

22 THE WITNESS: I'm sorry. You said

1 a sloped surface compared to the vertical surface?

2 BY MR. CHEN:

3 Q. Yes.

4 A. Hmm. (Pause). I don't think I could
5 speculate about that.

6 Q. Okay.

7 A. I think it's -- it's a more complicated
8 problem. If it's a slight tilt from vertical or a
9 slight tilt from -- from lateral, horizontal, I
10 don't think you'd expect a big effect. But at 45
11 degrees, sorry, I'm a scientist, I have to think
12 harder about that one.

13 Q. Okay. If the surface had a contour,
14 would that also affect the amount of etching that
15 occurs?

16 MR. COLAIANNI: Objection.

17 Incomplete hypothetical. Vague.

18 THE WITNESS: Well, I guess by
19 "contour" you mean it's curved?

20 BY MR. CHEN:

21 Q. Right.

22 A. So -- so it's -- so it's a slanted

1 version where the slant angle changes with position?

2 Q. Sure.

3 A. Yeah. No. If I can't really off the
4 top of my head speculate or -- no, I shouldn't
5 speculate -- answer about the slanted case, then I
6 certainly can't answer for a sloped surface, except
7 in the limit that it's a slight tilt from either
8 vertical or horizontal.

9 Q. So let me make sure I understand you.

10 In the event that there was only a very
11 slight tilt from either the vertical or horizontal,
12 in those situations there wouldn't be that much of
13 an effect on how much material is etched in an
14 anisotropic etch; correct?

15 MR. COLAIANNI: Incomplete
16 hypothetical. Vague. Asked and answered.

17 THE WITNESS: It's harder to know
18 about the -- the case near vertical than it is the
19 horizontal one. I think there wouldn't be much
20 effect for the horizontal one.

21 A vertical one, I'd have to look
22 at where the base charge layer looks and what is --

1 what is their resist mask above and where is that
2 located and are there entry paths into the space
3 charge region -- the sheath region I should say --
4 that would be impinged upon or not. It's harder to
5 say there.

6 BY MR. CHEN:

7 Q. So even a slight tilt or angle in the
8 vertical direction could have unpredictable effects
9 on the degree of etching that occurs?

10 A. No. No. I don't know. I haven't been
11 able to analyze that situation. It certainly isn't
12 unpredictable because what happens is something you
13 can measure, but I haven't done that.

14 Q. But you have to measure it to know?

15 A. Not necessarily.

16 MR. COLAIANNI: Objection to form.

17 THE WITNESS: There are people
18 like Tim Cale and Jim McVittie and lots of people
19 who do plasma modeling, and they can probably answer
20 that question in a matter of weeks if they use their
21 standard codes.

22 BY MR. CHEN:

1 Q. Okay.

2 A. They'd have a -- they'd have a
3 computational prediction of what would happen. That
4 would be nice. So, I mean, they understand how to
5 do that, but I'm an experimentalist. So I don't do
6 that.

7 Q. And is the same true that if there was
8 some contour to the surface, that also would lead to
9 effects on the amount of etching that could occur?

10 MR. COLAIANNI: Objection. Vague.
11 Incomplete hypothetical.

12 THE WITNESS: Well, I have -- I
13 have no idea without knowing which is what the
14 contour looks like.

15 The only case that -- that I feel
16 fairly comfortable about is if this is the surface
17 here and if you say, oh, it's tilted a couple
18 degrees that way, I would say probably it's not
19 going to be very different effect.

20 But if you're talking about this
21 (indicating) or you're talking about -- I'm glad we
22 have video today -- you're talking about this or

1 you're talking about this or you're talking about
2 this (indicating), plasmas are complicated to model
3 and so I -- I can't guess at that.

4 BY MR. CHEN:

5 Q. Okay. And so just to clarify, even
6 though we have a video.

7 A. (Laugh).

8 Q. The -- the only -- when you said that
9 the only case you feel fairly comfortable with, you
10 were referring to the situation where there was a
11 slight angle off of the horizontal surface; correct?

12 A. Yeah. Yeah, and the reason I say that
13 is that when you look at cross-sectional SEMs, like
14 I mentioned earlier, I mean, typically if you take a
15 very good ruler and you draw a very straight line
16 here, it's not exactly flat. There's a little bit
17 of curvature in it, but not enough to -- to spend
18 too much worry about. As long as it's not in some
19 endangered situation with neighboring structures.

20 Q. Okay. We've been going for a little
21 over an hour. Do you want to take a break?

22 I mean, I can keep going if you feel,

1 you know, you want to.

2 A. I'm okay for another 20 minutes maybe.

3 MR. COLAIANNI: Up to you.

4 THE WITNESS: I'm -- yeah,
5 let's -- let's keep going.

6 MR. CHEN: Okay. Exhibit 5.

7 (Document marked, for
8 identification purposes, as Rubloff Exhibit No. 5.)

9 MR. COLAIANNI: Thanks.

10 BY MR. CHEN:

11 Q. All right. Dr. Rubloff, I've asked the
12 court reporter to mark as Exhibit No. 5 Patent No.
13 6,277,720, which is the Doshi reference that I
14 believe you relied on in connection with the Samsung
15 IPR of the '997 patent; correct?

16 A. Yes.

17 Q. All right. Okay. If you turn to
18 column 9 of Exhibit No. 5, which is the Doshi
19 reference, and you look at line 46.

20 This is in the section that is
21 describing the contact opening etch process;
22 correct?

1 A. (Reviewing document). Yes.

2 Q. Okay. What is listed as the etching
3 compound used to etch the BPSG layer?

4 A. So I guess starting in line 44,
5 "chemical species of the etch of the BPSG layer 14."
6 What figure is this referring to? 3E. Includes
7 C4F8, CO, and argon.

8 Q. The C4F8, that is a fluorocarbon
9 plasma; correct?

10 A. Yes.

11 Q. Okay. And that's one of the
12 fluorocarbon plasmas listed in Table II of the VLSI
13 Handbook, which is Exhibit No. 4; correct?

14 A. (Reviewing document). No, I don't see
15 C4F8 in this. There's a C3F8.

16 Q. How come the compound there is not
17 listed in Table 2?

18 MR. COLAIANNI: Objection to form.

19 THE WITNESS: Well, these are
20 examples. There are other references which would
21 cite many other examples, but I'm not sure about
22 that. I have to think about it. Let's see. C4F8.

1 (Reviewing document).

2 I wonder if C3F8 was supposed to
3 be C4F8.

4 BY MR. CHEN:

5 Q. Are you saying in the --

6 A. In the --

7 Q. In the VLSI Handbook?

8 A. Yeah. Excuse me. My chemistry fails
9 me as to what the stoichiometry, by the time you get
10 up to 3 carbons, is. I think there's a formula for
11 it, but I don't remember offhand what it is.

12 Q. Right. In your experience, have you
13 dealt with C3F8 before?

14 A. No.

15 Q. But in your experience, you have dealt
16 with C4F8?

17 A. You mean practiced etching with it?

18 Q. Yeah.

19 A. No. No.

20 Q. Oh, you haven't.

21 Do you know whether C3F8 is a compound,
22 a fluorocarbon plasma compound that is used for this

1 type of etching?

2 A. I'd have to look that up in references
3 like this. I don't know how to resolve the
4 distinction between the Doshi reference and the
5 Einspruch article here.

6 Q. Okay.

7 A. I'd have to -- I'd have to look
8 something up.

9 Q. Okay.

10 A. They may both be perfectly legitimate.
11 It's just not all listed here.

12 Q. Okay.

13 A. I don't know.

14 Q. Okay. If you go down to column 9 line
15 59.

16 A. Yes.

17 Q. There it lists the compound that's used
18 for the subsequent nitride etch; correct?

19 A. Yes.

20 Q. And the compound listed there is CHF₃;
21 correct?

22 A. Yes.

1 Q. And the CHF3 compound is listed in
2 Table 2 of the VLSI Handbook; correct?

3 A. Yes.

4 Q. All right. Have you worked with CHF3
5 before?

6 A. Yeah, that's a much more common one.
7 I'm relatively familiar with it. Have I worked with
8 it?

9 So we usually run these processes in
10 our clean room facility, and I don't -- since I
11 don't run them and my group these days doesn't do a
12 lot of etching, I can't say that I've been close to
13 CHF3 etching.

14 However, there's work that I've done
15 with Gottlieb Oehrlein, collaborations. He's an
16 expert in plasma processing, and I'd have to look
17 through my publications to try to figure out whether
18 we ever used CHF3 in something that where I was
19 involved at that level.

20 But I wasn't turning the knob that lets
21 the CHF3 in. It's either student -- my student or
22 my collaborator's student who does that. But CHF3

1 is quite common, and I certainly recall my
2 collaborator Oehrlein having published things with
3 many of these: CF₄, CHF₃ hydrogen add mixtures, and
4 the like.

5 Q. And CHF₃ is highly selective over
6 silicon; correct?

7 A. Yeah, that's -- that's certainly what
8 it says. It's highly selective for oxide or nitride
9 over silicon, but it probably depends on what
10 additives are there. So, I mean, there are so many
11 etch chemistries. They're not all in my head,
12 that's for sure. So it may be C -- CHF₃ hydrogen,
13 CHF₃ oxygen. I don't know.

14 Q. Looking at the parameters that are
15 disclosed here in Doshi in column 9 --

16 A. Uh-huh.

17 Q. -- at lines 50 -- 61 through 65.

18 Do you have understanding whether the
19 etch compounds used there are highly selective to
20 silicon or not?

21 A. (Reviewing document). Well, I think --
22 I think that they probably are in the combination

1 that's given here. This is not answered in a table
2 from the Einspruch reference, but it's kind of
3 indicated that CHF₃ is one of the species that can
4 be high selectivity over silicon.

5 And, in fact, for the application here
6 where you're trying to remove a thin nitride layer
7 that's on top of silicon at least in the diffusion
8 regions, you'd like it to be selective and not to
9 etch very fully onto the silicon.

10 MR. CHEN: All right. Why don't
11 we take a quick break and I'll look over some stuff.

12 MR. COLAIANNI: Sure.

13 THE VIDEOGRAPHER: Going off the
14 record. The time is 10:37.

15 (Recess - 10:37 a.m. - 10:53 a.m.)

16 THE VIDEOGRAPHER: We are back on
17 the record. The time is 10:53.

18 BY MR. CHEN:

19 Q. Okay. Looking back at Exhibit 5, which
20 is the Doshi reference.

21 A. Uh-huh.

22 Q. Looking at the parameters that Doshi

1 discloses, for the PC contact etch, does Doshi
2 disclose what type of electrode materials are used
3 for the etch?

4 MR. COLAIANNI: Jerry, where are
5 you looking in 5? Where -- where you referring to
6 somewhere specific?

7 MR. CHEN: Yeah. Sorry. I was
8 referring to the section that begins at column 9
9 line 34. This is the portion of Doshi where they're
10 describing the PC contact hole etch.

11 MR. COLAIANNI: Okay. Thank you.

12 THE WITNESS: So the question is
13 what?

14 BY MR. CHEN:

15 Q. Does Doshi disclose the electrode
16 materials that are used for the etch process?

17 A. Why -- why do you say "electrode
18 materials"?

19 Q. Isn't that something that's used in a
20 plasma etch?

21 A. Well, you're not etching the electrode
22 as such. He's describing here the etching of

1 materials. It would be on a silicon substrate
2 that's sitting on an electrode.

3 So do you really mean the electrode
4 that's underneath everything?

5 Q. Does the electrode that's underneath
6 everything effect -- affect the etch?

7 A. The parameters of volt -- of voltage
8 power, I think, like temperature will, but the
9 electrode material should -- should have a
10 negligible effect on the etch.

11 Q. Okay. If we look back at Exhibit 4,
12 which is the VLSI Handbook.

13 A. Yes.

14 Q. And we look at page 6.

15 A. Yes.

16 Q. And you see under the paragraph under
17 the heading "Parameters Affecting Anisotropy and
18 Selectivity"?

19 A. Yes.

20 Q. Okay. In the last sentence, it says:

21 "The gas flow, electrode materials and
22 spacing, wafer temperature, and number of wafers

1 etched at one time (loading) can also have
2 significant effects."

3 Do you see that?

4 A. Yes. I wouldn't expect the electrode
5 material, except under unusual circumstances, to
6 have an effect significant as comparable to the
7 other factors that I see there.

8 Q. So --

9 A. There certainly are places, you know,
10 it says "loading" here. As I said, if you have more
11 wafers on the electrode or fewer wafers on the
12 electrode or larger chamber surface area or smaller
13 chamber, those things can have an effect on the
14 plasma conditions and thereby on the nature of the
15 etch.

16 I think this is probably referring to
17 -- yes. Yes. In this time frame, this was probably
18 written thinking about the configuration where you
19 would have a fairly large electrode and you could
20 put multiple wafers on it, and that means that the
21 plasma is exposed to and impinging on the electrode
22 and that could be a significant effect.

1 In the era when people started doing
2 single wafer etching, for the most part, the single
3 wafer would cover nearly all of the electrode and so
4 the electrode material would be much less important.

5 Q. So are you saying that what's contained
6 in the VLSI Handbook does not apply to what's
7 described in the Doshi reference?

8 A. Well, there's a broad description here
9 in the VLSI Handbook reference and, of course, that
10 applies at some level, but it is -- it is not saying
11 here that all of these factors are equally important
12 or under what conditions which combination of the
13 factors are important. And for sure with a list
14 that long, they can't all be the same importance.

15 Q. Okay.

16 A. Some will be more. Some will be less.
17 And the example I'm giving you is that if the
18 configuration is that you're going to use an
19 electrode where the wafers don't cover all of the
20 surface, then the plasma is impinging on the
21 electrode and so the material could matter.

22 In -- in -- in more advanced

1 technologies available at the time, you would have
2 very little, if any, of the electrode directly
3 exposed to the -- the direct plasma because it would
4 be a single wafer process.

5 Q. So do you disagree with the statement
6 that electrode materials can also have significant
7 effects on the anisotropy and selectivity of a
8 plasma-assisted etch?

9 A. Do I disagree with that?

10 Q. Yes.

11 A. No. No.

12 Q. Okay.

13 A. So, I mean, to take the example of
14 electrode materials, many of these capacitive plasma
15 discharge tools that are used for directional
16 etching as an anisotropic etching may have an
17 electrode that's -- I don't know -- 20, 30
18 centimeters across.

19 And if I put one one-inch wafer on it
20 or I fill it with one-inch wafers or -- or if I had
21 a wafer to cover the whole thing, I might see some
22 differences because the etching may be creating

1 volatile products coming from the exposed part of
2 the electrode that's not covered by my samples.
3 That goes into the gas-phase. It can change the
4 plasma chemistry. It can go into the walls. That
5 can change the plasma chemistry.

6 So I would not say it can't be an
7 effect, but I think it's -- it's not at the level of
8 influencing the processes as much as most of the
9 parameters listed in the Einspruch reference.

10 Q. Okay. Would you say that the loading
11 or the number of wafers etched at one time would
12 have much more of a significant effect on the
13 anisotropy or selectivity than the characteristic of
14 the electrode material?

15 A. Well, that would depend on which plasma
16 recipe is being used, and there are enough of them.
17 I don't think I should speculate --

18 Q. Okay.

19 A. -- about that because it would be too
20 general an answer and there would certainly be
21 exceptions to that answer.

22 Q. Okay. But you agree in general with

1 the statements in the VLSI Handbook that the
2 parameters like gas flow, electrode materials and
3 spacing, wafer temperature, and number of wafers
4 etched at one time can have significant effects on
5 the anisotropy or selectivity of the plasma-assisted
6 etch; correct?

7 A. Yes, I agree with that. It's at
8 different levels and you have to understand the
9 specific cases. Sure.

10 Q. Okay. And Doshi doesn't --

11 A. These are things which are relatively
12 well understood and for which there are known
13 protocols for assessing these things.

14 Q. Okay.

15 A. In other words, those of ordinary skill
16 in the art would know how to sort these issues
17 out --

18 Q. Okay.

19 A. -- with a well-defined set of
20 experiments.

21 Q. Sure. But Doshi doesn't disclose the
22 electrode materials for the PC contact etch;

1 correct?

2 A. (Reviewing document). No, I don't
3 think that Doshi does, and I don't think it's a
4 significant shortcoming.

5 Q. Okay. And Doshi also doesn't disclose
6 the RF frequency for the etch either; correct?

7 A. Yeah, that's an interesting question.
8 I didn't look for that. (Reviewing document).

9 I did not look for that. I would be --
10 I wouldn't be surprised if it's not here, and the
11 reason I say that is that -- I don't know -- 95
12 percent, maybe more, of directional anisotropic
13 etches that are done in this time frame with these
14 kinds of techniques are done at I want to say 13.56
15 megahertz.

16 And the reason -- I know that sounds
17 strange because there are many frequencies that
18 could be used, but it's rare cases where other
19 frequencies are used. There are dual frequency
20 applications and so on, but this, I think it's -- I
21 think it's 13.56 megahertz.

22 And when I teach this in my junior

1 level microprocessing class, I always ask them,
2 where do you think that numbers comes from? And the
3 answer is: It's assigned by the FCC so that the
4 rest of the world knows to avoid that frequency for
5 interference, electromagnetic interference.

6 So it's almost certainly 13.56
7 megahertz. Maybe that's why they didn't write it
8 down.

9 Q. Okay. But looking in the section of
10 Doshi describing the PC contact etch at column 9
11 line 34 through column 10 line 3, Doshi doesn't
12 disclose the specific frequency used for the etch
13 process; correct?

14 A. No, it doesn't say it explicitly.

15 Q. Okay. And Doshi also doesn't disclose
16 how many wafers are being etched at one time;
17 correct?

18 A. I don't think so.

19 Q. Okay. Are you familiar with the TEL
20 DRM reactor?

21 A. I don't -- I don't know that one
22 explicitly. TEL is Tokyo Electron Laboratories, I

1 think.

2 Q. Yeah.

3 A. TEL we call it.

4 Q. Right.

5 A. I know that company. In fact, I have
6 students who worked there after they left me.

7 Q. But you're not familiar --

8 A. But I don't know the DRM.

9 Q. -- specifically with the DRM? Yeah.

10 A. No.

11 Q. Okay. Okay. If we could look at
12 Exhibit 3, which is your reply declaration.

13 If we look at paragraph 2E, in this
14 paragraph, you reference a section of Doshi. I
15 believe it's column 10 lines 4 to 16, which states
16 that:

17 The two-step etch of the BPSG in
18 nitride is beneficial because 'damages to the
19 corners' -- sorry -- let me repeat that -- because
20 'damage to the corners of gate structures 10 and
21 sidewall filaments 11 is substantially minimized.'"

22 Do you see that?

1 A. Yes. Near the bottom of page 4; right?

2 Q. Yes. When it says that damage is
3 minimized, that indicates that the corners of the
4 gate structures and the sidewall filaments will
5 still suffer some damage; correct?

6 A. I'm sorry. You said the corners of
7 what?

8 Q. The gate structure.

9 A. Which part of the gate structure?

10 Q. Well, the quote that I just said, it
11 said "corners of gate structures 10 and sidewall
12 filaments 11."

13 A. Yeah. Let me -- let me read the 2D and
14 2E --

15 Q. Okay.

16 A. -- to put this into context.

17 Q. Sure. Take your time.

18 A. (Reviewing document).

19 Yeah. So your question at the end of
20 paragraph 2E really is a follow-on to paragraph 2A.
21 So HSC claimed that the etch of the nitride in Doshi
22 would completely remove the nitride layer 30 from

1 the sidewall of the structure, and that's not true.
2 It's clearly explained in -- in my declaration here.
3 This is an anisotropic etch and that's not how they
4 work.

5 Q. So all I'm asking is that where Doshi
6 says in column 10 lines 4 to 16 --

7 A. Now, wait. Let me find it. (Reviewing
8 document). Yes.

9 Q. And you say that -- well, in that
10 section, Doshi says that.

11 "The two-step etch of BPSG layer 14 and
12 nitride layer 30 is particularly beneficial, as
13 damage to the corners of gate structures 10 and
14 sidewall filaments 11 is substantially minimized."

15 You see where it says that?

16 A. Yes.

17 Q. Okay. When Doshi says that the damage
18 is "substantially minimized," that indicates that
19 the corners of gate structures 10 and sidewall
20 filaments 11 will still suffer some damage; correct?

21 A. Well, this gets to zeros or not zeros.
22 (Laugh).

1 It indicates that there could be a very
2 minimal amount of damage to the sidewall filaments.
3 So if you look at the structure in FIG. 3G, which is
4 I think the one you had -- had me looking at, the NC
5 region starts the nitride removal etch with the
6 nitride layer 30 covering the sidewall filaments 11
7 and the -- 3G -- and so this etch is intended to go
8 through the nitride and then stop as soon as the
9 silicon -- as the nitride is cleared from the
10 diffusion region below.

11 And so most of that edge won't -- won't
12 touch the sidewall filament or the gate structure,
13 except right at the end when the completely lateral
14 part of that NC region is finally cleared at the
15 same time as the diffusion region is cleared of
16 nitride.

17 And then it could be -- I don't know --
18 a couple of atomic layers or something like that,
19 depending on selectivity and how well the etch was
20 timed, may go into the sidewall filament a little
21 bit. But the sidewall filament protects the side of
22 the gate structure, the gate electron, which is the

1 one we're all worried about.

2 The nitride -- I think it's nitride --
3 cap layer on the gate electrode number 26 also
4 protects the conductor. And so by providing the
5 nitride etch stop layer for the BPSG that preceded
6 -- etch that preceded it and then doing the
7 anisotropic etch to create the sidewall spacer 30,
8 the edge of the actual gate electrode structure, the
9 electrical structure, is protected.

10 So I would never say that the damage is
11 zero because that's -- that's not realizable, but
12 it's minimal, and that's what Doshi is trying to
13 accomplish.

14 Q. But during this etch, you agree that
15 sidewall filaments 11 and nitride cap 26 will be
16 etched to some degree; correct?

17 A. Perhaps to a very minimal degree, but
18 it's the surface of those volumes that's furthest
19 removed on the opposite side from where the gate
20 electrode is.

21 Q. Okay.

22 A. And it's the side -- and -- and it's

1 the sidewall filament only near the top region
2 because it's an anisotropic etch.

3 Q. Looking at FIG. 3F.

4 A. F.

5 Q. This figure depicts the contact hole
6 etch process after the BPSG layer has been etched,
7 but before the nitride layer has been etched;
8 correct?

9 A. Yes.

10 Q. Okay. Looking at nitride layer 30, at
11 the top and at the bottom of nitride layer 30, the
12 layer has some contour; correct?

13 A. I'm sorry. At the top and the bottom?

14 Q. Where nitride layer 30 covers the top
15 corner of the gate --

16 A. Oh.

17 Q. -- there's a contour there; correct?

18 A. Where it says "nC" kind of?

19 Q. Yes.

20 A. Okay.

21 Q. Nitride layer 30 has a contour there;
22 correct?

1 A. Yes.

2 Q. And at the bottom of the corner of the
3 gate structure and the diffusion region --

4 A. Yeah.

5 Q. -- nitride layer 30 also has a contour
6 there; correct?

7 A. Yes.

8 Q. Okay. And nitride layer 30 on the
9 sidewall also has an angle; correct?

10 A. A slight angle. It's -- well, it's
11 drawn as a slight angle. Actually, I'm a little
12 surprised that it's drawn that way because I think
13 the height of the gate electrode structure is half
14 micron or more, and I think given that the nitride
15 is fairly thin, I wouldn't expect much of an angle
16 there. Although there could have been an angle
17 there for the exposed surface that's inherited from
18 the shape of the sidewall of the gate electrode or
19 something prior.

20 Q. But what's shown there, it has an
21 angle; correct?

22 A. It's shown as an angle.

1 Q. So it's not completely vertical?

2 A. A small -- small angle, yeah.

3 Q. Right. The nitride layer 30, Doshi
4 discloses that the nitride layer 30 is very thin;
5 correct?

6 A. I believe so.

7 Q. Doshi says that it should be as thin as
8 possible; correct?

9 A. Yeah. I have a quick way to tell me
10 where -- where we can find that. Ah. I see
11 actually 9-57. "As nitride layer is relatively
12 thin." Is that what you meant?

13 Q. It's there. I think it's also in
14 another place, and I'm going to find it for you.

15 Looking in column 8 line 14, you see it
16 says:

17 "It is preferred that nitride layer 30
18 be as thin as possible to minimize etch time."

19 A. Right, but sufficiently thick to do its
20 job as a spacer and -- and dopant diffusion barrier
21 in a few lines that follow that.

22 Q. Where does it say it's to do its job as

1 a spacer?

2 A. Well, I use the word "spacer" meaning a
3 barrier.

4 Q. Oh.

5 A. The barrier layers. Typically barrier.

6 Q. But the dopant diffusion layer is what
7 you are referring to?

8 A. Yeah. Yeah.

9 Q. Okay. Okay. Turning to paragraph 2H
10 of your declaration. Actually, let's look at Doshi
11 again.

12 So the second step of the PC contact
13 etch in Doshi is to etch the nitride layer 30;
14 correct?

15 A. I'm sorry. The second step of what did
16 you call it?

17 Q. I called it the PC contact.

18 A. Yeah, I think that's fair. There's the
19 BPSG oxide etch and then there's the nitride etch.

20 Q. Right. The first step is BPSG contact
21 etch?

22 A. Right.

1 Q. And the second step is the nitride --

2 A. Right.

3 Q. -- etch?

4 In the nitride etch, the purpose of
5 that etch is to remove nitride layer 30 and expose
6 the diffusion regions; correct?

7 A. That's one of the purposes.

8 Q. Okay. You do not want any nitride
9 material left on the diffusion region; correct?

10 A. Yeah, you'd like to remove all of it.

11 Q. You want to make sure that all -- any
12 nitride residue over the diffusion region is
13 completely removed; correct?

14 A. Yeah. Well, completely in the sense
15 that you want a contact area to be as large as
16 you've defined it lithographically or by
17 self-alignment technique. You have a target area.
18 So that's what you'd like to have.

19 The contact resistance is what's
20 important here. Well, it's more than that. It's
21 the Schottky barrier height of only a contact and so
22 there are many variables. One of those is the

1 contact resistance dependence on contact area.

2 So if, for example, there is a little
3 bit of nitride level someplace, it will reduce the
4 contact area and increase the contact resistance a
5 little bit. So to say that you have to completely
6 remove in the sense of every atom, that's not --
7 that's not the case.

8 Q. Having nitride material left in the
9 diffusion region would reduce the effectiveness --
10 effectiveness of the contact; correct?

11 A. Yes, by some amount proportional to the
12 area that's impeded.

13 Q. And that would reduce the performance
14 of the device you're trying to manufacture; correct?

15 A. That's a harder question. Because when
16 you ask about performance, typically you have a
17 number of things that contribute, and let me say, in
18 series to that performance. And so sometimes
19 there's one factor which could impede the
20 performance, but in the scheme of things, something
21 else is doing all the impeding of performance.

22 So if you make that a little bit

1 better, it doesn't help the performance. So
2 that's -- I mean, your statement is -- is, you know,
3 generally what we think about, but in specifics, I
4 don't think it's -- it's an accurate statement.

5 Generally speaking, we want to improve
6 each of these components to performance, but I
7 always hesitate to stretch things to say -- well,
8 the implication would be if I say that the contact
9 resistance and the amount of nitride that might be
10 stuck or something else on that surface -- could be
11 carbon contamination -- if I say that each one of
12 these things is going to affect performance, then
13 someplace I'm wrong.

14 Q. In general, you want to have good
15 contacts; correct?

16 A. Yes.

17 Q. Okay. And having nitride material left
18 on the diffusion region would affect the
19 effectiveness of the contact; correct?

20 A. By some amount, small or large or
21 whatever.

22 Q. So when manufacturing these devices,

1 you do not want to leave nitride material left on
2 the diffusion region; correct?

3 A. Correct. You'd like to remove the
4 nitride that you intended in designing the process
5 to do so.

6 Q. Okay. You want to get rid of as much
7 of the nitride material over the diffusion region as
8 possible; correct?

9 A. It's a little too much of a stretch
10 because it may well be that you have a situation
11 where, whether it's nitride or it's carbon residues
12 from the etch or something like that, there's a
13 problem, but it's a little problem.

14 And so if I say that I have to get rid
15 of as much as possible, I could have a process
16 engineer chasing this for three months full time
17 trying to get rid of that last little bit. And the
18 process integration engineer is saying, it doesn't
19 matter. Don't waste your time.

20 I'm sorry for being so detailed about
21 this, but I think it's a really important concept.
22 It's one I teach my students all the time. You have

1 to look at where are the bottlenecks in the system.

2 Q. No. I mean, semiconductor processes
3 are very complicated; right?

4 A. Yes.

5 Q. A lot of the different steps are
6 interrelated?

7 A. Yes.

8 Q. And certain factors can affect other
9 things in unpredictable ways; correct?

10 A. Yeah. Uh. Sometimes unpredictable.
11 (Laugh).

12 Q. However, you would agree that, in
13 general, you would like to remove the nitride over
14 the diffusion region in order to have a good
15 contact; correct?

16 A. I agree to that, yes.

17 Q. Okay.

18 A. That's -- that's the purpose of that
19 etch --

20 Q. And so --

21 A. -- in part.

22 Q. -- when designing the etch to remove

1 the nitride layer, you would design in some amount
2 of overetch to ensure that the nitride material is
3 removed; correct?

4 A. Yes, that's likely.

5 Q. When you're manufacturing these
6 devices, they are manufactured on wafers; correct?

7 A. Yes.

8 Q. And there are millions of these devices
9 on a single wafer; correct?

10 MR. COLAIANNI: Objection to form.
11 Vague.

12 THE WITNESS: By "device" do you
13 mean a transistor or do you mean a wafer or --

14 BY MR. CHEN:

15 Q. I don't mean a wafer.

16 A. -- a circuit?

17 Q. When I'm saying "a device," I'm
18 referring to, for example, the device that's being
19 described in, say, the Doshi reference. The --

20 A. Well, if you say how many you have when
21 you have a transistor, you have a gate electrode.
22 If you ask how many gate electrode points are there

1 where there's a source and drain associated with it,
2 yeah, it's millions.

3 Q. So the, for example, the contact hole
4 etching process that we've been talking about, there
5 are millions of these contact holes that need to be
6 etched across the wafer; correct?

7 A. Yes.

8 Q. Okay. And there will be minor
9 variations between each of the contact holes on the
10 wafer; correct?

11 A. Typically very minor, yes. That's why
12 the term "Six Sigma" was -- became very popular kind
13 of in that time frame.

14 Q. Right. You would like to keep the
15 vary -- variation as small as possible; correct?

16 A. Yeah.

17 Q. For manufacturability?

18 A. Yeah, right.

19 Q. But there still inevitably will be some
20 variation?

21 A. Yes, absolutely.

22 Q. And this variation would be, for

1 example, in the thickness of various layers;

2 correct?

3 A. Could be in the thickness, the
4 conductivity or some. Sure.

5 Q. Okay. And when you're designing the
6 process, you need to design the process to take into
7 account the fact that there will be minor variations
8 from device to device; correct?

9 A. Yes, you usually try to design -- you
10 usually try to design the processes, the masks, the
11 structures you're trying to make so that they have a
12 certain amount of tolerance to these variations,
13 yes.

14 Q. So, for example, for some contacts, the
15 nitride layer 30 might be a little bit thicker and
16 for other contacts, the nitride layer 30 might be a
17 little bit thinner; correct?

18 MR. COLAIANNI: Objection.
19 Hypothetical.

20 THE WITNESS: If you -- so -- so
21 normally when people develop let's say the nitride
22 CVD process, they will characterize uniformity

1 across the wafer. These days you have, and in those
2 days actually, that would have been 6- or 8-inch
3 wafers, something like that. You will have
4 specifications that the RMS uniformity has to be 1
5 percent on thickness, something like that.

6 So there are variations across the
7 wafer, and there may be local variations in -- in
8 thickness in deposition or in etch rate or something
9 like that, yes.

10 BY MR. CHEN:

11 Q. Okay. And so then when you're
12 designing the process to remove the nitride layer
13 30, you want to design it to make sure that it
14 removes that layer for all of your devices across
15 the wafer; correct?

16 A. Yes.

17 Q. So the etch, for example, would need to
18 be long enough for the device that has the thickest
19 layer of nitride layer 30; correct?

20 A. Yes. That's what the overage is about.

21 Q. Okay.

22 A. In part, at least.

1 Q. Can you turn to Doshi, which is Exhibit
2 5, and could you turn to FIG. 3K.

3 FIG. 3K depicts the results of the
4 bit-line contact etch; correct?

5 A. Yes, that's what it says, but that's
6 not what it is as depicted. This is detailed in my
7 reply.

8 Q. Doshi says that FIG. 3K shows the
9 result of the bit-line contact etch; correct?

10 A. I think that's what it says, yeah.
11 Which -- which column are you at?

12 Q. Column 11 lines 11 and 12, it says:
13 "Following the opening of bit-line
14 contact opening BLC as illustrated in FIG. 3K."

15 A. (Reviewing document). Yes, I know
16 that's what it says.

17 Q. Okay. Now, looking at FIG. 3K.

18 A. Yes.

19 Q. Looking at the gate structure that is
20 next to the bit-line contact opening.

21 A. Yes.

22 Q. FIG. 3K does not show damage to gate

1 structures 10 and sidewall filaments 11 of that gate
2 structure; correct?

3 A. Yeah, the problem is that FIG. 3K is
4 misdrawn by the draftsman -- draftsman and not
5 caught by the inventors, I guess.

6 I mean, it's totally inconsistent with
7 the description in the -- in the specification. It
8 is totally inconsistent with the teaching of the
9 patent. And if -- if you look at the description
10 of -- of the BLC etch process, it says at column 10
11 line 40:

12 "As in the formation of the plug
13 contact location PC, bit-line contact location, BLC
14 is formed by way of a two-step etch. The first step
15 is an oxide etch" blah blah blah "and this first
16 etch step is carried out under similar conditions as
17 the etch of the -- of the BPSG layer 14 at plug
18 contact locations PC."

19 And then later on for the nitride, it
20 says essentially the same thing. In other words,
21 this should look just like the plug contact. And
22 when I first studied this patent, I remember

1 thinking, what on earth is wrong here? This doesn't
2 make any sense. They're doing the same thing. It
3 should look -- you know, usually when you do the
4 same set of things, you get the same result.

5 Q. You noticed that when you first studied
6 the patent?

7 A. Yeah, I remember this. I said maybe I
8 won't have to worry about the bit-line contact
9 because maybe the issue is all the plug contact, and
10 I said I don't know. I don't have to worry. Until
11 they tell me that -- that I need to worry about it,
12 then I'll just ignore it, but it looked wrong.

13 Q. Okay.

14 A. It's a drafting error and they happen.
15 It's shocking how often they happen.

16 Q. So you saw this error when you first
17 studied the Doshi reference; correct?

18 A. I -- I looked through -- when I look at
19 a patent, I look at how long is the specification
20 and how many figures are there, and I glanced
21 through these and I saw that looks funny. I hope
22 that's a different embodiment, or something like

1 that. I didn't look at it after that because I
2 hoped that it wouldn't be relevant. But when I got
3 into this patent, then the focus was on the plug
4 contact.

5 Q. And then you noticed this alleged error
6 in 3K before you submitted your first declaration;
7 correct?

8 A. I vaguely remember noticing this. I
9 guess it -- I don't know. You know, these patents
10 often have a whole bunch of stuff that's not
11 relevant to the patent issue at hand, and some of
12 them have 30 figures and so on and so at least
13 that's my training in this business.

14 So I didn't notice this at the level
15 that I thought it was significant. I thought I
16 wouldn't have to worry about it. I don't remember
17 exactly when in the process I noticed this, but I
18 remember saying, something looks weird here.

19 Q. And this was before you submitted your
20 first declaration; correct?

21 A. I'm not sure when it was.

22 I mean, for example, FIG. 2C, the issue

1 at hand here is primarily the vertical profile
2 that's achieved by the set of steps to make these
3 structures and, in particular, on the self-aligned
4 contact description that involves two different
5 kinds of etches and sidewall structures and the
6 like.

7 So FIG. 2C, I glanced at it, but I
8 don't remember studying that part of the figures or
9 the patent in any great detail, and I don't know
10 when that would have been.

11 Q. Are you saying that there's errors in
12 FIG. 2C as well?

13 A. No, I'm not saying anything of the
14 like. The reason I know there's an error in 3K is
15 when I got to looking at what -- what do you mean by
16 the invention of a self-aligned contact here and the
17 two layers that are etched in doing that and the
18 sidewall spacer that's formed in doing that so you
19 can make a borderless contact, then I -- I came to
20 the point of focusing on the FIGS. 3 up through G
21 and then following it through because they should be
22 consistent.

1 And then I saw, oh, I really do have to
2 deal with this and, ah, this is a mistake. I
3 thought it was -- when I first -- when I first saw
4 it, I thought it was -- I don't know. I don't
5 remember what the scenario was, but the first time I
6 looked at it with any intensity, whenever that was,
7 it was pretty obvious to me that this was a drafting
8 error.

9 Q. But you don't remember whether you
10 looked at FIG. 3K with any intensity before you
11 submitted your first declaration in this case?

12 A. I don't remember timing. Because in
13 understanding the patent, I was focused on 3G and
14 the plug contact, which is most of the description
15 that's given in the spec.

16 Q. You said just a few minutes ago, when I
17 first referred you to FIG. 3K, you said:

18 "When I first studied this patent, I
19 remember thinking, what on earth is wrong here?
20 This doesn't make any sense. They're doing the same
21 thing. It should look -- you know, usually when you
22 do the same set of things, you get the same result."

1 So you said that you noticed this
2 alleged error or discrepancy between FIGS. 3G and 3K
3 when you first studied the patent; is that correct?

4 A. When I first studied that part of the
5 patent. So my recollection is that we had an
6 extensive discussion about the fact that there is
7 another place at the NC region in the plug contact
8 where there should have -- should have shown some
9 erosion at the top surface of layer 30 and that went
10 into my declaration because that --

11 Q. Your first declaration?

12 A. Yeah.

13 Q. Okay.

14 A. Yeah. So that went into my
15 declaration. I remember we had discussions about
16 that. What's the meaning of this? Is this drawn
17 wrong? And so on.

18 If I had thought much at that point
19 about FIG. 3K and the BLC contact, I would have put
20 that in as well into that declaration.

21 So I don't know when I first noticed
22 this, but I apologize if I prefer not to study

1 things that are not relevant to the case at hand.

2 Q. So when you submitted your first
3 declaration in connection with Samsung's IPR of the
4 '997, you didn't study the whole Doshi reference;
5 correct?

6 A. I studied it but, you know, you focus
7 on different things. So I didn't pick up on this
8 enough to flag it and say, hmm, this -- this is
9 wrong. Let's put it in the declaration.

10 Q. Looking at FIG. 3K, I asked you
11 previously.

12 FIG. 3K does not show damage to gate
13 structures 10 and filaments 11; correct?

14 A. You mean the left side or the right
15 side of the figure?

16 Q. If you look at FIG. 3K --

17 A. Yeah.

18 Q. -- and you look at the transistors or
19 the gate structures next to the bit-line contact
20 opening.

21 A. Okay.

22 Q. Do you see that?

1 A. Yeah, I see that.

2 Q. FIG. 3K does not show damage to the
3 gate structures 10 or filaments 11; correct?

4 A. Yeah, but I don't understand. I can't
5 speculate about that when the figure is drawn
6 incorrectly.

7 If you'd like to have the same
8 discussion about 3G, which is the structure that's
9 described here, then -- then we can do that. Or
10 there's a version -- I think I put a version in my
11 declaration of what it should have looked like at
12 the BLC contact, but this would be complete
13 speculation.

14 Q. I'm asking you about the figure that is
15 actually shown in the Doshi reference. Okay?

16 FIG. 3K in the Doshi reference, does it
17 show damage to gate structures 10 or filaments 11 in
18 the structures next to the BLC contact opening?

19 A. I don't know how I would know.

20 Remember, we talked about an etching in
21 the PC contact. We talked about etching the nitride
22 layer at the NC region. You asked if there would be

1 any damage to that edge of the sidewall structure --
2 what is it 11? -- 11. And I said yes, it would be
3 likely some overetch and so there would be damage,
4 but that's the side of the insulator furthest from
5 the gate electrode so it won't matter.

6 But that is -- that minimal amount of
7 erosion by the overetch of the nitride wouldn't show
8 up in the figure. So I can't tell it.

9 Besides the fact that the figure is a
10 cartoon that's inconsistent with the rest of the
11 patent. I don't know how to speculate. That's the
12 answer to your question.

13 Q. So you're saying you -- looking at FIG.
14 3K, you cannot answer whether FIG. 3K shows damage
15 to gate structures 10 or filaments 11; correct?

16 A. Well, I just don't think I should
17 speculate about a drawing that's clearly wrong.

18 I mean, this is not a self-aligned
19 contact hole because the hole in the mask is
20 directly above the edges of the diffusion region.
21 So this is contrary to everything that this patent
22 is about in terms of telling you how to make a

1 self-aligned contact that's tolerant of lithography
2 errors. The kinds of errors that you were talking
3 about just a few minutes ago.

4 Q. Doshi says that they're trying to form
5 self-aligned contacts?

6 A. Doshi -- as I recall, Doshi doesn't
7 make a big point about -- about calling them
8 self-aligned contacts, but the design is exactly the
9 same and accomplishes the same function.

10 Q. Doshi doesn't use the term
11 "self-aligned contacts" when referring to the
12 contact holes; correct?

13 A. I don't think it's emphasized. I don't
14 know if it's used. I'd have to look through. But
15 that's what's accomplished for sure because that's
16 what spacers are all about.

17 Spacers -- this formation of sidewall
18 spacers is one of the first things I learned when I
19 started moving from pure science to applied science
20 in my career, and it's a very basic principle.

21 Q. Doshi doesn't say that they're trying
22 to form sidewall spacers from nitride layer 30;

1 correct?

2 A. Well, I can look through. I don't
3 recall a place where it's emphasized. I don't know
4 if -- if the words are used that way, but it's
5 exactly what function is accomplished. One of the
6 functions that's accomplished.

7 (Reviewing document). Hmm. So in --
8 in Doshi column 3 line, oh, 45 -- this is in the
9 background of the invention -- Doshi talks about
10 using -- let me see.

11 Silicon nitride is a diffusion barrier
12 for boron and phosphorous which are going to go into
13 the plug contact that -- that fills the hole, and it
14 talks about etching and difficulties in the etch of
15 conformal nitride layers, "particularly in
16 overetching and degradation of the nitride film at
17 the upper corners of structures such as gate
18 structures 10 in FIG. 1.

19 Attention in this regard is directed to
20 commonly assigned copending application" number
21 number number entitled the "Silicon Nitride Sidewall
22 and Top Surface Layer Separating Conductors."

1 So the sidewall formation is mentioned
2 here. It's not -- but this doesn't say
3 "self-aligned contact," but one of ordinary skill
4 knows that one of the prime drivers for using
5 conformal deposition followed by anisotropic etching
6 is to form sidewall spacers that help in functioning
7 as diffusion barriers, electrical isolation
8 barriers, and self-alignment of contacts to improve
9 lithography. So I think it's implicit here.

10 Q. Doshi doesn't specifically say that
11 they're forming sidewall spacers with nitride layer
12 30; correct?

13 A. Well, it's clear that that's what
14 happens, and it's clear that that's the motivation
15 that's happening here from what I just cited.

16 I mean, down at the bottom of that
17 column, there's more about this.

18 "These silicon nitride sidewall
19 filaments are conventionally formed by CVD of
20 silicon nitride overall, followed by an anisotropic
21 nitride etch to remove the nitride from the flat
22 active regions, leaving sidewall filaments behind."

1 And you can do that once or you can do
2 it twice.

3 Q. There's no question there that Doshi
4 forms sidewall filaments; right?

5 A. Yeah.

6 Q. But when Doshi is describing nitride
7 layer 30 --

8 A. Uh-huh.

9 Q. -- which is not used to form the
10 sidewall filaments, Doshi does not specifically say
11 that that nitride layer 30 is used to form spacers;
12 correct?

13 MR. COLAIANNI: Objection to form.
14 Asked and answered.

15 THE WITNESS: (Reviewing
16 document). So in column 10, there's a description
17 of the consequences of the two-step etch of the BPSG
18 and the nitride layer, and it refers to the fact
19 that in -- as depicted in, let's say, 3, 3G or 3F,
20 3F, it talks about the NC region, the damage to
21 that. The corner there will be very little, and it
22 makes it clear we're talking about a highly

1 anisotropic etch to clear the region above the n+
2 region.

3 And so if there's very little
4 damage at the NC corner and it's a highly
5 anisotropic etch, then the layer 30 will remain on
6 the sidewall as depicted properly in 3F and 3G.

7 Answer: That's a spacer, whether
8 it's called a spacer or not.

9 BY MR. CHEN:

10 Q. Doshi doesn't say that layer 30 remains
11 on the sidewall; correct?

12 A. Well, he essentially does because he's
13 -- he's telling us that you use an anisotropic etch,
14 and that means it's like raindrops. It's coming
15 down from the top, and if there's very little
16 etching at the NC corner region so you'll make --
17 don't make damage to the structure -- the sidewall
18 filaments 11 and cap layer there, then it certainly
19 is the case that the sidewall part of layer 30 is
20 under the umbrella of that rain. It's not being
21 etched.

22 Q. Doshi doesn't specifically say that

1 layer 30 remains on the sidewall after the nitride
2 etch; correct?

3 A. Well, I can keep looking. I think he
4 implies it, at the very least.

5 Q. But he doesn't say it; correct?

6 A. (Reviewing document). Let me think.
7 (Reviewing document).

8 Well, he talks about barrier to dopant
9 diffusion as well.

10 I don't think the words are there, but
11 to one of ordinary skill in the art, I think it
12 would be very clear that the self-alignment
13 technique is practiced here and taught here, and
14 that a spacer does result from anisotropic etching
15 of the layer 30 nitride.

16 I mean, I thought the issue is whether
17 one of ordinary skill, having read this, would know
18 how to do what's taught in the '997 patent, and
19 someone reading Doshi would know how to do that.

20 Q. But you agree that Doshi doesn't
21 specifically teach that nitride layer 30 remains on
22 the sidewall of the gate structure after the nitride

1 etch; correct?

2 A. No, I disagree. One of ordinary skill,
3 having read the structures, the conformality of the
4 layers that's produced, and the anisotropy of the
5 etch, would certainly know that the nitride 30 is
6 left on the sidewalls.

7 Q. Doshi never states that nitride layer
8 30 remains on the sidewall of the gate structure
9 after the nitride etch; correct?

10 MR. COLAIANNI: Objection. Asked
11 and answered.

12 THE WITNESS: I think -- I think
13 it's implied directly. I haven't looked through
14 every word of the structure to see if there's any
15 other supporting evidence that he's being more or
16 less explicit about it, but the teaching is really
17 clear.

18 BY MR. CHEN:

19 Q. When Doshi is describing the nitride
20 etch of nitride layer 30, Doshi doesn't say that
21 nitride layer 30 remains on the sidewalls of the
22 gate structure after the nitride etch; correct?

1 MR. COLAIANNI: Asked and
2 answered.

3 THE WITNESS: Yeah, I think
4 I've -- I've said about all --

5 BY MR. CHEN:

6 Q. You have not answered the question.

7 I'm asking you: Does Doshi
8 specifically say that? Does it or does it not? Can
9 you answer that question?

10 A. Well, I --

11 MR. COLAIANNI: Asked and answered
12 multiple times.

13 THE WITNESS: I haven't looked --
14 you know, to say that something doesn't exist means
15 you have to look carefully and make sure that it
16 doesn't exist. So I have not looked carefully
17 through this.

18 He certainly does not make it
19 explicit in the words that you're saying, but to
20 anyone who reads Doshi and has reasonable ordinary
21 skill in the art, they would know it immediately.
22 My junior level students know it. (Laugh).

1 BY MR. CHEN:

2 Q. When you say you haven't looked
3 carefully at Doshi --

4 A. No, that's not what I said.

5 I haven't looked for the words you're
6 asking for.

7 Q. So in conducting your analysis for the
8 Samsung IPR, you did not look carefully through
9 Doshi to determine whether Doshi specifically says
10 that nitride layer 30 is left on the gate structure
11 after the nitride etch?

12 A. I followed the technical arguments
13 here, and I knew that it's there. I don't remember
14 that I scoured -- I mean, I wasn't faced with the
15 question you're asking, which is, do these words
16 appear in how many pages of text?

17 When I -- when I read -- I'm sorry.
18 I'm a -- I'm a technical person. When I read this,
19 I'm trying to understand what it teaches, and I can
20 easily see what it's teaching me. And in the
21 context of another patent like the '997, the
22 language that's used may be different to describe

1 that, but the function is the same.

2 Q. But you agree that words stating that
3 nitride layer 30 is left on the sidewalls of the
4 gate structure after the nitride etch do not appear
5 within Doshi; correct?

6 MR. COLAIANNI: Asked and
7 answered.

8 THE WITNESS: Well, as I said
9 before, I haven't found them here yet, but I have
10 not looked exactly for those words.

11 BY MR. CHEN:

12 Q. Sitting here today, you cannot point me
13 to any portion of Doshi which has the words that say
14 that nitride layer 30 is left on the sidewalls of
15 the gate structure after the nitride etch; correct?

16 A. Well, I haven't done that, but I think
17 you're pushing this to limits that, to me, don't
18 make sense.

19 I mean, if I -- if I fill this cup with
20 water and I disclose that I'm filling the cup with
21 water and somebody else says, well, there's water in
22 the cup, but I didn't say there's water in the cup,

1 is there water in the cup? Yes, I filled the cup
2 with water. This is kind of argument that I think
3 you're pushing here. The functionality is there.

4 Q. Dr. Rubloff, I just need you to answer
5 my questions. Okay?

6 Can you point me to any portion of
7 Doshi which has words that say that the nitride
8 layer 30 is left on the sidewalls of the gate
9 structure after the nitride etch?

10 MR. COLAIANNI: Objection. Asked
11 and answered multiple times.

12 THE WITNESS: The description of
13 the etch and its consequences here make it clear to
14 one of ordinary skill that that's the case, but I
15 don't see the words at this point in time.

16 MR. CHEN: All right. Why don't
17 we break for lunch.

18 THE VIDEOGRAPHER: We're going off
19 the record. The time is 12:08.

20 (Whereupon, at 12:08 p.m., a
21 luncheon recess was taken.)
22

1 AFTERNOON SESSION

2 (1:06 p.m.)

3 GARY W. RUBLOFF, PH.D.

4 called for continued examination and, having been
5 previously duly sworn, was examined and testified
6 further as follows:

7 CROSS-EXAMINATION (CONTINUED)

8 THE VIDEOGRAPHER: We are back on
9 the record. The time is 13:06.

10 BY MR. CHEN:

11 Q. Prior to the break, we were discussing
12 the Doshi reference, which was Exhibit No. 5.

13 The etch parameters that Doshi
14 describes for the plug contact etch are
15 substantially the same as the etch parameters that
16 Doshi describes for the bit-line contact etch;
17 correct?

18 A. I think that's right, but let me look
19 and make sure.

20 You mean for both -- for both etches,
21 BPSG or the nitride?

22 Q. Yeah, we can address them individually.

1 A. (Reviewing document). Yes, I've looked
2 at both the BPSG etch and the nitride etch. They
3 look essentially the same or certainly very close.

4 Q. The nitride etch described for the plug
5 contact etch and the bit-line contact etch are
6 identical; correct?

7 A. I -- I think so. I mean, I just
8 scanned them, but it looks that way. CHF3, 50 sscm
9 with CO 175, sscm timed etch 10 seconds or on the
10 order of 10 seconds for the BLC. Yeah, I think so.

11 Q. Okay. And you believe that the
12 resulting etch profiles for the plug contact etch
13 and the bit-line contact etch should look the same;
14 correct?

15 A. Well, yes, insofar as the starting
16 structures are the same. With regard to -- with
17 regard -- let's see how this -- are the heights any
18 different for the FETs? I think not.

19 I think so, yes. Certainly they should
20 look a lot more alike than they do with the drafting
21 error I cited in -- in 3J and K. K. I'm not -- not
22 J. K.

1 Q. You also cited a drafting error in FIG.
2 3G; correct? In the figure.

3 A. Yes.

4 Q. The sidewall filaments 11 shown in
5 Doshi are spacers; correct?

6 A. Yes.

7 Q. And Doshi describes the formation of
8 those sidewall filament spacers; correct?

9 A. Yes.

10 Q. And I believe Doshi describes the
11 formation of those sidewall filament spacers
12 beginning at column 7 line 57; correct?

13 A. Yes.

14 Q. And there Doshi states that:

15 "According to the preferred embodiment
16 of the invention, sidewall filaments 11 are formed
17 by first oxidizing the sides of the polysilicon
18 layer 22. A layer of silicon nitride is then
19 deposited overall, and then etched isotropically to
20 remove the nitride from the flat surfaces, leaving
21 sidewall filaments 11 behind."

22 Correct?

1 A. Yes.

2 Q. When Doshi describes the formation of
3 the sidewall filaments, Doshi explicitly states that
4 the nitride material is removed from the flat
5 surfaces while the nitride material on the sidewalls
6 are left behind; correct?

7 A. Yes.

8 Q. There is no such description, no such
9 explicit description of nitride material being left
10 behind on the sidewalls when Doshi is describing the
11 etch of nitride layer 30; correct?

12 A. (Reviewing document). So we're at
13 column 7 line 60 or something like that? That's
14 where you mean for the plug contact, this business
15 about the nitride residue?

16 Q. No. Column 7 beginning at lines 57 is
17 describing the formation of the sidewall
18 filaments --

19 A. Right. Right.

20 Q. -- that we agree are spacers; correct?

21 And when it's -- when Doshi is
22 describing the formation of the sidewall filaments,

1 it is explicitly stating that the etching of the
2 nitride material would leave that nitride material
3 on the sidewalls to form the sidewall filaments;
4 correct?

5 A. Yes.

6 Q. It explicitly states that material is
7 left behind on the sidewalls in this case; correct?

8 A. Yes.

9 Q. All right. But Doshi does not do that
10 when it's describing the nitride etch of nitride
11 layer 30 in the plug contact or bit-line contact
12 locations; correct?

13 A. (Reviewing document). So column 7 line
14 62 or so talks about "silicon nitride residue may
15 remain along the sides of field oxide structures 5."

16 And is that what you're trying to
17 compare to the layer 30?

18 Q. No.

19 A. I'm sorry, I'm not following you.

20 The statement about residues of silicon
21 nitride that I see is lines 62 to 65 or so, and it's
22 talking about the slanted regions at the bird's beak

1 of the -- of the field isolation regions.

2 Q. All right. Let's try this again.

3 Let's look at figure -- let's look at
4 FIG. 3A.

5 A. 3A?

6 Q. Yes.

7 Do you see on the gate structure there
8 is the sidewall filaments 11?

9 A. Yes.

10 Q. And that's a spacer; correct?

11 A. Yes.

12 Q. All right. Now, in the section in
13 column 7 of the Doshi reference, Doshi is describing
14 the formation of those sidewall filament 11s;
15 correct?

16 A. Yes.

17 Q. And what Doshi says beginning at column
18 7 line 57, it says:

19 "According to the preferred embodiment
20 of the invention, sidewall filaments 11 are formed
21 by first oxidizing the sides of the polysilicon
22 layer 22. A layer of silicon nitride is then

1 deposited overall and then etched anisotropically to
2 remove the nitride from flat surfaces, leaving
3 sidewall filaments 11 behind."

4 Correct?

5 A. Yes.

6 Q. That's what Doshi is saying when it's
7 describing the formation of the sidewall filaments?

8 A. Uh-huh.

9 Q. And when Doshi is describing the
10 formation of the sidewall filaments and Doshi is --
11 all right.

12 And when Doshi is describing the
13 nitride etch used to form the sidewall filaments,
14 which is an anisotropic etch, Doshi specifically
15 states that material, the nitride material, is left
16 on the sides of the gate structure to form those
17 sidewall filaments; correct?

18 A. Yeah, "leaving sidewall filaments 11
19 behind."

20 Q. Right.

21 A. That's on the side of the gate
22 electrode.

1 Q. Right. Right.

2 Doshi -- but when Doshi is describing
3 the nitride etch for the plug contacts or the
4 bit-line contacts, which are described at column 9
5 beginning at line 56 for the plug contact and column
6 10 line 63 for the bit-line contact, Doshi does not
7 explicitly state that after the nitride etch
8 material is left behind on the sidewalls of the
9 gate; correct?

10 A. (Reviewing document). Yes, I think
11 that's correct. It's not explicit here.

12 Q. Okay.

13 A. But it's the same recipe on 30 as it
14 was for 11. Conformal layer over a structure,
15 anisotropic etching leaves the sidewall field.

16 Q. Well, for the formation --

17 A. It doesn't state it explicitly the same
18 way.

19 Q. For the formation of sidewall filament
20 11, Doshi does not actually tell you what the
21 specific parameters of the nitride etch are;
22 correct?

1 A. Yes, I think that's right. It doesn't
2 give as much information. Because the focus of the
3 patent is more on the layers 30 and the BPSG, I
4 think.

5 Q. So we can't really say that the etch
6 for the formation of the sidewall filament is the
7 same as the etch for the nitride layer 30; correct?

8 A. The etch of the sidewall filament which
9 is CVD nitride. We can't say that because it's not
10 explicit.

11 I think one would naturally believe
12 that if you have an etch tool that does the
13 anisotropic etching of the nitride sidewall filament
14 and it works, and you have the same tool available
15 in the same factory to do what is essentially a
16 similar thing with nitride on the gate structure 30,
17 that you'd probably end up using that tool and maybe
18 a little different process parameters, but it would
19 be somewhat similar. At least that would be the
20 natural inference, but it's -- it's not explicit. I
21 agree.

22 Q. And the thickness of the nitride layer

1 used to form the sidewall filaments 11 would likely
2 be thicker; correct? Thicker than nitride layer 30;
3 correct?

4 A. I don't know that it says that. I
5 don't know if it would be or not.

6 Q. It could be?

7 A. It could be, sure.

8 Q. Okay. Let's look at your reply
9 declaration again. This is Exhibit No. 3. In this,
10 I'll direct you to paragraph 4A.

11 And I believe this is the section where
12 you state that some of your -- the testimony that
13 was cited from your prior deposition was -- the
14 characterization of that testimony was improper and
15 misleading; correct?

16 A. Yes.

17 Q. All right. If you could look at
18 Exhibit 1, which is Volume 1 of your first
19 deposition, and then let me direct you to page 194
20 line 20. Let's start there.

21 So my question at that time was:

22 "So you're saying then at the point of

1 the BPSG formation, the nitride layer 30 covering
2 the sidewalls of the gate electrode structure is
3 performing spacer function?"

4 And then you answered: "Yeah, and
5 diffusion barrier function. It's not highlighted
6 here because it's probably not as big a problem, but
7 I noticed that a lot of attention is given to the
8 diffusion barrier function of the nitride material
9 with regard to the source region."

10 I say: "Okay."

11 You say: "It's just a comment."

12 Then moving down to page 195 line 19, I
13 ask you:

14 "FIG. 3. Let's look at FIG. 3D. All
15 right? This is the figure before the contact
16 openings are etched, but you have BPSG layer 14, I
17 believe it is."

18 You say: "Uh-huh."

19 Then I ask: "Right. So looking at
20 FIG. 3D, a person of ordinary skill in the art would
21 look at the portion of nitride layer 30 covering the
22 sidewalls of the gate electrode and say that's a

1 spacer right there?"

2 And then you answer: "Well, I would
3 say it's a diffusion barrier during BPSG reflow,
4 which is an annealing step."

5 And my question was: "So it's not a
6 spacer?"

7 And you answer: "Well, a diffusion
8 barrier is a kind of spacer."

9 And then I say: "Okay. So it is a
10 spacer?"

11 And you say: "Yes."

12 You see that testimony?

13 A. Yes.

14 Q. And that testimony is accurate and
15 truthful; correct?

16 A. Well, there's a qualification which
17 follows.

18 There are numerous functions of a
19 spacer, and I was asked -- you had asked me whether
20 in FIG. 3D configuration where 30 has been deposited
21 as a nitride layer and then there's BPSG, which is
22 commonly deposited at fairly high temperatures and

1 reflow, whether the 30 is functioning as a spacer at
2 that point.

3 And my answer was yes, because it
4 serves as a diffusion barrier for the phosphorous
5 and boron and BPSG.

6 Q. And that was a spacer under your
7 definition of spacer; correct?

8 A. Under one of the functions that a
9 spacer can perform.

10 Later on, there's a spacer which is an
11 electrical spacer that's more central to this patent
12 at issue that has a different shape because it's
13 been morphed by the anisotropic etching process to
14 make a new shape. So that's a different spacer.

15 Q. So let's continue with your testimony
16 from your prior deposition.

17 So after I ask you: "Okay. So is it
18 is a spacer?"

19 And you answer: "Yes."

20 And I say: "Okay."

21 But then you say: "But that's not the
22 spacer that's at issue here. I realize that."

1 Then I say: "I don't follow you."

2 And then you say: "No. I think your
3 question was, at this stage after both etches of
4 BPSG and nitride is done, how do we know that
5 there's still a nitride sidewall spacer and that's a
6 different -- that's a different question."

7 I say: "That's a different."

8 And you say: "I may have raised an
9 irrelevant question. It was just an observation
10 because there's been so much attention in what you
11 read to the diffusion barrier properties of the
12 nitride."

13 I say: "Right."

14 And then you say: "Sorry if I got us
15 off-track."

16 Now we're at page 197.

17 A. I think at that point, I had kind of
18 jumped ahead of where your questions were.

19 Q. Now we're at page 197.

20 A. Yeah.

21 Q. Line 9.

22 And I say, my question: "No, no. I

1 just want to understand. I mean, maybe it's an
2 important point.

3 Because you're saying that during BPSG
4 formation, that portion of the nitride layer that's
5 on the sidewall is acting as a diffusion barrier in
6 the --"

7 And then you say: "Lateral."

8 Then I say: "Lateral direction."

9 And you say: "Yes."

10 I say: "Thank you."

11 And then I ask: "And I think your
12 point was, is that at that stage, that portion of
13 the nitride layer, the portion that's on the
14 sidewall of the gate is functioning as a spacer;
15 correct?"

16 And then you answer: "A diffusion
17 barrier spacer."

18 And then I ask: "And that diffusion
19 barrier spacer is within the definition of spacer
20 that you provided in the context of the '997?"

21 And you answer: "Yes."

22 Is that testimony I just read accurate?

1 A. It's accurate because the -- my
2 understanding of the definition of the word "spacer"
3 is something which spaces between things or
4 something of that order. And that's what I meant
5 when I said yes, it's consistent with the use in the
6 context of the '997.

7 The '99 -- this -- this shows in the
8 Doshi reference multiple types of spacers, but if I
9 go -- I was -- I was trying to address what the, I
10 guess, court-accepted interpretation is of the word
11 "spacer." Or agreed-upon interpretation? I
12 don't -- I don't know the difference.

13 Q. What you were saying in your testimony
14 was that the portion of nitride layer 30 that was on
15 the sidewall of the gate structure at that point in
16 the process was a spacer under the definition of
17 "spacer" in the context of the '997 patent; correct?

18 A. Yeah, my recollection is that there was
19 some determination that spacer means an element that
20 provides space between things. I'm paraphrasing
21 because I won't get the exact legal wording of it.
22 And in that sense, yes.

1 Q. Okay. Looking at paragraph 5A of your
2 declaration, and in this section you're talking
3 about whether a nitride material is removed during
4 the BPSG etch; correct?

5 A. Uh-huh. Yes.

6 Q. All right. And if you look at towards
7 the bottom of paragraph 5A, you say that:

8 "Thus, if any nitride layer is to be
9 removed during the initial oxide etch, a POSITA
10 would have understood that more nitride on the
11 diffusion region would have been removed than
12 nitride on the sidewall, the gate electrode, and
13 this would further help with the sidewall spacer
14 formation."

15 You say that; correct?

16 A. Yes.

17 Q. Okay. And I think you then cite FIG.
18 3F of Doshi; correct?

19 A. Yes.

20 Q. Let's look at FIG. 3F, and you can
21 refer to FIG. 3E as well, I think. FIG. 3E shows
22 the etch process before the BPSG etch and FIG. 3F

1 shows the etch process following the BPSG etch.

2 So during the BPSG etch of the plug
3 contact -- and I'm looking at FIG. 3F.

4 A. Yeah.

5 Q. The first part of the nitride layer 30
6 that would be exposed to etchant is at the top of
7 the gate; correct?

8 A. No. No. It would be the top of the
9 gate and the part above the diffusion region.

10 Q. You're saying that the portion of the
11 nitride exposed to etchant -- the portion -- okay.

12 What you're saying then is that during
13 the BPSG etch --

14 A. I'm sorry. During the BPSG etch.

15 Q. Right.

16 A. Excuse me. I misstated.

17 I was -- I was looking at 3F and
18 thinking about the nitride etch.

19 Q. Okay. So let me re-ask.

20 A. You're talking -- thank you.

21 Q. Let me re-ask the question.

22 During the BPSG etch --

1 A. Right.

2 Q. -- the first part of the nitride layer
3 30 that would be exposed to etchant is at the top of
4 the gate; correct?

5 A. Yes.

6 Q. Okay. And then as the BPSG etch
7 continues down, more and more of the nitride layer
8 30 would be exposed to etchant; correct?

9 A. Yes, laterally --

10 Q. Right.

11 A. -- for the most part, but yes.

12 Q. Okay.

13 A. The BPSG surface will recede downward
14 and, yes, that exposes more and more of the nitride
15 sidewall area to the environment of the etch.

16 Q. Right. And as the BP -- then the BPSG
17 continues downward until it hits the nitride over
18 diffusion -- over the diffusion region, which is the
19 flat horizontal portion of nitride layer 30;
20 correct?

21 A. Right.

22 Q. Okay. So the flat horizontal portion

1 of nitride layer 30 is only exposed to etchant for a
2 very brief period of time during the BPSG etch;
3 correct?

4 A. Well, brief meaning enough to remove
5 it.

6 Oh, I'm sorry. I'm sorry. The BPSG
7 etch. Excuse me.

8 The nitride is exposed to the BPSG etch
9 for a very brief time as the top surface of the BPSG
10 gets to the nitride top surface and then the BPSG is
11 gone.

12 Q. Right. So --

13 A. Yes.

14 Q. -- the portion of the nitride layer 30
15 over the diffusion region, that flat surface at the
16 bottom is only exposed to etchant during the BPSG
17 etch for a very brief period of time?

18 A. That's what I would expect.

19 Q. Okay. But the portion of nitride layer
20 30 at the top corner or on the sidewalls are exposed
21 to etchant for a longer period of time than the
22 portion of the nitride layer over the diffusion

1 region; correct?

2 A. They're exposed to the etchant
3 environment for a longer time, and the top portion
4 is exposed to the flux of -- of reactive ions that
5 do the etching much more than the sidewall is
6 because it's anisotropic etch.

7 Q. Okay. So you're saying more of that
8 top portion would potentially be etched than the
9 portion on the sidewall?

10 A. Yes.

11 Q. Okay. And the etching of that nitride
12 layer 30 during the BPSG etch would change the
13 contour of nitride layer 30; correct?

14 A. Well, I think minimally because it's a
15 selective etch.

16 Q. But it would have some effect?

17 A. Anything has some effect.

18 Q. But it would be fair to say that the
19 portion of nitride layer 30 near the top of the gate
20 would be etched more than portions of nitride layer
21 30 closer to the bottom of the gate just because
22 they're exposed to the etching environment for

1 longer period of time; correct?

2 A. For the BPSG etch, yes.

3 Q. Right. Okay.

4 Are BPSG and TEOS the same material?

5 A. Not quite. TEOS -- well, TEOS has two
6 different interpretations. It's a molecule. It's
7 tetraethyl orthosilicate. And usually in this field
8 when people say a TEOS layer, they mean an SiO₂
9 layer made from that molecule as one of the CVD
10 precursors.

11 BPSG is a different mixture of things
12 containing boron and phosphorous as dopants in SiO₂
13 and it's -- it's often deposited from a kind of a
14 spin -- spin-on process. I don't know if --
15 actually, I don't know if it's spin-on or not, but
16 then a high temperature annealing to turn it into --
17 to turn it into a SiO₂ lattice that has boron and
18 phosphorous impurities.

19 Q. Do they generally etch at the same
20 rates?

21 A. Well, certainly not the same rates, but
22 offhand I don't know how much different they are.

1 Q. Okay. Is it generally true that the
2 thicker the material, the longer it will take to
3 etch the material?

4 MR. COLAIANNI: Objection to form.

5 THE WITNESS: Well, in the
6 simplest case and perhaps usually, you would say the
7 etch rate is well-defined and independent of how far
8 you've etched so far. So, generally speaking,
9 that's a reasonable statement, but there are
10 exceptions that are important.

11 A good example is that in the
12 process of doing plasma etching -- plasma-based
13 etching, particularly anisotropic etching perhaps,
14 if you look at the etch rate of -- let's see, which
15 chemistry should I -- should I give?

16 If you look at the etch rate of
17 silicon in one of these fluorocarbon plasmas, an
18 early discovery in the field was that if you wanted
19 to etch oxide, silicon dioxide and stop on the
20 silicon, you etch through the oxide and I guess
21 that's a fixed rate. And when you hit the silicon,
22 you etch the silicon at some rate. But what happens

1 is, as you etch that silicon, you form a
2 fluorocarbon layer on the surface, which slows down
3 the etch.

4 So the etch products of the
5 reactive chemistry that's going on can change the
6 rate as you go through the material. So I guess
7 that's the counter-example that I give you, and
8 those things are fairly common. I mean, if you
9 think about what's the consequence of that.

10 If I can etch through oxide at a
11 reasonable rate, and then when I hit silicon after a
12 short time, it builds up this, this passivating
13 fluorocarbon layer, that makes it a selective etch
14 for oxide over silicon.

15 So the zeroth order conclusion is
16 probably yes, the rate doesn't change, but in fact
17 it's very important that in some cases it does
18 change quite dramatically because it gives rise to
19 selectivity.

20 BY MR. CHEN:

21 Q. Is all oxidation thermal oxidation?

22 A. Oxidation of what material?

1 Q. Silicon.

2 A. Of silicon? No, it's not all thermal
3 oxidation.

4 Q. Are there different forms of oxidizing
5 silicon?

6 A. Sure. You can -- you can oxidize it
7 with different gaseous reactants: O₂, H₂O, N₂O, and
8 so on.

9 Q. Right.

10 A. So that's a thermal oxidation, however,
11 with different species and then there's an anodic
12 oxidation. So you can do wet electrochemistry to
13 form what's called an anodic oxide.

14 And I guess you could call that a
15 thermal oxidation because there's no plasma
16 involved, but I doubt that it's useful for me to
17 speculate about semantics in these cases.

18 Q. What is -- how would one of ordinary
19 skill understand thermal oxidation?

20 A. Well, in the -- in the field of
21 electronics, most people would rather directly think
22 of heating the silicon, if we're talking about

1 silicon oxidizing, heating the silicon to relatively
2 high temperatures in the presence of O₂ or H₂O or
3 sometimes N₂O. These would be the most common ones.

4 Q. Okay.

5 A. And thereby causing the oxygen from the
6 gas-phase to react with the silicon to make SiO₂.
7 You could also use ozone.

8 Q. If you used ozone without heat
9 treatment, would that be considered thermal
10 oxidation?

11 A. Well, I think one could call it thermal
12 oxidation, but ozone is pretty reactive and so it
13 will happen at much lower temperatures. We use it
14 in my research group all the time.

15 The complication is that to create
16 ozone, you need something else to happen because,
17 fortunately, we're not breathing ozone when we're in
18 the air, and so you have to have a plasma or
19 ultraviolet light or something to turn O₂ into
20 ozone.

21 Q. Okay. But a person of ordinary skill
22 in the art wouldn't typically consider that type of

1 reaction to be thermal oxidation; correct?

2 A. No. If you say thermal oxidation, the
3 question that would come immediately I think is, oh,
4 you mean dry oxidation, which is O₂, wet oxidation,
5 which is O₂ and H₂O, or something else like N₂O.

6 Q. In combination with heat treatment like
7 in a furnace; correct?

8 A. Yeah. Yeah.

9 Q. Okay. What about rapid thermal
10 annealing?

11 A. Annealing?

12 Q. Or the use of a laser?

13 A. Well, I think I can infer a couple of
14 things from -- from what you're asking.

15 Q. Well, maybe I'm not using the term
16 correctly.

17 A. No, but I can explain.

18 So rapid thermal annealing is a
19 technique where you use typically flash lamps -- it
20 could be a laser, a CO₂ laser or something -- to
21 heat the silicon very fast in the presence of an
22 oxidant like O₂ and then cool it back down.

1 And the advantage is that you go to a
2 really high temperature, higher than you would in a
3 furnace probably, and you stay there for a short
4 time, and then you cool it down. So it's quick and
5 it's pretty commonly used.

6 It's called rapid thermal oxidation if
7 there's oxygen present, and the process of heating
8 and cooling in this, quote, rapid thermal way is
9 used even more broadly for rapid thermal annealing,
10 for example, to anneal the dopants that you've
11 implanted and make them active.

12 Laser is -- is more complicated if
13 you're not just using a laser to heat, and that
14 would be some kind of a photochemical oxidation
15 where the wavelength of light or the photon energy
16 of the light from the laser changes the reaction
17 sequence somehow, but, I mean, this would be only in
18 the research domain.

19 Q. But those would not be typically
20 considered thermal oxidation as one of ordinary
21 skill in the art would understand it?

22 A. You mean a photochemical oxidation?

1 Q. Right.

2 A. I think it would be such a niche
3 interest that probably nobody would know how to
4 answer the question.

5 Q. What about --

6 A. I doubt if anybody has thought about
7 it.

8 Q. Okay. What about the use of a laser to
9 very rapidly heat the surface of the wafer?

10 A. Well, rapid thermal oxidation by a
11 laser or flash lamps -- there's halogen lamps --
12 that's a thermal process. There's no plasma
13 involved. There's no electrochemistry involved. So
14 I would call that thermal oxidation.

15 Q. Okay. But the use of ozone to conduct
16 oxidation is not understood to be thermal oxidation;
17 correct?

18 A. Oh, I'm just saying it's something you
19 could do. I -- I don't know if many people do it.

20 Q. When a person of ordinary skill in the
21 art thinks of thermal oxidation, they would not
22 think of the use of ozone to do the oxidation;

1 correct?

2 A. No, I don't think so.

3 Q. All right. During thermal oxidation,
4 exposed silicon will oxidize faster than silicon
5 that is covered; correct?

6 A. Covered by what?

7 Q. Covered by some material.

8 A. Well, it's partly a question of
9 numbers. So, for example, if I have a silicon
10 surface and I measure the oxidation rate of that
11 silicon surface, I get a number. If I now cover it
12 by a thin oxide and I measure the oxidation rate,
13 meaning how much -- how much additional oxide did I
14 grow per unit time --

15 Q. Right.

16 A. -- I'll get the same number because
17 it's in the linear growth regime.

18 So for thin layers, the oxygen can
19 diffuse from the gas-phase to the silicon interface
20 and form new oxide, and in those cases the
21 rate-limiting step has nothing to do with the
22 thickness of the film that's there because that's

1 the fast step. The slow step is the bonds. When
2 the oxygen gets to the silicon, it has to re-form
3 bonds.

4 Q. At what point do you emerge from the
5 linear phase?

6 A. So that depends on temperature and --
7 let's see. Temperature. Assuming you're working at
8 an atmosphere of oxygen, it's something like a tenth
9 micron or something like that. I mean, it depends
10 on the temperature, of course.

11 What's happening is that when you grow
12 the initial oxide, the first layer or the tenth
13 layer or whatever, the oxide is so thin that the
14 oxygen comes, it absorbs, it diffuses through the
15 film, it finds the silicon surface, and it makes new
16 oxide and so that's a linear regime.

17 And because the slow step is the
18 interfacial reaction and as that grows, eventually
19 you get thick enough that now the slow step becomes
20 the diffusion through the oxide, and that's called
21 the parabolic regime and so this is kind of very
22 standard textbook stuff.

1 And I think for most typical oxidation
2 temperatures, it's going to be something like a
3 tenth micron. So that would be a thousand
4 angstroms, maybe more.

5 Q. How does temperature affect what is the
6 rate limiting step?

7 A. Yeah, I wish I had my textbook with me.
8 There's a plot of one over temperature and a log of
9 the rate and in the regime -- in the linear regime,
10 there is an activation energy which tells how
11 effective temperature change is in changing its
12 rate.

13 And for the parabolic part, when it
14 gets thicker and now the growth slows down, you're
15 then rate limited by diffusion of the oxygen in the
16 existing oxide and that has a different activation
17 energy, therefore, a different temperature
18 dependence, but I don't remember which one crosses
19 which one when.

20 Q. When you have higher temperature, the
21 oxygen will diffuse more quickly; correct?

22 A. Yeah.

1 Q. Okay.

2 A. Higher temperature will increase both
3 rates.

4 Q. The reaction rate as well as the
5 diffusion rate?

6 A. Yeah, if you want to call it that.
7 Yeah.

8 Q. Let's turn back to Doshi.

9 Having looked at Doshi a number of
10 times by now, do you have an opinion as to whether
11 the diffusion regions or source/drain regions, as
12 they're described in Doshi, are covered by a gate
13 oxide during the formation of the sidewall
14 filaments?

15 A. Let me -- let me go to the description
16 of the sidewall filament formation. That was --
17 (reviewing document). Yeah, it's very hard to
18 determine this for perhaps a couple of reasons.

19 So according to the preferred
20 embodiment, if that's the one to look at, sidewall
21 filaments are first formed by oxidizing the sides of
22 the polysilicon and then depositing conformal

1 silicon nitride and then anisotropic etching to
2 remove the nitride from flat surfaces which would
3 include diffusion region.

4 So during the thermal oxidation that
5 happens first of the sidewall of the polysilicon
6 gate structure, the diffusion region is -- is
7 exposed and so I would expect some oxidation to take
8 place then. But then it's followed by a CVD nitride
9 layer which is then etched from the diffusion
10 region.

11 So to have an opinion, I'd have to be
12 making a guess or having some knowledge of how that
13 etch is done.

14 Q. So you're saying that dermal -- during
15 the formation of the sidewall filaments 11, the
16 diffusion region is exposed to silicon?

17 A. During the oxidizing of the polysilicon
18 layer, what's happened before then is that the gate
19 structure is formed by etching. That would clear
20 the surface of the diffusion regions, presumably if
21 they cleaned up the residue, any RIE residue
22 correctly, and then the next step is to oxidize the

1 polysilicon. So what you -- I'm sorry. The next
2 step is the -- is the implantation which will cause
3 some damage and so on, and maybe the implanter isn't
4 as clean as it should be. So you might get some
5 oxidation then.

6 And after that, the CVD is put down and
7 then it's etched away. And I would guess that if
8 you wanted to overetch that, then you'd have exposed
9 silicon at the end.

10 Q. Okay.

11 A. And then you put the CVD stop layer
12 down.

13 Q. Is it your opinion that at the stage
14 where Doshi says "Sidewall filaments 11 are formed
15 by first oxidizing the sides of polysilicon layer
16 22" that the diffusion regions or source/drain
17 regions are exposed to silicon?

18 A. Assuming that in the reactive-ion
19 etching process, the anisotropic etching formed the
20 sidewall filaments has been done right -- I'm -- I'm
21 sorry.

22 Assuming that the etching to define the

1 gate didn't cover the silicon surface with residues
2 or the process was -- let me say it again.

3 You etch the gate structure. Typically
4 there's a certain amount of residue after etching
5 that could be on the silicon. So assuming that that
6 was cleaned up, which you can do as the end of the
7 etch step in different ways -- actually sometimes
8 you do it with oxygen to burn off carbon residues.

9 Okay. Let's assume an ideal case.

10 Q. Okay.

11 A. I'm sorry. I think -- I think I know
12 too many details for making this a simple question.

13 You etch the gate structure and let's
14 assume conditions are ideal and there's nothing
15 covering the diffusion region silicon. You implant
16 and, hopefully, you don't put a layer on top of that
17 then, and then you grow the sidewall oxidation of
18 the polysilicon. You would also grow some oxide on
19 the diffusion region.

20 Then you put the CVD nitride over the
21 whole structure, do an anisotropic etch, and when
22 you etch it away, the question is: If there was an

1 oxide underneath the nitride, do you etch that, too?

2 And I don't know the answer to that.

3 I'm sorry. I gave you much more than
4 you wanted.

5 Q. That's okay.

6 I want to focus only on that specific
7 step where the sides of polysilicon layer 22 are
8 oxidized, just right at that stage and in the --

9 A. You're looking at 3 what?

10 Q. I'm looking at column 7 line --

11 A. Okay. Okay. But, I mean, to visualize
12 it, it would be you're talking about structure 11?

13 Q. Structure 11 --

14 A. Right.

15 Q. -- is the sidewall filament, yes.

16 A. Right.

17 Q. Correct.

18 And in column 11 at line 57, it says:

19 "According to the preferred embodiment
20 of the invention, sidewall filaments 11 are formed
21 by first oxidizing the sides of the polysilicon
22 layer 22."

1 Correct?

2 A. Uh-huh. Yes.

3 Q. And it is your argument and Samsung's
4 argument that during that oxidizing step, the
5 diffusion region is exposed to silicon and therefore
6 would also be oxidized during that step; correct?

7 A. Right. If you're doing things right,
8 that's what would happen.

9 Q. Okay.

10 A. Meaning you know how to clean up the
11 RIE residue and stuff like that.

12 Q. And I just wanted to confirm that your
13 opinion was, was that in an ideal case, assuming
14 that you didn't have leftover residue from the
15 previous oxidation --

16 A. That oxidation, yeah.

17 Q. -- that the diffusion region is exposed
18 to silicon at the time that that polysilicon layer
19 22, the sides of that polysilicon layer 22 are being
20 oxidized?

21 A. Right.

22 Q. In the description here in Doshi where

1 it's talking about this oxidizing step, Doshi
2 doesn't actually say that the diffusion region or
3 the source/drain regions are oxidized; correct?

4 A. I think that's correct.

5 Q. Doshi also doesn't say that the gate
6 oxide layer over the diffusion region or
7 source/drain regions is thickened; correct?

8 A. Well, the question is whether the gate
9 oxide has been etched away over the diffusion region
10 or not. The part that's underneath the FET gate is
11 not exposed to oxygen, so it shouldn't thicken.

12 Q. Doshi doesn't say any oxide layer is
13 being thickened during this step; correct?

14 A. No, Doshi doesn't address what's going
15 on at the surface of the diffusion region at all.

16 Q. All right.

17 A. So we're left to infer from what we
18 know in the art what's likely to happen.

19 Q. And when Doshi discusses the oxidation
20 of the polysilicon layer 22, it just says that the
21 sides of that layer are oxidized; correct?

22 A. Yes, that's what he says.

1 Q. It doesn't say thermal oxidation;
2 correct?

3 A. (Reviewing document). No, it doesn't
4 say the word "thermal."

5 MR. CHEN: I want to take a break.
6 I'm going to check my notes, and then maybe we can
7 move on to the next one.

8 MR. COLAIANNI: Okay.

9 THE VIDEOGRAPHER: Okay. We're
10 going off the record. The time is 14:14.

11 (Recess - 2:14 p.m. - 2:41 p.m.)

12 THE VIDEOGRAPHER: We are back on
13 the record. The time is 14:41.

14 BY MR. CHEN:

15 Q. Looking back at Doshi, which is Exhibit
16 5, and my question is regarding the etch, the
17 nitride etch that's used to etch nitride layer 30 in
18 the plug contacts and bit-line contacts.

19 The etch of that nitride layer is
20 selective to silicon; correct?

21 A. Let me find it here just to make sure.
22 (Reviewing document).

1 Well, the description that I find
2 earliest is in column 9 describing CHF₃ and CO as a
3 timed etch. So I don't see that it says it's
4 selective, and I don't recall anything earlier than
5 that having said that.

6 Am I missing something?

7 Q. Do you have an opinion as to whether
8 that nitride etch is or is not selective to silicon?

9 A. So we had a discussion about the
10 Einspruch reference and the table which said that
11 CHF₃ can be anisotropic and it also said it can be
12 high selectivity compared to silicon.

13 So I would assume it's going to be
14 selective, but if it's a very thin layer nitride,
15 which it's fairly thin, selectivity may not be the
16 dominant quality necessary where there's a timed
17 etch.

18 But my -- my presumption is that that
19 chemistry will be selective. Usually you pick a
20 selective chemistry if you have it available.

21 Q. Assuming that the nitride etch is
22 selective to silicon, if you did have some amount of

1 overetch, you would not really damage the silicon
2 surface below; correct?

3 A. Well, if you're going to remove all of
4 the nitride, then you have to etch into the silicon
5 a little bit. Now, I wouldn't call that damage.
6 Unless the -- well, unless the ion energy is too
7 high, which it can be in these cases.

8 So, I mean, some of these etch
9 chemistries I know can involve quite deep
10 penetration of hydrogen atoms from the plasma. So,
11 you know, it's conceivable there would be some
12 damage. Hopefully not.

13 Q. With a selective nitride etch, the
14 intention is for the etching to stop on the silicon
15 surface; correct?

16 A. Yes.

17 Q. So that even if you designed in a
18 degree of overetch to make sure you cleared all the
19 nitride material from the contact, you would not
20 materially damage the silicon surface; correct?

21 A. That's certainly the goal.

22 Q. Okay. Turning to Doshi column 7, and

1 this is where Doshi is describing the formation of
2 the gate structure. I'd like to direct your
3 attention to column 7 line beginning at line 39,
4 where Doshi says that:

5 "Also in this example, gate structures
6 10 are formed as layered structures, including
7 polysilicon layer 22 in contact with gate oxide 8,
8 tungsten silicide layer 24 overlying polysilicon
9 layer 22, and silicon nitride layer 26 overlying
10 tungsten silicide layer 24."

11 You see that?

12 A. Yes.

13 Q. And that describes the various layers
14 within the gate stack; correct?

15 A. Yes.

16 Q. Okay. Then it says:

17 Each of polysilicon layer 22, tungs
18 silicide layer 24, and silicon nitride layer 26 are
19 deposited by way of CVD, and are then etched to the
20 desired pattern preferably, by first defining a
21 pattern using conventional photolithography to
22 protect nitride layer 26 at the gate structure

1 locations, and then etching nitride layer 26."

2 You see that?

3 A. Yes.

4 Q. Okay. And that is describing the step
5 where the gate stack is formed by etching the
6 various layers that were described above; right?

7 A. Yes.

8 Q. Okay. And then it goes on to say:

9 "The remaining portions of nitride
10 layer 26 serve as a hard mask during the etching of
11 tungsten silicide layer 24 and polysilicon layer
12 22."

13 Correct?

14 A. Yes.

15 Q. In this description of the formation of
16 the gate stack, Doshi does not state that gate oxide
17 8 is etched; correct?

18 A. You mean next to the gate structure?

19 Q. Correct.

20 A. He -- he does not state that. That is
21 right.

22 Q. And then Doshi goes on to then describe

1 the process of doing implantation and forming the
2 sidewall filaments 11; correct?

3 A. Yes.

4 Q. And then following the formation of
5 sidewall filaments 11, Doshi describes the
6 implantation and annealing that are used to form the
7 source/drain region, and this is at the bottom of
8 column 7 and the top of column 8; correct?

9 A. Yes.

10 Q. Okay. And then Doshi states at column
11 8 line 3:

12 "Following the formation of
13 source/drain regions 6, 7, gate oxide layer 8 is
14 removed overall, except from under gate structures
15 10."

16 A. Yes.

17 Q. You see that?

18 A. Yes.

19 Q. So what Doshi shows is that during the
20 formation of the sidewall filaments, the
21 source/drain regions or the diffusion regions are
22 still covered by gate oxide layer 8; correct?

1 A. Yes. I had -- I had forgotten that.

2 MR. CHEN: Okay. All right.

3 That's all my questions. I turn the witness over to
4 you.

5 MR. COLAIANNI: Okay. Let me just
6 take a few minute break to just collect my notes and
7 be right back.

8 MR. CHEN: Sure.

9 THE VIDEOGRAPHER: Going off the
10 record. The time is 14:50.

11 (Recess - 2:50 p.m. - 3:04 p.m.)

12 THE VIDEOGRAPHER: We're back on
13 the record. The time is 15:04.

14 REDIRECT EXAMINATION

15 BY MR. COLAIANNI:

16 Q. Good afternoon, Dr. Rubloff.

17 A. Good afternoon.

18 Q. I just have a few questions for you
19 based on your cross-examination testimony.

20 Can I refer you to paragraph 6B of your
21 declaration, which was marked as Exhibit 3?

22 A. Yeah.

1 Q. In paragraph 6B, you state:

2 "Thus, a person of ordinary skill in
3 the art would have understood that a thicker oxide
4 layer would be formed over the diffusion region
5 during thermal oxidation of the polysilicon gate
6 sidewalls."

7 Do you see that sentence?

8 A. Yes.

9 Q. Is it your opinion that Doshi discloses
10 thermal oxidation of the polysilicon gate sidewalls
11 and the diffusion region?

12 A. Yes. Yes. We just went through that,
13 actually.

14 Q. Could you explain the basis for that
15 opinion?

16 A. Well, it was -- I have to find it now.
17 (Reviewing document).

18 So let's see. This would be in column
19 -- this is Doshi. Let's say column 7 line 59. It
20 talks about sidewall filaments being formed by
21 oxidizing the sides of the polysilicon layer 22. A
22 layer of silicon nitride is deposited and so on. It

1 goes on about that.

2 And then right at the bottom of the
3 page "Following formation of sidewall filaments" --
4 up on the top of 8, it says.

5 "Following the formation of
6 source/drain regions, gate oxide layer 8 is removed
7 overall, except from under gate structures 10."

8 So what that means is there had been a
9 gate oxide every place. Then the gate structures
10 were formed, and up until this point we didn't know
11 if the formation of the gate structures involving
12 etching down through that stack had also removed the
13 gate oxide.

14 But here it says:

15 "Following the formation of
16 source/drain regions... gate oxide layer 8 is
17 removed overall."

18 So that tells me it was not etched off
19 when the FET gate is formed.

20 Q. And that's --

21 A. And you will remember, I was asked the
22 question whether the gate oxide was there or did

1 Doshi say it was etched, and Doshi didn't say it was
2 etched. And then this -- this sentence says that
3 no, it wasn't etched because we're taking it off now
4 because it was still there.

5 Q. And the portions of the Doshi reference
6 you just referenced supports your opinion that the
7 gate sidewalls and diffusion region are thermally
8 oxidized; correct?

9 A. Yes, that's right. That that --
10 (reviewing document).

11 Well, it doesn't matter how you count.
12 There's oxide there and that's what's removed in
13 column 8, where it says "gate oxide layer 8 is
14 removed overall."

15 The -- what would have happened here,
16 since the sentence in column 8 tells us that when
17 the gate is etched to define the gate structure, it
18 did not etch the gate oxide that was there. Then
19 the polysilicon oxidation is taking place on the
20 sidewall, and that will further grow oxide over the
21 diffusion region. And so all of that oxide would
22 then be removed where it says:

1 "Gate oxide layer 8 is removed overall,
2 except for under -- from under gate structures 10."

3 Does that answer the question?

4 MR. COLAIANNI: It does. Thank
5 you.

6 I don't have any further
7 questions.

8 THE VIDEOGRAPHER: Okay. We're
9 going off the record. The time is 15:09.

10 (Recess - 3:09 p.m. -

11 (Mr. Hsieh no longer present.)

12 (David Holt present.)

13 THE VIDEOGRAPHER: Here begins
14 disk 1 of the video deposition of Gary Rubloff taken
15 in the matter of Samsung Electronics Corporation
16 Limited, et al. v. Home Semiconductor Corporation,
17 before the Patent Trial and Appeal Board, patent
18 case number IPR 2015-00459.

19 Today's date is December 16, 2015.
20 The time on the video monitor is 15:15. This
21 deposition is being held at 1425 K Street,
22 Northwest, Washington, DC 20005.

1 The court reporter is Denise
2 Vickery on behalf of Esquire. The video camera
3 operator is Patrick Graham on behalf of Esquire.

4 Will counsel and others please
5 introduce themselves and state whom they represent,
6 beginning with the party noticing the deposition.

7 MR. CHEN: Okay. My name is Jerry
8 Chen from TechKnowledge Law Group representing Home
9 Semiconductor Corporation.

10 MR. COLAIANNI: Joseph Colaianni
11 of Fish & Richardson representing the Samsung
12 Petitioners.

13 MR. HOLT: David Holt also from
14 Fish & Richardson representing Samsung Petitioners.

15 THE VIDEOGRAPHER: Will the court
16 reporter please swear in the witness.

17 - - -

18 GARY W. RUBLOFF, PH.D.
19 called for examination, and, after having been duly
20 sworn, was examined and testified as follows:

21 CROSS-EXAMINATION

22 BY MR. CHEN:

1 Q. Dr. Rubloff, I know we've talked about
2 this before earlier, but since we've done a new
3 read-in, I just want to quickly go over the basic
4 ground rules again.

5 So on the cross-examination, I'm going
6 to be asking you regarding material related to the
7 reply declaration that you submitted in connection
8 with the Samsung IPR No. IPR 2015-00459.

9 I'm going to ask you questions related
10 to the subject matter which is discussed in your
11 reply declaration. You'll need to answer my
12 questions truthfully, completely, and the court
13 reporter will record my questions and your answers
14 in writing.

15 As explained, if your attorney objects,
16 you must still answer all my questions.

17 You understand?

18 A. Yes.

19 Q. And if you do not hear or understand my
20 questions, please ask me to repeat or clarify. If
21 you answer my questions, my assumption will be that
22 you understood the questions. Right?

1 A. Yes.

2 Q. Okay. And, of course, if you need a
3 break, please let me know and we'll take one.

4 A. Yes.

5 Q. And can you think of any reason that
6 might affect your ability to provide truthful and
7 complete answers to my questions?

8 A. No.

9 Q. Okay.

10 A. Unless I don't know the answer.

11 Q. Okay. And, Dr. Rubloff, you recall
12 that you were deposed earlier regarding a
13 declaration that you had submitted in connection
14 with the IPR 459; correct?

15 A. Yes.

16 Q. Okay. And in that prior deposition, I
17 had asked you to let me know whether you didn't -- I
18 had asked you to let me know if you didn't
19 understand any of my questions; correct?

20 A. Yes.

21 Q. And I told you that if you did not
22 understand my questions, you could ask me to repeat

1 or clarify; correct?

2 A. Yes.

3 Q. And I told that if you answered my
4 questions, my assumptions would be that you
5 understood my questions; correct?

6 A. That's what you said.

7 Q. And barring circumstances where you ask
8 me to repeat or clarify a question, you under --
9 repeat or clarify a question, you understood my
10 questions in that prior deposition; correct?

11 A. Yes, subject to the caveat that I said
12 in the previous exercise like this.

13 Q. And you were being truthful in that
14 prior deposition; correct?

15 A. Yes.

16 Q. And you gave complete answers to my
17 questions?

18 A. The best that I could at the time.

19 Q. And you stand by the answers you
20 provided in that prior deposition; correct?

21 A. Yes, in the context of clarifications
22 that are included in my reply declaration.

1 MR. CHEN: Okay. Are we on 6?

2 THE REPORTER: Yes.

3 (Document marked, for
4 identification purposes, as Rubloff Exhibit No. 6.)

5 BY MR. CHEN:

6 Q. Dr. Rubloff, I've asked the court
7 reporter to mark as Exhibit No. 6 the reply
8 declaration that you submitted in connection with
9 the IPR 459.

10 Is that now in front of you?

11 A. Yes.

12 Q. Okay. And this is your reply
13 declaration; correct?

14 A. Yes.

15 Q. Okay. And you drafted this
16 declaration?

17 A. Yes.

18 Q. Are you aware of any errors in this
19 declaration?

20 A. No.

21 Q. And there are no corrections you would
22 currently like to make to this declaration; correct?

1 A. No.

2 Q. How did you arrive at the opinions
3 included in this declaration?

4 A. I read the deposition testimony of
5 Mr. Maltiel. I considered what was said there. I
6 considered the documents which I used to arrive at
7 my first declaration. I had discussions with my
8 attorneys about some of these issues.

9 Let's see. What am I missing?

10 I thought about them, the various
11 documents relevant -- relevant to this, and I
12 thought about what I know about the state of the art
13 at the time and what one of ordinary skill would --
14 would be thinking, would interpret, would know what
15 to do or not to do.

16 I think that's it.

17 Q. Okay. And you arrived at the
18 conclusions in this declaration based on your own
19 analysis; correct?

20 A. Yes.

21 MR. CHEN: Okay. This is 7.

22 (Document marked, for

1 identification purposes, as Rubloff Exhibit No. 7.)

2 BY MR. CHEN:

3 Q. Dr. Rubloff, I've asked the court
4 reporter to mark as Exhibit No. 7 Patent No. US
5 6,312,994, which is the Nakamura reference.

6 This is the reference that you relied
7 on to support your opinions in connection with the
8 Samsung IPR 459?

9 A. Yes.

10 Q. Now, I'd like to direct your attention
11 to column 11 and column 12 of the Nakamura
12 reference, which is Exhibit No. 7.

13 At column 11 beginning at line 28, you
14 see it says "A Second Embodiment."

15 You see that?

16 A. Yes.

17 Q. What follows then is a description of
18 the Nakamura second embodiment and it continues from
19 column 11 line 28 through column 12 line 57;
20 correct?

21 A. Yes.

22 Q. All right. And then you see there at

1 column 11 beginning at line 30, it says:

2 "A method for fabricating a
3 semiconductor device according to a second
4 embodiment of the present invention will be
5 explained with reference to FIGS. 3A-3B and 4A-4D."

6 You see that?

7 A. Uh-huh.

8 Q. So Nakamura is using those figures to
9 describe the second embodiment; correct?

10 A. Yes.

11 Q. All right. And then following that
12 beginning at line 36, Nakamura says:

13 "FIGS. 3A and 3B are views which
14 explain the disadvantage of the method for
15 fabricating a semiconductor device according to the
16 first embodiment."

17 You see that?

18 A. Yes.

19 Q. Okay. So FIGS. 3A and 3B show the
20 problems with the first embodiment when disalignment
21 occurs; correct?

22 A. That's right.

1 Q. All right. So in Nakamura at column 11
2 beginning at line 49, it says:

3 "However, in a case that disalignment
4 takes place in the lithography step of opening the
5 contact holes 34, 36, and the patterned inter-layer
6 insulation film 26 is extended over the regions to
7 be the source/drain diffused layer 38, 40 (FIG. 3A),
8 the low-concentration diffused region of LDD may be
9 elongated with a result of higher parasitic
10 resistance (FIG. 3B)."

11 A. Yes.

12 Q. You see that?

13 So there it's describing the problem of
14 disalignment which could occur, and it's referencing
15 that with FIGS. 3A and 3B; correct?

16 A. Correct.

17 Q. All right. And then it says:

18 "Consequently, a margin for
19 disalignment in the lithography step for opening the
20 contact holes must be small, which makes the
21 patterning for the contact holes difficult."

22 Correct?

1 A. Yeah, I'm sorry. What line is this?

2 Q. This is column 11 line 56, beginning at
3 line 56.

4 A. Yes, I see that.

5 Q. So in the section that we just talked
6 about, Nakamura is talking about a problem that
7 could occur in the process of the first embodiment;
8 right? This disalignment problem?

9 A. Yes.

10 Q. All right. And then it goes on to
11 suggest a possible solution to this problem that
12 they just described; correct?

13 A. Yes.

14 Q. All right. It says beginning at line
15 59 of column 11:

16 "On the other hand, to ensure a
17 disalignment margin it is necessary to extend the
18 contact holes 34, 36 sufficiently over the gate
19 electrodes 18."

20 Right? Do you see that?

21 A. Uh-huh.

22 Q. So that's what they suggest as a

1 potential fix for the disalignment problem; right?

2 A. Yes.

3 Q. But then it says beginning at line 61:

4 "But this makes a width of the
5 inter-layer insulation film 26 remaining on the gate
6 electrodes 18 extremely narrow, which makes the
7 patterning of the contact holes 34, 36 difficult."

8 You see that?

9 A. Yes.

10 Q. Okay. And so what it's saying there is
11 that you could try to solve the disalignment with by
12 extending the contact holes, but that this would
13 create its own problems because the insulation film
14 26 on the gate electrodes would become extremely
15 narrow and the patterning of the contact holes would
16 become difficult; correct?

17 A. Yes.

18 Q. And you don't want the patterning of
19 the contact holes to become difficult; correct?

20 A. Right. You don't want any patterning
21 to become difficult.

22 Q. Right. In the sections that we just

1 described, does Nakamura -- Nakamura refers to FIGS.
2 3A and 3B; correct?

3 A. Yeah. Well, up earlier it says 4A to
4 4D but doesn't explain it yet.

5 Q. Right. Right. Okay.

6 Nakamura does not refer to FIGS. 2A or
7 2B; correct?

8 A. No, not explicitly, but it does refer
9 to first embodiment --

10 Q. Right.

11 A. -- which is realized in 2A, 2B.

12 Q. Right. But when describing this
13 disalignment problem or this ineffective solution to
14 the disalignment problem, it does not refer to FIG.
15 2A or 2B; correct?

16 A. (Reviewing document). Well, implicitly
17 in -- in column 11 line, say, 42, 43, it says in the
18 method for fabricating a device "according to the
19 first embodiment."

20 And previously first embodiment really
21 refers to FIG. 2 or 1 and 2. 1 and 2.

22 Q. In the section describing the second

1 embodiment, including the section that we just went
2 over, Nakamura never once references FIG. 2A or 2B;
3 correct?

4 MR. COLAIANNI: Objection. Asked
5 and answered.

6 THE WITNESS: Yeah, I think I -- I
7 think I did answer that.

8 It doesn't use FIG. 2A, 2B
9 explicitly, but it says "first embodiment" and that
10 is 2A, 2B. It's good enough for me.

11 BY MR. CHEN:

12 Q. In the section in the paragraph
13 beginning at column 11 line 59 through line 64,
14 Nakamura does not cite or refer to FIG. 2A or 2B;
15 correct?

16 A. Well, that's true. It doesn't -- it
17 doesn't say it explicitly, but just before that it's
18 introduced the discussion involving the first
19 embodiment. That's two paragraphs earlier, and then
20 the numbering systems are here.

21 And I think one of ordinary skill in
22 the art would understand, by reading the description

1 of FIGS. 1 and 2, what's being talked about here.
2 What's being talked about is as, for example, in 3B
3 where the insulating film over the gate electrode
4 has basically slid off the gate structure and now
5 causes problems in regard to the greater width of
6 the lightly doped drain, for example.

7 So I think it's people that are of
8 ordinary skill in this technology understand what's
9 being talked about here.

10 Q. Following the section that we just
11 discussed, Nakamura goes on to describe what is
12 effectively their second embodiment; correct?

13 A. Yes.

14 Q. All right. And that embodiment is
15 designed to address some of the problems cited
16 regarding the first embodiment; correct?

17 A. That's correct.

18 Q. But the second embodiment also has its
19 own issues or problems; correct?

20 A. Yeah, they all have something.

21 Q. All right. Beginning at column 12 line
22 59, Nakamura starts to describe its third

1 embodiment; correct?

2 A. Yes.

3 Q. And the third embodiment describes a
4 way to address the depth of focus issues that might
5 be associated with embodiments 1 and 2; correct?

6 A. Well, embodiment 2.

7 Q. Or just 2. Okay.

8 A. Yeah.

9 Q. The depth of focus issues associated
10 with embodiment 2?

11 A. Yes.

12 Q. Okay. Embodiment 3 addresses the depth
13 of focus problem by modifying the process during the
14 contact etch; correct?

15 A. Well, which process are you talking
16 about? And which contact etch? Can we be more
17 specific?

18 Q. Well, I think there's only one contact
19 etch for each of the embodiments; correct? Or one
20 series of processes or steps that are used to form
21 the contact hole; correct?

22 A. You mean etching of layers 26 and 24?

1 Q. Yes.

2 A. So -- so your question was that the
3 third embodiment what?

4 Q. The third embodiment tries to address
5 the depth of focus issue by proposing a different
6 way of performing the contact etch; correct?

7 A. I'm not sure that it's a different way
8 of. In what sense would you suggest that it's a
9 different way of doing the contact etch?

10 Q. In embodiment 3, during the contact
11 etch process, the photoresist is removed in the
12 middle of the contact etch; is that correct?

13 A. Right. So, but the etch process is
14 similar; right? I mean, the sequence of steps or
15 substeps is changed. That's true.

16 Q. Is the etch chemistry of one of the
17 etches also changed?

18 A. I'd have to look and see. I just don't
19 remember. And the materials are the same, except
20 for the mask. So I wouldn't think that it's
21 changed, but I'd have to look carefully to be sure.

22 Q. Okay. In embodiment 3, beginning at

1 line column 13 line 39, that's when they're starting
2 to describe the contact --

3 A. Uh-huh.

4 Q. -- etch process --

5 A. Yes.

6 Q. -- correct?

7 A. Yes.

8 Q. Okay. And in embodiment 3, the first
9 step of the process is to have the pattern
10 photoresist; correct?

11 A. Yes.

12 Q. And then the next step is to conduct an
13 anisotropic etch with the photoresist of inter-layer
14 insulation film 26; right?

15 A. Yes.

16 Q. Okay. And then the next step disclosed
17 in embodiment 3 is that the photoresist is removed?

18 A. Yes, that's line 47. Uh-huh.

19 Q. Right, of column 13.

20 And then after the photoresist is
21 removed, Nakamura says that the anisotropic etching
22 is then conducted under conditions which permit the

1 inter-layer insulation film 26 and the etch stopper
2 film 24 to be etched at substantially the same
3 etching rate.

4 You see that?

5 A. Yes.

6 Q. Okay.

7 A. So the question is whether that's
8 different from the first embodiment or the second
9 embodiment?

10 Q. Well, I'll get to that but --

11 A. Okay.

12 Q. -- that process of removing the
13 photoresist and then context -- conducting the next
14 portion of the etch where the insulation film 26,
15 which I believe is an oxide, and the etch stopper
16 film 24, which I believe is a nitride, are etched at
17 the same rate.

18 That is done for a specific purpose in
19 embodiment 3; correct?

20 A. Yes.

21 Q. And the purpose of that is so that the
22 inter-layer insulation film 26 is etched by a film

1 thickness substantially equal to a film thickness of
2 the etch stopper film 24, and the inter-layer
3 insulation film 26 would then have a height
4 substantially equal to the height of the insulation
5 film 20 exposed on the surface; correct?

6 A. Yes.

7 Q. And so the contact holes 34, 36 can be
8 opened with the surface maintained plane; correct?

9 A. Yes. Yes.

10 Q. And --

11 A. That's one of the outcomes.

12 Q. Right. And the purpose of this process
13 is to address the depth of focus issues that were?

14 A. Well, it's certainly a motivation for
15 that. There's other things that have happened.

16 For example, the way planarization is
17 done or by etching -- etching down to the layer 24,
18 which is the nitride conformal layer. So the -- the
19 removal of 26 down to 24 is different from
20 embodiment 1.

21 Q. Right. It's also different from
22 embodiment 2; correct?

1 A. Yeah. Embodiment 2 FIG. 4 it's
2 different.

3 Q. At the bottom of column 13 at line 63
4 to 64, Nakamura says that this etch process creates
5 a result where "contact holes 34, 36 can be opened
6 with a surface maintained plane."

7 You see that?

8 A. Yes.

9 Q. Okay. So planarity is important for
10 embodiment 3 in Nakamura; correct?

11 A. Yes, it's useful.

12 Q. All right.

13 A. I think I have that in my declaration,
14 a discussion of that --

15 Q. Right.

16 A. -- as one of the metrics.

17 Q. Right. Nakamura embodiment 3 was
18 specifically trying to achieve planarity; correct?

19 A. Among other things.

20 Q. If we turn to your declaration, which
21 is Exhibit 6 --

22 A. Yeah.

1 Q. -- and refer to paragraph 6. Actually,
2 of -- sorry. Paragraph 7.

3 In paragraph 7, you said that in your
4 earlier deposition I had asked about the proposed
5 combination, and I'm assuming that you're talking
6 about the combination of Nakamura third embodiment
7 with the first embodiment.

8 You said that you noted that:

9 "Planarity is a nice benefit if you can
10 get it, but it is not essential."

11 And you cite to portions of your prior
12 deposition pages 404 line 8 to 404 -- 405 line 5.

13 You see that?

14 A. Yes.

15 Q. You say that planarity is not
16 essential; correct? That's your statement?

17 A. Yes.

18 Q. Nakamura did not say that planarity is
19 not essential when discussing the third embodiment;
20 correct?

21 A. Well, I think the thrust of what he
22 said is it's desirable.

1 Q. Right. In fact, Nakamura embodiment 3
2 was designed specifically to try to achieve
3 planarity; correct?

4 A. To achieve better planarity while still
5 keeping the advantages of what the patent is about.

6 Q. Right. Okay. In paragraphs 10 and 11
7 of your declaration, you state that a person of
8 ordinary skill in the art would be aware of other
9 ways of addressing the depth of focus problems cited
10 in Nakamura; correct?

11 A. Yes.

12 Q. You cite things like optical proximity
13 correction and phase shift masks as alternative ways
14 of addressing depth of focus; correct?

15 A. Yes.

16 Q. Neither of these methods are described
17 in Nakamura; correct?

18 A. No, I don't think they are.

19 The purpose of those statements and my
20 comment about planarity is -- how did I say it? --
21 valuable but not essential is that these things --
22 this goes along the lines of something we said

1 earlier today, but these -- these things are part
2 and parcel of the whole, which is, how do you make
3 effective technologies?

4 And so depth of field and focus in --
5 in -- in a single plane is desirable, but it's --
6 it's not the case that one metric is the only one
7 that's important. So there are always trade-offs,
8 and I think we all know this very well as do skilled
9 practitioners.

10 So when I say that, it's a question of,
11 how nonplanar is this structure? If we can -- if we
12 can make it planar for free, of course we want to do
13 that. But usually nothing comes for free, and so
14 there are consequences in manufacturing costs or
15 trade-offs with some other metric about etching or
16 deposition or something.

17 And so that's the basis in which I said
18 that, and I wanted to mention proximity correction
19 of phase shift masks because these were -- these are
20 approaches that can do, let me say, first order
21 compensation for nonplanarity. And I know it's not
22 mentioned in Nakamura, but -- but people knew about

1 these things at the time.

2 Q. You had in your prior declaration
3 proposed a modification to Nakamura embodiment 3
4 where the photoresist is not removed; correct?

5 A. Yes.

6 Q. All right. By leaving the photoresist
7 in place, inter-layer insulation film 26 would not
8 be etched when etch stop 24 is being etched;
9 correct?

10 A. 26 under the photoresist.

11 Q. Right.

12 A. Yes, that's right.

13 Q. And that modification would describe a
14 process that is different than what is taught in
15 embodiment 3; correct?

16 A. Yes, that's right.

17 Q. As a result of leaving the resist in
18 place after the contact etch, the height of
19 inter-layer insulation film 26 would be greater than
20 the height of film 20; correct?

21 A. That's right.

22 Q. And that is, again, different from the

1 goals of what Nakamura embodiment 3 was trying to
2 achieve; correct?

3 A. Yes.

4 Q. All right.

5 A. So the motivation for that, which is
6 not as good, maybe perhaps close, in terms of
7 achieving the planarity advantage is the potentially
8 huge manufacturing advantage in terms of process
9 steps and their cost.

10 And people in the field certainly know
11 that if you have multiple materials to etch and you
12 have one pattern to do it with, you can use the
13 photoresist typically all the way through those
14 layers; or you can use a hard mask by removing the
15 photoresist partway through and the material you've
16 just patterned underneath it becomes an inorganic
17 material that serves as a mask. This is done
18 commonly.

19 And so I think one would have been
20 motivated to seek this trade-off which is, if
21 instead of following precisely embodiment 3, I
22 wanted to get a big manufacturing advantage by

1 leaving the photoresist in place and I'll pay
2 something in planarity to do that, that may be a
3 deal worth taking.

4 Q. In your proposed modification to
5 embodiment 3, you would not open contact holes with
6 a surface maintained plane as described in Nakamura
7 embodiment 3; correct?

8 A. Not as planar. I mean, remember, these
9 things depend on matching etch rates for two
10 materials and that's, you know, not -- not obvious
11 that one can do it really well.

12 Q. Nakamura embodiment 3 specifically says
13 that their process would open contact holes or
14 contact holes 34 and 36 can be opened with a surface
15 maintained plane; correct? That's at column 13 --

16 A. Yes.

17 Q. -- line 63 and 64?

18 A. Yes. If you can get the etch rates to
19 match, then it would be plane.

20 Q. Right. And that objective would not be
21 achieved based on your modification to Nakamura
22 embodiment 3 where the photoresist is not removed;

1 correct?

2 A. Yes, but the analysis that's in my
3 declaration, reply declaration indicates that
4 there's a configuration where it comes close, and it
5 depends on how thin or thick the nitride layer is
6 which acts as the stop layer. So if that's really
7 thin, then it could be close to planar and certainly
8 better than what -- what would happen from
9 embodiment 2. That's what's stated in the
10 declaration.

11 Q. If you could go to Exhibit 1. This is
12 the Volume 1 from your first deposition.

13 A. Yep.

14 Q. Okay. Sorry. Actually --

15 A. Might be 2.

16 Q. Exhibit 2.

17 A. Yeah.

18 Q. Go to Exhibit 2. This is Volume 2.

19 A. We did this on the second day, didn't
20 we?

21 Q. I don't remember the order anymore, but
22 yes, it's Exhibit 2, which is Volume 2 from your

1 first deposition.

2 Let's go to page 344 beginning at line
3 17.

4 And, actually, before we do that, let
5 me introduce another exhibit. This is 8.

6 (Document marked, for
7 identification purposes, as Rubloff Exhibit No. 8.)
8 BY MR. CHEN:

9 Q. So going to page 344 line 17 of Volume
10 2 of your first deposition, which is Exhibit No. 2,
11 I start where I ask the question:

12 "Moving down to claim 1, if you'll look
13 at the step that begins at column 6 line 53."

14 You see that?

15 A. I'm sorry. Which patent are we talking
16 about?

17 Q. We're actually looking at the second
18 volume --

19 A. Yeah, right.

20 Q. -- here?

21 A. But moving down to claim 1 --

22 Q. Right.

1 A. -- you just said. I don't know which
2 patent this is.

3 Q. We were discussing the '244 patent,
4 which is the patent --

5 A. That you just gave me.

6 Q. -- issued in the Samsung --

7 A. Yeah, okay.

8 Q. -- IPR 459.

9 A. Fine.

10 Q. Yes. Okay. So here, you see here
11 we're starting the discussion.

12 A. Oh, I see.

13 Q. And I was referring you to claim 1.

14 A. Okay.

15 Q. Right?

16 A. Yes.

17 Q. Okay. I'm going to read a portion from
18 your prior testimony beginning at column -- I mean,
19 beginning at page 344 line 17.

20 "Question: Moving down to claim 1, if
21 you will look at the step that begins at column 6
22 line 53.

1 Answer: We are on '244 now?

2 Question: Yes.

3 Answer: Column 6 line 53?

4 Question: Yes.

5 Answer: Yes.

6 Question: You see it says 'removing
7 said fourth dielectric layer other than said
8 portions masked by said second resist layer to form
9 a plurality of trenches adjacent to said gate
10 electrode structure.'

11 Do you see where it says that?

12 Answer: Yes.

13 Question: Would you agree that that
14 clause recites the specific step for 'removing said
15 fourth dielectric layer using the resist mask'?

16 Answer: Well, it uses the second
17 resist layer as a mask to etch away the fourth
18 dielectric layer.

19 Question: You see following that
20 clause, there's the phrase 'wherein portions of the
21 substrate are exposed'?

22 Yes.

1 Answer: Yes.

2 Question: What is your understanding
3 of that clause where it says 'wherein portions of
4 the substrate are exposed'?

5 Answer: Yes. That's all in my
6 disclosure in my declaration. I thought hard about
7 this question because I knew the interpretation is
8 important."

9 And then you read a portion, I believe,
10 of your previous declaration starting at paragraph
11 23 and that continues.

12 I believe you start reading from
13 paragraph 23 of your declaration to paragraph 35 of
14 your prior declaration and that continues from the
15 deposition transcript at page 345 line 20 and
16 continues all the way through page 355 line 20.

17 You see that?

18 A. Page -- I'm sorry. You said page 355?

19 Q. It's -- yes. You were reading from
20 your declaration and --

21 A. Oh, yes, you're right.

22 Q. -- you read it into the record, and

1 your recitation of your declaration continues all
2 the way beginning at 345 line 20 and it continues
3 all the way to page 355 line 20.

4 After which I ask you: "Are you
5 finished?"

6 And then you answer --

7 A. (Laugh).

8 Q. -- "I am finished reading. Did I
9 answer your question?"

10 You see that?

11 A. Yes. Yes.

12 Q. You recall that?

13 A. Yes.

14 Q. But you can see here in this testimony
15 we are specifically discussing the claims of the
16 '244 patent; correct? We're specifically discussing
17 the language of the claims of the '244 patent;
18 correct?

19 A. Yes.

20 Q. All right. All right. Now, continuing
21 on. After you finished your recitation of the
22 declaration, I ask you -- this is beginning at page

1 355 line 21.

2 I ask you: "Are you finished?"

3 You answer: "I am finished reading.

4 Did I answer your question?"

5 I say: "Not to my understanding. I

6 will repeat the question with a copy of that."

7 I don't know what that means.

8 "The answer is simply a recitation of a

9 number of pages from your declaration. You can just

10 say 'I have nothing more to say than what is in my

11 declaration' without just reading it all into the

12 record if that helps you. If you want to read it

13 all again, that is up to you."

14 So now I repeat my question.

15 So my question was: "Looking at the

16 limitation that begins with 'removing said fourth

17 dielectric layer other than said portions masked by

18 the second resist layer.'

19 Do you see that?"

20 And you answer: "Yes."

21 "Question: We agree that that clause

22 there recites a step for removing the fourth

1 dielectric layer using the resist mask; correct?

2 Answer: The clause up to the comma?

3 Question: Yes.

4 Answer: Yes."

5 Okay. So, again, there we are
6 specifically talking about the claim language;
7 correct?

8 A. Yes, that's right.

9 Q. All right. And then I ask you:

10 "My question was: Following the comma,
11 there is another phrase that says 'wherein portions
12 of the substrate are exposed.'

13 Do you see that?

14 Answer: Yes.

15 Question: My question was: What is
16 your understanding of that clause 'wherein portions
17 of the substrate are exposed'?"

18 And here you answer: "My understanding
19 of is it is a paragraph of three things are with two
20 'whereins' and at the same time this is describing
21 what happens in a single etch step using the resist
22 layer to drill through the two layers of dielectric.

1 Question: The clause 'wherein portions
2 of the substrate are exposed' is something that has
3 to occur during the step of 'removing said fourth
4 dielectric layer other than said portions masked by
5 the second resist layer'; correct?

6 Answer: Yes.

7 Question: And this next clause
8 'wherein spacers are formed on the sidewalls of the
9 gate electrode structure at the same time,' isn't it
10 something else that also has to occur during the
11 step of 'removing said fourth dielectric layer other
12 than said portions masked by second resist layer';
13 correct?

14 Answer: As in all three of those
15 things should be part of the etch step.

16 Question: The etch step where you used
17 the resist as a mask; correct?

18 Answer: Yes."

19 Okay. And in this section that we just
20 went through, we were again specifically discussing
21 the language of the claims; correct?

22 A. For the most part, except that the part

1 where I describe the single etch step using the
2 resist layer to drill two layers of dielectric, as I
3 explained in my dec -- reply declaration, I was
4 thinking in terms of the specification when I said
5 that. Because I was as tired as you of dealing with
6 the legalese that is -- that is in the claims, and I
7 wanted to get to the point that you need a -- you
8 need a mask, a lithographic mask to be able to
9 define where to remove material down to the
10 diffusion region.

11 So I would say that this is a case like
12 what I alluded to this morning, talking about this
13 specific example that, you know, it's not so -- it's
14 not so hard to understand that someone who isn't
15 dealing mainly with claim language like attorneys do
16 wants to get to a simplification of the matter to
17 understand what the goal is.

18 And the goal is to be able to pattern
19 the opening of contacts down to the diffusion region
20 in a way which is effective, essentially
21 self-aligned I would say, and allows one to then
22 accomplish a raised source/drain.

1 Q. My questions during the section that we
2 just discussed were all directed at the specific
3 language of the claims; correct?

4 A. I realize that.

5 Q. And you understood the questions that
6 were asked; correct?

7 A. Right. But the comment that I made
8 about drilling down was not a comment about the
9 claims.

10 Q. Okay.

11 A. It was an image in my head that I
12 wanted to convey, maybe incorrectly. From a legal
13 point of view it was probably inappropriate, but in
14 terms of what someone like me would be thinking is
15 the goal here. It's -- it's one embodiment that's
16 described in -- in the -- in not -- in patent of
17 what this is supposed to accomplish.

18 Q. Okay. And during your prior
19 deposition, you didn't tell me that you didn't
20 understand the questions; correct?

21 A. Yeah, I'm not a lawyer.

22 Q. And you didn't say that you were

1 discussing your interpretation of a preferred
2 embodiment; correct?

3 A. No, I gave an off-the-cuff description
4 of what I thought was kind of one example of how
5 this task should be accomplished.

6 Q. Okay. Now, the portion where you gave
7 the answer about drilling down, using the resist
8 layer to drill through two layers of dielectric,
9 that is at page 357 lines -- your answer is lines 2
10 through 6; right?

11 A. Uh-huh.

12 Q. And then I follow that with the
13 question and this is, again, referring specifically
14 to the language of the claims.

15 I asked you:

16 "Question: The clause 'wherein
17 portions of the substrate are exposed' is something
18 that has to occur during the step of 'removing said
19 fourth dielectric layer other than said portions
20 masked by said second resist layer'; correct?"

21 And you answered: "Yes."

22 You understood then at that time that

1 we were asking about the specific language of the
2 claims; correct?

3 A. I -- yes.

4 Q. And your answer was your understanding
5 of what the language of the claims meant; correct?

6 A. Yes, they should be -- all those three
7 things should be part of, but not all of, the etch
8 step.

9 Q. Okay.

10 A. And that can't be the case because
11 you've got a third layer that has to be removed as
12 well --

13 Q. Okay.

14 A. -- and that's not stated in the claim.

15 Q. And then the next -- I follow that with
16 the next question:

17 "And the next clause 'wherein spacers
18 are formed on the sidewalls of the gate electrode
19 structure at the same time --"

20 A. I'm sorry, I've lost you.

21 Q. Sorry. I'm at --

22 A. Which page are you?

1 Q. -- page 357 of the transcript line 13.

2 A. Okay.

3 Q. I ask another question:

4 "And this next clause" -- again

5 referring to the specific language of the claim --

6 "'wherein spacers are formed on the sidewalls of the
7 gate electrode structure at the same time," isn't it

8 something else that also has to occur during the

9 step of 'removing said fourth dielectric layer other

10 than said portions masked by said second resist

11 layer'; correct?"

12 And you answer: "As in all three of
13 those things should be part of the etch step."

14 And then I question -- and then

15 question: "The etch step where you use the resist
16 as a mask; correct?"

17 Answer: Yes."

18 Again, during this series of questions

19 and answers, you understood that we were

20 specifically asking -- talking about the language of
21 the claim; correct?

22 A. Yes. You're reading from the claim.

1 Q. Right.

2 A. Yeah.

3 Q. And your answers were your
4 understanding of what the language of the claim
5 meant; correct?

6 A. Yes.

7 MR. CHEN: Okay. Can we take a
8 quick break?

9 MR. COLAIANNI: Sure.

10 THE VIDEOGRAPHER: Going off the
11 record. The time is 16:13.

12 (Recess - 4:13 p.m. - 4:30 p.m.)

13 THE VIDEOGRAPHER: We are back on
14 the record. The time is 16:30.

15 BY MR. CHEN:

16 Q. Dr. Rubloff, I'd like to direct your
17 attention back to your declaration, your reply
18 declaration, which is Exhibit No. 6, and I want to
19 discuss the portion where you discuss depth of focus
20 and this is from paragraph 14 through -- through 19.

21 And I think this is where you discuss
22 how your modified methodology of the third

1 embodiment would still have a depth of -- depth of
2 focus that is better than the second embodiment;
3 right?

4 A. Okay.

5 Q. All right. If we look at the bottom of
6 paragraph 19 where you kind of -- or we're looking
7 at paragraph 19 where you kind of -- I think this is
8 your -- your conclusion from the analysis that you
9 performed.

10 There's -- you cite two figures from
11 Nakamura FIG. 4C, which I believe is the second
12 embodiment.

13 A. Uh-huh.

14 Q. And FIG. 5C, which is not the finished
15 product of the third embodiment, but part of the
16 third embodiment.

17 You have at the bottom there, in the
18 box you say:

19 "Modified third embodiment has better
20 depth of focus than second embodiment when --"

21 A. I'm sorry. You mean on page 13?

22 Q. On page 13. Yes.

1 There's a box there and inside the box
2 you say:

3 "Modified third embodiment has better
4 depth of focus than second embodiment when $X-T$ is
5 greater than T " and then in brackets you say "i.e.
6 when X is greater than $2T$."

7 In the figure, you have a certain
8 height in FIG. 4C which is labeled " $X-T$ " or maybe
9 it's X dash T , or whatever, and then in FIG. 5C you
10 have the figure and it's labeled a certain height
11 that's labeled " T ."

12 Do you see that?

13 A. Uh-huh.

14 Q. In those two figures, isn't $X-T$ equal
15 to T ? Isn't the height of $X-T$ in FIG. 4C equal to T
16 in FIG. 5C?

17 A. No, not necessarily. If you look back
18 to page 9, FIG. 4A, notice that X is defined as the
19 thickness of the layer 24.

20 Q. Uh-huh.

21 A. Plus whatever is remaining after
22 etchback or some kind of planarization to layer 26.

1 Q. Uh-huh.

2 A. And Nakamura doesn't tell us what that
3 number X is. So what it really means is that if X
4 is greater than $2T$ where T is -- remember, T is the
5 thickness of the layer 24, then there is an
6 advantage to the proposed embodiment 3 revision.

7 And I think that will be frequent
8 because 24 is very thin, and the etchback or
9 planarization to thin down 26 is from a much thicker
10 layer of material.

11 So I think there usually will be
12 advantages and planarity by adopting this modified
13 embodiment 3.

14 Q. Just looking at the figures that you
15 have annotated on page 13.

16 A. Yes.

17 Q. You've annotated one figure with $X-T$
18 and you annotated another figure with T ; right?

19 A. Yes.

20 Q. Those heights look the same to me.

21 Do they -- are they not the same?

22 A. No, they're not the same because we

1 don't know what X will be.

2 So if I'm the process engineer doing
3 this work, I have some recipe for thinning the BPSG
4 layer down, short of reaching the top of the nitride
5 layer -- layer, and depending on what that is will
6 determine whether there's a benefit and how much the
7 benefit is.

8 Q. Right. So you're saying there will be
9 a manage if $X-T$ is greater than T --

10 A. Yes.

11 Q. -- in a -- in a hypothetical world
12 where X is very large; correct?

13 A. Not very large. Large compared to T .

14 Q. Or more than -- more than $2T$?

15 A. Yeah, right.

16 Q. More than $2T$?

17 A. Right.

18 Q. All right. But specifically what's
19 shown in the figures that you've annotated; right?
20 Specifically what's shown in the figures, X isn't
21 greater than $2T$; correct?

22 A. Well, these -- these figures come from

1 the patent.

2 Q. Right.

3 A. Okay? And perhaps I should have drawn
4 my own version of the figures to make it clear, but
5 the math is right.

6 Q. Okay. So based on the figures that
7 come from the Nakamura patent, $X-T$ is not greater
8 than T , but mathematically what you're trying to
9 explain is something that you stand by?

10 A. I stand by it, with the addition of the
11 statement that I think in most cases if I were a
12 process engineer, or somebody was a process
13 engineer, etching back the BPSG layer or planarize
14 it in some way and I want to come -- I want to stop
15 someplace above the nitride layer 24, I doubt very
16 much I'm going to get down to a thickness equal to
17 the thin layer 24 dimension and so I think that this
18 condition will be met frequently.

19 Q. The figures from Nakamura do not show
20 $X-T$ being greater than T ; correct?

21 A. As drawn, they don't look very
22 different, no.

1 Q. Okay. Do you think that the figures in
2 Nakamura were drawn erroneously?

3 A. They were drawn to demonstrate certain
4 things in the patent. Like it's not erroneous, but
5 I don't think there was any particular reason to
6 decide what the thickness remaining of 26 would be
7 in making that -- that picture.

8 Q. They were not drawn to illustrate your
9 modified version of the third embodiment; correct?

10 A. That's correct.

11 Q. Because your modified version of the
12 third embodiment is not taught or disclosed in the
13 Nakamura reference; correct?

14 A. That's right.

15 Q. All right.

16 A. That's one that I think would have been
17 obvious.

18 Q. Okay. Looking at Exhibit 8, which is
19 the '244 patent.

20 A. Yes.

21 Q. And just looking at claim 1. This is
22 starting at column 6 line 27.

1 I believe you had previously testified
2 that -- in your prior deposition that all of the
3 steps that are listed in the claim should be
4 performed in order, other than the step which begins
5 with "removing a top portion of said fourth
6 dielectric layer" and the step that begins with
7 "forming on the substrate a patterned second resist
8 layer"; is that correct?

9 A. I don't think that's quite right.

10 Q. That's not right? Okay.

11 A. No. I -- I said that embodiment 1, for
12 example, will meet the claim limitations with the
13 reversal of those two in -- in the order that's
14 stated here, but I didn't say anything about not
15 changing the other ones.

16 Q. Okay.

17 A. Right. I mean, for that embodiment, I
18 don't change -- I wouldn't change them.

19 Q. And under your analysis the -- and this
20 relates to Nakamura embodiment 1 -- the -- the step
21 in Nakamura embodiment 1 that you believe satisfies
22 the "removing a top portion of said fourth

1 dielectric layer" is the contact hole etch step;
2 correct?

3 A. What do you mean by "contact hole etch
4 step"?

5 Q. The step where the contact hole etch is
6 being formed.

7 A. Well, there are sequence of activities
8 in opening up the contact hole, which is to remove a
9 top portion of the fourth dielectric layer and then
10 to expose and to remove the third dielectric layer
11 and get down to the substrate, form the sidewall and
12 so on.

13 Q. And it's that contact hole etch step
14 that you believe satisfies the step of "removing a
15 top portion of said fourth dielectric layer";
16 correct?

17 MR. COLAIANNI: Object. Outside
18 the scope of the reply declaration.

19 THE WITNESS: Well, are you
20 looking for me to walk through Nakamura first
21 embodiment reads on these claims? Is that what you
22 mean?

1 BY MR. CHEN:

2 Q. No, I don't want you to walk through
3 it.

4 I just wanted to confirm my
5 understanding of what you believe is the step in
6 Nakamura first embodiment that satisfies the
7 "removing a top portion of said fourth dielectric"
8 step in claim 1.

9 A. Well, in Nakamura embodiment 1, the
10 resist is in place. Okay? That's -- that's forming
11 a substrate patterned second resist. And then the
12 etch of the BPSG using that resist mask starts by
13 removing the top portion of the fourth dielectric
14 layer, and ultimately gets down to exposing the
15 portion of the third dielectric layer as the etching
16 front moves downward.

17 Q. Uh-huh.

18 A. I don't want to say because I don't
19 think it's right to say that that constitutes
20 opening the contacts. Because the phrase in the
21 claim "removing said fourth dielectric layer other
22 than said portion" etc., etc. leaves out things and

1 involves substeps, and it's important to recognize
2 that those -- those have to be there for this to
3 work.

4 Q. So the step that you just recited from
5 Nakamura, it's not the step that's used to open up
6 the contacts?

7 A. The clause about "removing said fourth
8 dielectric layer other than" is a requirement to be
9 able to open up the portions of the substrate, but
10 it's not everything that's going on there. It can't
11 be.

12 MR. CHEN: Okay. All right. Why
13 don't we take a break while I look through my notes.
14 I might have one or two short questions, and then I
15 should be done.

16 MR. COLAIANNI: Okay.

17 THE VIDEOGRAPHER: Going off the
18 record. The time is 16:47.

19 (Recess - 4:47 p.m. - 5:11 p.m.)

20 THE VIDEOGRAPHER: We are back on
21 the record. The time is 17:11.

22 MR. CHEN: Okay. I don't have any

1 further questions for Dr. Rubloff at this time.

2 MR. COLAIANNI: Okay. I just had,
3 hopefully, just one question on redirect.

4 REDIRECT EXAMINATION

5 BY MR. COLAIANNI:

6 Q. With respect to Exhibit 8, Dr. Rubloff,
7 which is the '244 patent.

8 A. Yeah.

9 Q. Could you explain what the purpose of
10 the layer 26 is in the '244 patent, as you
11 understand it?

12 A. (Reviewing document). 26. Yes. So
13 layer 26 is conformal CVD nitride, I believe. Let
14 me verify that.

15 Does it specify? Well, it -- let's
16 see. 26. (Reviewing document).

17 Well, it's a dielectric. It's
18 conformal over the gate and it's -- as you see in
19 FIG. 5, it remains protecting the gate on the
20 sidewall. When material 34 that is the polysilicon
21 that will ultimately allow the formation of the
22 raised source/drain by diffusion of impurities into

1 the substrate, it prevents that raised source/drain
2 structure from shorting to the gate electrode of the
3 transistor.

4 So it's essentially a spacer, a
5 sidewall spacer.

6 Q. Is it -- strike that.

7 Is layer 26 performing any role as an
8 etch stop?

9 A. Yes. It's an etch stop in between FIG.
10 4 and FIG. 5. So that when in FIG. 4 the resist
11 mask 30 is used to allow the BPSG or whatever the
12 dielectric 28 is to be removed, there's a place to
13 stop on that as an etch stop. So it really serves
14 as part of the self-alignment structure that
15 benefits the raised source/drain.

16 MR. COLAIANNI: Okay. Thank you.

17 Nothing further.

18 THE VIDEOGRAPHER: Good. Okay.

19 We are going off the record. The time is now 17:15.

20 (Signature having not been waived,
21 the taking of the deposition concluded at 5:15 p.m.)

22 * * *

CERTIFICATE OF COURT REPORTER

UNITED STATES OF AMERICA)

DISTRICT OF COLUMBIA)

I, DENISE D. VICKERY, the reporter before
whom the foregoing deposition was taken, do
hereby certify that the witness whose testimony
appears in the foregoing deposition was sworn by me;
that the testimony of said witness was taken by me
in machine shorthand and thereafter transcribed by
computer-aided transcription; that said deposition
is a true record of the testimony given by said
witness; that I am neither counsel for, related to,
nor employed by any of the parties to the action in
which this deposition was taken; and, further, that
I am not a relative or employee of any attorney or
counsel employed by the parties hereto, or
financially or otherwise interested in the outcome
of this action.

Denise D. Vickery

Notary Public in and for the
District of Columbia

My Commission expires February 14, 2018

DEPOSITION ERRATA SHEET

Our Assignment No. J0254984

Case Caption: SAMSUNG ELECTRONICS CO. LTD. vs. HOME
SEMICONDUCTOR CORPORATION

DECLARATION UNDER PENALTY OF PERJURY

I declare under penalty of perjury
that I have read the entire transcript of
my Deposition taken in the captioned matter
or the same has been read to me, and
the same is true and accurate, save and
except for changes and/or corrections, if
any, as indicated by me on the DEPOSITION
ERRATA SHEET hereof, with the understanding
that I offer these changes as if still under
oath.

Signed on the _____ day of
_____, 2015.

GARY W. RUBLOFF, PH.D.

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