

IPR2015-00460: PATENT NO. 6,146,997 ('997 PATENT)

Claim Construction

Disputed Terms

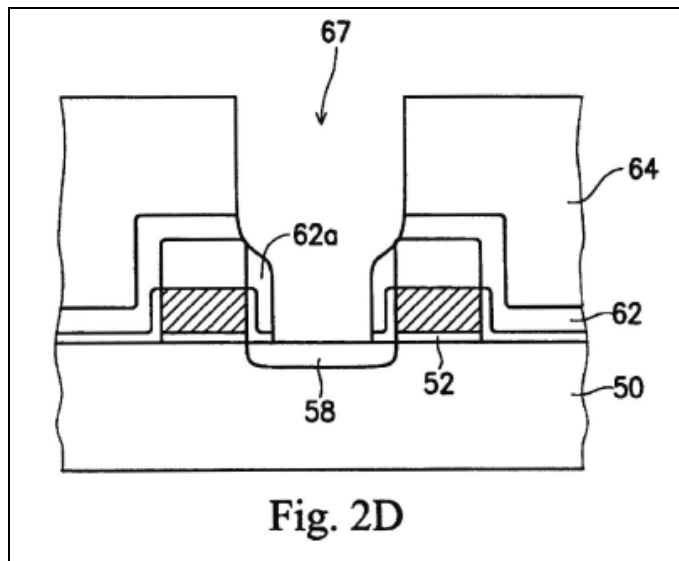
- “spacer” (claims 1 and 9)
- “forming an oxide layer over the diffusion region” (claims 2 and 9)

“Spacer”

Term: “spacer” (claims 1 and 9)

Home Semiconductor’s Construction	Samsung’s Construction
“structure designed to create[] physical separation between conducting structures.” Response (Paper 18) at p. 7.	“a structure that spaces between two conductive structures.” Petition (Paper 1) at p. 10.

“Spacer”



'997 Patent , Fig. 2D.

“Further, the same nitride layers anisotropically etched to form sidewall spacers that prevent shorting between the gate electrode and the conductive plug.”

'997 Patent at Col. 3:35-38.

“Over”

Term: “forming an oxide layer **over** the diffusion region”

Home Semiconductor’s Construction	Samsung’s Construction
“forming an oxide layer covering the diffusion region.” Response (Paper 18) at p. 8.	“forming an oxide layer above the diffusion region.” Petition (Paper 1) at p. 9.

Specification Uses “Over” To Refer To Covering

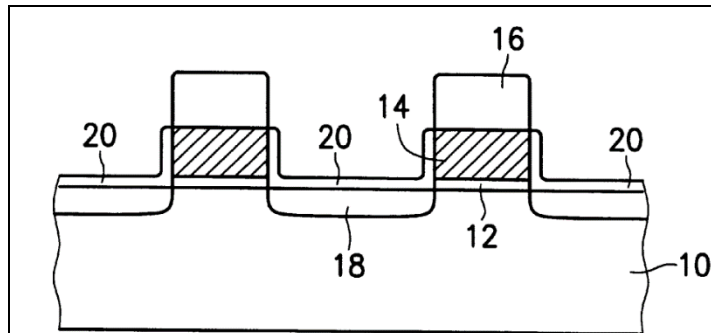


Fig. 1A (Prior Art)

“Next, a thin oxide layer 20 is formed over the substrate surface”

’997 Patent at Col. 3:29-31, Fig. 1A.

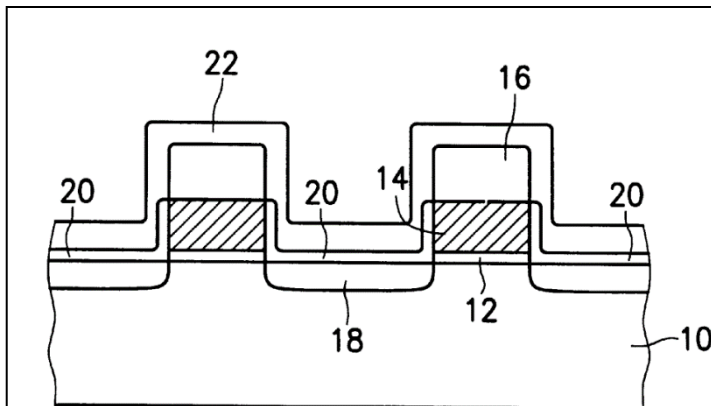
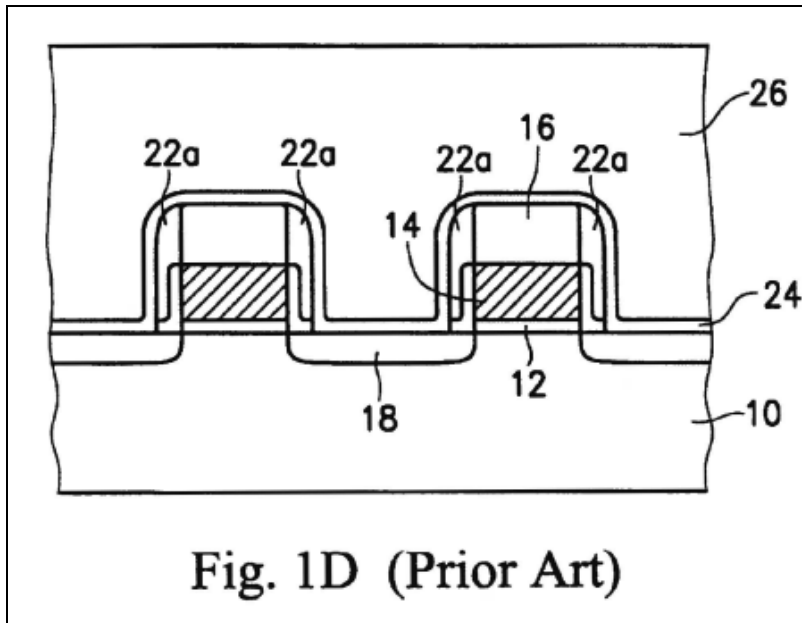


Fig. 1B (Prior Art)

“Referring to FIG. 1B, a conformal layer of silicon nitride 22 having a thickness of about 100 to 600 Å is deposited over the substrate surface[.]”

’997 Patent at Col. 1:32-34, Fig. 1B.

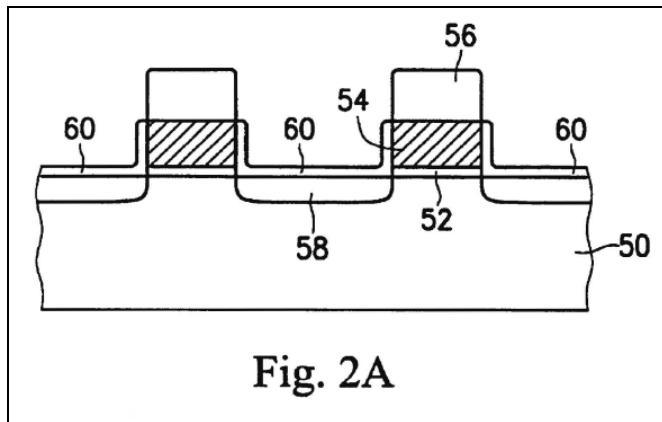
Specification Uses “Over” To Refer To Covering



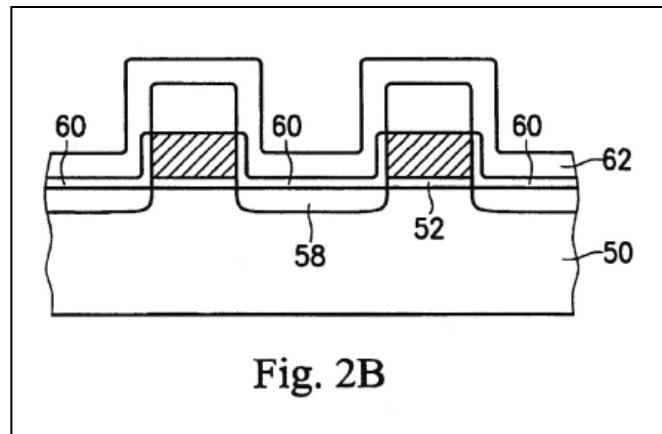
“Referring to FIG. 1D, a conformal layer of etch barrier material 24 is deposited over the diffusion region 18, the cap layers 16, and the sidewall spacers 22a. . . . A layer of insulator 26 is deposited over the substrate as inter-layer dielectric (ILD)[.]”

’997 Patent at Col. 1:41-46.

Specification Uses “Over” To Refer To Covering

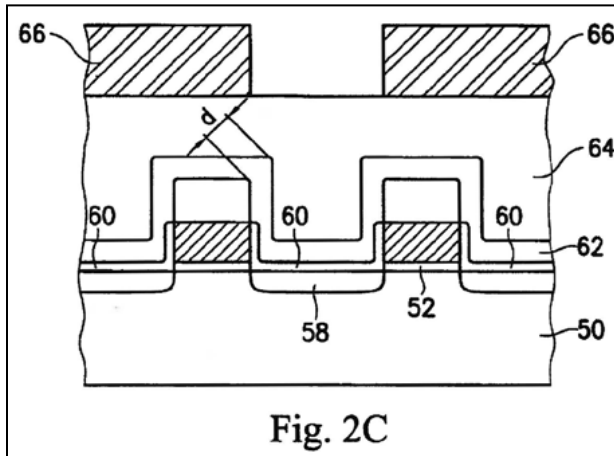


“[A] thin oxide layer 60 having a thickness of about 150 Å is formed over the substrate surface[.]”
’997 Patent at Col. 2:55-57, Fig. 2A.



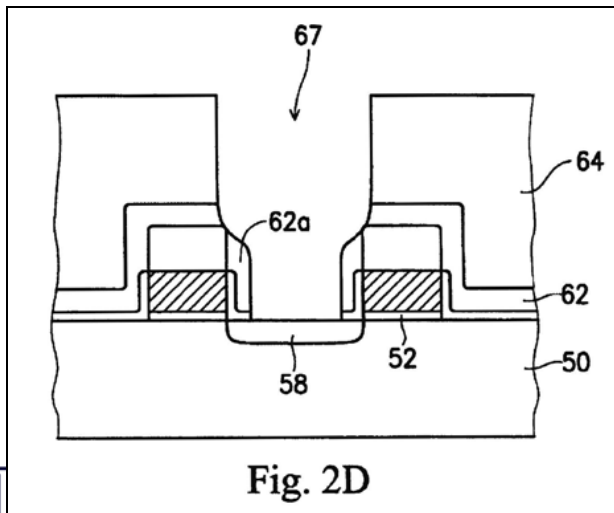
“Referring to FIG. 2B, a conformal layer of silicon nitride 62 is deposited over the substrate surface using low pressure chemical vapor deposition (LPCVD).”
’997 Patent at Col. 2:60-62, Fig. 2B.

Specification Uses “Over” To Refer To Covering



“Referring to FIG. 2C, a layer of insulator 64 is deposited over the substrate as inter-layer dielectric (ILD).”

’997 Patent at Col. 3:1-2, Fig. 2C.



“[T]he conformal nitride layer 62 underneath the opening is anisotropically etched to remove the portion over the diffusion region 58.”

’997 Patent at Col. 3:17-20, Fig. 2D.

Doshi Does Not Teach Simultaneous Formation of Spacer

“anisotropically etching the [barrier/silicon nitride] layer underneath the opening, thereby exposing the diffusion region **and simultaneously forming a spacer of [the etch barrier material/silicon nitride] on the sidewall of the gate electrode.**”

’997 Patent at Col. 4:1-4; 4:44-47.

Specification Teaches That Nitride Layer Is Removed From Within Contact Hole Locations

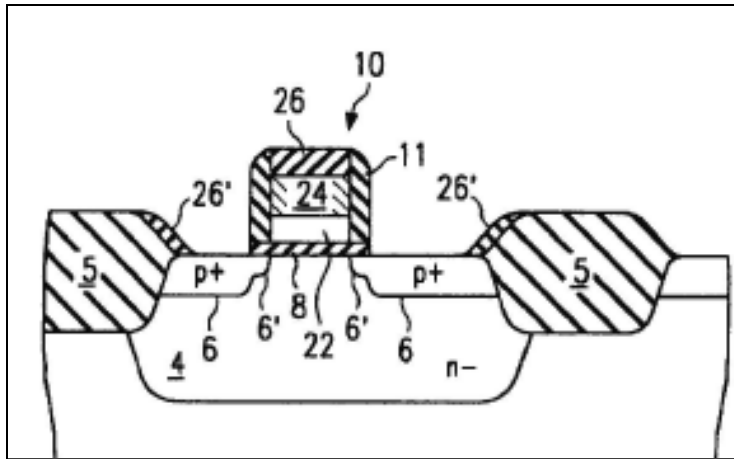
“[T]he brief nitride etch used to **clear nitride layer 30 from within plug contact locations PC** has been observed to be highly anisotropic[.]”

Doshi at Col. 10:11-13.

“The second step of the two-step etch is then performed **to remove nitride layer 30 from bit line contact location BLC.**”

Doshi at Col. 10:62-63.

When Doshi Forms Spacers, Doshi Is Explicit



Doshi, Fig. 3a.

“According to the preferred embodiment of the invention, sidewall filaments 11 are formed by first oxidizing the sides of polysilicon layer 22. A layer of silicon nitride is then deposited overall, and then etched anisotropically to remove the nitride from flat surfaces, **leaving sidewall filaments 11 behind**. As noted above, silicon nitride residue 26' may remain along the sides of field oxide structures 5, as these structures also extend above the surface of substrate 2 and have slight sidewalls.”

Doshi at Col. 7:57-65.

When Doshi Forms Spacers, Doshi Is Explicit

“Q. No. Column 7 beginning at lines 57 is describing the formation of the sidewall filaments --

A. Right. Right.

Q. -- that we agree are spacers; correct? And when it's -- when Doshi is describing the formation of the sidewall filaments, it is explicitly stating that the etching of the nitride material would leave that nitride material on the sidewalls to form the sidewall filaments; correct?

A. Yes.

Q. It explicitly states that material is left behind on the sidewalls in this case; correct?

A. Yes.”

Rubloff Reply Cross Tr. at 115:16-116:8.

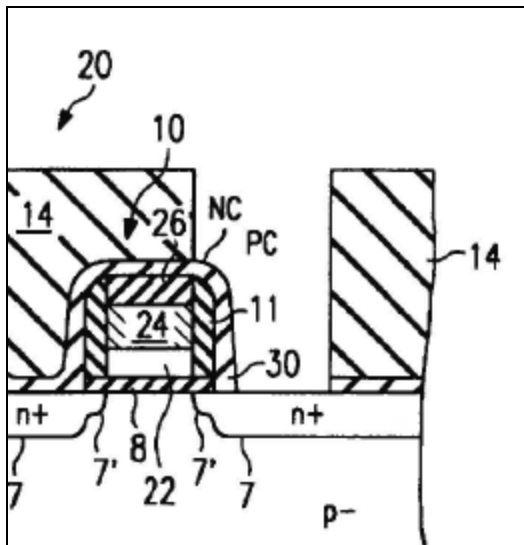
When Doshi Forms Spacers, Doshi Is Explicit

“Q. Right. Right. Doshi -- but when Doshi is describing the nitride etch for the plug contacts or the bit-line contacts, which are described at column 9 beginning at line 56 for the plug contact and column 10 line 63 for the bit-line contact, Doshi does not explicitly state that after the nitride etch material is left behind on the sidewalls of the gate; correct?”

A. (Reviewing document). Yes, I think that's correct. It's not explicit here.”

Rubloff Reply Cross Tr. at 119:1-11.

Fig. 3g Has Errors According to Dr. Rubloff



Doshi, Fig. 3g.

“I noticed that the corner of the silicon nitride layer 30, which is exposed to the silicon nitride dry etch, is not shown as etched in Fig. 3g. **I believe this is a mistake in Fig. 3g**, as an anisotropic etch of silicon nitride would have removed the same thickness of the silicon nitride covering the diffusion region and the silicon nitride at the corner.”

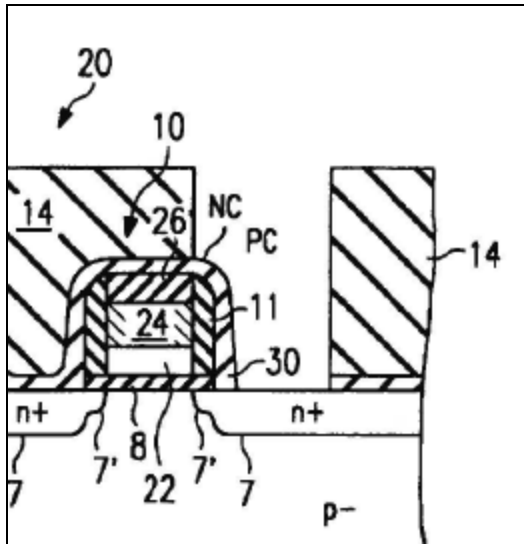
Rubloff Decl. at ¶ A-14.

“Q. And then you mention that you found an error in Figure 3g; correct?

A. **Yes. I think it was a little misleading.** I would have expected to see -- what page do I have this on? Yeah, on page 37. I would have expected to see some of the top nitride etched away there.”

Rubloff Cross Tr. at 203:11-204:17.

Fig. 3g Has Errors – Mr. Maltiel Agrees

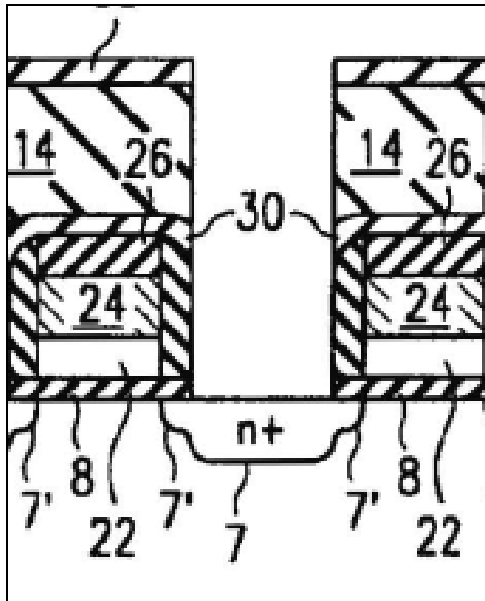


Doshi, Fig. 3g.

“The error isn’t just confined to just the top corner. The nitride etch process designed to clear the nitride layer 30 would etch other portions of layer 30 exposed under the contact opening. Oddly, Fig. 3g shows the portion of nitride layer 30 covering the gate as completely unaffected by this etch process. This is an undeniable error.”

Maltiel Decl. at ¶ 67.

Fig. 3k Is Reliable And Shows Nitride Layer Removed



Doshi, Fig. 3k.

“When depicting the BLC etch in Fig. 3k, Doshi shows the entire exposed portion of nitride layer 30 removed from the BLC contact location.”

Maltiel Decl. at ¶ 68.

“This result is both expected and consistent with how Doshi describes the nitride etch process. Doshi at Col. 10:63-64 (“The second step of the two-step etch is then performed to remove nitride layer 30 from bit line contact location BLC.”). There is no indication that Fig. 3k’s depiction of the etch process in the BLC location is erroneous or unreliable.”

Maltiel Decl. at ¶ 69.

Doshi Fig. 3g and 3k Nitride Etches Are Identical

“The second step of the two-step etch is then performed, to remove nitride layer 30 from bit line contact location BLC. **This second step is substantially identical to that performed in the two-step etch of plug contact locations PC**, which is a relatively brief etch under similar pressure, power, and temperature conditions as the first etch step. As before, the active species in this second step of the two-step etch preferably include CHF₃ at 50 sccm ($\pm 10\%$) in combination with CO at 175 seem ($\pm 10\%$). This second step is also preferably a timed etch, having a duration of on the order of 10 seconds. FIG. 3k illustrates integrated circuit 20 after the completion of the two-step etch of BPSG layer 14 and nitride layer 30, showing the clearing of the surface of source/drain region 7 within bit line contact opening BLC.”

Doshi at Cols. 10:63-11:10.

Dr. Rubloff Now Claims He Noticed Errors First Time He Saw Fig. 3k

“And when I first studied this patent, I remember thinking, what on earth is wrong here? This doesn't make any sense. They're doing the same thing. It should look -- you know, usually when you do the same set of things, you get the same result.”

Rubloff Reply Cross Tr. at 92:19-93:4.

“Q. You noticed that when you first studied the patent?

A. Yeah, I remember this. I said maybe I won't have to worry about the bit-line contact because maybe the issue is all the plug contact, and I said I don't know. I don't have to worry. Until they tell me that -- that I need to worry about it, then I'll just ignore it, but it looked wrong.”

Rubloff Reply Cross Tr. at 93:5-12.

When Asked, Dr. Rubloff Did Not Mention Errors In Fig. 3k In First Deposition

“Q. My question was simply that whether you had provided any opinions about the formation of the bit line contact opening.

A. No, I don't think so.

Q. Okay. And so you don't have an opinion as to whether the formation of the bit line contact opening is the same -- or you don't have any opinions as to whether the process used to form the bit line contact openings is the same as the process used to form the plug contact openings; correct?

A. I have not looked at the description of the bit line contact etch. I read it, but I didn't pay a lot of attention to it.”

Rubloff Cross Tr. at 211:21-212:11.

“Q. Are there other errors in the depiction of the etching of nitride layer 30 in the figures of the Doshi reference?

[. . .]

A. It's possible, but I don't know of any. I mean, we could argue – I think it's difficult. We could argue about exactly what the sidewall profile would look like after the nitride is etched to form the sidewall – sidewall spacer, and that has to do with how anisotropic the etch is and so on there. We could quibble about these details, but I know how these drawings are made. They're made by a draftsman who gets a sketch and tries to make it right, and they're not always accurate.”

Rubloff Cross Tr. at 209:8-210:1.

Doshi Would Include Overetch

“Q. And so --

A. -- in part.

Q. -- when designing the etch to remove the nitride layer, you would design in some amount of overetch to ensure that the nitride material is removed; correct?

A. Yes, that's likely.”

Rubloff Reply Cross Tr. at 86:20- 87:4.

“Q. With a selective nitride etch, the intention is for the etching to stop on the silicon surface; correct?

A. Yes.

Q. So that even if you designed in a degree of overetch to make sure you cleared all the nitride material from the contact, you would not materially damage the silicon surface; correct?

A. That's certainly the goal.”

Rubloff Reply Cross Tr. at 153:13-21.

BPSG Etch Would Etch Nitride Sidewalls

“Moreover, even though the nitride etch is anisotropic, it would still be able to clear a thin layer like nitride layer 30. First, some of the nitride layer would already be removed during the initial oxide etch.”

Maltiel Decl. at ¶ 71.

“Q. But it would be fair to say that the portion of nitride layer 30 near the top of the gate would be etched more than portions of nitride layer 30 closer to the bottom of the gate just because they're exposed to the etching environment for longer period of time; correct?

A. For the BPSG etch, yes.”

Rubloff Reply Cross Tr. at 1132:18-133:2.

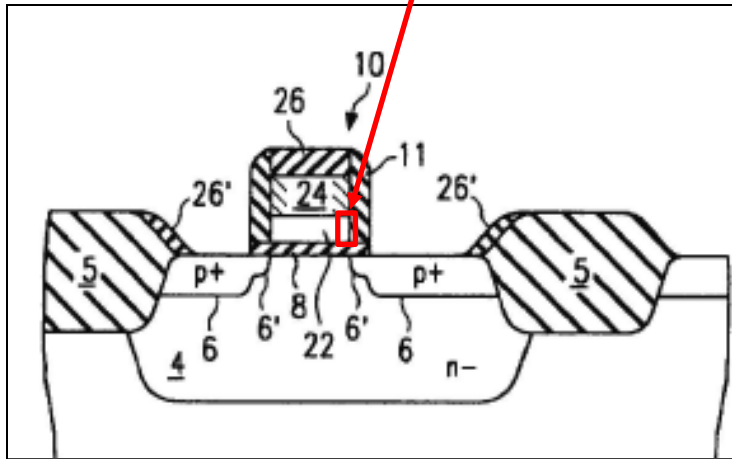
Doshi Does Not Anticipate Claims 2 and 9

2. The method as claimed in claim 1, further comprising a step of forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode by thermal oxidation prior to forming the barrier layer.

9. A method for forming a self-aligned contact hole, comprising the steps of:
[. . .]
(b) forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode by thermal oxidation;
[. . .]

Doshi Does Not Teach Forming An Oxide Over Diffusion Region

Oxidized sides of polysilicon layer 22

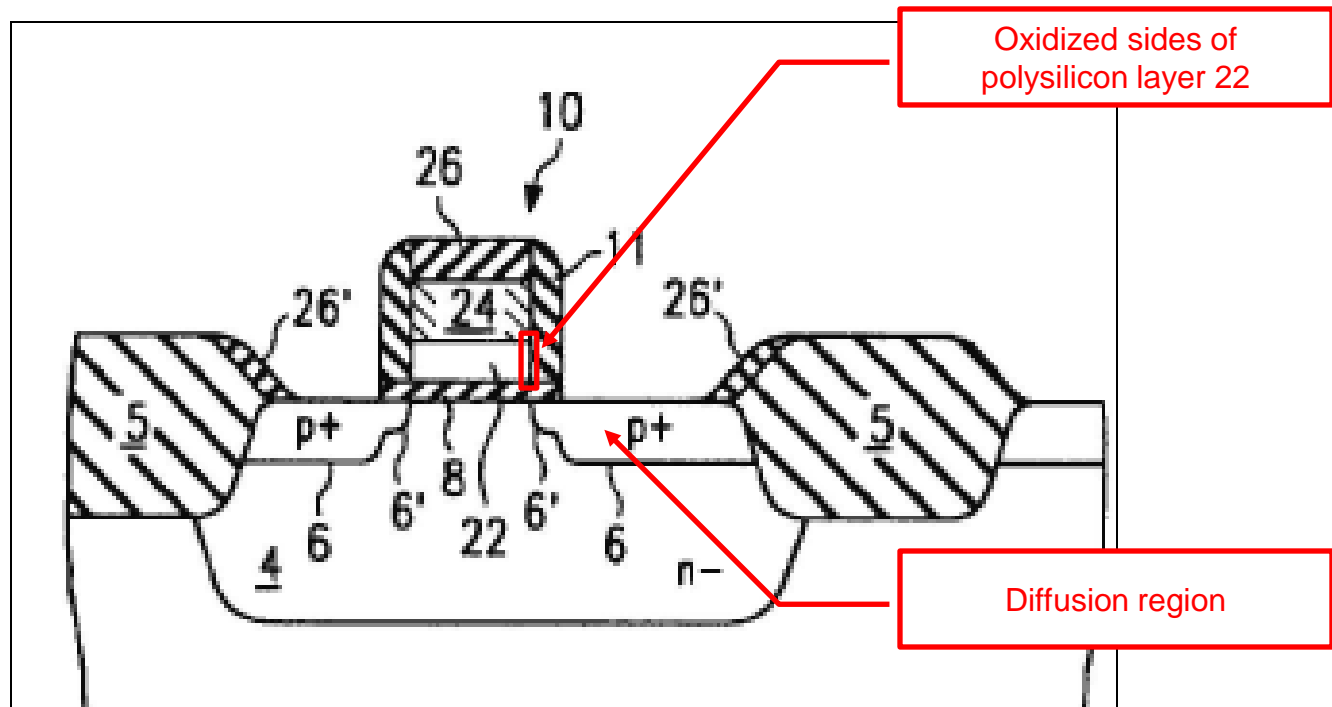


Doshi, Fig. 3a.

“According to the preferred embodiment of the invention sidewall filaments 11 are formed by first oxidizing the sides of the polysilicon layer 22.”

Doshi at Col. 7:57-59.

Oxidized Polysilicon Layer 22 Not “Over” Diffusion Region



Doshi, Fig. 3a.

Samsung Argues Oxide Formed Because Diffusion Regions Are Uncovered Silicon

“Although **not expressly disclosed in Doshi**, during the thermal oxidation of the sides of polysilicon layer 22, thermal oxide is also formed over the source/drain regions **because the source/drain regions are uncovered doped silicon**, which is susceptible to thermal oxidation.”

Petition (Paper 1) at p. 29.

“Notably, however, Petitioner has established that, during the thermal oxidation of the sides of polysilicon layer 22, thermal oxide is grown over the source/drain regions **because the source/drain regions are uncovered doped silicon**, which is susceptible to thermal oxidation.”

Petition Reply (Paper 21) at p. 24.

Doshi Diffusion Region Is Not Uncovered Silicon

“In Doshi, the diffusion region is not uncovered doped silicon during the oxidation step. That area, the source/drain regions, is covered by the gate oxide layer 8 which is not removed until after the oxidation process.”

Maltiel Decl. at ¶¶ 81-82.

“Q. So what Doshi shows is that during the formation of the sidewall filaments, the source/drain regions or the diffusion regions are still covered by gate oxide layer 8; correct?

A. Yes. I had -- I had forgotten that.”

Rubloff Reply Cross Tr. at 155:15-157:1.